Date: Feb. 3, 2017

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A074A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/I1D Descriptions in the Hardware User's Manual Rev. 2.10 Changed		Information Category	Technical Notification		
Applicable Product	RL78/I1D Group	Lot No. All lots	Reference Document	RL78/I1D User's Manual: Hardware Rev.2.10 R01UH0474EJ0210 (Jan. 2016)		

This document describes misstatements found in the RL78/I1D User's Manual: Hardware Rev.2.10 (R01UH0474EJ0210).

Corrections

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1.6 Outline of Functions	p.4	Incorrect descriptions revised
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Corrections in the User's Manual: Hardware

No	Corrections and Applicable Items			Pages in this document for corrections
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5	8.3.3 Subsystem clock supply mode control register(OSMC) 9.3.2 Subsystem clock supply mode control register(OSMC) 10.3.3Subsystem clock supply mode control register(OSMC)		p.291, p.323, p.333	p.7～p.9
6	12.5 Cautions of clock output/buzzer output controller		p.358	p.10
7	14.10 Cautions for A/D Converter		p.421	p.11
8	17.3.14 Serial output level register m(SOLm) Figure17-20 Examples of Reverse Transmit Data		p.486	p.12
9	17.5.7 SNOOZE mode function		p.541	p.13
10	19.5.7 DTC Activation Sources		p.669	p.14
11	20.3.1 Event output destination select register n(ELSELRn)(n=00 to 19)		p.673	p.15
12	34.3.2 Supply current characteristics		p.861	p.16
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Incorrect: Bold with underline; Correct: Gray hatched

Revision History

RL78/I1D User's Manual: Hardware Rev.2.10 Correction for Incorrect Description Notice

Document Number	Date	Description
TN-RL*- A074A/E	Feb. 3, 2017	First edition issued No.1 to No.13 incorrect descriptions revised

1. 1.3.4 32-pin products(p.10)

Old)

(omitted)

・32-pin plastic LQFP(7×7mm,**0.5**mm pitch)

(omitted)

New)

(omitted)

・32-pin plastic LQFP(7×7mm,0.8mm pitch)

(omitted)

2. 1.6 Outline of Funcations(p.14)

Incorrect)

(omitted)

Main system clock	High-speed system clock(f_{MX})	X1(crystal/ceramic) oscillation, external system clock input (EXCLK) 1～20MHz:VDD=2.7～3.6V,1～8MHz:VDD=1.8～2.7V,1～4MHz:VDD=1.6～1.8V
	High-speed on-chip oscillator clock (f_{IH})MAX:4MHz	HS(High-speed main)mode：1～24MHz(VDD=2.7～3.6V) HS(High-speed main)mode：1～16MHz(VDD=2.4～3.6V) LS(Low-speed main)mode：1～8MHz(VDD=1.8～3.6V) LV(Low-speed main)mode：1～4MHz(VDD=1.6～3.6V) LP(Low-speed main)mode：1MHz(VDD=1.8～3.6V)
	Middle-speed on-chip oscillator clock (f_{IM})Max:4MHz	

(omitted)

Correct)

(omitted)

Main system clock	High-speed system clock(f_{MX})	X1(crystal/ceramic) oscillation, external system clock input (EXCLK) HS(High-speed main)mode：1～24MHz(VDD=2.7～3.6V) HS(High-speed main)mode：1～16MHz(VDD=2.4～3.6V) LS(Low-speed main)mode：1～8MHz(VDD=1.8～3.6V) LV(Low-speed main)mode：1～4MHz(VDD=1.6～3.6V) LP(Low-speed main)mode：1MHz(VDD=1.8～3.6V)
	High-speed on-chip oscillator clock (f_{IH})MAX:4MHz	HS(High-speed main)mode：1～24MHz(VDD=2.7～3.6V) HS(High-speed main)mode：1～16MHz(VDD=2.4～3.6V) LS(Low-speed main)mode：1～8MHz(VDD=1.8～3.6V) LV(Low-speed main)mode：1～4MHz(VDD=1.6～3.6V) LP(Low-speed main)mode：1MHz(VDD=1.8～3.6V)
	Middle-speed on-chip oscillator clock (f_{IM})Max:4MHz	

(omitted)

3. 6.3.8 Subsystem clock supply mode control register(OSMC)(p.149)
Figure6-11 Format of Subsystem clock supply mode control register(OSMC)

Incorrect)

Figure6-11 Format of Subsystem clock supply mode control register(OSMC)

Address：F00F3H After reset：00H R/W[Note1]

Symbol	7	6	5	4	3	2	1	0
OSMC	RTCLPC	0	0	WUTMMCK0	0	0	0	0

(omitted)

Correct)

Figure6-11 Format of Subsystem clock supply mode control register(OSMC)

Address：F00F3H After reset：indefinite R/W[Note1]

Symbol	7	6	5	4	3	2	1	0
OSMC	RTCLPC	0	0	WUTMMCK0	×	×	0	0

(omitted)

Remark. ×：indefinite

4. 6.6.3 Example of setting XT1 oscillation clock(p.164)

Incorrect)

(omitted)

<1>To run only the real-time clock 2 and 12-bit interval timer on the subsystem clock (ultra-low current consumption) when in the STOP mode or **sub-HALT mode**, set the RTCLPC bit to 1.

	7	6	5	4	3	2	1	0
OSMC	RTCLPC 0/1	0	0	WUTMMCK0 0	**0**	**0**	0	0

(omitted)

Correct)

(omitted)

<1>To run only the real-time clock 2 and 12-bit interval timer on the subsystem clock (ultra-low current consumption) when in the STOP mode or HALT mode of CPU operation at sub-system clock, set the RTCLPC bit to 1.

	7	6	5	4	3	2	1	0
OSMC	RTCLPC 0/1	0	0	WUTMMCK0 0	×	×	0	0

(omitted)

Remark. ×：indefinite

5. 8.3.3 Subsystem clock supply mode control register(OSMC)(p.291)
Figure8-4 Format of Subsystem clock supply mode control register(OSMC)

Incorrect)

Figure8-4 Format of Subsystem clock supply mode control register(OSMC)

Address：F00F3H After reset：00H R/W[Note1]

Symbol	7	6	5	4	3	2	1	0
OSMC	RTCLPC	0	0	WUTMMCK0	0	0	0	0

(omitted)

Correct)

Figure8-4 Format of Subsystem clock supply mode control register(OSMC)

Address：F00F3H After reset：indefinite R/W[Note1]

Symbol	7	6	5	4	3	2	1	0
OSMC	RTCLPC	0	0	WUTMMCK0	×	×	0	0

(omitted)

Remark. ×：indefinite

9.3.2 Subsystem clock supply mode control register(OSMC)(p.323)

Figure9-3 Format of Subsystem clock supply mode control register(OSMC)

Incorrect)

Figure9-3 Format of Subsystem clock supply mode control register(OSMC)

Address：F00F3H After reset：00H R/W[Note1]

Symbol	7	6	5	4	3	2	1	0
OSMC	RTCLPC	0	0	WUTMMCK0	0	0	0	0

(omitted)

Correct)

Figure9-3 Format of Subsystem clock supply mode control register(OSMC)

Address：F00F3H After reset：indefinite R/W[Note1]

Symbol	7	6	5	4	3	2	1	0
OSMC	RTCLPC	0	0	WUTMMCK0	×	×	0	0

(omitted)

Remark. ×：indefinite

10.3.3 Subsystem clock supply mode control register(OSMC)(p.333)

Figure10-4 Format of Subsystem clock supply mode control register(OSMC)

Incorrect)

Figure10-4 Format of Subsystem clock supply mode control register(OSMC)

Address：F00F3H After reset：00H R/W[Note1]

Symbol	7	6	5	4	3	2	1	0
OSMC	RTCLPC	0	0	WUTMMCK0	0	0	0	0

(omitted)

Correct)

Figure10-4 Format of Subsystem clock supply mode control register(OSMC)

Address：F00F3H After reset：indefinite R/W[Note1]

Symbol	7	6	5	4	3	2	1	0
OSMC	RTCLPC	0	0	WUTMMCK0	×	×	0	0

(omitted)

Remark. ×：indefinite

6. 12.5 Cautions of clock output/buzzer output controller(p.358)

Incorrect)

12.5 Cautions of clock output/buzzer output controller

When the main system clock is selected for the PCLBUZn output (CSELn=0),if **STOP or HALT** mode is entered within 1.5 clock cycles output from the PCLBUZn pin after the output is disabled(PCLOEn=0),the PCLBUZn output width becomes shorter.

Correct)

12.5 Cautions of clock output/buzzer output controller

When the main system clock is selected for the PCLBUZn output (CSELn=0),if STOP mode is entered within 1.5 clock cycles output from the PCLBUZn pin after the output is disabled(PCLOEn=0),the PCLBUZn output width becomes shorter.

7. 14.10 Cautions for A/D Converter(p.421)

Incorrect)

(omitted)

(2)Input range of ANI0 to ANI13 and ANI16 to ANI18 pins

Observe the rated range of the ANI0 to ANI13 and ANI16 to ANI18 pins input voltage. **If a voltage of AVDD and AVREFP or higher and AVSS and AVREFM or lower**(even in the range of absolute maximum ratings)is input to an analog input channel, the converted value of that channel becomes undefined. In addition, the converted values of the other channels may also be affected.

When internal reference voltage(1.45V) is selected reference voltage source for the + side of the A/D converter, do not input internal reference voltage(1.45V) **or higher** voltage to a pin selected by the ADS register. However, it is no problem that a pin not selected by the ADS register is input voltage **greater** than the internal reference voltage(1.45V).

(omitted)

Correct)

(omitted)

(2)Input range of ANI0 to ANI13 and ANI16 to ANI18 pins

Observe the rated range of the ANI0 to ANI13 and ANI16 to ANI18 pins input voltage. If the supply voltage that is over the voltage of AVDD and AVREFP and or less the voltage of AVSS and AVREFM (even in the range of absolute maximum ratings)is input to an analog input channel, the converted value of that channel becomes undefined. In addition, the converted values of the other channels may also be affected.

When internal reference voltage(1.45V) is selected reference voltage source for the + side of the A/D converter, do not input internal reference voltage(1.45V) more than voltage to a pin selected by the ADS register. However, it is no problem that a pin not selected by the ADS register is input voltage over the internal reference voltage(1.45V).

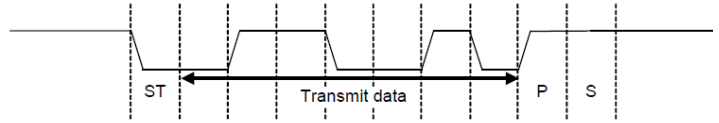
(omitted)

8. 17.3.14 Serial output level register m(SOLm)(p.486)
Figure17-20 Examples of Reverse Transmit Data

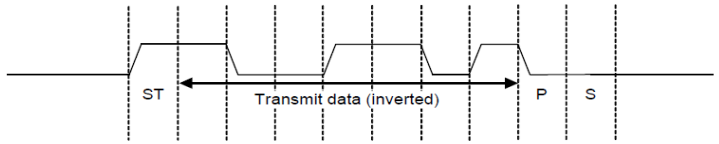
Incorrect)

Figure17-20 Examples of Reverse Transmit Data

(a) Non-reverse Output(SOLmn=0)



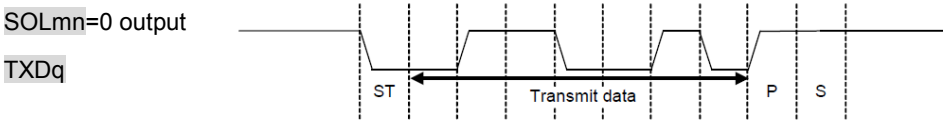
(b) Reverse Output(SOLmn=1)



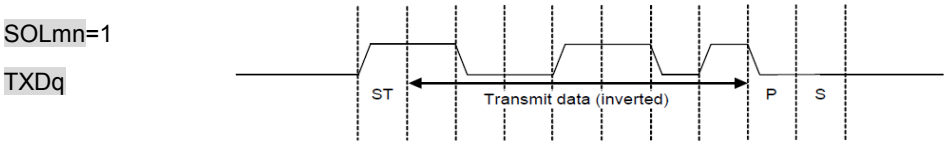
Correct)

Figure17-20 Examples of Reverse Transmit Data

(a) Non-reverse Output(SOLmn=0)



(b) Reverse Output(SOLmn=1)



9. 17.5.7 SNOOZE mode function(p.541)

Incorrect)

(omitted)

When using the SNOOZE mode function, set the SWCm bit of serial standby control register m(SSCm) to 1 just before switching to the STOP mode. After the initial setting has been completed, set the **SSm1** bit of serial channel start register m (SSm) to 1.

After a transition to the STOP mode, the CSI starts reception operations upon detection of an edge of the SCKp pin.

(omitted)

Correct)

(omitted)

When using the SNOOZE mode function, set the SWCm bit of serial standby control register m(SSCm) to 1 just before switching to the STOP mode. After the initial setting has been completed, set the SSm0 bit of serial channel start register m (SSm) to 1.

After a transition to the STOP mode, if an edge of the SCKp pin is detected, transition to the SNOOZE mode.

CSIp starts reception operations by the serial clock input of SCKp pin.

(omitted)

10. 19.5.7 DTC Activation Sources(p.669)

Incorrect)

・After inputting a DTC activation source, do not input the same activation source again until DTC transfer is completed.

・While a DTC activation source is generated, do not manipulate the DTC activation enable bit corresponding to the source.

・If DTC activation sources conflict, their priority levels are determined in order to select the for activation when the CPU acknowledges the DTC transfer. For details on the priority levels of activation sources, refer to **19.3.3 Vector Table**.

(omitted)

Correct)

・After inputting a DTC activation source, do not input the same activation source again until DTC transfer is completed.

・While a DTC activation source is generated, do not manipulate the DTC activation enable bit corresponding to the source.

・Selecting 8 bit interrupt timer or 12 bit interrupt timer In DTC activation sources, when DTC is retransferred after DTC transfer is completed, 1 clock of every timer action clock set 1 at register DTCENi(i=0~2)(activation enable).

・If DTC activation sources conflict, their priority levels are determined in order to select the for activation when the CPU acknowledges the DTC transfer. For details on the priority levels of activation sources, refer to **19.3.3 Vector Table**.

(omitted)

11. 20.3.1 Event output destination select register n (ELSELRn)(n=00 to 19)(p.673)

Incorrect)

(omitted)

Set an ELSELRn register during a period when no event output peripheral functions are generating event signals.

(omitted)

Correct)

(omitted)

Set an ELSELRn register during a period when no event output peripheral functions are generating event signals and event output destination (event receive side) function is stopping.

(omitted)

12. 34.3.2 Supply current characteristics(p.861)

Incorrect)

(T_A = -40 to +85°C, 1.6 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V)
(T_A = +85 to +105°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V) (1/4)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) mode	f_{IH} = 24 MHz Note 3, T_A = -40 to +105°C	Basic operation	V_{DD} = 3.0 V		1.4		mA
			HS (high-speed main) mode	f_{IH} = 24 MHz Note 3, T_A = -40 to +85°C	Normal operation	V_{DD} = 3.0 V		3.2	6.3	mA
				f_{IH} = 24 MHz Note 3, T_A = +85 to +105°C	Normal operation	V_{DD} = 3.0 V			6.7	
				f_{IH} = 16 MHz Note 3, T_A = -40 to +85°C	Normal operation	V_{DD} = 3.0 V		2.4	4.6	
				f_{IH} = 16 MHz Note 3, T_A = +85 to +105°C	Normal operation	V_{DD} = 3.0 V			4.9	
			LS (low-speed main) mode (MCSEL = 0)	f_{IH} = 8 MHz Note 3, T_A = -40 to +85°C	Normal operation	V_{DD} = 3.0 V		1.1	2.0	mA
						V_{DD} = 2.0 V		1.1	2.0	
			LS (low-speed main) mode (MCSEL = 1)	f_{IH} = 4 MHz Note 3, T_A = -40 to +85°C	Normal operation	V_{DD} = 3.0 V		0.72	1.30	mA
						V_{DD} = 2.0 V		0.72	1.30	
				f_{IM} = 4 MHz Note 7, T_A = -40 to +85°C	Normal operation	V_{DD} = 3.3 V		0.58	1.10	
						V_{DD} = 3.0 V		0.58	1.10	
			LV (low-voltage main) mode	f_{IH} = 4 MHz Note 3, T_A = -40 to +85°C	Normal operation	V_{DD} = 3.0 V		1.2	1.8	mA
						V_{DD} = 2.0 V		1.2	1.8	

(omitted)

Correct)

(T_A = -40 to +85°C, 1.6 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V)
(T_A = +85 to +105°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V) (1/4)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) mode	f_{IH} = 24 MHz Note 3, T_A = -40 to +105°C	Basic operation	V_{DD} = 3.0 V		1.4		mA
			HS (high-speed main) mode	f_{IH} = 24 MHz Note 3, T_A = -40 to +85°C	Normal operation	V_{DD} = 3.0 V		3.2	6.3	mA
				f_{IH} = 24 MHz Note 3, T_A = +85 to +105°C	Normal operation	V_{DD} = 3.0 V			6.7	
				f_{IH} = 16 MHz Note 3, T_A = -40 to +85°C	Normal operation	V_{DD} = 3.0 V		2.4	4.6	
				f_{IH} = 16 MHz Note 3, T_A = +85 to +105°C	Normal operation	V_{DD} = 3.0 V			4.9	
			LS (low-speed main) mode (MCSEL = 0)	f_{IH} = 8 MHz Note 3, T_A = -40 to +85°C	Normal operation	V_{DD} = 3.0 V		1.1	2.0	mA
						V_{DD} = 2.0 V		1.1	2.0	
			LS (low-speed main) mode (MCSEL = 1)	f_{IH} = 4 MHz Note 3, T_A = -40 to +85°C	Normal operation	V_{DD} = 3.0 V		0.72	1.30	mA
						V_{DD} = 2.0 V		0.72	1.30	
				f_{IM} = 4 MHz Note 7, T_A = -40 to +85°C	Normal operation	V_{DD} = 3.0V		0.58	1.10	
						V_{DD} = 2.0V		0.58	1.10	
			LV (low-voltage main) mode	f_{IH} = 3 MHz Note 3, T_A = -40 to +85°C	Normal operation	V_{DD} = 3.0 V		1.2	1.8	mA
						V_{DD} = 2.0 V		1.2	1.8	

(omitted)

13. 34.3.2 Supply current characteristics(p.863)

Incorrect)

(TA = -40 to +85°C, 1.6 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)
(TA = +85 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V) (3/4)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	IDD2 Note 2	HALT mode	HS (high-speed main) mode	fIH = 24 MHz Note 4, TA = -40 to +85°C	VDD = 3.0 V		0.37	1.83	mA
				fIH = 24 MHz Note 4, TA = +85 to +105°C	VDD = 3.0 V			2.85	
				fIH = 16 MHz Note 4, TA = -40 to +85°C	VDD = 3.0 V		0.36	1.38	
				fIH = 16 MHz Note 4, TA = +85 to +105°C	VDD = 3.0 V			2.08	
			LS (low-speed main) mode (MCSEL = 0)	fIH = 8 MHz Note 4, TA = -40 to +85°C	VDD = 3.0 V		250	710	µA
					VDD = 2.0 V		250	710	
			LS (low-speed main) mode (MCSEL = 1)	fIH = 4 MHz Note 4, TA = -40 to +85°C	VDD = 3.0 V		204	400	µA
					VDD = 2.0 V		204	400	
				fIM = 4 MHz Note 7, TA = -40 to +85°C	VDD = 3.0 V		40	250	
					VDD = 2.0 V		40	250	
			LV (low-voltage main) mode	fIH = 4 MHz Note 4, TA = -40 to +85°C	VDD = 3.0 V		425	800	mA
					VDD = 2.0 V		425	800	
			LP (low-power main) mode (MCSEL = 1)	fIH = 1 MHz Note 4, TA = -40 to +85°C	VDD = 3.0 V		192	400	µA
					VDD = 2.0 V		192	400	
				fIM = 1 MHz Note 6, TA = -40 to +85°C	VDD = 3.0 V		27	100	
					VDD = 2.0 V		27	100	

(omitted)

Correct)

(TA = -40 to +85°C, 1.6 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)
(TA = +85 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V) (3/4)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	IDD2 Note 2	HALT mode	HS (high-speed main) mode	fIH = 24 MHz Note 4, TA = -40 to +85°C	VDD = 3.0 V		0.37	1.83	mA
				fIH = 24 MHz Note 4, TA = +85 to +105°C	VDD = 3.0 V			2.85	
				fIH = 16 MHz Note 4, TA = -40 to +85°C	VDD = 3.0 V		0.36	1.38	
				fIH = 16 MHz Note 4, TA = +85 to +105°C	VDD = 3.0 V			2.08	
			LS (low-speed main) mode (MCSEL = 0)	fIH = 8 MHz Note 4, TA = -40 to +85°C	VDD = 3.0 V		250	710	µA
					VDD = 2.0 V		250	710	
			LS (low-speed main) mode (MCSEL = 1)	fIH = 4 MHz Note 4, TA = -40 to +85°C	VDD = 3.0 V		204	400	µA
					VDD = 2.0 V		204	400	
				fIM = 4 MHz Note 7, TA = -40 to +85°C	VDD = 3.0 V		40	250	
					VDD = 2.0 V		40	250	
			LV (low-voltage main) mode	fIH = 3 MHz Note 4, TA = -40 to +85°C	VDD = 3.0 V		425	800	µA
					VDD = 2.0 V		425	800	
			LP (low-power main) mode (MCSEL = 1)	fIH = 1 MHz Note 4, TA = -40 to +85°C	VDD = 3.0 V		192	400	µA
					VDD = 2.0 V		192	400	
				fIM = 1 MHz Note 7, TA = -40 to +85°C	VDD = 3.0 V		27	100	
					VDD = 2.0 V		27	100	

(omitted)