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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SH7-A787A/E	Rev.	1.00
Title	Correction of Errors in SH7280 Group Hardware Manual		Information Category	Technical Notification		
Applicable Product	SH7280 Series, SH7243 Series	Lot No. All lots	Reference Document	SH7280 Group Hardware Manual (REJ09B0393-0100)		

Thank you for your consistent patronage of Renesas semiconductor products.

We would like to inform you of the corrections to errors in the hardware manual of the above applicable products.

Refer to the following for details.

Figure 1.1 "Block Diagram" in section 1 "Overview" on p. 9 is corrected separately for SH7286/SH7285 and SH7243 as follows.

[Before change]

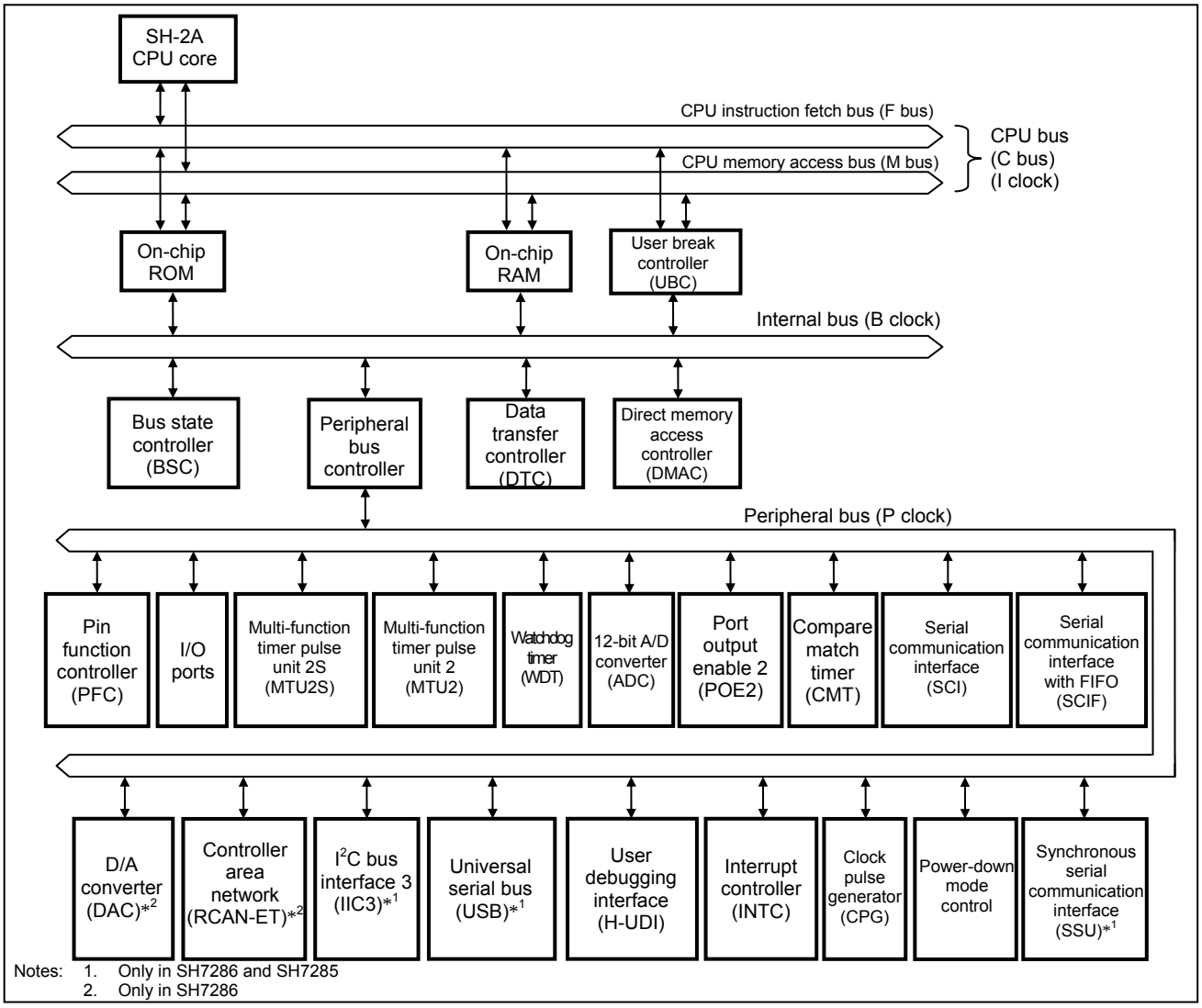


Figure 1.1 Block Diagram

[After change]

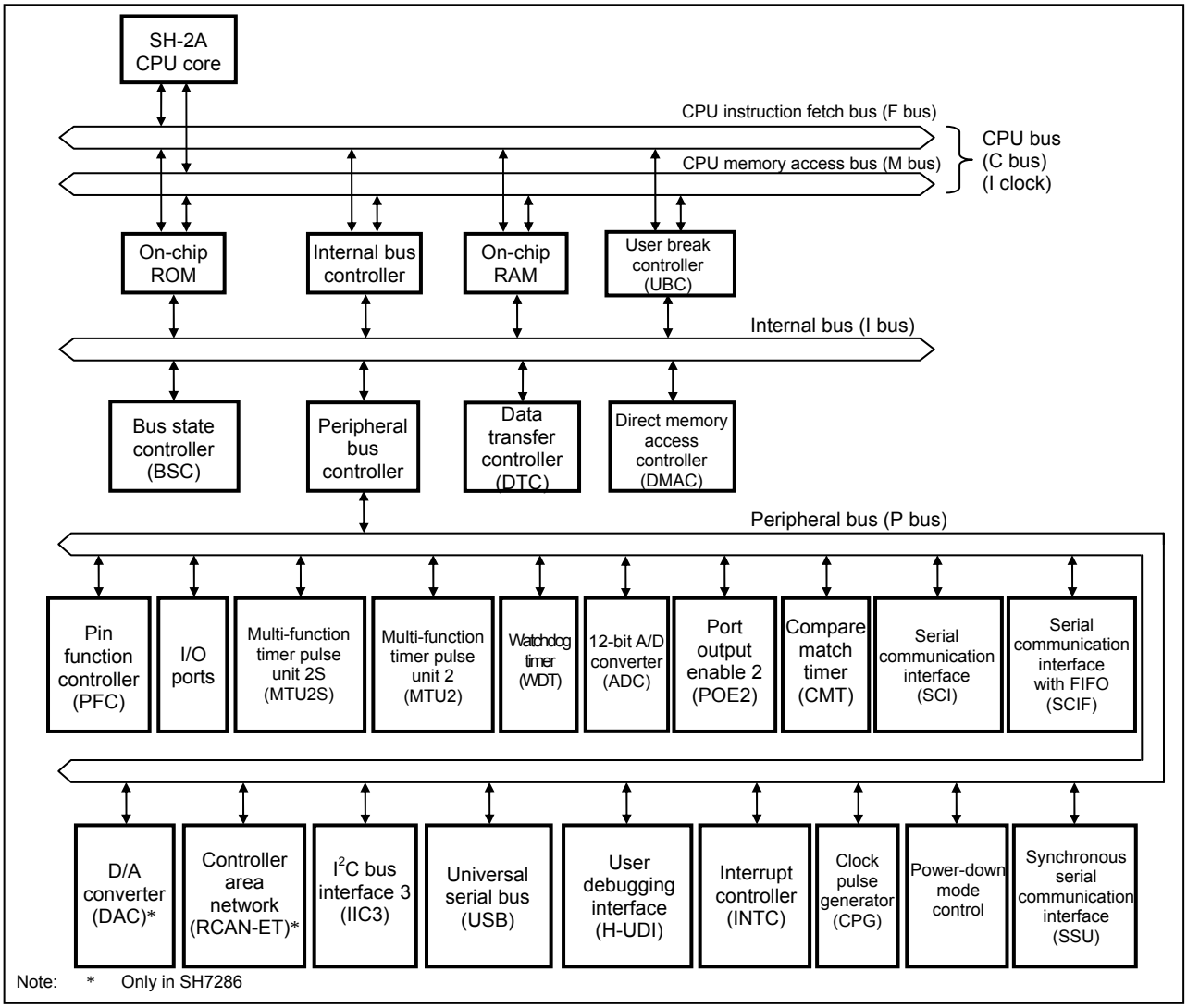


Figure 1.1 (a) Block Diagram (SH7285, SH7286)

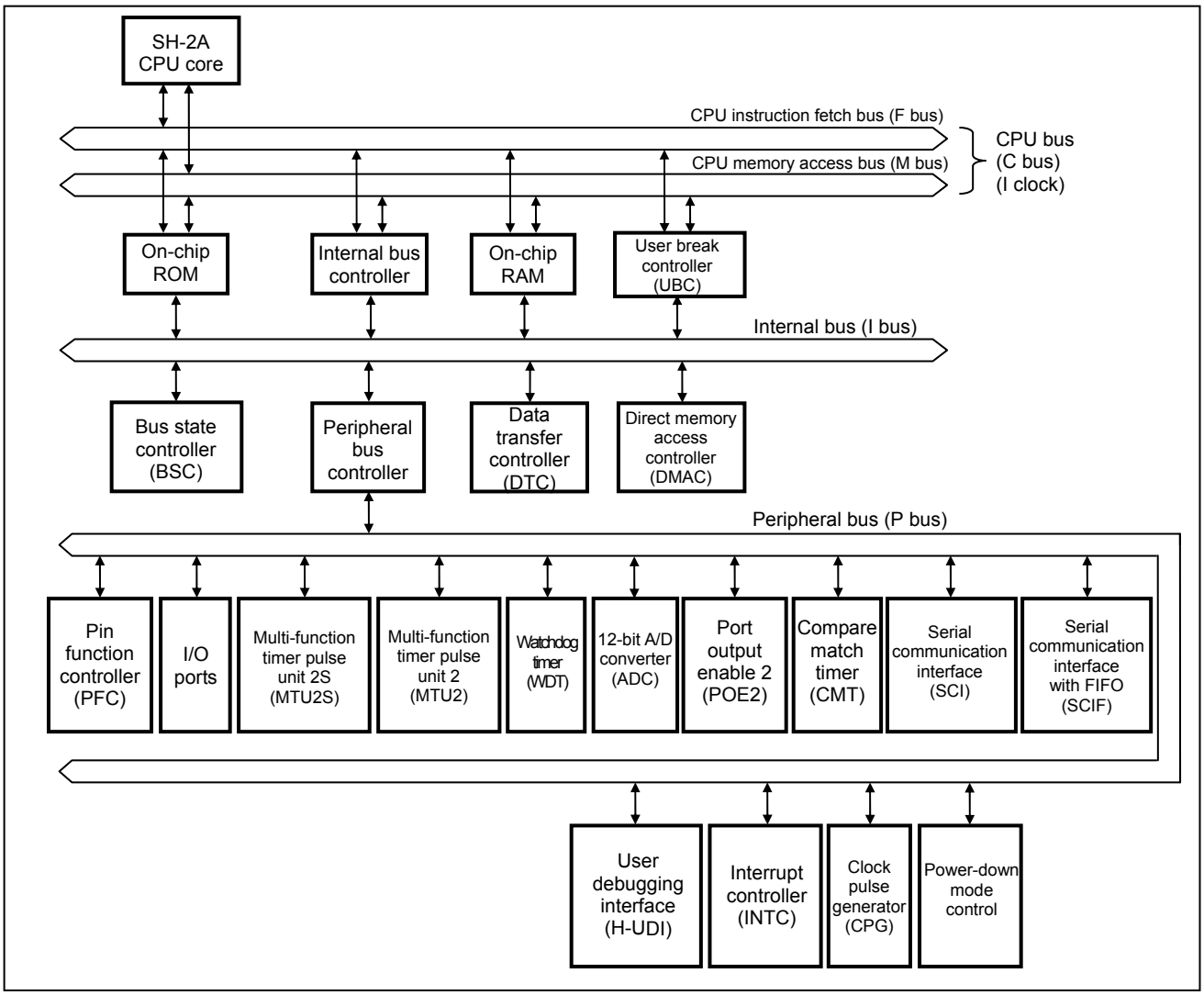


Figure 1.1 (b) Block Diagram (SH7243)

The description in section 4.4.1 "Frequency Control Register (FRQCR)" of section 4 "Clock Pulse Generator (CPG)" on p. 81 is corrected as follows.

[Before change]

After executing an instruction for modifying the FRQCR, be sure to execute 32 NOP instructions. Especially when writing/erasing to the flush memory, execute the NOP operation for 32Pϕ clock after having confirmed the set value by reading the FRQCR.

[After change]

After executing an instruction for modifying FRQCR, be sure to execute NOP instructions for 32 cycles of Pϕ. FRQCR should be modified by a program in the on-chip ROM or on-chip RAM.

A part of figure 4.5 "Example of Connecting a Ceramic Resonator" in section 4 "Clock Pulse Generator (CPG)" on p. 91 is corrected as follows.

[Before change]

Ceramic resonator: CSTCZ48M0X11R***-RD

(Murata Manufacturing Co., Ltd.)

Contact your Renesas Technology sales agency for detailes of Rf and Rd values.

Ta = −30 to +85 °C

[After change]

Ceramic resonator: CSTCW48M0X11***-R0

(Murata Manufacturing Co., Ltd.)

Contact your Renesas Technology sales agency for details of Rf and Rd values.

Ta = 0 to 70 °C

The following description is added to section 7 "User Break Controller (UBC)" on p. 196.

[After change]

7.5 Interrupt Source

7.5.1 Interrupt Source

The UBC has the user break interrupt as an interrupt source. Table 7.4 gives details on this interrupt source.

A user break interrupt is generated when one of the compare match flags (SCMFD3 to SCMFD0 and SCMFC3 to SCMFC0) in the break control register (BRCR) is set to 1. Clearing the interrupt flag bit to 0 cancels the interrupt request.

Table 7.4 Interrupt Source

Interrupt Name	Interrupt Source	Interrupt Enable Bit	Interrupt Flags	Interrupt Level
User break	User break interrupt	—	SCMFD3, SCMFD2, SCMFD1, SCMFD0,SCMFC3, SCMFC2, SCMFC1, and SCMFC0	Fixed to 15

The description in section 8.5.9 "DTC Bus Release Timing" of section 8 "Data Transfer Controller (DTC)" on p. 233 is corrected as follows.

[Before change]

The DTC requests the bus mastership to the bus arbiter when an activation request occurs.

[After change]

The DTC requests the bus mastership of the internal bus (I bus) to the bus arbiter when an activation request occurs.

Table 8.11 "DTC Bus Release Timing" in section 8 "Data Transfer Controller (DTC)" on p. 234 is corrected as follows.

[Before change]

	Bus Function Extending Register (BSCEHR) Setting		Bus Release Timing (O: Bus must be released; x: Bus is not released)				
						After Write-Back of Transfer Information	
	DTLOCK	DTBST	After Vector Read	After Transfer Information Read	After a Single Data Transfer	Normal Transfer	Continuous Transfer
Setting 1	0	0	×	×	×	O	O
Setting 2*	0	1	×	×	×	O	×
Setting 3	1	0	O	O	O	O	O

Note: * The following restrictions apply to setting 2.

- The clock setting through the frequency control register (FROCR) must be Iϕ : Bϕ : Pϕ = 8 : 4 : 4, 4 : 2 : 2, or 2 : 1 : 1.
- The vector information must be stored in the on-chip ROM or RAM.
- The transfer information must be stored in the on-chip RAM.
- Transfer must be between the on-chip RAM and an on-chip peripheral module or between the external memory and an on-chip peripheral module.

[After change]

	Bus Function Extending Register (BSCEHR) Setting		Bus Release Timing (O: Bus must be released; x: Bus is not released)				
						After Write-Back of Transfer Information	
	DTLOCK	DTBST	After Vector Read	After Transfer Information Read	After a Single Data Transfer	Normal Transfer	Continuous Transfer
Setting 1	0	0	×	×	×	O	O
Setting 2*[1]	0	1	×	×	×	O	×
Setting 3*[2]	1	0	O	O	O	O	O

Notes: 1. The following restrictions apply to setting 2.

- The clock setting through the frequency control register (FROCR) must be Iϕ : Bϕ : Pϕ : Mϕ : Aϕ = 8 : 4 : 4 : 8 : 4 or 8 : 4 : 4 : 4 : 4.
- The vector information must be stored in the on-chip ROM or RAM.
- The transfer information must be stored in the on-chip RAM.
- Transfer must be between the on-chip RAM and an on-chip peripheral module or between the external memory and an on-chip peripheral module.

2. The following restriction applies to setting 3.

- The DTPR bit in BSCEHR should be 0. Setting the DTPR bit to 1 is prohibited.

The following description is added to section 8.5.10 "DTC Activation Priority Order" in section 8 "Data Transfer Controller (DTC)" on p. 236.

[Before change]

If multiple DTC activation requests are generated while the DTC is inactive, whether to start the DTC transfer from the first activation request or according to the DTC activation priority can be selected through the DTPR bit setting in the bus function extending register (BSCEHR).

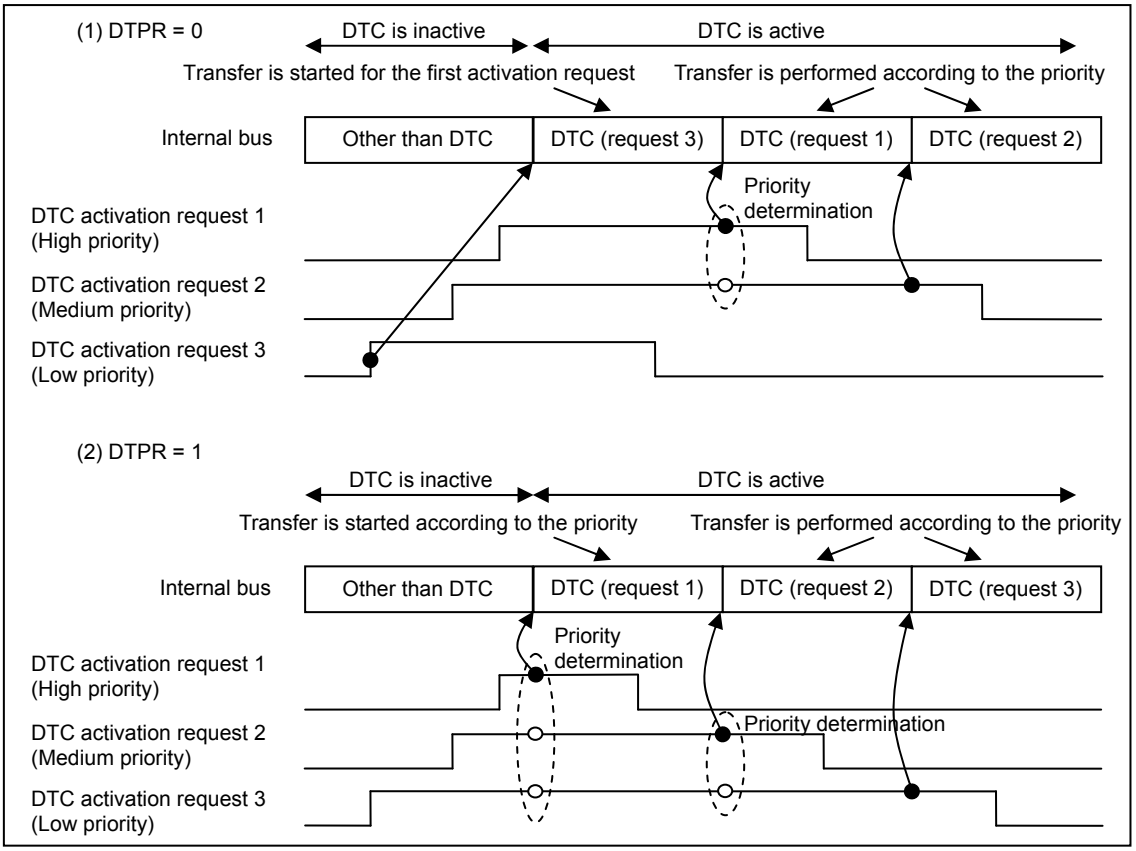
[After change]

If multiple DTC activation requests are generated while the DTC is inactive, whether to start the DTC transfer from the first activation request* or according to the DTC activation priority can be selected through the DTPR bit setting in the bus function extending register (BSCEHR).

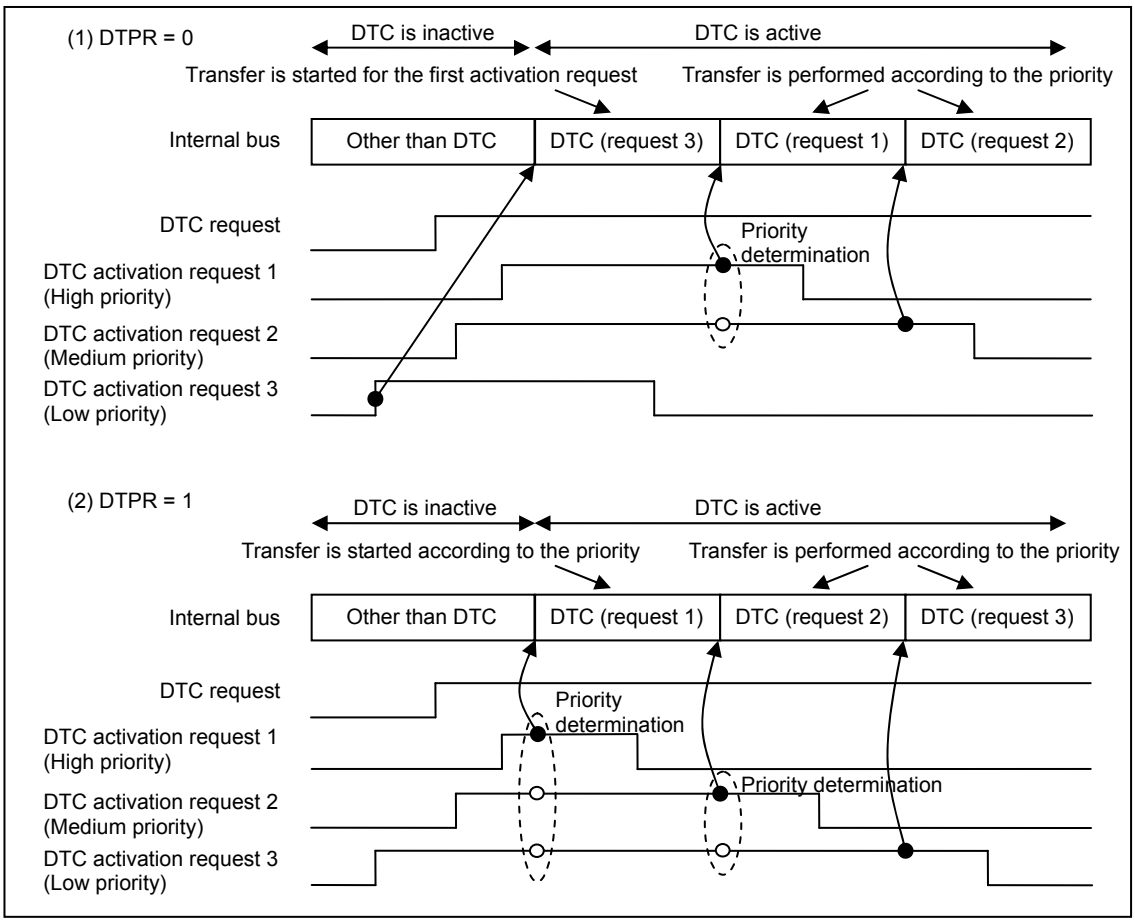
Note: * When one DTC activation request is generated before another, transfer starts with the first request. When an activation request with a higher priority is generated before a pending DTC request is accepted, transfer starts for the request with higher priority. The timing of DTC request generation varies according to the operating state of internal buses.

Figure 8.17 "Example of DTC Activation According to Priority" in section 8 "Data Transfer Controller (DTC)" on p. 236 is corrected as follows.

[Before change]



[After change]



Note 3 for the BSZ[1:0] bits in section 9.4.2 "CSn Space Bus Control Register (CSnBCR) (n = 0 to 7)" of section 9 "Bus State Controller (BSC)" on p. 263 is corrected as follows.

[Before change]

3. If area 2 or area 3 is specified as SDRAM space, the bus width can be specified as 16 bits only.

[After change]

3. If area 2 or area 3 is specified as SDRAM space, the bus width can be specified as 16 bits or 32 bits.

Note 1 for the DTBST bit in section 9.4.8 "Bus Function Extending Register (BSCEHR)" of section 9 "Bus State Controller (BSC)" on p. 302 is corrected as follows.

[Before change]

1. Clock setting through the frequency control register (FRQCR) must be Iϕ : Bϕ : Pϕ : Mϕ : Aϕ = 8 : 4 : 4 : 4 : 4, 4 : 2 : 2 : 2 : 2, or 2 : 1 : 1 : 1 : 1.

[After change]

1. Clock setting through the frequency control register (FRQCR) must be Iϕ : Bϕ : Pϕ : Mϕ : Aϕ = 8 : 4 : 4 : 4 : 4 or 8 : 4 : 4 : 8 : 4.

The description of the DTPR bit in section 9.4.8 "Bus Function Extending Register (BSCEHR)" of section 9 "Bus State Controller (BSC)" on p. 303 is corrected as follows.

[Before change]

DTC Activation Priority

Selects whether to start transfer from the first DTC activation request or according to the DTC activation priority when multiple DTC activation requests are generated before the DTC is activated.

Note that DTC transfer is always started according to the DTC activation priority when multiple DTC activation requests are generated while the DTC is active.

0: Starts transfer from the DTC activation request generated first.

1: Starts transfer according to the DTC activation priority.

Notes: When this bit is set to 1, the following restrictions apply.

1. The vector information must be stored in the on-chip ROM or on-chip RAM.
2. The transfer information must be stored in the on-chip RAM.
3. The function for skipping the transfer information read step is always disabled.

[After change]

DTC Activation Priority

Selects whether to start transfer from the first DTC activation request or according to the DTC activation priority when multiple DTC activation requests are generated before the DTC is activated.

For details, see section 8.5.10, DTC Activation Priority Order.

0: Starts transfer from the DTC activation request generated first.

1: Starts transfer according to the DTC activation priority.

Notes: When this bit is set to 1, the following restrictions apply.

1. The vector information must be stored in the on-chip ROM or on-chip RAM.
2. The transfer information must be stored in the on-chip RAM.
3. The function for skipping the transfer information read step is always disabled.
4. The DTLOCK bit should be 0. Setting the DTLOCK bit to 1 is prohibited.

The titles of figures 9.14 and 9.15 in section 9 "Bus State Controller (BSC)" on p. 323 and p. 324, respectively, are corrected as follows.

[Before change]

Figure 9.14 Example of 32-Bit Data Width SRAM Connection ($\overline{\text{RASU}}$ and $\overline{\text{CASU}}$ are Not Used)

Figure 9.15 Example of 16-Bit Data Width SRAM Connection ($\overline{\text{RASU}}$ and $\overline{\text{CASU}}$ are Not Used)

[After change]

Figure 9.14 Example of 32-Bit Data Width SDRAM Connection ($\overline{\text{RASU}}$ and $\overline{\text{CASU}}$ are Not Used)

Figure 9.15 Example of 16-Bit Data Width SDRAM Connection ($\overline{\text{RASU}}$ and $\overline{\text{CASU}}$ are Not Used)

Table 9.17 "Relationship between Bus Width, Access Size, and Number of Bursts" in section 9 "Bus State Controller (BSC)" on p. 360 is corrected as follows.

[Before change]

Bus Width	Access Size	CSnWCR. BST[1:0] Bits	Number of Bursts	Access Count
8 bits	8 bits	Not affected	1	1
	16 bits	Not affected	2	1
	32 bits	Not affected	4	1
	16 bytes	x0	16	1
		10	4	4
16 bits	8 bits	Not affected	1	1
	16 bits	Not affected	2	1
	32 bits	Not affected	8	1
	16 bytes	00	2	4
		01	4	2
		10*	2, 4, 2	3

Note: * When the bus width is 16 bits, the access size is 16 bits, and the BST[1:0] bits in CSnWCR are 10, the number of bursts and access count depend on the access start address. At address H'xxx0 or H'xxx8, 4-4 burst access is performed. At address H'xxx4 or H'xxxC, 2-4-2 burst access is performed.

[After change]

Bus Width	Access Size	CSnWCR.BST[1:0] Bits	Number of Bursts	Access Count
8 bits	8 bits	Not affected	1	1
	16 bits	Not affected	2	1
	32 bits	Not affected	4	1
	16 bytes*2	x0	16	1
		10	4	4
16 bits	8 bits	Not affected	1	1
	16 bits	Not affected	2	1
	32 bits	Not affected	8	1
	16 bytes*2	00	2	4
		01	4	2
		10*1	2, 4, 2	3

Notes: 1. When the bus width is 16 bits, the access size is 16 bits, and the BST[1:0] bits in CSnWCR are 10, the number of bursts and access count depend on the access start address. At address H'xxx0 or H'xxx8, 4-4 burst access is performed. At address H'xxx4 or H'xxxC, 2-4-2 burst access is performed.

2. Only the DMAC is capable of transfer with 16 bytes as the unit of access. The maximum unit of access for the DTC and CPU is 32 bits.

The description of section 9.5.9 "Burst ROM (Clock Synchronous) Interface" in section 9 "Bus State Controller (BSC)" on p. 367 is corrected as follows.

[Before change]

These invalid data read cycles increase the memory access time and degrade the program execution speed and DMA transfer speed. To prevent this problem, using 16-byte read by cache fill in the cache-enabled space or 16-byte read by the DMA is recommended. The burst ROM interface performs write access in the same way as normal space access.

[After change]

These invalid data read cycles increase the memory access time and degrade the program execution speed and DMA transfer speed. To prevent this problem, using 16-byte read by the DMA is recommended. The burst ROM interface performs write access in the same way as normal space access.

The description of (5) Read data transfer cycle, in table 9.18 "Conditions for Determining Number of Idle Cycles" in section 9 "Bus State Controller (BSC)" on p. 370 is corrected as follows.

[Before change]

This is neither generated when the HM[1:0] bits in CSnWCR are not B'00.

[After change]

This is neither generated when the WM[1:0] bits in CSnWCR are not B'00.

The following description is added to section 9 "Bus State Controller (BSC)" on p. 380.

[After change]

9.6 Interrupt Source

9.6.1 Interrupt Source

The BSC has the compare match interrupt (CMI) as an interrupt source.

Table 9.23 gives details on this interrupt source. The compare match interrupt enable bit (CMIE) in the refresh timer control/status register (RTCSR) can be used to enable or disable the interrupt source.

The compare match interrupt (CMI) is generated when both the compare match flag (CMF) and compare match interrupt enable bit (CMIE) in RTCSR are set to 1.

Clearing the interrupt flag bit to 0 cancels the interrupt request.

Table 9.23 Interrupt Source

Interrupt Name	Interrupt Source	Interrupt Enable Bit	Interrupt Flag
CMI	Compare match interrupt	CMIE	CMF

The following description is added to section 10 "Direct Memory Access Controller (DMAC)" on p. 431.

[After change]

10.5 Interrupt Sources

10.5.1 Interrupt Sources and Priority

The interrupt sources of the DMAC are the data transfer end interrupt (DEI) and data transfer half-end interrupt (HEI) for each channel.

Table 10.11 lists the interrupt sources and their priority. The IE and HIE bits in the DMA channel control registers (CHCRs) enable or disable the respective interrupt sources. Furthermore, the interrupt requests are independently conveyed to the interrupt controller.

A data transfer end interrupt (DEI) is generated when both the transfer end flag and transfer end interrupt enable (IE) bit in the DMA channel control register (CHCR) are set to 1.

A data transfer half-end interrupt (HEI) is generated when both the half-end flag and half-end interrupt enable (HIE) bit in the DMA channel control register (CHCR) are set to 1.

Clearing the interrupt flag bit to 0 cancels the interrupt request.

Priority among the channels is adjustable by the interrupt controller. The priority for interrupts of a given channel is fixed. For details, refer to section 6, Interrupt Controller (INTC).

Table 10.11 Interrupt Sources

Channel	Interrupt Source	Interrupt Enable Bit	Interrupt Flag	Priority
0	Data transfer end interrupt (TEI_0)	IE	TE	High
	Data transfer half-end interrupt (HEI_0)	HIE	HE	
1	Data transfer end interrupt (TEI_1)	IE	TE	
	Data transfer half-end interrupt (HEI_1)	HIE	HE	
2	Data transfer end interrupt (TEI_2)	IE	TE	
	Data transfer half-end interrupt (HEI_2)	HIE	HE	
3	Data transfer end interrupt (TEI_3)	IE	TE	
	Data transfer half-end interrupt (HEI_3)	HIE	HE	
4	Data transfer end interrupt (TEI_4)	IE	TE	
	Data transfer half-end interrupt (HEI_4)	HIE	HE	
5	Data transfer end interrupt (TEI_5)	IE	TE	
	Data transfer half-end interrupt (HEI_5)	HIE	HE	
6	Data transfer end interrupt (TEI_6)	IE	TE	
	Data transfer half-end interrupt (HEI_6)	HIE	HE	
7	Data transfer end interrupt (TEI_7)	IE	TE	
	Data transfer half-end interrupt (HEI_7)	HIE	HE	Low

The description of the WRE bit in section 11.3.32 "Timer Waveform Control Register (TWCR)" of section 11 "Multi-Function Timer Pulse Unit 2 (MTU2)" on p. 521 is corrected as follows.

[Before change]

Waveform Retain Enable

Selects the waveform output when synchronous counter clearing occurs in complementary PWM mode.

The output waveform is retained only when synchronous clearing occurs within the Tb interval at the trough in complementary PWM mode. When synchronous clearing occurs outside this interval, the initial value specified in TOCR is output regardless of the WRE bit setting. The initial value is also output when synchronous clearing occurs in the Tb interval at the trough immediately after TCNT_3 and TCNT_4 start operation.

For the Tb interval at the trough in complementary PWM mode, see figure 11.40.

0: Outputs the initial value specified in TOCR

1: Retains the waveform output immediately before synchronous clearing

[Setting condition]

- When 1 is written to WRE after reading WRE = 0

[After change]

Initial Output Suppression Enable

Selects the waveform output when synchronous counter clearing occurs in complementary PWM mode.

The initial output is suppressed only when synchronous clearing occurs within the Tb interval at the trough in complementary PWM mode. When synchronous clearing occurs outside this interval, the initial value specified in TOCR is output regardless of the WRE bit setting. The initial value is also output when synchronous clearing occurs in the Tb interval at the trough immediately after TCNT_3 and TCNT_4 start operation.

For the Tb interval at the trough in complementary PWM mode, see figure 11.40.

0: Outputs the initial value specified in TOCR

1: Suppresses initial output

[Setting condition]

- When 1 is written to WRE after reading WRE = 0

The following table is added to section 14.4.1 "Interrupt Sources and DTC/DMA Transfer Requests" in section 14 "Compare Match Timer (CMT)" on p. 730.

[After change]

Table 14.2 Interrupt Sources

Channel	Interrupt Source	Interrupt Enable Bit	Interrupt Flag	DMAC/DTC Activation	Priority
0	CMI0	CMIE	CMF	Possible	High
1	CMI1	CMIE	CMF	Possible	Low

The description in section 15.3.2 "Watchdog Timer Control/Status Register (WTCSR)" of section 15 "Watchdog Timer (WDT)" on p. 739 is corrected as follows.

[Before change]

WTCSR is initialized to H'18 by a power-on reset caused by the $\overline{\text{RES}}$ pin or in software standby mode.

[After change]

WTCSR is initialized to H'18 by a power-on reset caused by the $\overline{\text{RES}}$ pin, an internal reset caused by the WDT, or in software standby mode.

The following is added to the description in section 15.4.2 "Using Watchdog Timer Mode" of section 15 "Watchdog Timer (WDT)" on p. 746.

[After change]

7. Since WTCSR is initialized by an internal reset caused by the WDT, the TME bit in WTCSR is cleared to 0. This makes the counter stop (be initialized). To use the WDT in watchdog timer mode again, after clearing the WOVF flag in WRCSR, set watchdog timer mode again.

The following description is added to section 15 "Watchdog Timer (WDT)" on p. 748.

[After change]

15.5 Interrupt Source

15.5.1 Interrupt Source

The WDT has the interval timer interrupt (ITI) as an interrupt source.

Table 15.3 gives details on this interrupt source. The interval timer interrupt (ITI) is generated when the interval timer overflow flag (IOVF) in the watchdog timer control/status register (WTCSR) is set to 1. Clearing the interrupt flag bit to 0 cancels the interrupt request.

Table 15.3 Interrupt Source

Interrupt Name	Interrupt Source	Interrupt Enable Bit	Interrupt Flag
ITI	Interval timer interrupt	—	Interval timer overflow (IOVF)

The description of a clearing condition or setting condition in section 16.3.7 "Serial Status Register (SCSSR)" of section 16 "Serial Communication Interface (SCI)" on p. 763 to p. 768 are corrected as follows.

[Before change]

- By a power-on reset or in standby mode

[After change]

- By a power-on reset or in module standby mode

Figure 16.12 "Sample Flowchart for Receiving Serial Data (1)" in section 16 "Serial Communication Interface (SCI)" on p. 801 is corrected as follows.

[Before change]

Set the CKE1 and CKE0 bits in SCSCR

(TE and RE bits are 0)

[After change]

Read the receive data in SCRDR and clear RDRF flag in SCSSR to 0

The description in section 16.5 "SCI Interrupt Sources and DTC" of section 16 "Serial Communication Interface (SCI)" on p. 811 is corrected as follows.

[Before change]

When the ORER, FER, or PER flag in SCSSR is set to 1, an ERI interrupt request is generated. This request cannot be used to activate the DTC. When processing the received data through the DTC and handling the receive error by an interrupt requested to the CPU, set the RIE bit to 1 and set the EIO bit in SCSPTR to 1 to issue an interrupt to the CPU only when a receive error is detected. If the EIO bit is cleared to 0, an interrupt is issued to the CPU even when correct data is received.

[After change]

When the ORER, FER, or PER flag in SCSSR is set to 1, an ERI interrupt request is generated. This request cannot be used to activate the DTC. In processing for data reception, generation of ERI interrupt requests can only be enabled if generation of RXI interrupt requests is disabled. In this case, set the RIE bit and the EIO bit in SCSPTR to 1. However, note that the DMAC or DTC will not transfer received data since RXI interrupt requests are not generated while the EIO bit is set to 1.

The description of the ICE bit in section 19.3.1 "I^2C Bus Control Register 1 (ICCR1)" of section 19 "I^2C Bus Interface 3 (IIC3)" on p. 929 is corrected as follows.

[Before change]

I^2C Bus Interface 3 Enable

0: This module is halted. (SCL and SDA pins function as ports.)

1: This bit is enabled for transfer operations. (SCL and SDA pins are bus drive state.)

[After change]

I^2C Bus Interface 3 Enable

0: Output from SCL and SDA is disabled. (Input to SCL and SDA enabled .)

1: This bit is enabled for transfer operations. (SCL and SDA pins are bus drive state.)

The description of the NAKIE bit in section 19.3.4 "I^{2}C Bus Interrupt Enable Register (ICIER)" of section 19 "I^{2}C Bus Interface 3 (IIC3)" on p. 937 is corrected as follows.

[Before change]

NACK Receive Interrupt Enable

Enables or disables the NACK detection interrupt request (NAKI) and the overrun error (OVE set in ICSR) interrupt request (ERI) in the clocked synchronous format when the NACKF or AL/OVE bit in ICSR is set. NAKI can be canceled by clearing the NACKF, AL/OVE, or NAKIE bit to 0.

0: NACK receive interrupt request (NAKI) is disabled.

1: NACK receive interrupt request (NAKI) is enabled.

[After change]

NACK Receive Interrupt Enable

Enables or disables the NACK detection interrupt request (NAKI) when the NACKF or AL/OVE bit in ICSR is set. NAKI can be canceled by clearing the NACKF, AL/OVE, or NAKIE bit to 0.

0: NACK receive interrupt request (NAKI) is disabled.

1: NACK receive interrupt request (NAKI) is enabled.

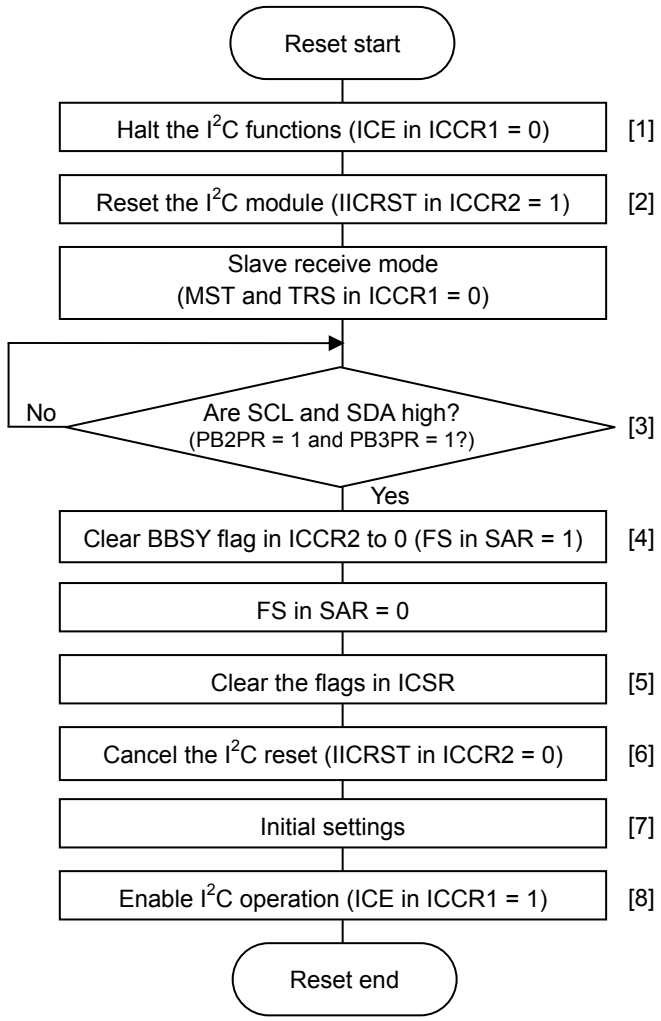
The following description is added to section 19 "I^{2}C Bus Interface 3 (IIC3)" on p. 958.

[After change]

19.4.8 IIC3 Reset

Some registers and the control part for I^{2}C of the I^{2}C bus interface 3 can be reset by writing 1 to the IICRST bit in ICCR2. An example of the sequence for resetting the I^{2}C bus interface 3 by using the IICRST bit is shown in the following.

1. Write 0 to the ICE bit in ICCR1 to halt functioning of the I^{2}C bus interface 3.
2. Write 1 to the IICRST bit in ICCR2 to reset some registers and the control part of the I^{2}C bus interface 3 module.
3. Write 0 to the MST and TRS bits in ICCR1 to switch the operating mode to slave receive mode.
4. Wait until the bus is released. Determine whether the bus is released by reading the I/O port bits (PB2PR and PB3PR bits in PBPRL) corresponding to SCL and SDA.
5. Write 1 to the FS bit in SAR and clear the BBSY flag in ICCR2 to 0. After the BBSY flag has been cleared to 0, write 0 to the FS bit.
6. Clear the flags (TEND, RDRF, NACKF, STOP, AL/OVE, AAS, and ADZ) in ICSR to 0.
7. Write 0 to the IICRST bit in ICCR2 to release the I^{2}C module from the reset state.
8. Initialize I^{2}C registers (ICCR1, ICCR2, ICMR, ICIER, SAR, and NF2CYC).
9. Write 1 to the ICE bit in ICCR1 to enable transfer operations.



[1] Halts the I^2C functions.

[2] Resets the I^2C. The BBSY flag in ICCR2 becomes undefined.

[3] Waits until the bus is released. Determines whether the bus is released by reading the I/O port bits corresponding to SCL and SDA.

[4] Clears the BBSY flag in ICCR2 to 0.

[5] Clears the flags (TEND, RDRF, NACKF, STOP, AL/OVE, AAS, and ADZ) in ICSR to 0.

[6] Cancels the I^2C reset.

[7] Initializes I^2C registers (ICCR1, ICCR2, ICMR, ICIER, SAR, and NF2CYC).

[8] Enables transfer operations.

Figure 19.18 Sample I^2C Reset Procedure in Master Transmit Mode and Master Receive Mode

The description in section 19.8.2 "Note on Master Receive Mode" of section 19 "I^2C Bus Interface 3 (IIC3)" on p. 968 is corrected as follows.

[Before change]

Use either 1 or 2 below as a measure against the situations above.

1. In master receive mode, read ICDRR before the rising edge of the 8th clock.
2. In master receive mode, set the RCVD bit to 1 so that transfer proceeds in byte units.

[After change]

Use the following measure against the situations above.

- In master receive mode, read ICDRR before the rising edge of the 8th clock.

The following description is added to section 19.8 "Usage Notes" in section 19 "I²C Bus Interface 3 (IIC3)" on p. 969.

[After change]

19.8.5 Access to ICE and IICRST Bits during I²C Bus Operations

Writing 0 to the ICE bit in ICCR1 or 1 to the IICRST bit in ICCR2 while this LSI is in any of the following states (1 to 4) causes the BBSY flag in ICCR2 and the STOP flag in ICSR to become undefined.

1. This module is the I²C bus master in master transmit mode (MST = 1 and TRS = 1 in ICCR1).
2. This module is the I²C bus master in master receive mode (MST = 1 and TRS = 0 in ICCR1).
3. This module is transmitting data in slave transmit mode (MST = 0 and TRS = 1 in ICCR1).
4. This module is transmitting acknowledge signals in slave receive mode (MST = 0 and TRS = 0 in ICCR1).

Executing any of the following procedures releases the BBSY flag in ICCR2 from the undefined state.

- Input a start condition (falling edge of SDA while SCL is at the high level) to set the BBSY flag to 1.
- Input a stop condition (rising edge of SDA while SCL is at the high level) to clear the BBSY flag to 0.
- If the module is in master transmit mode, issue a start condition by writing 1 and 0 to the BBSY flag and the SCP bit in ICCR2, respectively, while SCL and SDA are at the high level. The BBSY flag is set to 1 on output of the start condition (falling edge of SDA while SCL is at the high level).
- With the module in master transmit or master receive mode, SDA at the low level, and no other device holding SCL at the low level, issue a stop condition by writing 0 to the BBSY flag and the SCP bit in ICCR2. The BBSY flag is cleared to 0 on output of the stop condition (rising edge of SDA while SCL is at the high level).
- Writing 1 to the FS bit in SAR clears the BBSY flag to 0 (only in products having the FS bit in SAR).

19.8.6 Using the IICRST Bit to Initialize the Registers

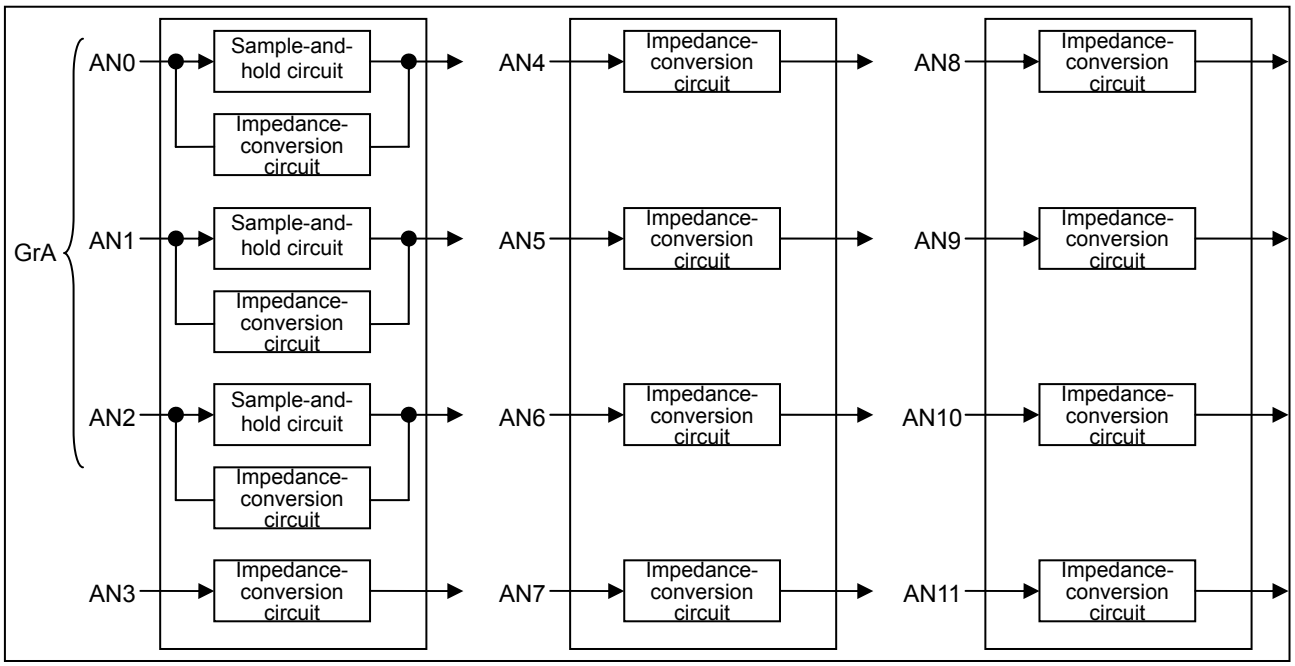
- Writing 1 to the IICRST bit sets the SDAO and SCLO bits in ICCR2 to 1.
- Writing 1 to the IICRST bit in master transmit mode or slave transmit mode sets the TDRE flag in ICSR to 1.
- During a reset due to the IICRST bit being set to 1, writing to the BBSY flag and the SCP and SDAO bits in ICCR2 is disabled.
- Even during a reset due to the IICRST bit being set to 1, the input of a start condition (falling edge of SDA while SCL is at the high level) or stop condition (rising edge of SDA while SCL is at the high level) on SCL and SDA causes the BBSY flag to be set to 1 or cleared to 0, respectively.

19.8.7 Operation of I²C Bus Interface 3 while ICE = 0

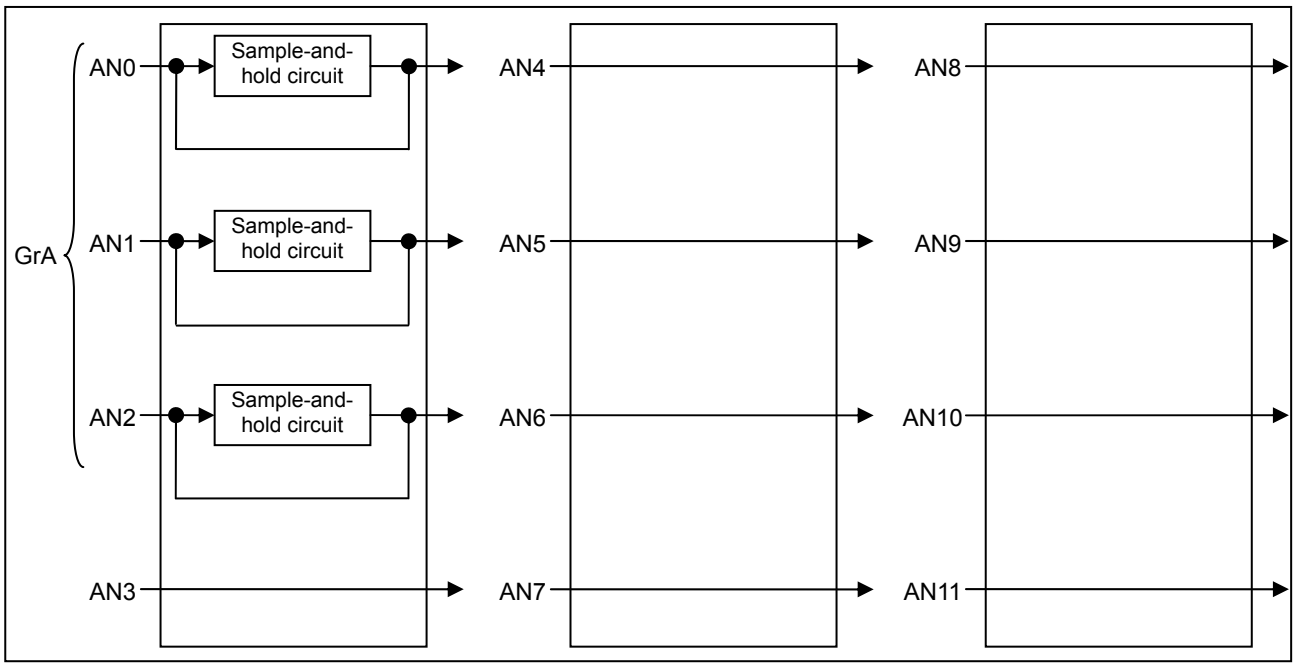
Writing 0 to the ICE bit in ICCR1 disables output on SCL and SDA. However, input on SCL and SDA remains valid. This module operates in accord with the signals input on SCL and SDA.

A part of figure 20.1 "Block Diagram of A/D Converter" in section 20 "A/D Converter (ADC)" on p. 973 is corrected as follows.

[Before change]



[After change]



The description in section 20.3.5 "A/D Bypass Control Registers 0 to 2 (ADBYPSCR_0 to ADBYPSCR_2)" of section 20 "A/D Converter (ADC)" on p. 984 is corrected as follows.

[Before change]

For A/D conversion of group A (GrA), it can be selected whether to use the sample-and-hold circuits dedicated to the group A channels or to use the impedance-conversion circuits in the same way as A/D conversion of other channels.

Setting the SH bit in ADBYPSCR_0 to 0 selects the impedance-conversion circuits; setting the SH bit to 1 selects the sample-and-hold circuits dedicated to the channels. When the impedance-conversion circuit is selected, the A/D conversion time does not include the time for sampling in the dedicated sample-and-hold circuits. For details, refer to section 20.4, Operation.

[After change]

For A/D conversion of group A (GrA), it can be selected whether or not to use the sample-and-hold circuits dedicated to the group A channels.

Setting the SH bit in ADBYPSCR_0 to 1 selects the sample-and-hold circuits dedicated to the channels. When the sample-and-hold circuits are not to be used, the A/D conversion time does not include the time for sampling in the dedicated sample-and-hold circuits. For details, refer to section 20.4, Operation.

The description of the SH bit in section 20.3.5 "A/D Bypass Control Registers 0 to 2 (ADBYPSCR_0 to ADBYPSCR_2)" of section 20 "A/D Converter (ADC)" on p. 984 is corrected as follows.

[Before change]

Dedicated Sample-and-Hold Circuit Select (ADBYPSCR_0 only)

0: Selects the impedance-conversion circuits

1: Selects the sample-and-hold circuits

[After change]

Dedicated Sample-and-Hold Circuit Select (ADBYPSCR_0 only)

0: Does not select the sample-and-hold circuits

1: Selects the sample-and-hold circuits

The description in section 20.7.5 "Notes on Noise Countermeasures" of section 20 "A/D Converter (ADC)" on p. 1008 is corrected as follows.

[Before change]

To prevent damage due to an abnormal voltage, such as an excessive surge at the analog input pins (AN0 to AN11) and analog reference power supply (AVREF), a protection circuit should be connected between the AVcc and AVss, as shown in figure 20.14. The bypass capacitors connected to AVREF and the filter capacitor connected to ANn should be connected to the AVss. If a filter capacitor is connected as shown in figure 20.14, the input currents at the analog input pin (ANn) are averaged, and an error may occur. Careful consideration is therefore required when deciding the circuit constants.

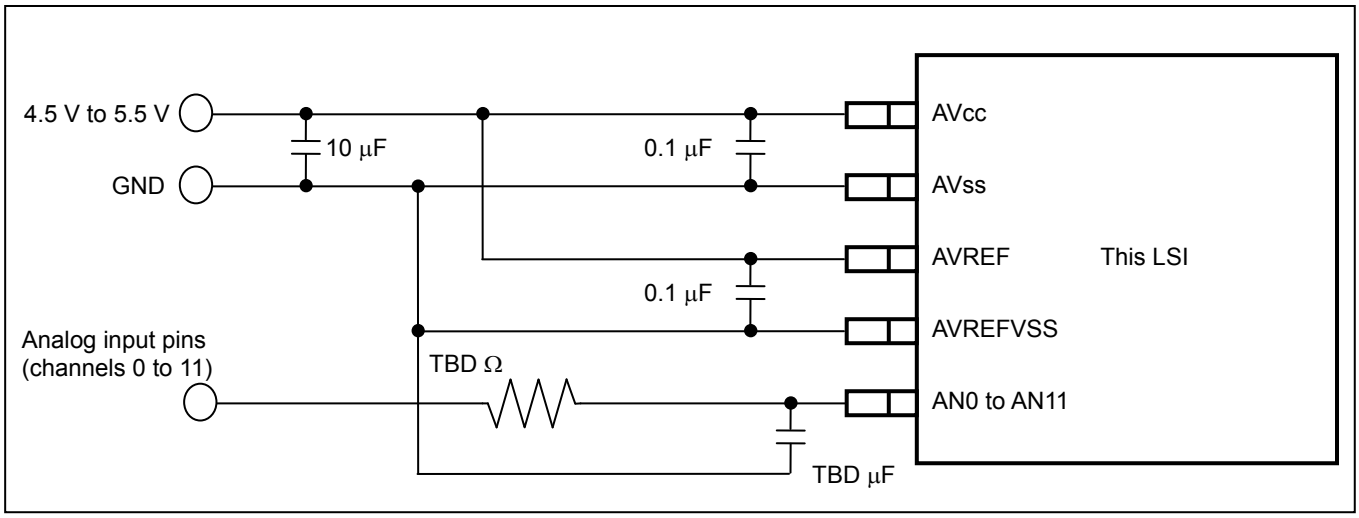


Figure 20.14 Example of Analog Input Pin Protection Circuit

[After change]

To prevent damage due to an abnormal voltage, such as an excessive surge at the analog input pins (AN0 to AN11) and analog reference power supply (AVREF), a protection circuit should be connected between the AVcc and AVss, as shown in figure 20.14. The bypass capacitors connected to AVREF and the filter capacitor connected to ANn should be connected to the AVREFVSS. If a filter capacitor is connected as shown in figure 20.14, the input currents at the analog input pin (ANn) are averaged, and an error may occur. Careful consideration is therefore required when deciding the circuit constants. The 0.1-µF capacitor in figure 20.14 should be placed close to the pin.

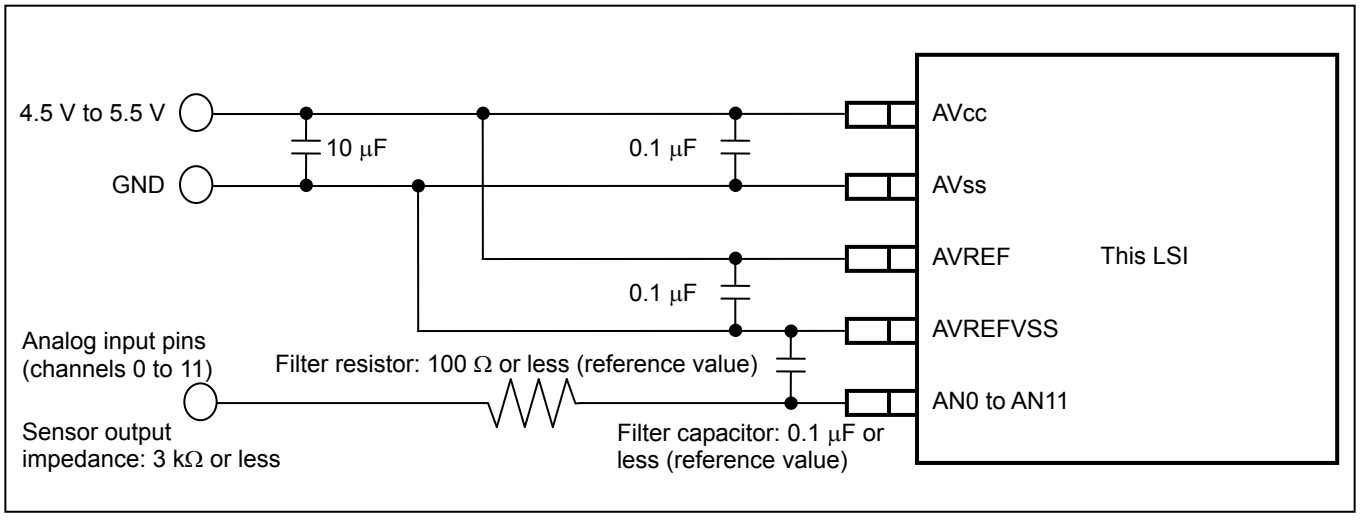


Figure 20.14 Example of Analog Input Pin Protection Circuit

The description of the BRP[7:0] bits of BCR0 in (3) Bit Configuration Register (BCR0, BCR1), in section 22.3.3 "RCAN-ET Control Registers" of section 22 "Controller Area Network (RCAN-ET)" on p. 1041 is corrected as follows.

[Before change]

Bits 7 to 0—Baud Rate Pre-scale (BRP[7:0] = BCR0 [7:0]): These bits are used to define the peripheral bus clock periods contained in a Time Quantum.

Bit 7: BRP[7]	Bit 6: BRP[6]	Bit 5: BRP[5]	Bit 4: BRP[4]	Bit 3: BRP[3]	Bit 2: BRP[2]	Bit 1: BRP[1]	Bit 0: BRP[0]	Description
0	0	0	0	0	0	0	0	2 × peripheral bus clock (Initial value)
0	0	0	0	0	0	0	1	4 × peripheral bus clock
0	0	0	0	0	0	1	0	6 × peripheral bus clock
:	:	:	:	:	:	:	:	2 × (register value + 1) × peripheral bus clock
:	:	:	:	:	:	:	:	
1	1	1	1	1	1	1	1	512 × peripheral bus clock

[After change]

Bits 7 to 0—Baud Rate Pre-scale (BRP[7:0] = BCR0 [7:0]): These bits are used to define the peripheral bus clock periods contained in a Time Quantum.

Bit 7: BRP[7]	Bit 6: BRP[6]	Bit 5: BRP[5]	Bit 4: BRP[4]	Bit 3: BRP[3]	Bit 2: BRP[2]	Bit 1: BRP[1]	Bit 0: BRP[0]	Description
0	0	0	0	0	0	0	0	2 × peripheral bus clock (Initial value)
0	0	0	0	0	0	0	1	4 × peripheral bus clock
0	0	0	0	0	0	1	0	6 × peripheral bus clock
:	:	:	:	:	:	:	:	2 × (register value + 1) × peripheral bus clock
:	:	:	:	:	:	:	:	
0	1	1	1	1	1	1	1	512 × peripheral bus clock

The following description is added to section 22.9 "Usage Notes" in section 22 "Controller Area Network (RCAN-ET)".

[After change]

22.9 Usage Notes

22.9.1 Module Stop Mode

The clock supply to RCAN-ET can be stopped or started by using the standby control register 6 (STBCR6). With the initial value, the clock supply is stopped. Access to the RCAN-ET registers should be made only after releasing RCAN-ET from module stop mode.

22.9.2 Reset

RCAN-ET can be reset by hardware reset or software reset.

- Hardware reset
  RCAN-ET is reset to the initial state by power-on reset or on entering module stop mode.
- Software reset
  By setting the MCR0 bit in Master Control Register (MCR), RCAN-ET registers, excluding the MCR0 bit, and the CAN communication circuitry are initialized.

Since the IRR0 bit in Interrupt Request Register (IRR) is set by the initialization upon reset, it should be cleared while RCAN-ET is in configuration mode during the reset sequence.

The areas except for message control field 1 (CONTROL1) of mailboxes are not initialized by reset because they are in RAM. After power-on reset, all mailboxes should be initialized while RCAN-ET is in configuration mode during the reset sequence.

22.9.3 CAN Sleep Mode

In CAN sleep mode, the clock supply to the major parts in the module is stopped. Therefore, do not make access in CAN sleep mode except for access to the MCR, GSR, IRR, and IMR registers.

22.9.4 Register Access

If the mailbox area is accessed while the CAN communication circuitry in RCAN-ET is storing a received CAN bus frame in a mailbox, a 0 to five peripheral clock cycles of wait state is generated.

22.9.5 Interrupts

As shown in table 22.2, a Mailbox 0 receive interrupt can activate the DTC. If configured such that the DTC is activated by a Mailbox 0 receive interrupt and clearing of the interrupt source flag upon DTC transfer is enabled, use block transfer mode and read the whole Mailbox 0 message up to the message control field 1 (CONTROL1).

The description of the PB12MD[2:0] bits in "Port B Control Register L4 (PBCRL4)" in section 23.1.5 "Port B Control Registers H1 and L1 to L4 (PBCRH1 and PBCRL1 to PBCRL4)" of section 23 "Pin Function Controller (PFC)" on p. 1141 is corrected as follows.

[Before change]

Select the function of the PB12/$\overline{\text{CS1}}$/$\overline{\text{CS7}}$/IRQ1/TXD2/$\overline{\text{SC3}}$ pin.

[After change]

Select the function of the PB12/$\overline{\text{CS1}}$/$\overline{\text{CS7}}$/IRQ1/TXD2/$\overline{\text{CS3}}$ pin.

The description in section 24.1.3 "Port A Port Registers H and L (PAPRH and PAPRL)" of section 24 "I/O Ports" on p. 1281 is corrected as follows.

[Before change]

PAPRH and PAPRL are 16-bit readable/writable registers, which always return the states of the pins regardless of the PFC setting.

[After change]

PAPRH and PAPRL are 16-bit read-only registers, which return the states of the pins. However, when the SCIF function is selected for PA8, the TE bit in SCSCR is 0, and the SPB2IO bit in SCSPTR is 0, the states of the corresponding pins cannot be read out.

The description in section 24.4.3 "Port D Port Registers H and L (PDPRH and PDPRL)" of section 24 "I/O Ports" on p. 1310 is corrected as follows.

[Before change]

PDPRH and PDPRL are 16-bit read-only registers, which always return the states of the pins regardless of the PFC setting.

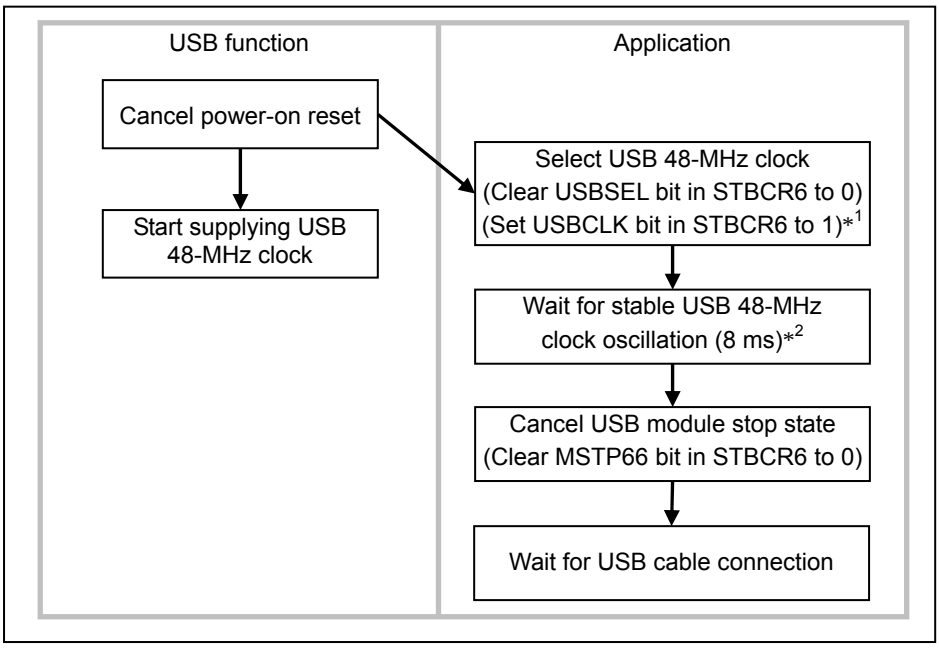
[After change]

PDPRH and PDPRL are 16-bit read-only registers, which return the states of the pins. However, when the SCIF function is selected for PD18, the TE bit in SCSCR is 0, and the SPB2IO bit in SCSPTR is 0, the states of the corresponding pins cannot be read out.

The following description is added to section 25.5 "Operation" in section 25 "USB Function Module" on p. 1349.

[After change]

25.5.1 Initial Settings



Notes: 1. This setting is not required when the ceramic resonator for USB is connected or the external 48-MHz clock is input.

2. The initial values of the USBSEL and USBCLK bits in STBCR6 immediately after a power-on reset are 0 and 1, respectively. Wait for the power-on oscillation settling time indicated in section 33.3.1, Clock Timing, before release from the power-on reset state. This secures the oscillation settling time for the 48-MHz USB clock. After halting the clock to change the values of the USBSEL and USBCLK bits, secure the oscillation settling time when restarting the clock.

The following description is added to section 26.1 "Features" in section 26 "Flash Memory" on p. 1381.

[After change]

- High-speed reading through ROM cache
  Both the user MAT and user boot MAT can be read at high speed through the ROM cache. They can be read only in on-chip ROM enabled mode.

The description in section 26.1 "Features" of section 26 "Flash Memory" on p. 1382 is corrected as follows.

[Before change]

The operating frequency for programming/erasing is 40 MHz (Pϕ).

[After change]

The operating frequency for programming/erasing is 50 MHz (Pϕ).

The following is added to table 26.2 "Comparison of Programming Modes" in section 26 "Flash Memory" on p. 1386.

[After change]

Table 26.2 Comparison of Programming Modes

	Boot Mode	User Program Mode	User Boot Mode*3	USB Boot Mode*3	Programmer Mode
Pin state	CK: output Other pins: input (same as the states in MCU extension mode 2) RxD1 and TxD1: valid	Dependent on user settings	CK: output (initial setting) Other pins: input (initial setting)	CK: output Other pins: input (same as the states in MCU extension mode 2)	Programmer dedicated pins

Table 26.4 (1) "Register Configuration" in section 26 "Flash Memory" on p. 1392 is corrected as follows.

[Before change]

Table 26.4 (1) Register Configuration

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size
Flash code control and status register	FCCS	R, W*1	H'00*2 H'80*2	H'FFFFA800	8
Flash program code select register	FPCS	R/W	H'00	H'FFFFA801	8
Flash erase code select register	FECS	R/W	H'00	H'FFFFA802	8
Flash key code register	FKEY	R/W	H'00	H'FFFFA804	8
Flash MAT select register	FMATS	R/W	H'00*3 H'AA*3	H'FFFFA805	8
Flash transfer destination address register	FTDAR	R/W	H'00	H'FFFFA806	8

[After change]

Table 26.4 (1) Register Configuration

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size
Flash code control and status register	FCCS	R, W*1	H'00*2 H'80*2	H'FFFFA800	8
Flash program code select register	FPCS	R/W	H'00	H'FFFFA801	8
Flash erase code select register	FECS	R/W	H'00	H'FFFFA802	8
Flash key code register	FKEY	R/W	H'00	H'FFFFA804	8
Flash MAT select register	FMATS	R/W	H'00*3 H'AA*3	H'FFFFA805	8
Flash transfer destination address register	FTDAR	R/W	H'00	H'FFFFA806	8
ROM cache control register	RCCR	R/W	H'00000001	H'FFFC1400	32

The following is added to section 26 "Flash Memory" on p. 1401.

[After change]

(7) ROM Cache Control Register (RCCR)

RCCR contains the RCF bit that controls the disabling of all lines in the ROM cache.

This register can be accessed only in longwords.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	RCF	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3	RCF	0	R/W	ROM Cache Flush Writing 1 to this bit disables (flushes) the instructions or data in the ROM cache. This bit is read as 0. 0: Does not disable the instructions or data in the ROM cache 1: Disables the instructions or data in the ROM cache [Clearing condition] • By a power-on reset or in standby mode [Setting condition] • Writing 1 to this bit
2, 1	—	All 0	R	Reserved The write value should always be 0; otherwise normal operation cannot be guaranteed.
0	—	1	R	Reserved The write value should always be 1; otherwise normal operation cannot be guaranteed.

The description in (2) Programming/Erasing Initialization, in section 26.4.3 "Programming/Erasing Interface Parameters" of section 26 "Flash Memory" on p. 1405 is corrected as follows.

[Before change]

(2.1) Flash Programming/Erasing Frequency Parameter (FPEFEQ: General Register R4 of CPU)

This parameter sets the operating frequency of the CPU.

The flash programming/erasing frequency of this LSI is limited to 40 MHz.

[After change]

(2.1) Flash Programming/Erasing Frequency Parameter (FPEFEQ: General Register R4 of CPU)

This parameter sets the operating frequency of the CPU.

For the operating frequency of this LSI, see section 31.3.1, Clock Timing.

The description in (3) Programming Execution, in section 26.4.3 "Programming/Erasing Interface Parameters" of section 26 "Flash Memory" on p. 1409 is corrected as follows.

[Before change]

2. The program data for the user MAT must be prepared in the consecutive area. The program data must be in the consecutive space which can be accessed by using the MOV.B instruction of the CPU and is not the flash memory space.

[After change]

2. The program data for the user MAT must be prepared in the consecutive area. The program data must be in the consecutive space which can be accessed by using the MOV.L instruction of the CPU and is not the flash memory space.

Table 26.7 in section 26.5.1 "Boot Mode" of section 26 "Flash Memory" on p. 1418 is corrected as follows.

[Before change]

Host Bit Rate	Peripheral Clock (Pϕ) Frequency That Can Automatically Adjust LSI's Bit Rate
9,600 bps	20 to 25 MHz
19,200 bps	

[After change]

Host Bit Rate	Peripheral Clock (Pϕ) Frequency That Can Automatically Adjust LSI's Bit Rate
9,600 bps	10 to 50 MHz
19,200 bps	

The description in figure 26.11 "Programming/Erasing Overview Flow" in section 26 "Flash Memory" on p. 1424 is corrected as follows.

[Before change]

2. Programming/erasing is executed only in the on-chip RAM. However, if the program data is in a consecutive area and can be accessed by the MOV.B instruction of the CPU like SRAM/ROM, the program data can be in an external space.

[After change]

2. Programming/erasing is executed only in the on-chip RAM. However, if the program data is in a consecutive area and can be accessed by the MOV.L instruction of the CPU like SRAM/ROM, the program data can be in an external space.

The description in (2) Programming Procedure in User Program Mode, in section 26.5.3 "User Program Mode" of section 26 "Flash Memory" on p. 1426 is corrected as follows.

[Before change]

Specify 1/4:1/4:1/4 (initial value) as the frequency division ratios of an internal clock (Iϕ), a bus clock (Bϕ), and a peripheral clock (Pϕ) through the frequency control register (FRQCR).

[After change]

Specify Iϕ = Bϕ = Pϕ as the frequency division ratios of an internal clock (Iϕ), a bus clock (Bϕ), and a peripheral clock (Pϕ) through the frequency control register (FRQCR).

The description in (2.6) in section 26.5.3 "User Program Mode" of section 26 "Flash Memory" on p. 1429 is corrected as follows.

[Before change]

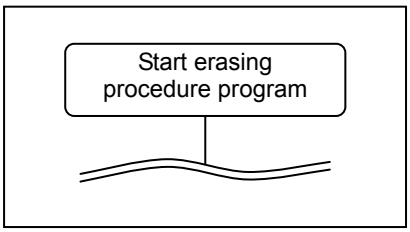
1. The current frequency of the CPU clock is set to the FPEFEQ parameter (general register R4). The settable Iϕ of the FPEFEQ parameter is 40 MHz.

[After change]

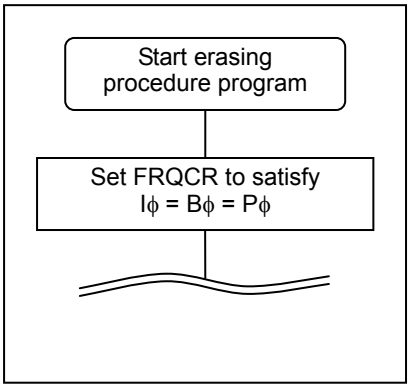
1. The current frequency of the CPU clock is set to the FPEFEQ parameter (general register R4). The settable FPEFEQ parameter is Iϕ ≤ 50 MHz.

Figure 26.14 "Erasing Procedure" in section 26 "Flash Memory" on p. 1432 is corrected as follows.

[Before change]



[After change]



The description in (3) Erasing Procedure in User Program Mode, in section 26.5.3 "User Program Mode" of section 26 "Flash Memory" on p. 1432 is corrected as follows.

[Before change]

The frequency division ratio of an internal clock (Iϕ), a bus clock (Bϕ), and a peripheral clock (Pϕ) is specified as 1/4:1/4:1/4 (initial value) by the frequency control register (FRQCR).

[After change]

The frequency division ratio of an internal clock (Iϕ), a bus clock (Bϕ), and a peripheral clock (Pϕ) is specified as Iϕ = Bϕ = Pϕ ≤ 50 MHz by the frequency control register (FRQCR).

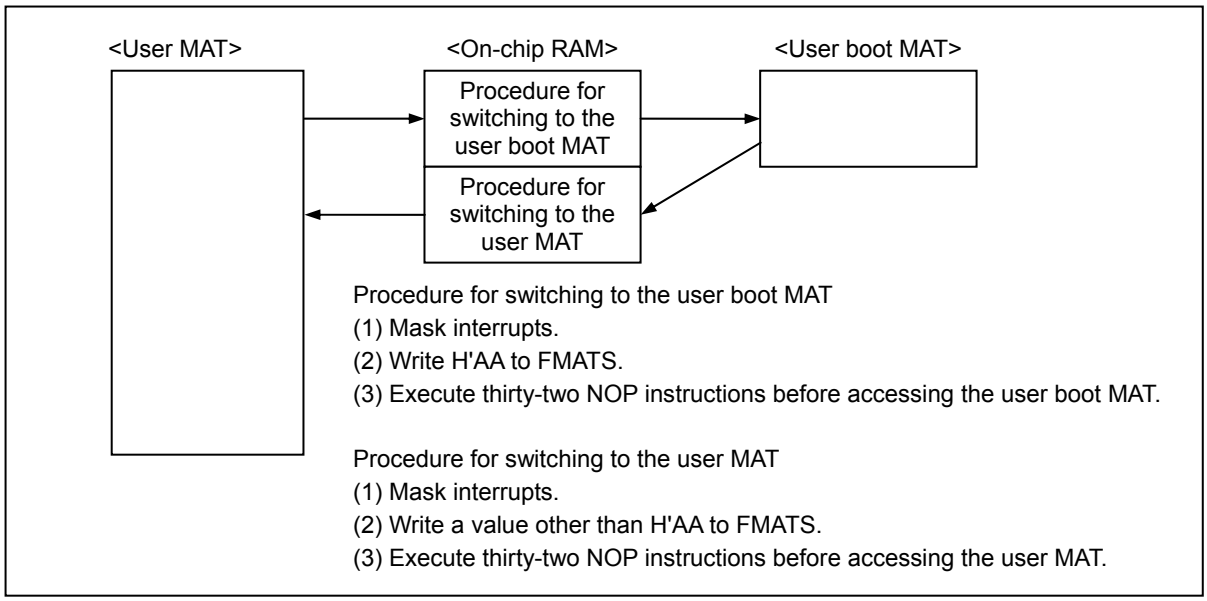
The following description is added to section 26.7.1 "Switching between User MAT and User Boot MAT" in section 26 "Flash Memory" on p. 1444.

[After change]

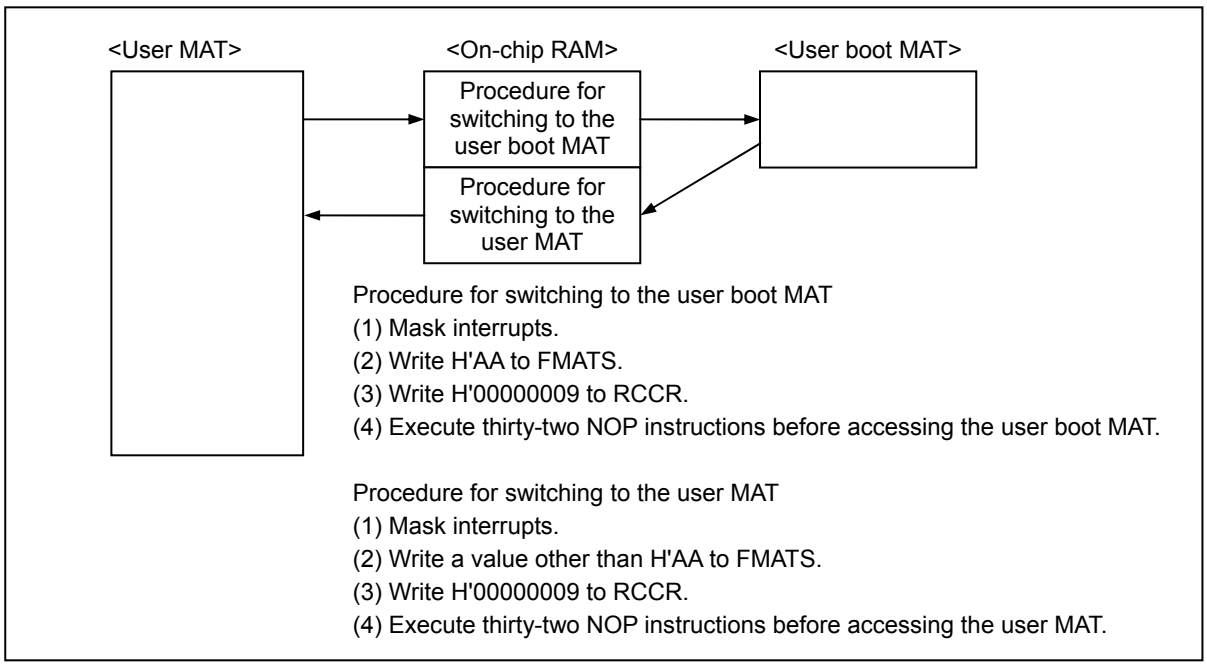
6. Disable (flush) the instructions or data cached in the ROM cache by writing 1 to the RCF bit in RCCR after the MATs have been switched.

Figure 26.19 "Switching between User MAT and User Boot MAT" in section 26 "Flash Memory" on p. 1445 is corrected as follows.

[Before change]



[After change]



The description in section 26.9 "Programmer Mode" of section 26 "Flash Memory" on p. 1488 is corrected as follows.

[Before change]

Use a PROM programmer that supports the Renesas 512-Kbyte flash memory on-chip MCU device type (ZTAT512DV5A/FZTAT1024DV5A)

[After change]

Use a PROM programmer that supports the Renesas 512-Kbyte flash memory on-chip MCU device type (FZTAT512DV5A/FZTAT1024DV5A).

The description of the FLC in section 30.1 "Register Addresses (by functional module, in order of the corresponding section numbers)" of section 30 "List of Registers" on p. 1543 and p.1544 is corrected as follows.

[Before change]

Module Name	Register Name	Abbreviation	Number of Bits	Address	Access Size
FLC	Flash code control and status register	FCCS	8	H'FFFFA800	8
	Flash program code select register	FPCS	8	H'FFFFA801	8
	Flash erase code select register	FECS	8	H'FFFFA802	8
	Flash key code register	FKEY	8	H'FFFFA804	8
	Flash MAT select register	FMATS	8	H'FFFFA805	8
	Flash transfer destination address register	FTDAR	8	H'FFFFA806	8

[After change]

Module Name	Register Name	Abbreviation	Number of Bits	Address	Access Size
FLC	Flash code control and status register	FCCS	8	H'FFFFA800	8
	Flash program code select register	FPCS	8	H'FFFFA801	8
	Flash erase code select register	FECS	8	H'FFFFA802	8
	Flash key code register	FKEY	8	H'FFFFA804	8
	Flash MAT select register	FMATS	8	H'FFFFA805	8
	Flash transfer destination address register	FTDAR	8	H'FFFFA806	8
	ROM cache control register	RCCR	32	H'FFFC1400	32

The FLASH registers in section 30.2 "Register Bits" of section 30 "List of Registers" on p. 1572 are corrected as follows.

[Before change]

Module Name	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 25/17/9/1
FLASH	FCCS	FWE	MAT	—	FLER	—	—	—	SCO
	FPCS	—	—	—	—	—	—	—	PPVS
	FECS	—	—	—	—	—	—	—	EPVB
	FKEY	K7	K6	K5	K4	K3	K2	K1	K0
	FMATS	MS7	MS6	MS5	MS4	MS3	MS2	MS1	MS0
	FTDAR	TDER	TDA6	TDA5	TDA4	TDA3	TDA2	TDA1	TDA0

[After change]

Module Name	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
FLASH	FCCS	FWE	MAT	—	FLER	—	—	—	SCO
	FPCS	—	—	—	—	—	—	—	PPVS
	FECS	—	—	—	—	—	—	—	EPVB
	FKEY	K7	K6	K5	K4	K3	K2	K1	K0
	FMATS	MS7	MS6	MS5	MS4	MS3	MS2	MS1	MS0
	FTDAR	TDER	TDA6	TDA5	TDA4	TDA3	TDA2	TDA1	TDA0
	RCCR	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	RCF	—	—	—

The FLASH register states in section 30.3 "Register States in Each Operating Mode" of section 30 "List of Registers" on p. 1588 are corrected as follows.

[Before change]

Module Name	Register	Power-on Reset	Manual Reset	Software Standby	Module Standby	Sleep
FLASH	FCCS	Initialized	Retained	Initialized	Initialized	Retained
	FPCS	Initialized	Retained	Initialized	Initialized	Retained
	FECS	Initialized	Retained	Initialized	Initialized	Retained
	FKEY	Initialized	Retained	Initialized	Initialized	Retained
	FMATS	Initialized	Retained	Initialized	Initialized	Retained
	FTDAR	Initialized	Retained	Initialized	Initialized	Retained

[After change]

Module Name	Register	Power-on Reset	Manual Reset	Software Standby	Module Standby	Sleep
FLASH	FCCS	Initialized	Retained	Initialized	—	Retained
	FPCS	Initialized	Retained	Initialized	—	Retained
	FECS	Initialized	Retained	Initialized	—	Retained
	FKEY	Initialized	Retained	Initialized	—	Retained
	FMATS	Initialized	Retained	Initialized	—	Retained
	FTDAR	Initialized	Retained	Initialized	—	Retained
	RCCR	Initialized	Retained	Retained	Retained	Retained

Table 31.1 "Absolute Maximum Ratings" in section 31 "Electrical Characteristics" on p. 1591 is corrected as follows.

[Before change]

Item	Symbol	Value	Unit
Power supply voltage (Internal)	DrV_{CC}	–0.3 to +4.3	V

[After change]

Item	Symbol	Value	Unit
Power supply voltage (Internal)	DrV_{CC}	–0.3 to +7.0	V

Table 31.2 "DC Characteristics (1) [Common Items]" in section 31 "Electrical Characteristics" on p. 1592 and p. 1593 is corrected as follows.

[Before change]

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog power supply current	During A/D or D/A conversion	AI_{CC}	—	3.0	5.0	mA	Per 1 module
	Waiting for A/D or D/A conversion		—	30	50	μA	Per 1 module
Reference power supply current	During A/D or D/A conversion		—	2.0	3.0	mA	Per 1 module
	Waiting for A/D or D/A conversion		—	1.5	2.0	mA	Per 1 module

[After change]

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog power supply current	During A/D or D/A conversion	AI_{CC}	—	3.0	5.0	mA	Per 1 module
	Waiting for A/D or D/A conversion		—	30	50	μA	Per 1 module
Reference power supply current	During A/D or D/A conversion	AI_{ref}	—	2.0	3.0	mA	Per 1 module
	Waiting for A/D or D/A conversion		—	1.5	2.0	mA	Per 1 module

The following items are added to table 31.7 "Bus Timing" in section 31 "Electrical Characteristics".

[After change]

		Bϕ = 50 MHz*			
Item	Symbol	Min.	Max.	Unit	Figure
Read data access time	t_{ACC}	$t_{cyc}(n + 1.5) - 32$	—	ns	Figures 31.10 to 31.13
Access time from read strobe	t_{OE}	$t_{cyc}(n + 1) - 32$	—	ns	Figures 31.10 to 31.13

Table 31.10 "MTU2, MTU2S Module Timing" in section 31 "Electrical Characteristics" on p. 1635 is corrected as follows.

[Before change]

Note: t_{pcyc} indicates peripheral clock (Pϕ) cycle.

[After change]

Note: t_{pcyc} indicates peripheral clock (Pϕ) cycle. The MTU2S operates on Mϕ.