To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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Date: Jan. 05, 2010

RENESAS TECHNICAL UPDATE

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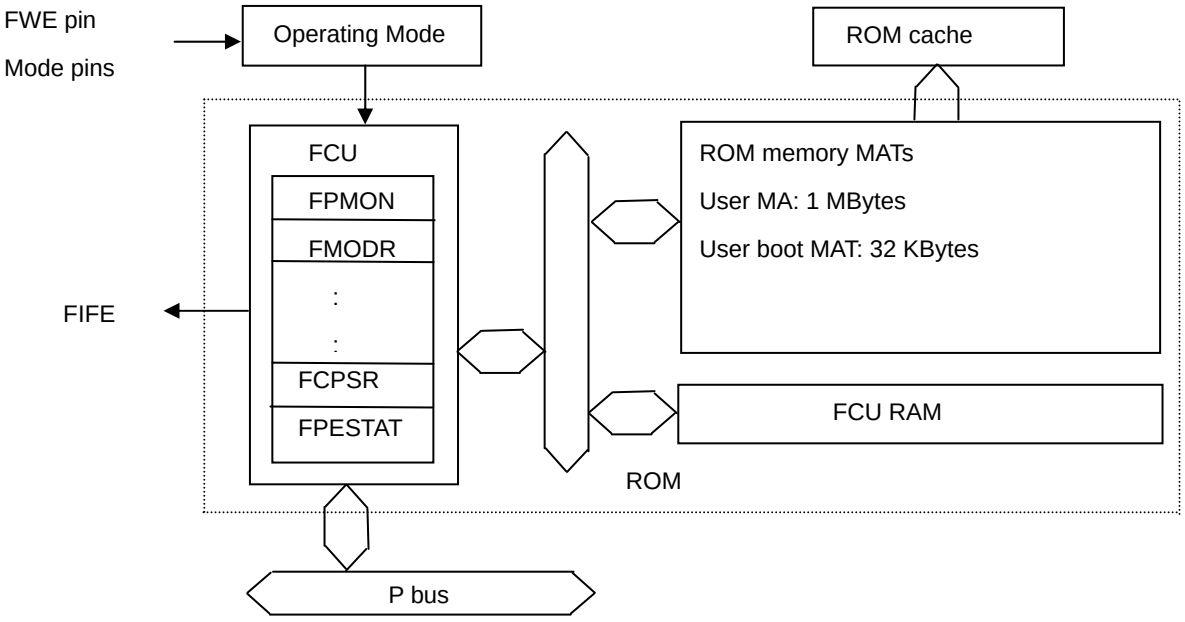
Product Category	MPU MCU		Document No.	TN-SH7-A761A/E	Rev.	1.00
Title	Correction of errors in SH7216 Group Hardware Manual		Information Category	Technical Notification		
Applicable Product	SH7216 Group SH7214 Group	Lot No. after 0948(EIA code)	Reference Document	SH7216 Group Hardware Manual Rev. 1.01 (REJ09B0543-0101)		

We would like to inform you that errors have been found in the hardware manuals of applicable products mentioned above.

For details, see below.

"Figure 27.2, Block Diagram of ROM" on page 1439 in section 27, Flash Memory (ROM), was amended as follows.

[Before Change]



[Legend]

FPMON : Flash pin monitor register

:

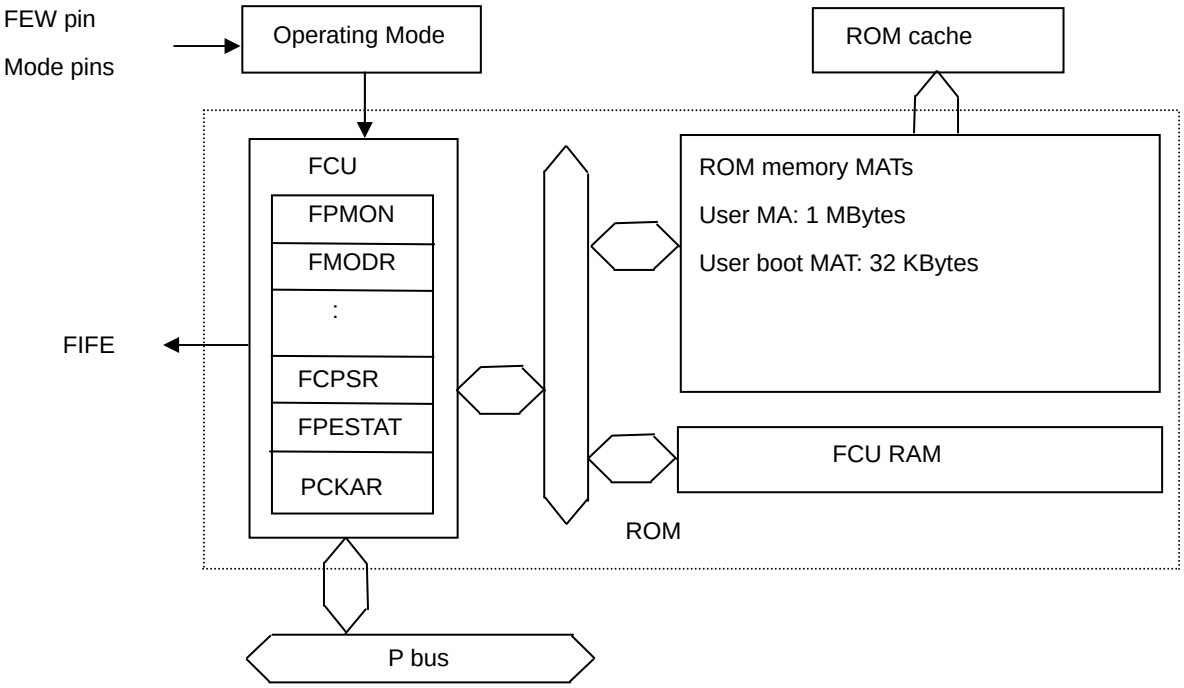
:

FPESTAT : Flash P/E status register

FIFE : Flash interface error interrupt

Figure 27.2 Block Diagram of ROM

[After Change]



[Legend]

FPMON : Flash pin monitor register

:

:

FPESTAT : Flash P/E status register

PCKAR : Peripheral clock notification register

FIFE : Flash interface error interrupt

Figure 27.2 Block Diagram of ROM

The following register was added to “table 27.2, Register Configuration” on page 1832 in section 27, Flash Memory (ROM).

Table 27.2 Register Configuration

Register Name	Symbol	R/W*[1]	Initial Value	Address	Access Size
Peripheral clock notification register	PCKAR	R/W	H'0000*[5]	H'FFFFA938	8, 16

The following command was added to “table 27.3, FCMDR Status after a Command is Accepted” on page 1461 in section 27, Flash Memory (ROM).

Table 27.3 FCMDR Status after a Command is Accepted

Command	CMDR	PCMDR
Peripheral clock notification	H'E9	Previous command

The following description was added as “section 27.3, Register Descriptions” in section 27, Flash Memory (ROM).

[After Change]

27.3.16 Peripheral Clock Notification Register (PCKAR)

PCKAR is used to notify the sequencer of information regarding the frequency setting of the peripheral clock (Pϕ) for programming or erasure of the ROM or data flash memory. The setting governs the time programming or erasure takes. In modes where the internal ROM is disabled, the value read from the PCKAR will be H'0000 and writing to the PCKAR will be ineffective. PCKAR is initialized by a power-on reset or by writing 1 to the PRESET bit in FRESETR.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	PCKA[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 8	-	0	R	Reserved These bits are always read as 0. When writing to the register, always write 0 to these bits. Operation is not guaranteed if 1 is written to any or all of these bits.
7 to 1	PCKA[7:0]	0	R/W	Peripheral Clock Notification These bits are used to notify the peripheral clock (Pϕ) for programming or erasure of the ROM or data flash memory. Set the frequency of Pϕ by setting these bits before programming or erasure, and then issue a peripheral clock notification command. Do not change the frequency while the ROM or data flash memory is being programmed or erased. Follow the procedure below to calculate the setting. 1. Convert the frequency expressed in MHz units to binary notation, and write the value to the PCKA[7:0] bits. For example, if the frequency of the peripheral clock is 35.9 MHz, the setting is derived as follows. 2. Round 35.9 up to obtain 36. 3. Convert 36 into binary form, producing H'00 as the higher-order byte and H'24 (B'0010 0100) as the lower-order byte, and set the PCKA[7:0] bits to this value. Notes 1. Do not issue the command for overwriting the ROM or data flash memory if the setting of the PCKA[7:0] bits is for a frequency outside the range from 20 to 50 MHz. 2. If the frequency set by the PCKA[7:0] bits differs from the actual frequency, there is a possibility of destroying the ROM or data flash memory.

The following command was added to “table 27.11, FCU Command List (ROM-Related Commands)” on page 1832 in section 27, Flash Memory (ROM).

[After Change]

Table 27.11 FCU Command List (ROM-Related Commands)

Command	Function
Peripheral clock notification	Notifies the sequencer of the peripheral clock frequency

"Table 27.12 FCU Command Format", on page 1507 in section 27, Flash Memory (ROM), was amended as follows.

[Before change]

Table 27.12 FCU Command Format

Command	Number of Bus Cycles	First Cycle		Second Cycle		Third Cycle		Fourth to 130th Cycles		131st Cycle	
		Address	Data	Address	Data	Address	Data	Address	Data	Address	Data
Normal mode transition	1	RA	H'FF	-	-	-	-	-	-	-	-
Status read mode transition	1	RA	H'70	-	-	-	-	-	-	-	-
Lock bit read mode transition (lock bit read 1)	1	RA	H'71	-	-	-	-	-	-	-	-
Program	131	RA	H'E8	RA	H'80	WA	WD1	RA	WDn	RA	H'D0
Block erase	2	RA	H'20	BA	H'D0	-	-	-	-	-	-
P/E suspend	1	RA	H'B0	-	-	-	-	-	-	-	-
P/E resume	1	RA	H'D0	-	-	-	-	-	-	-	-
Status register clear	1	RA	H'50	-	-	-	-	-	-	-	-
Lock bit read 2	2	RA	H'71	BA	H'D0	-	-	-	-	-	-
Lock bit program	2	RA	H'77	BA	H'D0	-	-	-	-	-	-

[After Change]

Table 27.12 FCU Command Format

Command	Number of Bus Cycles	First Cycle		Second Cycle		Third Cycle		Forth and Fifth Cycles		Sixth Cycle		Seventh to 130th Cycles		131st Cycle	
		Address	Data	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data
Normal mode transition	1	RA	H'FF	-	-	-	-	-	-	-	-	-	-	-	-
Status read mode transition	1	RA	H'70	-	-	-	-	-	-	-	-	-	-	-	-
Lock bit read mode transition (lock bit read 1)	1	RA	H'71	-	-	-	-	-	-	-	-	-	-	-	-
Program	131	RA	H'E8	RA	H'80	WA	WD1	RA	WDn	RA	WDn	RA	WDn	RA	H'D0
Block erase	2	RA	H'20	BA	H'D0	-	-	-	-	-	-	-	-	-	-
P/E suspend	1	RA	H'B0	-	-	-	-	-	-	-	-	-	-	-	-
P/E resume	1	RA	H'D0	-	-	-	-	-	-	-	-	-	-	-	-
Status register clear	1	RA	H'50	-	-	-	-	-	-	-	-	-	-	-	-
Lock bit read 2	2	RA	H'71	BA	H'D0	-	-	-	-	-	-	-	-	-	-
Lock bit program	2	RA	H'77	BA	H'D0	-	-	-	-	-	-	-	-	-	-
Peripheral clock notification	6	RA	H'E9	RA	H'03	WA	H'0F0F	WA	H'0F0F	RA	H'D0	-	-	-	-

The following command was added to “table 27.13 FCU Modes/States and Acceptable Commands” on page 1511 in section 27, Flash Memory (ROM).

[Before Change]

Table 27.13 FCU Modes/States and Acceptable Commands

	P/E Normal Mode			Status Read Mode							Lock Bit Read Mode		
Item	Programming-Suspended	Erasure-Suspended	Other State	Programming/Erasure Processing	Programming/Erasure Suspension Processing	Lock Bit Read 2 Processing	Programming-Suspended	Erasure-Suspended	Command-Locked	Other State	Programming-Suspended	Erasure-Suspended	Other State
FRDY bit in FSTATR0	1	1	1	0	0	0	1	1	0/1	1	1	1	1
:	:	:	:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:	:	:	:
Lock bit program	X	*	A	X	X	X	X	*	X	A	X	*	A

[After Change]

Table 27.13 FCU Modes/States and Acceptable Commands

	P/E Normal Mode			Status Read Mode							Lock Bit Read Mode		
Item	Programming-Suspended	Erasure-Suspended	Other State	Programming/Erasure Processing	Programming/Erasure Suspension Processing	Lock Bit Read 2 Processing	Programming-Suspended	Erasure-Suspended	Command-Locked	Other State	Programming-Suspended	Erasure-Suspended	Other State
FRDY bit in FSTATR0	1	1	1	0	0	0	1	1	0/1	1	1	1	1
:	:	:	:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:	:	:	:
Lock bit program	×	*	A	×	×	×	×	*	×	A	×	*	A
Peripheral clock notification	×	×	A	×	×	×	×	×	×	A	×	×	A

The description under “section 27.6.3, FCU Command Usage” on page 1512 in section 27, Flash Memory (ROM), was amended as follows.

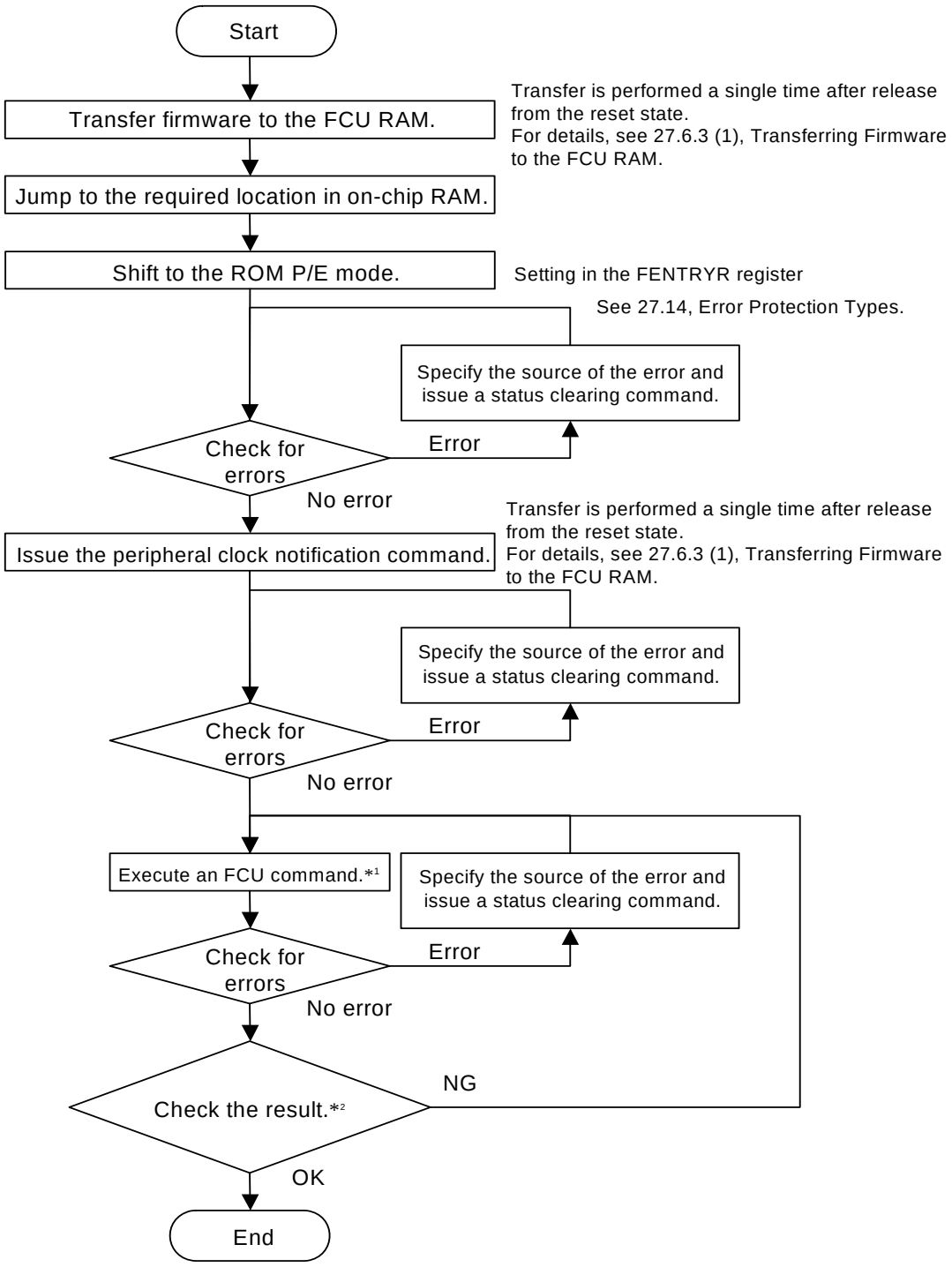
[Before Change]

The state of error occurrence can be checked via the ILGLERR, ERSERR, and PRGERR bits.

[After Change]

The state of error occurrence can be checked via the ILGLERR, ERSERR, and PRGERR bits.

Figure 27.16 gives an overview of the flow of processing for programming and erasure.



Notes: 1. This is a program, block erase, lock-bit program, or lock-bit read 2 command.
2. To confirm the result of programming or erasure, place the ROM in ROM-read mode and then read the data. For details, see 27.6.3(4), Transition to ROM-read mode.

Figure 27.16 Overview of the Flow of Processing for Programming and Erasure

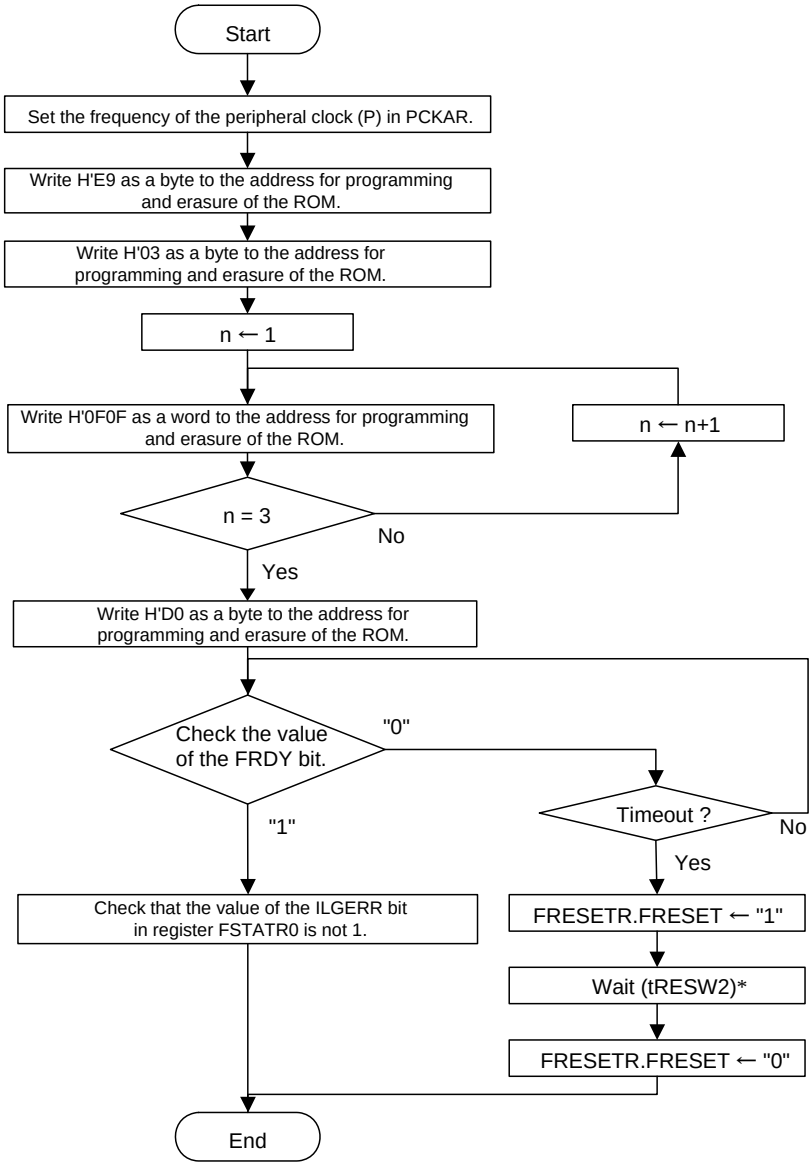
The following description was added as “(4) Using the peripheral clock notification command” on page 1514 in section 27, Flash Memory (ROM).

[After Change]

The frequency of the peripheral clock to be used for programming or erasure of the flash memory (ROM) must be set in the PCKAR. Selectable values are in the range from 20 to 50 MHz. If the setting is not in this range, the FCU detects an error and enters the command-locked state (see section 27.9.3, Error Protection).

The peripheral clock notification command is used after setting the PCKAR register. For a peripheral clock notification command, H'E9 and H'03 are written in byte units in the first and second cycles, respectively, to the address for programming or erasure of the ROM. In the third to fifth cycles of the command, writing is executed in word units. As the first address, use an address that is aligned with a four-byte boundary. After H'0F0F has been written as a word unit three times to the address for programming or erasure of the ROM, when H'D0 is written as a byte unit to the address for programming or erasure of the ROM, the FCU starts processing for setting the frequency of the peripheral clock. Completion of the setting can be confirmed by checking the value of the FRDY bit in the FSTATR0 register.

After release from the reset state, if the peripheral clock settings in use are not changed, execution once makes the setting valid for subsequent FCU commands.



Note: tRESW2 denotes the width of a reset pulse during programming or erasure (see section 33.3.2, Control Signal Timing, in section 33, Electrical Characteristics).

Figure 27.18 Flow for Using the Peripheral Clock Notification Command

“Table 27.14, Error Protection Types” on page 1536 in section 27, Flash Memory (ROM), was amended as follows.

[Before Change]

Table 27.14 Error Protection Types

Error	Description	ILGLERR	ERSERR	PRGERR	FCUERR	ROMAE
Illegal command error	An undefined code has been specified in the first cycle of an FCU command.	1	0	0	0	0
	The value specified in the last of the multiple cycles of an FCU command is not H'D0.	1	0	0	0	0
	The command issued during programming or erasure is not a suspend command.	1	0	0	0	0
	:					
	:					
	A command has been issued in command-locked state.	1	0/1	0/1	0/1	0/1

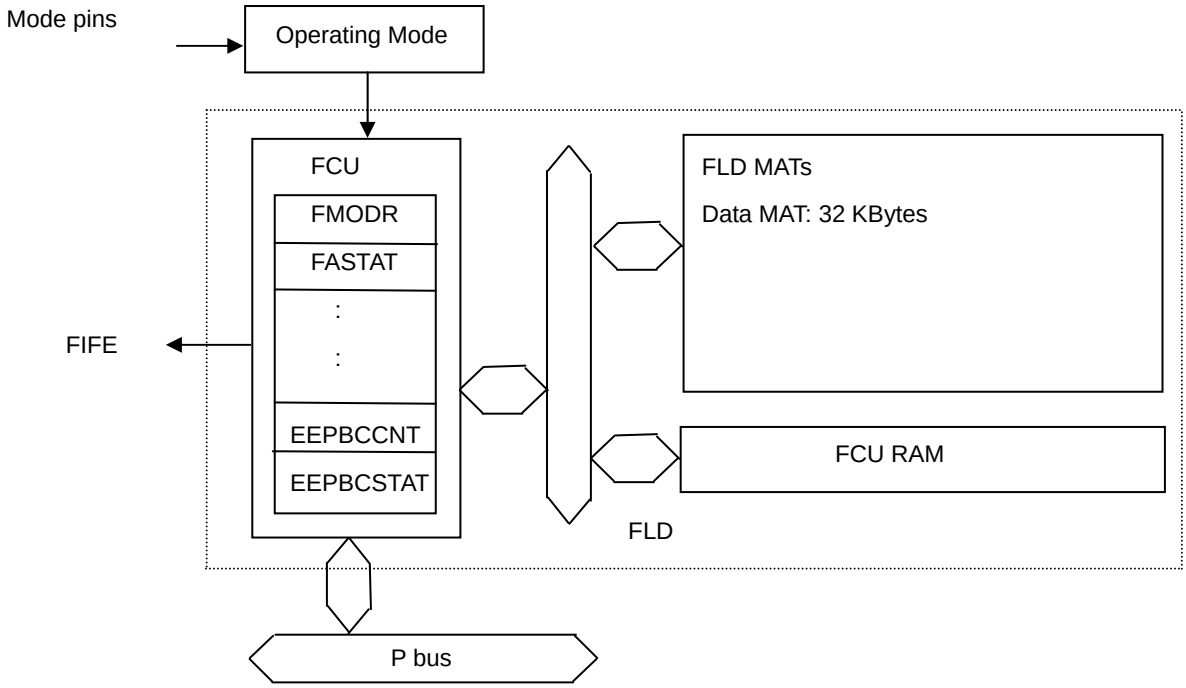
[After Change]

Table 27.14 Error Protection Types

Error	Description	ILGLERR	ERSERR	PRGERR	FCUERR	ROMAE
Illegal command error	An undefined code has been specified in the first cycle of an FCU command.	1	0	0	0	0
	The value specified in the last of the multiple cycles of an FCU command is not H'D0.	1	0	0	0	0
	The peripheral clock specified in the PCKAR register is not in the range from 20 to 50 MHz.	1	0	0	0	0
	The command issued during programming or erasure is not a suspend command.	1	0	0	0	0
	:					
	:					
	A command has been issued in command-locked state.	1	0/1	0/1	0/1	0/1

"Figure 28.2, Block Diagram of FLD" on page 1547, in section 28, Data Flash (FLD), was amended as follows.

[Before Change]



[Legend]

FMODR: Flash mode register

:

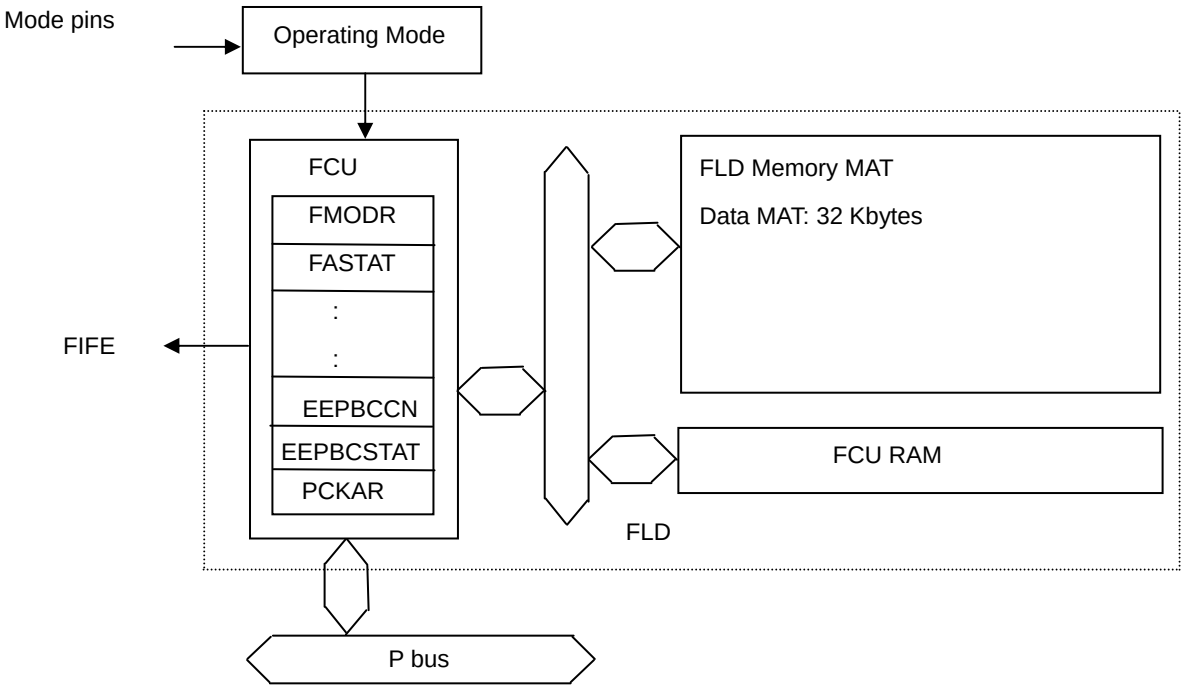
:

EEPBCSTAT: FLD blank check status register

FIFE: Flash interface error interrupt

Figure 28.2 Block Diagram of FLD

[After Change]



[Legend]

FMODR: Flash mode register

:

:

EEPBCSTAT: FLD blank check status register

PCKAR: Peripheral clock notification register

FIFE: Flash interface error interrupt

Figure 28.2 Block Diagram of FLD

The following register was added to “table 28.2, Register Configuration” on page 1551 in section 28, Data Flash (FLD).

[After Change]

Table 28.2 Register Configuration

Register Name	Symbol	R/W*[1]	Initial Value	Address	Access Size
Peripheral clock notification register	PCKAR	R/W	H'0000*[5]	H'FFFFA938	8, 16

The following command was added to “table 28.6, FCU Commands List (FLD-Related Commands)” on page 1571 in section 28, Data Flash (FLD).

[After Change]

Table 28.6 FCU Commands List (FLD-Related Commands)

Command	Function
Peripheral clock notification	Notifies the sequencer of the peripheral clock frequency

The following command was added to “table 28.8, FCU Modes/States and Acceptable Commands” on page 1576 in section 28, Data Flash (FLD).

[Before Change]

Table 28.8 FCU Modes/States and Acceptable Commands

	P/E Normal Mode			Status Read Mode							Lock Bit Read Mode		
Item	Programming-Suspended	Erasure-Suspended	Other State	Programming/Erasure Processing	Programming/Erasure Suspension Processing	Blank Check Processing	Programming-Suspended	Erasure-Suspended	Command-Locked	Other State	Programming-Suspended	Erasure-Suspended	Other State
FRDY bit in FSTATR0	1	1	1	0	0	0	1	1	0/1	1	1	1	1
:	:	:	:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:	:	:	:
Blank check	A	A	A	×	×	×	A	A	×	A	A	A	A

[After Change]

Table 28.8 FCU Modes/States and Acceptable Commands

	P/E Normal Mode			Status Read Mode							Lock Bit Read Mode		
Item	Programming-Suspended	Erasure-Suspended	Other State	Programming/Erasure Processing	Programming/Erasure Suspension Processing	Blank Check Processing	Programming-Suspended	Erasure-Suspended	Command-Locked	Other State	Programming-Suspended	Erasure-Suspended	Other State
FRDY bit in FSTATR0	1	1	1	0	0	0	1	1	0/1	1	1	1	1
:	:	:	:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:	:	:	:
Blank check	A	A	A	×	×	×	A	A	×	A	A	A	A
Peripheral clock notification	×	×	A	×	×	×	×	×	×	A	×	×	A

The following description was added under “28.6.3, FCU Command Usage” on page 1577 in section 28, Data Flash (FLD).

[After Change]

(1) Using the peripheral clock notification command

The command is used for notification of the peripheral clock frequency. For details, see section 27.6.3, Using FCU Commands, in section 27, Flash Memory (ROM). Proceed by setting the FENTRYD bit in the FENTRYR register to 1 and specifying the address as an address within the region corresponding to the data-flash memory.