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RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-SH7-A917A/E	Rev.	1.00
Title	Clearing condition of PER and DER bits in Direct Memory Access Controller for Local Bus and Peripheral Modules (LBSC-DMAC/HPB-DMAC)		Information Category	Technical Notification		
Applicable Products	SH7734	Lot No. All lots	Reference Document	SH7734 User's Manual: Hardware Rev.1.00 (R01UH0233EJ0100)		

We would like to inform you of a usage note regarding the clearing condition of the UltraATA Error Indication Register bit of the Direct Memory Access Controller for Local Bus and Peripheral Modules (LBSC-DMAC/HPB-DMAC) descried in the SH7734 User's Manual: Hardware.

The description on Table 6A.2 (1), List of LBSC-DMAC Registers, has been corrected as shown below.

[Before change]

Address (Bytes)	Name	Abbreviation	Access Type	Access Size
H'FF8014CC	[Common to LBSC-DMAC] UltraATA error indication register	UATTER	R/W	32

[After change]

Address (Bytes)	Name	Abbreviation	Access Type	Access Size
H'FF8014CC	[Common to LBSC-DMAC] UltraATA error indication register	UATTER	R/WC1	32

The description on section 6A.4.32, UltraATA Error Indication Register (UATTER), has been corrected as shown below.

[Before change]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PER	DER
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	PER	0	R/W	Indicates whether PIO access is executed for the area allocated to the ATA space during UltraATA DMA operation. (The PIO access attempted for the area allocated to the ATA space during UltraATA DMA operation is ignored.) 0: No PIO access has been executed for the area allocated to the ATA space during UltraATA DMA operation. 1: PIO access has been executed for the area allocated to the ATA space during UltraATA DMA operation.
0	DER	0	R/W	Indicates whether timeout occurs due to a temporary communication stop (no change in DSTROBE) during UltraATA DMA read operation. The timeout period is specified through UATTSR and UATMR2. (When reading) 0: No timeout error has occurred. 1: A timeout error has occurred (interrupt is generated when enabled through UATIER). (When writing) No timeout detection.

Note: For the UltraATA DMA operation, refer to section 6B, LBSC within Bus Bridge.

[After change]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PER	DER
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/WC1	R/WC1

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	PER	0	R/WC1	Indicates whether PIO access is executed for the area allocated to the ATA space during UltraATA DMA operation. (The PIO access attempted for the area allocated to the ATA space during UltraATA DMA operation is ignored.) 0: No PIO access has been executed for the area allocated to the ATA space during UltraATA DMA operation. 1: PIO access has been executed for the area allocated to the ATA space during UltraATA DMA operation. [Clearing condition] Writing 1 to this bit clears the flag. Writing 0 to this bit is ignored. 0 should be written to this bit except for when clearing this bit.
0	DER	0	R/WC1	Indicates whether timeout occurs due to a temporary communication stop (no change in DSTROBE) during UltraATA DMA read operation. The timeout period is specified through UATTSR and UATMR2. (When reading) 0: No timeout error has occurred. 1: A timeout error has occurred (interrupt is generated when enabled through UATIER). (When writing) No timeout detection. [Clearing condition] Writing 1 to this bit clears the flag. Writing 0 to this bit is ignored. 0 should be written to this bit except for when clearing this bit.

Note: For the UltraATA DMA operation, refer to section 6B, LBSC within Bus Bridge.

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