

To our customers,

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## Old Company Name in Catalogs and Other Documents

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On April 1<sup>st</sup>, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: <http://www.renesas.com>

April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

Send any inquiries to <http://www.renesas.com/inquiry>.

# RENESAS TECHNICAL UPDATE

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan  
Renesas Technology Corp.

Product Category	MPU/MCU		Document No.	TN-SH7-A740A/E	Rev.	1.00
Title	Additional specs concerning SH7205 electric characteristic tRDH3		Information Category	Technical Notification		
Applicable Product	SH7205 Group	Lot No.	Reference Document	SH7205 Group Hardware Manual (REJ09B0372-0100)		
		All				

This is to notify you of the addition of the bus timing for read data hold time 3 (tRDH3) of electric characteristic of SH7205.

## (1) Addition to the Table 33.8 Bus Timing

[The contents before manual correction]

Table 33.8 Bus Timing

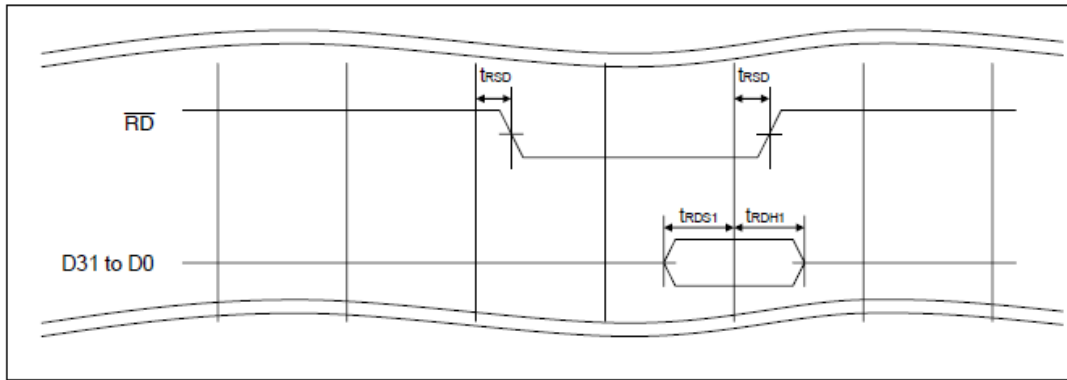
Item	Symbol	B $\phi$ =66.66MHz *		Unit	Figure
		Min.	Max.		
Read data hold time 2 (SDRAM space)	t <sub>RDH2</sub>	2	-	ns	Figures 33.16, 33.18, 33.20
Read/write mode delay time	t <sub>RWM</sub>	1	13	ns	Figures 33.11 to 33.15

[The contents after manual correction]

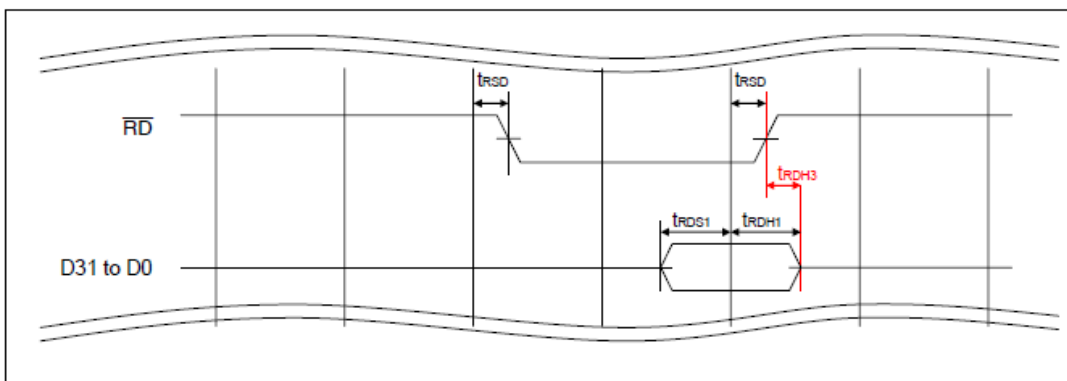
Item	Symbol	B $\phi$ =66.66MHz *		Unit	Figure
		Min.	Max.		
Read data hold time 2 (SDRAM space)	t <sub>RDH2</sub>	2	-	ns	Figures 33.16, 33.18, 33.20
Read data hold time 3 (external space)	t <sub>RDH3</sub>	0	-	ns	Figures 33.11 to 33.13, 33.15
Read/write mode delay time	t <sub>RWM</sub>	1	13	ns	Figures 33.11 to 33.15

(2) Figure 33.11 External Address Space: Basic Bus Timing (Normal Access, Cycle Wait Control, CS Extended Cycle)

[The contents before manual correction]

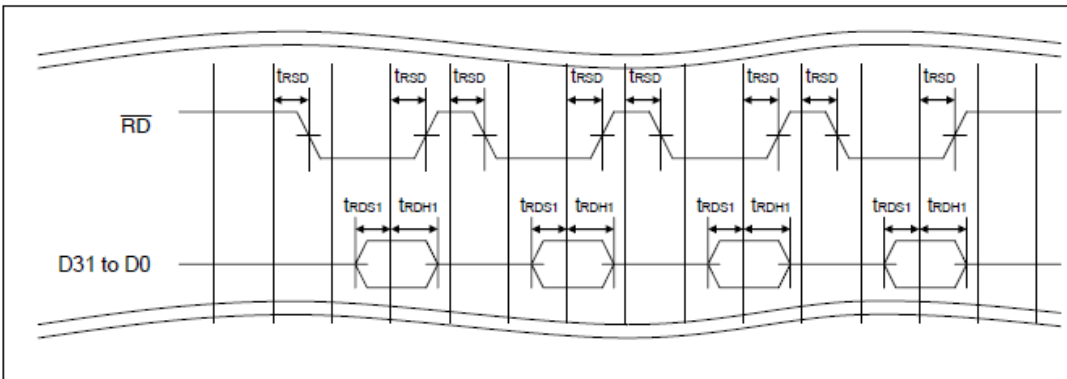


[The contents after manual correction]

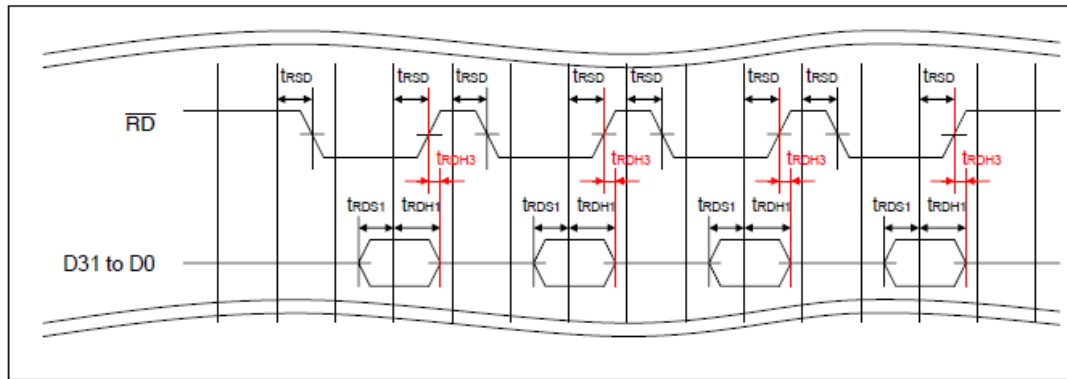


(3) Figure 33.12 External Address Space: Basic Bus Timing (Page Read Access, Normal Access Compatible Mode)

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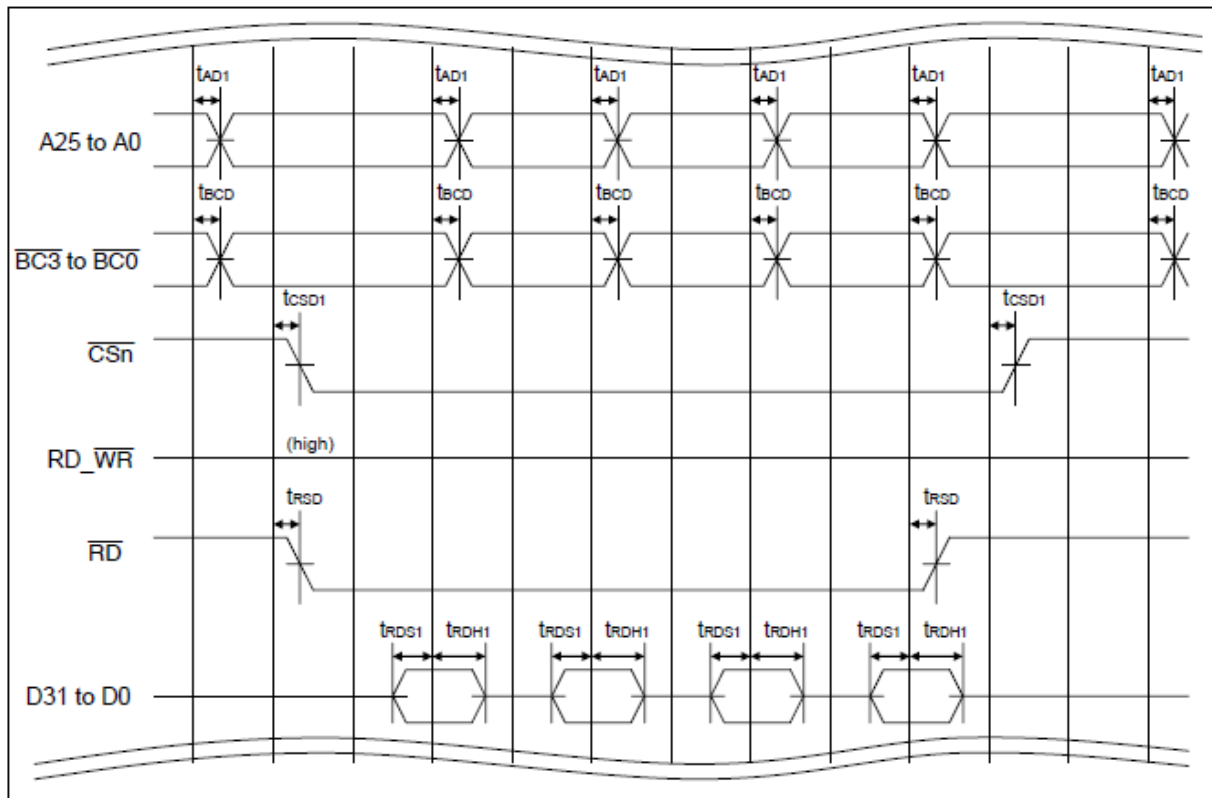


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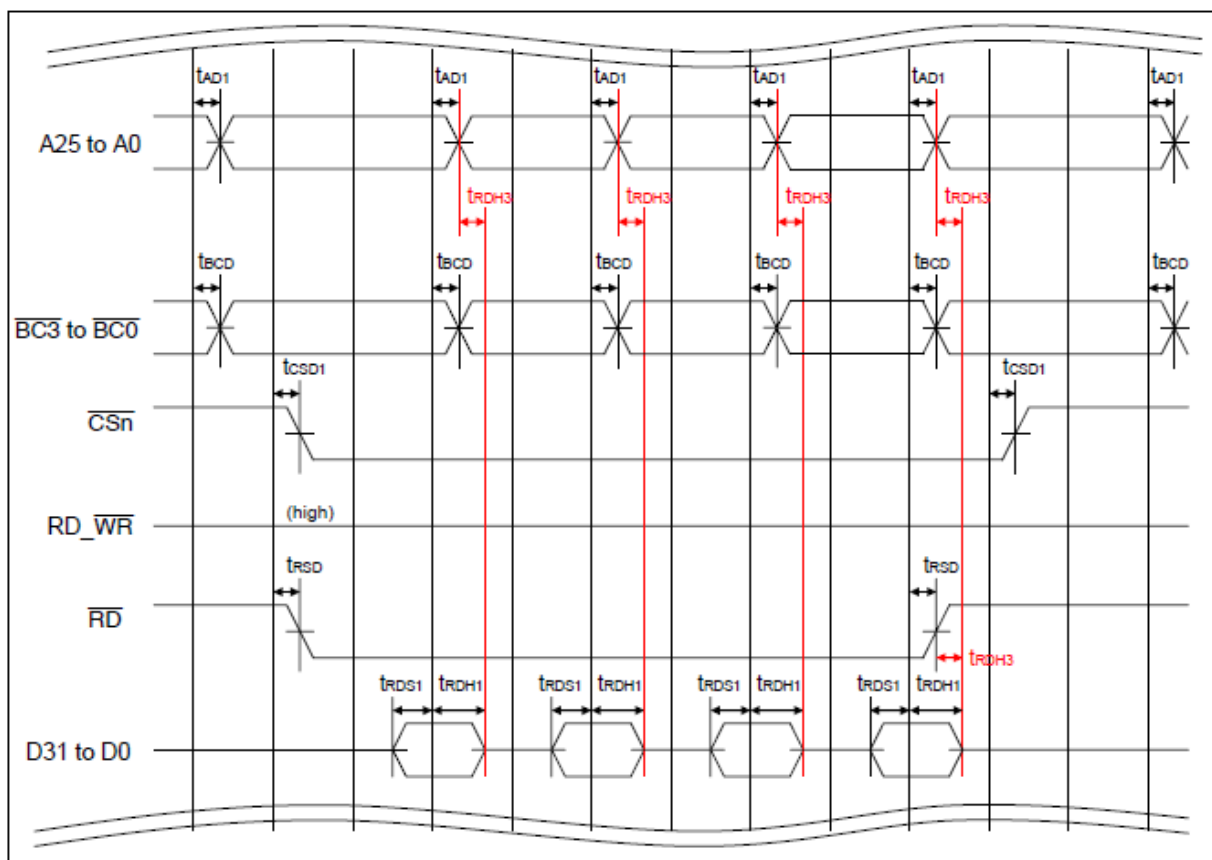


(4) Figure 33.13 External Address Space: Basic Bus Timing (Page Read Access, External Read Data Continuous Assert Mode)

[The contents before manual correction]

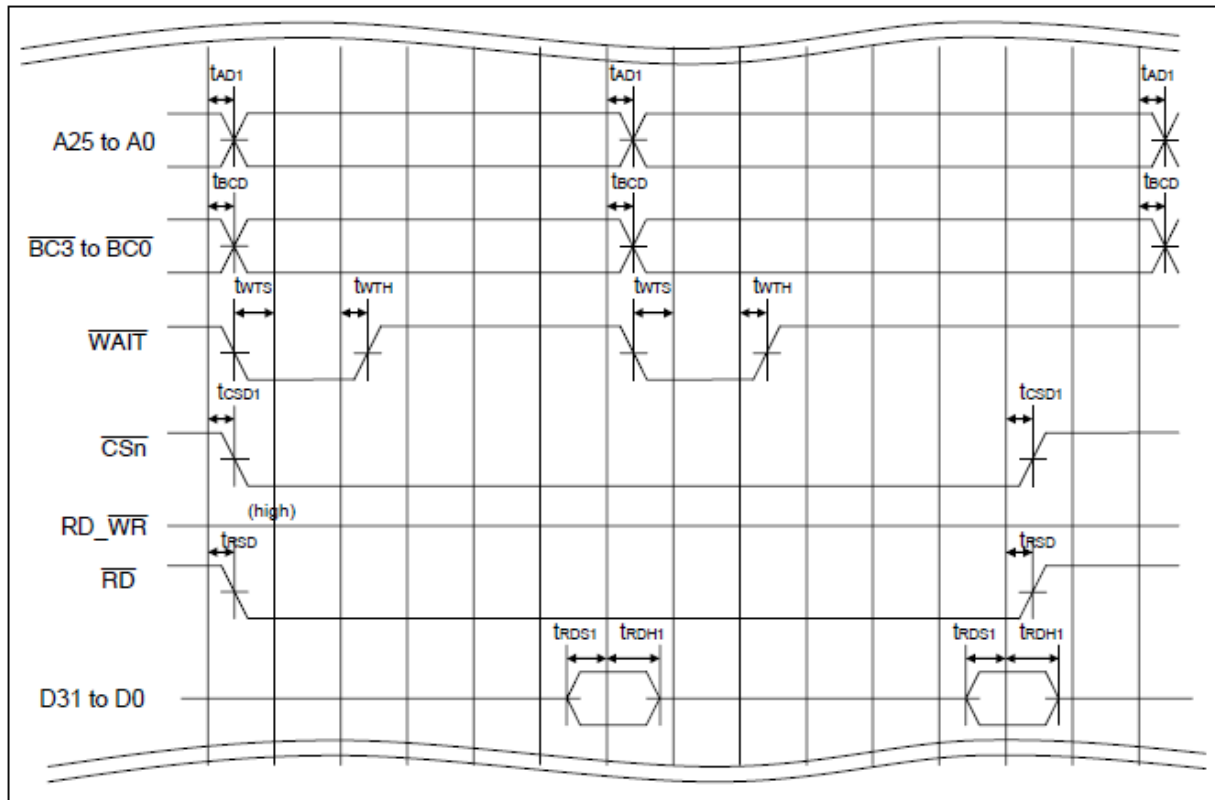


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(5) Figure 33.15 External Address Space: Timing with External Wait (Page Read Access to 16-bit Width Channel, External Read Data Continuous Asser Mode)

[The contents before manual correction]



[The contents after manual correction]

