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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SH7-A895A/E	Rev.	1.00
Title	Addition of the description about the minimum number of idle cycles on the internal bus of the bus state controller (BSC)		Information Category	Technical Notification		
Applicable Product	SH7231 Series	Lot No. All lots	Reference Document	SH7231 Group User's Manual: Hardware (R01UH0073EJ0200)		

We would like to inform you of the corrections in the minimum number of idle cycles on the internal bus of the bus state controller (BSC) in the above applicable products.

[Correction of Errors in the User's Manual]

10.5.10 Wait between Access Cycles

[Before correction (p.411)]

Table 10.20 Minimum Number of Idle Cycles on Internal Bus (CPU Operation)

CPU Operation	Clock Ratio (Iϕ:Bϕ)			
	8:1	4:1	2:1	1:1
Write → write	1	2	2	3
Write → read	0	0	0	1
Read → write	1	2	2	3
Read → read	0	0	0	1

[After correction]

Table 10.20 Minimum Number of Idle Cycles on Internal Bus (CPU Operation)

CPU Operation	Clock Ratio (Iϕ:Bϕ)			
	8:1	4:1	2:1	1:1
Write → write	0	0	0	0
Write → read	0	0	0	0
Read → write	1 or 0*1	1 or 0*1	2 or 0*1	3 or 0*1
Read → read	0	0	0	0

Operating conditions:

1. The bits for setting the idle cycles between access cycles in CS1BCR and CS2BCR are all set to 0.
2. In CS1WCR and CS2WCR, the WM bit is set to 1 (external $\overline{\text{WAIT}}$ pin disabled), the SW[1:0] bits are set to 00 ($\overline{\text{CS}}$ assertion is not extended), and the HW[1:0] bits are set to 00 ($\overline{\text{CS}}$ negation is not extended).
3. For both the CS1 and CS2 spaces, SRAM devices are connected, the bit width is 16 bits.
4. The unit of access by the CPU data transfer instructions is 16 bits (MOV.W).

Note: 1. This is the case where fetching of an instruction from the external bus (through the F bus) is followed by a data transfer instruction writing to the external bus (through the M bus).

[Before correction (p.411)]

Table 10.21 Minimum Number of Idle Cycles on Internal Bus (DMAC Operation)

DMAC Operation	Transfer Mode	
	Dual Address	Single Address
Write → write	0	2
Write → read	0 or 2	0
Read → write	0	0
Read → read	0	2

Notes: 1. The write → write and read → read columns in dual address transfer indicate the cycles in the divided access cycles.

2. For the write → read cycles in dual address transfer, 0 is applicable when different channels are activated successively and 2 is applicable when the same channel is activated successively. When a DMAC activation request is issued from an on-chip peripheral module and the activation is made successively in burst mode, the number of cycle is 0 even when the same channel is activated successively.

3. The write → read and read → write columns in single address transfer indicate the case when different channels are activated successively. The "write" means transfer from a device with DACK to external memory and the "read" means transfer from external memory to a device with DACK.

[After correction]

Table 10.21 Minimum Number of Idle Cycles on Internal Bus (DMAC Operation)

DMAC Operation	Transfer Mode				
	Dual Address				
	Auto Request	Peripheral Module	External Request (Level, AM = 0)	External Request (Level, AM = 1)	External Request (Edge)
Write → write*3	2	2	4*1 or 2*2	9*1*4 or 2*2	4*1 or 2*2
Write → read*3	0	0	2*1 or 0*2	6*1*4 or 0*2	1*1 or 0*2
Read → write	0	0	0	0	0
Read → read	2	2	5*1 or 2*2	4*1 or 2*2	4*1 or 2*2

DMAC Operation	Transfer Mode	
	Single Address	
	External Request (Level)	External Request (Edge)
Write → write*3	7*1*4 or 0*2	2*1 or 0*2
Write → read*3	0*2	0*2
Read → write	0*2	0*2
Read → read	5*1 or 0*2	2*1 or 0*2

Operating conditions:

1. The bits for setting the idle cycles between access cycles in CS1BCR and CS2BCR are all set to 0.
2. In CS1WCR and CS2WCR, the WM bit is set to 1 (external $\overline{\text{WAIT}}$ pin disabled), the SW[1:0] bits are set to 00 ($\overline{\text{CS}}$ assertion is not extended), and the HW[1:0] bits are set to 00 ($\overline{\text{CS}}$ negation is not extended).
3. For both the CS1 and CS2 spaces, SRAM devices are connected, the bit width is 16 bits.
4. The DMA transfer size is 16 bits. The operating mode of the DMAC is burst mode.
5. Numbers of cycles given for write → write sequences in dual address transfer are for data transfer between the on-chip memory and external memory, those given for read → read sequences are for data transfer between external memory and the on-chip memory, and those given for write → read and read → write sequences are for data transfer between locations in external memory.
6. In single address transfer, “write” means transfer from a device that has DACK to external memory and “read” means transfer from external memory to a device that has DACK.

Notes: 1. The minimum number of idle cycles in continuous DMA transfer on the same channel.

2. The minimum number of idle cycles in continuous DMA transfer between different channels.

3. When $\overline{\text{CS}}$ assertion extension (Th), access wait cycles (Tw), and $\overline{\text{CS}}$ negation extension (Tf) have been inserted for the previous access, the minimum numbers of idle cycles are reduced from the values in the table by Th+Tw+Tf due to the effect of the write buffer.

4. The effect of the write buffer does not reduce the minimum number of idle cycles.

[Before correction (p.412)]

Table 10.22 Number of Idle Cycles Inserted between Access Cycles to Different Memory Types

Previous Cycle	Next Cycle							
	SRAM	Burst ROM (Asynchronous)	MPX-I/O	Byte SRAM (BAS = 0)	Byte SRAM (BAS = 1)	SDRAM	SDRAM (Low-Frequency Mode)	Burst ROM (Synchronous)
SRAM	0	0	1	0	1	1	1.5	0
Burst ROM (asynchronous)	0	0	1	0	1	1	1.5	0
MPX-I/O	1	1	0	1	1	1	1.5	1
Byte SRAM (BAS = 0)	0	0	1	0	1	1	1.5	0
Byte SRAM (BAS = 1)	1	1	2	1	0	0	1.5	1
SDRAM	1	1	2	1	0	0	-	1
SDRAM (low-frequency mode)	1.5	1.5	2.5	1.5	0.5	-	1	1.5
Burst ROM (synchronous)	0	0	1	0	1	1	1.5	0

[After correction]

Table 10.22 Number of Idle Cycles Inserted between Access Cycles to Different Memory Types

Previous Access	Next Access							
	SRAM	Burst ROM (Asynchronous)	MPX-I/O	Byte SRAM (BAS = 0)	Byte SRAM (BAS = 1)	SDRAM	SDRAM (Low-Frequency Mode)	Burst ROM (Synchronous)
SRAM	0	0	1	0	1	1	1.5	0
Burst ROM (asynchronous)	0	0	1	0	1	1	1.5	0
MPX-I/O	1	1	0	1	1	1	1.5	1
Byte SRAM (BAS = 0)	0	0	1	0	1	1	1.5	0
Byte SRAM (BAS = 1)	1	1	2	1	0	0	1.5	1
SDRAM	1	1	2	1	0	0	-	1
SDRAM (low-frequency mode)	1.5	1.5	2.5	1.5	0.5	-	1	1.5
Burst ROM (synchronous)	0	0	1	0	1	1	1.5	0

[Before correction (p.413)]

Sample Estimation of Idle Cycles between Access Cycles

This example estimates the idle cycles for data transfer from the CS1 space to CS2 space by CPU access. Transfer is repeated in the following order: CS1 read ® CS1 read ® CS2 write ® CS2 write ® CS1 read ® ...

· Conditions
The bits for setting the idle cycles between access cycles in CS1BCR and CS2BCR are all set to 0.
In CS1WCR and CS2WCR, the WM bit is set to 1 (external WAIT pin disabled) and the HW[1:0] bits are set to 00 (CS negation is not extended).
If:Bf is set to 4:1, and no other processing is done during transfer.
For both the CS1 and CS2 spaces, normal SRAM devices are connected, the bus width is 32 bits, and access size is also 32 bits.

The idle cycles generated under each condition are estimated for each pair of access cycles. In the following table, R indicates a read cycle and W indicates a write cycle.

Condition	R ® R	R ® W	W ® W	W ® R	Note
[1] or [2]	0	0	0	0	CSnBCR is set to 0.
[3] or [4]	0	0	0	0	The WM bit is set to 1.
[5]	1	1	0	0	Generated after a read cycle.
[6]	0	2	2	0	See the If:Bf = 4:1 column in table 10.20.
[7]	0	1	0	0	No idle cycle is generated for the second time due to the write buffer effect.
[5] + [6] + [7]	1	4	2	0	
[8]	0	0	0	0	Value for SRAM ® SRAM access
Estimated idle cycles	1	4	2	0	Maximum value among conditions [1] or [2], [3] or [4], [5] + [6] + [7], and [8]
Actual idle cycles	1	4	2	1	The estimated value does not match the actual value in the W ® R cycles because the internal idle cycles due to condition [6] is estimated as 0 but actually an internal idle cycle is generated due to execution of a loop condition check instruction.

Figure 10.43 Comparison between Estimated Idle Cycles and Actual Value

[After correction]

Sample Estimation of Idle Cycles between Access Cycles

This example estimates the idle cycles for data transfer from the CS1 space to CS2 space by CPU access. Transfer is repeated in the following order: CS1 read ® CS1 read ® CS2 write ® CS2 write ® CS1 read ® ...

· Conditions
The bits for setting the idle cycles between access cycles in CS1BCR and CS2BCR are all set to 0.
In CS1WCR and CS2WCR, the WM bit is set to 1 (external WAIT pin disabled) and the HW[1:0] bits are set to 00 (CS negation is not extended).
If:Bf is set to 4:1, and no other processing is done during transfer.
For both the CS1 and CS2 spaces, SRAM devices are connected, the bus width is 16 bits, and access size is also 16 bits.

The idle cycles generated under each condition are estimated for each pair of access cycles. In the following table, R indicates a read cycle and W indicates a write cycle.

Condition	R ® R	R ® W	W ® W	W ® R	Note
[1] or [2]	0	0	0	0	CSnBCR is set to 0.
[3] or [4]	0	0	0	0	The WM bit is set to 1.
[5]	1	1	0	0	Generated after a read cycle.
[6]	0	1	0	0	See the If:Bf = 4:1 column in table 10.20.
[7]	0	1	0	0	No idle cycle is generated for the second time due to the write buffer effect.
[5] + [6] + [7]	1	3	0	0	
[8]	0	0	0	0	Value for SRAM ® SRAM access
Estimated idle cycles	1	3	0	0	Maximum value among conditions [1] or [2], [3] or [4], [5] + [6] + [7], and [8]
Actual idle cycles	1	3	0	1	The estimated value does not match the actual value in the W ® R cycles because the internal idle cycles due to condition [6] is estimated as 0 but actually an internal idle cycle is generated due to execution of a loop condition check instruction.

Figure 10.43 Comparison between Estimated Idle Cycles and Actual Value

10.5.11 Bus Arbitration

(4) Number of Access Cycles

Tables 10.23 Number of Access Cycles (1), **(2)**, and **(3)** have been modified as shown below. For table number n, read numerals from 1 to 3.

[Before correction (p.419 to 424)]

Table 10.23 Number of Access Cycles (n)

			Iϕ Bϕ			
			1:1	2:1	4:1	8:1
Bϕ Pϕ	1:1	m1	2Iϕ	2Iϕ to 3Iϕ	2Iϕ to 5Iϕ	2Iϕ to 9Iϕ
		m2	1Bϕ	1Bϕ	1Bϕ	1Bϕ
		m3	2Iϕ	3Iϕ	4Iϕ	4Iϕ
	2:1	m1	2Iϕ	2Iϕ to 3Iϕ	2Iϕ to 5Iϕ	2Iϕ to 9Iϕ
		m2	1Bϕ to 2Bϕ	1Bϕ to 2Bϕ	1Bϕ to 2Bϕ	1Bϕ to 2Bϕ
		m3	2Iϕ	3Iϕ	4Iϕ	4Iϕ
	4:1	m1	2Iϕ	2Iϕ to 3Iϕ	2Iϕ to 5Iϕ	2Iϕ to 9Iϕ
		m2	1Bϕ to 4Bϕ	1Bϕ to 4Bϕ	1Bϕ to 4Bϕ	1Bϕ to 4Bϕ
		m3	2Iϕ	3Iϕ	4Iϕ	4Iϕ
	8:1	m1	2Iϕ	2Iϕ to 3Iϕ	2Iϕ to 5Iϕ	2Iϕ to 9Iϕ
		m2	1Bϕ to 8Bϕ	1Bϕ to 8Bϕ	1Bϕ to 8Bϕ	1Bϕ to 8Bϕ
		m3	2Iϕ	3Iϕ	4Iϕ	4Iϕ

[After correction]

Table 10.23 Number of Access Cycles (n)

			Iϕ : Bϕ			
			1:1	2:1	4:1	8:1
Bϕ : Pϕ	1:1	m1	2Iϕ	2Iϕ to 3Iϕ	2Iϕ to 5Iϕ	2Iϕ to 9Iϕ
		m2	1Bϕ	1Bϕ	1Bϕ	1Bϕ
		m3	2Iϕ	2Iϕ	2Iϕ to 3Iϕ	3Iϕ
	2:1	m1	2Iϕ	2Iϕ to 3Iϕ	2Iϕ to 5Iϕ	2Iϕ to 9Iϕ
		m2	1Bϕ to 2Bϕ	1Bϕ to 2Bϕ	1Bϕ to 2Bϕ	1Bϕ to 2Bϕ
		m3	2Iϕ	2Iϕ	2Iϕ to 3Iϕ	3Iϕ
	4:1	m1	2Iϕ	2Iϕ to 3Iϕ	2Iϕ to 5Iϕ	2Iϕ to 9Iϕ
		m2	1Bϕ to 4Bϕ	1Bϕ to 4Bϕ	1Bϕ to 4Bϕ	1Bϕ to 4Bϕ
		m3	2Iϕ	2Iϕ	2Iϕ to 3Iϕ	3Iϕ
	8:1	m1	2Iϕ	2Iϕ to 3Iϕ	2Iϕ to 5Iϕ	2Iϕ to 9Iϕ
		m2	1Bϕ to 8Bϕ	1Bϕ to 8Bϕ	1Bϕ to 8Bϕ	1Bϕ to 8Bϕ
		m3	2Iϕ	2Iϕ	2Iϕ to 3Iϕ	3Iϕ

[Before correction (p.425)]

Figure 10.45 shows an example of the timing of write access to the peripheral bus when Iϕ:Bϕ:Pϕ = 4:4:1. Data are output to the CPU bus, which is connected to the CPU, in synchronization with Iϕ. When Iϕ:Bϕ = 1:1, transfer of data from the CPU bus to the internal bus takes $2 \times I\phi + 1 \times B\phi$.

[After correction]

Figure 10.45 shows an example of the timing of write access to the peripheral bus when Iϕ:Bϕ:Pϕ = 4:4:1. Data are output to the CPU bus, which is connected to the CPU, in synchronization with Iϕ. When Iϕ:Bϕ = 1:1, transfer of data from the CPU bus to the internal bus takes $2 \times I\phi$.

[Before correction (p.426)]

Figure 10.46 shows an example of timing of read access to the peripheral bus when Iϕ:Bϕ:Pϕ = 4:2:1. Transfer from the CPU bus to the peripheral bus is performed in the same way as for write access. In the case of reading, however, values output onto the peripheral bus must be transferred to the CPU. Although transfers from the peripheral bus to the internal bus and from the internal bus to the CPU bus are performed in synchronization with the rising edge of the respective bus clocks, a period of 3 × Iϕ is actually required because Iϕ ≥ Bϕ≥ Pϕ. In the case shown in the **figure 10.46**, the time required for access is 3 × Iϕ + 2 × Bϕ + 2 × Pϕ + 3 × Iϕ.

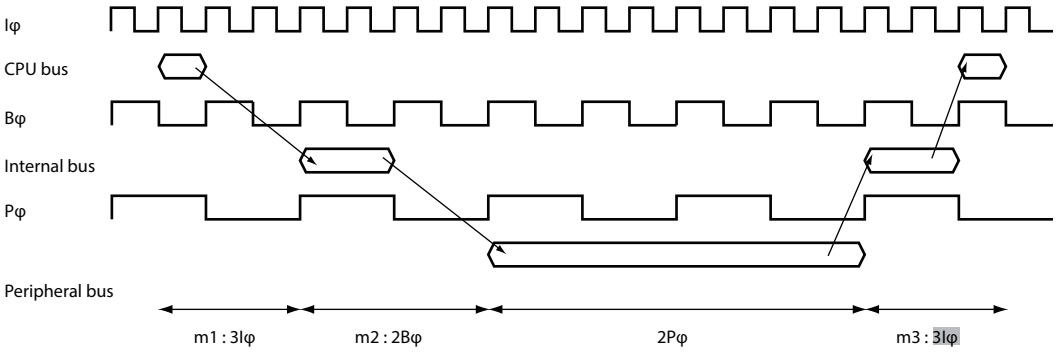

Figure 10.46 Timing of Read Access to On-Chip Peripheral I/O Registers and On-Chip RAM (for Data Retention) When Iϕ:Bϕ:Pϕ = 4:2:1

[After correction]

Figure 10.46 shows an example of timing of read access to the peripheral bus when Iϕ:Bϕ:Pϕ = 4:2:1. Transfer from the CPU bus to the peripheral bus is performed in the same way as for write access. In the case of reading, however, values output onto the peripheral bus must be transferred to the CPU. Transfers from the peripheral bus to the internal bus and from the internal bus to the CPU bus are performed in synchronization with the rising edge of the respective bus clocks, requiring a period of 2 × Iϕ. In the case shown in the **figure 10.46**, the time required for access is 3 × Iϕ + 2 × Bϕ + 2 × Pϕ + 2 × Iϕ.

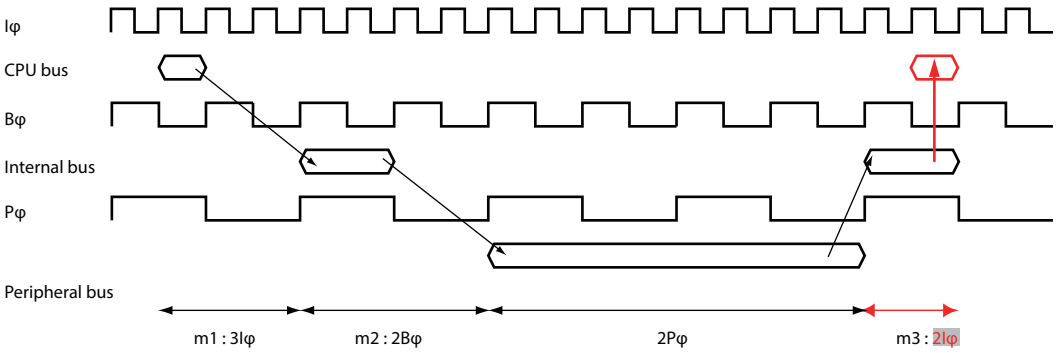

Figure 10.46 Timing of Read Access to On-Chip Peripheral I/O Registers and On-Chip RAM (for Data Retention) When Iϕ:Bϕ:Pϕ = 4:2:1