

# CS+ RX Simulator V3.02.00

Thank you for using the CS+ integrated development environment.

This document describes restrictions on and points for caution regarding the simulator. Read this document before using the product.

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# Chapter 1. Target Devices

CS+ Simulator for RX supports simulation of timer in addition to simulation of the RX CPU core. A list below shows devices supported by this simulator.

Known as	Device name
RX700	RX700 series
RX600	RX600 series
RX200	RX200 series
RX100	RX100 series



# Chapter 2. User's Manuals

Please read the following user's manuals together with this document.

Manual Name	Document Number
CS+ V8.02.00 RX Debug Tool	R20UT4528EJ0100



# Chapter 3. Supported Function

This section describes the scope of the supported functions of the RX simulator debugger.

(1) The simulator debugger supports the following items:

- All CPU instructions
- Exception processing
- Registers
- All address space
- Trigonometric function calculator
- Peripheral module (timer and memory protection unit)

(2) The simulator debugger does not support the following RX functions.

No.	Item	Remarks
1	Low power consumption state	Simulation is stopped on the execution of a WAIT instruction.
2	Non-maskable interrupt (NMI)	
3	Reception of an interrupt during execution of any of the following instructions: (RMPA, SCMPU, SMOVF, SMOVB, SMOVU, SSTR, SUNTIL, and SWHILE)	The interrupt is accepted when execution of the instruction is completed.
4	Values in memory and registers that become undefined after the execution of instructions	
5	Lower-order 16 bits of the accumulator (ACC) Notes: RXv1 core	The simulator debugger returns 0.



## Chapter 4. Simulation of Peripheral Modules

This section describes support for peripheral modules by the simulator debugger.

### 4.1 Timer

(1) Supported Range

The simulator debugger supports compare match timer (CMT) units with two 16-bit timer channels.

RX700, RX600 and RX200- two units (unit 0 and unit 1), four channels in total.RX100- one unit(unit0), two channels in total.

(2) Control Registers

The registers supported by this simulator are listed below.

Note: In access to control registers, make sure that the unit of access corresponds to the size of the register.

Unit	Supported Control Register	Support
Unit0	CMSTR0	YES
	CMCR0 and CMCR1	YES
	CMCNT0 and CMCNT1	YES
	CMCOR0 and CMCOR1	YES
Unit1	CMSTR1	YES
	CMCR2 and CMCR3	YES
	CMCNT2 and CMCNT3	YES
	CMCOR2 and CMCOR3	YES

Note: YES indicates support for the corresponding register.



## 4.2 Interrupt Controller

#### (1) Supported Range

The simulator debugger supports the interrupt controller unit (ICU) in relation to the CMT and double-precision floating-point exception. Only interrupts for the CPU are supported; that is, activation of the DTC and DMAC is not supported.

#### (2) Control Registers

The simulator supports the registers listed below.

Note: In access to control registers, make sure that the unit of access corresponds to the size of the register.

Supported Control Register	Support
IRn (n = 028 to 029)	YES
IER03	NO
IPRm (m = 04 to 07)	YES
FIR	YES

- Note: YES indicates support for the corresponding register; NO indicates that only the CMT-related functions are supported.
- (3) Control Registers ( for products that support the software configurable interrupt function ) The simulator supports the registers listed below.
  - Note: In access to control registers, make sure that the unit of access corresponds to the size of the register.

Supported Control Register	Support
IRn (n=028, 029, 128 to 207)	YES
IERm (m = 03, 10 to 19)	NO
IPRn (n=004, 005, 128 to 207)	YES
FIR	YES
PIBRm (m = 00)	NO
SLIBXRn (n = 128 to 143)	NO
SLIBRn (n = 144 to 207)	
SLIPRCR	YES

Note: YES indicates support for the corresponding register. NO indicates that only the CMT-related functions are supported.

- (4) Control Registers ( for products equipped with double-precision floating-point coprocessor ) The simulator supports the registers listed below.
  - Note: In access to control registers, make sure that the unit of access corresponds to the size of the register.

Supported Control Register	Support
IRn (n = 017, 028, 029, 128 to 207)	YES
IERm (m = 02, 03, 10 to 19)	NO
IPRn (n = 000, 004, 005, 128 to 207)	YES
FIR	YES
NMISR	NO
NMIER	NO
NMICLR	NO
EXNMISR	NO
EXNMIER	NO
EXNMICLR	NO
GPRIE0	NO
GENIE0	NO
GCRIE0	NO
PIBRm (m = 00)	NO
SLIBXRn (n = 128 to 143)	NO
SLIBRn (n = 144 to 207)	
SLIPRCR	YES

Note: YES indicates support for the corresponding register. NO indicates that only functions related to CMT and double-precision floating-point exception are supported.



## 4.3 Memory Protection Unit

#### (1) Scope of Support

The simulator debugger supports the memory protection unit (MPU).

#### (2) Control Registers

Below is a list of registers supported by this simulator.

Note: In access to control registers, make sure that the unit of access corresponds to the size of the register.

Supported Control Register	Support
RSPAGEn (n = 0 to 7)	YES
REPAGEn (n = 0 to 7)	YES
MPEN	YES
MPBAC	YES
MPECLR	YES
MPESTS	YES
MPDEA	YES
MPSA	YES
MPOPS	YES
MPOPI	YES
MHITI	YES
MHITD	YES

Note: YES indicates the corresponding register is supported



# Chapter 5. Changes

This chapter describes changes from V3.01.00 to V3.02.00 of RX simulator.

## 5.1 Support for double-precision floating-point processing instructions

The programs using double-precision floating-point processing instructions can be simulated. These instructions are available in products that have double-precision floating-point coprocessor.

## 5.2 Support for the trigonometric function calculator

The programs using the trigonometric function calculator can be simulated. This function is available in products that have the trigonometric function calculator.



# Chapter 6. Cautions

This section describes points for caution when using the RX simulator debugger.

## 6.1 Caution on time measurement results on return out

#### (1) Run-Break timer

The displayed total execution time and numbers of cycles for execution and of instructions executed may be incorrect.

(2) Trace

When use of the trace function is selected by specifying [Yes] in [Accumulate trace time], displayed trace times may be incorrect.

## 6.2 Caution on tracing within desired ranges

When tracing is started by an execution-related event, the simulator collects execution history from the address of the instruction immediately before the location for which execution was set as an event to start tracing. When tracing ends with an execution-related event, the simulator collects execution history up to the address of the instruction immediately before the location for which execution was set as an event to end tracing.

## 6.3 Caution on measuring execution time within desired ranges

When time measurement ends with an execution-related event, the simulator measures execution time up to the address of the instruction immediately before the location for which execution was set as an event to end tracing

## 6.4 Caution on access to the external area

Different types of memory in the external area are not supported. If you are using the external area with a ROM-less device, for example, add either [Emulation ROM area] or [Emulation RAM area] to [Memory Mappings] as a substitute for the actual type of memory on the Property panel. Access (both reading and writing) to the emulation ROM and RAM areas takes one cycle.



## 6.5 Caution on Python functions while a program is being executed

Do not call the Python functions listed below while a program is being executed.

- debugger.Option.Coverage
- debugger.Option.Trace
- debugger.XTrace.Addup
- debugger.Map.Set

Calls of the Python functions listed above while a program is being executed change the state of the contents of the Property panel and status bar to which has been set. The state of the simulator, however, is still that before the change to the Property panel and status bar.

When this cautionary note becomes applicable, stop the program and return the changed settings to their original states.

# 6.6 Caution on cycle accuracy of products equipped with RXv2 or RXv3 core

There may be a difference between the numbers of cycles measured by the simulator and actual numbers of cycles on the CPU.



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(Rev.4.0-1 November 2017)

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