ISL9123xIIx-EVZ

The ISL9123xIIx-EVZ platform allows quick evaluation of the high-performance features of the ISL9123, ISL9123A, and ISL9123B buck regulator. The ISL9123 is a highly integrated buck switching regulator that accepts input voltages above the regulated output voltage. It features a remarkably low quiescent current consumption, excellent efficiency, and an I^2C interface that allows access its internal registers for output voltage and operation mode control.

Features

- Small, compact design
- I^2C interface for programmable V_{OUT}, slew rate and various operation modes (Forced Bypass (ISL9123/A only), Auto-PFM, Forced PWM)
- Connectors, test points, and jumpers for easy probing

Specifications

The board operates with the following conditions:

- Input voltage rating from 1.8V to 5.5V
- Programmable output voltage range of 0.4V to 5.375V (ISL9123/A), and to 1.180V (ISL9123B), and selectable transition slew rate through I^2C interface
- Up to 600mA output current (VIN > 2.5V)
- Operating temperature range: -40°C to +85°C

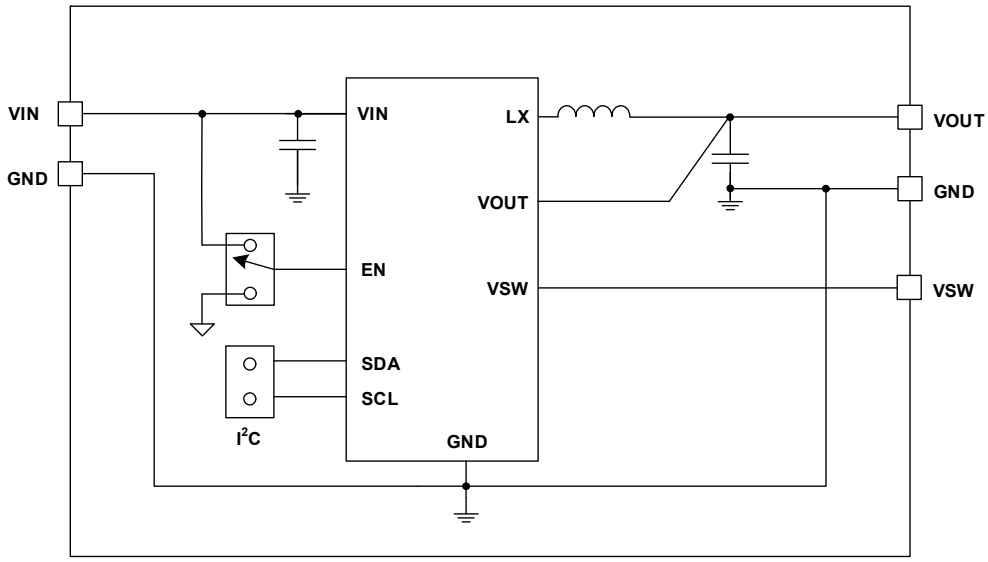

Figure 1. ISL9123xIIx-EVZ Block Diagram

Contents

1. Functional Description

The evaluation board (EVB) provides a simple platform to evaluate the feature-rich ISL9123/A/B buck regulator. The board regulates to the device default output voltage after start-up. The output voltage can be programmed by I^2C. Each evaluation board is optimized to perform best with the ISL9123/A/B IC series. The input power and load connections are provided through multi-pin connectors for high-current operations.

The evaluation board is shown in Board Design. Table 1 lists the test points and jumpers for the boards. The ISL9123 internal registers can be accessed by I^2C through the on-board jumper header J5, and its mode control register configures the part into the various operation modes. See the Evaluation Software Installation and Use to configure the board output voltage and operation modes.

Table 1. Description of Test Points and Jumpers

Test Points	Description
J1	Header for connecting input power
J2	Header for connecting external load
J4	Header for the EN pin, J4 = GND disables the part output; J4 = V_{IN} enables the part output
J5	Header for connecting I^2C interface
J1 S+/S-	V_{IN} Kelvin connection for efficiency measurements
J2 S+/S-	V_{OUT} Kelvin connection for efficiency measurements
TP1	Through Hole Mount PCB test point for LX
TP2	Through Hole Mount PCB test point for VSW (Auxiliary output). Do not use for ISL9123B.
TP3	Through Hole Mount PCB test point for VOUT
TP4	Single Turret Terminal test point for VIN
TP5	Single Turret Terminal test point for VOUT
TP6	Single Turret Terminal test point for GND
TP7	Single Turret Terminal test point for GND
TP8	Single Turret Terminal test point for GND

1.1 Operational Characteristics

The V_{IN} range is 1.8V to 5.5V while the adjustable V_{OUT} range is 0.4V to 5.375V (ISL9123/A) and to 1.180V (ISL9123B). The I_{OUT} range of the board is 0 to 600mA. The operating ambient temperature range is -40°C to +85°C.

1.2 Setup and Configuration

Use the following procedures to configure and power-up the board for proper operation. During the power-on process, the expected waveforms are shown in Figure 2.

1. Connect the power supply to J1, with voltage setting between 1.8V and 5.5V but higher than output voltage setting for buck mode operation.
2. Connect the electronic load to J2.
3. Place the scope probes on VOUT test point and other test points of interest.
4. Ensure that the EN pin jumper (J4) is pulled up to VIN.
5. Turn on the power supply. At the end of the soft-start sequence, the ISL9123/A/B is operating in Regulation mode at the default output voltage setting. *Note*: A minimum effective output capacitance of 6µF is required.

Therefore, depending on the performance specifications of the capacitor, an additional output capacitor might be required for higher output voltage settings.

6. Monitor the output voltage start-up sequence on the scope. The waveforms should look similar to those shown in Figure 2.
7. Turn on the electronic load.
8. Measure the output voltage with the voltmeter. The voltage should regulate within the datasheet specification limits.
9. To determine efficiency, measure input and output voltages at the Kelvin sense test points (S+ and S-), which are part of J1 and J2 headers. The bench power supply can be connected to the VIN and GND headers on J1. The electronic load can be connected to the VOUT and GND headers on J2. Measure the input and output currents. Calculate the efficiency based on these measurements.
10. VSW (auxiliary output) should be left floating if not connected to a load. Refer the part datasheet for additional information on VSW pin. Leave floating for ISL9123B.

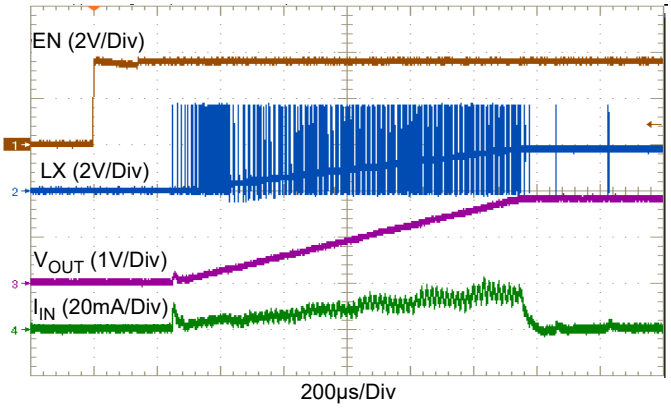

Figure 2. ISL9123/A Start-Up with V_{IN} = 3.6V and V_{OUT} = 1.8V

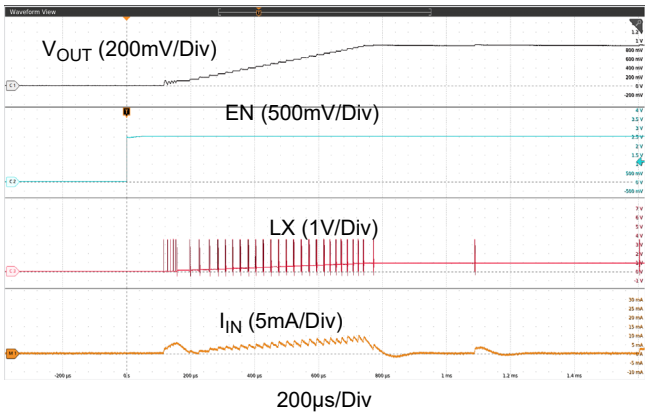

Figure 3. ISL9123B Start-Up with V_{IN} = 3.6V and V_{OUT} = 0.88V

1.3 Evaluation Software Installation and Use

The ISL9123 evaluation software and evaluation software manual are available for download from the Renesas website.

1. Save the evaluation software executable file and install the evaluation software (see the evaluation software manual). When the evaluation software launches, (see the Setup and Configuration and) connect the power supply, DC load, and other test equipment to the evaluation board; next, apply power.
2. The ISL9123/A/B has various control registers. See the ISL9123/A and ISL9123B datasheets for detailed register descriptions.
3. Register **RO_REG1** (Address: 0x02) provides chip identification information. The Get **IC INFO_RO_REG1** button reads from this read-only register.
4. To change the output voltage, use the **VSET Control** slider in the **VSET** register (Address: 0x11) panel and perform a Write REG operation. The output voltage ramps up at the slew rate specified in the **DVSRATE** setting of **CONV_CFG** register. If the modified output voltage is lower than the initial value, its ramp down rate depends on the applied load and output capacitance. The **Read REG** button provides the contents of the register, so adjust the slider accordingly.
5. Register **INTFLG_REG** (Address: 0x03) contains the fault flags. The background color changes from green to red: when (1) a fault occurs, and (2) this register is read using either the **Check Fault** button or the **READ ALL** button. Each bit is set by a fault event and cleared when read. When the bit is cleared after reading, the background color changes from red back to green.
6. Register **CONV_CFG** (Address: 0x12) contains crucial converter configuration bits. Selecting the **Write** (or **Read**) button writes (or reads) the entire **CONV_CFG** register in one go.
7. Use **EN_AND** bit to disable the converter through I^2C by toggling the **Soft Start EN_AND** button from **Soft Start enabled** to **Soft Start inhibit**.
8. Selecting the **Soft DSCHG enabled** button presents a soft discharge resistor on the output pin, when the converter is disabled through I^2C using the EN_AND bit and VIN is still HIGH. By default, the **Soft DSCHG disabled** button is selected. (ISL9123/B only)
9. Use the **DVSRATE** drop-down list to modify the dynamic voltage scaling rate for voltage ramp up, when output voltage is modified using the **VSET** register.
10. Use the **FMODE** drop-down list to select one of the forced operating modes: **Normal** (Auto-PFM, default), **Forced PWM**, and **Forced Bypass** (ISL9123/A only).
11. Use the **CTRL Type** drop-down list to select the control mode between **Type I** and **Type II** error amplifier.
12. Register **INTFLG_MASK** (Address: 0x13) contains additional features influencing the part behavior. Selecting the **Write** (or **Read**) button writes (or reads) the entire **INTFLG_MASK** register in one go.
13. Use the **OC_FAULT** drop-down to select the over-current handling mechanism for the part.
14. Use the **EN_OR** drop-down list to enable a push-button ON functionality for the EN pin.

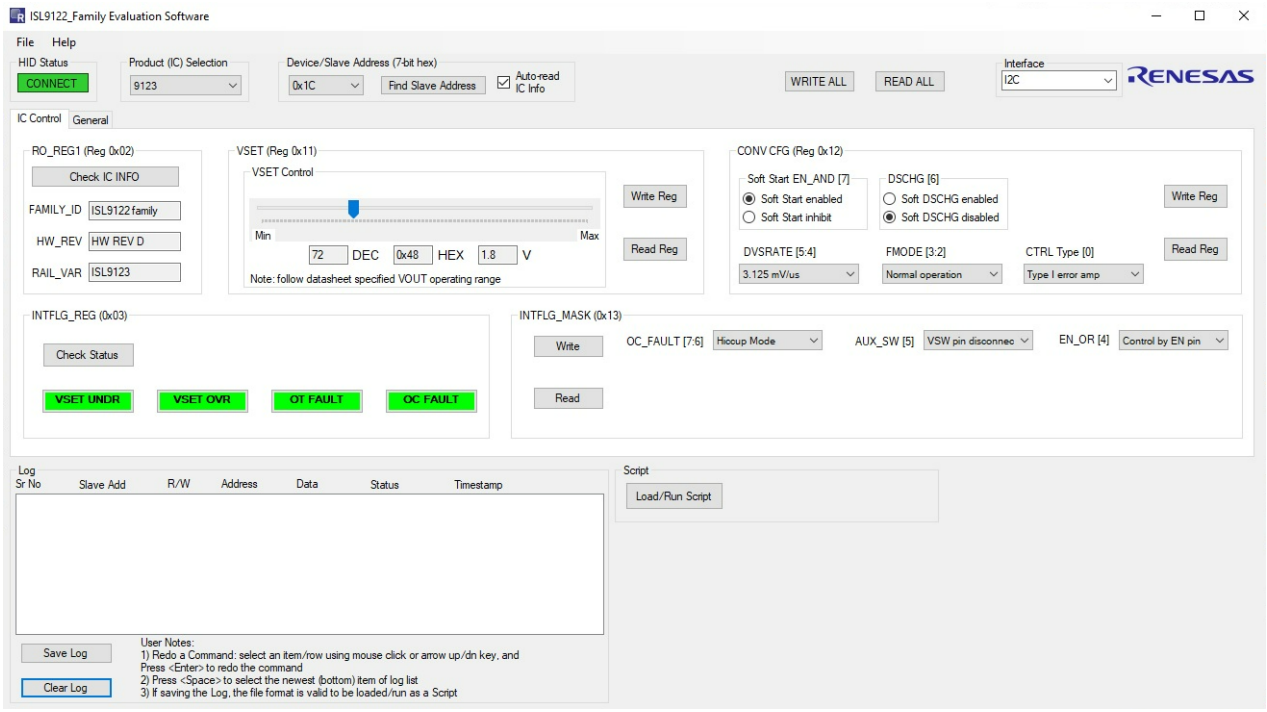

Figure 4. ISL9123 Evaluation Software Window

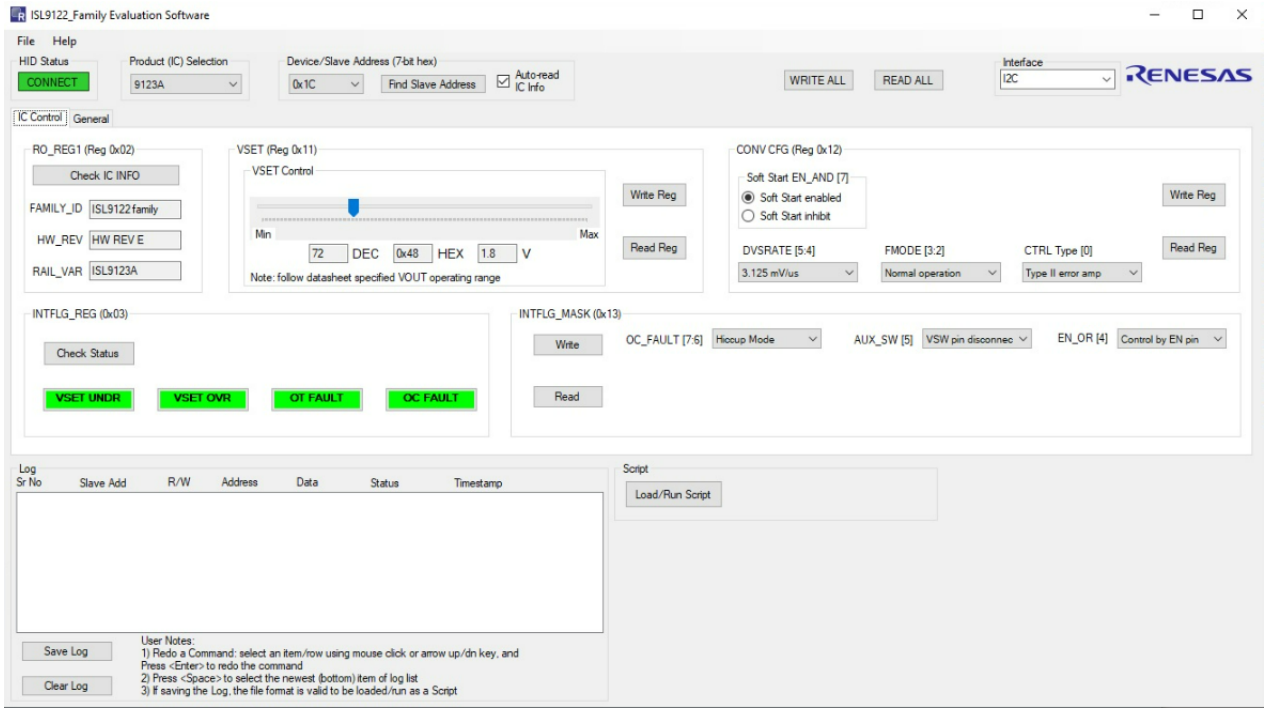

Figure 5. ISL9123A Evaluation Software Window

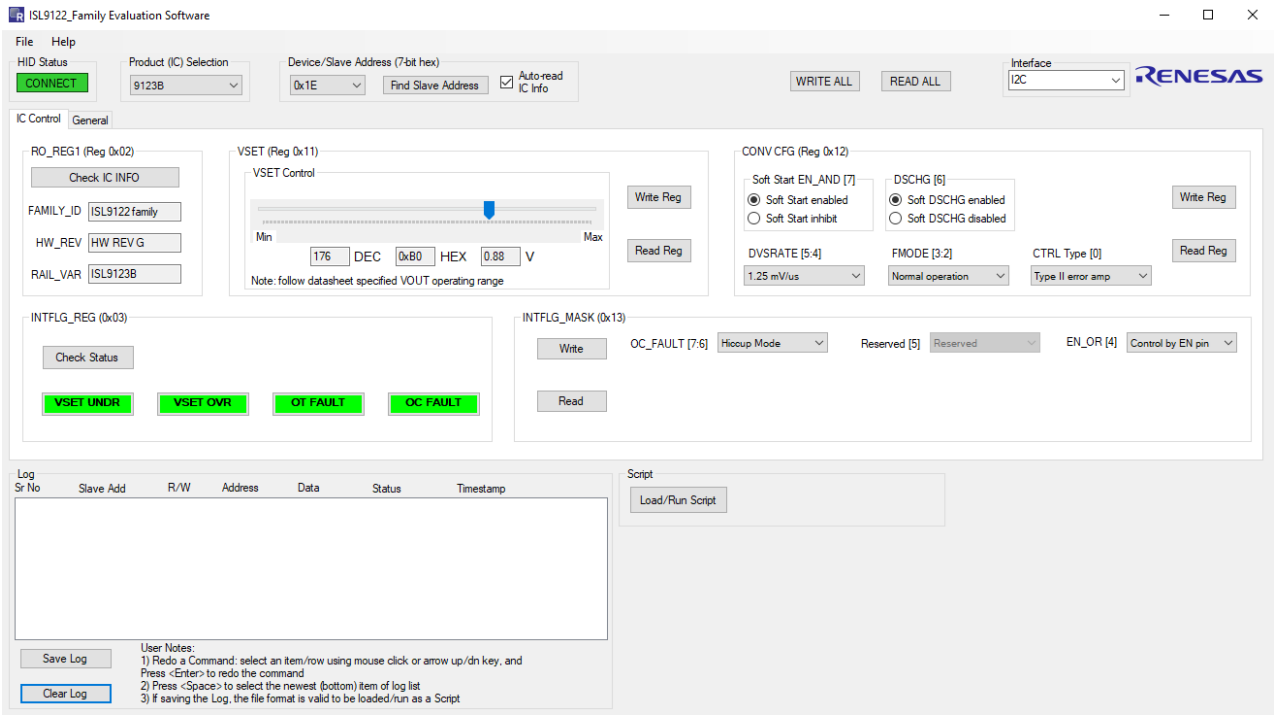

Figure 6. ISL9123B Evaluation Software Window

2. Board Design

2.1 ISL9123xIIx-EVZ (WLCSP)

2.1.1 Board Image

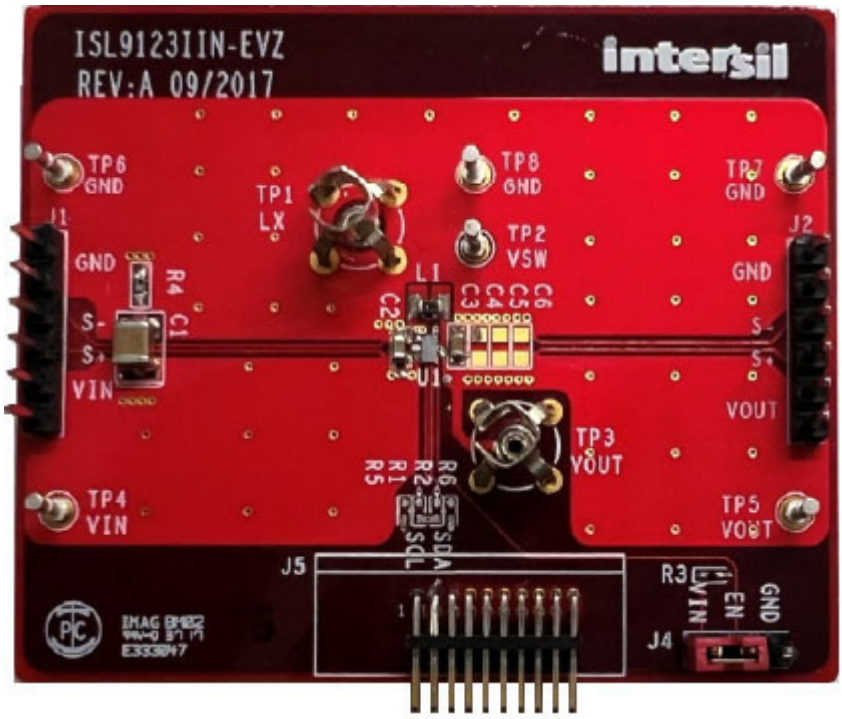

Figure 7. ISL9123xIIx-EVZ Evaluation Board (Top)

2.1.2 Circuit Schematic

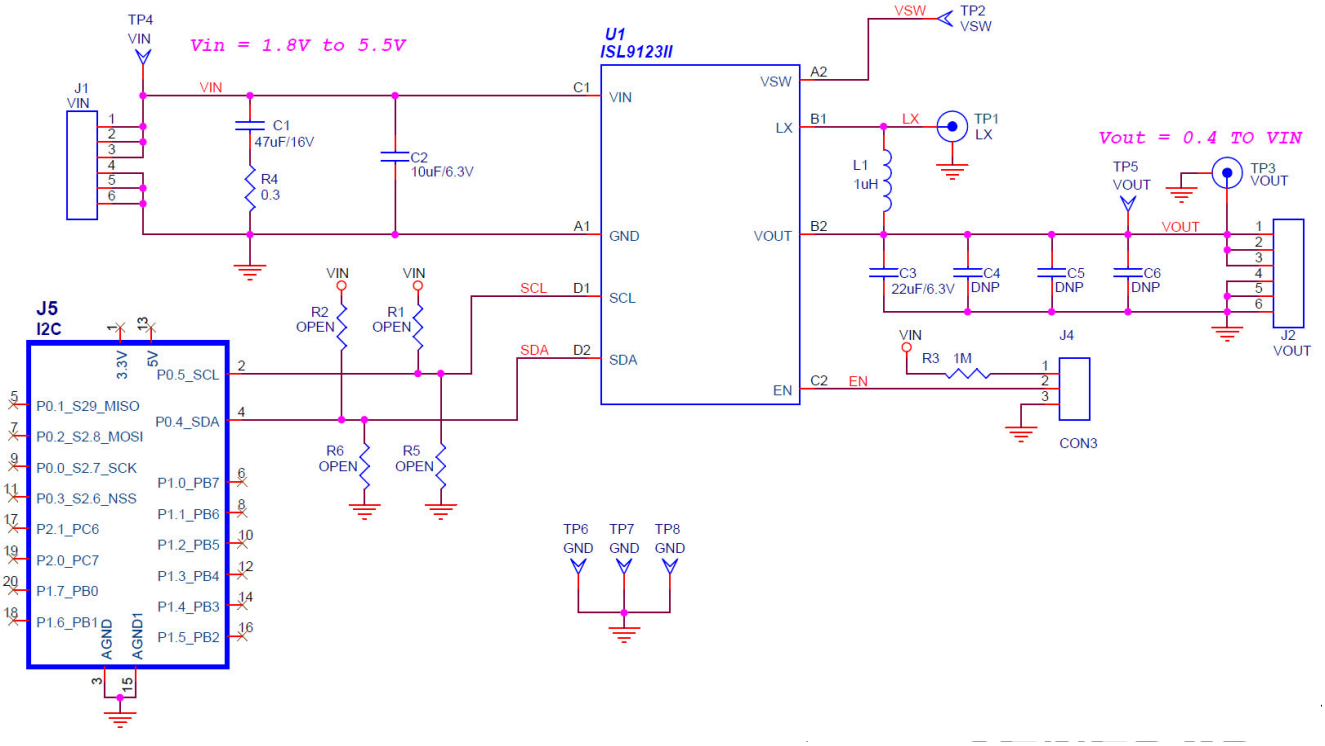

Figure 8. ISL9123xIIx-EVZ Circuit Schematic

2.1.3 Bill of Materials

Qty	Reference Designator	Description	Manufacturer Part Number	Manufacturer
1	C1	CAP, SMD, 1210, 47µF, 16V, 20%, ROHS	GRM32ER61C476ME15	Murata
1	C2	CAP, SMD, 0603, 10µF, 6.3V, 20%, X5R, ROHS	GRM188R60J106ME84D	Murata
2	C3, C4[1]	CAP, SMD, 0603, 22µF, 6.3V, 20%, X5R, ROHS	GRM188R60J226ME15D	Murata
2	C5, C6	CAP, SMD, 0603, DNP-PLACE HOLDER, ROHS	Open	Any
2	J1, J2	CONN-HEADER, 1×6, BRKAWY 1×36, 2.54mm, ROHS	68000-236	FCI
1	J4	CONN-HEADER, 1×3, BRKAWY 1×36, 2.54mm, ROHS	68000-236	FCI
1	J5	CONN-HEADER, TH, 2×10, 1.27mm PITCH, R/A, ROHS	M50-3901042	Harwin Inc
1	L1	COIL-PWR INDUCTOR, SMD, 0603, 1µH, 20% 1.7A, 128mΩ, ROHS	DFE18SAN1R0MG0L	Murata
4	R1, R2, R5, R6	RES, SMD, 0402, DNP-PLACE HOLDER, TF, ROHS	Open	Any
1	R3	RES, SMD, 0402, 1MΩ, 1/16W, 1%, TF, ROHS	ERJ-2RKF1004X	Panasonic
1	R4	RES, SMD, 0603, 0.3Ω, 1/10W, 1%, TF, ROHS	RL0603FR-070R3L	Yageo
2	TP1, TP3	CONN-SCOPE PROBE TEST PT, COMPACT, PCB MNT, ROHS	131-5031-00	Tektronix
6	TP2, TP4, TP5, TP6, TP7, TP8	CONN-TURRET, TH, SWAGE MNT, 0.230 LENGTH, ROHS	2110-2-00-80-00-00-07-0	Mill-Max

Qty	Reference Designator	Description	Manufacturer Part Number	Manufacturer
1	U1[2]	IC, ULTRA-LOW IQ BUCK REGULATOR, 1.8V, WLCSP, ROHS	ISL9123IICZ	Renesas Electronics
		IC, ULTRA-LOW IQ BUCK REGULATOR, 3.0V, WLCSP, ROHS	ISL9123IINZ	
		IC, ULTRA-LOW IQ BUCK REGULATOR, 1.8V, WLCSP, ROHS	ISL9123AIICZ	
		IC, ULTRA-LOW IQ BUCK REGULATOR, 0.88V, WLCSP, ROHS	ISL9123BII9Z	
1	J4-Pins 1-2	CONN-JUMPER, SHUNT, 2P, 2.54mmPITCH, BLK, 6mm, ROHS	SPC02SYAN	Sullins

1. C4 is DNP in default configuration. It is required to be populated if effective capacitance of C3 is less than 6µF at the operating output voltage.
2. All related WLCSP packaged device(s) use the same printed circuit board design (ISL9123IIN-EVZ), with an appropriate silk screen or label according to the unique orderable evaluation board part number.

2.1.4 Board Layout

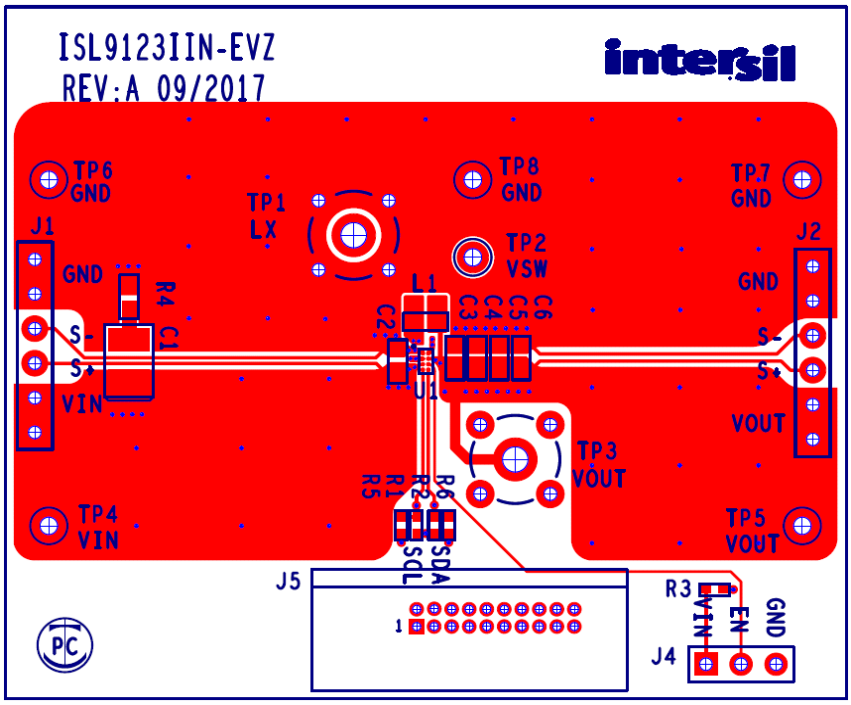

Figure 9. ISL9123xIIx-EVZ Top Layer Silk Screen

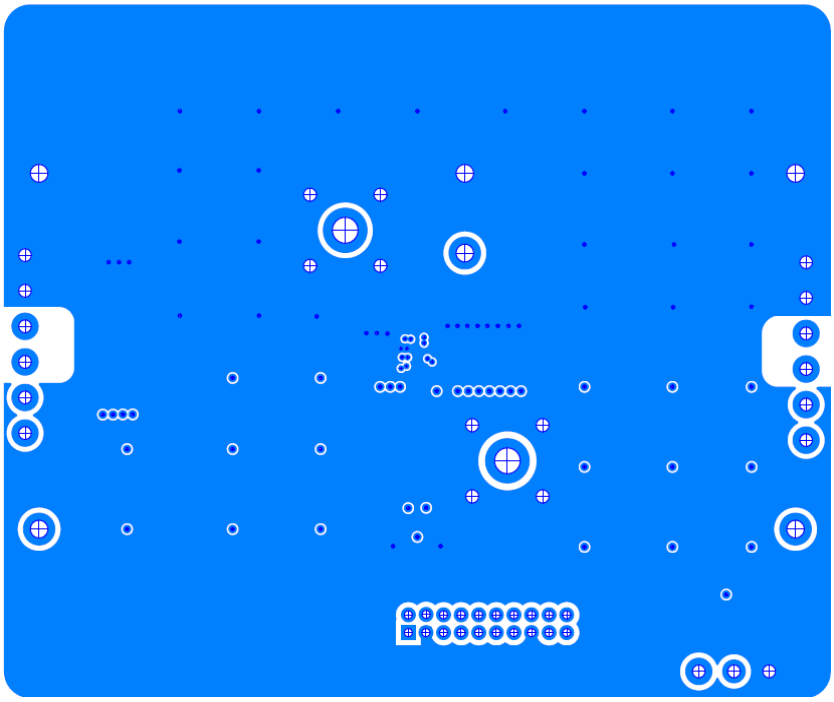

Figure 10. ISL9123xIIx-EVZ Inner Layer 2

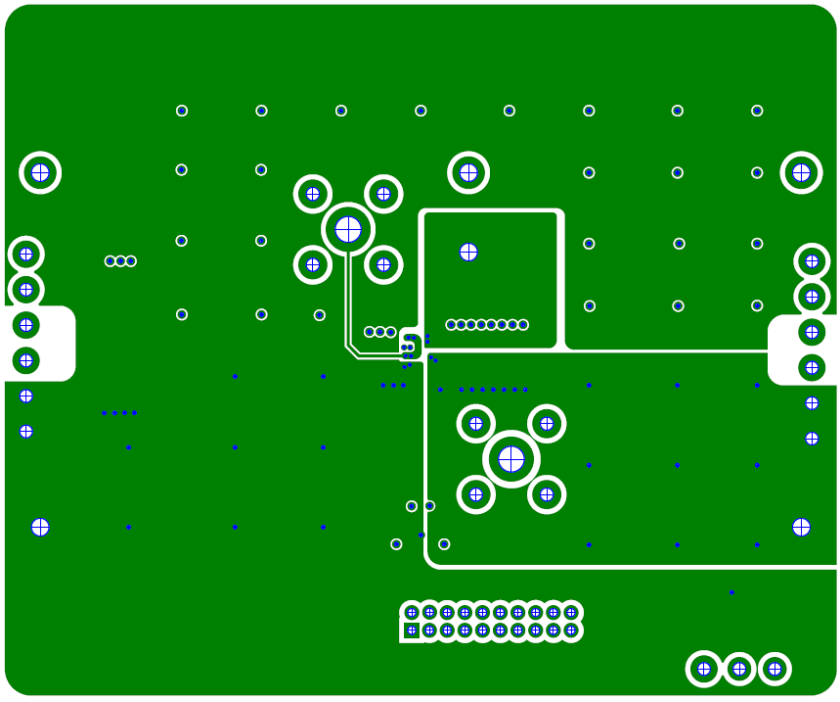

Figure 11. ISL9123xIIx-EVZ Inner Layer 3

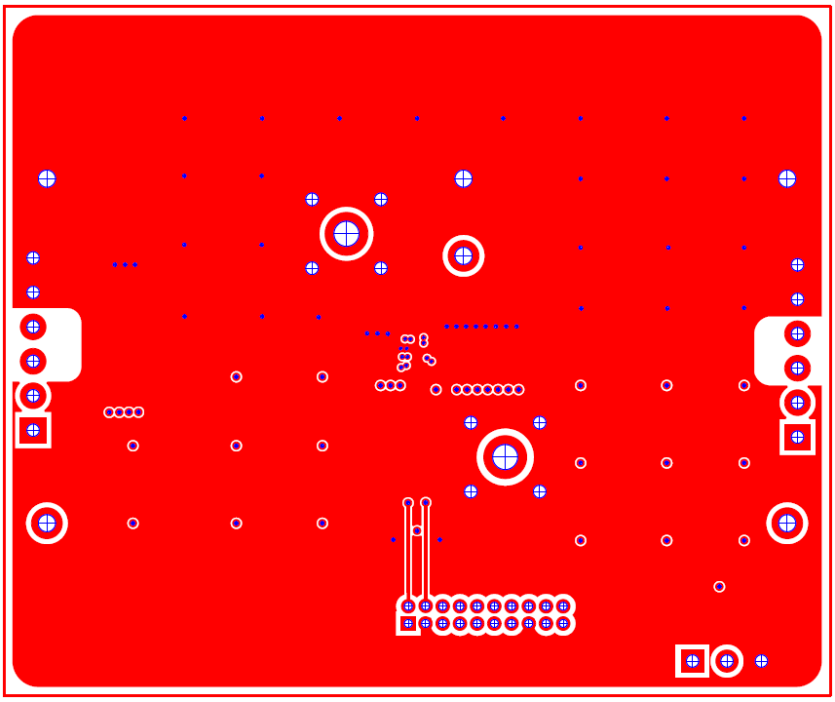

Figure 12. ISL9123xIIx-EVZ Bottom Layer Silk Screen

2.2 Layout Guidelines

The evaluation board PCB layout is optimized for electrical and thermal performance.

- Position the input and output capacitors as close to the IC as possible. The input currents are discontinuous in a buck converter; therefore, it is important to place the input capacitors as close as possible.
- Keep the ground connections of the input and output capacitors as short as possible and on the component layer to avoid problems that are caused by high-switching currents flowing through PCB vias. If it is necessary to use the vias, use multiple vias to minimize the effective trace inductance.
- It is strongly advised that the second layer is a clean GND to mitigate problems that arise from long GND traces and subsequent parasitic inductive components. Also, a clean GND shields the intermediate layers from high power traces on the top layer.
- After placing short input and output loops, place an inductor as close as possible to the IC. While being cautious of any EMI concerns, ensure that the switch node traces (from LX to the inductor) are short and wide.
- Finally, EN, SCL, SDA should be routed away from high energy and high dV/dt traces to prevent mis-triggering. These traces can be routed through the intermediate layers.

Note: C1 and R4 are on the evaluation board to stabilize the input supply with long test leads, and they are not required in actual system boards.

3. Ordering Information

Part Number	Description
ISL9123IIC-EVZ	Evaluation board for ISL9123IICZ, WLCSP
ISL9123IIN-EVZ	Evaluation board for ISL9123IINZ, WLCSP
ISL9123AIIC-EVZ	Evaluation board for ISL9123IICZ, WLCSP
ISL9123BII9-EVZ	Evaluation board for ISL9123II9Z, WLCSP

4. Revision History

Revision	Date	Description
1.01	Jul 26, 2023	Added info for ISL9123A and ISL9123B devices. Set register and bit name references to bold text. Updated section titles and figure titles. Updated BOM. Updated GUI screenshot for ISL9123.
1.00	Apr 1, 2022	Initial release

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