User's Manual

32

RZ/N1D Group, RZ/N1S Group, RZ/N1L Group

User's Manual: PWMTimer

RZ Family
RZ/N Series

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

How to Use This Manual

1. Objective and Target Users

This manual was written to explain the hardware functions and electrical characteristics of this LSI to the target users, i.e. those who will be using this LSI in the design of application systems. Target users are expected to understand the fundamentals of electrical circuits, logic circuits, and microcomputers.

This manual is organized in the following items: an overview of the product, descriptions of the CPU, system control functions, and peripheral functions, electrical characteristics of the device, and usage notes.

When designing an application system that includes this LSI, take all points to note into account.
Points to note are given in their contexts and at the final part of each section, and in the section giving usage notes.

The list of revisions is a summary of major points of revision or addition for earlier versions. It does not cover all revised items. For details on the revised points, see the actual locations in the manual.

The following documents have been prepared for reference.

■ Documents related to RZ/N1

Document Name	Document Number
RZ/N1D Group, RZ/N1S Group, RZ/N1L Group DATASHEET	R01DS0323EJ****
RZ/N1D Group, RZ/N1S Group, RZ/N1L Group User's Manual: System Introduction, Multiplexing, Electrical and Mechanical Information	R01UH0750EJ****
RZ/N1D Group, RZ/N1S Group, RZ/N1L Group User's Manual: System Control and Peripheral	R01UH0751EJ****
RZ/N1D Group, RZ/N1S Group, RZ/N1L Group User's Manual: Peripherals	R01UH0752EJ****
RZ/N1D Group, RZ/N1S Group, RZ/N1L Group User's Manual: R-IN Engine and Ethernet Peripherals	R01UH0753EJ****
RZ/N1D Group, RZ/N1S Group, RZ/N1L Group User's Manual: PWMTimer	R01UH0913EJ**** (this manual)

2. Description of Registers

Each register description includes a bit chart, illustrating the arrangement of bits, and a table of bits, describing the meanings of the bit settings. The standard format and notation for bit charts and tables are described below.

X.X.X [Register Name]

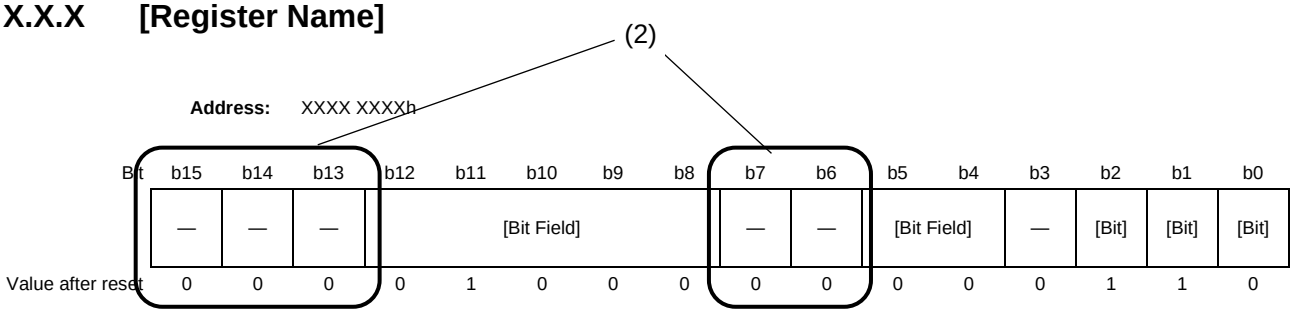


Table X.X [Register Name] Register Contents

Bit Position	Bit Name	Function	R/W
b12 to b8	[Bit Field]	[Description]	R/W
b5 to b4	[Bit Field]	[Description] 2'b00: Hi-Z 2'b01: L Output Others: Prohibited (3)	R/W
b2	[Bit]	[Description] 1'b0: Hi-Z 1'b1: Output (default)	R/W
b1	[Bit]	[Description] 1'b0: Hi-Z 1'b1: Output (default)	R/W
b0	[Bit]	[Description] 1'b0: Hi-Z 1'b1: Output	R/W (1)

(1) R/W: The bit or field is readable and writable.

R/(W): The bit or field is readable and writable. However, writing to this bit or field has some limitations. For details on the limitations, see the description or notes of respective registers.

R: The bit or field is readable. Writing to this bit or field has no effect.

W: The bit or field is writable. Reading to this bit or field is not guaranteed.

(2) Reserved. Make sure to use the specified value when writing to this bit or field; otherwise, the correct operation is not guaranteed.

(3) Setting prohibited. The correct operation is not guaranteed if such a setting is performed.

3. List of Abbreviations and Acronyms

Abbreviation	Full Form
AHB	Arm Advanced High-performance Bus
APB	Arm Advanced Peripheral Bus
AXI	Arm Advanced eXtensible Interface
bps	bits per second
CA7	Arm Cortex-A7 module
CM3	Arm Cortex-M3 module
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
Hi-Z	High Impedance
HSR	High-availability Seamless Redundancy
HW-RTOS	Hard Ware Real Time OS
I/O	Input/Output
INTC	Interrupt Controller
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connect
NoC	Network-on-Chip
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
UART	Universal Asynchronous Receiver/Transmitter
OTP	One Time Programmable
PTP	Precision Time Protocol
PRP	Parallel Redundancy Protocol
SoC	System On Chip

4. Description of the Access Size

Access size:

8 bits = Byte

16 bits = HalfWord

32 bits = Word

Table of Content

Section 1 PWMTimer

1.1 Overview

The PWMTimer provides 16 basic 16-bit counters with compare match and capture functions.

The PWMTimer features:

- Six filtered inputs with following features:
  - Bounce filter
  - Polarity selection
  - Force & Enable system
  - 40 external inputs (PWM_IN)
- 16 basic 16-bit counters that can be cascaded to generate 32-bit counter:
  - Can be synchronized with other counters
  - Programmable management of event on:
    - Clock: External input and clock prescaler
    - Up/Down: max/min value detection
    - Capture trigger: External input and max/min value detection
  - Organized in two PWM modules with for each, the following resources:
    - Eight 16-bit counters
    - Two clock prescalers 10-bit
    - 32-bit counter by cascading two 16-bit counters
    - Programmable resources for each counter can be configured in following functions:
      (1) Capture registers (up to 2)
      (2) Compare register
      (3) Registers for buffer transfer
      (4) Ranged mode (by setting the max value register)
  - Waveform with synchronized phases:
    - Sawtooth waveform
    - Triangular waveform
  - Event counting
- 16 outputs controllers with following features:
  - Force & Enable system
  - Polarity selection
  - 20 external outputs (PWM_OUT)
- Interruption management
- Operating frequency: 100 MHz

The potential pins which can be used by PWMTimer Top are:

- PWM_IN[39:0]
- PWM_OUT[19:0]

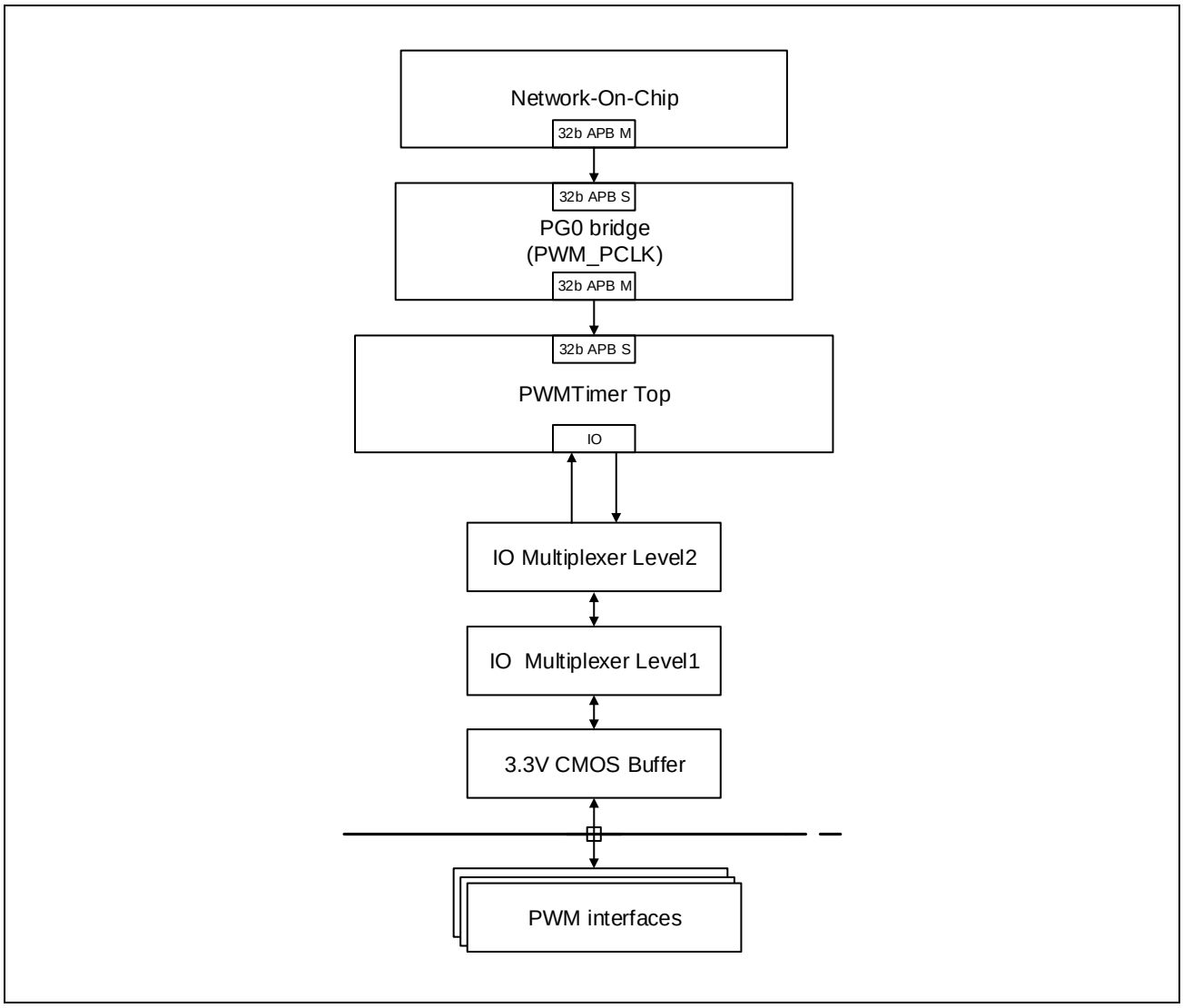


Figure 1.1 PWMTimer Top Interfaces and Connections

1.2 Signal Interfaces

Table 1.1 Signal Interface

Signal Name	Input Output	Description
Clock		
PWM_PCLK	Input	Internal bus clock (APB)
Interrupt		
PWM_Int	Output	Level sensitive interrupt output, Active High
External Signal		
PWM_IN[39:0]	Input	Input dedicated to PWMTimer Top. Each input can be linked to several inputs of PWMTimer Core.
PWM_OUT[19:0]	Output	Output dedicated to PWMTimer Top. Each output can be linked to several outputs of PWMTimer Core.

1.3 Register Map

NOTE

This section basically uses the following indexes.

- k: PWM module (k = 0..1)
- i: Single counter module (i = 0..7)
  - d: Each of two single counters (d = int(i/2), d = 0..3)
  - q: Each of four single counters (q = int(i/4), q = 0..1)
- r: Option register: OR (r = 0..3)

Table 1.2 Register Map

Address	Register Symbol	Register Name
4006 8000h + 2h × s	rPWMTimer_FILTER_IN_[s] (s = 0, 2, 10, 12)	Configuration of FilterIN Modules
4006 80A0h + 4h × n	rPWMTimer_FORCE_INPUT_[n] (n = 0..1)	Force the Output Value of FilterIN Modules
4006 8200h + 4h × n	rPWMTimer_OUTPUTCTRL_[n] (n = 0..3)	Configuration of OutputCtrl Modules
4006 8330h	rPWMTimer_OUTPUTCTRL_FORCE_OUT_0	Force the Output Value of OutputCtrl Modules
4006 8340h	rPWMTimer_OUTPUTCTRL_RELEASE_OUT	Release the Output Value Forced in OutputCtrl Modules
4006 8C00h	rPWMTimer_EVENT_MANAGER_INT_STATUS	Global Interrupt System Status
4006 8C80h	rPWMTimer_EVENT_MANAGER_INT_MASK	Mask for Global Interrupt System
4006 8CC4h	rPWMTimer_PWM_CMP1_MASK	Mask for PWM CMP1 Flags
4006 8CC8h	rPWMTimer_PWM_OVERFLOW_MASK	Mask for PWM Overflow Flags
4006 8CCCh	rPWMTimer_PWM_UNDERFLOW_MASK	Mask for PWM Underflow Flags
4006 8CD0h + 4h × r	rPWMTimer_HWSTORE_OR[r]_STORE_MASK (r = 1, 3)	Mask for PWM OR[r] Store Trigger Flags
4006 9000h + 400h × k	rPWMTimer_PWM_MODE_[k] (k = 0..1)	Management of the Timebase Mode
4006 9030h + 400h × k + 4h × q	rPWMTimer_PWM_CLOCK_[q]_[k] (q = 0..1, k = 0..1)	Configuration of the Clock Input in the PWM Modules
4006 9040h + 400h × k + 4h × d	rPWMTimer_PWM_UPDOWN_[d]_[k] (d = 0..3, k = 0..1)	Configuration of the Up/Down Input in the PWM Modules
4006 9070h + 400h × k	rPWMTimer_PWM_TRIG0_[k] (k = 0..1)	Configuration of the Trig0 Input in the PWM Modules
4006 9080h + 400h × k	rPWMTimer_PWM_TRIG1_[k] (k = 0..1)	Configuration of the Trig1 Input in the PWM Modules
4006 90C0h + 400h × k + 4h × d	rPWMTimer_PWM_OUTPUTGEN[d]_[k] (d = 0..3, k = 0..1)	Configuration of the Outputs Generator in the PWM Modules
4006 90E0h + 400h × k	rPWMTimer_PWM_BLOCK_CLOCK_[k] (k = 0..1)	Configuration of the Block_Clock in the PWM Module
4006 9100h + 400h × k + 4h × i	rPWMTimer_TIMEBASE_[i]_[k] (i = 0..7, k = 0..1)	Current Counter Value of the 16bits Timebase
4006 9120h + 400h × k + 4h × n	rPWMTimer_TIMEBASE_[n*2][n*2+1]_[k] (n = 0..3, k = 0..1)	Current Counter Value of the 32bits Cascaded Timebase
4006 9130h + 400h × k + 4h × n	rPWMTimer_TIMEBASE_[(n+1)*2-1][(n+1)*2]_[k] (n = 0..2, k = 0..1)	Current Counter Value of the 32bits Cascaded Timebase
4006 9140h + 400h × k + 4h × i	rPWMTimer_SCALEVALUE_[i]_[k] (i = 0..7, k = 0..1)	Cascade Value Setting
4006 91A0h + 400h × k + 4h × q	rPWMTimer_TIMEBASE_MUX_[q]_[k] (q = 0..1, k = 0..1)	Configuration of the Compare/Capture System Input Mux Table

Address	Register Symbol	Register Name
4006 91B0h + 400h × k + 4h × i	rPWMTimer_HWSTORE_CONF_[i]_[k] (i = 0..7, k = 0..1)	Configuration of the Hardware Store Trigger System in the PWM Modules
4006 91D0h + 400h × k + 4h × i	rPWMTimer_HWSTORE_MUX_[i]_[k] (i = 0..7, k = 0..1)	Multiplexers Configuration of the Hardware Store Trigger System in the PWM Modules
4006 91F0h + 400h × k	rPWMTimer_HWSTORE_LOCK_[k] (k = 0..1)	Lock or Read Lock Status of the Option Registers in the PWM Modules
4006 91F4h + 400h × k	rPWMTimer_HWSTORE_UNLOCK_[k] (k = 0..1)	Unlock the Option Registers in the PWM Modules
4006 9200h + 400h × k + 40h × r + 4h × i	rPWMTimer_OPTIONREG[r]_[i]_[k] (i = 0..7, r = 0..3, k = 0..1)	Option Register [r] Value of the 16bits Timebase
4006 9220h + 400h × k + 40h × r + 4h × n	rPWMTimer_OPTIONREG[r]_[n*2][n*2+1]_[k] (n = 0..3, r = 0..3, k = 0..1)	Option Register [r] Value of the 32bits Cascaded Timebase
4006 9230h + 400h × k + 40h × r + 4h × n	rPWMTimer_OPTIONREG[r]_[(n+1)*2-1][(n+1)*2]_[k] (n = 0..2, r = 0..3, k = 0..1)	Option Register [r] Value of the 32bits Cascaded Timebase
4006 A010h	rPWMTimer_PWM_SOFTSTART	Set the Count Enable Input of the PWM Modules in "Start" Mode
4006 A018h	rPWMTimer_PWM_SOFTSTOP	Set the Count Enable Input of the PWM Modules in "Stop" Mode
4006 A040h	rPWMTimer_PWM_SOFTUPDOWN_0	Set the Up/Down Outputs of the PWM Modules
4006 A050h	rPWMTimer_PWM_SOFTRESET	Set the Reset Trigger of the Timebases
4006 A0D4h	rPWMTimer_PWM_CMP1_FLAG_POLARITY	PWM CMP1 Flags Configuration
4006 A0DCh	rPWMTimer_PWM_CMP1_FLAG	PWM CMP1 Flags
4006 A108h	rPWMTimer_PWM_MAX_OVERFLOW	PWM Overflow Detection Flags
4006 A10Ch	rPWMTimer_PWM_MIN_UNDERFLOW	PWM Underflow Detection Flags
4006 A1D0h + 4h × r	rPWMTimer_HWSTORE_OR[r]_STORE_FLAG (r = 1, 3)	PWM OR[r] Store Trigger Flags
4006 B100h + 4h × s	rPWMTimer_ROUTING_IN_[s] (s = 0, 2)	Configuration of the PWMTimer's Multiplexed Inputs "IN"
4006 B200h + 4h × n	rPWMTimer_ROUTING_OUT_[n] (n = 0..3)	Configuration of the PWMTimer's Multiplexed Outputs "OUT"
4006 B800h	rPWMTimer_ROUTING_OUTCTRL_0	Configuration of OutputCtrl0 Module's Inputs
4006 B804h	rPWMTimer_ROUTING_OUTCTRL_1	Configuration of OutputCtrl1 Module's Inputs
4006 B808h	rPWMTimer_ROUTING_OUTCTRL_2	Configuration of OutputCtrl2 Module's Inputs
4006 B80Ch	rPWMTimer_ROUTING_OUTCTRL_3	Configuration of OutputCtrl3 Module's Inputs
4006 B810h	rPWMTimer_ROUTING_OUTCTRL_4	Configuration of OutputCtrl4 Module's Inputs
4006 B814h	rPWMTimer_ROUTING_OUTCTRL_5	Configuration of OutputCtrl5 Module's Inputs
4006 B818h	rPWMTimer_ROUTING_OUTCTRL_6	Configuration of OutputCtrl6 Module's Inputs
4006 B81Ch	rPWMTimer_ROUTING_OUTCTRL_7	Configuration of OutputCtrl7 Module's Inputs
4006 B820h	rPWMTimer_ROUTING_OUTCTRL_8	Configuration of OutputCtrl8 Module's Inputs
4006 B824h	rPWMTimer_ROUTING_OUTCTRL_9	Configuration of OutputCtrl9 Module's Inputs
4006 B828h	rPWMTimer_ROUTING_OUTCTRL_10	Configuration of OutputCtrl10 Module's Inputs
4006 B82Ch	rPWMTimer_ROUTING_OUTCTRL_11	Configuration of OutputCtrl11 Module's Inputs
4006 B830h	rPWMTimer_ROUTING_OUTCTRL_12	Configuration of OutputCtrl12 Module's Inputs
4006 B834h	rPWMTimer_ROUTING_OUTCTRL_13	Configuration of OutputCtrl13 Module's Inputs
4006 B838h	rPWMTimer_ROUTING_OUTCTRL_14	Configuration of OutputCtrl14 Module's Inputs
4006 B83Ch	rPWMTimer_ROUTING_OUTCTRL_15	Configuration of OutputCtrl15 Module's Inputs

1.4 Register Description

1.4.1 rPWMTimer_FILTER_IN_[s] − Configuration of FilterIN Modules (s = 0, 10)

For FilterIN module 0..1, 10..11 (For Trig1 and Trig0)

These registers use a specific mask system.

Address: 4006 8000h + 2h × s

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	bMOST_SIGNIFICANT_BIT_REGISTER_ACCESS	—		bBOUNCE_STEP_[s+1]	bBOUNCE_THRESHOLD_[s+1]										—	bPOLAR_IN_[s+1]
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	bLEAST_SIGNIFICANT_BIT_REGISTER_ACCESS	—		bBOUNCE_STEP_[s]	bBOUNCE_THRESHOLD_[s]										—	bPOLAR_IN_[s]
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.3 rPWMTimer_FILTER_IN_[s] Register Contents

Bit Position	Bit Name	Function	R/W
b31	bMOST_SIGNIFICANT_BIT_REGISTER_ACCESS	Always read as 0. Writing '1' in this register activates the write enable of the 16 most significant bits of the register for the current access.	W
b30 to b29	Reserved	Keep initial value.	R/W
b28	bBOUNCE_STEP_[s+1]	Clock Divider Used by the Bounce Filter of FilterIN [s+e]: 1'b0: PWM_PCLK/8 1'b1: PWM_PCLK/2048 For this bit e:1 (FilterIN 1,11)	R/W
b27 to b18	bBOUNCE_THRESHOLD_[s+1]	Configuration of the Bounce Filter of FilterIN [s+e]: 10'd0: Direct (No bounce filter) 10'd1: 1 bounce clock period 10'd2: 2 bounce clock periods 10'dX: X bounce clock periods 10'd1023: 1023 bounce clock periods For these bits e:1 (FilterIN 1,11)	R/W
b17	Reserved	Keep initial value.	R/W
b16	bPOLAR_IN_[s+1]	Polarity Selection of FilterIN [s+e]: 1'b0: Direct 1'b1: Inverted For this bit e:1 (FilterIN 1,11)	R/W
b15	bLEAST_SIGNIFICANT_BIT_REGISTER_ACCESS	Always read as 0. Writing '1' in this register activates the write enable of the 16 least significant bits of the register for the current access.	W
b14 to b13	Reserved	Keep initial value.	R/W
b12	bBOUNCE_STEP_[s]	See above bBOUNCE_STEP_[s+1] with e:0 (FilterIN 0,10)	R/W
b11 to b2	bBOUNCE_THRESHOLD_[s]	See above bBOUNCE_THRESHOLD_[s+1] with e:0 (FilterIN 0,10)	R/W

Bit Position	Bit Name	Function	R/W
b1	Reserved	Keep initial value.	R/W
b0	bPOLAR_IN_[s]	See above bPOLAR_IN_[s+1] with e:0 (FilterIN 0,10)	R/W

1.4.2 rPWMTimer_FILTER_IN_[s] − Configuration of FilterIN Modules (s = 2, 12)

For FilterIN module 2, 12 (For ClockIn)

These registers use a specific mask system.

Address: 4006 8000h + 2h × s

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—								—							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	bLEAST_SIGNIFICANT_BIT_REGISTER_ACCESS	—		bBOUNCE_STEP_[s]	bBOUNCE_THRESHOLD_[s]										—	bPOLAR_IN_[s]
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.4 rPWMTimer_FILTER_IN_[s] Register Contents

Bit Position	Bit Name	Function	R/W
b31	Reserved	Write with 0.	W
b30 to b16	Reserved	Keep initial value.	R/W
b15	bLEAST_SIGNIFICANT_BIT_REGISTER_ACCESS	Always read as 0. Writing '1' in this register activates the write enable of the 16 least significant bits of the register for the current access.	W
b14 to b13	Reserved	Keep initial value.	R/W
b12	bBOUNCE_STEP_[s]	Clock Divider Used by the Bounce Filter of FilterIN [s]: 1'b0: PWM_PCLK/8 1'b1: PWM_PCLK/2048 (FilterIN 2, 12)	R/W
b11 to b2	bBOUNCE_THRESHOLD_[s]	Configuration of the Bounce Filter of FilterIN [s]: 10'd0: Direct (No bounce filter) 10'd1: 1 bounce clock period 10'd2: 2 bounce clock periods 10'dX: X bounce clock periods 10'd1023: 1023 bounce clock periods (FilterIN 2, 12)	R/W
b1	Reserved	Keep initial value.	R/W
b0	bPOLAR_IN_[s]	Polarity Selection of FilterIN [s]: 1'b0: Direct 1'b1: Inverted (FilterIN 2, 12)	R/W

1.4.3 rPWMTimer_FORCE_INPUT_[n] − Force the Output Value of FilterIN Modules (n = 0..1)

For FilterIN module 0..2, 10..12. These registers use a specific mask system.

Address: 4006 80A0h + 4h × n

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—		—	—		—	—		—	—		—	—		—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—		bMASK_SET_RESET_[n*10+2]	bFORCE_IN_[n*10+2]		bMASK_SET_RESET_[n*10+1]	bFORCE_IN_[n*10+1]		bMASK_SET_RESET_[n*10]	bFORCE_IN_[n*10]	
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.5 rPWMTimer_FORCE_INPUT_[n] Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b30	Reserved	Always read as 0.	R
b29	Reserved	Write with 0.	W
b28 to b27	Reserved	Keep initial value.	R/W
b26	Reserved	Write with 0.	W
b25 to b24	Reserved	Keep initial value.	R/W
b23	Reserved	Write with 0.	W
b22 to b21	Reserved	Keep initial value.	R/W
b20	Reserved	Write with 0.	W
b19 to b18	Reserved	Keep initial value.	R/W
b17	Reserved	Write with 0.	W
b16 to b15	Reserved	Keep initial value.	R/W
b14	Reserved	Write with 0.	W
b13 to b12	Reserved	Keep initial value.	R/W
b11	Reserved	Write with 0.	W
b10 to b9	Reserved	Keep initial value.	R/W
b8	bMASK_SET_RESET_[n*10+2]	Always read as 0. Writing '1' in this register activates the write enable of the bits 7 and 6 of the register for the current access.	W
b7 to b6	bFORCE_IN_[n*10+2]	Force Configuration for FilterIN [n*10+e]: 2'b00: Direct, output follows the input. 2'b01: Output is forced to "1". 2'b1X: Output is forced to "0". For these bits e:2 (FilterIN 2, 12)	R/W
b5	bMASK_SET_RESET_[n*10+1]	Always read as 0. Writing '1' in this register activates the write enable of the bits 4 and 3 of the register for the current access.	W
b4 to b3	bFORCE_IN_[n*10+1]	See above bFORCE_IN_[n*10+2] with e:1 (FilterIN 1, 11)	R/W
b2	bMASK_SET_RESET_[n*10]	Always read as 0. Writing '1' in this register activates the write enable of the bits 1 and 0 of the register for the current access.	W
b1 to b0	bFORCE_IN_[n*10]	See above bFORCE_IN_[n*10+2] with e:0 (FilterIN 0, 10)	R/W

1.4.4 rPWMTimer_OUTPUTCTRL_[n] − Configuration of OutputCtrl Modules (n = 0..3)

For OutputCtrl module 0..15.

Address: 4006 8200h +4h × n

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	bBYPASS_MODE_[n*4+3]	—				bINVERTED_SET_[n*4+3]	—		bBYPASS_MODE_[n*4+2]	—				bINVERTED_SET_[n*4+2]	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	bBYPASS_MODE_[n*4+1]	—				bINVERTED_SET_[n*4+1]	—		bBYPASS_MODE_[n*4]	—				bINVERTED_SET_[n*4]	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.6 rPWMTimer_OUTPUTCTRL_[n] Register Contents

Bit Position	Bit Name	Function	R/W
b31	Reserved	Keep initial value.	R/W
b30	bBYPASS_MODE_[n*4+3]	Select OutputCtrl [n*4+e] Mode Should be set to 1. For this bit e:3 (OutputCtrl 3, 7, 11, 15)	R/W
b29 to b26	Reserved	Keep initial value.	R/W
b25	bINVERTED_SET_[n*4+3]	Select the Polarity of the Input of OutputCtrl [n*4+e]: 1'b0: Direct mode 1'b1: Inverted mode For this bit e:3 (OutputCtrl 3, 7, 11, 15)	R/W
b24 to b23	Reserved	Keep initial value.	R/W
b22	bBYPASS_MODE_[n*4+2]	See above bBYPASS_MODE_[n*4+3] with e:2 (OutputCtrl 2, 6, 10, 14)	R/W
b21 to b18	Reserved	Keep initial value.	R/W
b17	bINVERTED_SET_[n*4+2]	See above bINVERTED_SET_[n*4+3] with e:2 (OutputCtrl 2, 6, 10, 14)	R/W
b16 to b15	Reserved	Keep initial value.	R/W
b14	bBYPASS_MODE_[n*4+1]	See above bBYPASS_MODE_[n*4+3] with e:1 (OutputCtrl 1, 5, 9, 13)	R/W
b13 to b10	Reserved	Keep initial value.	R/W
b9	bINVERTED_SET_[n*4+1]	See above bINVERTED_SET_[n*4+3] with e:1 (OutputCtrl 1, 5, 9, 13)	R/W
b8 to b7	Reserved	Keep initial value.	R/W
b6	bBYPASS_MODE_[n*4]	See above bBYPASS_MODE_[n*4+3] with e:0 (OutputCtrl 0, 4, 8, 12)	R/W
b5 to b2	Reserved	Keep initial value.	R/W
b1	bINVERTED_SET_[n*4]	See above bINVERTED_SET_[n*4+3] with e:0 (OutputCtrl 0, 4, 8, 12)	R/W
b0	Reserved	Keep initial value.	R/W

1.4.5 rPWMTimer_OUTPUTCTRL_FORCE_OUT_0 − Force the Output Value of OutputCtrl Modules

Force the output value of OutputCtrl module 0..15.

This register uses a specific mask system. The 16 most significant bits are used as mask for the 16 least significant bits representing the data to be written.

Address: 4006 8330h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	bFORCE_OUT_MASK															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	bFORCE_OUT_15	bFORCE_OUT_14	bFORCE_OUT_13	bFORCE_OUT_12	bFORCE_OUT_11	bFORCE_OUT_10	bFORCE_OUT_9	bFORCE_OUT_8	bFORCE_OUT_7	bFORCE_OUT_6	bFORCE_OUT_5	bFORCE_OUT_4	bFORCE_OUT_3	bFORCE_OUT_2	bFORCE_OUT_1	bFORCE_OUT_0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.7 rPWMTimer_OUTPUTCTRL_FORCE_OUT_0 Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b16	bFORCE_OUT_MASK	Always read as 0. Writing '1' in a bit of this register activates the write enable of the corresponding bit for the current access.	W
b15	bFORCE_OUT_15	Force Output Configuration for OutputCtrl [e]: This bit is W with mask. Write "1" sets output to "1". Write "0" sets output to "0". Write has no effect if the corresponding Mask bit = "0". For this bit e:15 (OutputCtrl 15)	W
b14	bFORCE_OUT_14	See above with e:14 (OutputCtrl 14)	W
b13	bFORCE_OUT_13	See above with e:13 (OutputCtrl 13)	W
b12	bFORCE_OUT_12	See above with e:12 (OutputCtrl 12)	W
b11	bFORCE_OUT_11	See above with e:11 (OutputCtrl 11)	W
b10	bFORCE_OUT_10	See above with e:10 (OutputCtrl 10)	W
b9	bFORCE_OUT_9	See above with e:9 (OutputCtrl 9)	W
b8	bFORCE_OUT_8	See above with e:8 (OutputCtrl 8)	W
b7	bFORCE_OUT_7	See above with e:7 (OutputCtrl 7)	W
b6	bFORCE_OUT_6	See above with e:6 (OutputCtrl 6)	W
b5	bFORCE_OUT_5	See above with e:5 (OutputCtrl 5)	W
b4	bFORCE_OUT_4	See above with e:4 (OutputCtrl 4)	W
b3	bFORCE_OUT_3	See above with e:3 (OutputCtrl 3)	W
b2	bFORCE_OUT_2	See above with e:2 (OutputCtrl 2)	W
b1	bFORCE_OUT_1	See above with e:1 (OutputCtrl 1)	W
b0	bFORCE_OUT_0	See above with e:0 (OutputCtrl 0)	W

1.4.6 rPWMTimer_OUTPUTCTRL_RELEASE_OUT − Release the Output Value Forced in OutputCtrl Modules

Address: 4006 8340h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	bRELEASE_OUT_15	bRELEASE_OUT_14	bRELEASE_OUT_13	bRELEASE_OUT_12	bRELEASE_OUT_11	bRELEASE_OUT_10	bRELEASE_OUT_9	bRELEASE_OUT_8	bRELEASE_OUT_7	bRELEASE_OUT_6	bRELEASE_OUT_5	bRELEASE_OUT_4	bRELEASE_OUT_3	bRELEASE_OUT_2	bRELEASE_OUT_1	bRELEASE_OUT_0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.8 rPWMTimer_OUTPUTCTRL_RELEASE_OUT Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b16	Reserved	Write with 0.	W
b15	bRELEASE_OUT_15	Release Force Output for OutputCtrl [e]: Write "0" has no effect. Write "1" release output force value. Initial output is released. For this bit e:15 (OutputCtrl 15)	W
b14	bRELEASE_OUT_14	See above with e:14 (OutputCtrl 14)	W
b13	bRELEASE_OUT_13	See above with e:13 (OutputCtrl 13)	W
b12	bRELEASE_OUT_12	See above with e:12 (OutputCtrl 12)	W
b11	bRELEASE_OUT_11	See above with e:11 (OutputCtrl 11)	W
b10	bRELEASE_OUT_10	See above with e:10 (OutputCtrl 10)	W
b9	bRELEASE_OUT_9	See above with e:9 (OutputCtrl 9)	W
b8	bRELEASE_OUT_8	See above with e:8 (OutputCtrl 8)	W
b7	bRELEASE_OUT_7	See above with e:7 (OutputCtrl 7)	W
b6	bRELEASE_OUT_6	See above with e:6 (OutputCtrl 6)	W
b5	bRELEASE_OUT_5	See above with e:5 (OutputCtrl 5)	W
b4	bRELEASE_OUT_4	See above with e:4 (OutputCtrl 4)	W
b3	bRELEASE_OUT_3	See above with e:3 (OutputCtrl 3)	W
b2	bRELEASE_OUT_2	See above with e:2 (OutputCtrl 2)	W
b1	bRELEASE_OUT_1	See above with e:1 (OutputCtrl 1)	W
b0	bRELEASE_OUT_0	See above with e:0 (OutputCtrl 0)	W

1.4.7 rPWMTimer_EVENT_MANAGER_INT_STATUS − Global Interrupt System Status

Address: 4006 8C00h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	bINT_FROM_HWSTORE_OR3_STORE_FLAG	—	bINT_FROM_HWSTORE_OR1_STORE_FLAG	—	bINT_FROM_PWM_UNDERFLOW	bINT_FROM_PWM_OVERFLOW	bINT_FROM_PWM_CMP1_FLAG	—								
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.9 rPWMTimer_EVENT_MANAGER_INT_STATUS Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b16	Reserved	Always read as 0.	R
b15	bINT_FROM_HWSTORE_OR3_STORE_FLAG	Interrupt Status from rPWMTimer_HWSTORE_OR3_STORE_FLAG Flags Register This bit is set to "1" by hardware when a not-masked flag is equal to "1". This bit is set to "0" by hardware when all the not-masked flags are equal to "0" or when all the flags are masked.	R
b14	Reserved	Always read as 0.	R
b13	bINT_FROM_HWSTORE_OR1_STORE_FLAG	Interrupt Status from rPWMTimer_HWSTORE_OR1_STORE_FLAG Flags Register See above bINT_FROM_HWSTORE_OR3_STORE_FLAG	R
b12	Reserved	Always read as 0.	R
b11	bINT_FROM_PWM_UNDERFLOW	Interrupt Status from rPWMTimer_PWM_MIN_UNDERFLOW Flags Register See above bINT_FROM_HWSTORE_OR3_STORE_FLAG	R
b10	bINT_FROM_PWM_OVERFLOW	Interrupt Status from rPWMTimer_PWM_MAX_OVERFLOW Flags Register See above bINT_FROM_HWSTORE_OR3_STORE_FLAG	R
b9	bINT_FROM_PWM_CMP1_FLAG	Interrupt Status from rPWMTimer_PWM_CMP1_FLAG Flags Register See above bINT_FROM_HWSTORE_OR3_STORE_FLAG	R
b8 to b0	Reserved	Always read as 0.	R

1.4.8 rPWMTimer_EVENT_MANAGER_INT_MASK − Mask for Global Interrupt System

Address: 4006 8C80h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	bMASK_FOR_HWSTORE_OR3_STORE_FLAG	—	bMASK_FOR_HWSTORE_OR1_STORE_FLAG	—	bMASK_FOR_PWM_UNDERFLOW	bMASK_FOR_PWM_OVERFLOW	bMASK_FOR_PWM_CMP1_FLAG	—								
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.10 rPWMTimer_EVENT_MANAGER_INT_MASK Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b16	Reserved	Always read as 0.	R
b15	bMASK_FOR_HWSTORE_OR3_STORE_FLAG	Mask for Interrupt Status from rPWMTimer_HWSTORE_OR3_STORE_FLAG Flags Register 1'b0: Register is masked; flags from this register cannot trigger an interrupt. 1'b1: Register is not masked; not-masked flags from this register trigger an interrupt.	R/W
b14	Reserved	Keep initial value.	R/W
b13	bMASK_FOR_HWSTORE_OR1_STORE_FLAG	Mask for Interrupt Status from rPWMTimer_HWSTORE_OR1_STORE_FLAG Flags Register See above bMASK_FOR_HWSTORE_OR3_STORE_FLAG	R/W
b12	Reserved	Keep initial value.	R/W
b11	bMASK_FOR_PWM_UNDERFLOW	Mask for Interrupt Status from rPWMTimer_PWM_MIN_UNDERFLOW Flags Register See above bMASK_FOR_HWSTORE_OR3_STORE_FLAG	R/W
b10	bMASK_FOR_PWM_OVERFLOW	Mask for Interrupt Status from rPWMTimer_PWM_MAX_OVERFLOW Flags Register See above bMASK_FOR_HWSTORE_OR3_STORE_FLAG	R/W
b9	bMASK_FOR_PWM_CMP1_FLAG	Mask for Interrupt Status from rPWMTimer_PWM_CMP1_FLAG Flags Register See above bMASK_FOR_HWSTORE_OR3_STORE_FLAG	R/W
b8 to b0	Reserved	Keep initial value.	R/W

1.4.9 rPWMTimer_PWM_CMP1_MASK − Mask for PWM CMP1 Flags

Address: 4006 8CC4h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	bPWM_CMP1_MASK_15	bPWM_CMP1_MASK_14	bPWM_CMP1_MASK_13	bPWM_CMP1_MASK_12	bPWM_CMP1_MASK_11	bPWM_CMP1_MASK_10	bPWM_CMP1_MASK_9	bPWM_CMP1_MASK_8	bPWM_CMP1_MASK_7	bPWM_CMP1_MASK_6	bPWM_CMP1_MASK_5	bPWM_CMP1_MASK_4	bPWM_CMP1_MASK_3	bPWM_CMP1_MASK_2	bPWM_CMP1_MASK_1	bPWM_CMP1_MASK_0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.11 rPWMTimer_PWM_CMP1_MASK Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b16	Reserved	Keep initial value.	R/W
b15	bPWM_CMP1_MASK_15	Mask for CMP1 Status Flag of Single Counter [i] from PWM [k] 1'b0: Flag is masked; This flag cannot trigger an interrupt. 1'b1: Flag is not masked; This flag can trigger an interrupt. For this bit i:7 and k:1 (PWM 1: single counter 7)	R/W
b14	bPWM_CMP1_MASK_14	See above with i:6 and k:1 (PWM 1: single counter 6)	R/W
b13	bPWM_CMP1_MASK_13	See above with i:5 and k:1 (PWM 1: single counter 5)	R/W
b12	bPWM_CMP1_MASK_12	See above with i:4 and k:1 (PWM 1: single counter 4)	R/W
b11	bPWM_CMP1_MASK_11	See above with i:3 and k:1 (PWM 1: single counter 3)	R/W
b10	bPWM_CMP1_MASK_10	See above with i:2 and k:1 (PWM 1: single counter 2)	R/W
b9	bPWM_CMP1_MASK_9	See above with i:1 and k:1 (PWM 1: single counter 1)	R/W
b8	bPWM_CMP1_MASK_8	See above with i:0 and k:1 (PWM 1: single counter 0)	R/W
b7	bPWM_CMP1_MASK_7	See above with i:7 and k:0 (PWM 0: single counter 7)	R/W
b6	bPWM_CMP1_MASK_6	See above with i:6 and k:0 (PWM 0: single counter 6)	R/W
b5	bPWM_CMP1_MASK_5	See above with i:5 and k:0 (PWM 0: single counter 5)	R/W
b4	bPWM_CMP1_MASK_4	See above with i:4 and k:0 (PWM 0: single counter 4)	R/W
b3	bPWM_CMP1_MASK_3	See above with i:3 and k:0 (PWM 0: single counter 3)	R/W
b2	bPWM_CMP1_MASK_2	See above with i:2 and k:0 (PWM 0: single counter 2)	R/W
b1	bPWM_CMP1_MASK_1	See above with i:1 and k:0 (PWM 0: single counter 1)	R/W
b0	bPWM_CMP1_MASK_0	See above with i:0 and k:0 (PWM 0: single counter 0)	R/W

1.4.10 rPWMTimer_PWM_OVERFLOW_MASK − Mask for PWM Overflow Flags

Address: 4006 8CC8h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	bPWM_OVERFLOW_MASK_7_1	bPWM_OVERFLOW_MASK_6_1	bPWM_OVERFLOW_MASK_5_1	bPWM_OVERFLOW_MASK_4_1	bPWM_OVERFLOW_MASK_3_1	bPWM_OVERFLOW_MASK_2_1	bPWM_OVERFLOW_MASK_1_1	bPWM_OVERFLOW_MASK_0_1	bPWM_OVERFLOW_MASK_7_0	bPWM_OVERFLOW_MASK_6_0	bPWM_OVERFLOW_MASK_5_0	bPWM_OVERFLOW_MASK_4_0	bPWM_OVERFLOW_MASK_3_0	bPWM_OVERFLOW_MASK_2_0	bPWM_OVERFLOW_MASK_1_0	bPWM_OVERFLOW_MASK_0_0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.12 rPWMTimer_PWM_OVERFLOW_MASK Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b16	Reserved	Keep initial value.	R/W
b15	bPWM_OVERFLOW_MASK_7_1	Mask for Overflow Flag from the Single Counter [i] of PWM [k] 1'b0: Flag is masked; This flag cannot trigger an interrupt. 1'b1: Flag is not masked; This flag can trigger an interrupt. For this bit i:7 and k:1 (PWM 1: single counter 7)	R/W
b14	bPWM_OVERFLOW_MASK_6_1	See above with i:6 and k:1 (PWM 1: single counter 6)	R/W
b13	bPWM_OVERFLOW_MASK_5_1	See above with i:5 and k:1 (PWM 1: single counter 5)	R/W
b12	bPWM_OVERFLOW_MASK_4_1	See above with i:4 and k:1 (PWM 1: single counter 4)	R/W
b11	bPWM_OVERFLOW_MASK_3_1	See above with i:3 and k:1 (PWM 1: single counter 3)	R/W
b10	bPWM_OVERFLOW_MASK_2_1	See above with i:2 and k:1 (PWM 1: single counter 2)	R/W
b9	bPWM_OVERFLOW_MASK_1_1	See above with i:1 and k:1 (PWM 1: single counter 1)	R/W
b8	bPWM_OVERFLOW_MASK_0_1	See above with i:0 and k:1 (PWM 1: single counter 0)	R/W
b7	bPWM_OVERFLOW_MASK_7_0	See above with i:7 and k:0 (PWM 0: single counter 7)	R/W
b6	bPWM_OVERFLOW_MASK_6_0	See above with i:6 and k:0 (PWM 0: single counter 6)	R/W
b5	bPWM_OVERFLOW_MASK_5_0	See above with i:5 and k:0 (PWM 0: single counter 5)	R/W
b4	bPWM_OVERFLOW_MASK_4_0	See above with i:4 and k:0 (PWM 0: single counter 4)	R/W
b3	bPWM_OVERFLOW_MASK_3_0	See above with i:3 and k:0 (PWM 0: single counter 3)	R/W
b2	bPWM_OVERFLOW_MASK_2_0	See above with i:2 and k:0 (PWM 0: single counter 2)	R/W
b1	bPWM_OVERFLOW_MASK_1_0	See above with i:1 and k:0 (PWM 0: single counter 1)	R/W
b0	bPWM_OVERFLOW_MASK_0_0	See above with i:0 and k:0 (PWM 0: single counter 0)	R/W

1.4.11 rPWMTimer_PWM_UNDERFLOW_MASK − Mask for PWM Underflow Flags

Address: 4006 8CCCh

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	bPWM_UNDERFLOW_MASK_7_1	bPWM_UNDERFLOW_MASK_6_1	bPWM_UNDERFLOW_MASK_5_1	bPWM_UNDERFLOW_MASK_4_1	bPWM_UNDERFLOW_MASK_3_1	bPWM_UNDERFLOW_MASK_2_1	bPWM_UNDERFLOW_MASK_1_1	bPWM_UNDERFLOW_MASK_0_1	bPWM_UNDERFLOW_MASK_7_0	bPWM_UNDERFLOW_MASK_6_0	bPWM_UNDERFLOW_MASK_5_0	bPWM_UNDERFLOW_MASK_4_0	bPWM_UNDERFLOW_MASK_3_0	bPWM_UNDERFLOW_MASK_2_0	bPWM_UNDERFLOW_MASK_1_0	bPWM_UNDERFLOW_MASK_0_0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.13 rPWMTimer_PWM_UNDERFLOW_MASK Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b16	Reserved	Keep initial value.	R/W
b15	bPWM_UNDERFLOW_MASK_7_1	Mask for Underflow Flag from the Single Counter [i] of PWM [k] 1'b0: Flag is masked; This flag cannot trigger an interrupt. 1'b1: Flag is not masked; This flag can trigger an interrupt. For this bit i:7 and k:1 (PWM 1: single counter 7)	R/W
b14	bPWM_UNDERFLOW_MASK_6_1	See above with i:6 and k:1 (PWM 1: single counter 6)	R/W
b13	bPWM_UNDERFLOW_MASK_5_1	See above with i:5 and k:1 (PWM 1: single counter 5)	R/W
b12	bPWM_UNDERFLOW_MASK_4_1	See above with i:4 and k:1 (PWM 1: single counter 4)	R/W
b11	bPWM_UNDERFLOW_MASK_3_1	See above with i:3 and k:1 (PWM 1: single counter 3)	R/W
b10	bPWM_UNDERFLOW_MASK_2_1	See above with i:2 and k:1 (PWM 1: single counter 2)	R/W
b9	bPWM_UNDERFLOW_MASK_1_1	See above with i:1 and k:1 (PWM 1: single counter 1)	R/W
b8	bPWM_UNDERFLOW_MASK_0_1	See above with i:0 and k:1 (PWM 1: single counter 0)	R/W
b7	bPWM_UNDERFLOW_MASK_7_0	See above with i:7 and k:0 (PWM 0: single counter 7)	R/W
b6	bPWM_UNDERFLOW_MASK_6_0	See above with i:6 and k:0 (PWM 0: single counter 6)	R/W
b5	bPWM_UNDERFLOW_MASK_5_0	See above with i:5 and k:0 (PWM 0: single counter 5)	R/W
b4	bPWM_UNDERFLOW_MASK_4_0	See above with i:4 and k:0 (PWM 0: single counter 4)	R/W
b3	bPWM_UNDERFLOW_MASK_3_0	See above with i:3 and k:0 (PWM 0: single counter 3)	R/W
b2	bPWM_UNDERFLOW_MASK_2_0	See above with i:2 and k:0 (PWM 0: single counter 2)	R/W
b1	bPWM_UNDERFLOW_MASK_1_0	See above with i:1 and k:0 (PWM 0: single counter 1)	R/W
b0	bPWM_UNDERFLOW_MASK_0_0	See above with i:0 and k:0 (PWM 0: single counter 0)	R/W

1.4.12 rPWMTimer_HWSTORE_OR[r]_STORE_MASK − Mask for PWM OR[r] Store Trigger Flags (r = 1, 3)

Address: 4006 8CD0h + 4h × r

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	bOR[r]_STORE_MASK_15	bOR[r]_STORE_MASK_14	bOR[r]_STORE_MASK_13	bOR[r]_STORE_MASK_12	bOR[r]_STORE_MASK_11	bOR[r]_STORE_MASK_10	bOR[r]_STORE_MASK_9	bOR[r]_STORE_MASK_8	bOR[r]_STORE_MASK_7	bOR[r]_STORE_MASK_6	bOR[r]_STORE_MASK_5	bOR[r]_STORE_MASK_4	bOR[r]_STORE_MASK_3	bOR[r]_STORE_MASK_2	bOR[r]_STORE_MASK_1	bOR[r]_STORE_MASK_0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.14 rPWMTimer_HWSTORE_OR[r]_STORE_MASK Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b16	Reserved	Keep initial value.	R/W
b15	bOR[r]_STORE_MASK_15	Mask for OR[r] Store Trigger Flag from the Single Counter [i] from PWM [k] 1'b0: Flag is masked; This flag cannot trigger an interrupt. 1'b1: Flag is not masked; This flag can trigger an interrupt. For this bit i:7 and k:1 (PWM 1: single counter 7)	R/W
b14	bOR[r]_STORE_MASK_14	See above with i:6 and k:1 (PWM 1: single counter 6)	R/W
b13	bOR[r]_STORE_MASK_13	See above with i:5 and k:1 (PWM 1: single counter 5)	R/W
b12	bOR[r]_STORE_MASK_12	See above with i:4 and k:1 (PWM 1: single counter 4)	R/W
b11	bOR[r]_STORE_MASK_11	See above with i:3 and k:1 (PWM 1: single counter 3)	R/W
b10	bOR[r]_STORE_MASK_10	See above with i:2 and k:1 (PWM 1: single counter 2)	R/W
b9	bOR[r]_STORE_MASK_9	See above with i:1 and k:1 (PWM 1: single counter 1)	R/W
b8	bOR[r]_STORE_MASK_8	See above with i:0 and k:1 (PWM 1: single counter 0)	R/W
b7	bOR[r]_STORE_MASK_7	See above with i:7 and k:0 (PWM 0: single counter 7)	R/W
b6	bOR[r]_STORE_MASK_6	See above with i:6 and k:0 (PWM 0: single counter 6)	R/W
b5	bOR[r]_STORE_MASK_5	See above with i:5 and k:0 (PWM 0: single counter 5)	R/W
b4	bOR[r]_STORE_MASK_4	See above with i:4 and k:0 (PWM 0: single counter 4)	R/W
b3	bOR[r]_STORE_MASK_3	See above with i:3 and k:0 (PWM 0: single counter 3)	R/W
b2	bOR[r]_STORE_MASK_2	See above with i:2 and k:0 (PWM 0: single counter 2)	R/W
b1	bOR[r]_STORE_MASK_1	See above with i:1 and k:0 (PWM 0: single counter 1)	R/W
b0	bOR[r]_STORE_MASK_0	See above with i:0 and k:0 (PWM 0: single counter 0)	R/W

1.4.13 rPWMTimer_PWM_MODE_[k] − Management of the Timebase Mode (k = 0..1)

Address: 4006 9000h + 400h × k

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	bPWM_RANGEDMODE_7	bPWM_CASCADED_MODE_7	bPWM_MASTER_SINGLE_COUNTER_7		bPWM_RANGEDMODE_6	bPWM_CASCADED_MODE_6	bPWM_MASTER_SINGLE_COUNTER_6		bPWM_RANGEDMODE_5	bPWM_CASCADED_MODE_5	bPWM_MASTER_SINGLE_COUNTER_5		bPWM_RANGEDMODE_4	bPWM_CASCADED_MODE_4	bPWM_MASTER_SINGLE_COUNTER_4	
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	bPWM_RANGEDMODE_3	bPWM_CASCADED_MODE_3	bPWM_MASTER_SINGLE_COUNTER_3		bPWM_RANGEDMODE_2	bPWM_CASCADED_MODE_2	bPWM_MASTER_SINGLE_COUNTER_2		bPWM_RANGEDMODE_1	bPWM_CASCADED_MODE_1	—	bPWM_MASTER_SINGLE_COUNTER_1	bPWM_RANGEDMODE_0	—		
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.15 rPWMTimer_PWM_MODE_[k] Register Contents

Bit Position	Bit Name	Function	R/W
b31	bPWM_RANGEDMODE_7	Counting Mode of the Single Counter 7 of PWM [k]: 1'b0: Free running mode: Max value is 16'hFFFF. 1'b1: Ranged mode: Max value is determined by an option register 0.	R/W
b30	bPWM_CASCADED_MODE_7	Functional Mode of the Single Counter 7 of PWM [k]: 1'b0: Stand alone or first element of cascaded counters. 1'b1: Cascaded with previous counter, cascaded logic is enabled.	R/W
b29 to b28	bPWM_MASTER_SINGLE_COUNTER_7	Configuration of the Master Counter Feature of the Single Counter 7 of PWM [k]: 2'b00: Disabled 2'b01: Single counter 6 is the master counter. 2'b10: Single counter 5 is the master counter. 2'b11: Single counter 4 is the master counter.	R/W
b27	bPWM_RANGEDMODE_6	Counting Mode of the Single Counter 6 of PWM [k]: See above bPWM_RANGEDMODE_7	R/W
b26	bPWM_CASCADED_MODE_6	Functional Mode of the Single Counter 6 of PWM [k]: See above bPWM_CASCADED_MODE_7	R/W
b25 to b24	bPWM_MASTER_SINGLE_COUNTER_6	Configuration of the Master Counter Feature of the Single Counter 6 of PWM [k]: 2'b00: Disabled 2'b01: Single counter 5 is the master counter. 2'b10: Single counter 4 is the master counter. 2'b11: Single counter 3 is the master counter.	R/W
b23	bPWM_RANGEDMODE_5	Counting Mode of the Single Counter 5 of PWM [k]: See above bPWM_RANGEDMODE_7	R/W
b22	bPWM_CASCADED_MODE_5	Functional Mode of the Single Counter 5 of PWM [k]: See above bPWM_CASCADED_MODE_7	R/W
b21 to b20	bPWM_MASTER_SINGLE_COUNTER_5	Configuration of the Master Counter Feature of the Single Counter 5 of PWM [k]: 2'b00: Disabled 2'b01: Single counter 4 is the master counter. 2'b10: Single counter 3 is the master counter. 2'b11: Single counter 2 is the master counter.	R/W
b19	bPWM_RANGEDMODE_4	Counting Mode of the Single Counter 4 of PWM [k]: See above bPWM_RANGEDMODE_7	R/W

Bit Position	Bit Name	Function	R/W
b18	bPWM_CASCADED_MODE_4	Functional Mode of the Single Counter 4 of PWM [k]: See above bPWM_CASCADED_MODE_7	R/W
b17 to b16	bPWM_MASTER_SINGLE_COUNTER_4	Configuration of the Master Counter Feature of the Single Counter 4 of PWM [k]: 2'b00: Disabled 2'b01: Single counter 3 is the master counter. 2'b10: Single counter 2 is the master counter. 2'b11: Single counter 1 is the master counter.	R/W
b15	bPWM_RANGEDMODE_3	Counting Mode of the Single Counter 3 of PWM [k]: See above bPWM_RANGEDMODE_7	R/W
b14	bPWM_CASCADED_MODE_3	Functional Mode of the Single Counter 3 of PWM [k]: See above bPWM_CASCADED_MODE_7	R/W
b13 to b12	bPWM_MASTER_SINGLE_COUNTER_3	Configuration of the Master Counter Feature of the Single Counter 3 of PWM [k]: 2'b00: Disabled 2'b01: Single counter 2 is the master counter. 2'b10: Single counter 1 is the master counter. 2'b11: Single counter 0 is the master counter.	R/W
b11	bPWM_RANGEDMODE_2	Counting Mode of the Single Counter 2 of PWM [k]: See above bPWM_RANGEDMODE_7	R/W
b10	bPWM_CASCADED_MODE_2	Functional Mode of the Single Counter 2 of PWM [k]: See above bPWM_CASCADED_MODE_7	R/W
b9 to b8	bPWM_MASTER_SINGLE_COUNTER_2	Configuration of the Master Counter Feature of the Single Counter 2 of PWM [k]: 2'b00: Disabled 2'b01: Single counter 1 is the master counter. 2'b10: Single counter 0 is the master counter. 2'b11: Reserved	R/W
b7	bPWM_RANGEDMODE_1	Counting Mode of the Single Counter 1 of PWM [k]: See above bPWM_RANGEDMODE_7	R/W
b6	bPWM_CASCADED_MODE_1	Functional Mode of the Single Counter 1 of PWM [k]: See above bPWM_CASCADED_MODE_7	R/W
b5	Reserved	Always read as 0.	R
b4	bPWM_MASTER_SINGLE_COUNTER_1	Configuration of the Master Counter Feature of the Single Counter 1 of PWM [k]: 1'b0: Disabled 1'b1: Single counter 0 is the master counter.	R/W
b3	bPWM_RANGEDMODE_0	Counting Mode of the Single Counter 0 of PWM [k]: See above bPWM_RANGEDMODE_7	R/W
b2 to b0	Reserved	Keep initial value.	R/W

1.4.14 rPWMTimer_PWM_CLOCK_[q]_[k] − Configuration of the Clock Input in the PWM Modules (q = 0..1, k = 0..1)

Address: 4006 9030h + 400h × k + 4h × q

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—		bEDGE_CLOCK_[q*4+3]		—	bMUXEDCLOCK_[q*4+3]			—		bEDGE_CLOCK_[q*4+2]		—	bMUXEDCLOCK_[q*4+2]		
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—		bEDGE_CLOCK_[q*4+1]		_	bMUXEDCLOCK_[q*4+1]			—		bEDGE_CLOCK_[q*4]		—	bMUXEDCLOCK_[q*4]		
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.16 rPWMTimer_PWM_CLOCK_[q]_[k] Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b30	Reserved	Always read as 0.	R
b29 to b28	bEDGE_CLOCK_[q*4+3]	Clock Edge Detector Configuration of the Clock Input [q*4+e] in PWM [k]: 2'b00: Direct, output follows the input. 2'b01: Pulse on input rising edge. 2'b10: Pulse on input falling edge. 2'b11: Pulse on both input rising and falling edge. For these bits e:3 (single counter 3, 7)	R/W
b27	Reserved	Always read as 0.	R
b26 to b24	bMUXEDCLOCK_[q*4+3]	Clock Multiplexer of the Clock Input [q*4+e] in PWM [k]: 3'b000: Mux output = 1 (PWM_PCLK) 3'b001: Mux output = ClockIn.[k] 3'b110: Mux output = Block_Clock.0.[k] 3'b111: Mux output = Block_Clock.1.[k] Others: Reserved For these bits e:3 (single counter 3, 7)	R/W
b23 to b22	Reserved	Always read as 0.	R
b21 to b20	bEDGE_CLOCK_[q*4+2]	See above bEDGE_CLOCK_[q*4+3] with e:2 (single counter 2, 6)	R/W
b19	Reserved	Always read as 0.	R
b18 to b16	bMUXEDCLOCK_[q*4+2]	See above bMUXEDCLOCK_[q*4+3] with e:2 (single counter 2, 6)	R/W
b15 to b14	Reserved	Always read as 0.	R
b13 to b12	bEDGE_CLOCK_[q*4+1]	See above bEDGE_CLOCK_[q*4+3] with e:1 (single counter 1, 5)	R/W
b11	Reserved	Always read as 0.	R
b10 to b8	bMUXEDCLOCK_[q*4+1]	See above bMUXEDCLOCK_[q*4+3] with e:1 (single counter 1, 5)	R/W
b7 to b6	Reserved	Always read as 0.	R
b5 to b4	bEDGE_CLOCK_[q*4]	See above bEDGE_CLOCK_[q*4+3] with e:0 (single counter 0, 4)	R/W
b3	Reserved	Always read as 0.	R
b2 to b0	bMUXEDCLOCK_[q*4]	See above bMUXEDCLOCK_[q*4+3] with e:0 (single counter 0, 4)	R/W

1.4.15 rPWMTimer_PWM_UPDOWN_[d]_[k] − Configuration of the Up/Down Input in the PWM Modules (d = 0..3, k = 0..1)

Address: 4006 9040h + 400h × k + 4h × d

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	bUPDOWN_MODE_[d*2+1]		bOREDDOWN_[d*2+1]	—		—	—			bOREDUP_[d*2+1]	—		—	—		
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	bUPDOWN_MODE_[d*2]		bOREDDOWN_[d*2]	—		—	—			bOREDUP_[d*2]	—		—	—		
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.17 rPWMTimer_PWM_UPDOWN_[d]_[k] Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b30	bUPDOWN_MODE_[d*2+1]	Up/Down Mode of Up/Down Input [d*2+e] in PWM [k]: 2'b00: Set/Reset mode: Set by "Set signal", Reset by "Reset signal". 2'b01: Reserved 2'b10: Bypass mode: Up/Down = "Set signal" 2'b11: Bypass mode: Up/Down = Inverted "Reset signal" Refer to **Section 1.5.6.2(1)(b), Up/Down Input** for Set signal and Reset signal. For these bits e:1 (single counter 1, 3, 5, 7)	R/W
b29	bOREDDOWN_[d*2+1]	MAX Detection Input for "Reset signal" of Up/Down Input [d*2+e] in PWM [k]: 1'b0: Mux output = 0 1'b1: Mux output = MAX.[d*2+e].in For this bit e:1 (single counter 1, 3, 5, 7)	R/W
b28 to b27	Reserved	Keep initial value.	R/W
b26	Reserved	Always read as 0.	R
b25 to b23	Reserved	Keep initial value.	R/W
b22	bOREDUP_[d*2+1]	MIN Detection Input for "Set signal" of Up/Down Input [d*2+e] in PWM [k]: 1'b0: Mux output = 0 1'b1: Mux output = MIN.[d*2+e].in For this bit e:1 (single counter 1, 3, 5, 7)	R/W
b21 to b20	Reserved	Keep initial value.	R/W
b19	Reserved	Always read as 0.	R
b18 to b16	Reserved	Keep initial value.	R/W
b15 to b14	bUPDOWN_MODE_[d*2]	See above bUPDOWN_MODE_[d*2+1] with e:0 (single counter 0, 2, 4, 6)	R/W
b13	bOREDDOWN_[d*2]	See above bOREDDOWN_[d*2+1] with e:0 (single counter 0, 2, 4, 6).	R/W
b12 to b11	Reserved	Keep initial value.	R/W
b10	Reserved	Always read as 0.	R
b9 to b7	Reserved	Keep initial value.	R/W
b6	bOREDUP_[d*2]	See above bOREDUP_[d*2+1] with e:0 (single counter 0, 2, 4, 6).	R/W
b5 to b4	Reserved	Keep initial value.	R/W
b3	Reserved	Always read as 0.	R
b2 to b0	Reserved	Keep initial value.	R/W

1.4.16 rPWMTimer_PWM_TRIG0_[k] − Configuration of the Trig0 Input in the PWM Modules (k = 0..1)

Address: 4006 9070h + 400h × k

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	bTRIG0_7			—	bTRIG0_6			—	bTRIG0_5			—	bTRIG0_4		
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	bTRIG0_3			—	bTRIG0_2			—	bTRIG0_1			—	bTRIG0_0		
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.18 rPWMTimer_PWM_TRIG0_[k] Register Contents

Bit Position	Bit Name	Function	R/W
b31	Reserved	Always read as 0.	R
b30 to b28	bTRIG0_7	Trig0 Input of the Single Counter [i] in PWM [k]: 3'b000: Mux output = 0 3'b001: Mux output = Trig0.[i] Others: Reserved For these bits i:7	R/W
b27	Reserved	Always read as 0.	R
b26 to b24	bTRIG0_6	See above with i:6	R/W
b23	Reserved	Always read as 0.	R
b22 to b20	bTRIG0_5	See above with i:5	R/W
b19	Reserved	Always read as 0.	R
b18 to b16	bTRIG0_4	See above with i:4	R/W
b15	Reserved	Always read as 0.	R
b14 to b12	bTRIG0_3	See above with i:3	R/W
b11	Reserved	Always read as 0.	R
b10 to b8	bTRIG0_2	See above with i:2	R/W
b7	Reserved	Always read as 0.	R
b6 to b4	bTRIG0_1	See above with i:1	R/W
b3	Reserved	Always read as 0.	R
b2 to b0	bTRIG0_0	See above with i:0	R/W

1.4.17 rPWMTimer_PWM_TRIG1_[k] − Configuration of the Trig1 Input in the PWM Modules (k = 0..1)

Address: 4006 9080h + 400h × k

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	bTRIG1_7			—	bTRIG1_6			—	bTRIG1_5			—	bTRIG1_4		
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	bTRIG1_3			—	bTRIG1_2			—	bTRIG1_1			—	bTRIG1_0		
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.19 rPWMTimer_PWM_TRIG1_[k] Register Contents

Bit Position	Bit Name	Function	R/W
b31	Reserved	Always read as 0.	R
b30 to b28	bTRIG1_7	Trig1 Input of the Single Counter [i] in PWM [k]: 3'b000: Mux output = 0 3'b001: Mux output = Trig1.[i] Others: Reserved For these bits i:7	R/W
b27	Reserved	Always read as 0.	R
b26 to b24	bTRIG1_6	See above with i:6	R/W
b23	Reserved	Always read as 0.	R
b22 to b20	bTRIG1_5	See above with i:5	R/W
b19	Reserved	Always read as 0.	R
b18 to b16	bTRIG1_4	See above with i:4	R/W
b15	Reserved	Always read as 0.	R
b14 to b12	bTRIG1_3	See above with i:3	R/W
b11	Reserved	Always read as 0.	R
b10 to b8	bTRIG1_2	See above with i:2	R/W
b7	Reserved	Always read as 0.	R
b6 to b4	bTRIG1_1	See above with i:1	R/W
b3	Reserved	Always read as 0.	R
b2 to b0	bTRIG1_0	See above with i:0	R/W

1.4.18 rPWMTimer_PWM_OUTPUTGEN[d]_[k] − Configuration of the Outputs Generator in the PWM Modules (d = 0..3, k = 0..1)

Address: 4006 90C0h + 400h × k + 4h × d

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—			—			bCMP1_STOPPED_MODE_[d*2+1]		—			—				
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—			—			bCMP1_STOPPED_MODE_[d*2]		—			—				
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.20 rPWMTimer_PWM_OUTPUTGEN[d]_[k] Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b29	Reserved	Always read as 0.	R
b28 to b26	Reserved	Keep initial value.	R/W
b25 to b24	bCMP1_STOPPED_MODE_[d*2+1]	The Output CMP1 of the Single Counter [d*2+e] in PWM [k], When Count Enable Is Disable State 2'b00: Reset: 1'b0 2'b01: Set: 1'b1 Others: Reserved For these bits e:1 (single counter 1, 3, 5, 7)	R/W
b23 to b21	Reserved	Always read as 0.	R
b20 to b16	Reserved	Keep initial value.	R/W
b15 to b13	Reserved	Always read as 0.	R
b12 to b10	Reserved	Keep initial value.	R/W
b9 to b8	bCMP1_STOPPED_MODE_[d*2]	See above bCMP1_STOPPED_MODE_[d*2+1] with e:0 (single counter 0, 2, 4, 6)	R/W
b7 to b5	Reserved	Always read as 0.	R
b4 to b0	Reserved	Keep initial value.	R/W

1.4.19 rPWMTimer_PWM_BLOCK_CLOCK_[k] − Configuration of the Block_Clock in the PWM Module (k = 0..1)

Any write access to this register restart the prescaler system.

Address: 4006 90E0h + 400h × k

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—						bPWM_CLOCK_PRESCALER_1									
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—						bPWM_CLOCK_PRESCALER_0									
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.21 rPWMTimer_PWM_BLOCK_CLOCK_[k] Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b26	Reserved	Always read as 0.	R
b25 to b16	bPWM_CLOCK_PRESCALER_1	Clock Divider for the Block_Clock [e] Prescaler System in PWM [k]: 10'd0: PWM_PCLK/2 10'd1: PWM_PCLK/4 10'd2: PWM_PCLK/6 10'dX: PWM_PCLK/((X+1) × 2) 10'd1023: PWM_PCLK/2048 For these bits e:1	R/W
b15 to b10	Reserved	Always read as 0.	R
b9 to b0	bPWM_CLOCK_PRESCALER_0	See above with e:0	R/W

1.4.20 rPWMTimer_TIMEBASE_[i]_[k] − Current Counter Value of the 16bits Timebase (i = 0..7, k = 0..1)

Address: 4006 9100h + 400h × k + 4h × i

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	bTIMEBASE_COUNT_[i]_[k]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.22 rPWMTimer_TIMEBASE_[i]_[k] Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b16	Reserved	Always read as 0.	R
b15 to b0	bTIMEBASE_COUNT_[i]_[k]	Current Value of the Timebase Counter in the Single Counter [i] of PWM [k]	R/W

1.4.21 rPWMTimer_TIMEBASE_[n*2][n*2+1]_[k] − Current Counter Value of the 32bits Cascaded Timebase (n = 0..3, k = 0..1)

Address: 4006 9120h + 400h × k + 4h × n

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	bTIMEBASE_COUNT_[n*2+1]_[k]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	bTIMEBASE_COUNT_[n*2]_[k]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.23 rPWMTimer_TIMEBASE_[n*2][n*2+1]_[k] Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b16	bTIMEBASE_COUNT_[n*2+1]_[k]	Current Value of the Timebase Counter in the Single Counter [n*2+e] of PWM [k] For these bits e:1 (single counter 1, 3, 5, 7)	R/W
b15 to b0	bTIMEBASE_COUNT_[n*2]_[k]	See above with e:0 (single counter 0, 2, 4, 6)	R/W

1.4.22 rPWMTimer_TIMEBASE_[(n+1)*2-1][(n+1)*2]_[k] − Current Counter Value of the 32bits Cascaded Timebase (n = 0..2, k = 0..1)

Address: 4006 9130h + 400h × k + 4h × n

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	bTIMEBASE_COUNT_[(n+1)*2-0]_[k]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	bTIMEBASE_COUNT_[(n+1)*2-1]_[k]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.24 rPWMTimer_TIMEBASE_[(n+1)*2-1][(n+1)*2]_[k] Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b16	bTIMEBASE_COUNT_[(n+1)*2-0]_[k]	Current Value of the Timebase Counter in the Single Counter [(n+1)*2-e] of PWM [k] For these bits e:0 (single counter 2, 4, 6)	R/W
b15 to b0	bTIMEBASE_COUNT_[(n+1)*2-1]_[k]	See above with e:1 (single counter 1, 3, 5)	R/W

1.4.23 rPWMTimer_SCALEVALUE_[i]_[k] − Cascade Value Setting (i = 0..7, k = 0..1)

Address: 4006 9140h + 400h × k + 4h × i

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—								bSCALEVALUE_[i]_[k]							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Table 1.25 rPWMTimer_SCALEVALUE_[i]_[k] Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b8	Reserved	Always read as 0.	R
b7 to b0	bSCALEVALUE_[i]_[k]	Cascade Value of the Timebase Counter in the Single Counter [i] of PWM [k]. ***Caution*)** If the cascaded logic in the single counter [i] of PWM [k] is enable (rPWMTimer_PWM_MODE_[k].bPWM_CASCADED_MODE_[i] = 1), these bits should be set to 8'h00. In other cases, these bits should be set to 8'h01.	R/W

1.4.24 rPWMTimer_TIMEBASE_MUX_[q]_[k] − Configuration of the Compare/Capture System Input Mux Table (q = 0..1, k = 0..1)

Address: 4006 91A0h+ 400h × k + 4h × q

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—		—				bTIMEBASE_MUX_OR2_[q*4+3]	bTIMEBASE_MUX_OR0_[q*4+3]	—		—				bTIMEBASE_MUX_OR2_[q*4+2]	bTIMEBASE_MUX_OR0_[q*4+2]
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—		—				bTIMEBASE_MUX_OR2_[q*4+1]	bTIMEBASE_MUX_OR0_[q*4+1]	—		—				bTIMEBASE_MUX_OR2_[q*4]	bTIMEBASE_MUX_OR0_[q*4]
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.26 rPWMTimer_TIMEBASE_MUX_[q]_[k] Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b30	Reserved	Always read as 0.	R
b29 to b26	Reserved	Keep initial value.	R/W
b25	bTIMEBASE_MUX_OR2_[q*4+3]	Enable Buffer Transfer to OR2 in the Single Counter [q*4+e]: Should be set to 1. For this bit e:3 (single counter 3, 7)	R/W
b24	bTIMEBASE_MUX_OR0_[q*4+3]	Enable Buffer Transfer to OR0 in the Single Counter [q*4+e]: Should be set to 1. For this bit e:3 (single counter 3, 7)	R/W
b23 to b22	Reserved	Always read as 0.	R
b21 to b18	Reserved	Keep initial value.	R/W
b17	bTIMEBASE_MUX_OR2_[q*4+2]	See above bTIMEBASE_MUX_OR2_[q*4+3] with e:2 (single counter 2, 6)	R/W
b16	bTIMEBASE_MUX_OR0_[q*4+2]	See above bTIMEBASE_MUX_OR0_[q*4+3] with e:2 (single counter 2, 6)	R/W
b15 to b14	Reserved	Always read as 0.	R
b13 to b10	Reserved	Keep initial value.	R/W
b9	bTIMEBASE_MUX_OR2_[q*4+1]	See above bTIMEBASE_MUX_OR2_[q*4+3] with e:1 (single counter 1, 5)	R/W
b8	bTIMEBASE_MUX_OR0_[q*4+1]	See above bTIMEBASE_MUX_OR0_[q*4+3] with e:1 (single counter 1, 5)	R/W
b7 to b6	Reserved	Always read as 0.	R
b5 to b2	Reserved	Keep initial value.	R/W
b1	bTIMEBASE_MUX_OR2_[q*4]	See above bTIMEBASE_MUX_OR2_[q*4+3] with e:0 (single counter 0, 4)	R/W
b0	bTIMEBASE_MUX_OR0_[q*4]	See above bTIMEBASE_MUX_OR0_[q*4+3] with e:0 (single counter 0, 4)	R/W

1.4.25 rPWMTimer_HWSTORE_CONF_[i]_[k] − Configuration of the Hardware Store Trigger System in the PWM Modules (i = 0..7, k = 0..1)

Address: 4006 91B0h+ 400h × k + 4h × i

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—			—			—				bHWSTORE_SYNC_TRIG_2	—			
Value after reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—		—	—	—				—			bHWSTORE_SYNC_TRIG_0	—			
Value after reset	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0

Table 1.27 rPWMTimer_HWSTORE_CONF_[i]_[k] Register Contents

Bit Position	Bit Name	Function	R/W
b31	Reserved	Keep initial value.	R/W
b30 to b28	Reserved	Always read as 0.	R
b27 to b25	Reserved	Keep initial value.	R/W
b24 to b21	Reserved	Always read as 0.	R
b20	bHWSTORE_SYNC_TRIG_2	Enable or Disable the Store Trigger Resynchronization System for Option Register OR2 in the Single Counter [i] of PWM [k]: 1'b0: No resynchronization 1'b1: Synchronous with Timebase's clock Set to 0 when transferring the capture value, otherwise set to 1.	R/W
b19 to b16	Reserved	Keep initial value.	R/W
b15 to b14	Reserved	Always read as 0.	R
b13	Reserved	Keep initial value.	R/W
b12	Reserved	Always read as 0.	R
b11 to b8	Reserved	Keep initial value.	R/W
b7 to b5	Reserved	Always read as 0.	R
b4	bHWSTORE_SYNC_TRIG_0	Enable or Disable the Store Trigger Resynchronization System for Option Register OR0 in the Single Counter [i] of PWM [k]: 1'b0: No resynchronization 1'b1: Synchronous with Timebase's clock Set to 0 when transferring the capture value, otherwise set to 1.	R/W
b3 to b0	Reserved	Keep initial value.	R/W

1.4.26 rPWMTimer_HWSTORE_MUX_[i]_[k] − Multiplexers Configuration of the Hardware Store Trigger System in the PWM Modules (i = 0..7, k = 0..1)

Address: 4006 91D0h + 400h × k + 4h × i

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—				bHWSTORE_TRIG2_GENSYS				bHWSTORE_EDGE_OR3		bHWSTORE_EDGE_OR2		bHWSTORE_EDGE_OR1		bHWSTORE_EDGE_OR0	
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—		bHWSTORE_MUXED_TRIG_OR3		—		bHWSTORE_MUXED_TRIG_OR2		—		bHWSTORE_MUXED_TRIG_OR1		—		bHWSTORE_MUXED_TRIG_OR0	
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.28 rPWMTimer_HWSTORE_MUX_[i]_[k] Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b28	Reserved	Always read as 0.	R
b27 to b24	bHWSTORE_TRIG2_GENSYS	Trig2 Generation System Configuration in the Single Counter [i] of PWM [k]: 4'b0000: Trig2 = Reserved 4'b0001: Trig2 = MIN.i.in 4'b0010: Trig2 = MAX.i.in 4'b0011: Trig2 = MAX.i.in or MIN.i.in Others: Trig2 = Reserved	R/W
b23 to b22	bHWSTORE_EDGE_OR3	Input Trigger Multiplexer Edge Detector Configuration for Option Register OR[r] in the Single Counter [i] of PWM [k]: 2'b00: Direct, output follows the input 2'b01: Pulse on input rising edge 2'b10: Pulse on input falling edge 2'b11: Pulse on both input rising and falling edge For these bits r:3	R/W
b21 to b20	bHWSTORE_EDGE_OR2	See above bHWSTORE_EDGE_OR3 with r:2	R/W
b19 to b18	bHWSTORE_EDGE_OR1	See above bHWSTORE_EDGE_OR3 with r:1	R/W
b17 to b16	bHWSTORE_EDGE_OR0	See above bHWSTORE_EDGE_OR3 with r:0	R/W
b15 to b14	Reserved	Always read as 0.	R
b13 to b12	bHWSTORE_MUXED_TRIG_OR3	Input Trigger Multiplexer Configuration for Option Register OR[r] in the Single Counter [i] of the PWM [k]: 2'b00: Mux output = 0 2'b01: Mux output = Trig0 2'b10: Mux output = Trig1 2'b11: Mux output = Trig2 For these bits r:3	R/W
b11 to b10	Reserved	Always read as 0.	R
b9 to b8	bHWSTORE_MUXED_TRIG_OR2	See above bHWSTORE_MUXED_TRIG_OR3 with r:2	R/W
b7 to b6	Reserved	Always read as 0.	R
b5 to b4	bHWSTORE_MUXED_TRIG_OR1	See above bHWSTORE_MUXED_TRIG_OR3 with r:1	R/W
b3 to b2	Reserved	Always read as 0.	R
b1 to b0	bHWSTORE_MUXED_TRIG_OR0	See above bHWSTORE_MUXED_TRIG_OR3 with r:0	R/W

1.4.27 rPWMTimer_HWSTORE_LOCK_[k] − Lock or Read Lock Status of the Option Registers in the PWM Modules (k = 0..1)

Address: 4006 91F0h + 400h × k

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	bHWSTORE_OR3_LOCK_7	bHWSTORE_OR2_LOCK_7	bHWSTORE_OR1_LOCK_7	bHWSTORE_OR0_LOCK_7	bHWSTORE_OR3_LOCK_6	bHWSTORE_OR2_LOCK_6	bHWSTORE_OR1_LOCK_6	bHWSTORE_OR0_LOCK_6	bHWSTORE_OR3_LOCK_5	bHWSTORE_OR2_LOCK_5	bHWSTORE_OR1_LOCK_5	bHWSTORE_OR0_LOCK_5	bHWSTORE_OR3_LOCK_4	bHWSTORE_OR2_LOCK_4	bHWSTORE_OR1_LOCK_4	bHWSTORE_OR0_LOCK_4
Value after reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	bHWSTORE_OR3_LOCK_3	bHWSTORE_OR2_LOCK_3	bHWSTORE_OR1_LOCK_3	bHWSTORE_OR0_LOCK_3	bHWSTORE_OR3_LOCK_2	bHWSTORE_OR2_LOCK_2	bHWSTORE_OR1_LOCK_2	bHWSTORE_OR0_LOCK_2	bHWSTORE_OR3_LOCK_1	bHWSTORE_OR2_LOCK_1	bHWSTORE_OR1_LOCK_1	bHWSTORE_OR0_LOCK_1	bHWSTORE_OR3_LOCK_0	bHWSTORE_OR2_LOCK_0	bHWSTORE_OR1_LOCK_0	bHWSTORE_OR0_LOCK_0
Value after reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 1.29 rPWMTimer_HWSTORE_LOCK_[k] Register Contents

Bit Position	Bit Name	Function	R/W
b31	bHWSTORE_OR3_LOCK_7	Lock System Status of the Option Register OR[r] in the Single Counter [i]: Read status: 1'b0: Option register is not locked. 1'b1: Option register is locked. Write: Writing "1" will lock the option register. Writing "0" has no effect. For this bit i:7 and r:3 (single counter 7: option register OR3) Refer to **Section 1.4.28, rPWMTimer_HWSTORE_UNLOCK_[k] − Unlock the Option Registers in the PWM Modules (k = 0..1)** for registers details.	R/W
b30	bHWSTORE_OR2_LOCK_7	See above with i:7 and r:2 (single counter 7: option register OR2)	R/W
b29	bHWSTORE_OR1_LOCK_7	See above with i:7 and r:1 (single counter 7: option register OR1)	R/W
b28	bHWSTORE_OR0_LOCK_7	See above with i:7 and r:0 (single counter 7: option register OR0)	R/W
b27	bHWSTORE_OR3_LOCK_6	See above with i:6 and r:3 (single counter 6: option register OR3)	R/W
b26	bHWSTORE_OR2_LOCK_6	See above with i:6 and r:2 (single counter 6: option register OR2)	R/W
b25	bHWSTORE_OR1_LOCK_6	See above with i:6 and r:1 (single counter 6: option register OR1)	R/W
b24	bHWSTORE_OR0_LOCK_6	See above with i:6 and r:0 (single counter 6: option register OR0)	R/W
b23	bHWSTORE_OR3_LOCK_5	See above with i:5 and r:3 (single counter 5: option register OR3)	R/W
b22	bHWSTORE_OR2_LOCK_5	See above with i:5 and r:2 (single counter 5: option register OR2)	R/W
b21	bHWSTORE_OR1_LOCK_5	See above with i:5 and r:1 (single counter 5: option register OR1)	R/W
b20	bHWSTORE_OR0_LOCK_5	See above with i:5 and r:0 (single counter 5: option register OR0)	R/W
b19	bHWSTORE_OR3_LOCK_4	See above with i:4 and r:3 (single counter 4: option register OR3)	R/W
b18	bHWSTORE_OR2_LOCK_4	See above with i:4 and r:2 (single counter 4: option register OR2)	R/W

Bit Position	Bit Name	Function	R/W
b17	bHWSTORE_OR1_LOCK_4	See above with i:4 and r:1 (single counter 4: option register OR1)	R/W
b16	bHWSTORE_OR0_LOCK_4	See above with i:4 and r:0 (single counter 4: option register OR0)	R/W
b15	bHWSTORE_OR3_LOCK_3	See above with i:3 and r:3 (single counter 3: option register OR3)	R/W
b14	bHWSTORE_OR2_LOCK_3	See above with i:3 and r:2 (single counter 3: option register OR2)	R/W
b13	bHWSTORE_OR1_LOCK_3	See above with i:3 and r:1 (single counter 3: option register OR1)	R/W
b12	bHWSTORE_OR0_LOCK_3	See above with i:3 and r:0 (single counter 3: option register OR0)	R/W
b11	bHWSTORE_OR3_LOCK_2	See above with i:2 and r:3 (single counter 2: option register OR3)	R/W
b10	bHWSTORE_OR2_LOCK_2	See above with i:2 and r:2 (single counter 2: option register OR2)	R/W
b9	bHWSTORE_OR1_LOCK_2	See above with i:2 and r:1 (single counter 2: option register OR1)	R/W
b8	bHWSTORE_OR0_LOCK_2	See above with i:2 and r:0 (single counter 2: option register OR0)	R/W
b7	bHWSTORE_OR3_LOCK_1	See above with i:1 and r:3 (single counter 1: option register OR3)	R/W
b6	bHWSTORE_OR2_LOCK_1	See above with i:1 and r:2 (single counter 1: option register OR2)	R/W
b5	bHWSTORE_OR1_LOCK_1	See above with i:1 and r:1 (single counter 1: option register OR1)	R/W
b4	bHWSTORE_OR0_LOCK_1	See above with i:1 and r:0 (single counter 1: option register OR0)	R/W
b3	bHWSTORE_OR3_LOCK_0	See above with i:0 and r:3 (single counter 0: option register OR3)	R/W
b2	bHWSTORE_OR2_LOCK_0	See above with i:0 and r:2 (single counter 0: option register OR2)	R/W
b1	bHWSTORE_OR1_LOCK_0	See above with i:0 and r:1 (single counter 0: option register OR1)	R/W
b0	bHWSTORE_OR0_LOCK_0	See above with i:0 and r:0 (single counter 0: option register OR0)	R/W

1.4.28 rPWMTimer_HWSTORE_UNLOCK_[k] − Unlock the Option Registers in the PWM Modules (k = 0..1)

Address: 4006 91F4h+ 400h × k

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	bHWSTORE_OR3_UNLOCK_7	bHWSTORE_OR2_UNLOCK_7	bHWSTORE_OR1_UNLOCK_7	bHWSTORE_OR0_UNLOCK_7	bHWSTORE_OR3_UNLOCK_6	bHWSTORE_OR2_UNLOCK_6	bHWSTORE_OR1_UNLOCK_6	bHWSTORE_OR0_UNLOCK_6	bHWSTORE_OR3_UNLOCK_5	bHWSTORE_OR2_UNLOCK_5	bHWSTORE_OR1_UNLOCK_5	bHWSTORE_OR0_UNLOCK_5	bHWSTORE_OR3_UNLOCK_4	bHWSTORE_OR2_UNLOCK_4	bHWSTORE_OR1_UNLOCK_4	bHWSTORE_OR0_UNLOCK_4
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	bHWSTORE_OR3_UNLOCK_3	bHWSTORE_OR2_UNLOCK_3	bHWSTORE_OR1_UNLOCK_3	bHWSTORE_OR0_UNLOCK_3	bHWSTORE_OR3_UNLOCK_2	bHWSTORE_OR2_UNLOCK_2	bHWSTORE_OR1_UNLOCK_2	bHWSTORE_OR0_UNLOCK_2	bHWSTORE_OR3_UNLOCK_1	bHWSTORE_OR2_UNLOCK_1	bHWSTORE_OR1_UNLOCK_1	bHWSTORE_OR0_UNLOCK_1	bHWSTORE_OR3_UNLOCK_0	bHWSTORE_OR2_UNLOCK_0	bHWSTORE_OR1_UNLOCK_0	bHWSTORE_OR0_UNLOCK_0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.30 rPWMTimer_HWSTORE_UNLOCK_[k] Register Contents

Bit Position	Bit Name	Function	R/W
b31	bHWSTORE_OR3_UNLOCK_7	Unlock the Option Register OR[r] in the Single Counter [i]: Writing "1" will unlock the option register. Writing "0" has no effect. For this bit i:7 and r:3 (single counter 7: option register OR3)	W
b30	bHWSTORE_OR2_UNLOCK_7	See above with i:7 and r:2 (single counter 7: option register OR2)	W
b29	bHWSTORE_OR1_UNLOCK_7	See above with i:7 and r:1 (single counter 7: option register OR1)	W
b28	bHWSTORE_OR0_UNLOCK_7	See above with i:7 and r:0 (single counter 7: option register OR0)	W
b27	bHWSTORE_OR3_UNLOCK_6	See above with i:6 and r:3 (single counter 6: option register OR3)	W
b26	bHWSTORE_OR2_UNLOCK_6	See above with i:6 and r:2 (single counter 6: option register OR2)	W
b25	bHWSTORE_OR1_UNLOCK_6	See above with i:6 and r:1 (single counter 6: option register OR1)	W
b24	bHWSTORE_OR0_UNLOCK_6	See above with i:6 and r:0 (single counter 6: option register OR0)	W
b23	bHWSTORE_OR3_UNLOCK_5	See above with i:5 and r:3 (single counter 5: option register OR3)	W
b22	bHWSTORE_OR2_UNLOCK_5	See above with i:5 and r:2 (single counter 5: option register OR2)	W
b21	bHWSTORE_OR1_UNLOCK_5	See above with i:5 and r:1 (single counter 5: option register OR1)	W
b20	bHWSTORE_OR0_UNLOCK_5	See above with i:5 and r:0 (single counter 5: option register OR0)	W
b19	bHWSTORE_OR3_UNLOCK_4	See above with i:4 and r:3 (single counter 4: option register OR3)	W
b18	bHWSTORE_OR2_UNLOCK_4	See above with i:4 and r:2 (single counter 4: option register OR2)	W
b17	bHWSTORE_OR1_UNLOCK_4	See above with i:4 and r:1 (single counter 4: option register OR1)	W
b16	bHWSTORE_OR0_UNLOCK_4	See above with i:4 and r:0 (single counter 4: option register OR0)	W

Bit Position	Bit Name	Function	R/W
b15	bHWSTORE_OR3_UNLOCK_3	See above with i:3 and r:3 (single counter 3: option register OR3)	W
b14	bHWSTORE_OR2_UNLOCK_3	See above with i:3 and r:2 (single counter 3: option register OR2)	W
b13	bHWSTORE_OR1_UNLOCK_3	See above with i:3 and r:1 (single counter 3: option register OR1)	W
b12	bHWSTORE_OR0_UNLOCK_3	See above with i:3 and r:0 (single counter 3: option register OR0)	W
b11	bHWSTORE_OR3_UNLOCK_2	See above with i:2 and r:3 (single counter 2: option register OR3)	W
b10	bHWSTORE_OR2_UNLOCK_2	See above with i:2 and r:2 (single counter 2: option register OR2)	W
b9	bHWSTORE_OR1_UNLOCK_2	See above with i:2 and r:1 (single counter 2: option register OR1)	W
b8	bHWSTORE_OR0_UNLOCK_2	See above with i:2 and r:0 (single counter 2: option register OR0)	W
b7	bHWSTORE_OR3_UNLOCK_1	See above with i:1 and r:3 (single counter 1: option register OR3)	W
b6	bHWSTORE_OR2_UNLOCK_1	See above with i:1 and r:2 (single counter 1: option register OR2)	W
b5	bHWSTORE_OR1_UNLOCK_1	See above with i:1 and r:1 (single counter 1: option register OR1)	W
b4	bHWSTORE_OR0_UNLOCK_1	See above with i:1 and r:0 (single counter 1: option register OR0)	W
b3	bHWSTORE_OR3_UNLOCK_0	See above with i:0 and r:3 (single counter 0: option register OR3)	W
b2	bHWSTORE_OR2_UNLOCK_0	See above with i:0 and r:2 (single counter 0: option register OR2)	W
b1	bHWSTORE_OR1_UNLOCK_0	See above with i:0 and r:1 (single counter 0: option register OR1)	W
b0	bHWSTORE_OR0_UNLOCK_0	See above with i:0 and r:0 (single counter 0: option register OR0)	W

1.4.29 rPWMTimer_OPTIONREG[r]_[i]_[k] − Option Register [r] Value of the 16bits Timebase (i = 0..7, r = 0..3, k = 0..1)

Address: 4006 9200h + 400h × k + 40h × r + 4h × i

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	bTIMEBASE_OR[r]_[i]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.31 rPWMTimer_OPTIONREG[r]_[i]_[k] Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b16	Reserved	Always read as 0.	R
b15 to b0	bTIMEBASE_OR[r]_[i]	Value of the Option Register OR[r] in the Single Counter [i] of PWM [k]	R/W

1.4.30 rPWMTimer_OPTIONREG[r]_[n*2][n*2+1]_[k] − Option Register [r] Value of the 32bits Cascaded Timebase (n = 0..3, r = 0..3, k = 0..1)

Address: 4006 9220h + 400h × k + 40h × r + 4h × n

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	bTIMEBASE_OR[r]_[n*2+1]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	bTIMEBASE_OR[r]_[n*2+0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.32 rPWMTimer_OPTIONREG[r]_[n*2][n*2+1]_[k] Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b16	bTIMEBASE_OR[r]_[n*2+1]	Value of the Option Register OR[r] in the Single Counter [n*2+e] of PWM [k] For these bits e:1 (single counter 1, 3, 5, 7).	R/W
b15 to b0	bTIMEBASE_OR[r]_[n*2+0]	See above with e:0 (single counter 0, 2, 4, 6)	R/W

1.4.31 rPWMTimer_OPTIONREG[r]_[(n+1)*2-1][(n+1)*2]_[k] − Option Register [r] Value of the 32bits Cascaded Timebase (n = 0..2, r = 0..3, k = 0..1)

Address: 4006 9230h + 400h × k + 40h × r + 4h × n

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	bTIMEBASE_OR[r]_[(n+1)*2-0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	bTIMEBASE_OR[r]_[(n+1)*2-1]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.33 rPWMTimer_OPTIONREG[r]_[(n+1)*2-1][(n+1)*2]_[k] Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b16	bTIMEBASE_OR[r]_[(n+1)*2-0]	Value of the Option Register OR[r] in the Single Counter [(n+1)*2-e] of PWM [k] For these bits e:0 (single counter 2, 4, 6)	R/W
b15 to b0	bTIMEBASE_OR[r]_[(n+1)*2-1]	See above with e:1 (single counter 1, 3, 5)	R/W

1.4.32 rPWMTimer_PWM_SOFTSTART − Set the Count Enable Input of the PWM Modules in "Start" Mode

Address: 4006 A010h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	bSOFTSTART_7_1	bSOFTSTART_6_1	bSOFTSTART_5_1	bSOFTSTART_4_1	bSOFTSTART_3_1	bSOFTSTART_2_1	bSOFTSTART_1_1	bSOFTSTART_0_1	bSOFTSTART_7_0	bSOFTSTART_6_0	bSOFTSTART_5_0	bSOFTSTART_4_0	bSOFTSTART_3_0	bSOFTSTART_2_0	bSOFTSTART_1_0	bSOFTSTART_0_0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.34 rPWMTimer_PWM_SOFTSTART Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b16	Reserved	Write with 0.	W
b15	bSOFTSTART_7_1	Start Event for the Single Counter [i] of PWM [k]: Write "0" has no effect. Write "1" sets Count Enable to "Enable state". For this bit i:7 and k:1 (PWM 1: single counter 7)	W
b14	bSOFTSTART_6_1	See above with i:6 and k:1 (PWM 1: single counter 6)	W
b13	bSOFTSTART_5_1	See above with i:5 and k:1 (PWM 1: single counter 5)	W
b12	bSOFTSTART_4_1	See above with i:4 and k:1 (PWM 1: single counter 4)	W
b11	bSOFTSTART_3_1	See above with i:3 and k:1 (PWM 1: single counter 3)	W
b10	bSOFTSTART_2_1	See above with i:2 and k:1 (PWM 1: single counter 2)	W
b9	bSOFTSTART_1_1	See above with i:1 and k:1 (PWM 1: single counter 1)	W
b8	bSOFTSTART_0_1	See above with i:0 and k:1 (PWM 1: single counter 0)	W
b7	bSOFTSTART_7_0	See above with i:7 and k:0 (PWM 0: single counter 7)	W
b6	bSOFTSTART_6_0	See above with i:6 and k:0 (PWM 0: single counter 6)	W
b5	bSOFTSTART_5_0	See above with i:5 and k:0 (PWM 0: single counter 5)	W
b4	bSOFTSTART_4_0	See above with i:4 and k:0 (PWM 0: single counter 4)	W
b3	bSOFTSTART_3_0	See above with i:3 and k:0 (PWM 0: single counter 3)	W
b2	bSOFTSTART_2_0	See above with i:2 and k:0 (PWM 0: single counter 2)	W
b1	bSOFTSTART_1_0	See above with i:1 and k:0 (PWM 0: single counter 1)	W
b0	bSOFTSTART_0_0	See above with i:0 and k:0 (PWM 0: single counter 0)	W

1.4.33 rPWMTimer_PWM_SOFTSTOP − Set the Count Enable Input of the PWM Modules in "Stop" Mode

Address: 4006 A018h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	bSOFTSTOP_7_1	bSOFTSTOP_6_1	bSOFTSTOP_5_1	bSOFTSTOP_4_1	bSOFTSTOP_3_1	bSOFTSTOP_2_1	bSOFTSTOP_1_1	bSOFTSTOP_0_1	bSOFTSTOP_7_0	bSOFTSTOP_6_0	bSOFTSTOP_5_0	bSOFTSTOP_4_0	bSOFTSTOP_3_0	bSOFTSTOP_2_0	bSOFTSTOP_1_0	bSOFTSTOP_0_0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.35 rPWMTimer_PWM_SOFTSTOP Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b16	Reserved	Write with 0.	W
b15	bSOFTSTOP_7_1	Stop Event for the Single Counter [i] of PWM [k]: Write "0" has no effect. Write "1" sets Count Enable to "Disable state". For this bit i:7 and k:1 (PWM 1: single counter 7)	W
b14	bSOFTSTOP_6_1	See above with i:6 and k:1 (PWM 1: single counter 6)	W
b13	bSOFTSTOP_5_1	See above with i:5 and k:1 (PWM 1: single counter 5)	W
b12	bSOFTSTOP_4_1	See above with i:4 and k:1 (PWM 1: single counter 4)	W
b11	bSOFTSTOP_3_1	See above with i:3 and k:1 (PWM 1: single counter 3)	W
b10	bSOFTSTOP_2_1	See above with i:2 and k:1 (PWM 1: single counter 2)	W
b9	bSOFTSTOP_1_1	See above with i:1 and k:1 (PWM 1: single counter 1)	W
b8	bSOFTSTOP_0_1	See above with i:0 and k:1 (PWM 1: single counter 0)	W
b7	bSOFTSTOP_7_0	See above with i:7 and k:0 (PWM 0: single counter 7)	W
b6	bSOFTSTOP_6_0	See above with i:6 and k:0 (PWM 0: single counter 6)	W
b5	bSOFTSTOP_5_0	See above with i:5 and k:0 (PWM 0: single counter 5)	W
b4	bSOFTSTOP_4_0	See above with i:4 and k:0 (PWM 0: single counter 4)	W
b3	bSOFTSTOP_3_0	See above with i:3 and k:0 (PWM 0: single counter 3)	W
b2	bSOFTSTOP_2_0	See above with i:2 and k:0 (PWM 0: single counter 2)	W
b1	bSOFTSTOP_1_0	See above with i:1 and k:0 (PWM 0: single counter 1)	W
b0	bSOFTSTOP_0_0	See above with i:0 and k:0 (PWM 0: single counter 0)	W

1.4.34 rPWMTimer_PWM_SOFTUPDOWN_0 − Set the Up/Down Outputs of the PWM Modules

This register uses a specific mask system. The 16 most significant bits are used as mask for the 16 least significant bits representing the data to be written.

Address: 4006 A040h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	bSOFTUPDOWN_MASK															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	bSOFTUPDOWN_7_1	bSOFTUPDOWN_6_1	bSOFTUPDOWN_5_1	bSOFTUPDOWN_4_1	bSOFTUPDOWN_3_1	bSOFTUPDOWN_2_1	bSOFTUPDOWN_1_1	bSOFTUPDOWN_0_1	bSOFTUPDOWN_7_0	bSOFTUPDOWN_6_0	bSOFTUPDOWN_5_0	bSOFTUPDOWN_4_0	bSOFTUPDOWN_3_0	bSOFTUPDOWN_2_0	bSOFTUPDOWN_1_0	bSOFTUPDOWN_0_0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.36 rPWMTimer_PWM_SOFTUPDOWN_0 Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b16	bSOFTUPDOWN_MASK	Always read as 0. Writing '1' in a bit of this register activates the write enable of the corresponding bit for the current access.	W
b15	bSOFTUPDOWN_7_1	Set the Up/Down Output of the Single Counter [i] of PWM [k]: This bit is W with mask. 1'b0: To "0": Count-down 1'b1: To "1": Count-up For this bit i:7 and k:1 (PWM 1: single counter 7) ***Note*)** If software controls counter directions, use Set/Reset mode and fix Set/Reset input to 0. Refer to **Section 1.5.6.2(1)(b), Up/Down Input**.	W
b14	bSOFTUPDOWN_6_1	See above with i:6 and k:1 (PWM 1: single counter 6)	W
b13	bSOFTUPDOWN_5_1	See above with i:5 and k:1 (PWM 1: single counter 5)	W
b12	bSOFTUPDOWN_4_1	See above with i:4 and k:1 (PWM 1: single counter 4)	W
b11	bSOFTUPDOWN_3_1	See above with i:3 and k:1 (PWM 1: single counter 3)	W
b10	bSOFTUPDOWN_2_1	See above with i:2 and k:1 (PWM 1: single counter 2)	W
b9	bSOFTUPDOWN_1_1	See above with i:1 and k:1 (PWM 1: single counter 1)	W
b8	bSOFTUPDOWN_0_1	See above with i:0 and k:1 (PWM 1: single counter 0)	W
b7	bSOFTUPDOWN_7_0	See above with i:7 and k:0 (PWM 0: single counter 7)	W
b6	bSOFTUPDOWN_6_0	See above with i:6 and k:0 (PWM 0: single counter 6)	W
b5	bSOFTUPDOWN_5_0	See above with i:5 and k:0 (PWM 0: single counter 5)	W
b4	bSOFTUPDOWN_4_0	See above with i:4 and k:0 (PWM 0: single counter 4)	W
b3	bSOFTUPDOWN_3_0	See above with i:3 and k:0 (PWM 0: single counter 3)	W

Bit Position	Bit Name	Function	R/W
b2	bSOFTUPDOWN_2_0	See above with i:2 and k:0 (PWM 0: single counter 2)	W
b1	bSOFTUPDOWN_1_0	See above with i:1 and k:0 (PWM 0: single counter 1)	W
b0	bSOFTUPDOWN_0_0	See above with i:0 and k:0 (PWM 0: single counter 0)	W

1.4.35 rPWMTimer_PWM_SOFTRESET − Set the Reset Trigger of the Timebases

Address: 4006 A050h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	bSOFTRESET_7_1	bSOFTRESET_6_1	bSOFTRESET_5_1	bSOFTRESET_4_1	bSOFTRESET_3_1	bSOFTRESET_2_1	bSOFTRESET_1_1	bSOFTRESET_0_1	bSOFTRESET_7_0	bSOFTRESET_6_0	bSOFTRESET_5_0	bSOFTRESET_4_0	bSOFTRESET_3_0	bSOFTRESET_2_0	bSOFTRESET_1_0	bSOFTRESET_0_0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.37 rPWMTimer_PWM_SOFTRESET Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b16	Reserved	Write with 0.	W
b15	bSOFTRESET_7_1	Reset Event for the Single Counter [i] of PWM [k]: Write "0" has no effect. Write "1" sets to reset. For this bit i:7 and k:1. (PWM 1: single counter 7)	W
b14	bSOFTRESET_6_1	See above with i:6 and k:1 (PWM 1: single counter 6)	W
b13	bSOFTRESET_5_1	See above with i:5 and k:1 (PWM 1: single counter 5)	W
b12	bSOFTRESET_4_1	See above with i:4 and k:1 (PWM 1: single counter 4)	W
b11	bSOFTRESET_3_1	See above with i:3 and k:1 (PWM 1: single counter 3)	W
b10	bSOFTRESET_2_1	See above with i:2 and k:1 (PWM 1: single counter 2)	W
b9	bSOFTRESET_1_1	See above with i:1 and k:1 (PWM 1: single counter 1)	W
b8	bSOFTRESET_0_1	See above with i:0 and k:1 (PWM 1: single counter 0)	W
b7	bSOFTRESET_7_0	See above with i:7 and k:0 (PWM 0: single counter 7)	W
b6	bSOFTRESET_6_0	See above with i:6 and k:0 (PWM 0: single counter 6)	W
b5	bSOFTRESET_5_0	See above with i:5 and k:0 (PWM 0: single counter 5)	W
b4	bSOFTRESET_4_0	See above with i:4 and k:0 (PWM 0: single counter 4)	W
b3	bSOFTRESET_3_0	See above with i:3 and k:0 (PWM 0: single counter 3)	W
b2	bSOFTRESET_2_0	See above with i:2 and k:0 (PWM 0: single counter 2)	W
b1	bSOFTRESET_1_0	See above with i:1 and k:0 (PWM 0: single counter 1)	W
b0	bSOFTRESET_0_0	See above with i:0 and k:0 (PWM 0: single counter 0)	W

1.4.36 rPWMTimer_PWM_CMP1_FLAG_POLARITY − PWM CMP1 Flags Configuration

Address: 4006 A0D4h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—															
Value after reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	bCMP1_FLAG_EDGE_15	bCMP1_FLAG_EDGE_14	bCMP1_FLAG_EDGE_13	bCMP1_FLAG_EDGE_12	bCMP1_FLAG_EDGE_11	bCMP1_FLAG_EDGE_10	bCMP1_FLAG_EDGE_9	bCMP1_FLAG_EDGE_8	bCMP1_FLAG_EDGE_7	bCMP1_FLAG_EDGE_6	bCMP1_FLAG_EDGE_5	bCMP1_FLAG_EDGE_4	bCMP1_FLAG_EDGE_3	bCMP1_FLAG_EDGE_2	bCMP1_FLAG_EDGE_1	bCMP1_FLAG_EDGE_0
Value after reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 1.38 rPWMTimer_PWM_CMP1_FLAG_POLARITY Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b16	Reserved	Keep initial value.	R/W
b15	bCMP1_FLAG_EDGE_15	Select the Edge Event That Sets the CMP1 Flag of Single Counter [i] from PWM [k]: 1'b1: Flag is set on CMP1 rising edge. 1'b0: Flag is set on CMP1 falling edge. For this bit i:7 and k:1. (PWM 1: single counter 7)	R/W
b14	bCMP1_FLAG_EDGE_14	See above with i:6 and k:1 (PWM 1: single counter 6)	R/W
b13	bCMP1_FLAG_EDGE_13	See above with i:5 and k:1 (PWM 1: single counter 5)	R/W
b12	bCMP1_FLAG_EDGE_12	See above with i:4 and k:1 (PWM 1: single counter 4)	R/W
b11	bCMP1_FLAG_EDGE_11	See above with i:3 and k:1 (PWM 1: single counter 3)	R/W
b10	bCMP1_FLAG_EDGE_10	See above with i:2 and k:1 (PWM 1: single counter 2)	R/W
b9	bCMP1_FLAG_EDGE_9	See above with i:1 and k:1 (PWM 1: single counter 1)	R/W
b8	bCMP1_FLAG_EDGE_8	See above with i:0 and k:1 (PWM 1: single counter 0)	R/W
b7	bCMP1_FLAG_EDGE_7	See above with i:7 and k:0 (PWM 0: single counter 7)	R/W
b6	bCMP1_FLAG_EDGE_6	See above with i:6 and k:0 (PWM 0: single counter 6)	R/W
b5	bCMP1_FLAG_EDGE_5	See above with i:5 and k:0 (PWM 0: single counter 5)	R/W
b4	bCMP1_FLAG_EDGE_4	See above with i:4 and k:0 (PWM 0: single counter 4)	R/W
b3	bCMP1_FLAG_EDGE_3	See above with i:3 and k:0 (PWM 0: single counter 3)	R/W
b2	bCMP1_FLAG_EDGE_2	See above with i:2 and k:0 (PWM 0: single counter 2)	R/W
b1	bCMP1_FLAG_EDGE_1	See above with i:1 and k:0 (PWM 0: single counter 1)	R/W
b0	bCMP1_FLAG_EDGE_0	See above with i:0 and k:0 (PWM 0: single counter 0)	R/W

1.4.37 rPWMTimer_PWM_CMP1_FLAG − PWM CMP1 Flags

The content of this register is used by the event manager to generate the PWMTimer interruption. Refer to **Section 1.5.7, Event Manager Module** for details.

Address: 4006 A0DCh

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	bPWM_CMP1_FLAG_15	bPWM_CMP1_FLAG_14	bPWM_CMP1_FLAG_13	bPWM_CMP1_FLAG_12	bPWM_CMP1_FLAG_11	bPWM_CMP1_FLAG_10	bPWM_CMP1_FLAG_9	bPWM_CMP1_FLAG_8	bPWM_CMP1_FLAG_7	bPWM_CMP1_FLAG_6	bPWM_CMP1_FLAG_5	bPWM_CMP1_FLAG_4	bPWM_CMP1_FLAG_3	bPWM_CMP1_FLAG_2	bPWM_CMP1_FLAG_1	bPWM_CMP1_FLAG_0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.39 rPWMTimer_PWM_CMP1_FLAG Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b16	Reserved	Keep initial value.	R/W
b15	bPWM_CMP1_FLAG_15	CMP1 Status Flag of the Single Counter [i] from PWM [k]: This bit is set to "1" by hardware when the selected edge is detected on CMP1. Write "1" will clean the flag. Write "0" has no effect. For this bit i:7 and k:1. (PWM 1: single counter 7)	R/W
b14	bPWM_CMP1_FLAG_14	See above with i:6 and k:1 (PWM 1: single counter 6)	R/W
b13	bPWM_CMP1_FLAG_13	See above with i:5 and k:1 (PWM 1: single counter 5)	R/W
b12	bPWM_CMP1_FLAG_12	See above with i:4 and k:1 (PWM 1: single counter 4)	R/W
b11	bPWM_CMP1_FLAG_11	See above with i:3 and k:1 (PWM 1: single counter 3)	R/W
b10	bPWM_CMP1_FLAG_10	See above with i:2 and k:1 (PWM 1: single counter 2)	R/W
b9	bPWM_CMP1_FLAG_9	See above with i:1 and k:1 (PWM 1: single counter 1)	R/W
b8	bPWM_CMP1_FLAG_8	See above with i:0 and k:1 (PWM 1: single counter 0)	R/W
b7	bPWM_CMP1_FLAG_7	See above with i:7 and k:0 (PWM 0: single counter 7)	R/W
b6	bPWM_CMP1_FLAG_6	See above with i:6 and k:0 (PWM 0: single counter 6)	R/W
b5	bPWM_CMP1_FLAG_5	See above with i:5 and k:0 (PWM 0: single counter 5)	R/W
b4	bPWM_CMP1_FLAG_4	See above with i:4 and k:0 (PWM 0: single counter 4)	R/W
b3	bPWM_CMP1_FLAG_3	See above with i:3 and k:0 (PWM 0: single counter 3)	R/W
b2	bPWM_CMP1_FLAG_2	See above with i:2 and k:0 (PWM 0: single counter 2)	R/W
b1	bPWM_CMP1_FLAG_1	See above with i:1 and k:0 (PWM 0: single counter 1)	R/W
b0	bPWM_CMP1_FLAG_0	See above with i:0 and k:0 (PWM 0: single counter 0)	R/W

1.4.38 rPWMTimer_PWM_MAX_OVERFLOW − PWM Overflow Detection Flags

The content of this register is used by the event manager to generate the PWMTimer interruption. Refer to **Section 1.5.7, Event Manager Module** for details.

Address: 4006 A108h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	bPWM_OVERFLOW_FLAG_7_1	bPWM_OVERFLOW_FLAG_6_1	bPWM_OVERFLOW_FLAG_5_1	bPWM_OVERFLOW_FLAG_4_1	bPWM_OVERFLOW_FLAG_3_1	bPWM_OVERFLOW_FLAG_2_1	bPWM_OVERFLOW_FLAG_1_1	bPWM_OVERFLOW_FLAG_0_1	bPWM_OVERFLOW_FLAG_7_0	bPWM_OVERFLOW_FLAG_6_0	bPWM_OVERFLOW_FLAG_5_0	bPWM_OVERFLOW_FLAG_4_0	bPWM_OVERFLOW_FLAG_3_0	bPWM_OVERFLOW_FLAG_2_0	bPWM_OVERFLOW_FLAG_1_0	bPWM_OVERFLOW_FLAG_0_0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.40 rPWMTimer_PWM_MAX_OVERFLOW Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b16	Reserved	Keep initial value.	R/W
b15	bPWM_OVERFLOW_FLAG_7_1	Overflow Flag from the Single Counter [i] of PWM [k]: This bit is set by hardware. Write "1" will clean the overflow flag. Write "0" has no effect. For this bit i:7 and k:1. (PWM 1: single counter 7)	R/W
b14	bPWM_OVERFLOW_FLAG_6_1	See above with i:6 and k:1 (PWM 1: single counter 6)	R/W
b13	bPWM_OVERFLOW_FLAG_5_1	See above with i:5 and k:1 (PWM 1: single counter 5)	R/W
b12	bPWM_OVERFLOW_FLAG_4_1	See above with i:4 and k:1 (PWM 1: single counter 4)	R/W
b11	bPWM_OVERFLOW_FLAG_3_1	See above with i:3 and k:1 (PWM 1: single counter 3)	R/W
b10	bPWM_OVERFLOW_FLAG_2_1	See above with i:2 and k:1 (PWM 1: single counter 2)	R/W
b9	bPWM_OVERFLOW_FLAG_1_1	See above with i:1 and k:1 (PWM 1: single counter 1)	R/W
b8	bPWM_OVERFLOW_FLAG_0_1	See above with i:0 and k:1 (PWM 1: single counter 0)	R/W
b7	bPWM_OVERFLOW_FLAG_7_0	See above with i:7 and k:0 (PWM 0: single counter 7)	R/W
b6	bPWM_OVERFLOW_FLAG_6_0	See above with i:6 and k:0 (PWM 0: single counter 6)	R/W
b5	bPWM_OVERFLOW_FLAG_5_0	See above with i:5 and k:0 (PWM 0: single counter 5)	R/W
b4	bPWM_OVERFLOW_FLAG_4_0	See above with i:4 and k:0 (PWM 0: single counter 4)	R/W
b3	bPWM_OVERFLOW_FLAG_3_0	See above with i:3 and k:0 (PWM 0: single counter 3)	R/W
b2	bPWM_OVERFLOW_FLAG_2_0	See above with i:2 and k:0 (PWM 0: single counter 2)	R/W
b1	bPWM_OVERFLOW_FLAG_1_0	See above with i:1 and k:0 (PWM 0: single counter 1)	R/W
b0	bPWM_OVERFLOW_FLAG_0_0	See above with i:0 and k:0 (PWM 0: single counter 0)	R/W

1.4.39 rPWMTimer_PWM_MIN_UNDERFLOW − PWM Underflow Detection Flags

The content of this register is used by the event manager to generate the PWMTimer interruption. Refer to **Section 1.5.7, Event Manager Module** for details.

Address: 4006 A10Ch

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	bPWM_UNDERFLOW_FLAG_7_1	bPWM_UNDERFLOW_FLAG_6_1	bPWM_UNDERFLOW_FLAG_5_1	bPWM_UNDERFLOW_FLAG_4_1	bPWM_UNDERFLOW_FLAG_3_1	bPWM_UNDERFLOW_FLAG_2_1	bPWM_UNDERFLOW_FLAG_1_1	bPWM_UNDERFLOW_FLAG_0_1	bPWM_UNDERFLOW_FLAG_7_0	bPWM_UNDERFLOW_FLAG_6_0	bPWM_UNDERFLOW_FLAG_5_0	bPWM_UNDERFLOW_FLAG_4_0	bPWM_UNDERFLOW_FLAG_3_0	bPWM_UNDERFLOW_FLAG_2_0	bPWM_UNDERFLOW_FLAG_1_0	bPWM_UNDERFLOW_FLAG_0_0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.41 rPWMTimer_PWM_MIN_UNDERFLOW Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b16	Reserved	Keep initial value.	R/W
b15	bPWM_UNDERFLOW_FLAG_7_1	Underflow Flag from the Single Counter [i] of PWM [k]: This bit is set by hardware. Write "1" will clean the underflow flag. Write "0" has no effect. For this bit i:7 and k:1. (PWM 1: single counter 7)	R/W
b14	bPWM_UNDERFLOW_FLAG_6_1	See above with i:6 and k:1 (PWM 1: single counter 6)	R/W
b13	bPWM_UNDERFLOW_FLAG_5_1	See above with i:5 and k:1 (PWM 1: single counter 5)	R/W
b12	bPWM_UNDERFLOW_FLAG_4_1	See above with i:4 and k:1 (PWM 1: single counter 4)	R/W
b11	bPWM_UNDERFLOW_FLAG_3_1	See above with i:3 and k:1 (PWM 1: single counter 3)	R/W
b10	bPWM_UNDERFLOW_FLAG_2_1	See above with i:2 and k:1 (PWM 1: single counter 2)	R/W
b9	bPWM_UNDERFLOW_FLAG_1_1	See above with i:1 and k:1 (PWM 1: single counter 1)	R/W
b8	bPWM_UNDERFLOW_FLAG_0_1	See above with i:0 and k:1 (PWM 1: single counter 0)	R/W
b7	bPWM_UNDERFLOW_FLAG_7_0	See above with i:7 and k:0 (PWM 0: single counter 7)	R/W
b6	bPWM_UNDERFLOW_FLAG_6_0	See above with i:6 and k:0 (PWM 0: single counter 6)	R/W
b5	bPWM_UNDERFLOW_FLAG_5_0	See above with i:5 and k:0 (PWM 0: single counter 5)	R/W
b4	bPWM_UNDERFLOW_FLAG_4_0	See above with i:4 and k:0 (PWM 0: single counter 4)	R/W
b3	bPWM_UNDERFLOW_FLAG_3_0	See above with i:3 and k:0 (PWM 0: single counter 3)	R/W
b2	bPWM_UNDERFLOW_FLAG_2_0	See above with i:2 and k:0 (PWM 0: single counter 2)	R/W
b1	bPWM_UNDERFLOW_FLAG_1_0	See above with i:1 and k:0 (PWM 0: single counter 1)	R/W
b0	bPWM_UNDERFLOW_FLAG_0_0	See above with i:0 and k:0 (PWM 0: single counter 0)	R/W

1.4.40 rPWMTimer_HWSTORE_OR[r]_STORE_FLAG − PWM OR[r] Store Trigger Flags (r = 1, 3)

The content of this register is used by the event manager to generate the PWMTimer interruption. Refer to **Section 1.5.7, Event Manager Module** for details.

Address: 4006 A1D0h + 4h × r

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	bOR[r]_STORE_FLAG_15	bOR[r]_STORE_FLAG_14	bOR[r]_STORE_FLAG_13	bOR[r]_STORE_FLAG_12	bOR[r]_STORE_FLAG_11	bOR[r]_STORE_FLAG_10	bOR[r]_STORE_FLAG_9	bOR[r]_STORE_FLAG_8	bOR[r]_STORE_FLAG_7	bOR[r]_STORE_FLAG_6	bOR[r]_STORE_FLAG_5	bOR[r]_STORE_FLAG_4	bOR[r]_STORE_FLAG_3	bOR[r]_STORE_FLAG_2	bOR[r]_STORE_FLAG_1	bOR[r]_STORE_FLAG_0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.42 rPWMTimer_HWSTORE_OR[r]_STORE_FLAG Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b16	Reserved	Keep initial value.	R/W
b15	bOR[r]_STORE_FLAG_15	OR[r] Store Trigger Flag of the Single Counter [i] from PWM [k]: This bit is set to "1" by hardware when a positive edge is detected on OR[r]_TRIG.[i] output signal. Write "1" will clean the flag. Write "0" has no effect. For this bit i:7 and k:1. (PWM 1: single counter 7)	R/W
b14	bOR[r]_STORE_FLAG_14	See above with i:6 and k:1 (PWM 1: single counter 6)	R/W
b13	bOR[r]_STORE_FLAG_13	See above with i:5 and k:1 (PWM 1: single counter 5)	R/W
b12	bOR[r]_STORE_FLAG_12	See above with i:4 and k:1 (PWM 1: single counter 4)	R/W
b11	bOR[r]_STORE_FLAG_11	See above with i:3 and k:1 (PWM 1: single counter 3)	R/W
b10	bOR[r]_STORE_FLAG_10	See above with i:2 and k:1 (PWM 1: single counter 2)	R/W
b9	bOR[r]_STORE_FLAG_9	See above with i:1 and k:1 (PWM 1: single counter 1)	R/W
b8	bOR[r]_STORE_FLAG_8	See above with i:0 and k:1 (PWM 1: single counter 0)	R/W
b7	bOR[r]_STORE_FLAG_7	See above with i:7 and k:0 (PWM 0: single counter 7)	R/W
b6	bOR[r]_STORE_FLAG_6	See above with i:6 and k:0 (PWM 0: single counter 6)	R/W
b5	bOR[r]_STORE_FLAG_5	See above with i:5 and k:0 (PWM 0: single counter 5)	R/W
b4	bOR[r]_STORE_FLAG_4	See above with i:4 and k:0 (PWM 0: single counter 4)	R/W
b3	bOR[r]_STORE_FLAG_3	See above with i:3 and k:0 (PWM 0: single counter 3)	R/W
b2	bOR[r]_STORE_FLAG_2	See above with i:2 and k:0 (PWM 0: single counter 2)	R/W
b1	bOR[r]_STORE_FLAG_1	See above with i:1 and k:0 (PWM 0: single counter 1)	R/W

Bit Position	Bit Name	Function	R/W
b0	bOR[r]_STORE_FLAG_0	See above with i:0 and k:0 (PWM 0: single counter 0)	R/W

1.4.41 rPWMTimer_ROUTING_IN_[s] − Configuration of the PWMTimer's Multiplexed Inputs "IN" (s = 0, 2)

Configuration of the PWMTimer input (IN 0..2, 10..12)

Address: 4006 B100h + 4h × s

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—		—												bROUTING_INPUT_IN_[2+s*5]	
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	bROUTING_INPUT_IN_[2+s*5]				bROUTING_INPUT_IN_[1+s*5]						bROUTING_INPUT_IN_[0+s*5]					
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 1.43 rPWMTimer_ROUTING_IN_[s] Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b30	Reserved	Always read as 0.	R
b29 to b18	Reserved	Keep initial value.	R/W
b17 to b12	bROUTING_INPUT_IN_[2+s*5]	Clock Input (ClockIn) Selection for PWM [s/2]: Configuration of PWMTimer Core input IN[e+s*5] 6'd0: PWMTimer Core IN = PWM_IN[0] 6'd1: PWMTimer Core IN = PWM_IN[1] 6'dX: PWMTimer Core IN = PWM_IN[X] (X = 0..39) 6'd39: PWMTimer Core IN = PWM_IN[39] 6'dY: Reserved (Y = 40..63) For these bits e:2 (PWMTimer Core input IN 2, 12). ***Note*)** The value after reset is based on suffix number [e+s*5].	R/W
b11 to b6	bROUTING_INPUT_IN_[1+s*5]	Capture Trigger 0 Input (Trig0) Selection for PWM [s/2] See above with e:1 (PWMTimer Core input IN 1, 11).	R/W
b5 to b0	bROUTING_INPUT_IN_[0+s*5]	Capture Trigger 1 Input (Trig1) Selection for PWM [s/2] See above with e:0 (PWMTimer Core input IN 0, 10).	R/W

1.4.42 rPWMTimer_ROUTING_OUT_[n] − Configuration of the PWMTimer's Multiplexed Outputs "OUT" (n = 0..3)

Configuration of the PWMTimer output (PWM_OUT 0..19)

Address: 4006 B200h + 4h × n

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—			bROUTING_OUTPUT_OUT_[4+n*5]					—	bROUTING_OUTPUT_OUT_[3+n*5]					—	bROUTING_OUTPUT_OUT_[2+n*5]
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	bROUTING_OUTPUT_OUT_[2+n*5]				—	bROUTING_OUTPUT_OUT_[1+n*5]					—	bROUTING_OUTPUT_OUT_[0+n*5]				
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 1.44 rPWMTimer_ROUTING_OUT_[n] Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b29	Reserved	Always read as 0.	R
b28 to b24	bROUTING_OUTPUT_OUT_[4+n*5]	Configuration of the Output PWM_OUT[e+n*5]: 5'd0: PWM_OUT = PWMTimer Core OUT[0] 5'd1: PWM_OUT = PWMTimer Core OUT[1] 5'dX: PWM_OUT = PWMTimer Core OUT[X] (X = 0..15) 5'd15: PWM_OUT = PWMTimer Core OUT[15] 5'dY: Reserved (Y = 16..31) For these bits e:4 (PWM_OUT 4, 9, 14, 19). ***Note*)** The value after reset is based on suffix number [e+n*5].	R/W
b23	Reserved	Always read as 0.	R
b22 to b18	bROUTING_OUTPUT_OUT_[3+n*5]	See above with e:3 (PWM_OUT 3, 8, 13, 18)	R/W
b17	Reserved	Always read as 0.	R
b16 to b12	bROUTING_OUTPUT_OUT_[2+n*5]	See above with e:2 (PWM_OUT 2, 7, 12, 17)	R/W
b11	Reserved	Always read as 0.	R
b10 to b6	bROUTING_OUTPUT_OUT_[1+n*5]	See above with e:1 (PWM_OUT 1, 6, 11, 16)	R/W
b5	Reserved	Always read as 0.	R
b4 to b0	bROUTING_OUTPUT_OUT_[0+n*5]	See above with e:0 (PWM_OUT 0, 5, 10, 15)	R/W

1.4.43 rPWMTimer_ROUTING_OUTCTRL_0 − Configuration of OutputCtrl0 Module's Inputs

Address: 4006 B800h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—					—			—			—				
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—			bROUTING_OUTCTRL_SET_0					—			—				
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.45 rPWMTimer_ROUTING_OUTCTRL_0 Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b27	Reserved	Always read as 0.	R
b26 to b24	Reserved	Keep initial value.	R/W
b23 to b21	Reserved	Always read as 0.	R
b20 to b16	Reserved	Keep initial value.	R/W
b15 to b13	Reserved	Always read as 0.	R
b12 to b8	bROUTING_OUTCTRL_SET_0	Configuration of OutputCtrl Input Signal 5'h00: OutputCtrl0.Set = 1'b0 5'h03: OutputCtrl0.Set = CMP1.0.0 Others: Reserved	R/W
b7 to b5	Reserved	Always read as 0.	R
b4 to b0	Reserved	Keep initial value.	R/W

1.4.44 rPWMTimer_ROUTING_OUTCTRL_1 − Configuration of OutputCtrl1 Module's Inputs

Address: 4006 B804h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—					—			—			—				
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—			bROUTING_OUTCTRL_SET_1					—			—				
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.46 rPWMTimer_ROUTING_OUTCTRL_1 Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b27	Reserved	Always read as 0.	R
b26 to b24	Reserved	Keep initial value.	R/W
b23 to b21	Reserved	Always read as 0.	R
b20 to b16	Reserved	Keep initial value.	R/W
b15 to b13	Reserved	Always read as 0.	R
b12 to b8	bROUTING_OUTCTRL_SET_1	Configuration of OutputCtrl Input Signal 5'h00: OutputCtrl1.Set = 1'b0 5'h05: OutputCtrl1.Set = CMP1.1.0 Others: Reserved	R/W
b7 to b5	Reserved	Always read as 0.	R
b4 to b0	Reserved	Keep initial value.	R/W

1.4.45 rPWMTimer_ROUTING_OUTCTRL_2 − Configuration of OutputCtrl2 Module's Inputs

Address: 4006 B808h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—					—			—			—				
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—			bROUTING_OUTCTRL_SET_2					—			—				
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.47 rPWMTimer_ROUTING_OUTCTRL_2 Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b27	Reserved	Always read as 0.	R
b26 to b24	Reserved	Keep initial value.	R/W
b23 to b21	Reserved	Always read as 0.	R
b20 to b16	Reserved	Keep initial value.	R/W
b15 to b13	Reserved	Always read as 0.	R
b12 to b8	bROUTING_OUTCTRL_SET_2	Configuration of OutputCtrl Input Signal 5'h00: OutputCtrl2.Set = 1'b0 5'h07: OutputCtrl2.Set = CMP1.2.0 Others: Reserved	R/W
b7 to b5	Reserved	Always read as 0.	R
b4 to b0	Reserved	Keep initial value.	R/W

1.4.46 rPWMTimer_ROUTING_OUTCTRL_3 − Configuration of OutputCtrl3 Module's Inputs

Address: 4006 B80Ch

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—					—			—			—				
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—			bROUTING_OUTCTRL_SET_3					—			—				
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.48 rPWMTimer_ROUTING_OUTCTRL_3 Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b27	Reserved	Always read as 0.	R
b26 to b24	Reserved	Keep initial value.	R/W
b23 to b21	Reserved	Always read as 0.	R
b20 to b16	Reserved	Keep initial value.	R/W
b15 to b13	Reserved	Always read as 0.	R
b12 to b8	bROUTING_OUTCTRL_SET_3	Configuration of OutputCtrl Input Signal 5'h00: OutputCtrl3.Set = 1'b0 5'h09: OutputCtrl3.Set = CMP1.3.0 Others: Reserved	R/W
b7 to b5	Reserved	Always read as 0.	R
b4 to b0	Reserved	Keep initial value.	R/W

1.4.47 rPWMTimer_ROUTING_OUTCTRL_4 − Configuration of OutputCtrl4 Module's Inputs

Address: 4006 B810h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—					—			—			—				
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—			bROUTING_OUTCTRL_SET_4					—			—				
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.49 rPWMTimer_ROUTING_OUTCTRL_4 Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b27	Reserved	Always read as 0.	R
b26 to b24	Reserved	Keep initial value.	R/W
b23 to b21	Reserved	Always read as 0.	R
b20 to b16	Reserved	Keep initial value.	R/W
b15 to b13	Reserved	Always read as 0.	R
b12 to b8	bROUTING_OUTCTRL_SET_4	Configuration of OutputCtrl Input Signal 5'h00: OutputCtrl4.Set = 1'b0 5'h0B: OutputCtrl4.Set = CMP1.4.0 Others: Reserved	R/W
b7 to b5	Reserved	Always read as 0.	R
b4 to b0	Reserved	Keep initial value.	R/W

1.4.48 rPWMTimer_ROUTING_OUTCTRL_5 − Configuration of OutputCtrl5 Module's Inputs

Address: 4006 B814h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—					—			—			—				
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—			bROUTING_OUTCTRL_SET_5					—			—				
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.50 rPWMTimer_ROUTING_OUTCTRL_5 Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b27	Reserved	Always read as 0.	R
b26 to b24	Reserved	Keep initial value.	R/W
b23 to b21	Reserved	Always read as 0.	R
b20 to b16	Reserved	Keep initial value.	R/W
b15 to b13	Reserved	Always read as 0.	R
b12 to b8	bROUTING_OUTCTRL_SET_5	Configuration of OutputCtrl Input Signal 5'h00: OutputCtrl5.Set = 1'b0 5'h0D: OutputCtrl5.Set = CMP1.5.0 Others: Reserved	R/W
b7 to b5	Reserved	Always read as 0.	R
b4 to b0	Reserved	Keep initial value.	R/W

1.4.49 rPWMTimer_ROUTING_OUTCTRL_6 − Configuration of OutputCtrl6 Module's Inputs

Address: 4006 B818h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—					—			—			—				
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—			bROUTING_OUTCTRL_SET_6					—			—				
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.51 rPWMTimer_ROUTING_OUTCTRL_6 Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b27	Reserved	Always read as 0.	R
b26 to b24	Reserved	Keep initial value.	R/W
b23 to b21	Reserved	Always read as 0.	R
b20 to b16	Reserved	Keep initial value.	R/W
b15 to b13	Reserved	Always read as 0.	R
b12 to b8	bROUTING_OUTCTRL_SET_6	Configuration of OutputCtrl Input Signal 5'h00: OutputCtrl6.Set = 1'b0 5'h0F: OutputCtrl6.Set = CMP1.6.0 Others: Reserved	R/W
b7 to b5	Reserved	Always read as 0.	R
b4 to b0	Reserved	Keep initial value.	R/W

1.4.50 rPWMTimer_ROUTING_OUTCTRL_7 − Configuration of OutputCtrl7 Module's Inputs

Address: 4006 B81Ch

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—					—			—			—				
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—			bROUTING_OUTCTRL_SET_7					—			—				
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.52 rPWMTimer_ROUTING_OUTCTRL_7 Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b27	Reserved	Always read as 0.	R
b26 to b24	Reserved	Keep initial value.	R/W
b23 to b21	Reserved	Always read as 0.	R
b20 to b16	Reserved	Keep initial value.	R/W
b15 to b13	Reserved	Always read as 0.	R
b12 to b8	bROUTING_OUTCTRL_SET_7	Configuration of OutputCtrl Input Signal 5'h00: OutputCtrl7.Set = 1'b0 5'h11: OutputCtrl7.Set = CMP1.7.0 Others: Reserved	R/W
b7 to b5	Reserved	Always read as 0.	R
b4 to b0	Reserved	Keep initial value.	R/W

1.4.51 rPWMTimer_ROUTING_OUTCTRL_8 − Configuration of OutputCtrl8 Module's Inputs

Address: 4006 B820h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—					—			—			—				
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—			bROUTING_OUTCTRL_SET_8					—			—				
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.53 rPWMTimer_ROUTING_OUTCTRL_8 Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b27	Reserved	Always read as 0.	R
b26 to b24	Reserved	Keep initial value.	R/W
b23 to b21	Reserved	Always read as 0.	R
b20 to b16	Reserved	Keep initial value.	R/W
b15 to b13	Reserved	Always read as 0.	R
b12 to b8	bROUTING_OUTCTRL_SET_8	Configuration of OutputCtrl Input Signal 5'h00: OutputCtrl8.Set = 1'b0 5'h03: OutputCtrl8.Set = CMP1.0.1 Others: Reserved	R/W
b7 to b5	Reserved	Always read as 0.	R
b4 to b0	Reserved	Keep initial value.	R/W

1.4.52 rPWMTimer_ROUTING_OUTCTRL_9 − Configuration of OutputCtrl9 Module's Inputs

Address: 4006 B824h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—					—			—			—				
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—			bROUTING_OUTCTRL_SET_9					—			—				
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.54 rPWMTimer_ROUTING_OUTCTRL_9 Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b27	Reserved	Always read as 0.	R
b26 to b24	Reserved	Keep initial value.	R/W
b23 to b21	Reserved	Always read as 0.	R
b20 to b16	Reserved	Keep initial value.	R/W
b15 to b13	Reserved	Always read as 0.	R
b12 to b8	bROUTING_OUTCTRL_SET_9	Configuration of OutputCtrl Input Signal 5'h00: OutputCtrl9.Set = 1'b0 5'h05: OutputCtrl9.Set = CMP1.1.1 Others: Reserved	R/W
b7 to b5	Reserved	Always read as 0.	R
b4 to b0	Reserved	Keep initial value.	R/W

1.4.53 rPWMTimer_ROUTING_OUTCTRL_10 − Configuration of OutputCtrl10 Module's Inputs

Address: 4006 B828h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—					—			—			—				
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—			bROUTING_OUTCTRL_SET_10					—			—				
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.55 rPWMTimer_ROUTING_OUTCTRL_10 Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b27	Reserved	Always read as 0.	R
b26 to b24	Reserved	Keep initial value.	R/W
b23 to b21	Reserved	Always read as 0.	R
b20 to b16	Reserved	Keep initial value.	R/W
b15 to b13	Reserved	Always read as 0.	R
b12 to b8	bROUTING_OUTCTRL_SET_10	Configuration of OutputCtrl Input Signal 5'h00: OutputCtrl10.Set = 1'b0 5'h07: OutputCtrl10.Set = CMP1.2.1 Others: Reserved	R/W
b7 to b5	Reserved	Always read as 0.	R
b4 to b0	Reserved	Keep initial value.	R/W

1.4.54 rPWMTimer_ROUTING_OUTCTRL_11 − Configuration of OutputCtrl11 Module's Inputs

Address: 4006 B82Ch

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—					—			—			—				
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—			bROUTING_OUTCTRL_SET_11					—			—				
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.56 rPWMTimer_ROUTING_OUTCTRL_11 Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b27	Reserved	Always read as 0.	R
b26 to b24	Reserved	Keep initial value.	R/W
b23 to b21	Reserved	Always read as 0.	R
b20 to b16	Reserved	Keep initial value.	R/W
b15 to b13	Reserved	Always read as 0.	R
b12 to b8	bROUTING_OUTCTRL_SET_11	Configuration of OutputCtrl Input Signal 5'h00: OutputCtrl11.Set = 1'b0 5'h09: OutputCtrl11.Set = CMP1.3.1 Others: Reserved	R/W
b7 to b5	Reserved	Always read as 0.	R
b4 to b0	Reserved	Keep initial value.	R/W

1.4.55 rPWMTimer_ROUTING_OUTCTRL_12 − Configuration of OutputCtrl12 Module's Inputs

Address: 4006 B830h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—					—			—			—				
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—			bROUTING_OUTCTRL_SET_12					—			—				
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.57 rPWMTimer_ROUTING_OUTCTRL_12 Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b27	Reserved	Always read as 0.	R
b26 to b24	Reserved	Keep initial value.	R/W
b23 to b21	Reserved	Always read as 0.	R
b20 to b16	Reserved	Keep initial value.	R/W
b15 to b13	Reserved	Always read as 0.	R
b12 to b8	bROUTING_OUTCTRL_SET_12	Configuration of OutputCtrl Input Signal 5'h00: OutputCtrl12.Set = 1'b0 5'h0B: OutputCtrl12.Set = CMP1.4.1 Others: Reserved	R/W
b7 to b5	Reserved	Always read as 0.	R
b4 to b0	Reserved	Keep initial value.	R/W

1.4.56 rPWMTimer_ROUTING_OUTCTRL_13 − Configuration of OutputCtrl13 Module's Inputs

Address: 4006 B834h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—					—			—			—				
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—			bROUTING_OUTCTRL_SET_13					—			—				
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.58 rPWMTimer_ROUTING_OUTCTRL_13 Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b27	Reserved	Always read as 0.	R
b26 to b24	Reserved	Keep initial value.	R/W
b23 to b21	Reserved	Always read as 0.	R
b20 to b16	Reserved	Keep initial value.	R/W
b15 to b13	Reserved	Always read as 0.	R
b12 to b8	bROUTING_OUTCTRL_SET_13	Configuration of OutputCtrl Input Signal 5'h00: OutputCtrl13.Set = 1'b0 5'h0D: OutputCtrl13.Set = CMP1.5.1 Others: Reserved	R/W
b7 to b5	Reserved	Always read as 0.	R
b4 to b0	Reserved	Keep initial value.	R/W

1.4.57 rPWMTimer_ROUTING_OUTCTRL_14 − Configuration of OutputCtrl14 Module's Inputs

Address: 4006 B838h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—					—			—			—				
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—			bROUTING_OUTCTRL_SET_14					—			—				
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.59 rPWMTimer_ROUTING_OUTCTRL_14 Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b27	Reserved	Always read as 0.	R
b26 to b24	Reserved	Keep initial value.	R/W
b23 to b21	Reserved	Always read as 0.	R
b20 to b16	Reserved	Keep initial value.	R/W
b15 to b13	Reserved	Always read as 0.	R
b12 to b8	bROUTING_OUTCTRL_SET_14	Configuration of OutputCtrl Input Signal 5'h00: OutputCtrl14.Set = 1'b0 5'h0F: OutputCtrl14.Set = CMP1.6.1 Others: Reserved	R/W
b7 to b5	Reserved	Always read as 0.	R
b4 to b0	Reserved	Keep initial value.	R/W

1.4.58 rPWMTimer_ROUTING_OUTCTRL_15 − Configuration of OutputCtrl15 Module's Inputs

Address: 4006 B83Ch

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—					—			—			—				
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—			bROUTING_OUTCTRL_SET_15					—			—				
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1.60 rPWMTimer_ROUTING_OUTCTRL_15 Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b27	Reserved	Always read as 0.	R
b26 to b24	Reserved	Keep initial value.	R/W
b23 to b21	Reserved	Always read as 0.	R
b20 to b16	Reserved	Keep initial value.	R/W
b15 to b13	Reserved	Always read as 0.	R
b12 to b8	bROUTING_OUTCTRL_SET_15	Configuration of OutputCtrl Input Signal 5'h00: OutputCtrl15.Set = 1'b0 5'h11: OutputCtrl15.Set = CMP1.7.1 Others: Reserved	R/W
b7 to b5	Reserved	Always read as 0.	R
b4 to b0	Reserved	Keep initial value.	R/W

1.5 Operation

1.5.1 PWMTimer Top Interconnect and Multiplexing

The 40 external inputs are synchronized, and each can be assigned to PWMTimer Core input signals. It is also possible to assign the same external input.

PWMTimer Core output signals can be assigned to each of the 20 external outputs.

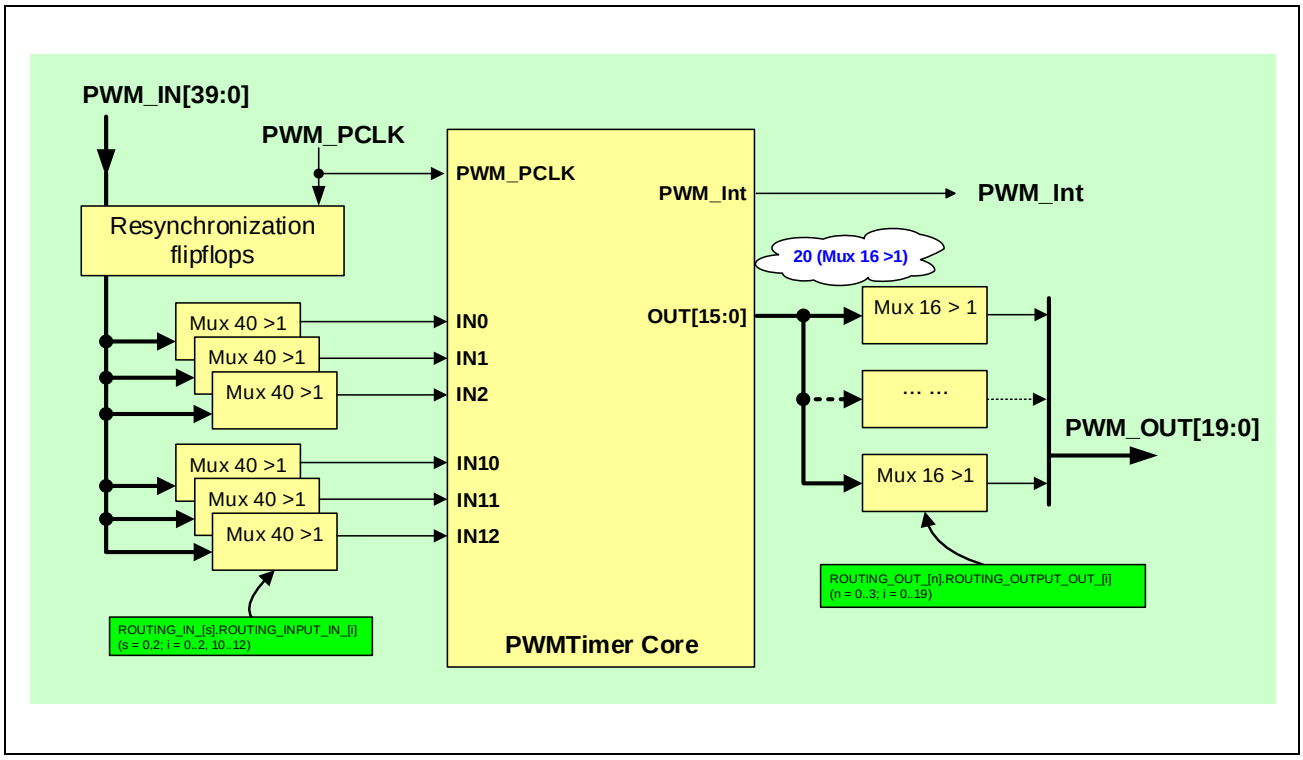


Figure 1.2 PWMTimer Top Synoptic

See rPWMTimer_ROUTING_IN_[s] (s = 0, 2) and rPWMTimer_ROUTING_OUT_[n] (n = 0..3) for registers details.

NOTE

In the figures in this chapter, register and bit names are shown in an abbreviated form.

1.5.2 PWMTimer Core

The figure below summarizes the features and the routing possibilities available in the PWMTimer Core system.

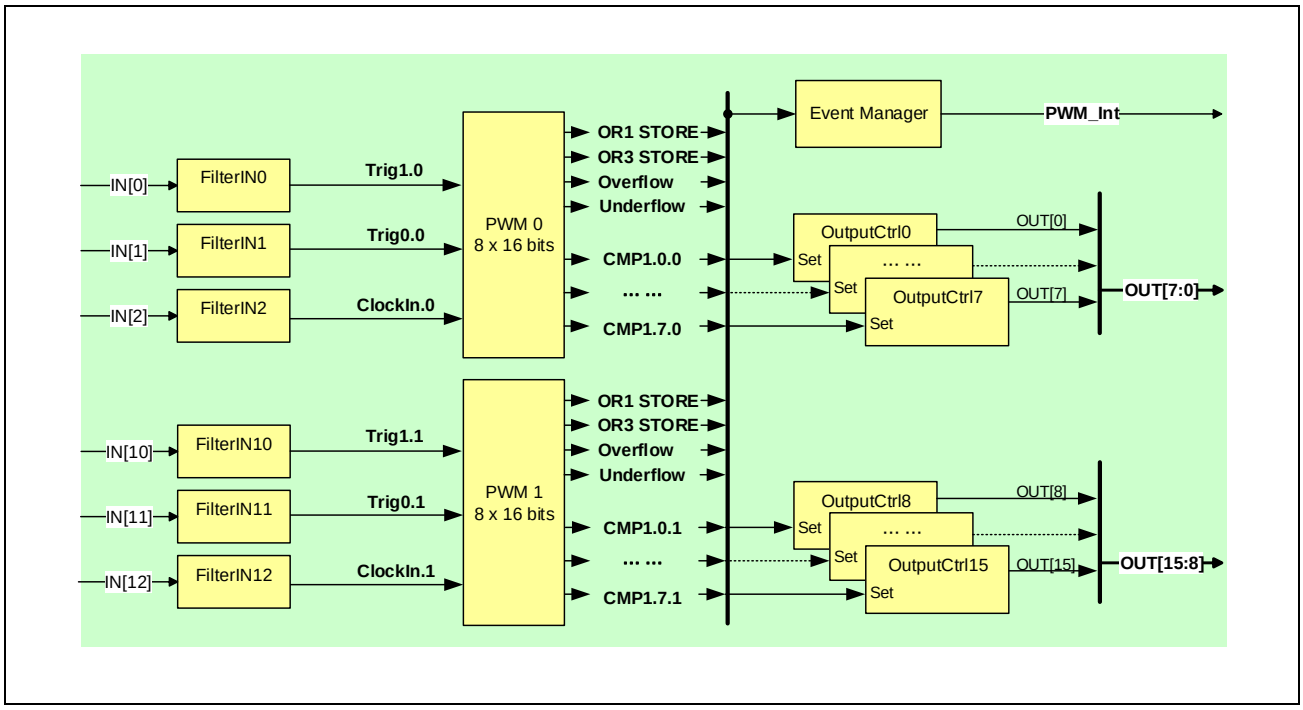


Figure 1.3 PWMTimer Core Synoptic

1.5.3 PWMTimer Core Interconnection

The following tables show the interconnection possibilities between PWMTimer Core signals and the inputs of PWM module and OutputCtrl modules. Refer to **Section 1.5.2, PWMTimer Core**.

1.5.3.1 PWM Module Routing Tables

Refer to **Section 1.5.6, PWM Module** for more details about the functions and the input signals. Each PWM module has two trigger inputs and one clock input.

Table 1.61 PWM Input Connection

From FilterIN Output	To PWM 0 Input
FilterIN0	Trig1.0
FilterIN1	Trig0.0
FilterIN2	ClockIn.0
From FilterIN Output	To PWM 1 Input
FilterIN10	Trig1.1
FilterIN11	Trig0.1
FilterIN12	ClockIn.1

1.5.3.2 OutputCtrl Module Routing Tables

Refer to **Section 1.5.5, OutputCtrl Module** for more details about the functions and the input signals.

Table 1.62 OutputCtrl Input Connection

From PWM 0 Output	To OutputCtrl Input
CMP1.0.0 (single counter 0)	OutputCtrl0.Set
CMP1.1.0 (single counter 1)	OutputCtrl1.Set
CMP1.2.0 (single counter 2)	OutputCtrl2.Set
CMP1.3.0 (single counter 3)	OutputCtrl3.Set
CMP1.4.0 (single counter 4)	OutputCtrl4.Set
CMP1.5.0 (single counter 5)	OutputCtrl5.Set
CMP1.6.0 (single counter 6)	OutputCtrl6.Set
CMP1.7.0 (single counter 7)	OutputCtrl7.Set
From PWM 1 Output	To OutputCtrl Input
CMP1.0.1 (single counter 0)	OutputCtrl8.Set
CMP1.1.1 (single counter 1)	OutputCtrl9.Set
CMP1.2.1 (single counter 2)	OutputCtrl10.Set
CMP1.3.1 (single counter 3)	OutputCtrl11.Set
CMP1.4.1 (single counter 4)	OutputCtrl12.Set
CMP1.5.1 (single counter 5)	OutputCtrl13.Set
CMP1.6.1 (single counter 6)	OutputCtrl14.Set
CMP1.7.1 (single counter 7)	OutputCtrl15.Set

See rPWMTimer_ROUTING_OUTCTRL_[n] (n = 0..15) for registers details.

1.5.4 FilterIN Module

This section describes the filtering stage of PWMTimer.

Each PWMTimer input from IN0 to IN2 and IN10 to IN12 has its own FilterIN module.

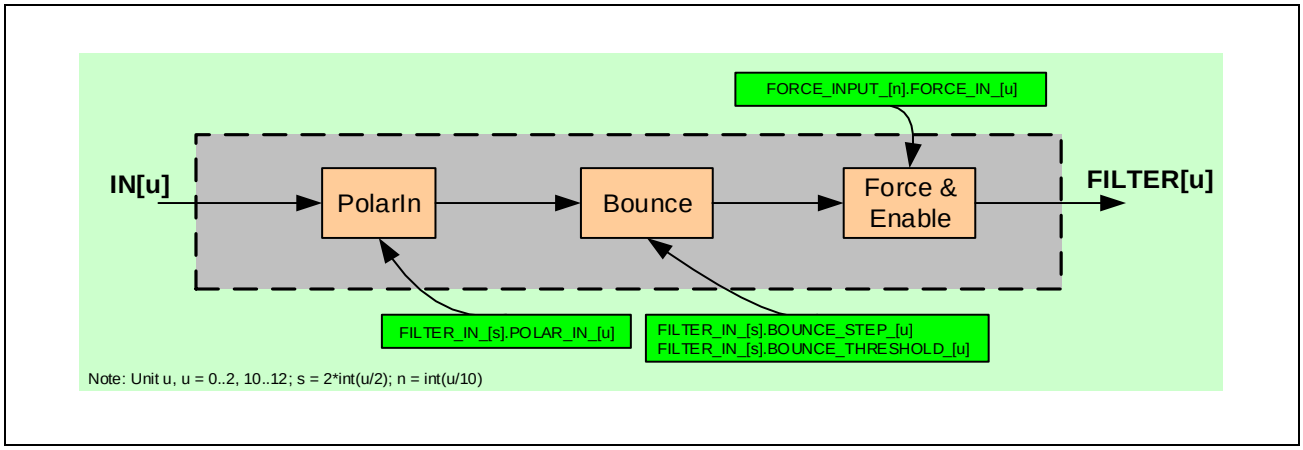


Figure 1.4 FilterIN Module

FilterIN module has three functions that are explained in the sections below.

See rPWMTimer_FILTER_IN_[s] (s = 0, 2, 10, 12) and rPWMTimer_FORCE_INPUT_[n] (n = 0..1) for registers details.

1.5.4.1 PolarIn

The purpose is to allow the user to switch between Direct and Inverted logical signal coming from the outside of the chip.

See rPWMTimer_FILTER_IN_[s] (s = 0, 2, 10, 12) for registers details.

1.5.4.2 Bounce

The Bounce is a configurable bounce filter; it can use two different clocks, one for fast input allowing bounce filter value from 0 to 81.84 µs with a precision of 80 ns; and one for slow input allowing bounce filter value from 0 to 20.95104 ms with a precision of 20.48 µs.

Any transition on the input of the Bounce will reset the counter.

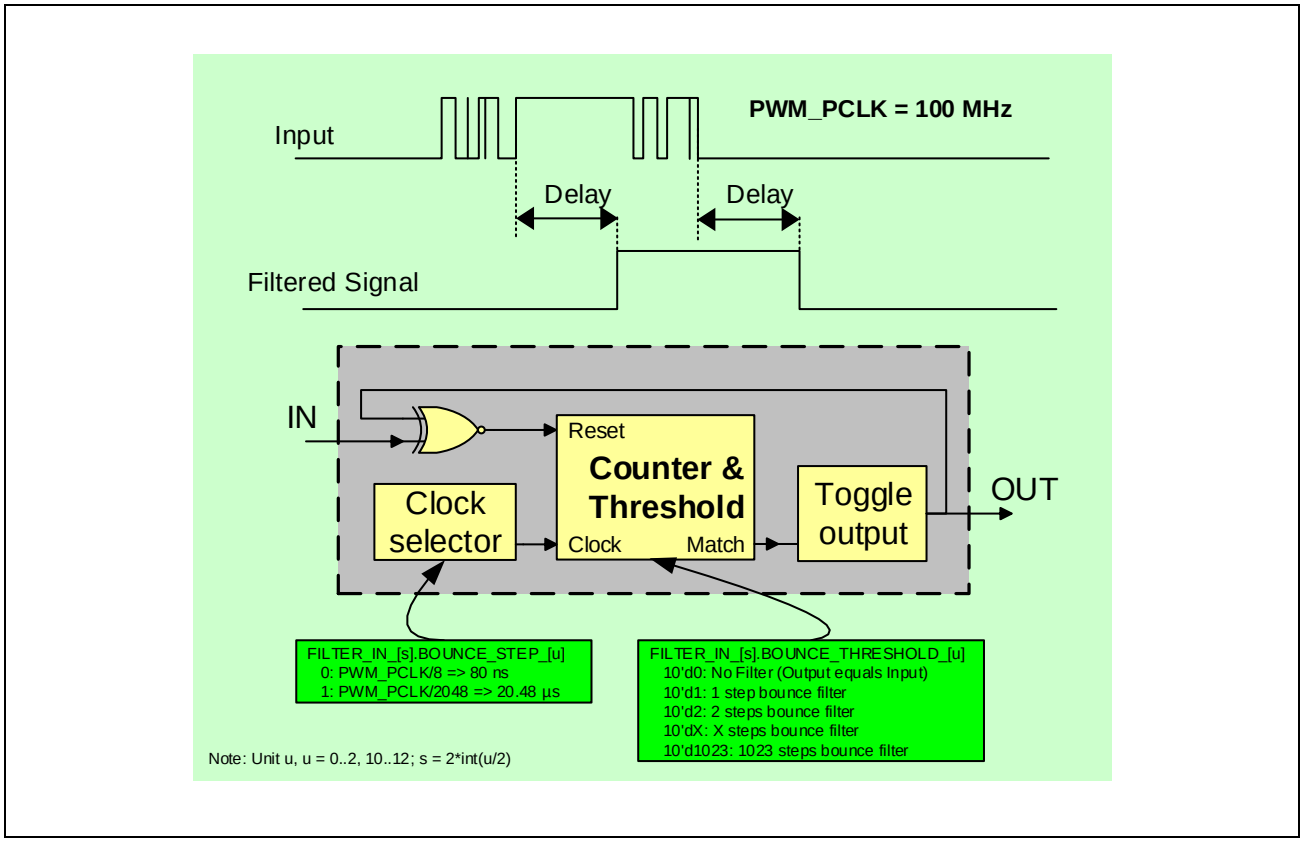


Figure 1.5 Bounce

See rPWMTimer_FILTER_IN_[s] (s = 0, 2, 10, 12) for registers details.

1.5.4.3 Force & Enable

The Force & Enable gives the user the opportunity to force a signal to ‘1’ or ‘0’.

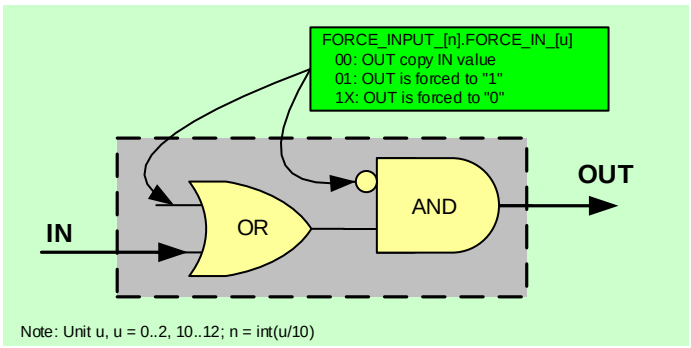


Figure 1.6 Force & Enable

See rPWMTimer_FORCE_INPUT_[n] (n = 0..1) for registers details.

NOTE

The Force & Enable is also used by OutputCtrl; “Force & Enable” seen in the architecture refers to this chapter.

1.5.5 OutputCtrl Module

This module generates the outputs of the PWMTimer.

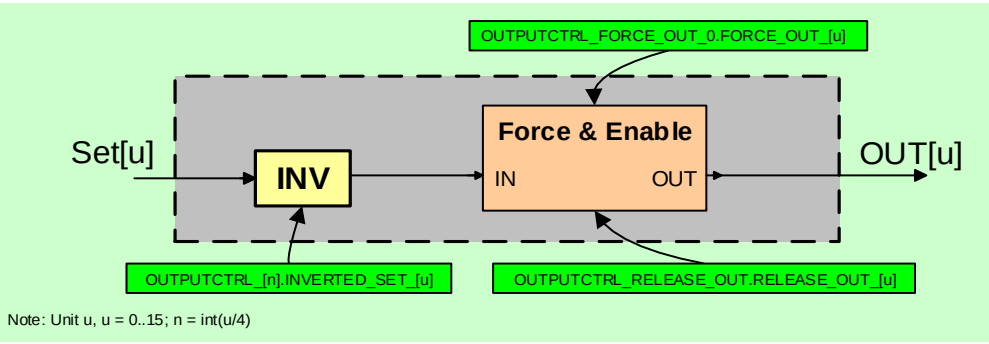


Figure 1.7 OutputCtrl Module

In the released state (after reset), OUT copy IN value in ”Force & Enable”.

The output signal is generated on PWM_PCLK and it can be inverted or force to “0” or “1”.

See rPWMTimer_OUTPUTCTRL_[n] (n = 0..3), rPWMTimer_OUTPUTCTRL_FORCE_OUT_0 and rPWMTimer_OUTPUTCTRL_RELEASE_OUT for registers details.

1.5.6 PWM Module

The PWM module is a bundle of 16-bit counters that can share triggers, inputs or be cascaded for 32-bit counter.

- Each PWM contains eight single counter modules, two Clock Prescalers.
- Each single counter module can be cascaded with the next single counter module in order to add 16 bits at the deep of the counter, cascading two the counters will result in a 32-bit deep counter.
- Each single counter module can generate a output signals using the controls detailed in **Section 1.5.6.2(3), Outputs Generator**.

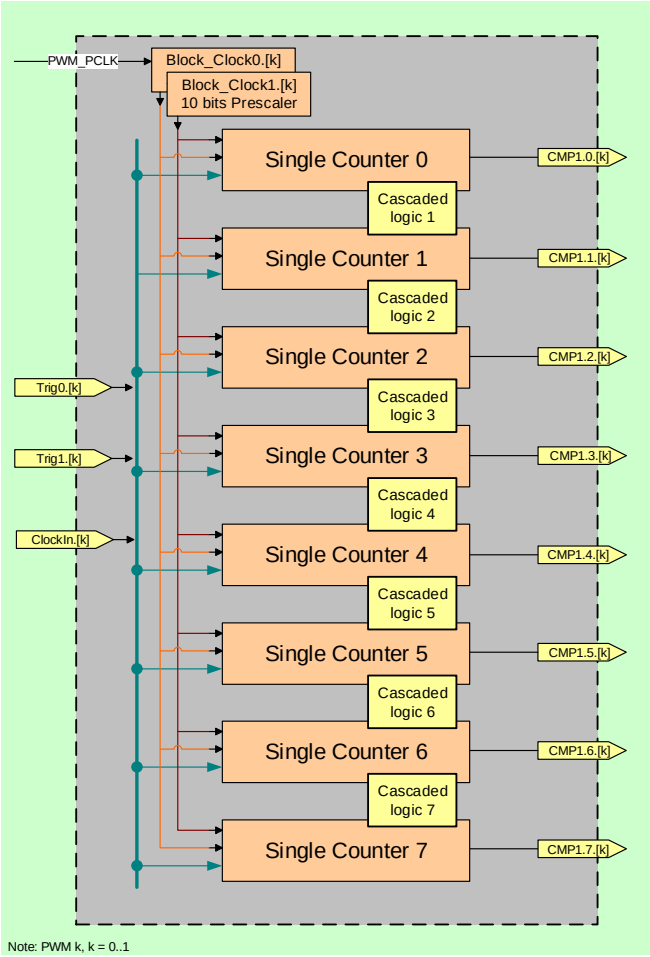


Figure 1.8 PWM Module

NOTE

This section basically uses the following indexes.

- k: PWM module (k = 0..1)
- i: Single counter module (i = 0..7)

1.5.6.1 Clock Prescaler

Each PWM module contains two Clock prescaler named Block_Clock0.[k] and Block_Clock1.[k] that divide the PWM_PCLK clock from 2 to 2048 to generate a derived clock.

See rPWMTimer_PWM_BLOCK_CLOCK_[k] (k = 0..1) for registers details.

1.5.6.2 Single Counter Module

In cascaded mode, MAX.[i], MIN.[i] and CMP1.[i] signals are generated by the cascade logic. CarryIn.[i] is only used in cascaded mode.

Each operation of the Timebase counter is controlled by external input, internal signal and software request.

- Start, Stop and Reset: software request
- Clock: external input (ClockIn) or PWM_PCLK prescaler
- Set the counter direction: on max/min value detection or software request
- Capture: at Trig0, Trig1 or internal event Trig2 (max/min value detection)
- Buffer transfer: at Trig0, Trig1 or internal event Trig2 (max/min value detection)

Management of the capture and buffer transfer is detailed in **Section (2)(c), Hardware Store Trigger Generator**.

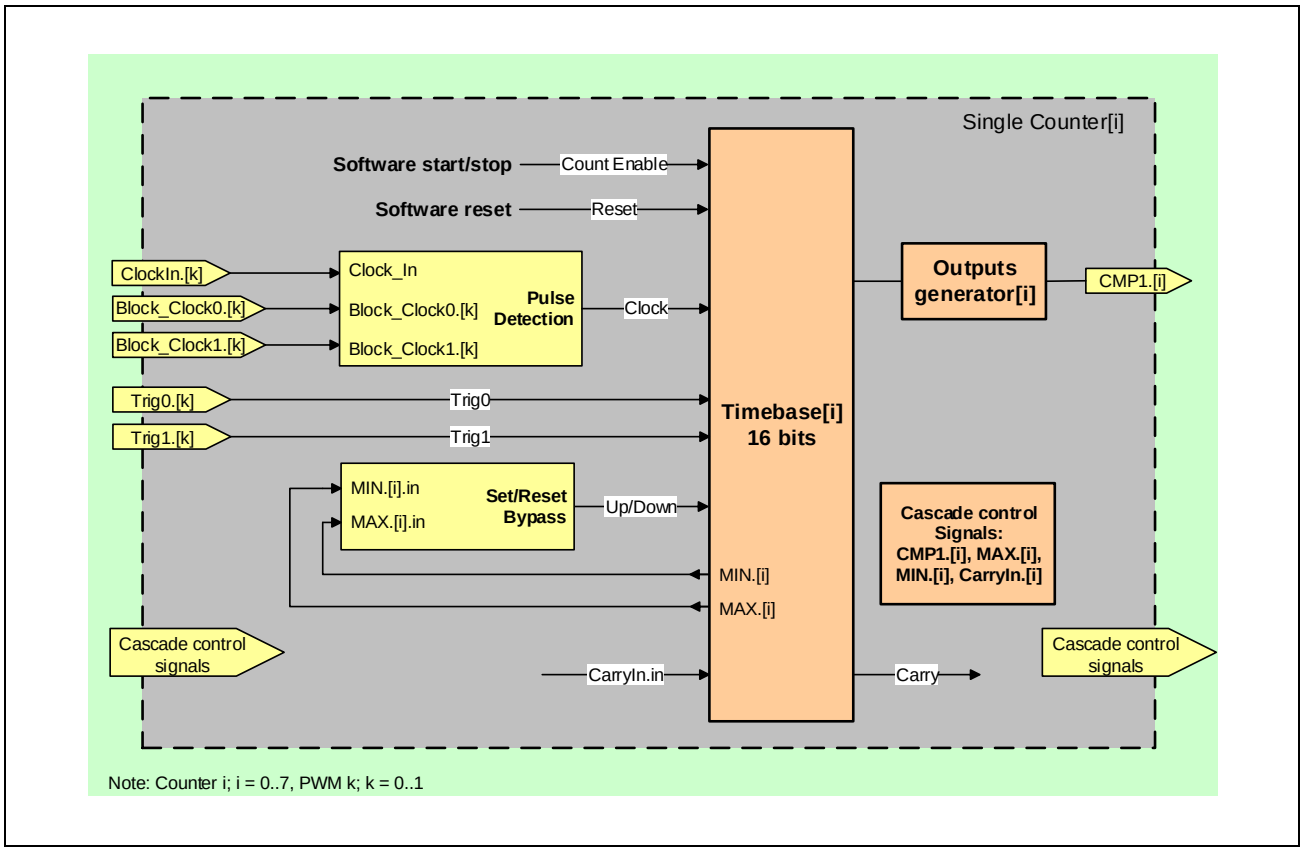


Figure 1.9 Single Counter Module

(1) Single Counter Input Multiplexers

The table below show the signals that can be selected from the external signals.

Table 1.63 Single Counter External Signals Input

Signal of Single Counter	External Signal (PWM k, k = 0..1)
Clock	ClockIn.[k]
Trig0	Trig0.[k]
Trig1	Trig1.[k]

(a) Clock Input

The clock input allows the user to count on each:

- PWM_PCLK period
- Clock prescaler (using the edge detector system)
- ClockIn.[k] input (using the edge detector system)

Using ClockIn.[k] input without the edge detector enables the pulse size measurement.

In order to count on each PWM_PCLK period, the setting
"rPWMTimer_PWM_CLOCK_[q]_[k].bMUXEDCLOCK_[i] = 3'b000" is required.

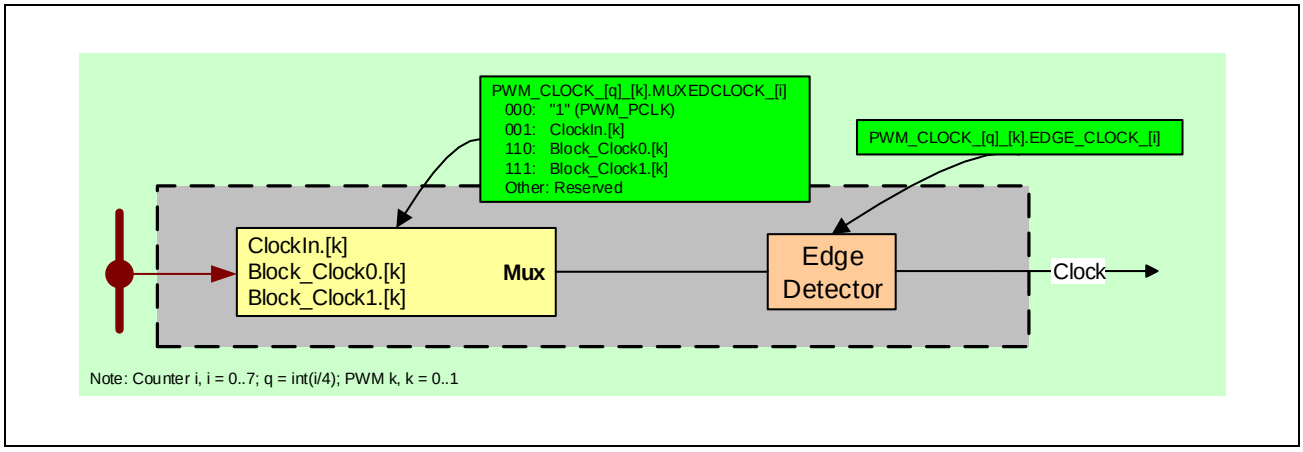


Figure 1.10 Clock Input

See rPWMTimer_PWM_CLOCK_[q]_[k] (q = 0..1, k = 0..1) for registers details.

(b) Up/Down Input

The Up/Down input manages the count direction of the Timebase, it can be used in Set/Reset or Bypass.

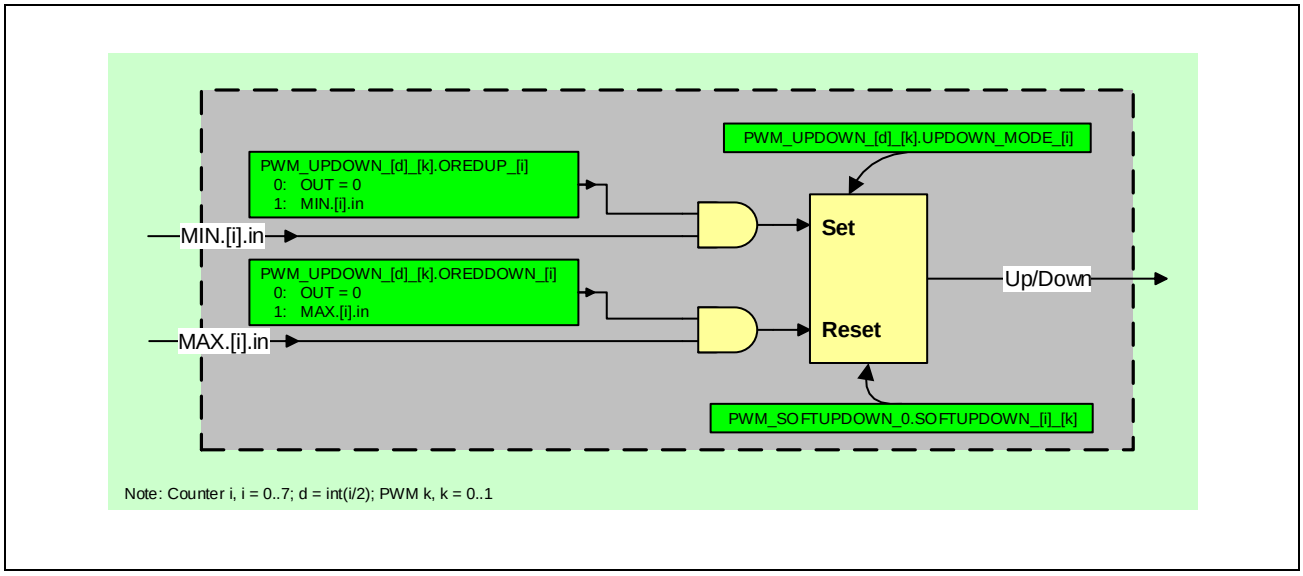


Figure 1.11 Up/Down Input

The Up/Down signal after reset is set to Up.

Min and Max value detection can only be used in Set/Reset mode.

If simultaneous events happen in the Up/Down input while in Set/Reset mode, the Up/Down signal will be set to Up.

NOTE

If software controls counter directions, use Set/Reset mode and fix Set/Reset input to 0.

See rPWMTimer_PWM_UPDOWN_[d]_[k] (d = 0..3, k = 0..1) and rPWMTimer_PWM_SOFTUPDOWN_0 for registers details.

(c) Other Input Functions

- Count Enable function

The Count Enable function manages the Timebase in “enable” or “disable” state, it is synchronized with Timebase’s clock (counting clock).

- The Start event can be triggered by software event.
- The Stop event can be triggered by software event.

The Stop event is kept until next Timebase’s clock if Count Enable is on Enable state. If multiple events happen simultaneously, the system will be set to Stop.

See rPWMTimer_PWM_SOFTSTART and rPWMTimer_PWM_SOFTSTOP for registers details.

- Reset function

The Reset function manages the reset of the Timebase module, it is synchronized with Timebase’s clock (counting clock).

- The Reset event can be triggered by software event.

The Reset event is kept until next Timebase’s clock if Count Enable is on Enable state; the Reset event is transferred immediately when Count Enable is on disable state.

See rPWMTimer_PWM_SOFTRESET for registers details.

- Trig0 and Trig1 input

The Trig0 and Trig1 input are used in the Hardware Store trigger generator which is used for capture and buffer transfer functions (refer to **Section 1.5.6.2(2)(c), Hardware Store Trigger Generator** for more details).

See rPWMTimer_PWM_TRIG0_[k] (k = 0..1) and rPWMTimer_PWM_TRIG1_[k] (k = 0..1) for registers details.

(2) Timebase Module

The Timebase module is the main part of the counter system. This module can be used as a capture or compare function. It manages counting, comparator, capture, reset and buffer transfer systems and generate the events CMP1, MAX, MIN, Underflow, Overflow and Carry.

List of the elements of the Timebase:

- COUNTER VALUE: current counter value.
- 16 bits ALU: increase or decrease the COUNTER VALUE by one.
- OPTION REGISTER: four registers that can be used as compare register, capture registers, max value register or registers for buffer transfer.
- 16 bits comparator: compare the COUNTER VALUE to OPTION REGISTER 2.
- Ranged mode: handle the ranged mode using OPTION REGISTER 0 as the counter max value.
- Hardware Store trigger generator: manage the buffer transfer and capture functions.
- Flag manager: triggers overflow and underflow flags.

For example, the Max signal can use to switch the direction command to “Down” in the Up/Down input, the count-down starts as soon as it reach the max value and will not trigger the overflow flag.

In order to be used easily in cascaded mode, the COUNT_[i][15:0] can also access adjacent 32 bits, see rPWMTimer_TIMEBASE_[i]_[k], rPWMTimer_TIMEBASE_01_[k], rPWMTimer_TIMEBASE_23_[k], rPWMTimer_TIMEBASE_45_[k], rPWMTimer_TIMEBASE_67_[k], rPWMTimer_TIMEBASE_12_[k], rPWMTimer_TIMEBASE_34_[k] and rPWMTimer_TIMEBASE_56_[k] (i = 0..7, k = 0..1) for registers details.

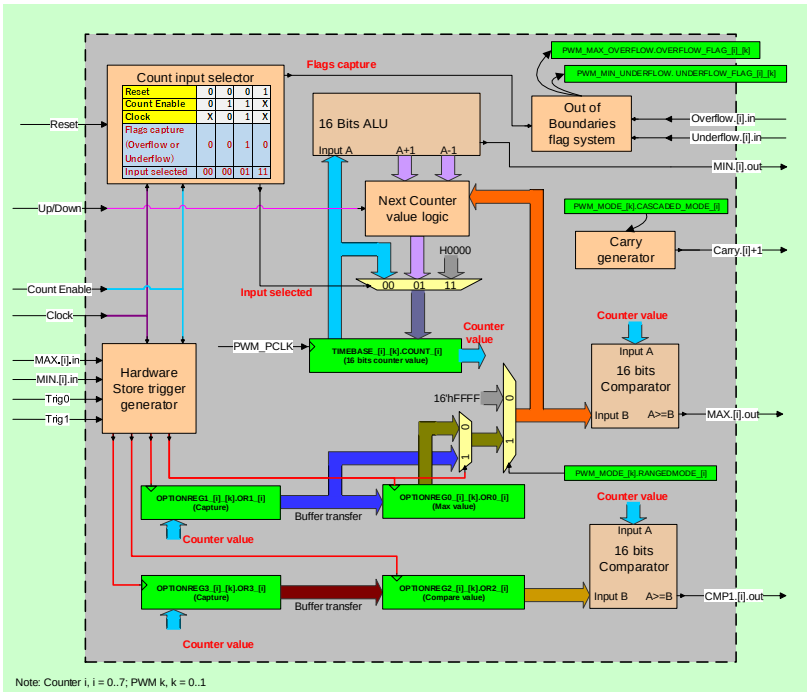


Figure 1.12 Timebase Module

(a) Events Generated by the Timebase Module

The Timebase module generates events on:

- Max value detection: Timebase's counter = max value (Range mode) or 16'hFFFF (Free running mode)
- Min value detection: Timebase's counter = 16'h0000
- Overflow detection: Max value detection and counting up
- Underflow detection: Min value detection and counting down
- Compare match: Timebase's counter ≥ the compare register

The waveform below shows an example of Timebase module event generation.

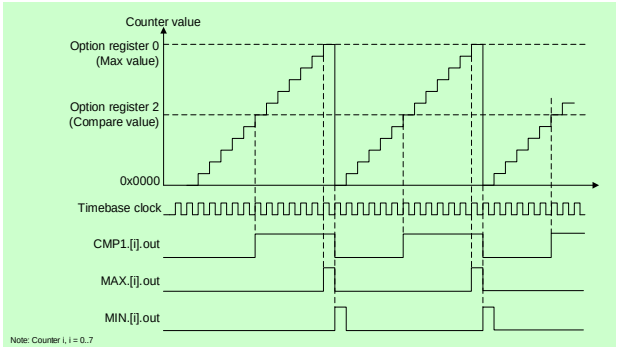


Figure 1.13 Events Generation in Sawtooth

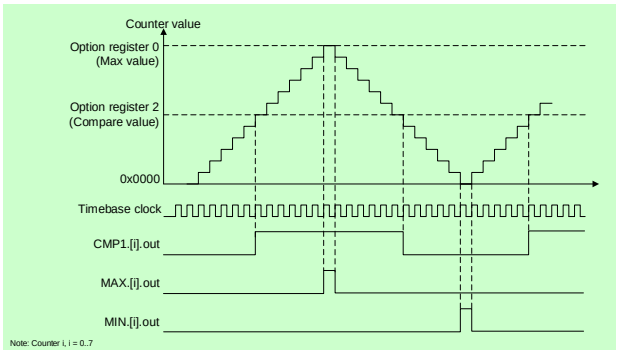


Figure 1.14 Events Generation in Triangular

Interrupt flags can be set on overflow/underflow detection.

See rPWMTimer_PWM_MAX_OVERFLOW and rPWMTimer_PWM_MIN_UNDERFLOW for overflow and underflow flags registers details.

(b) Option Registers System

The four option registers available in each Timebase module can be used for several functions.

Table 1.64 Option Registers Functions

Option Register (OR)	Compare Match	Capture	Max Value	Buffer Transfer
OR0_[i]	Not available	Not available	Yes	From OR1_[i]
OR1_[i]	Not available	Yes	Not available	To OR0_[i]
OR2_[i]	CMP1.[i]	Not available	Not available	From OR3_[i]
OR3_[i]	Not available	Yes	Not available	To OR2_[i]

Functions description:

- Compare Match: Internal signals CMP1.[i] is set to “1” when COUNT_[i] is superior or equal to OR2_[i].
- Capture: Store the COUNT_[i] value in OR1_[i]/OR3_[i] on the store trigger.
- Max Value: OR0_[i] is used to manage Overflow.[i] and MAX.[i] event in ranged mode;
  Load max value from OR0_[i] in COUNT_[i] on underflow event.
- Buffer Transfer: OR1_[i] value is transferred in OR0_[i] on the store trigger.
- Buffer Transfer: OR3_[i] value is transferred in OR2_[i] on the store trigger.

The store trigger of capture and buffer transfer is controlled by the Hardware Store trigger generator.

Details about buffer transfer can be found in the rPWMTimer_TIMEBASE_MUX_[q]_[k] (q = 0..1, k = 0..1) registers description.

See rPWMTimer_OPTIONREG[r]_[i]_[k], rPWMTimer_OPTIONREG[r]_01_[k], rPWMTimer_OPTIONREG[r]_23_[k], rPWMTimer_OPTIONREG[r]_45_[k], rPWMTimer_OPTIONREG[r]_67_[k], rPWMTimer_OPTIONREG[r]_12_[k], rPWMTimer_OPTIONREG[r]_34_[k] and rPWMTimer_OPTIONREG[r]_56_[k] (r = 0..3, i = 0..7, k = 0..1) for option registers details.

(c) Hardware Store Trigger Generator

The Hardware Store trigger generator handles the store trigger of every option register, those triggers are used for capture and buffer transfer functions according to the user configuration.

Store triggers can be set by:

- Max limit reached (using Trig2 signal).
- Min limit reached (using Trig2 signal).
- External event (using Trig0 or Trig1 signals).

Store triggers are synchronous or asynchronous to the Timebase's clock:

In synchronous mode, the store trigger is latched until the next Timebase's clock event (only available for OR0_[i] and OR2_[i]). Any latched trigger is immediately transferred if the Count Enable input switches to "Disable mode". Set to asynchronous when transferring the capture value, otherwise set to synchronous.

Store triggers can be locked by software:

- Lock: rPWMTimer_HWSTORE_LOCK_[k].bHWSTORE_OR[r]_LOCK_[i] (r = 0..3, i = 0..7, k = 0..1)
- Unlock: rPWMTimer_HWSTORE_UNLOCK_[k].bHWSTORE_OR[r]_UNLOCK_[i] (r = 0..3, i = 0..7, k = 0..1)
- Store trigger is locked after reset.

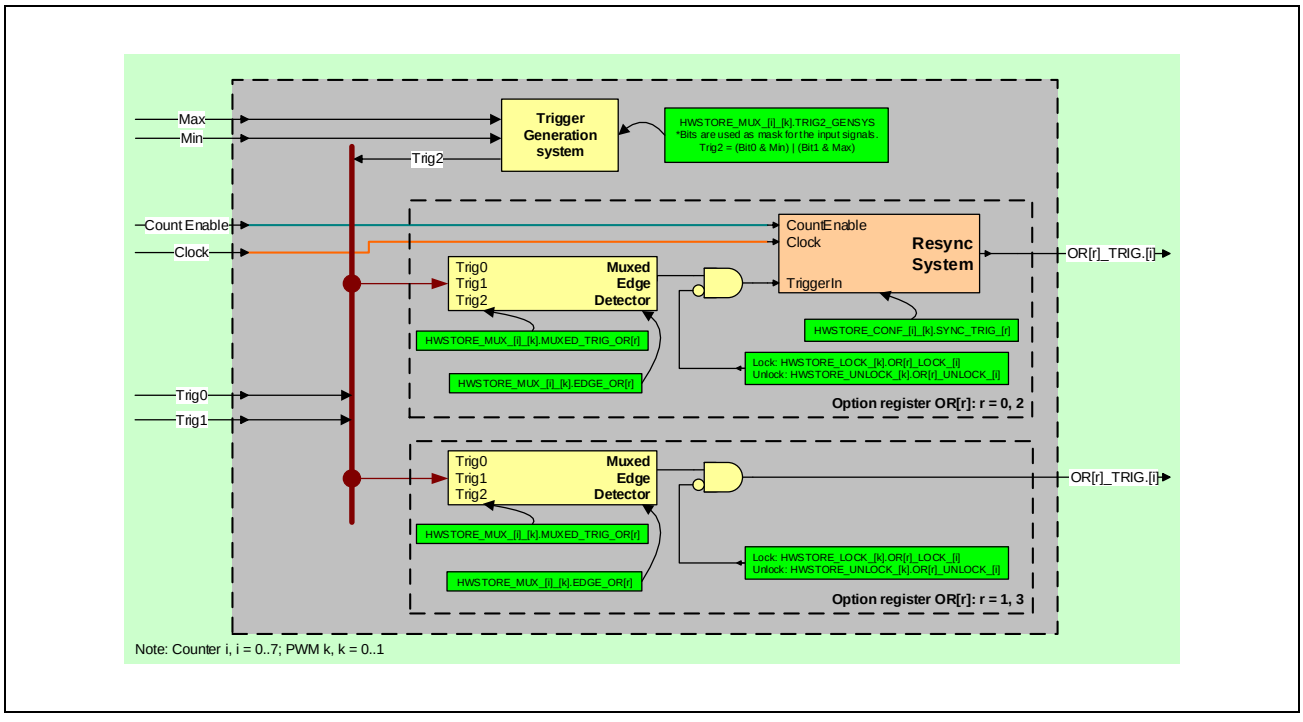


Figure 1.15 Hardware Store Trigger Generator

See rPWMTimer_HWSTORE_CONF_[i]_[k], rPWMTimer_HWSTORE_MUX_[i]_[k], rPWMTimer_HWSTORE_LOCK_[k] and rPWMTimer_HWSTORE_UNLOCK_[k] (i = 0..7, k = 0..1) for registers details.

(d) Ranged Mode

The ranged mode is a mode where the max value is delimited by option register 0, the triggers “MAX.[i]” and “Overflow.[i]” is controlled by the comparison between COUNT_[i] value and the option register 0. In this mode, an overflow will set COUNT_[i] to 0x0000 and an underflow will set COUNT_[i] to the max value programmed.

See rPWMTimer_PWM_MODE_[k] (k = 0..1) for register details.

(3) Outputs Generator

The Outputs generator is the last step of the waveform generation for the PWM module.

The output signal CMP1.[i]:

- Counter Enable = 1
  - Direct: Simple compare match result from Timebase (CMP1.[i].in).
- Count Enable = 0 (disable state)
  - Reset: The output signal is tied to zero.
  - Set: The output signal is tied to one.

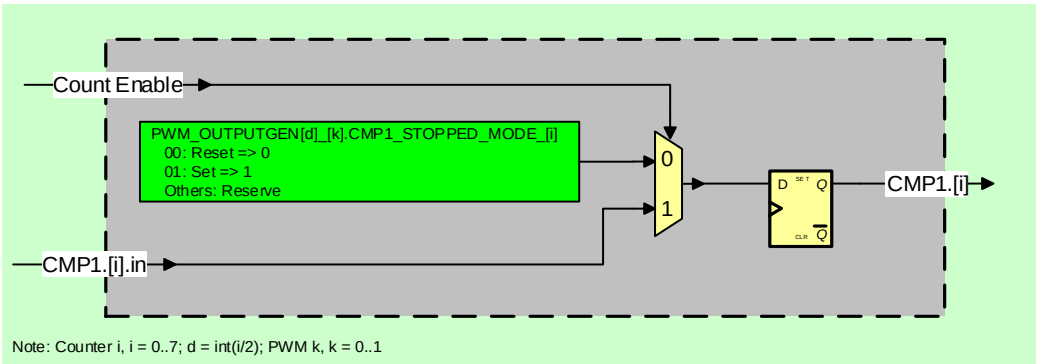


Figure 1.16 Outputs Generator

The signal CMP1.[i].in is resynchronized with the PWM_PCLK clock.

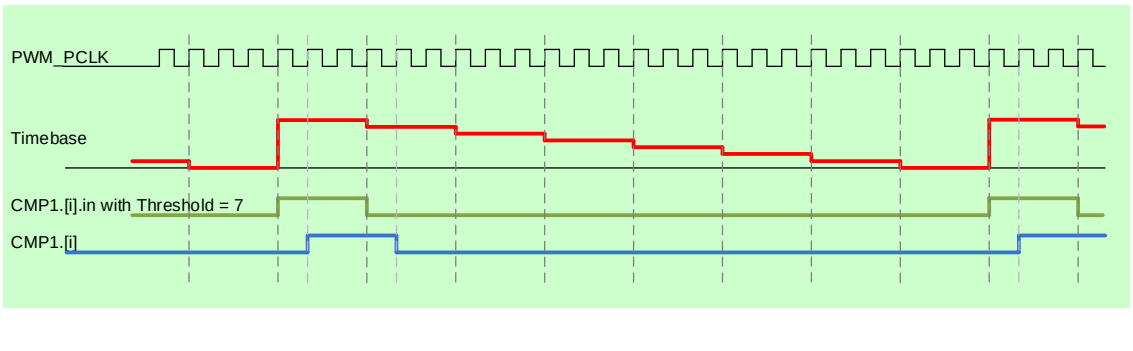


Figure 1.17 Outputs Generator Timing Chart

See rPWMTimer_PWM_OUTPUTGEN[d]_[k] (d = 0..3, k = 0..1) for registers details.

1.5.6.3 Cascading Single Counter Modules

The PWM module creating a counter to 32 bits length using the two single counters.

Be aware when you set the input multiplexer in cascaded mode you will still have to trigger the two single counters involved, for example, if you want to use a filtered input to clock your cascaded counter, the filtered input must be configured to trigger the “Clock” input of the two single counter involved.

Some signals have to be shared and reshaped to be relevant to the cascaded counter created. When the cascaded mode is enabled, the signal generated by the cascade logic is input to each single counter.

The Carry is used as an internal enable for the next counter, allowing it to increase or decrease its value.

The Carry is set when:

- The lower counter value will toggle from 16’h0000 to 16’hFFFF (down-counting).
- The lower counter value will toggle from 16’hFFFF to 16’h0000 (up-counting).
- The 32-bit counter will toggle from “0” to its max value (down-counting).
- The 32-bit counter will toggle from its max value to “0” (up-counting).

Cascaded mode warnings and limitations:

- The single counter input multiplexer settings and the mode (ranged/free-running) must be the same in each counter involved in the 32-bit counter.

NOTE

Cascaded logic [i] configures a 32-bit counter with the previous counter [i-1] as the lower 16-bit. When creating a 32-bit counter, enable cascaded mode for only the upper 16-bit counter [i]. Also, the cascade value setting of the upper 16-bit counter (rPWMTimer_SCALEVALUE_[i]_[k]) should be set to zero.

See rPWMTimer_PWM_MODE_[k] (k = 0..1) for register details about the activation of the cascaded mode between two single counter modules.

1.5.6.4 Master Counter Feature of the Single Counter Modules

In order to improve the flexibility of the PWM, users can set the master counter feature available in rPWMTimer_PWM_MODE_[k] (k = 0..1) register.

Activating this feature on a single counter “S” will replace its own current counter value by the one from the selected single counter “M”; in other words, the single counter “S” will become a slave of the selected single counter “M”, it won’t be able to modify the current counter value anymore and will apply all of its logic (compare and capture system) to the current counter value from single counter “M”. Along with the counter value, the overflow, underflow, min, and max signals are also transferred from the master single counter to its slave(s).

The feature is applied as a chain, meaning that the master counter value selection is propagated along the chain allowing the user to use all the logic elements from up to 8 single counters (compare and capture system) with the same current counter value.

Example: If the single counter 2 is a slave of the single counter 0 and the single counter 3 is a slave of the single counter 2, the single counter 3 will be in fact the slave of the single counter 0. Refer to the figure below.

Rules to follow when using this feature:

- The slave single counter must be set in the same modes (ranged mode, cascaded mode) than its master.
- The slave counter settings of Clock, Count Enable and Up/Down signals must be the same as the master counter.
- Software Reset access to the single counter input multiplexers must be done for both the master single counter and its slave(s) during the same access.

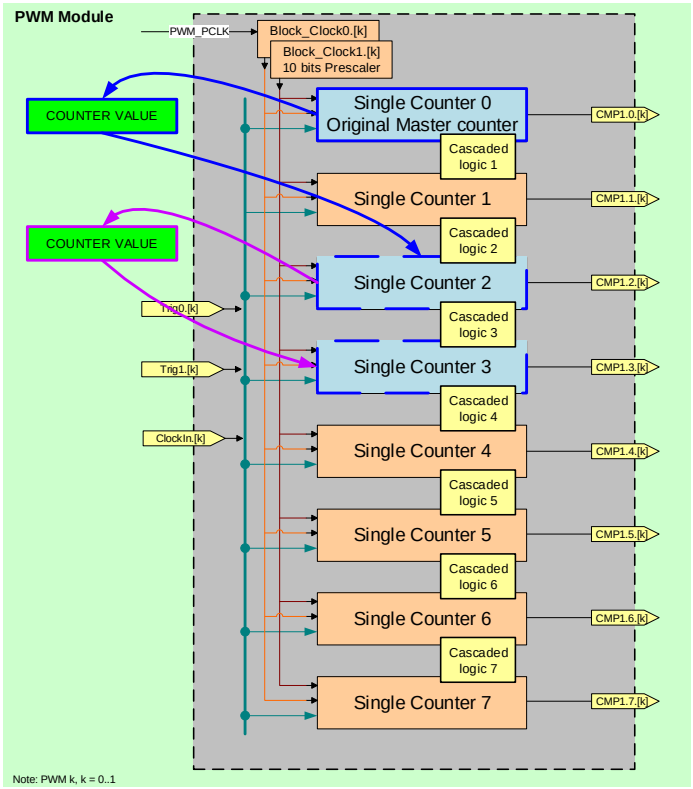
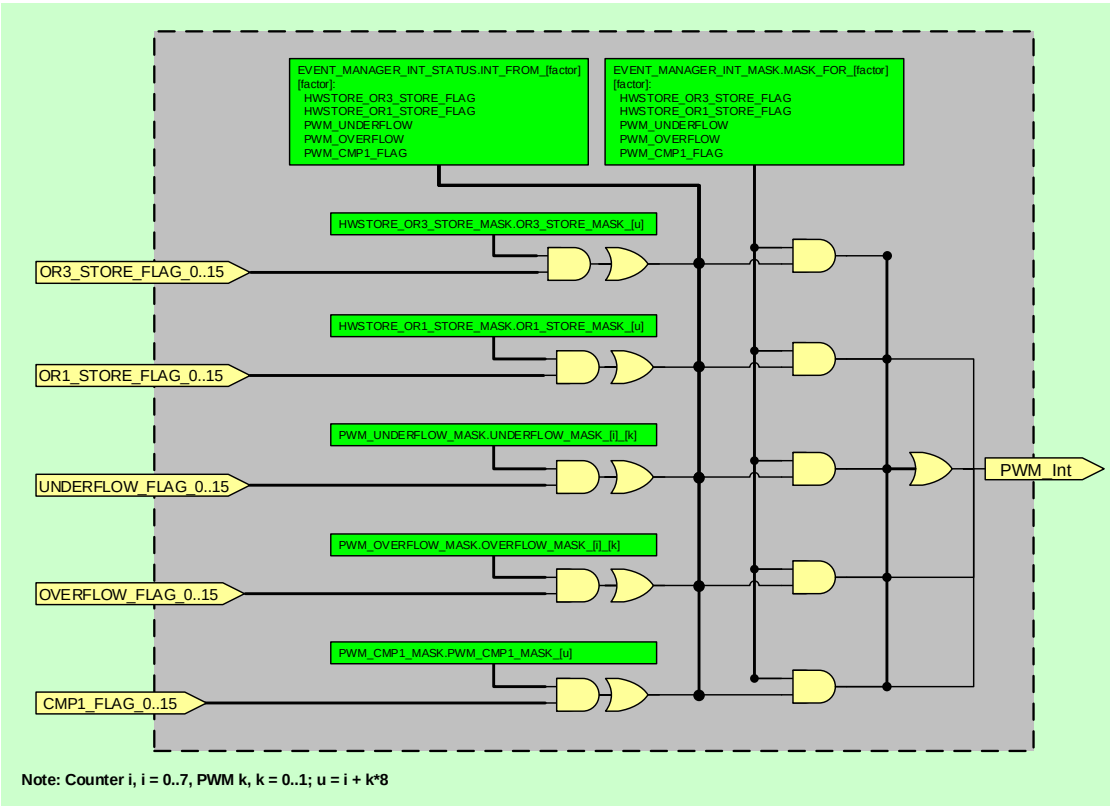


Figure 1.18 Master Counter Feature Example

1.5.7 Event Manager Module

The Event Manager module generates PWMTimer interrupt.

The list of the signals available to generate interrupts is shown in the figure below. The Event Manager summarize the flags of the entire system, if a not-masked flag become active PWMTimer interrupt will be set.



Caution: When the flags set once, they must be reset by software.

Figure 1.19 Event Manager Module

The Event Manager has inputs of factor flags and can be masked at two levels.

The flag status is reflected to the global interrupt system status register according to the mask register that controls each factor. The mask for global interrupt system register masks the global interrupt status and generates the interrupt. In order to disable the interrupt, it is necessary to mask at either level or to clear the factor itself.

See rPWMTimer_EVENT_MANAGER_INT_STATUS, rPWMTimer_PWM_CMP1_FLAG_POLARITY, rPWMTimer_PWM_CMP1_FLAG, rPWMTimer_PWM_MAX_OVERFLOW, rPWMTimer_PWM_MIN_UNDERFLOW, rPWMTimer_HWSTORE_OR1_STORE_FLAG, rPWMTimer_HWSTORE_OR3_STORE_FLAG, rPWMTimer_EVENT_MANAGER_INT_MASK, rPWMTimer_PWM_CMP1_MASK, rPWMTimer_PWM_OVERFLOW_MASK, rPWMTimer_PWM_UNDERFLOW_MASK, rPWMTimer_HWSTORE_OR1_STORE_MASK and rPWMTimer_HWSTORE_OR3_STORE_MASK for Flag collector registers details.

1.5.8 Programming PWMTimer

1.5.8.1 Common Initial Setting Example

Recommended common initial settings for basic operation are as follows.

- Enable OutputCtrl mode

  Set 1'b1 to rPWMTimer_OUTPUTCTRL_[n].bBYPASS_MODE_[u] (u = 0..15, n = 0..3).

  rPWMTimer_OUTPUTCTRL_[n] = 0x40404040

- Enable Trig0 input of Single counter

  Set 3'b001 to rPWMTimer_PWM_TRIG0_[k].bTRIG0_[i] (i = 0..7, k = 0..1).

  rPWMTimer_PWM_TRIG0_[k] = 0x11111111

- Enable Trig1 input of Single counter

  Set 3'b001 to rPWMTimer_PWM_TRIG1_[k].bTRIG1_[i] (i = 0..7, k = 0..1).

  rPWMTimer_PWM_TRIG1_[k] = 0x11111111

- Enable buffer transfer setting for option register

  Set 1'b1 to rPWMTimer_TIMEBASE_MUX_[q]_[k].bTIMEBASE_MUX_OR[r]_[i]
  (r = 0, 2, i = 0..7, q = 0..1, k = 0..1).

  rPWMTimer_TIMEBASE_MUX_[q]_[k] = 0x03030303

- Setting the store trigger for option register (when transferring the capture value)

  Set 1'b0 to rPWMTimer_HWSTORE_CONF_[i]_[k].bHWSTORE_SYNC_TRIG_[r] (r = 0, 2, i = 0..7, k = 0..1).

  rPWMTimer_HWSTORE_CONF_[i]_[k] = 0x00000000

- Unlock for option register

  Set 1'b1 to rPWMTimer_HWSTORE_UNLOCK_[k].bHWSTORE_OR[r]_UNLOCK_[i] (r = 0..3, i = 0..7, k = 0..1).

  rPWMTimer_HWSTORE_UNLOCK_[k] = 0xFFFFFFFF

- Enable input for OutputCtrl

  Set (5'h03 + [n mod 8] * 2) to rPWMTimer_ROUTING_OUTCTRL_[n].bROUTING_OUTCTRL_SET_[n] (n = 0..15).

  rPWMTimer_ROUTING_OUTCTRL_0/rPWMTimer_ROUTING_OUTCTRL_8 = 0x00000300

  rPWMTimer_ROUTING_OUTCTRL_1/rPWMTimer_ROUTING_OUTCTRL_9 = 0x00000500

  rPWMTimer_ROUTING_OUTCTRL_2/rPWMTimer_ROUTING_OUTCTRL_10 = 0x00000700

  rPWMTimer_ROUTING_OUTCTRL_3/rPWMTimer_ROUTING_OUTCTRL_11 = 0x00000900

  rPWMTimer_ROUTING_OUTCTRL_4/rPWMTimer_ROUTING_OUTCTRL_12 = 0x00000B00

  rPWMTimer_ROUTING_OUTCTRL_5/rPWMTimer_ROUTING_OUTCTRL_13 = 0x00000D00

  rPWMTimer_ROUTING_OUTCTRL_6/rPWMTimer_ROUTING_OUTCTRL_14 = 0x00000F00

  rPWMTimer_ROUTING_OUTCTRL_7/rPWMTimer_ROUTING_OUTCTRL_15 = 0x00001100

1.5.8.2 PWM Output by Compare Match

The compare match signal (counter value ≥ compare value) can be output from PWM_OUT.

In this example, the up counter is operated in range mode and the compare match signal is output. When the counter value reaches the value in option register 0 (maximum), the overflow occurs, and the interrupt can output from PWM_Int.

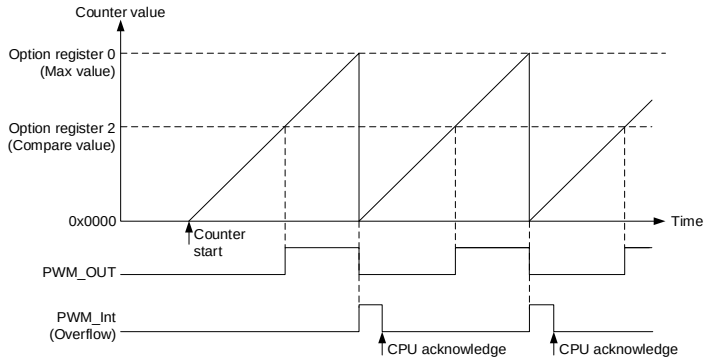


Figure 1.20 Example of PWM Output Operation

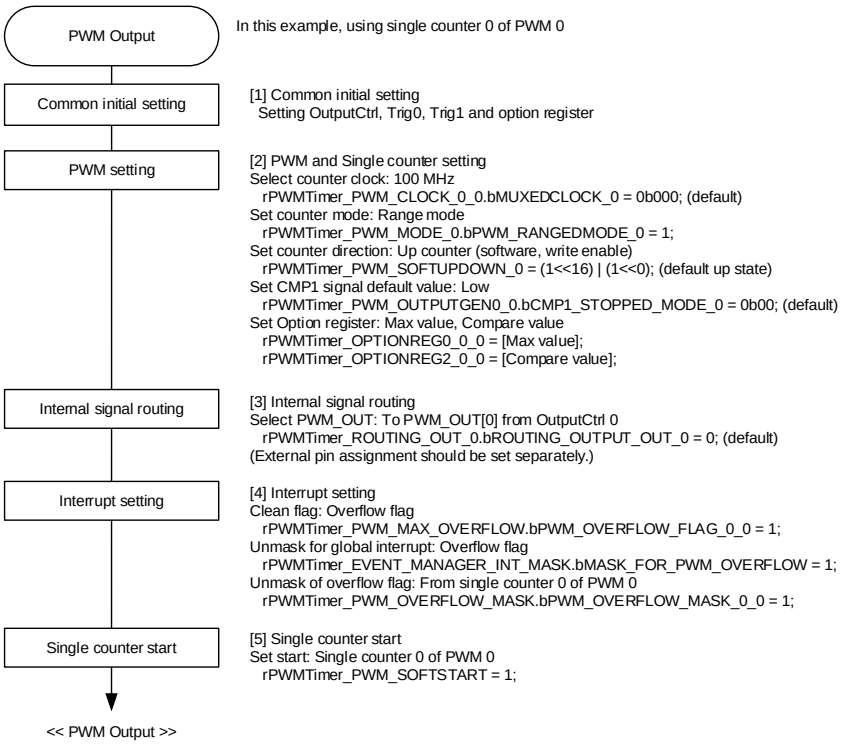


Figure 1.21 Example of PWM Output Setting

1.5.8.3 Master Counter

The master counter function can increase the number of the capture input and the compare match output. Refer to **Section 1.5.6.4, Master Counter Feature of the Single Counter Modules**.

In this example, the master counter function is used to operate three counters synchronously, and each compare match signal is output from PWM_OUT.

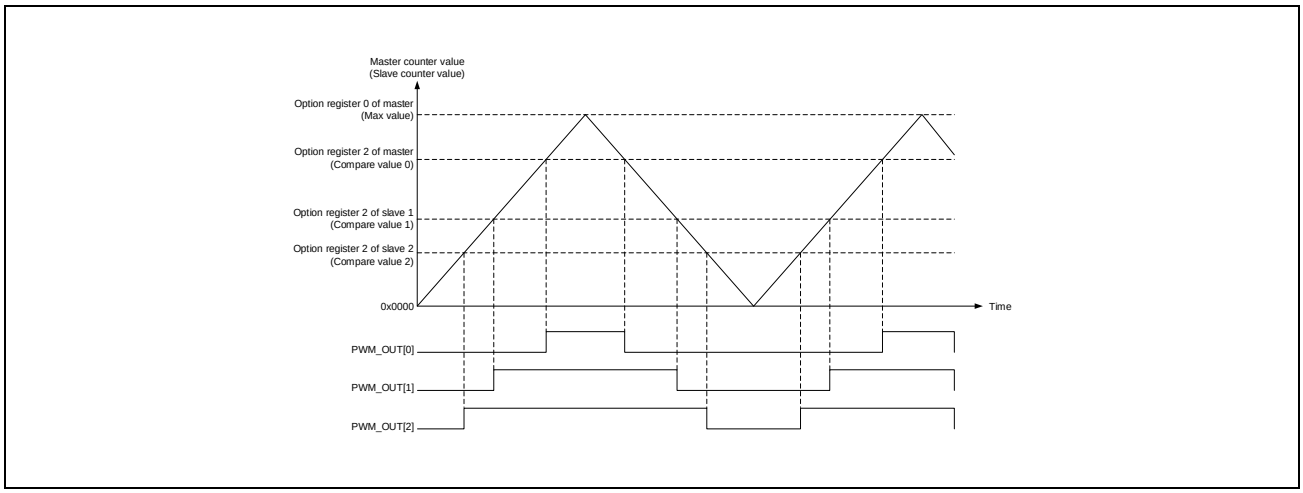


Figure 1.22 Example of Master Counter Operation

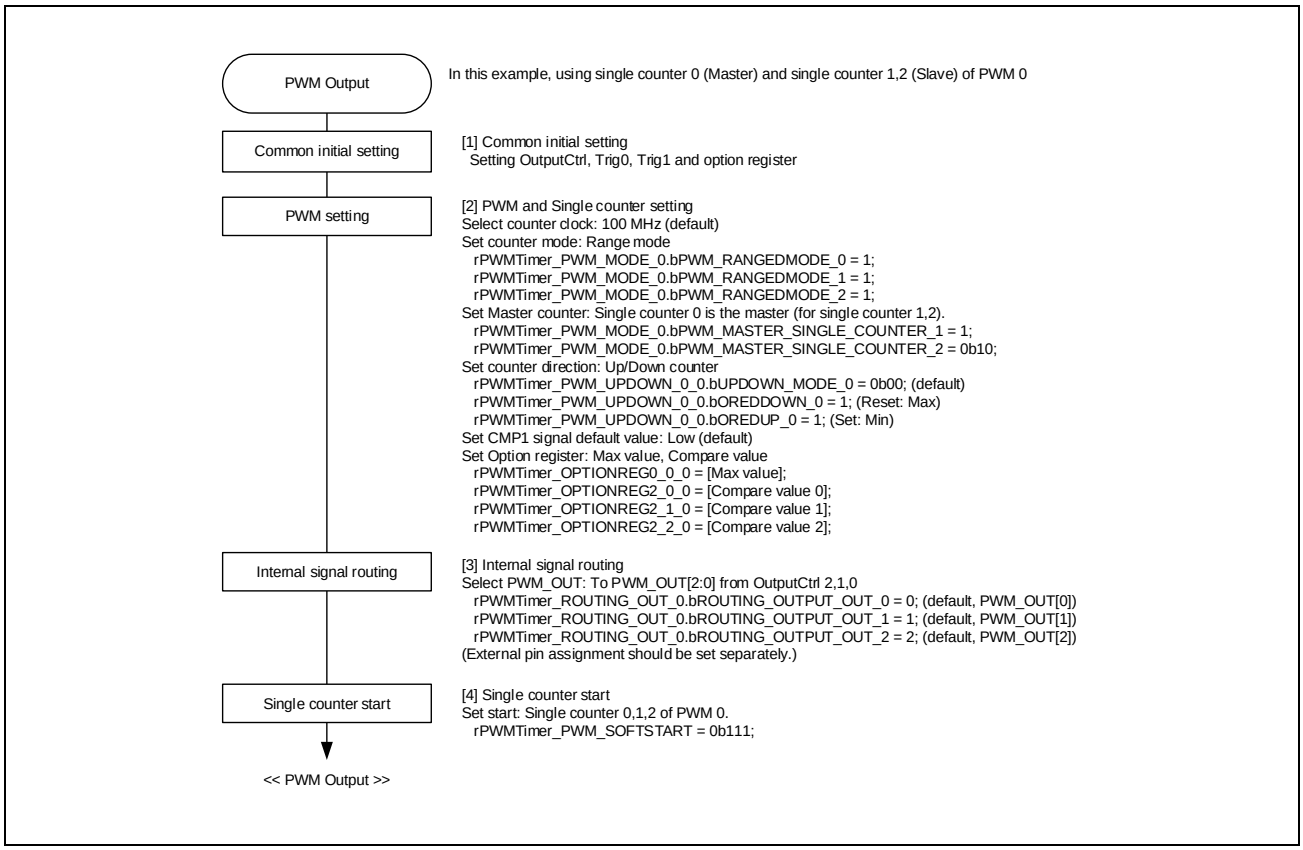


Figure 1.23 Example of Master Counter Setting

1.5.8.4 Input Capture

Using PWM_IN as the trigger input can be capture of counter values and buffer transfer.

In this example, at the rising edge of PWM_IN, the counter value is captured in option register 3 and buffer transferred to option register 2.

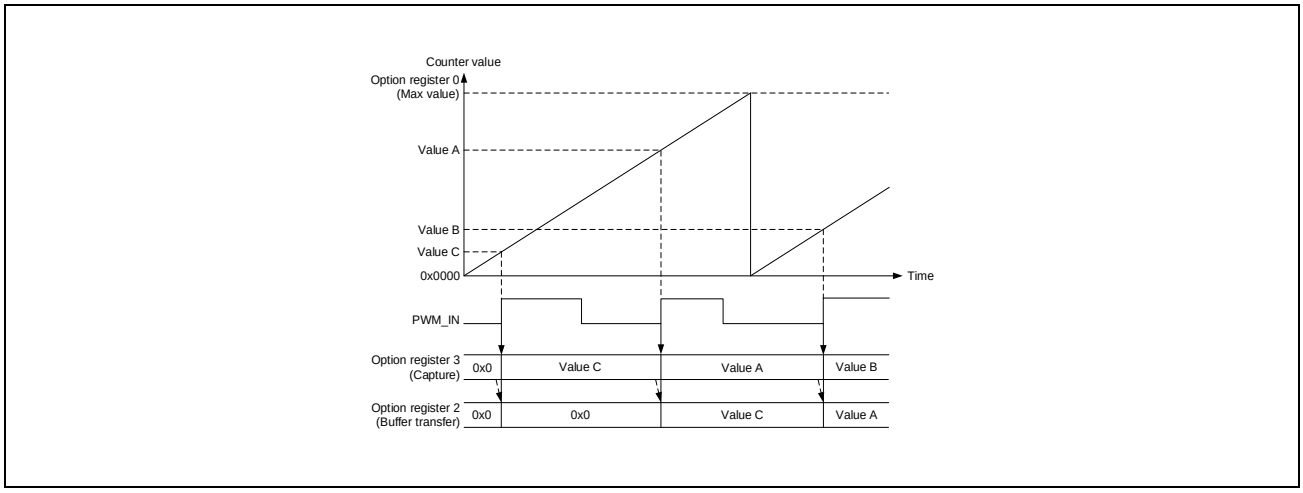


Figure 1.24 Example of Input Capture Operation

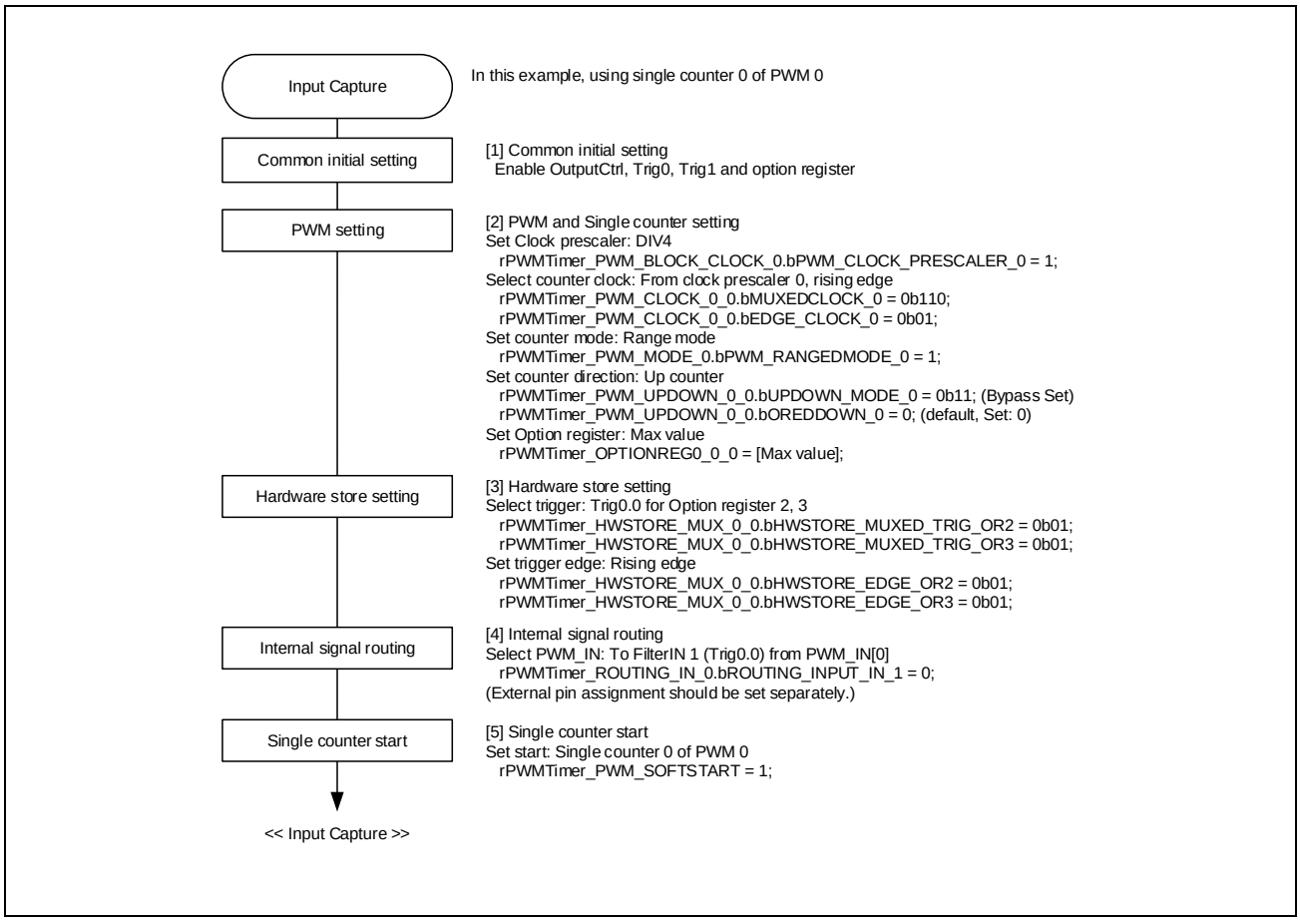


Figure 1.25 Example of Input Capture Setting

1.5.8.5 Pulse Measurement

Using PWM_IN as a clock input without edge detection enables the pulse width measurements.

In this example, same PWM_IN is assigned to the clock and trigger inputs, and the capture and buffer transfer is operating on the falling edge of the trigger. The pulse width can be measured by subtracting the value of option register 2 from the value of option register 3 at the trigger interrupt (OR3_STORE_FLAG) of option register 3.

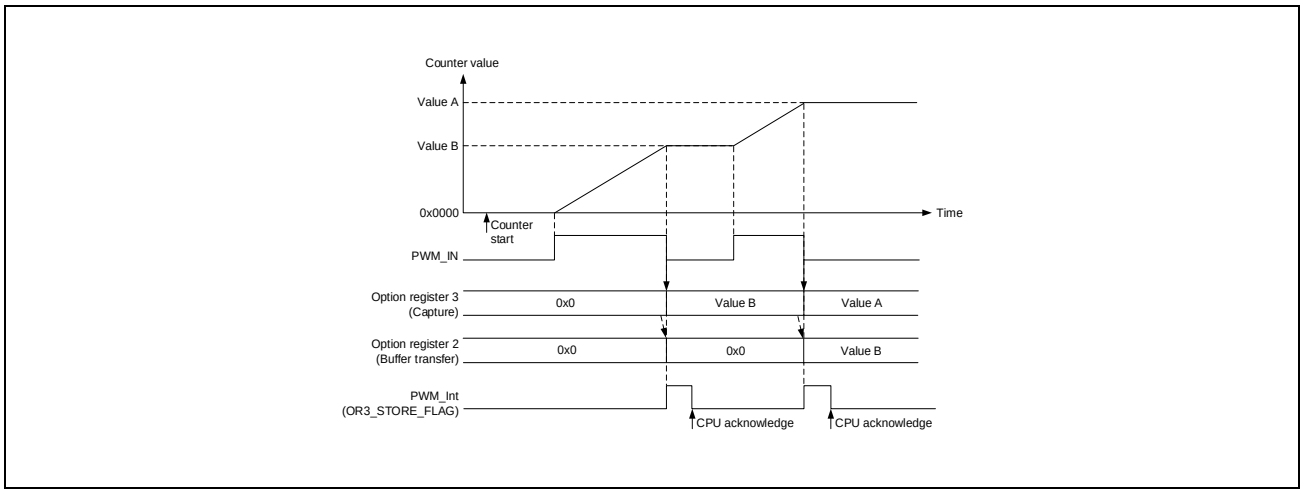


Figure 1.26 Example of Pulse Measurement Operation

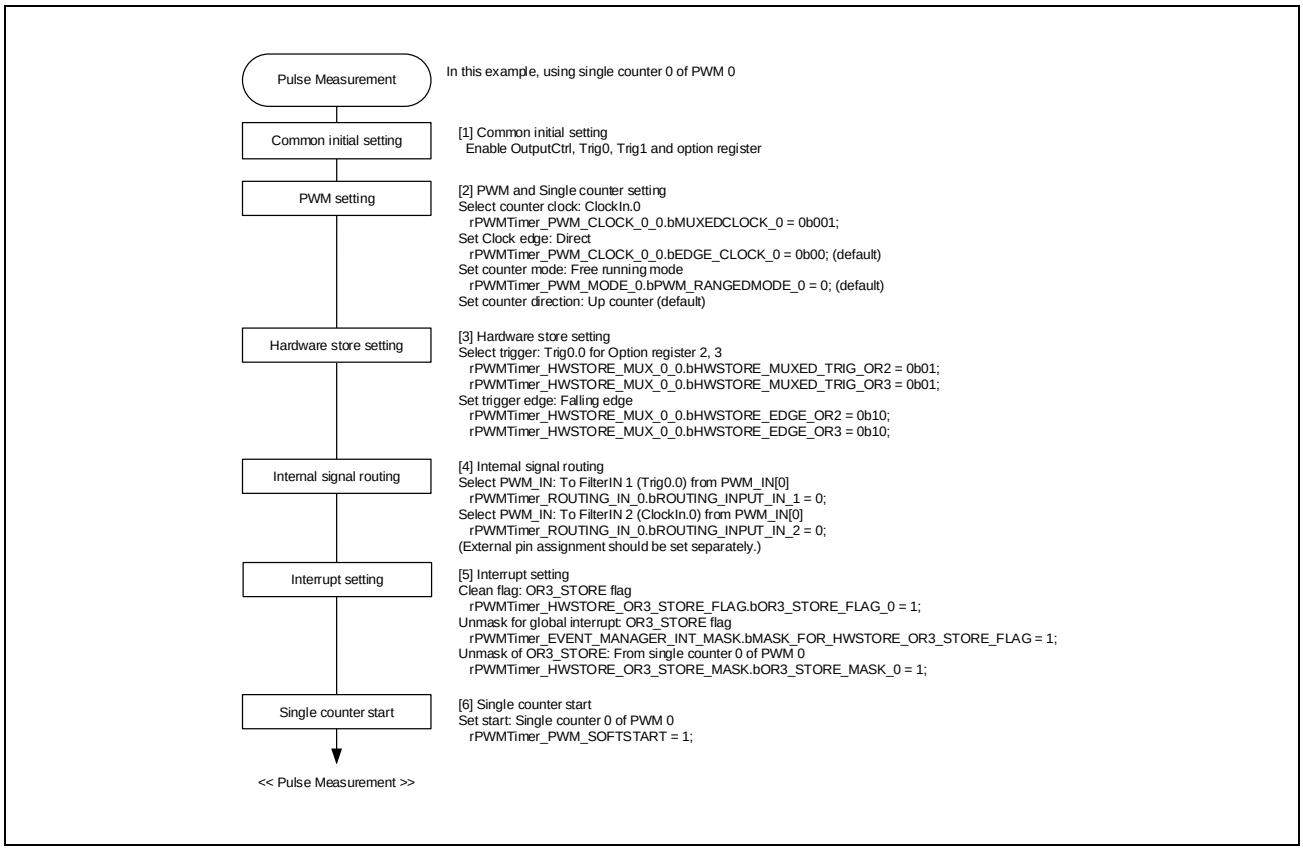


Figure 1.27 Example of Pulse Measurement Setting

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