User's Manual

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RX24U Group

User's Manual: Hardware

RENESAS 32-Bit MCU
RX Family / RX200 Series

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NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   ¾ The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   ¾ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   ¾ The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   ¾ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   ¾ The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

How to Use This Manual

1. Objective and Target Users

This manual was written to explain the hardware functions and electrical characteristics of this LSI to the target users, i.e. those who will be using this LSI in the design of application systems. Target users are expected to understand the fundamentals of electrical circuits, logic circuits, and microcomputers.
This manual is organized in the following items: an overview of the product, descriptions of the CPU, system control functions, and peripheral functions, electrical characteristics of the device, and usage notes.

When designing an application system that includes this LSI, take all points to note into account.
Points to note are given in their contexts and at the final part of each section, and in the section giving usage notes.

The list of revisions is a summary of major points of revision or addition for earlier versions. It does not cover all revised items. For details on the revised points, see the actual locations in the manual.

The following documents have been prepared for the RX24U Group. Before using any of the documents, please visit our website to verify that you have the most up-to-date available version of the document.

Document Type	Contents	Document Title	Document No.
Datasheet	Overview of hardware and electrical characteristics	RX24U Group Datasheet	R01DS0278EJ
User's Manual: Hardware	Hardware specifications (pin assignments, memory maps, peripheral specifications, electrical characteristics, and timing charts) and descriptions of operation	RX24U Group User's Manual: Hardware	This User's manual
User's Manual: Software	Detailed descriptions of the CPU and instruction set	RX Family RXv2 Instruction Set Architecture User's Manual: Software	R01US0071EJ
Application Note	Notes on Printed Circuit Board Patterns	RX Family Hardware Design Guide	R01AN1411EJ
	Examples of register initial setting	RX24U Group Initial Setting Examples	R01AN3425EJ
	Examples of applications and sample programs	—	—
Renesas Technical Update	Preliminary report on the specifications of a product, document, etc.	—	—

2. Description of Registers

Each register description includes a bit chart, illustrating the arrangement of bits, and a table of bits, describing the meanings of the bit settings. The standard format and notation for bit charts and tables are described below.

X.X.X ... Register

Address(es): xxxx xxxxh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	...[1:0]		...4	—	—	—	...0
Value after reset:	x	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b0	...0	.....	0: ..... 1: Setting prohibited (3)	R/W (1)
b3 to b1	—	Reserved (2)	These bits are read as 0. The write value should be 0.	R/W
b4	...4	.....	0: 1:	R
b6, b5	...[1:0]	.....	0 0: ..... 0 1: ..... Settings other than above are prohibited. (3)	R/(W)*1
b7	—	Reserved	The read value is undefined. Writing to this bit has no effect.	R

(1) R/W: The bit or field is readable and writable.
R/(W): The bit or field is readable and writable. However, writing to this bit or field has some limitations. For details on the limitations, see the description or notes of respective registers.
R: The bit or field is readable. Writing to this bit or field has no effect.

(2) Reserved.
Use the specified value when writing to this bit or field; otherwise, the correct operation is not guaranteed.

(3) Setting prohibited. The correct operation is not guaranteed if such a setting is performed.

3. List of Abbreviations and Acronyms

Abbreviation	Full Form
ACIA	Asynchronous Communications Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connect
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

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Contents

RX24U Group

Renesas MCUs

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80-MHz 32-bit RX MCUs, on-chip FPU, 153.6 DMIPS, power supply 5V,
12-bit ADC (equipped with 3-channel synchronous S/H circuits, double data registers, operating amplifiers, comparator) 3 units, Simultaneous sampling up to ADC 5 channels, gain setting reference GND port, CAN, 80-MHz PWM (three-phase complementary output × 2 channels + single-phase complementary output × 4 channels or three-phase complementary × 3 channels + single-phase complementary × 1 channel)

Features

■ 32-bit RXv2 CPU core

- Max. operating frequency: 80 MHz
  Capable of 153.6 DMIPS in operation at 80 MHz
- Enhanced DSP: 32-bit multiply-accumulate and 16-bit multiply-subtract instructions supported
- Built-in FPU: 32-bit single-precision floating point (compliant to IEEE754)
- Divider (fastest instruction execution takes two CPU clock cycles)
- Fast interrupt
- CISC Harvard architecture with 5-stage pipeline
- Variable-length instructions, ultra-compact code
- On-chip debugging circuit
- Memory protection unit (MPU) supported

■ Low power design and architecture

- Operation from a single 2.7-V to 5.5-V supply
- Three low power consumption modes

■ On-chip code flash memory

- 512-/384-/256-Kbyte capacities
- On-board or off-board user programming
- For instructions and operands

■ On-chip data flash memory

- 8-Kbyte (Number of erase/write cycles: 1,000,000 (typ))
- BGO (Back Ground Operation)

■ On-chip SRAM, no wait states

- 32 Kbytes of SRAM

■ Data transfer functions

- DTC: Four transfer modes

■ Reset and supply management

- Seven types of reset, including the power-on reset (POR)
- Low voltage detection (LVD) with voltage settings

■ Clock functions

- Main clock oscillator frequency: 1 to 20 MHz
- External clock input frequency: Up to 20 MHz
- PLL circuit input: 4 MHz to 12.5 MHz
- On-chip low-speed oscillators, on-chip high-speed oscillators, dedicated on-chip oscillator for the IWDT
- Clock frequency accuracy measurement circuit (CAC)

■ Independent watchdog timer

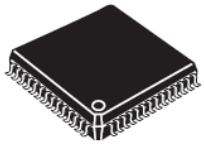
- 15-kHz on-chip oscillator produces a dedicated clock signal to drive IWDT operation.

■ Useful functions for IEC60730 compliance

- Self-diagnostic and disconnection-detection assistance functions for the A/D converter, clock frequency accuracy measurement circuit, independent watchdog timer, RAM test assistance functions using the DOC, etc.

■ MPC

- Multiple locations are selectable for I/O pins of peripheral functions



PLQP0144KA-B 20 × 20 mm, 0.5 mm pitch
PLQP0100KB-B 14 × 14 mm, 0.5 mm pitch

■ Up to 9 communications channels

- CAN (compliant with ISO11898-1), incorporating 16 message boxes (1 channel)
- SCI with many useful functions (6 channels)
  Asynchronous mode, clock synchronous mode, smart card interface mode, simplified SPI, simplified I²C, and extended serial mode.
- I²C bus interface: Transfer at up to 400 kbps, capable of SMBus operation (1 channel)
- RSPI capable of high speed connection Transfer at up to 20 Mbps (1 channel)

■ Up to 25 extended-function timers (Up to three-phase complementary PWM 3-channel simultaneous output)

- 16-bit MTU3: 80 MHz operation, input capture, output compare, three-phase complementary PWM × 2 channels output, CPU-efficient complementary PWM, phase counting mode (nine channels)
- 16-bit GPT: 80 MHz operation, input capture, output compare, PWM wave-form single-phase complementary × 4 channels output or three-phase complementary × 1 channel + single-phase complementary × 1 channel output, comparator interlocking operation (Count operation, PWM negate control) (4 channels)
- 8-bit TMRs (8 channels)
- 16-bit compare-match timers (4 channels)

■ 12-bit A/D converter: 22 channels in 3 units

- Incorporating sample-and-hold circuit 12 bits × 3 units (unit 0: 5 channels, unit 1: 5 channels, unit 2: 12 channels)
- Sampling time can be set for each channel
- Group scan priority control mode (3 levels)
- Self-diagnostic function and analog input disconnection detection assistance function (compliant to IEC60730)
- Input signal amplitude by the programmable gain amplifier (4 channels)
- Gain setting reference GND port: 2 ports
- ADC: 3-channel simultaneous sample-and-hold circuit (3 shunt method), double data register (1 shunt method), amplifiers (4 channels), comparator (4 channels)

■ 8-bit D/A converter: 2 channels

- This can be used as reference voltage for a comparator

■ Register write protection function can protect values in important registers against overwriting.

■ Up to 111 pins for general I/O ports

- 5-V tolerant, open drain, input pull-up, switching of driving capacity

■ Operating temperature range

- –40 to +85°C

■ Applications

- General industrial and consumer equipment

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications, and Table 1.2 gives a comparison of the functions of the products in different packages.
Table 1.1 is for products with the greatest number of functions, so the number of peripheral modules and channels will differ in accordance with the package type. For details, see Table 1.2, Comparison of Functions for Different Packages.

Table 1.1 Outline of Specifications (1/4)

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 80 MHz • 32-bit RX CPU (RX v2) • Minimum instruction execution time: One instruction per clock cycle • Address space: 4-Gbyte linear • Register set General purpose: Sixteen 32-bit registers Control: Ten 32-bit registers Accumulator: Two 72-bit registers • Basic instructions: 75 Variable-length instruction format • Floating-point instructions: 11 • DSP instructions: 23 • Addressing modes: 11 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32-bit × 32-bit → 64-bit • On-chip divider: 32-bit ÷ 32-bit → 32-bit • Barrel shifter: 32 bits • ROM cache 2 Kbytes (disabled by default)
	FPU	• Single precision (32-bit) floating point • Data types and floating-point exceptions in conformance with the IEEE754 standard
Memory	ROM	• Capacity: 256 K/384 K/512 Kbytes • Up to 32 MHz, no-wait memory access 32 to 80 MHz: wait states • Off-board programming • Programming/erasing method: Serial programming (asynchronous serial communication), self-programming
	RAM	• Capacity: 32 Kbytes • 80 MHz, no-wait memory access
	E2 DataFlash	• Capacity: 8 Kbytes • Number of erase/write cycles: 1,000,000 (typ)
MCU operating mode		Single-chip mode
Clock	Clock generation circuit	• Main clock oscillator, low- and high-speed on-chip oscillators, PLL frequency synthesizer, and IWDT-dedicated on-chip oscillator • Independent settings for the system clock (ICLK), peripheral module clock (PCLK), and FlashIF clock (FCLK) The CPU and system sections such as other bus masters run in synchronization with the system clock (ICLK): 80 MHz (at max.) The MTU3, GPT, and SCI11 modules run in synchronization with the PCLKA: 80 MHz (at max.) The peripheral modules other than MTU3, GPT, and SCI11 run in synchronization with the PCLKB: 40 MHz (at max.) ADCLK operated in S12AD runs in synchronization with the PCLKD: 40 MHz (at max.) The flash memory peripheral circuit runs in synchronization with the FCLK: 32 MHz (at max.)
Resets		RES# pin reset, power-on reset, voltage monitoring reset, independent watchdog timer reset, and software reset
Voltage detection	Voltage detection circuit (LVDAb)	• When the voltage on VCC falls below the voltage detection level, an internal reset or internal interrupt is generated. Voltage detection circuit 0 is capable of selecting the detection voltage from 3 levels Voltage detection circuit 1 is capable of selecting the detection voltage from 9 levels Voltage detection circuit 2 is capable of selecting the detection voltage from 4 levels
Low power consumption	Low power consumption functions	• Module stop function • Three low power consumption modes Sleep mode, deep sleep mode, and software standby mode
	Function for lower operating power consumption	• Operating power control modes High-speed operating mode and middle-speed operating mode

Table 1.1 Outline of Specifications (2/4)

Classification	Module/Function	Description
Interrupt	Interrupt controller (ICUb)	• Interrupt vectors: 175 • External interrupts: 9 (NMI, IRQ0 to IRQ7 pins) • Non-maskable interrupts: 5 (NMI pin, oscillation stop detection interrupt, voltage monitoring 1 interrupt, voltage monitoring 2 interrupt, and IWDT interrupt) • 16 levels specifiable for the order of priority
DMA	Data transfer controller (DTCa)	• Transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Interrupts • Chain transfer function
I/O ports	General I/O ports	144-/100-pin • I/O: 110/79 • Input: 1/1 • Pull-up resistors: 110/79 • Open-drain outputs: 90/61 • 5-V tolerance: 2/2
Multi-function pin controller (MPC)		Capable of selecting the input/output function from multiple pins
Timers	Multi-function timer pulse unit 3 (MTU3d)	• 9 units (16 bits × 9 channels) • Provides up to 28 pulse-input/output lines and three pulse-input lines • Select from among fourteen counter-input clock signals for each channel (PCLK/1, PCLK/2, PCLK/4, PCLK/8, PCLK/16, PCLK/32, PCLK/64, PCLK/256, PCLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD, MTIOC1A) other than channel 1/3/4/6/7, for which only eleven signals are available, channel 2 for 12, channel 5 for 10 • 43 general registers including 28 output compare/input capture registers • Counter clear operation (with compare match- or input capture-sourced simultaneous counter clear capability) • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous register input/output by synchronous counter operation • Buffer operation • Cascaded operation • 45 interrupt sources • Automatic transfer of register data • Pulse output modes: Toggle/PWM/complementary PWM/reset-synchronized PWM • Complementary PWM output mode 3-phase non-overlapping waveform output for inverter control Automatic dead time setting Adjustable PWM duty cycle: from 0 to 100% A/D conversion request delaying function Interrupt at crest/trough can be skipped Double buffer function • Reset-synchronized PWM mode Outputs three phases each for positive and negative PWM waveforms in user-specified duty cycle • Phase counting modes: 16-bit mode (channel 1 and 2)/32-bit mode (channel 1 and 2) • Dead time compensation counter function • A/D converter start trigger can be generated • A/D converter start triggers can be skipped • Signals from the input capture and external counter clock pins are input via a digital filter
	Port output enable 3 (POE3A)	• High impedance control of the MTU3/GPT waveform output pins and switching them to operate as general I/O ports • Startup by input from signal sources on 6 pins (POE0#, POE4#, POE8#, POE10#, POE11#, and POE12#) • Startup by detection of short-circuited outputs (detection of simultaneous PMW output at the active level) • Startup on detection of oscillation stopping or by a comparator, or under software control • Control of the addition of pins for output control is programmable

Table 1.1 Outline of Specifications (3/4)

Classification	Module/Function	Description
Timers	General PWM timer (GPTB)	• 16 bits × 4 channels • Two channels can be cascaded and used as a 32-bit timer • Counting up or down (saw waves), or counting up and down (triangle waves) is selectable for each counter. • A count clock is selectable from 13 types (PCLK/1, PCLK/2, PCLK/4, PCLK/8, PCLK/16,PCLK/32, PCLK/64, PCLK/256, PCLK/1024, GTECLKA, GTECLKB, GTECLKC, and GTECLKD) for each channel. • Two I/O pins per channel • Two output compare/input capture registers per channel • For the two output compare/input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at crests or troughs, enabling the generation of laterally asymmetric PWM waveforms. • Registers for setting up frame cycles in each channel (with capability for generating interrupts at overflow or underflow) • Synchronous operation of the several counters • Modes of synchronous operation (synchronized or displaced by a desired time to obtain relative phase shifts) • Generation of dead times in PWM operation • Through combination of three counters, generation of three-phased PWM waveforms incorporating dead times • Starting, clearing, and stopping counters in response to external or internal triggers • Internal trigger sources: output of the comparator detection, MTU3 count start, software, compare match • Noise filter function for signals on the Input capture, external trigger pins, and the external count clock pins • A/D converter start triggers can be generated
	Compare match timer (CMT)	• (16 bits × 2 channels) × 2 units • Select from among four clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Independent watchdog timer (IWDTa)	• 14 bits × 1 channel • Count clock: Dedicated low-speed on-chip oscillator for the IWDT-dedicated on-chip oscillator Frequency divided by 1, 16, 32, 64, 128, or 256
	8-bit timer (TMR)	• (8 bits × 2 channels) × 4 units • Seven internal clocks (PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, and PCLK/8192) and an external clock can be selected • Pulse output and PWM output with any duty cycle are available • Two channels can be cascaded and used as a 16-bit timer • Generates A/D conversion start trigger • Generates baud rate clock for the SCI5 and SCI6
Communication functions	Serial communications interfaces (SCIg)	• 6 channels (channel 1, 5, 6, 8, 9 and 11: SCIg) • SCIg Serial communications: asynchronous, clock synchronous, and smart-card interface On-chip baud rate generator allows selection of the desired bit rate Selection of LSB-first or MSB first transfer Average transfer rate clocks for SCI5 and SCI6 can be input from TMR timers Simple I^2C Simple SPI Multi-processor function Detection of the start bit: Level or edge is selectable. 9-bit transfer mode Bit rate modulation
	I^2C bus interface (RIICa)	• 1 channel • Communications formats: I^2C bus format/SMBus format • Master mode or slave mode selectable • Supports fast mode
	CAN module (RSCAN)	• Single channel • ISO11898-1 specifications compliant (standard and extended frames) • 16 message boxes
	Serial peripheral interface (RSPIb)	• 1 channel • Transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) • Capable of handling serial transfer as a master or slave • Data formats Choice of LSB-first or MSB-first transfer The number of bits in each transfer can be changed to 8 to 16, 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Double buffers for both transmission and reception

Table 1.1 Outline of Specifications (4/4)

Classification	Module/Function	Description
12-bit A/D converter (S12ADF)		• 12 bits (5 channels × 2 units/12 channels × 1 unit) • 12-bit resolution • Minimum conversion time: 1.0 µs per channel when the ADCLK is operating at 40 MHz • Operating modes Scan mode (single scan mode, continuous scan mode, and 3 group scan mode) Group A priority control (only for 3 group scan mode) • Sampling variable Sampling time can be set up for each channel • Self-diagnostic function • Double trigger mode (A/D conversion data duplicated) • Assist on analog input disconnection detection • A/D conversion start conditions A software trigger, a trigger from a timer (MTU3, GPT, TMR), or an external trigger signal • Sample-and-hold function Sample-and-hold circuit included (3 channels for unit 1) • Amplification of input signals by a programmable gain amplifier (1 channel for unit 0, 3 channels for unit 1) Amplification rate: 2.0 times, 2.5 times, 3.077 times, 3.636 times, 4.0 times, 4.444 times, 5.0 times, 6.667 times, 8.0 times, 10.0 times, 13.333 times (total of 11 steps)
Comparator C (CMPC)		• 4 channels • Function to compare the reference voltage and the analog input voltage • Reference voltage: DA0 or DA1 output is selectable • Analog input voltage is selectable from 4 inputs
8-bit D/A converter (DAa)		• 2 channels • 8-bit resolution • Output voltage: 0 V to AVCC2
Safety	Memory protection unit (MPU)	• Protection area: Eight areas (max.) can be specified in the range from 0000 0000h to FFFF FFFFh. • Minimum protection unit: 16 bytes • Reading from, writing to, and enabling the execution access can be specified for each area. • An address exception occurs when the detected access is not in the permitted area.
	Register write protection function	• Protects important registers from being overwritten for in case a program runs out of control.
	CRC calculator (CRC)	• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.
	Main clock oscillation stop function	• Main clock oscillation stop detection: Available
	Clock frequency accuracy measurement circuit (CAC)	• Monitors the clock output from the main clock oscillator, high-speed on-chip oscillator, low-speed on-chip oscillator, the PLL frequency synthesizer, IWDT-dedicated on-chip oscillator, and PCLKB.
	Data operation circuit (DOC)	The function to compare, add, or subtract 16-bit data
Power supply voltages/Operating frequencies		VCC = 2.7 to 5.5 V: 80 MHz
Packages		144-pin LFQFP 0.5 mm pitch 100-pin LFQFP 0.5 mm pitch
On-chip debugging system		E1 emulator (FINE interface)

Table 1.2 Comparison of Functions for Different Packages

Module/Functions		RX24U Group	
		144 Pins	100 Pins
Memory	ROM	512 Kbytes	
	RAM	32 Kbytes	
	E2 Data Flash	8 Kbytes	
Interrupts	External interrupts	NMI, IRQ0 to IRQ7	
DTC	Data transfer controller (DTCa)	Available	
Timers	Multi-function timer pulse unit 3 (MTU3d)	9 channels	
	General PWM timer (GPTB)	4 channels	
	Port output enable 3 (POE3A)	POE0#, POE4#, POE8#, POE10#, POE11#, POE12#	
	8-bit timer (TMR)	2 channels × 4 units	
	Compare match timer (CMT)	2 channels × 2 units	
	Independent watchdog timer (IWDTa)	Available	
Communication functions	Serial communications interfaces (SCIg) [including simple I^2C and simple SPI]	6 channels (SCI1, 5, 6, 8, 9, 11)	4 channels (SCI1, 5, 6, 11)
	I^2C bus interface (RIICa)	1 channel	
	Serial peripheral interface (RSPIb)	1 channel	
	CAN module (RSCAN)	1 channel	
12-bit A/D converter (including high-precision channels) (S12ADF)		5 channels × 2 units, 12 channels × 1 unit (4 channels × 2 units, 12 channels × 1 unit)	5 channels × 2 units, 10 channels × 1 unit (4 channels × 2 units, 10 channels × 1 unit)
	3 channels simultaneous sampling function	3 channels/unit 1	
	Programmable gain amplifier	1 channel/unit 0, 3 channels/unit 1	
Comparator C (CMPC)		4 channels	
D/A converter (DAa)		2 channels	
CRC calculator (CRC)		Available	
Packages		144-pin LFQFP	100-pin LFQFP

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no., memory capacity, and package type.

Table 1.3 List of Products

Group	Part No.	Part No. (for Orders)	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency (max.)	Operating Temperature
RX24U	R5F524UEADFB	R5F524UEADFB#30	PLQP0144KA-B	512 Kbytes	32 Kbytes	8 Kbytes	80 MHz	–40 to + 85°C
	R5F524UEADFP	R5F524UEADFP#30	PLQP0100KB-B					
	R5F524UCADFB	R5F524UCADFB#30	PLQP0144KA-B	384 Kbytes				
	R5F524UCADFP	R5F524UCADFP#30	PLQP0100KB-B					
	R5F524UBADFB	R5F524UBADFB#30	PLQP0144KA-B	256 Kbytes				
	R5F524UBADFP	R5F524UBADFP#30	PLQP0100KB-B					

Note: The part numbers for orders above are used for products in mass production or under development when this manual is issued. Refer to the Renesas Electronics Corporation website for the latest part numbers.

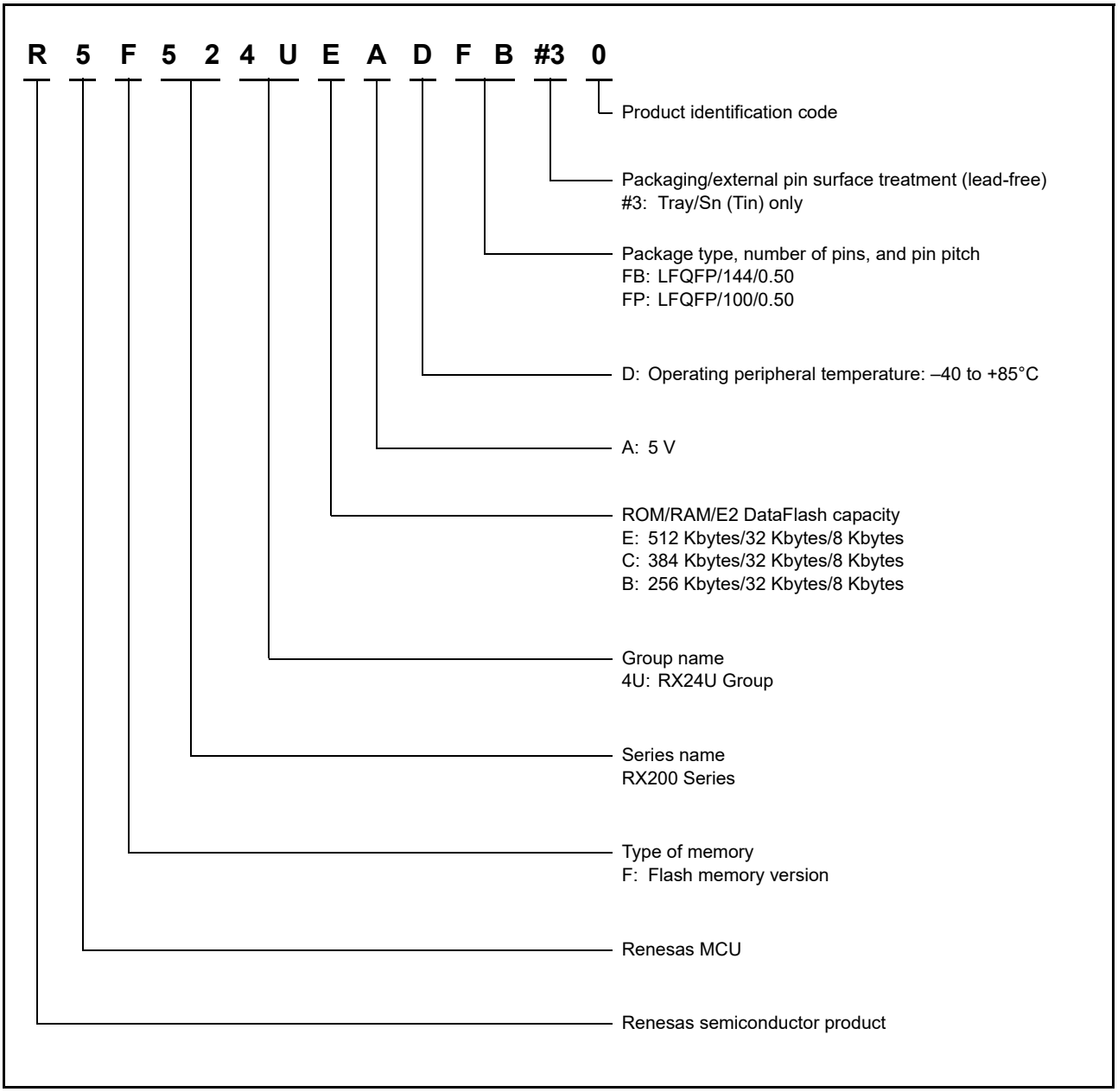


Figure 1.1 How to Read the Product Part Number

1.3 Block Diagram

Figure 1.2 shows a block diagram.

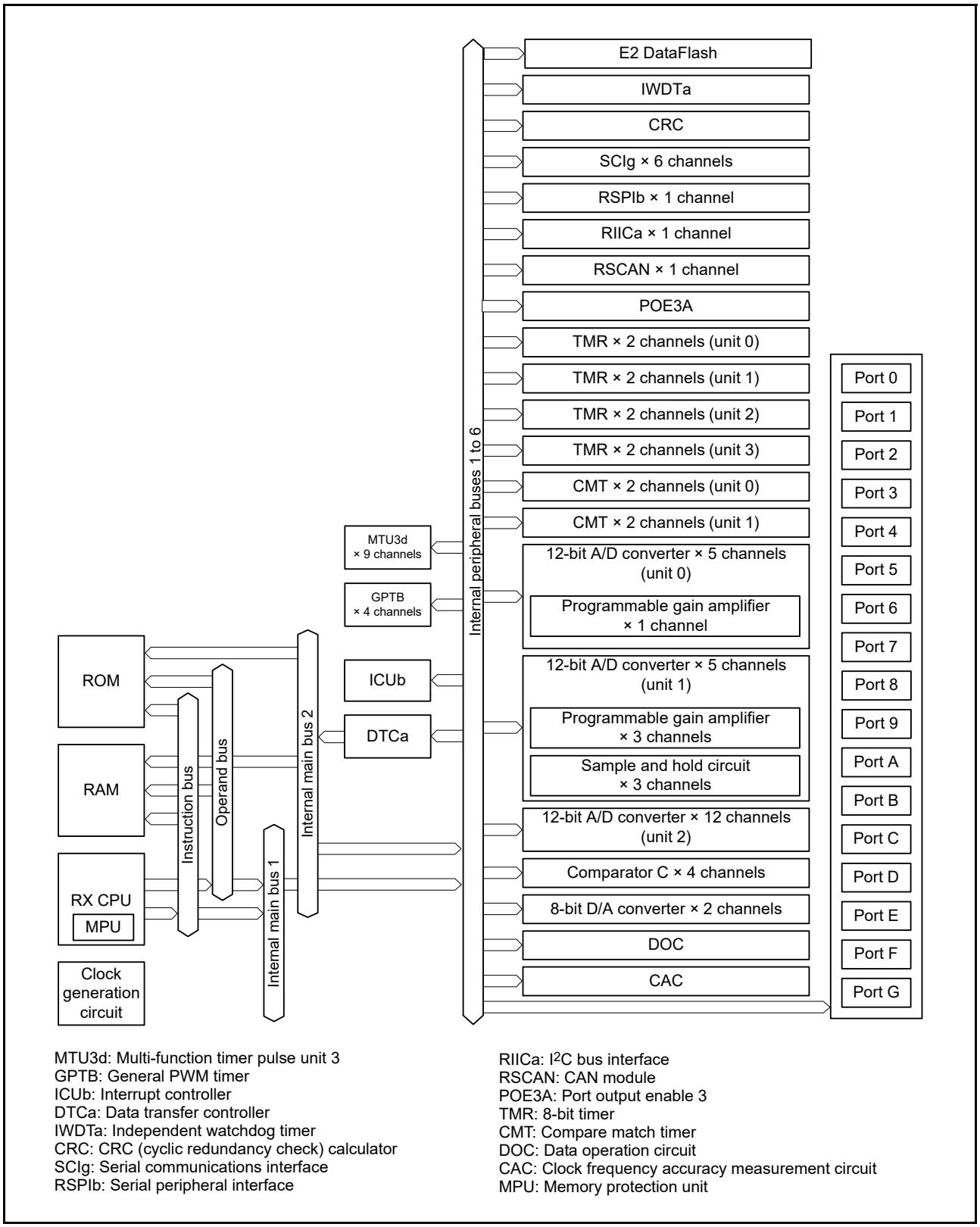


Figure 1.2 Block Diagram

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1/4)

Classifications	Pin Name	I/O	Description
Power supply	VCC	—	Power supply pin. Connect it to the system power supply.
	VCL	—	Connect this pin to the VSS pin via the 4.7 μF smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	—	Ground pin. Connect it to the system power supply (0 V).
Clock	XTAL	Output	Pins for connecting a crystal. An external clock can be input through the EXTAL pin.
	EXTAL	Input	
Operating mode control	MD	Input	Pin for setting the operating mode. The signal levels on this pin must not be changed during operation.
System control	RES#	Input	Reset pin. This MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Input pin for the clock frequency accuracy measurement circuit.
On-chip emulator	FINED	I/O	FINE interface pin.
Interrupts	NMI	Input	Non-maskable interrupt request pin.
	IRQ0 to IRQ7	Input	Interrupt request pins.
Multi-function timer pulse unit 3 (MTU3d)	MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins.
	MTIOC0A#, MTIOC0B#, MTIOC0C#, MTIOC0D#	I/O	The TGRA0 to TGRD0 input capture inverted input/output compare inverted output/PWM inverted output pins.
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins.
	MTIOC1A#, MTIOC1B#	I/O	The TGRA1 and TGRB1 input capture inverted input/output compare inverted output/PWM inverted output pins.
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins.
	MTIOC2A#, MTIOC2B#	I/O	The TGRA2 and TGRB2 input capture inverted input/output compare inverted output/PWM inverted output pins.
	MTIOC3A, MTIOC3B, MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins.
	MTIOC3A#, MTIOC3B#, MTIOC3C#, MTIOC3D#	I/O	The TGRA3 to TGRD3 input capture inverted input/output compare inverted output/PWM inverted output pins.
	MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins.
	MTIOC4A#, MTIOC4B#, MTIOC4C#, MTIOC4D#	I/O	The TGRA4 to TGRD4 input capture inverted input/output compare inverted output/PWM inverted output pins.
	MTIC5U, MTIC5V, MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/external pulse input pins.
	MTIC5U#, MTIC5V#, MTIC5W#	Input	The TGRU5, TGRV5, and TGRW5 input capture inverted input/external pulse inverted input pins.
	MTIOC6A, MTIOC6B, MTIOC6C, MTIOC6D	I/O	The TGRA6 to TGRD6 input capture input/output compare output/PWM output pins.
	MTIOC6A#, MTIOC6B#, MTIOC6C#, MTIOC6D#	I/O	The TGRA6 to TGRD6 input capture inverted input/output compare inverted output/PWM inverted output pins.
	MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D	I/O	The TGRA7 to TGRD7 input capture input/output compare output/PWM output pins.
	MTIOC7A#, MTIOC7B#, MTIOC7C#, MTIOC7D#	I/O	The TGRA7 to TGRD7 input capture inverted input/output compare inverted output/PWM inverted output pins.
	MTIOC9A, MTIOC9B, MTIOC9C, MTIOC9D	I/O	The TGRA9 to TGRD9 input capture input/output compare output/PWM output pins.

Table 1.4 Pin Functions (2/4)

Classifications	Pin Name	I/O	Description
Multi-function timer pulse unit 3 (MTU3d)	MTIOC9A#, MTIOC9B#, MTIOC9C#, MTIOC9D#	I/O	The TGRA9 to TGRD9 input capture inverted input/output compare inverted output/PWM inverted output pins.
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	Input pins for the external clock.
	MTCLKA#, MTCLKB#, MTCLKC#, MTCLKD#	Input	Inverted input pins for the external clock.
	ADSM0, ADSM1	Output	A/D trigger output pins.
General PWM timer (GPTB)	GTIOC0A, GTIOC0B	I/O	The GPT0.GTGRA and GPT0.GTGRB input capture input/output compare output/PWM output pins
	GTIOC0A#, GTIOC0B#	I/O	The GPT0.GTGRA and GPT0.GTGRB input capture inverted input/output compare inverted output/PWM inverted output pins
	GTIOC1A, GTIOC1B	I/O	The GPT1.GTGRA and GPT1.GTGRB input capture input/output compare output/PWM output pins
	GTIOC1A#, GTIOC1B#	I/O	The GPT1.GTGRA and GPT1.GTGRB input capture inverted input/output compare inverted output/PWM inverted output pins
	GTIOC2A, GTIOC2B	I/O	The GPT2.GTGRA and GPT2.GTGRB input capture input/output compare output/PWM output pins
	GTIOC2A#, GTIOC2B#	I/O	The GPT2.GTGRA and GPT2.GTGRB input capture inverted input/output compare inverted output/PWM inverted output pins
	GTIOC3A, GTIOC3B	I/O	The GPT3.GTGRA and GPT3.GTGRB input capture input/output compare output/PWM output pins
	GTIOC3A#, GTIOC3B#	I/O	The GPT3.GTGRA and GPT3.GTGRB input capture inverted input/output compare inverted output/PWM inverted output pins
	GTETRG	Input	External trigger input pin for GPT0 to GPT3
	GTECLKA, GTECLKB, GTECLKC, GTECLKD	Input	Input pins A to D for the external clock
	GTADSM0, GTADSM1	Output	A/D conversion start request monitoring output pins
8-bit timer (TMR)	TMO0 to TMO7	Output	Compare match output pins.
	TMCI0 to TMCI7	Input	Input pins for the external clock to be input to the counter.
	TMRI0 to TMRI7	Input	Counter reset input pins.
Port output enable 3 (POE3A)	POE0#, POE4#, POE8#, POE10#, POE11#, POE12#	Input	Input pins for request signals to switch the MTU and GPT pins between the high impedance state or operation as general I/O port pins
Serial communications interface (SCIg)	• Asynchronous mode/clock synchronous mode		
	SCK1, SCK5, SCK6, SCK8, SCK9, SCK11	I/O	Input/output pins for the clock.
	RXD1, RXD5, RXD6, RXD8, RXD9, RXD11	Input	Input pins for received data.
	TXD1, TXD5, TXD6, TXD8, TXD9, TXD11	Output	Output pins for transmitted data.
	CTS1#, CTS5#, CTS6#, CTS8#, CTS9#, CTS11#	Input	Input pins for controlling the start of transmission and reception.
	RTS1#, RTS5#, RTS6#, RTS8#, RTS9#, RTS11#	Output	Output pins for controlling the start of transmission and reception.
	• Simple I^2C mode		
	SSCL1, SSCL5, SSCL6, SSCL8, SSCL9, SSCL11	I/O	Input/output pins for the I^2C clock.
	SSDA1, SSDA5, SSDA6, SSDA8, SSDA9, SSDA11	I/O	Input/output pins for the I^2C data.
	• Simple SPI mode		
	SCK1, SCK5, SCK6, SCK8, SCK9, SCK11	I/O	Input/output pins for the clock.

Table 1.4 Pin Functions (3/4)

Classifications	Pin Name	I/O	Description
Serial communications interface (SCIg)	SMISO1, SMISO5, SMISO6, SMISO8, SMISO9, SMISO11	I/O	Input/output pins for slave transmit data.
	SMOSI1, SMOSI5, SMOSI6, SMOSI8, SMOSI9, SMOSI11	I/O	Input/output pins for master transmit data.
	SS1#, SS5#, SS6#, SS8#, SS9#, SS11#	Input	Chip-select input pins.
I2C bus interface (RIICa)	SCL0	I/O	Input/output pin for I2C bus interface clocks. Bus can be directly driven by the N-channel open drain output.
	SDA0	I/O	Input/output pin for I2C bus interface data. Bus can be directly driven by the N-channel open drain output.
Serial peripheral interface (RSPIb)	RSPCKA	I/O	Input/output pin for the RSPI clock.
	MOSIA	I/O	Input/output pin for transmitting data from the RSPI master.
	MISOA	I/O	Input/output pin for transmitting data from the RSPI slave.
	SSLA0	I/O	Input/output pin to select the slave for the RSPI.
	SSLA1 to SSLA3	Output	Output pins to select the slave for the RSPI.
CAN module (RSCAN)	CRXD0	Input	Input pin
	CTXD0	Output	Output pin
12-bit A/D converter (S12ADF)	AN000 to AN003, AN016, AN100 to AN103, AN116, AN200 to AN211	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADST0, ADST1, ADST2	Output	Output pins for A/D conversion status.
	ADTRG0#, ADTRG1#, ADTRG2#	Input	Input pins for the external trigger signals that start the A/D conversion.
	PGAVSS0	Input	AN000 PGA gain setting resistor reference ground pin: Connect to AVSS0 when the PGA is not used.
	PGAVSS1	Input	AN100 to 102 PGA gain setting resistor reference ground pin: Connect to AVSS1 when the PGA is not used.
8-bit D/A converter (DAa)	DA0, DA1	Output	Output pins for the analog signals to be processed by the D/A converter
Comparator C (CMPC)	COMP0 to COMP3	Output	Comparator detection result output pins.
	CMPC00 to CMPC03	Input	Analog input pins for CMPC0
	CMPC10 to CMPC13	Input	Analog input pins for CMPC1
	CMPC20 to CMPC23	Input	Analog input pins for CMPC2
	CMPC30 to CMPC33	Input	Analog input pins for CMPC3
Analog power supply	AVCC0	—	Analog power supply and reference power supply pin for 12-bit A/D converter unit 0. Connect the AVCC0 pin to AVCC1, or AVCC2 when 12-bit A/D converter unit 0 is not used.
	AVSS0	—	Analog ground and reference ground pin for 12-bit A/D converter unit 0. Connect the AVSS0 pin to AVSS1 or AVSS2 when 12-bit A/D converter unit 0 is not used.
	AVCC1	—	Analog power supply and reference power supply pin for 12-bit A/D converter unit 1. Connect the AVCC1 pin to AVCC0, or AVCC2 when 12-bit A/D converter unit 1 is not used.
	AVSS1	—	Analog ground and reference ground pin for 12-bit A/D converter unit 1. Connect the AVSS1 pin to AVSS0 or AVSS2 when 12-bit A/D converter unit 1 is not used.

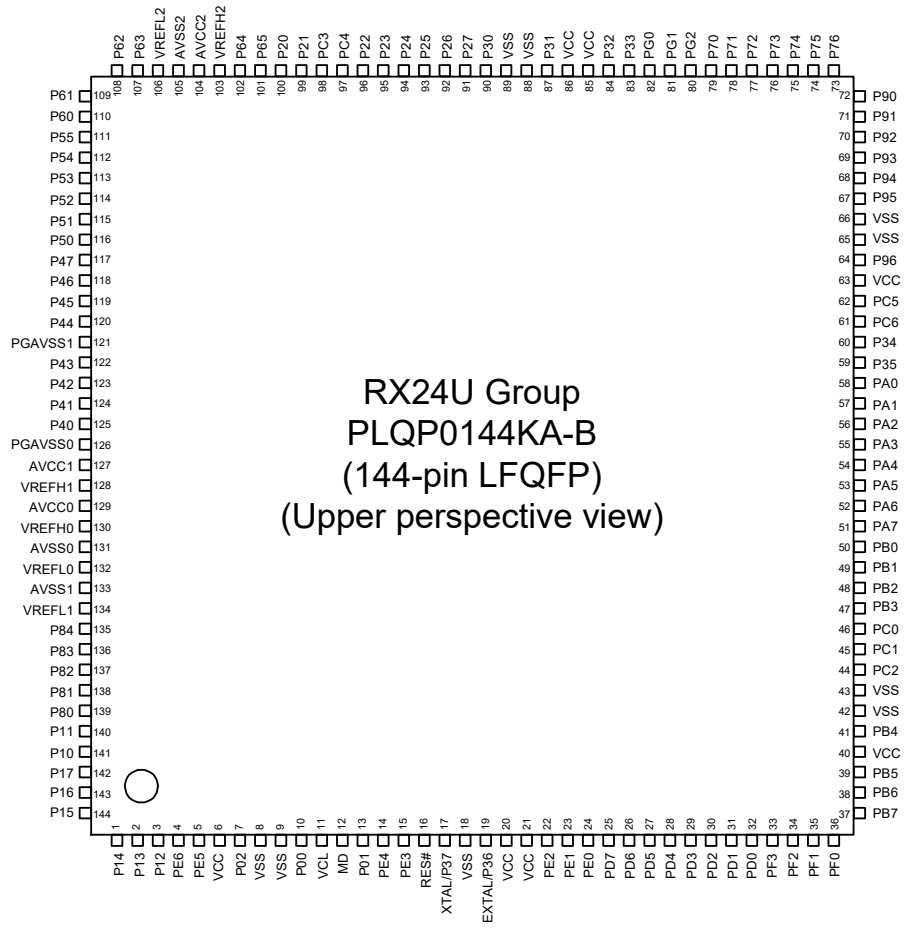
Table 1.4 Pin Functions (4/4)

Classifications	Pin Name	I/O	Description
Analog power supply	AVCC2	—	Analog power supply and reference power supply pin for 12-bit A/D converter unit 2. Analog power supply pin for D/A converter. Analog power supply pin for comparator C. Connect the AVCC2 pin to AVCC0, or AVCC1 when these modules are not used.
	AVSS2	—	Analog ground and reference ground pin for 12-bit A/D converter unit 2. Analog ground pin for D/A converter. Analog ground pin for comparator C. Connect the AVSS2 pin to AVSS0 or AVSS1 when these modules are not used.
	VREFH0	—	Reference voltage supply pin for the 12-bit A/D converter unit 0.: Connect to AVCC0.
	VREFL0	—	Reference ground pin for the 12-bit A/D converter unit 0.: Connect to AVSS0.
	VREFH1	—	Reference voltage supply pin for the 12-bit A/D converter unit 1. Connect to AVCC1.
	VREFL1	—	Reference ground pin for the 12-bit A/D converter unit 1. Connect to AVSS1.
	VREFH2	—	Reference voltage supply pin for the 12-bit A/D converter unit 2.: Connect to AVCC2.
	VREFL2	—	Reference ground pin for the 12-bit A/D converter unit 2.: Connect to AVSS2.
I/O ports	P00 to P02	I/O	3-bit input/output pins.
	P10 to P17	I/O	8-bit input/output pins.
	P20 to P27	I/O	8-bit input/output pins.
	P30 to P37	I/O	8-bit input/output pins.
	P40 to P47	I/O	8-bit input/output pins.
	P50 to P55	I/O	6-bit input/output pins.
	P60 to P65	I/O	6-bit input/output pins.
	P70 to P76	I/O	7-bit input/output pins.
	P80 to P84	I/O	5-bit input/output pins.
	P90 to P96	I/O	7-bit input/output pins.
	PA0 to PA7	I/O	8-bit input/output pins.
	PB0 to PB7	I/O	8-bit input/output pins.
	PC0 to PC6	I/O	7-bit input/output pins.
	PD0 to PD7	I/O	8-bit input/output pins.
	PE0 to PE6	I/O	7-bit input/output pins (PE2: input).
	PF0 to PF3	I/O	4-bit input/output pins.
	PG0 to PG2	I/O	3-bit input/output pins.

Note: When the A/D converter, D/A converter, and comparator C are not used, connect the AVCC0, AVCC1, AVCC2, VREFH0, VREFH1 and VREFH2 pins to VCC, and connect the AVSS0, AVSS1, AVSS2, VREFL0, VREFL1 and VREFL2 pins to VSS, respectively.

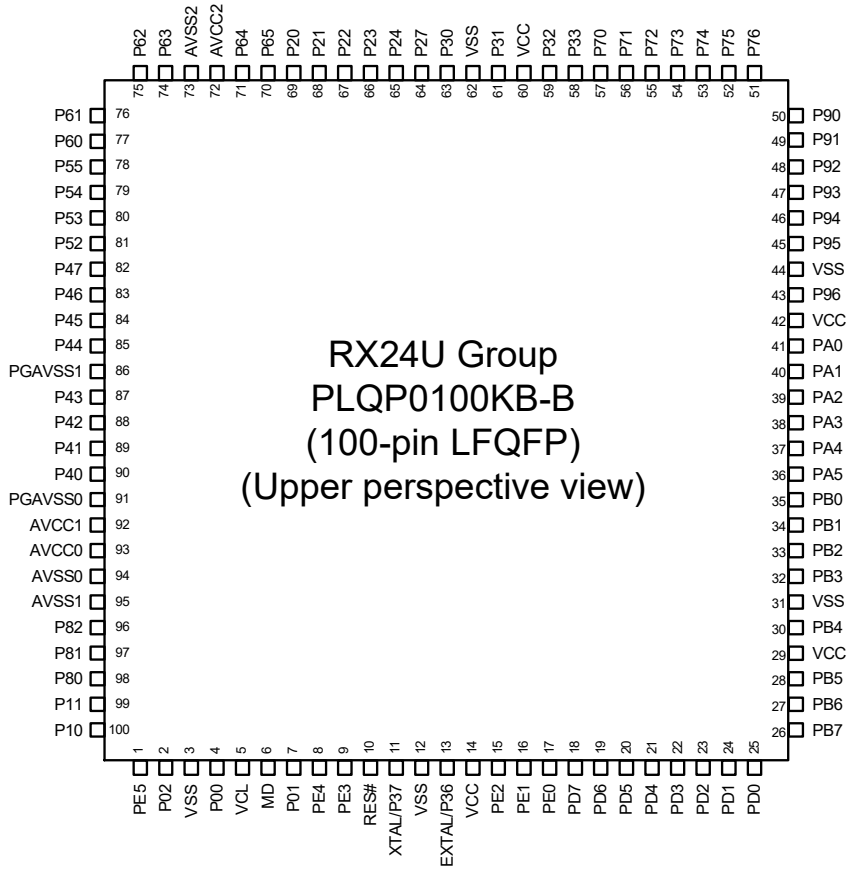
1.5 Pin Assignments

Figure 1.3 and Figure 1.4 show the pin assignments. Table 1.5 and Table 1.6 show the lists of pins and pin functions.



Note: This figure indicates the power supply pins and I/O port pins.
For the pin configuration, see the table “List of Pins and Pin Functions (144-Pin LFQFP)”.

Figure 1.3 Pin Assignments of the 144-Pin LFQFP



Note: This figure indicates the power supply pins and I/O port pins.
For the pin configuration, see the table “List of Pins and Pin Functions (100-Pin LFQFP)”.

Figure 1.4 Pin Assignments of the 100-Pin LFQFP

Table 1.5 List of Pins and Pin Functions (144-Pin LFQFP) (1/4)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (TMR, MTU3, POE, CAC, GPT)	Communications (SCI, RSPI, RIIC, RSCAN)	Others
1		P14	MTIOC4B, MTIOC4B#, GTIOC2A, GTIOC2A#		
2		P13	MTIOC4A, MTIOC4A#, GTIOC1A, GTIOC1A#		
3		P12	MTIOC3B, MTIOC3B#, GTIOC0A, GTIOC0A#		
4		PE6	POE10#		IRQ3
5		PE5			IRQ0
6	VCC				
7		P02	MTIOC9D, MTIOC9D#	CTS1#, RTS1#, SS1#	IRQ5, ADST0
8	VSS				
9	VSS				
10		P00			IRQ2, ADST1
11	VCL				
12	MD				FINED
13		P01	POE12#		IRQ4, ADST2
14		PE4	MTCLKC, MTCLKC#, POE10#		IRQ1
15		PE3	MTCLKD, MTCLKD#, POE11#		IRQ2
16	RES#				
17	XTAL	P37			
18	VSS				
19	EXTAL	P36			
20	VCC				
21	VCC				
22		PE2	POE10#		NMI
23		PE1	MTIOC9D, MTIOC9D#, TMO5	CTS5#, RTS5#, SS5#, SSLA3	
24		PE0	MTIOC9B, MTIOC9B#, TMCI1, TMCI5	RXD5, SMISO5, SSCL5, SSLA2	
25		PD7	MTIOC9A, MTIOC9A#, TMRI1, TMRI5, GTIOC3A, GTIOC3A#	TXD5, SMOSI5, SSDA5, SSLA1	
26		PD6	MTIOC9C, MTIOC9C#, TMO1, GTIOC3B, GTIOC3B#	CTS1#, RTS1#, SS1#, CTS11#, RTS11#, SS11#, SSLA0	IRQ5, ADST0
27		PD5	TMRI0, TMRI6, GTECLKA	RXD1, SMISO1, SSCL1, RXD11, SMISO11, SSCL11	IRQ3
28		PD4	TMCI0, TMCI6, GTECLKB	SCK1, SCK11	IRQ2
29		PD3	TMO0, GTECLKC	TXD1, SMOSI1, SSDA1, TXD11, SMOSI11, SSDA11	
30		PD2	TMCI1, TMO4, GTIOC0A, GTIOC0A#	SCK5, MOSIA	
31		PD1	TMO2, GTIOC0B, GTIOC0B#	MISOA	
32		PD0	TMO6, GTIOC1A, GTIOC1A#	RSPCKA	
33		PF3	TMO7	CTS11#, RTS11#, SS11#, CRXD0	COMP0
34		PF2	TMO3	SCK11, CTXD0	COMP1
35		PF1	TMO5	RXD11, SMISO11, SSCL11	COMP2
36		PF0	TMO1	TXD11, SMOSI11, SSDA11	COMP3
37		PB7	GTIOC1B, GTIOC1B#	SCK5	
38		PB6	GTIOC2A, GTIOC2A#	RXD5, SMISO5, SSCL5	IRQ5
39		PB5	GTIOC2B, GTIOC2B#	TXD5, SMOSI5, SSDA5	
40	VCC				
41		PB4	POE8#, GTETRG, GTECLKD	CTS5#, RTS5#, SS5#	IRQ3
42	VSS				
43	VSS				
44		PC2	ADSM0, GTADSM0	SCK8	
45		PC1	ADSM1, GTADSM1	TXD8, SMOSI8, SSDA8	
46		PC0		RXD8, SMISO8, SSCL8	COMP3
47		PB3	MTIOC0A, MTIOC0A#, CACREF	SCK6, RSPCKA	
48		PB2	MTIOC0B, MTIOC0B#, TMRI0, ADSM0	TXD6, SMOSI6, SSDA6, SDA0	
49		PB1	MTIOC0C, MTIOC0C#, TMCI0, ADSM1	RXD6, SMISO6, SSCL6, SCL0	

Table 1.5 List of Pins and Pin Functions (144-Pin LFQFP) (2/4)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (TMR, MTU3, POE, CAC, GPT)	Communications (SCI, RSPI, RIIC, RSCAN)	Others
50		PB0	MTIOC0D, MTIOC0D#, TMO0	TXD6, SMOSI6, SSDA6, MOSIA	ADTRG2#
51		PA7	TMO2, ADSM0		
52		PA6	TMO6, ADSM1		
53		PA5	MTIOC1A, MTIOC1A#, TMCI3	RXD6, SMISO6, SSCL6, MISOA	IRQ1, ADTRG1#
54		PA4	MTIOC1B, MTIOC1B#, TMCI7	SCK6, RSPCKA	ADTRG0#
55		PA3	MTIOC2A, MTIOC2A#, TMRI7, GTADSM0	SSLA0	
56		PA2	MTIOC2B, MTIOC2B#, TMO7, GTADSM1	CTS6#, RTS6#, SS6#, SSLA1	
57		PA1	MTIOC6A, MTIOC6A#, TMO4	SSLA2, CRXD0	ADTRG0#
58		PA0	MTIOC6C, MTIOC6C#, TMO2	SSLA3, CTXD0	
59		P35	TMO0, GTADSM0	CTS8#, RTS8#, SS8#	
60		P34	TMO4, GTADSM1	CTS9#, RTS9#, SS9#	
61		PC6	MTIOC1A, MTIOC1A#	RXD11, SMISO11, SSCL11	
62		PC5	MTIOC1B, MTIOC1B#	TXD11, SMOSI11, SSDA11	
63	VCC				
64		P96	POE4#	CTS8#, RTS8#, SS8#	IRQ4
65	VSS				
66	VSS				
67		P95	MTIOC6B, MTIOC6B#		
68		P94	MTIOC7A, MTIOC7A#		
69		P93	MTIOC7B, MTIOC7B#		
70		P92	MTIOC6D, MTIOC6D#		
71		P91	MTIOC7C, MTIOC7C#		
72		P90	MTIOC7D, MTIOC7D#		
73		P76	MTIOC4D, MTIOC4D#, GTIOC2B, GTIOC2B#		
74		P75	MTIOC4C, MTIOC4C#, GTIOC1B, GTIOC1B#		
75		P74	MTIOC3D, MTIOC3D#, GTIOC0B, GTIOC0B#		
76		P73	MTIOC4B, MTIOC4B#, GTIOC2A, GTIOC2A#		
77		P72	MTIOC4A, MTIOC4A#, GTIOC1A, GTIOC1A#		
78		P71	MTIOC3B, MTIOC3B#, GTIOC0A, GTIOC0A#		
79		P70	POE0#	CTS9#, RTS9#, SS9#	IRQ5
80		PG2	GTETRG	SCK9	COMP0
81		PG1		TXD9, SMOSI9, SSDA9	COMP1
82		PG0		RXD9, SMISO9, SSCL9	COMP2
83		P33	MTIOC3A, MTIOC3A#, MTCLKA, MTCLKA#, TMO0	SSLA3	
84		P32	MTIOC3C, MTIOC3C#, MTCLKB, MTCLKB#, TMO6	SSLA2	
85	VCC				
86	VCC				
87		P31	MTIOC0A, MTIOC0A#, MTCLKC, MTCLKC#, TMRI6	SSLA1	IRQ6
88	VSS				
89	VSS				
90		P30	MTIOC0B, MTIOC0B#, MTCLKD, MTCLKD#, TMCI6	SSLA0	IRQ7, COMP3
91		P27	MTIOC1A, MTIOC1A#		
92		P26	MTIOC9A, MTIOC9A#	CTS1#, RTS1#, SS1#	ADST0
93		P25	MTIOC9C, MTIOC9C#	SCK1	ADST1
94		P24	MTIC5U, MTIC5U#, TMCI2, TMO6	RSPCKA	COMP0, DA0
95		P23	MTIC5V, MTIC5V#, TMO2, CACREF	MOSIA	COMP1, DA1

Table 1.5 List of Pins and Pin Functions (144-Pin LFQFP) (3/4)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (TMR, MTU3, POE, CAC, GPT)	Communications (SCI, RSPI, RIIC, RSCAN)	Others
96		P22	MTIC5W, MTIC5W#, TMRI2, TMO4	MISOA	ADTRG2#, COMP2
97		PC4		TXD1, SMOSI1, SSDA1	ADST2
98		PC3		RXD1, SMISO1, SSCL1	
99		P21	MTCLKA, MTCLKA#, MTIOC9A, MTIOC9A#, TMCI4		IRQ6, ADTRG1#, AN116
100		P20	MTCLKB, MTCLKB#, MTIOC9C, MTIOC9C#, TMRI4		IRQ7, ADTRG0#, AN016
101		P65			AN205
102		P64			AN204
103	VREFH2				
104	AVCC2				
105	AVSS2				
106	VREFL2				
107		P63			AN203, IRQ7
108		P62			AN202, IRQ6
109		P61			AN201, IRQ5
110		P60			AN200, IRQ4
111		P55			AN211, IRQ3
112		P54			AN210, IRQ2
113		P53			AN209, IRQ1
114		P52			AN208, IRQ0
115		P51			AN207
116		P50			AN206
117		P47			AN103
118		P46			AN102, CMPC12, CMPC13, CMPC30, CMPC31
119		P45			AN101, CMPC02, CMPC03, CMPC20, CMPC21
120		P44			AN100, CMPC10, CMPC11, CMPC32, CMPC33
121	PGAVSS1				
122		P43			AN003
123		P42			AN002
124		P41			AN001
125		P40			AN000, CMPC00, CMPC01, CMPC22, CMPC23
126	PGAVSS0				
127	AVCC1				
128	VREFH1				
129	AVCC0				
130	VREFH0				
131	AVSS0				
132	VREFL0				
133	AVSS1				
134	VREFL1				
135		P84		TXD8, SMOSI8, SSDA8	
136		P83		RXD8, SMISO8, SSCL8	
137		P82	MTIC5U, MTIC5U#, TMO4	SCK6	
138		P81	MTIC5V, MTIC5V#, TMCI4	TXD6, SMOSI6, SSDA6	
139		P80	MTIC5W, MTIC5W#, TMRI4	RXD6, SMISO6, SSCL6	
140		P11	MTIOC3A, MTIOC3A#, MTCLKC, MTCLKC#, TMO3		IRQ1
141		P10	MTIOC9B, MTIOC9B#, MTCLKD, MTCLKD#, TMRI3, POE12#	CTS6#, RTS6#, SS6#	IRQ0
142		P17	MTIOC4D, MTIOC4D#, GTIOC2B, GTIOC2B#		

Table 1.5 List of Pins and Pin Functions (144-Pin LFQFP) (4/4)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (TMR, MTU3, POE, CAC, GPT)	Communications (SCI, RSPI, RIIC, RSCAN)	Others
143		P16	MTIOC4C, MTIOC4C#, GTIOC1B, GTIOC1B#		
144		P15	MTIOC3D, MTIOC3D#, GTIOC0B, GTIOC0B#		

Table 1.6 List of Pins and Pin Functions (100-Pin LFQFP) (1/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (TMR, MTU3, POE, CAC, GPT)	Communications (SCI, RSPI, RIIC, RSCAN)	Others
1		PE5			IRQ0
2		P02	MTIOC9D, MTIOC9D#	CTS1#, RTS1#, SS1#	IRQ5, ADST0
3	VSS				
4		P00			IRQ2, ADST1
5	VCL				
6	MD				FINED
7		P01	POE12#		IRQ4, ADST2
8		PE4	MTCLKC, MTCLKC#, POE10#		IRQ1
9		PE3	MTCLKD, MTCLKD#, POE11#		IRQ2
10	RES#				
11	XTAL	P37			
12	VSS				
13	EXTAL	P36			
14	VCC				
15		PE2	POE10#		NMI
16		PE1	MTIOC9D, MTIOC9D#, TMO5	CTS5#, RTS5#, SS5#, SSLA3	
17		PE0	MTIOC9B, MTIOC9B#, TMCI1, TMCI5	RXD5, SMISO5, SSCL5, SSLA2	
18		PD7	MTIOC9A, MTIOC9A#, TMRI1, TMRI5, GTIOC3A, GTIOC3A#	TXD5, SMOSI5, SSDA5, SSLA1	
19		PD6	MTIOC9C, MTIOC9C#, TMO1, GTIOC3B, GTIOC3B#	CTS1#, RTS1#, SS1#, CTS11#, RTS11#, SS11#, SSLA0	IRQ5, ADST0
20		PD5	TMRI0, TMRI6, GTECLKA	RXD1, SMISO1, SSCL1, RXD11, SMISO11, SSCL11	IRQ3
21		PD4	TMCI0, TMCI6, GTECLKB	SCK1, SCK11	IRQ2
22		PD3	TMO0, GTECLKC	TXD1, SMOSI1, SSDA1, TXD11, SMOSI11, SSDA11	
23		PD2	TMCI1, TMO4, GTIOC0A, GTIOC0A#	SCK5, MOSIA	
24		PD1	TMO2, GTIOC0B, GTIOC0B#	MISOA	
25		PD0	TMO6, GTIOC1A, GTIOC1A#	RSPCKA	
26		PB7	GTIOC1B, GTIOC1B#	SCK5	
27		PB6	GTIOC2A, GTIOC2A#	RXD5, SMISO5, SSCL5	IRQ5
28		PB5	GTIOC2B, GTIOC2B#	TXD5, SMOSI5, SSDA5	
29	VCC				
30		PB4	POE8#, GTETRG, GTECLKD	CTS5#, RTS5#, SS5#	IRQ3
31	VSS				
32		PB3	MTIOC0A, MTIOC0A#, CACREF	SCK6, RSPCKA	
33		PB2	MTIOC0B, MTIOC0B#, TMRI0, ADSM0	TXD6, SMOSI6, SSDA6, SDA0	
34		PB1	MTIOC0C, MTIOC0C#, TMCI0, ADSM1	RXD6, SMISO6, SSCL6, SCL0	
35		PB0	MTIOC0D, MTIOC0D#, TMO0	TXD6, SMOSI6, SSDA6, MOSIA	ADTRG2#
36		PA5	MTIOC1A, MTIOC1A#, TMCI3	RXD6, SMISO6, SSCL6, MISOA	IRQ1, ADTRG1#
37		PA4	MTIOC1B, MTIOC1B#, TMCI7	SCK6, RSPCKA	ADTRG0#
38		PA3	MTIOC2A, MTIOC2A#, TMRI7, GTADSM0	SSLA0	
39		PA2	MTIOC2B, MTIOC2B#, TMO7, GTADSM1	CTS6#, RTS6#, SS6#, SSLA1	
40		PA1	MTIOC6A, MTIOC6A#, TMO4	SSLA2, CRXD0	ADTRG0#
41		PA0	MTIOC6C, MTIOC6C#, TMO2	SSLA3, CTXD0	
42	VCC				
43		P96	POE4#		IRQ4
44	VSS				
45		P95	MTIOC6B, MTIOC6B#		
46		P94	MTIOC7A, MTIOC7A#		
47		P93	MTIOC7B, MTIOC7B#		
48		P92	MTIOC6D, MTIOC6D#		
49		P91	MTIOC7C, MTIOC7C#		
50		P90	MTIOC7D, MTIOC7D#		

Table 1.6 List of Pins and Pin Functions (100-Pin LFQFP) (2/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (TMR, MTU3, POE, CAC, GPT)	Communications (SCI, RSPI, RIIC, RSCAN)	Others
51		P76	MTIOC4D, MTIOC4D#, GTIOC2B, GTIOC2B#		
52		P75	MTIOC4C, MTIOC4C#, GTIOC1B, GTIOC1B#		
53		P74	MTIOC3D, MTIOC3D#, GTIOC0B, GTIOC0B#		
54		P73	MTIOC4B, MTIOC4B#, GTIOC2A, GTIOC2A#		
55		P72	MTIOC4A, MTIOC4A#, GTIOC1A, GTIOC1A#		
56		P71	MTIOC3B, MTIOC3B#, GTIOC0A, GTIOC0A#		
57		P70	POE0#		IRQ5
58		P33	MTIOC3A, MTIOC3A#, MTCLKA, MTCLKA#, TMO0	SSLA3	
59		P32	MTIOC3C, MTIOC3C#, MTCLKB, MTCLKB#, TMO6	SSLA2	
60	VCC				
61		P31	MTIOC0A, MTIOC0A#, MTCLKC, MTCLKC#, TMRI6	SSLA1	IRQ6
62	VSS				
63		P30	MTIOC0B, MTIOC0B#, MTCLKD, MTCLKD#, TMCI6	SSLA0	IRQ7, COMP3
64		P27	MTIOC1A, MTIOC1A#		
65		P24	MTIC5U, MTIC5U#, TMCI2, TMO6	RSPCKA	COMP0, DA0
66		P23	MTIC5V, MTIC5V#, TMO2, CACREF	MOSIA	COMP1, DA1
67		P22	MTIC5W, MTIC5W#, TMRI2, TMO4	MISOA	ADTRG2#, COMP2
68		P21	MTCLKA, MTCLKA#, MTIOC9A, MTIOC9A#, TMCI4		IRQ6, ADTRG1#, AN116
69		P20	MTCLKB, MTCLKB#, MTIOC9C, MTIOC9C#, TMRI4		IRQ7, ADTRG0#, AN016
70		P65			AN205
71		P64			AN204
72	AVCC2				
73	AVSS2				
74		P63			AN203, IRQ7
75		P62			AN202, IRQ6
76		P61			AN201, IRQ5
77		P60			AN200, IRQ4
78		P55			AN211, IRQ3
79		P54			AN210, IRQ2
80		P53			AN209, IRQ1
81		P52			AN208, IRQ0
82		P47			AN103
83		P46			AN102, CMPC12, CMPC13, CMPC30, CMPC31
84		P45			AN101, CMPC02, CMPC03, CMPC20, CMPC21
85		P44			AN100, CMPC10, CMPC11, CMPC32, CMPC33
86	PGAVSS1				
87		P43			AN003
88		P42			AN002
89		P41			AN001
90		P40			AN000, CMPC00, CMPC01, CMPC22, CMPC23
91	PGAVSS0				

Table 1.6 List of Pins and Pin Functions (100-Pin LFQFP) (3/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (TMR, MTU3, POE, CAC, GPT)	Communications (SCI, RSPI, RIIC, RSCAN)	Others
92	AVCC1				
93	AVCC0				
94	AVSS0				
95	AVSS1				
96		P82	MTIC5U, MTIC5U#, TMO4	SCK6	
97		P81	MTIC5V, MTIC5V#, TMCI4	TXD6, SMOSI6, SSDA6	
98		P80	MTIC5W, MTIC5W#, TMRI4	RXD6, SMISO6, SSCL6	
99		P11	MTIOC3A, MTIOC3A#, MTCLKC, MTCLKC#, TMO3		IRQ1
100		P10	MTIOC9B, MTIOC9B#, MTCLKD, MTCLKD#, TMRI3, POE12#	CTS6#, RTS6#, SS6#	IRQ0

2. CPU

The RXv2 instruction set architecture (RXv2) has upward compatibility with the RXv1 instruction set architecture (RXv1).

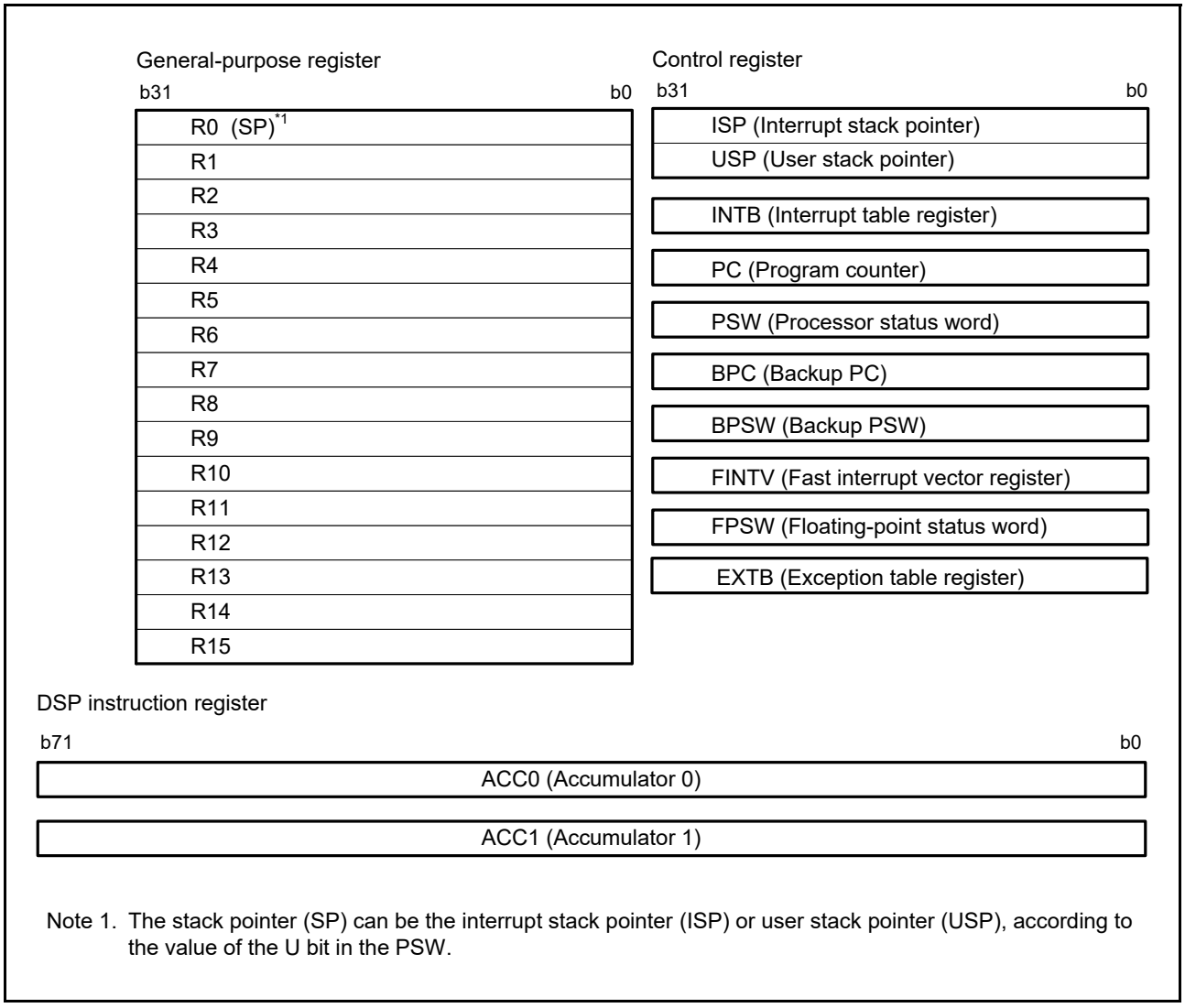
- Adoption of variable-length instruction format
  As with RXv1, the RXv2 CPU has short formats for frequently used instructions, facilitating the development of efficient programs that take up less memory.
- Powerful instruction set
  The RXv2 supports 109 selected instructions. Moreover, DSP instructions and floating-point operation instructions are added, thus realizing high-speed arithmetic processing.
- Versatile addressing modes
  The RXv2 CPU has 11 versatile addressing modes, with register-register operations, register-memory operations, and bitwise operations included. Data transfer between memory locations is also possible.

2.1 Features

- Minimum instruction execution rate: One clock cycle
- Address space: 4-Gbyte linear addresses
- Register set of the CPU
  General purpose: Sixteen 32-bit registers
  Control: Ten 32-bit registers
  Accumulator: Two 72-bit registers
- Variable-length instruction format (lengths from one to eight bytes)
- 109 instructions/11 addressing modes
  Basic instructions: 75
  Floating-point operation instructions: 11
  DSP instructions: 23
- Processor modes
  Supervisor mode and user mode
- Vector tables
  Exception vector table and interrupt vector table
- Memory protection unit
- Data arrangement
  Selectable as little endian or big endian

2.2 Register Set of the CPU

The RXv2 CPU has sixteen general-purpose registers, ten control registers, and two accumulator used for DSP instructions.



Note 1. The stack pointer (SP) can be the interrupt stack pointer (ISP) or user stack pointer (USP), according to the value of the U bit in the PSW.

Figure 2.1 Register Set of the CPU

2.2.1 General-Purpose Registers (R0 to R15)

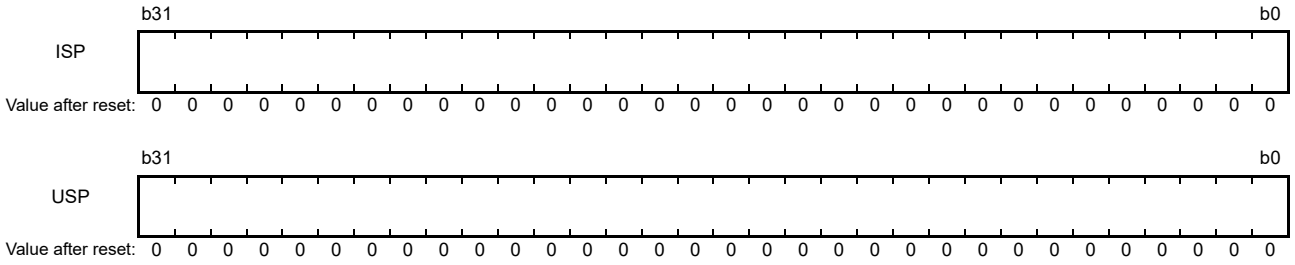
This CPU has sixteen 32-bit general-purpose registers (R0 to R15). R0 to R15 can be used as data registers or address registers.
R0, a general-purpose register, also functions as the stack pointer (SP).
The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2.2 Control Registers

This CPU has the following ten control registers.

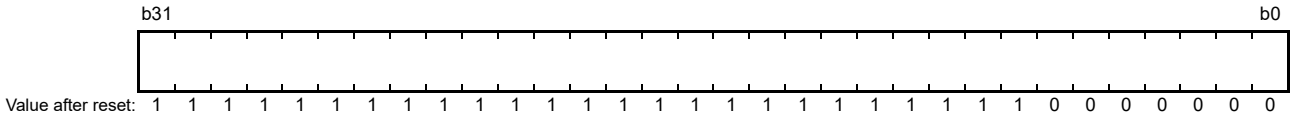
- Interrupt stack pointer (ISP)
- User stack pointer (USP)
- Exception table register (EXTB)
- Interrupt table register (INTB)
- Program counter (PC)
- Processor status word (PSW)
- Backup PC (BPC)
- Backup PSW (BPSW)
- Fast interrupt vector register (FINTV)
- Floating-point status word (FPSW)

2.2.2.1 Interrupt Stack Pointer (ISP)/User Stack Pointer (USP)



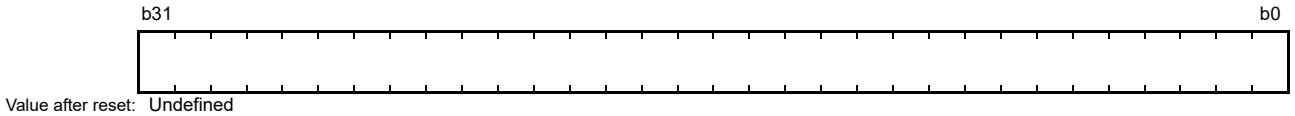
The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).
Set the ISP or USP to a multiple of 4 to reduce the number of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

2.2.2.2 Exception Table Register (EXTB)



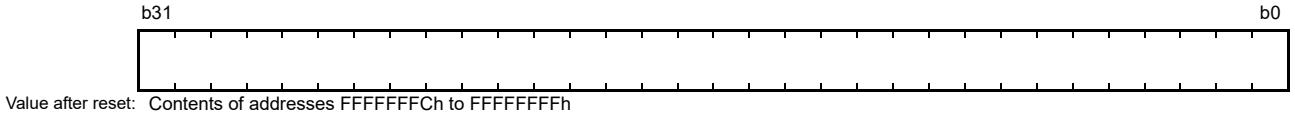
The exception table register (EXTB) specifies the address where the exception vector table starts.
Set the EXTB to a multiple of 4 to reduce the number of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

2.2.2.3 Interrupt Table Register (INTB)



The interrupt table register (INTB) specifies the address where the interrupt vector table starts.
Set the INTB to a multiple of 4 to reduce the number of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

2.2.2.4 Program Counter (PC)



The program counter (PC) indicates the address of the instruction being executed.

2.2.2.5 Processor Status Word (PSW)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	IPL[3:0]				—	—	—	PM	—	—	U	I
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	O	S	Z	C
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	C	Carry Flag	0: No carry has occurred. 1: A carry has occurred.	R/W
b1	Z	Zero Flag	0: Result is non-zero. 1: Result is 0.	R/W
b2	S	Sign Flag	0: Result is a positive value or 0. 1: Result is a negative value.	R/W
b3	O	Overflow Flag	0: No overflow has occurred. 1: An overflow has occurred.	R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	I*1	Interrupt Enable	0: Interrupt disabled. 1: Interrupt enabled.	R/W
b17	U*1	Stack Pointer Select	0: Interrupt stack pointer (ISP) is selected. 1: User stack pointer (USP) is selected.	R/W
b19, b18	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b20	PM*1, *2, *3	Processor Mode Select	0: Supervisor mode is selected. 1: User mode is selected.	R/W
b23 to b21	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b27 to b24	IPL[3:0]*1	Processor Interrupt Priority Level	b27 b24 0 0 0 0: Priority level 0 (lowest) 0 0 0 1: Priority level 1 0 0 1 0: Priority level 2 0 0 1 1: Priority level 3 0 1 0 0: Priority level 4 0 1 0 1: Priority level 5 0 1 1 0: Priority level 6 0 1 1 1: Priority level 7 1 0 0 0: Priority level 8 1 0 0 1: Priority level 9 1 0 1 0: Priority level 10 1 0 1 1: Priority level 11 1 1 0 0: Priority level 12 1 1 0 1: Priority level 13 1 1 1 0: Priority level 14 1 1 1 1: Priority level 15 (highest)	R/W
b31 to b28	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. In user mode, writing to the IPL[3:0], PM, U, and I bits by an MVTC or a POPC instruction is ignored. Writing to the IPL[3:0] bits by an MVTIPL instruction generates a privileged instruction exception.
Note 2. In supervisor mode, writing to the PM bit by an MVTC or a POPC instruction is ignored, but writing to the other bits is possible.
Note 3. Switching from supervisor mode to user mode requires execution of an RTE instruction after having set the PSW.PM bit saved on the stack to 1 or executing an RTFI instruction after having set the BPSW.PM bit to 1.

The processor status word (PSW) indicates the results of instruction execution or the state of the CPU.

C Flag (Carry Flag)

This flag retains the state of the bit after a carry, borrow, or shift-out has occurred.

Z Flag (Zero Flag)

This flag is set to 1 if the result of an operation is 0; otherwise its value is cleared to 0.

S Flag (Sign Flag)

This flag is set to 1 if the result of an operation is negative; otherwise its value is cleared to 0.

O Flag (Overflow Flag)

This flag is set to 1 if the result of an operation overflows; otherwise its value is cleared to 0.

I Bit (Interrupt Enable)

This bit enables interrupt requests. When a WAIT instruction is executed, the value of this bit becomes 1. It becomes 0 when an exception is accepted.

U Bit (Stack Pointer Select)

This bit specifies the stack pointer as either the ISP or USP. When an exception request is accepted, this bit is set to 0. When the processor mode is switched from supervisor mode to user mode, this bit is set to 1.

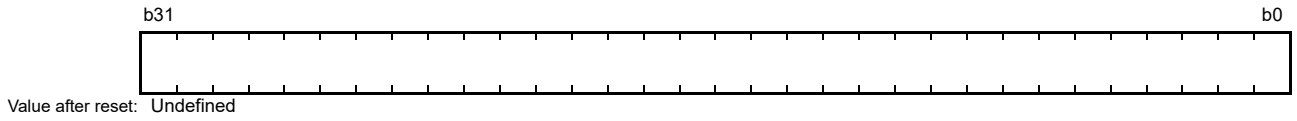
PM Bit (Processor Mode Select)

This bit specifies the processor mode. When an exception is accepted, the value of this bit becomes 0.

IPL[3:0] Bits (Processor Interrupt Priority Level)

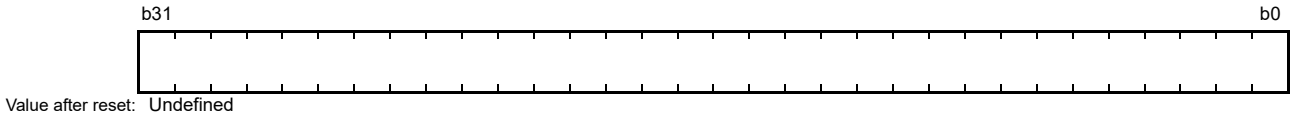
The IPL[3:0] bits specify the processor interrupt priority level as one of sixteen levels from zero to fifteen, wherein priority level zero is the lowest and priority level fifteen the highest. When the priority level of a requested interrupt is higher than the processor interrupt priority level, the interrupt is enabled. Setting the IPL[3:0] bits to level fifteen (Fh) disables all interrupt requests. The IPL[3:0] bits are set to level fifteen (Fh) when a non-maskable interrupt is generated. When interrupts in general are generated, the bits are set to the priority levels of accepted interrupts.

2.2.2.6 Backup PC (BPC)



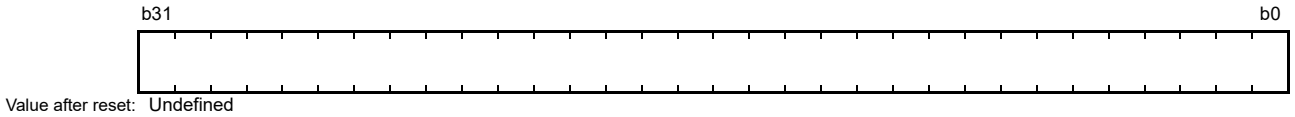
The backup PC (BPC) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC register.

2.2.2.7 Backup PSW (BPSW)



The backup PSW (BPSW) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

2.2.2.8 Fast Interrupt Vector Register (FINTV)



The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.
The FINTV register specifies a branch destination address when a fast interrupt has been generated.

2.2.2.9 Floating-Point Status Word (FPSW)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	FS	FX	FU	FZ	FO	FV	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	EX	EU	EZ	EO	EV	—	DN	CE	CX	CU	CZ	CO	CV	RM[1:0]	
Value after reset:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	RM[1:0]	Floating-Point Rounding-Mode Setting	b1 b0 0 0: Rounding towards the nearest value 0 1: Rounding towards 0 1 0: Rounding towards +∞ 1 1: Rounding towards –∞	R/W
b2	CV	Invalid Operation Cause Flag	0: No invalid operation has been encountered. 1: Invalid operation has been encountered.	R/(W) *1
b3	CO	Overflow Cause Flag	0: No overflow has occurred. 1: Overflow has occurred.	R/(W) *1
b4	CZ	Division-by-Zero Cause Flag	0: No division-by-zero has occurred. 1: Division-by-zero has occurred.	R/(W) *1
b5	CU	Underflow Cause Flag	0: No underflow has occurred. 1: Underflow has occurred.	R/(W) *1
b6	CX	Inexact Cause Flag	0: No inexact exception has been generated. 1: Inexact exception has been generated.	R/(W) *1
b7	CE	Unimplemented Processing Cause Flag	0: No unimplemented processing has been encountered. 1: Unimplemented process has been encountered.	R/(W) *1
b8	DN	0 Flush Bit of Denormalized Number	0: A denormalized number is handled as a denormalized number. 1: A denormalized number is handled as 0.*2	R/W
b9	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b10	EV	Invalid Operation Exception Enable	0: Invalid operation exception is masked. 1: Invalid operation exception is enabled.	R/W
b11	EO	Overflow Exception Enable	0: Overflow exception is masked. 1: Overflow exception is enabled.	R/W
b12	EZ	Division-by-Zero Exception Enable	0: Division-by-zero exception is masked. 1: Division-by-zero exception is enabled.	R/W
b13	EU	Underflow Exception Enable	0: Underflow exception is masked. 1: Underflow exception is enabled.	R/W
b14	EX	Inexact Exception Enable	0: Inexact exception is masked. 1: Inexact exception is enabled.	R/W
b25 to b15	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b26	FV*3	Invalid Operation Flag	0: No invalid operation has been encountered. 1: Invalid operation has been encountered.*8	R/W
b27	FO*4	Overflow Flag	0: No overflow has occurred. 1: Overflow has occurred.*8	R/W
b28	FZ*5	Division-by-Zero Flag	0: No division-by-zero has occurred. 1: Division-by-zero has occurred.*8	R/W
b29	FU*6	Underflow Flag	0: No underflow has occurred. 1: Underflow has occurred.*8	R/W
b30	FX*7	Inexact Flag	0: No inexact exception has been generated. 1: Inexact exception has been generated.*8	R/W

Bit	Symbol	Bit Name	Description	R/W
b31	FS	Floating-Point Error Summary Flag	This bit reflects the logical OR of the FU, FZ, FO, and FV flags.	R

Note 1. Writing 0 to the bit clears it. Writing 1 to the bit does not affect its value.
Note 2. Positive denormalized numbers are treated as +0, negative denormalized numbers as –0.
Note 3. When the EV bit is set to 0, the FV flag is enabled.
Note 4. When the EO bit is set to 0, the FO flag is enabled.
Note 5. When the EZ bit is set to 0, the FZ flag is enabled.
Note 6. When the EU bit is set to 0, the FU flag is enabled.
Note 7. When the EX bit is set to 0, the FX flag is enabled.
Note 8. Once the bit has been set to 1, this value is retained until it is cleared to 0 by software.

The floating-point status word (FPSW) indicates the results of floating-point operations.
When an exception handling enable bit (Ej) enables the exception handling (Ej = 1), the exception cause can be identified by checking the corresponding Cj flag in the exception handling routine. If the exception handling is masked (Ej = 0), the occurrence of exception can be checked by reading the Fj flag at the end of a series of processing. Once the Fj flag has been set to 1, this value is retained until it is cleared to 0 by software (j = X, U, Z, O, or V).

RM[1:0] Bits (Floating-Point Rounding-Mode Setting)

These bits specify the floating-point rounding-mode.

Explanation of Floating-Point Rounding Modes

- Rounding towards the nearest value (the default behavior) : An inexact result is rounded to the available value that is closest to the result which would be obtained with an infinite number of digits. If two available values are equally close, rounding is to the even alternative.
- Rounding towards 0 : An inexact result is rounded to the smallest available absolute value, i.e. in the direction of zero (simple truncation).
- Rounding towards +∞ : An inexact result is rounded to the nearest available value in the direction of positive infinity.
- Rounding towards –∞ : An inexact result is rounded to the nearest available value in the direction of negative infinity.

(1) Rounding to the nearest value is specified as the default mode and returns the most accurate value.
(2) Modes such as rounding towards 0, rounding towards +∞, and rounding towards –∞ are used to ensure precision when interval arithmetic is employed.

CV Flag (Invalid Operation Cause Flag), CO Flag (Overflow Cause Flag), CZ Flag (Division-by-Zero Cause Flag), CU Flag (Underflow Cause Flag), CX Flag (Inexact Cause Flag), and CE Flag (Unimplemented Processing Cause Flag)

Floating-point exceptions include the five specified in the IEEE754 standard, namely overflow, underflow, inexact, division-by-zero, and invalid operation. For a further floating-point exception that is generated upon detection of unimplemented processing, the corresponding flag (CE) is set to 1.

- The bit that has been set to 1 is cleared to 0 when the FPU instruction is executed.
- When 0 is written to the bit by the MVTC and POPC instructions, the bit is set to 0; the bit retains the previous value when 1 is written by the instruction.

DN Bit (0 Flush Bit of Denormalized Number)

When this bit is set to 0, a denormalized number is handled as a denormalized number. When this bit is set to 1, a denormalized number is handled as 0.

EV Bit (Invalid Operation Exception Enable), EO Bit (Overflow Exception Enable), EZ Bit (Division-by-Zero Exception Enable), EU Bit (Underflow Exception Enable), and EX Bit (Inexact Exception Enable)

When any of five floating-point exceptions specified in the IEEE754 standard is generated by the floating-point

operation instruction, the bit decides whether the CPU will start handling the exception. When the bit is set to 0, the exception handling is masked; when the bit is set to 1, the exception handling is enabled.

FV Flag (Invalid Operation Flag), FO Flag (Overflow Flag), FZ Flag (Division-by-Zero Flag), FU Flag (Underflow Flag), and FX Flag (Inexact Flag)

While the exception handling enable bit (Ej) is 0 (exception handling is masked), if any of five floating-point exceptions specified in the IEEE754 standard is generated, the corresponding bit is set to 1.

- When Ej is 1 (exception handling is enabled), the value of the flag remains.
- When the corresponding flag is set to 1, it remains 1 until it is cleared to 0 by software. (accumulation flag)

FS Flag (Floating-Point Error Summary Flag)

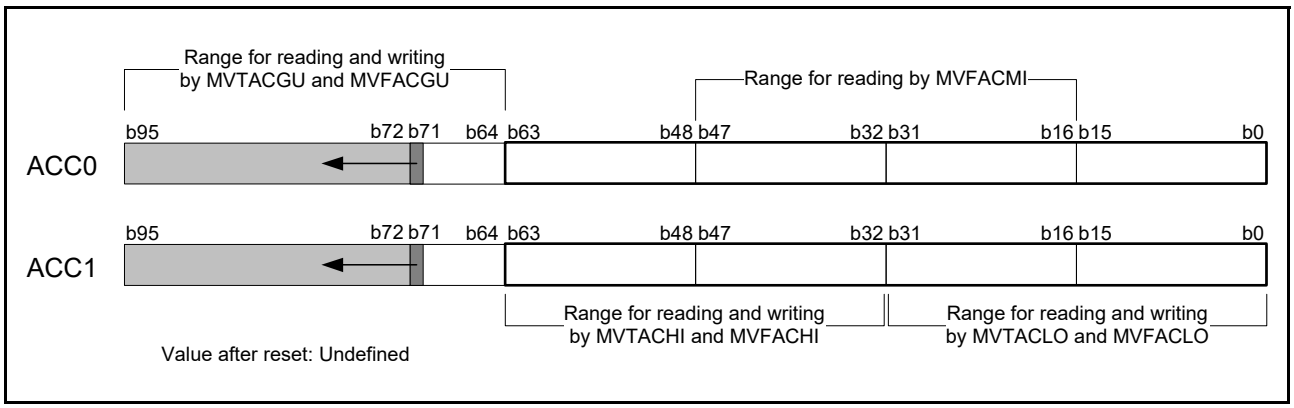
This bit reflects the logical OR of the FU, FZ, FO, and FV flags.

2.2.3 Accumulator

The accumulator (ACC0 or ACC1) is a 72-bit register used for DSP instructions. The accumulator is handled as a 96-bit register for reading and writing. At this time, when bits 95 to 72 of the accumulator are read, the value where the value of bit 71 is sign extended is read. Writing to bits 95 to 72 of the accumulator is ignored. ACC0 is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, FMUL, MUL, and RMPA, in which case the prior value in ACC0 is modified by execution of the instruction.

Use the MVTACGU, MVTACHI, and MVTACLO instructions for writing to the accumulator. The MVTACGU, MVTACHI, and MVTACLO instructions write data to bits 95 to 64, the higher-order 32 bits (bits 63 to 32), and the lower-order 32 bits (bits 31 to 0), respectively.

Use the MVFACGU, MVFACHI, MVFACMI, and MVFACLO instructions for reading data from the accumulator. The MVFACGU, MVFACHI, MVFACMI, and MVFACLO instructions read data from the guard bits (bits 95 to 64), higher-order 32 bits (bits 63 to 32), the middle 32 bits (bits 47 to 16), and the lower-order 32 bits (bits 31 to 0), respectively.



Note: The value of bit 71 is sign extended for bits 95 to 72 and the extended value is always read. Writing to this area is ignored.

2.3 Processor Mode

The RXv2 CPU supports two processor modes, supervisor and user. These processor modes and the memory protection function enable the realization of a hierarchical CPU resource protection and memory protection mechanism. Each processor mode imposes a level on rights of access to memory and the instructions that can be executed. Supervisor mode carries greater rights than user mode. The initial state after a reset is supervisor mode.

2.3.1 Supervisor Mode

In supervisor mode, all CPU resources are accessible and all instructions are available. However, writing to the processor mode select bit (PM) in the processor status word (PSW) by executing an MVTC or a POPC instruction will be ignored. For details on how to write to the PM bit, refer to section 2.2.2.5, Processor Status Word (PSW).

2.3.2 User Mode

In user mode, write access to the CPU resources listed below is restricted. The restriction applies to any instruction capable of write access.

- Some bits (bits IPL[3:0], PM, U, and I) in the processor status word (PSW)
- Interrupt stack pointer (ISP)
- Exception table register (EXTB)
- Interrupt table register (INTB)
- Backup PSW (BPSW)
- Backup PC (BPC)
- Fast interrupt vector register (FINTV)

2.3.3 Privileged Instruction

Privileged instructions can only be executed in supervisor mode. Executing a privileged instruction in user mode produces a privileged instruction exception. Privileged instructions include the RTFI, MVTIPL, RTE, and WAIT instructions.

2.3.4 Switching Between Processor Modes

Manipulating the processor mode select bit (PM) in the processor status word (PSW) switches the processor mode. However, rewriting to the PM bit by executing an MVTC or a POPC instruction is prohibited. Switch the processor mode by following the procedures described below.

(1) Switching from user mode to supervisor mode

After an exception has been generated, the PSW.PM bit is set to 0 and the CPU switches to supervisor mode. The hardware pre-processing is executed in supervisor mode. The state of the processor mode before the exception was generated is retained in the copy of PSW.PM bit is saved on the stack.

(2) Switching from supervisor mode to user mode

Executing an RTE instruction when the value of the copy of the PSW.PM bit that has been preserved on the stack is 1 or an RTFI instruction when the value of the copy of the PSW.PM bit that has been preserved in the backup PSW (BPSW) is 1 causes a transition to user mode. In the transition to user mode, the value of the stack pointer designation bit (the U bit in the PSW) becomes 1.

2.4 Data Types

The RXv2 CPU can handle four types of data: integer, floating-point, bit, and string.
For details, refer to RX Family RXv2 Instruction Set Architecture User's Manual: Software.

2.4.1 Integer

An integer can be signed or unsigned. For signed integers, negative values are represented by two's complements.

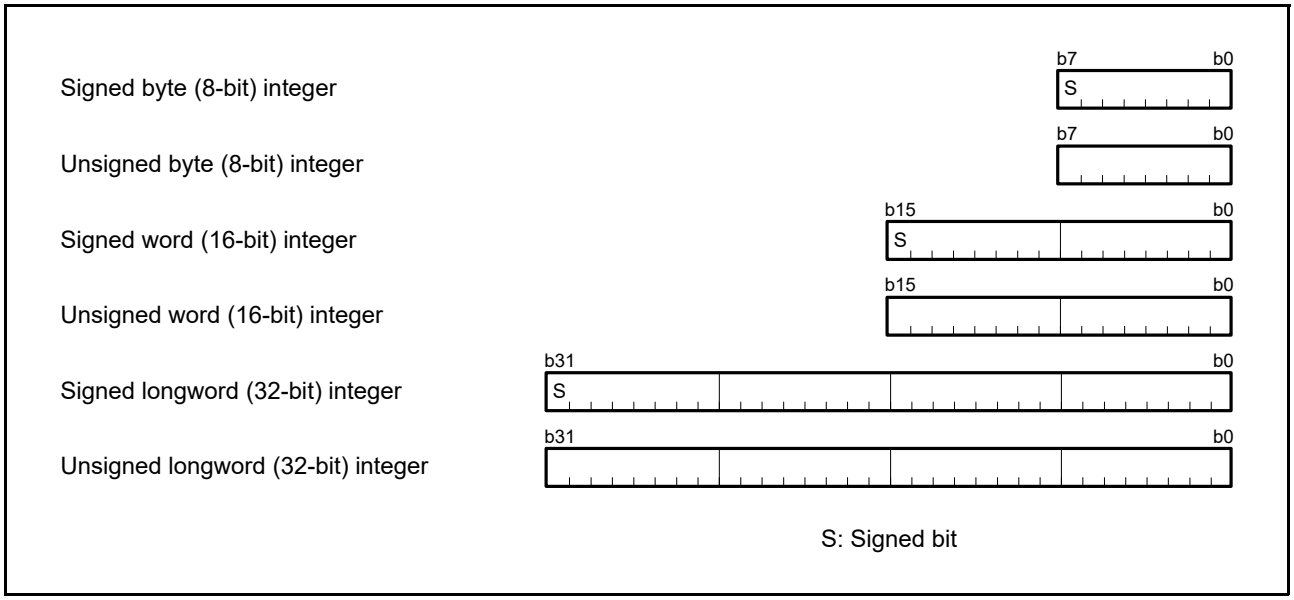


Figure 2.2 Integer

2.4.2 Floating-Points

Floating-point support is for the single-precision floating-point type specified in the IEEE754 standard; operands of this type can be used in eleven floating-point operation instructions: FADD, FCMP, FDIV, FMUL, FSQRT, FSUB, FTOI, FTOU, ITOF, ROUND, and UTOF.

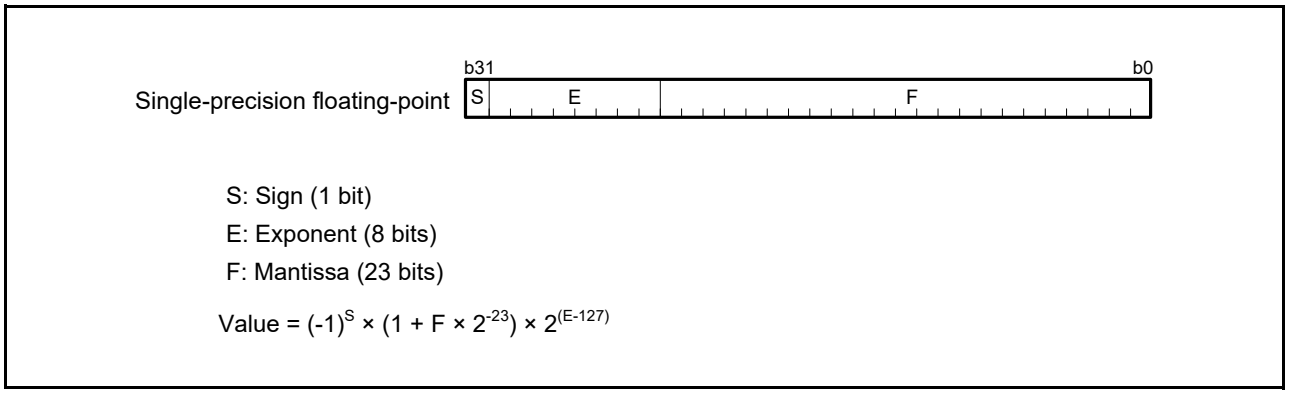


Figure 2.3 Floating-Point

The floating-point format supports the values listed below.

0 < E < 255 (normal numbers)
E = 0 and F = 0 (signed zero)
E = 0 and F > 0 (denormalized numbers)*1
E = 255 and F = 0 (infinity)
E = 255 and F > 0 (NaN: Not-a-Number)

Note 1. The number is treated as 0 when the FPSW.DN bit is 1. When the DN bit is 0, an unimplemented processing exception is generated.

2.4.3 Bitwise Operations

Five bit-manipulation instructions are provided for bitwise operations: BCLR, BMCnd, BNOT, BSET, and BTST.
A bit in a register is specified as the destination register and a bit number in the range from 31 to 0.
A bit in memory is specified as the destination address and a bit number from 7 to 0. The addressing modes available to specify addresses are register indirect and register relative.

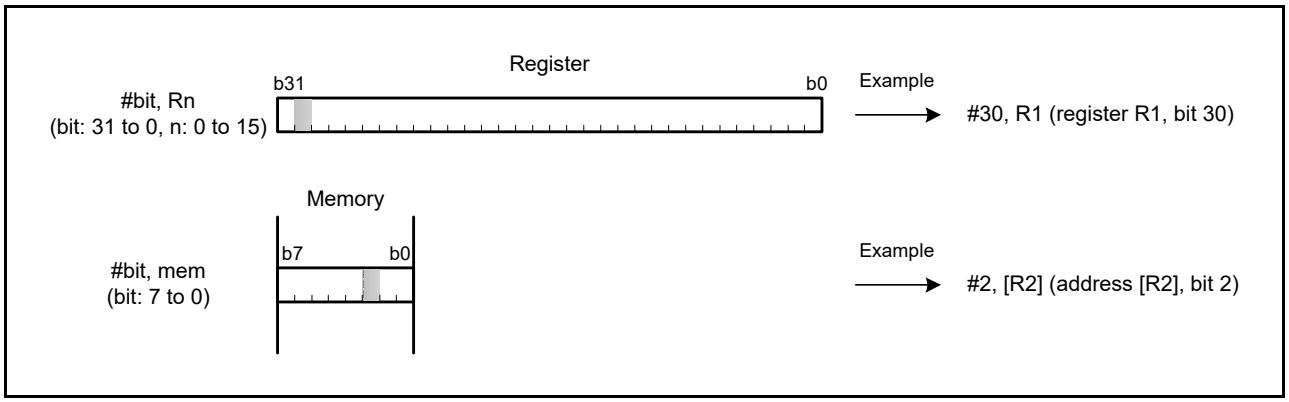


Figure 2.4 Bit

2.4.4 Strings

The string data type consists of an arbitrary number of consecutive byte (8-bit), word (16-bit), or longword (32-bit) units. Seven string manipulation instructions are provided for use with strings: SCMPU, SMOVB, SMOVF, SMOVU, SSTR, SUNTIL, and SWHILE.

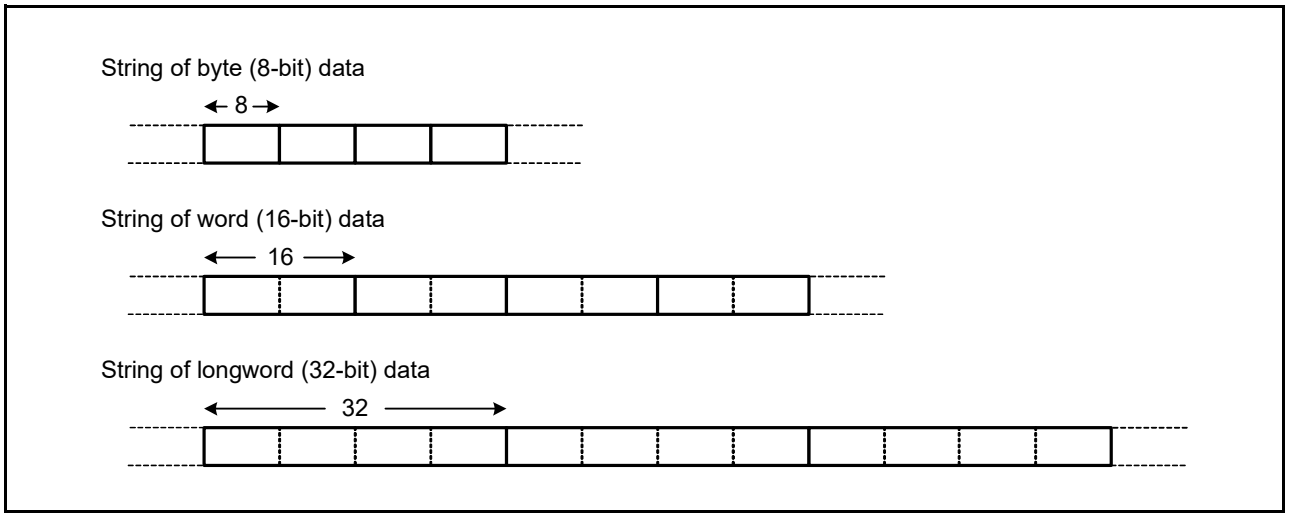


Figure 2.5 String

2.5 Endian

For the RXv2 CPU, instructions are little endian, but the treatment of data is selectable as little or big endian.

2.5.1 Switching the Endian

As arrangements of bytes, this MCU supports both big endian, where the higher-order byte (MSB) is at location 0, and little endian, where the lower-order byte (LSB) is at location 0.
For details on the endian setting, see section 3, Operating Modes.
Operations for access differ according to the endian setting and, depending on the instruction, whether 8-, 16- or 32-bit access has been selected. Operations for access in the various possible cases are described in Table 2.1 to Table 2.12.
In the tables,

LL indicates bits D7 to D0 of the general-purpose register,
LH indicates bits D15 to D8 of the general-purpose register,
HL indicates bits D23 to D16 of the general-purpose register, and
HH indicates bits D31 to D24 of the general-purpose register.

	D31 to D24	D23 to D16	D15 to D8	D7 to D0
General purpose register: Rm	HH	HL	LH	LL

Table 2.1 32-Bit Read Operations when Little Endian has been Selected

Operation / Address of src	Reading a 32-bit unit from address 0	Reading a 32-bit unit from address 1	Reading a 32-bit unit from address 2	Reading a 32-bit unit from address 3	Reading a 32-bit unit from address 4
Address 0	Transfer to LL	—	—	—	—
Address 1	Transfer to LH	Transfer to LL	—	—	—
Address 2	Transfer to HL	Transfer to LH	Transfer to LL	—	—
Address 3	Transfer to HH	Transfer to HL	Transfer to LH	Transfer to LL	—
Address 4	—	Transfer to HH	Transfer to HL	Transfer to LH	Transfer to LL
Address 5	—	—	Transfer to HH	Transfer to HL	Transfer to LH
Address 6	—	—	—	Transfer to HH	Transfer to HL
Address 7	—	—	—	—	Transfer to HH

Table 2.2 32-Bit Read Operations when Big Endian has been Selected

Operation / Address of src	Reading a 32-bit unit from address 0	Reading a 32-bit unit from address 1	Reading a 32-bit unit from address 2	Reading a 32-bit unit from address 3	Reading a 32-bit unit from address 4
Address 0	Transfer to HH	—	—	—	—
Address 1	Transfer to HL	Transfer to HH	—	—	—
Address 2	Transfer to LH	Transfer to HL	Transfer to HH	—	—
Address 3	Transfer to LL	Transfer to LH	Transfer to HL	Transfer to HH	—
Address 4	—	Transfer to LL	Transfer to LH	Transfer to HL	Transfer to HH
Address 5	—	—	Transfer to LL	Transfer to LH	Transfer to HL
Address 6	—	—	—	Transfer to LL	Transfer to LH
Address 7	—	—	—	—	Transfer to LL

Table 2.3 32-Bit Write Operations when Little Endian has been Selected

Operation / Address of dest	Writing a 32-bit unit to address 0	Writing a 32-bit unit to address 1	Writing a 32-bit unit to address 2	Writing a 32-bit unit to address 3	Writing a 32-bit unit to address 4
Address 0	Transfer from LL	—	—	—	—
Address 1	Transfer from LH	Transfer from LL	—	—	—
Address 2	Transfer from HL	Transfer from LH	Transfer from LL	—	—
Address 3	Transfer from HH	Transfer from HL	Transfer from LH	Transfer from LL	—
Address 4	—	Transfer from HH	Transfer from HL	Transfer from LH	Transfer from LL
Address 5	—	—	Transfer from HH	Transfer from HL	Transfer from LH
Address 6	—	—	—	Transfer from HH	Transfer from HL
Address 7	—	—	—	—	Transfer from HH

Table 2.4 32-Bit Write Operations when Big Endian has been Selected

Operation / Address of dest	Writing a 32-bit unit to address 0	Writing a 32-bit unit to address 1	Writing a 32-bit unit to address 2	Writing a 32-bit unit to address 3	Writing a 32-bit unit to address 4
Address 0	Transfer from HH	—	—	—	—
Address 1	Transfer from HL	Transfer from HH	—	—	—
Address 2	Transfer from LH	Transfer from HL	Transfer from HH	—	—
Address 3	Transfer from LL	Transfer from LH	Transfer from HL	Transfer from HH	—
Address 4	—	Transfer from LL	Transfer from LH	Transfer from HL	Transfer from HH
Address 5	—	—	Transfer from LL	Transfer from LH	Transfer from HL
Address 6	—	—	—	Transfer from LL	Transfer from LH
Address 7	—	—	—	—	Transfer from LL

Table 2.5 16-Bit Read Operations when Little Endian has been Selected

Operation / Address of src	Reading a 16-bit unit from address 0	Reading a 16-bit unit from address 1	Reading a 16-bit unit from address 2	Reading a 16-bit unit from address 3	Reading a 16-bit unit from address 4	Reading a 16-bit unit from address 5	Reading a 16-bit unit from address 6
Address 0	Transfer to LL	—	—	—	—	—	—
Address 1	Transfer to LH	Transfer to LL	—	—	—	—	—
Address 2	—	Transfer to LH	Transfer to LL	—	—	—	—
Address 3	—	—	Transfer to LH	Transfer to LL	—	—	—
Address 4	—	—	—	Transfer to LH	Transfer to LL	—	—
Address 5	—	—	—	—	Transfer to LH	Transfer to LL	—
Address 6	—	—	—	—	—	Transfer to LH	Transfer to LL
Address 7	—	—	—	—	—	—	Transfer to LH

Table 2.6 16-Bit Read Operations when Big Endian has been Selected

Operation / Address of src	Reading a 16-bit unit from address 0	Reading a 16-bit unit from address 1	Reading a 16-bit unit from address 2	Reading a 16-bit unit from address 3	Reading a 16-bit unit from address 4	Reading a 16-bit unit from address 5	Reading a 16-bit unit from address 6
Address 0	Transfer to LH	—	—	—	—	—	—
Address 1	Transfer to LL	Transfer to LH	—	—	—	—	—
Address 2	—	Transfer to LL	Transfer to LH	—	—	—	—
Address 3	—	—	Transfer to LL	Transfer to LH	—	—	—
Address 4	—	—	—	Transfer to LL	Transfer to LH	—	—
Address 5	—	—	—	—	Transfer to LL	Transfer to LH	—
Address 6	—	—	—	—	—	Transfer to LL	Transfer to LH
Address 7	—	—	—	—	—	—	Transfer to LL

Table 2.7 16-Bit Write Operations when Little Endian has been Selected

Operation / Address of dest	Writing a 16-bit unit to address 0	Writing a 16-bit unit to address 1	Writing a 16-bit unit to address 2	Writing a 16-bit unit to address 3	Writing a 16-bit unit to address 4	Writing a 16-bit unit to address 5	Writing a 16-bit unit to address 6
Address 0	Transfer from LL	—	—	—	—	—	—
Address 1	Transfer from LH	Transfer from LL	—	—	—	—	—
Address 2	—	Transfer from LH	Transfer from LL	—	—	—	—
Address 3	—	—	Transfer from LH	Transfer from LL	—	—	—
Address 4	—	—	—	Transfer from LH	Transfer from LL	—	—
Address 5	—	—	—	—	Transfer from LH	Transfer from LL	—
Address 6	—	—	—	—	—	Transfer from LH	Transfer from LL
Address 7	—	—	—	—	—	—	Transfer from LH

Table 2.8 16-Bit Write Operations when Big Endian has been Selected

Operation / Address of dest	Writing a 16-bit unit to address 0	Writing a 16-bit unit to address 1	Writing a 16-bit unit to address 2	Writing a 16-bit unit to address 3	Writing a 16-bit unit to address 4	Writing a 16-bit unit to address 5	Writing a 16-bit unit to address 6
Address 0	Transfer from LH	—	—	—	—	—	—
Address 1	Transfer from LL	Transfer from LH	—	—	—	—	—
Address 2	—	Transfer from LL	Transfer from LH	—	—	—	—
Address 3	—	—	Transfer from LL	Transfer from LH	—	—	—
Address 4	—	—	—	Transfer from LL	Transfer from LH	—	—
Address 5	—	—	—	—	Transfer from LL	Transfer from LH	—
Address 6	—	—	—	—	—	Transfer from LL	Transfer from LH
Address 7	—	—	—	—	—	—	Transfer from LL

Table 2.9 8-Bit Read Operations when Little Endian has been Selected

Operation / Address of src	Reading an 8-bit unit from address 0	Reading an 8-bit unit from address 1	Reading an 8-bit unit from address 2	Reading an 8-bit unit from address 3
Address 0	Transfer to LL	—	—	—
Address 1	—	Transfer to LL	—	—
Address 2	—	—	Transfer to LL	—
Address 3	—	—	—	Transfer to LL

Table 2.10 8-Bit Read Operations when Big Endian has been Selected

Operation / Address of src	Reading an 8-bit unit from address 0	Reading an 8-bit unit from address 1	Reading an 8-bit unit from address 2	Reading an 8-bit unit from address 3
Address 0	Transfer to LL	—	—	—
Address 1	—	Transfer to LL	—	—
Address 2	—	—	Transfer to LL	—
Address 3	—	—	—	Transfer to LL

Table 2.11 8-Bit Write Operations when Little Endian has been Selected

Operation / Address of dest	Writing an 8-bit unit to address 0	Writing an 8-bit unit to address 1	Writing an 8-bit unit to address 2	Writing an 8-bit unit to address 3
Address 0	Transfer from LL	—	—	—
Address 1	—	Transfer from LL	—	—
Address 2	—	—	Transfer from LL	—
Address 3	—	—	—	Transfer from LL

Table 2.12 8-Bit Write Operations when Big Endian has been Selected

Operation / Address of dest	Writing an 8-bit unit to address 0	Writing an 8-bit unit to address 1	Writing an 8-bit unit to address 2	Writing an 8-bit unit to address 3
Address 0	Transfer from LL	—	—	—
Address 1	—	Transfer from LL	—	—
Address 2	—	—	Transfer from LL	—
Address 3	—	—	—	Transfer from LL

2.5.2 Access to I/O Registers

The addresses of I/O registers are fixed, and this is regardless of whether the setting is for little endian or big endian. Accordingly, changes to the endian do not affect access to I/O registers. For the arrangements of I/O registers, refer to the descriptions of registers in the relevant sections.

2.5.3 Notes on Access to I/O Registers

Ensure that access to I/O registers is in accord with the following rules.

- With I/O registers for which a bus width of eight bits is indicated, use instructions having operands of the same width (eight bits). That is, access these registers by using instructions with .B as the size specifier (.size), or with .B or .UB as the size-extension specifier (.memex).
- With I/O registers for which a bus width of 16 bits is indicated, use instructions having operands of the same width (16 bits). That is, access these registers by using instructions with .W as the size specifier (.size), or with .W or .UW as the size-extension specifier (.memex).
- With I/O registers for which a bus width of 32 bits is indicated, use instructions having operands of the same width (32 bits). That is, access these registers by using instructions with .L as the size specifier (.size), or with .L size-extension specifier (.memex).

2.5.4 Data Arrangement

2.5.4.1 Data Arrangement in Registers

Figure 2.6 shows the relation between the sizes of registers and bit numbers.

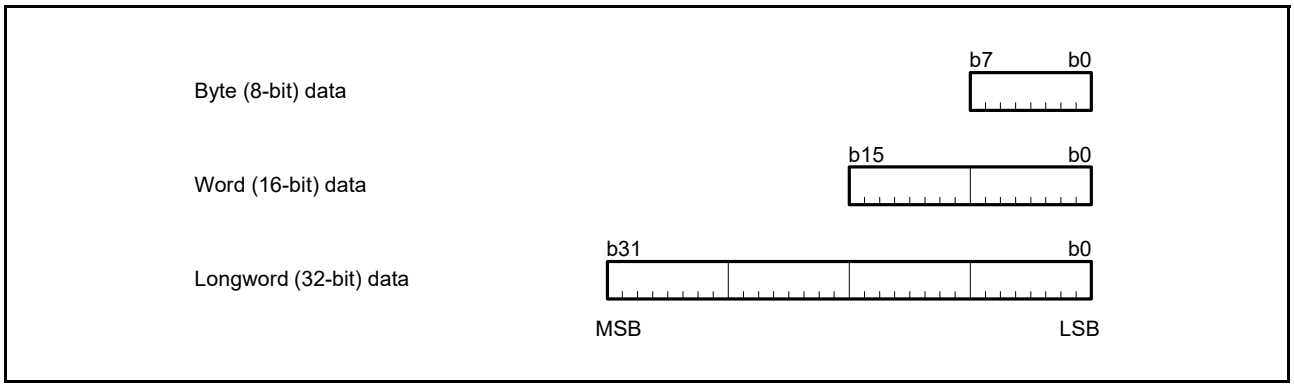


Figure 2.6 Data Arrangement in Registers

2.5.4.2 Data Arrangement in Memory

Data in memory have three sizes: byte (8-bit), word (16-bit), and longword (32-bit). The data arrangement is selectable as little endian or big endian. Figure 2.7 shows the arrangement of data in memory.

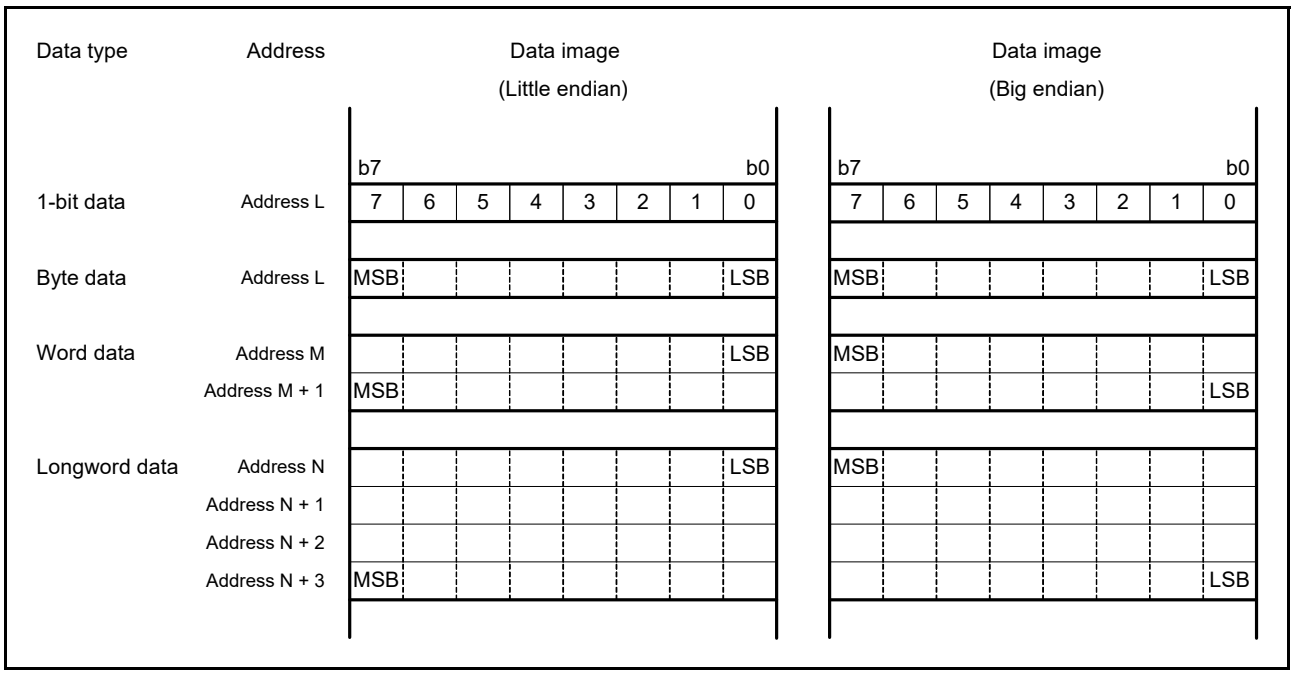


Figure 2.7 Data Arrangement in Memory

2.5.5 Notes on the Allocation of Instruction Codes

The allocation of instruction codes to an external space where the endian differs from that of the chip is prohibited. If the instruction codes are allocated to the external space, they must be allocated to areas where the endian setting is the same as that for the chip.

2.6 Vector Table

There are two types of vector table: exception and interrupt. Each vector in the vector table consists of four bytes and specifies the address where the corresponding exception handling routine starts.

2.6.1 Exception Vector Table

In the exception vector table, the individual vectors for the privileged instruction exception, access exception, undefined instruction exception, floating-point exception, and non-maskable interrupt are allocated to the 124-byte area where the value indicated by the exception table register (EXTB) is used as the starting address (ExtBase). The reset vector is always allocated to FFFFFFFCh, regardless of the value of the exception vector table.
Figure 2.8 shows the exception vector table.

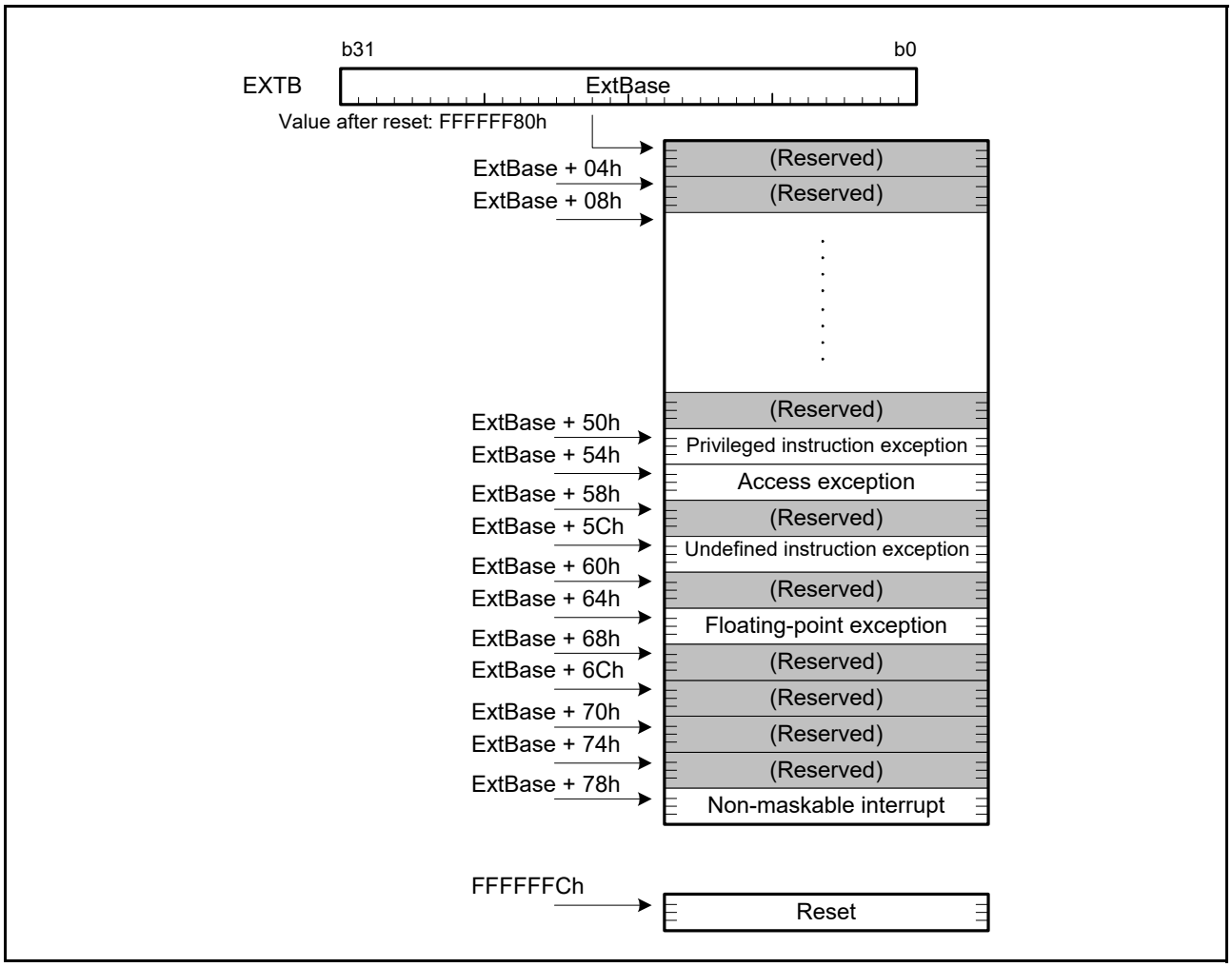


Figure 2.8 Exception Vector Table

2.6.2 Interrupt Vector Table

The address where the interrupt vector table is placed can be adjusted. The table is a 1,024-byte region that contains all vectors for unconditional traps and interrupts and starts at the address (IntBase) specified in the interrupt table register (INTB). Figure 2.9 shows the interrupt vector table.

Each vector in the interrupt vector table has a vector number from 0 to 255. Each of the INT instructions, which act as the sources of unconditional traps, is allocated to the vector that has the same number as is specified as the operand of the instruction itself (from 0 to 255). The BRK instruction is allocated to the vector with number 0. Furthermore, vector numbers (from 0 to 255) are allocated to interrupt requests in a fixed way for each product. For more on interrupt vector numbers, see section 14.3.1, Interrupt Vector Table.

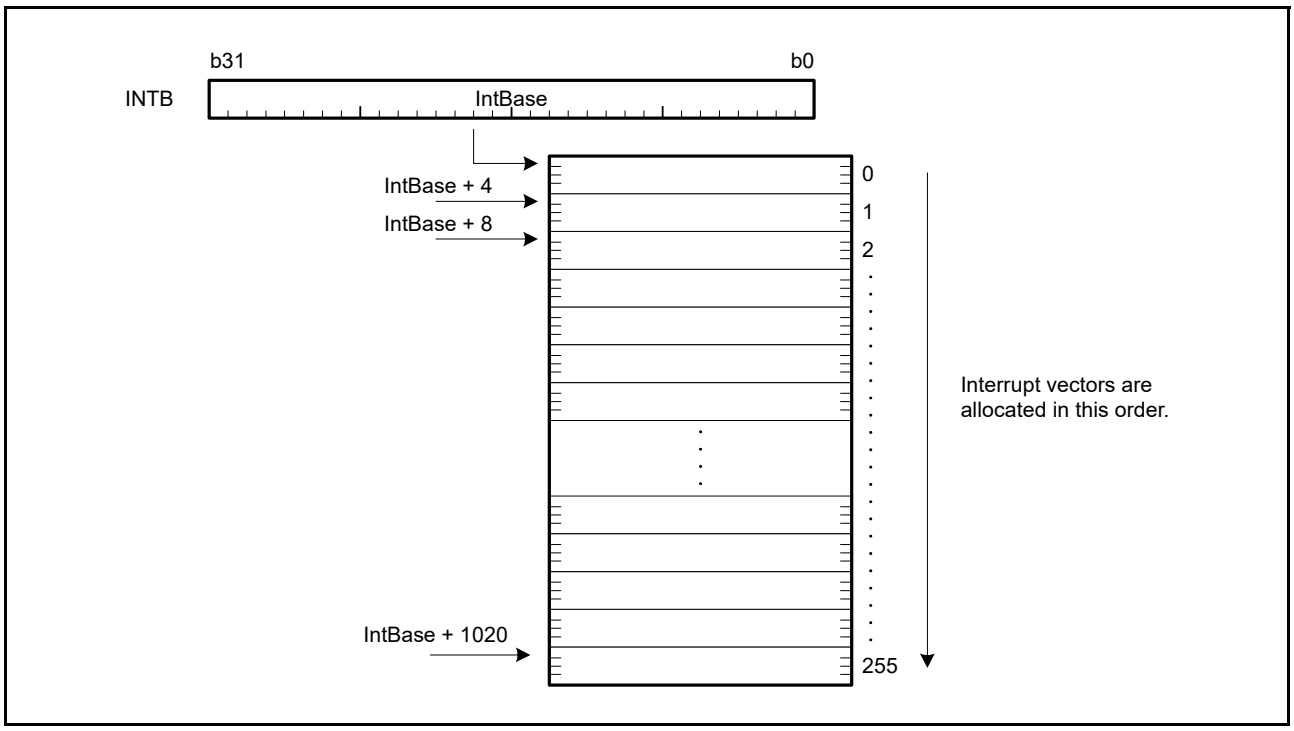


Figure 2.9 Interrupt Vector Table

2.7 Operation of Instructions

2.7.1 Restrictions on RMPA and String-Manipulation Instructions

2.7.1.1 Transfer Size and Data Prefetching

The RMPA instruction and the string-manipulation instructions (SCMPU, SMOVB, SMOVF, SMOVU, SSTR, SUNTIL, and SWHILE instructions) transfer data in longword units to speed up the reading of data from and writing of data to the memory. If the last of the data to be processed is less than a longword, data transfer proceeds with the sizes described below:

- RMPA, SSTR, SUNTIL, and SWHILE instructions: Size specified by the size specifier
- SCMPU, SMOVB, SMOVF, and SMOVU instructions: Byte

Additionally, in the above processing, the RMPA instruction and the string-manipulation instructions other than the SSTR instruction (that is, the SCMPU, SMOVB, SMOVF, SMOVU, SUNTIL, and SWHILE instructions) prefetch data when reading data from the memory. Data is prefetched from the prefetching start position with three bytes as the upper limit. The prefetching start positions of each operation are shown below.

- RMPA instruction: The multiplicand address specified by R1, and the multiplier address specified by R2
- SCMPU instruction: The source address specified by R1 for comparison, and the destination address specified by R2 for comparison
- SUNTIL and SWHILE instructions: The destination address specified by R1 for comparison
- SMOVB, SMOVF, and SMOVU instructions: The source address specified by R2 for transfer

2.7.1.2 Access to I/O Registers

The allocation of data to be handled by RMPA or string-manipulation instructions (SCMPU, SMOVB, SMOVF, SMOVU, SSTR, SUNTIL, and SWHILE instructions) to I/O registers is prohibited, and operation is not guaranteed if this restriction is not observed.

2.8 Number of Cycles

2.8.1 Instruction and Number of Cycle

Table 2.13 to Table 2.20 show the number of cycles in operation of each instruction. The listed numbers of cycles for access to memory are the numbers of cycles during no-wait access. The operands in the table below indicate the following meanings.

#IMM: Immediate
flag: bit, flag
Rs, Rs2, Rd, Rd2, Ri, Rb: General-purpose register
As, Ad: Accumulator
CR: Control register
dsp: displacement
pcdsp: displacement

Table 2.13 Number of Cycles for Arithmetic/logic Instructions

Instruction	Mnemonic (indicates the common operation when the size is omitted)	Number of Cycles
Arithmetic/logic instructions (register-register, immediate-register)	• {ABS, NEG, NOT} “Rd”/“Rs, Rd” • {ADC, MAX, MIN, ROTL, ROTR, XOR} “#IMM, Rd”/“Rs, Rd” • ADD “#IMM, Rd”/“Rs, Rd”/“#IMM, Rs, Rd”/“Rs, Rs2, Rd” • {AND, MUL, OR, SUB} “#IMM, Rd”/“Rs, Rd”/“Rs, Rs2, Rd” • {CMP, TST} “#IMM, Rs”/“Rs, Rs2” • NOP • {ROLC, RORC, SAT} “Rd” • SBB “Rs, Rd” • {SHAR, SHLL, SHLR} “#IMM, Rd”/“Rs, Rd”/“#IMM, Rs, Rd”	1
	• DIV “#IMM, Rd”/“Rs, Rd”	3 to 20*1
	• DIVU “#IMM, Rd”/“Rs, Rd”	2 to 18*1
	• {EMUL, EMULU} “#IMM, Rd”/“Rs, Rd”	2
	• SATR	3
Arithmetic/logic instructions (memory source operand)	• {ADC, ADD, AND, MAX, MIN, MUL, OR, SBB, SUB, XOR} “[Rs], Rd”/“dsp[Rs], Rd” • {CMP, TST} “[Rs], Rs2”/“dsp[Rs], Rs2”	3
	• DIV “[Rs], Rd / dsp[Rs], Rd”	5 to 22
	• DIVU“[Rs], Rd / dsp[Rs], Rd”	4 to 20
	• {EMUL, EMULU} “[Rs], Rd”/“dsp[Rs], Rd”	4
	• RMPA.B	6+7×floor(n/4)+4×(n%4) n: Number of processing bytes*2
	• RMPA.W	6+5×floor(n/2)+4×(n%2) n: Number of processing words*2
	• RMPA.L	6+4n n: Number of processing longwords*2

Note 1. The number of cycles for the dividing instruction varies according to the divisor and dividend.
Note 2. floor (x): Max. integer that is smaller than x.

Table 2.14 Number of Cycles for Transfer Instructions

Instruction	Mnemonic (indicates the common operation when the size is omitted)	Number of Cycles
Transfer instructions (register-register, immediate-register)	• MOV “#IMM, Rd”/“Rs, Rd” • {MOVU, REVL, REVW} “Rs, Rd” • SCC*nd* “Rd” • {STNZ, STZ} “#IMM, Rd”/ “Rs, Rd”	1
	• XCHG “Rs, Rd”	2
Transfer instructions (load operation)	• {MOV, MOVU} “[Rs], Rd”/“dsp[Rs], Rd”/“[Rs+], Rd”/“[-Rs], Rd”/“[Ri, Rb], Rd” • LDL “[Rs], Rd” • POP “Rd”	Throughput: 1 Latency: 2*1
	• POPC “CR”	Throughput: 3 Latency: 4*1
	• POPM “Rd-Rd2”	Throughput: n Latency: n+1 n: Number of registers*1, *2
Transfer instructions (store operation)	• MOV “Rs, [Rd]”/“Rs, dsp[Rd]”/“Rs, [Rd+]”/“Rs, [-Rd]”/“Rs, [Ri, Rb]”/“#IMM, dsp[Rd]”/“#IMM, [Rd]” • PUSH “Rs” • PUSHC “CR” • SCCnd “[Rd]”/“dsp[Rd]” • STC “Rs, [Rd]”	1
	• PUSHM “Rs-Rs2”	n n: Number of registers*3
Transfer instructions (memory-register)	• XCHG “[Rs], Rd”/“dsp[Rs], Rd”	2
Transfer instructions (memory-memory)	• MOV “[Rs], [Rd]”/“dsp[Rs], [Rd]”/“[Rs], dsp[Rd]”/“dsp[Rs], dsp[Rd]” • PUSH “[Rs]”/“dsp[Rs]”	3

Note 1. When the load data is used by the subsequent instruction, the number of cycles described as “latency” is counted as the number of cycles for the memory load instruction. For the cycles other than the memory load instruction, the number of cycles described as “throughput” is counted.

Note 2. The POPM instruction is converted into multiple load operations. The processing is the same as the one for the load operations of the MOV instruction, where the operation is repeated for the number of specified registers.

Note 3. The PUSHM instruction is converted into multiple store operations. The processing is the same as the one for the store operations of the MOV instruction, where the operation is repeated for the number of specified registers.

Table 2.15 Number of Cycles for Bit Manipulation Instructions

Instruction	Mnemonic (indicates the common operation when the size is omitted)	Number of Cycles
Bit manipulation instructions (register)	• {BCLR, BNOT, BSET} “#IMM, Rd”/“Rs, Rd” • BMCnd “#IMM, Rd” • BTST “#IMM, Rs”/“Rs, Rs2”	1
Bit manipulation instructions (memory source operand)	• {BCLR, BNOT, BSET} “#IMM, [Rd]”/“#IMM, dsp[Rd]”/“Rs, [Rd]”/“Rs, dsp[Rd]” • BMCnd “#IMM, [Rd]”/“#IMM, dsp[Rd]” • BTST “#IMM, [Rs]”/“#IMM, dsp[Rs]”/“Rs, [Rs2]”/“Rs, dsp[Rs2]”	3

Table 2.16 Number of Cycles for Branch Instructions

Instruction	Mnemonic (indicates the common operation when the size is omitted)	Number of Cycles
Branch instructions	• B*Cnd* “pcdsp” • {BRA, BSR} “pcdsp”/“Rs” • {JMP, JSR} “Rs”	Branch taken: 3 Branch not taken: 1
	• RTE	6
	• RTFI	3
	• RTS	5
	• RTSD “#IMM”	5
	• RTSD “#IMM, Rd-Rd2”	Throughput: n<5?5:1+n Latency: n<4?5:2+n n: Number of registers*1

?: Conditional operator

Note 1. When the load data is used by the subsequent instruction, the number of cycles described as “latency” is counted as the number of cycles for the memory load instruction. For the cycles other than the memory load instruction, the number of cycles described as “throughput” is counted.

Table 2.17 Number of Cycles for Floating-Point Operation Instructions

Instruction	Mnemonic (indicates the common operation when the size is omitted)	Number of Cycles
Floating-point operation instructions (register-register, immediate-register)	• {FADD, FSUB} “#IMM, Rd”/ “Rs, Rd”/ “Rs, Rs2, Rd”	2
	• FCMP “#IMM, Rs”/“Rs, Rs2”	1
	• FDIV “#IMM, Rd”/“Rs, Rd”	16
	• FMUL “#IMM, Rd”/ “Rs, Rd” / “Rs, Rs2, Rd”	2
	• FSQRT “Rs, Rd”	16
	• {FTOI, ROUND, ITOF} “Rs, Rd”	2
	• {FTOU, UTOF} “Rs, Rd”	2
Floating-point operation instructions (memory source operand)	• {FADD, FSUB} “[Rs], Rd”/“dsp[Rs], Rd”	4
	• FCMP “[Rs], Rs2”/“dsp[Rs], Rs2”	3
	• FDIV “[Rs], Rd”/“dsp[Rs], Rd”	18
	• FMUL “[Rs], Rd”/“dsp[Rs], Rd”	4
	• FSQRT “[Rs], Rd”/“dsp[Rs], Rd”	18
	• {FTOI, ROUND, ITOF} “[Rs], Rd”/“dsp[Rs], Rd”	4
	• {FTOU, UTOF} “[Rs], Rd”/“dsp[Rs], Rd”	4

Table 2.18 Number of Cycles for DSP Instructions

Instruction	Mnemonic (indicates the common operation when the size is omitted)	Number of Cycles
DSP instructions	• {EMULA, EMACA, EMSBA, MULLH, MULHI, MULLO, MACLH, MACHI, MACLO, MSBLH, MSBHI, MSBLO}“Rs, Rs2, Ad” • {MVFACHI, MVFACMI, MVFACLO, MVFACGU} “#IMM, As, Rd” • {MVTACHI, MVTACLO, MVTACGU} “As, Rd” • {RDACW, RDACL, RACW, RACL} “#IMM, Ad”	1

Table 2.19 Number of Cycles for String Manipulation Instructions

Instruction	Mnemonic (indicates the common operation when the size is omitted)	Number of Cycles
String manipulation instructions*1	• SCMPU	2+4×floor(n/4)+4×(n%4) n: Number of comparison bytes*2
	• SMOVB	n>3?6+3×floor(n/4)+3×(n%4):2+3n n: Number of transfer bytes*2
	• SMOVF, SMOVU	2+3×floor(n/4)+3×(n%4) n: Number of transfer bytes*2
	• SSTR.B	2+floor(n/4)+n%4 n: Number of transfer bytes*2
	• SSTR.W	2+floor(n/2)+n%2 n: Number of transfer words*2
	• SSTR.L	2+n n: Number of transfer longwords
	• SUNTIL.B, SWHILE.B	3+3×floor(n/4)+3×(n%4) n: Number of comparison bytes*2
	• SUNTIL.W, SWHILE.W	3+3×floor(n/2)+3×(n%2) n: Number of comparison words*2
	• SUNTIL.L, SWHILE.L	3+3×n n: Number of comparison longwords

?: Conditional operator

Note 1. Each of the SCMPU, SMOVU, SWHILE, and SUNTIL instructions ends the execution regardless of the specified cycles, if the end condition is satisfied during execution.
Note 2. floor (x): Max. integer that is smaller than x.

Table 2.20 Number of Cycles for System Manipulation Instructions

Instruction	Mnemonic (indicates the common operation when the size is omitted)	Number of Cycles
System manipulation instructions	• {CLRPSW, SETPSW}“flag” • MVTC “#IMM, CR”/“Rs, CR” • MVFC “CR, Rd” • MVTIPL “#IMM”	1
	• RTE	6
	• RTFI	3

2.8.2 Numbers of Cycles for Response to Interrupts

Table 2.21 lists numbers of cycles taken by processing for response to interrupts.

Table 2.21 Numbers of Cycles for Response to Interrupts

Type of Interrupt Request/Details of Processing	Fast Interrupt	Other Interrupts
ICU Judgment of priority order	2 cycles	
CPU Number of cycles from notification to acceptance of the interrupt request	N cycles (varies with the instruction being executed at the time the interrupt was received)	
CPU Pre-processing by hardware Saving the current PC and PSW values in RAM (or in control registers in the case of the fast interrupt) Reading of the vector Branching to the start of the exception handling routine	4 cycles	6 cycles

Times calculated from the values in Table 2.21 will be applicable when access to memory from the CPU is processed with no waiting. The RAM and code flash memory in this MCU allow such access. Numbers of cycles for response to interrupts can be minimized by placing program code (and vectors) in code flash memory and the stack in RAM. Furthermore, place the addresses where the exception handling routine start on 8-byte boundaries.
For information on the number of cycles from notification to acceptance of the interrupt request, indicated by N in the table above, see Table 2.13 to Table 2.20.
The timing of interrupt acceptance depends on the execution state of the instruction. For more information on this, see section 13.3.1, Acceptance Timing and Saved PC Value.

3. Operating Modes

3.1 Operating Mode Types and Selection

There are two types of operating-mode selection: one is be selected by the level on pins at the time of release from the reset state, and the other is selected by software after release from the reset state.

Table 3.1 shows the relationship between levels on the mode-setting pins (MD) on release from the reset state and the operating mode selected at that time. For details on each of the operating modes, see section 3.3, Details of Operating Modes.

Table 3.1 Selection of Operating Modes by the Mode-Setting Pins

Mode-Setting Pin	
MD*1	**Operating Mode**
Low	Boot mode (SCI)
High	Single-chip mode

Note 1. Do not change the level on the MD pin while the MCU is operating.

The endian is selectable in single-chip mode. Endian is set by the MDE.MDE[2:0] bits in the option-setting memory. For the correspondence between the setting and endian, see Table 3.2.

Table 3.2 Selection of Endian

MDE.MDE[2:0] Bit Setting	Endian
000b	Big endian
111b	Little endian

3.2 Register Descriptions

3.2.1 Mode Monitor Register (MDMONR)

Address(es): 0008 0000h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MD
Value after reset:	0	0	0	0	0	0	0	x	0	0	0	0	0	0	0	0/1*1

Note 1. This affects the level on the MD pin at the time of release from the reset state.

Bit	Symbol	Bit Name	Description	R/W
b0	MD	MD Pin Status Flag	0: The MD pin is low. 1: The MD pin is high.	R
b7 to b1	—	Reserved	These bits are read as 0.	R
b8	—	Reserved	The read value is undefined.	R
b15 to b9	—	Reserved	These bits are read as 0.	R

3.2.2 System Control Register 1 (SYSCR1)

Address(es): 0008 0008h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RAME
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	RAME	RAM Enable	0: The RAM is disabled. 1: The RAM is enabled.	R/W
b15 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

RAME Bit (RAM Enable)

The RAME bit enables or disables the RAM.

A 0 should not be written to this bit during access to the RAM. When accessing the RAM immediately after changing the RAME bit from 0 (RAM disabled) to 1 (RAM enabled), make sure that the RAME bit is 1 before the access.

3.3 Details of Operating Modes

3.3.1 Single-Chip Mode

In this mode, all I/O ports can be used as general input/output ports, peripheral function input/output, or interrupt input pins.
The chip starts up in single-chip mode if the high level is on the MD pin on release from the reset state.

3.3.2 Boot Mode

In this mode, the on-chip flash memory modifying program (boot program) stored in a dedicated area within the MCU operates. The on-chip flash memory (ROM and E2 DataFlash) can be modified from outside the MCU by using a universal asynchronous receiver/transmitter (SCI1). For details, see section 36, Flash Memory.
When a reset is released while the MD pin is low, boot mode is selected.

3.3.2.1 Boot Mode (SCI)

When a reset is released while the MD pin is low, boot mode (SCI) is selected. For details on boot mode (SCI), refer to section 36.8.1, Boot Mode (SCI).

3.4 Transitions of Operating Modes

3.4.1 Operating Mode Transitions Determined by the Mode-Setting Pins

Figure 3.1 shows operating mode transitions determined by the settings of the MD pin.

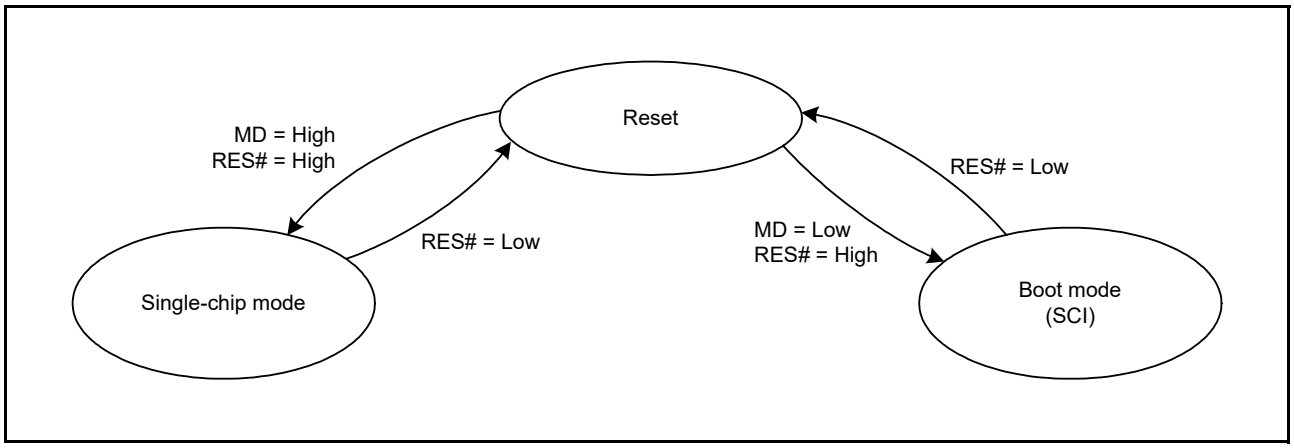
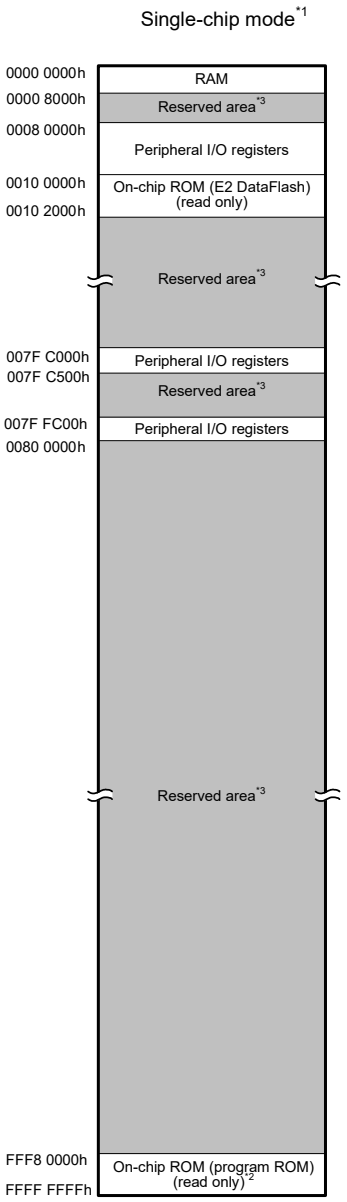


Figure 3.1 Mode-Setting Pin Levels and Operating Modes

4. Address Space

4.1 Address Space

This MCU has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.
Figure 4.1 shows the memory maps.



Note 1. The address space in boot mode is the same as the address space in single-chip mode.
Note 2. The capacity of ROM differs depending on the products.

ROM (bytes)		RAM (bytes)		E2 DataFlash (bytes)	
Capacity	**Address**	**Capacity**	**Address**	**Capacity**	**Address**
512 K	FFF8 0000h to FFFF FFFFh	32 K	0000 0000h to 0000 7FFFh	8 K	0010 0000h to 0010 1FFFh
384 K	FFFA 0000h to FFFF FFFFh				
256 K	FFFC 0000h to FFFF FFFFh				

Note: See Table 1.3 List of Products, for the product type name.

Note 3. Reserved areas should not be accessed.

Figure 4.1 Memory Map in Each Operating Mode

5. I/O Registers

This section provides information on the on-chip I/O register addresses and bit configuration. The information is given as shown below. Notes on writing to registers are also given below.

(1) I/O register addresses (address order)

- Registers are listed from the lower allocation addresses.
- Registers are classified according to module symbols.
- Numbers of cycles for access indicate numbers of cycles of the given base clock.
- Among the internal I/O register area, addresses not listed in the list of registers are reserved. Reserved addresses must not be accessed. Do not access these addresses; otherwise, the operation when accessing these bits and subsequent operations cannot be guaranteed.

(2) Notes on writing to I/O registers

When writing to an I/O register, the CPU starts executing the subsequent instruction before completing I/O register write. This may cause the subsequent instruction to be executed before the post-update I/O register value is reflected on the operation.
As described in the following examples, special care is required for the cases in which the subsequent instruction must be executed after the post-update I/O register value is actually reflected.

[Examples of cases requiring special care]

- The subsequent instruction must be executed while an interrupt request is disabled with the IENj bit in IERn of the ICU (interrupt request enable bit) cleared to 0.
- A WAIT instruction is executed immediately after the preprocessing for causing a transition to the low power consumption state.

In the above cases, after writing to an I/O register, wait until the write operation is completed using the following procedure and then execute the subsequent instruction.

(a) Write to an I/O register.
(b) Read the value from the I/O register to a general register.
(c) Execute the operation using the value read.
(d) Execute the subsequent instruction.

[Instruction examples]

- Byte-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.B  #SFR_DATA, [R1]
CMP    [R1].UB, R1
;; Next process
```

- Word-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.W  #SFR_DATA, [R1]
CMP    [R1].W, R1
;; Next process
```

- Longword-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.L  #SFR_DATA, [R1]
CMP    [R1].L, R1
;; Next process
```

If multiple registers are written to and a subsequent instruction should be executed after the write operations are entirely completed, only read the I/O register that was last written to and execute the operation using the value; it is not necessary to read or execute operation for all the registers that were written to.

(3) Number of Access Cycles to I/O Registers

For numbers of clock cycles for access to I/O registers, see Table 5.1, List of I/O Registers (Address Order).
The number of access cycles to I/O registers is obtained by following equation.*1

Number of access cycles to I/O registers = Number of bus cycles for internal main bus 1 +
Number of divided clock synchronization cycles +
Number of bus cycles for internal peripheral bus 1 to 6

The number of bus cycles of internal peripheral bus 1 to 6 differs according to the register to be accessed.
When peripheral functions connected to internal peripheral bus 2 to 6 are accessed, the number of divided clock synchronization cycles is added.
In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access cycles shown in Table 5.1.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with the bus access from the different bus master (DTC).

(4) Restrictions in Relation to RMPA and String-Manipulation Instructions

The allocation of data to be handled by RMPA or string-manipulation instructions to I/O registers is prohibited, and operation is not guaranteed if this restriction is not observed.

(5) Notes on Sleep Mode and Mode Transitions

During sleep mode or mode transitions, do not write to the system control related registers (indicated by ‘SYSTEM’ in the Module Symbol column in Table 5.1, List of I/O Registers (Address Order)).

5.1 I/O Register Addresses (Address Order)

Table 5.1 List of I/O Registers (Address Order) (1/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Reference Section
0008 0000h	SYSTEM	Mode Monitor Register	MDMONR	16	16	3 ICLK	section 3.
0008 0008h	SYSTEM	System Control Register 1	SYSCR1	16	16	3 ICLK	section 3.
0008 000Ch	SYSTEM	Standby Control Register	SBYCR	16	16	3 ICLK	section 11.
0008 0010h	SYSTEM	Module Stop Control Register A	MSTPCRA	32	32	3 ICLK	section 11.
0008 0014h	SYSTEM	Module Stop Control Register B	MSTPCRB	32	32	3 ICLK	section 11.
0008 0018h	SYSTEM	Module Stop Control Register C	MSTPCRC	32	32	3 ICLK	section 11.
0008 0020h	SYSTEM	System Clock Control Register	SCKCR	32	32	3 ICLK	section 9.
0008 0026h	SYSTEM	System Clock Control Register 3	SCKCR3	16	16	3 ICLK	section 9.
0008 0028h	SYSTEM	PLL Control Register	PLLCR	16	16	3 ICLK	section 9.
0008 002Ah	SYSTEM	PLL Control Register 2	PLLCR2	8	8	3 ICLK	section 9.
0008 0031h	SYSTEM	Memory Wait Cycle Setting Register	MEMWAIT	8	8	3 ICLK	section 9.
0008 0032h	SYSTEM	Main Clock Oscillator Control Register	MOSCCR	8	8	3 ICLK	section 9.
0008 0034h	SYSTEM	Low-Speed On-Chip Oscillator Control Register	LOCOCR	8	8	3 ICLK	section 9.
0008 0035h	SYSTEM	IWDT-Dedicated On-Chip Oscillator Control Register	ILOCOCR	8	8	3 ICLK	section 9.
0008 0036h	SYSTEM	High-Speed On-Chip Oscillator Control Register	HOCOCR	8	8	3 ICLK	section 9.
0008 0037h	SYSTEM	High-Speed On-Chip Oscillator Control Register 2	HOCOCR2	8	8	3 ICLK	section 9.
0008 003Ch	SYSTEM	Oscillation Stabilization Flag Register	OSCOVFSR	8	8	3 ICLK	section 9.
0008 0040h	SYSTEM	Oscillation Stop Detection Control Register	OSTDCR	8	8	3 ICLK	section 9.
0008 0041h	SYSTEM	Oscillation Stop Detection Status Register	OSTDSR	8	8	3 ICLK	section 9.
0008 00A0h	SYSTEM	Operating Power Control Register	OPCCR	8	8	3 ICLK	section 11.
0008 00A2h	SYSTEM	Main Clock Oscillator Wait Control Register	MOSCWTCR	8	8	3 ICLK	section 9.
0008 00A5h	SYSTEM	High-Speed On-Chip Oscillator Wait Control Register	HOCOWTCR	8	8	3 ICLK	section 9.
0008 00C0h	SYSTEM	Reset Status Register 2	RSTSR2	8	8	3 ICLK	section 6.
0008 00C2h	SYSTEM	Software Reset Register	SWRR	16	16	3 ICLK	section 6.
0008 00E0h	SYSTEM	Voltage Monitoring 1 Circuit Control Register 1	LVD1CR1	8	8	3 ICLK	section 8.
0008 00E1h	SYSTEM	Voltage Monitoring 1 Circuit Status Register	LVD1SR	8	8	3 ICLK	section 8.
0008 00E2h	SYSTEM	Voltage Monitoring 2 Circuit Control Register 1	LVD2CR1	8	8	3 ICLK	section 8.
0008 00E3h	SYSTEM	Voltage Monitoring 2 Circuit Status Register	LVD2SR	8	8	3 ICLK	section 8.
0008 03FEh	SYSTEM	Protect Register	PRCR	16	16	3 ICLK	section 12.
0008 1000h	FLASH	ROM Cache Enable Register	ROMCE	16	16	3 ICLK	section 36.
0008 1004h	FLASH	ROM Cache Invalidate Register	ROMCIV	16	16	3 ICLK	section 36.
0008 1300h	BSC	Bus Error Status Clear Register	BERCLR	8	8	2 ICLK	section 15.
0008 1304h	BSC	Bus Error Monitoring Enable Register	BEREN	8	8	2 ICLK	section 15.
0008 1308h	BSC	Bus Error Status Register 1	BERSR1	8	8	2 ICLK	section 15.
0008 130Ah	BSC	Bus Error Status Register 2	BERSR2	16	16	2 ICLK	section 15.
0008 1310h	BSC	Bus Priority Control Register	BUSPRI	16	16	2 ICLK	section 15.
0008 2400h	DTC	DTC Control Register	DTCCR	8	8	2 ICLK	section 17.
0008 2404h	DTC	DTC Vector Base Register	DTCVBR	32	32	2 ICLK	section 17.
0008 2408h	DTC	DTC Address Mode Register	DTCADMOD	8	8	2 ICLK	section 17.
0008 240Ch	DTC	DTC Module Start Register	DTCST	8	8	2 ICLK	section 17.
0008 240Eh	DTC	DTC Status Register	DTCSTS	16	16	2 ICLK	section 17.
0008 6400h	MPU	Region-0 Start Page Number Register	RSPAGE0	32	32	1 ICLK	section 16.
0008 6404h	MPU	Region-0 End Page Number Register	REPAGE0	32	32	1 ICLK	section 16.
0008 6408h	MPU	Region-1 Start Page Number Register	RSPAGE1	32	32	1 ICLK	section 16.
0008 640Ch	MPU	Region-1 End Page Number Register	REPAGE1	32	32	1 ICLK	section 16.
0008 6410h	MPU	Region-2 Start Page Number Register	RSPAGE2	32	32	1 ICLK	section 16.
0008 6414h	MPU	Region-2 End Page Number Register	REPAGE2	32	32	1 ICLK	section 16.
0008 6418h	MPU	Region-3 Start Page Number Register	RSPAGE3	32	32	1 ICLK	section 16.
0008 641Ch	MPU	Region-3 End Page Number Register	REPAGE3	32	32	1 ICLK	section 16.

Table 5.1 List of I/O Registers (Address Order) (2/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Reference Section
0008 6420h	MPU	Region-4 Start Page Number Register	RSPAGE4	32	32	1 ICLK	section 16.
0008 6424h	MPU	Region-4 End Page Number Register	REPAGE4	32	32	1 ICLK	section 16.
0008 6428h	MPU	Region-5 Start Page Number Register	RSPAGE5	32	32	1 ICLK	section 16.
0008 642Ch	MPU	Region-5 End Page Number Register	REPAGE5	32	32	1 ICLK	section 16.
0008 6430h	MPU	Region-6 Start Page Number Register	RSPAGE6	32	32	1 ICLK	section 16.
0008 6434h	MPU	Region-6 End Page Number Register	REPAGE6	32	32	1 ICLK	section 16.
0008 6438h	MPU	Region-7 Start Page Number Register	RSPAGE7	32	32	1 ICLK	section 16.
0008 643Ch	MPU	Region-7 End Page Number Register	REPAGE7	32	32	1 ICLK	section 16.
0008 6500h	MPU	Memory-Protection Enable Register	MPEN	32	32	1 ICLK	section 16.
0008 6504h	MPU	Background Access Control Register	MPBAC	32	32	1 ICLK	section 16.
0008 6508h	MPU	Memory-Protection Error Status-Clearing Register	MPECLR	32	32	1 ICLK	section 16.
0008 650Ch	MPU	Memory-Protection Error Status Register	MPESTS	32	32	1 ICLK	section 16.
0008 6514h	MPU	Data Memory-Protection Error Address Register	MPDEA	32	32	1 ICLK	section 16.
0008 6520h	MPU	Region Search Address Register	MPSA	32	32	1 ICLK	section 16.
0008 6524h	MPU	Region Search Operation Register	MPOPS	16	16	1 ICLK	section 16.
0008 6526h	MPU	Region Invalidation Operation Register	MPOPI	16	16	1 ICLK	section 16.
0008 6528h	MPU	Instruction-Hit Region Register	MHITI	32	32	1 ICLK	section 16.
0008 652Ch	MPU	Data-Hit Region Register	MHITD	32	32	1 ICLK	section 16.
0008 7010h	ICU	Interrupt Request Register 016	IR016	8	8	2 ICLK	section 14.
0008 7017h	ICU	Interrupt Request Register 023	IR023	8	8	2 ICLK	section 14.
0008 701Bh	ICU	Interrupt Request Register 027	IR027	8	8	2 ICLK	section 14.
0008 701Ch	ICU	Interrupt Request Register 028	IR028	8	8	2 ICLK	section 14.
0008 701Dh	ICU	Interrupt Request Register 029	IR029	8	8	2 ICLK	section 14.
0008 701Eh	ICU	Interrupt Request Register 030	IR030	8	8	2 ICLK	section 14.
0008 701Fh	ICU	Interrupt Request Register 031	IR031	8	8	2 ICLK	section 14.
0008 7020h	ICU	Interrupt Request Register 032	IR032	8	8	2 ICLK	section 14.
0008 7021h	ICU	Interrupt Request Register 033	IR033	8	8	2 ICLK	section 14.
0008 7022h	ICU	Interrupt Request Register 034	IR034	8	8	2 ICLK	section 14.
0008 7028h	ICU	Interrupt Request Register 040	IR040	8	8	2 ICLK	section 14.
0008 7029h	ICU	Interrupt Request Register 041	IR041	8	8	2 ICLK	section 14.
0008 702Ch	ICU	Interrupt Request Register 044	IR044	8	8	2 ICLK	section 14.
0008 702Dh	ICU	Interrupt Request Register 045	IR045	8	8	2 ICLK	section 14.
0008 702Eh	ICU	Interrupt Request Register 046	IR046	8	8	2 ICLK	section 14.
0008 702Fh	ICU	Interrupt Request Register 047	IR047	8	8	2 ICLK	section 14.
0008 7030h	ICU	Interrupt Request Register 048	IR048	8	8	2 ICLK	section 14.
0008 7031h	ICU	Interrupt Request Register 049	IR049	8	8	2 ICLK	section 14.
0008 7032h	ICU	Interrupt Request Register 050	IR050	8	8	2 ICLK	section 14.
0008 7033h	ICU	Interrupt Request Register 051	IR051	8	8	2 ICLK	section 14.
0008 7034h	ICU	Interrupt Request Register 052	IR052	8	8	2 ICLK	section 14.
0008 7035h	ICU	Interrupt Request Register 053	IR053	8	8	2 ICLK	section 14.
0008 7036h	ICU	Interrupt Request Register 054	IR054	8	8	2 ICLK	section 14.
0008 7037h	ICU	Interrupt Request Register 055	IR055	8	8	2 ICLK	section 14.
0008 7038h	ICU	Interrupt Request Register 056	IR056	8	8	2 ICLK	section 14.
0008 7039h	ICU	Interrupt Request Register 057	IR057	8	8	2 ICLK	section 14.
0008 703Bh	ICU	Interrupt Request Register 059	IR059	8	8	2 ICLK	section 14.
0008 703Ch	ICU	Interrupt Request Register 060	IR060	8	8	2 ICLK	section 14.
0008 703Dh	ICU	Interrupt Request Register 061	IR061	8	8	2 ICLK	section 14.
0008 703Eh	ICU	Interrupt Request Register 062	IR062	8	8	2 ICLK	section 14.
0008 703Fh	ICU	Interrupt Request Register 063	IR063	8	8	2 ICLK	section 14.
0008 7040h	ICU	Interrupt Request Register 064	IR064	8	8	2 ICLK	section 14.
0008 7041h	ICU	Interrupt Request Register 065	IR065	8	8	2 ICLK	section 14.

Table 5.1 List of I/O Registers (Address Order) (3/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Reference Section
0008 7042h	ICU	Interrupt Request Register 066	IR066	8	8	2 ICLK	section 14.
0008 7043h	ICU	Interrupt Request Register 067	IR067	8	8	2 ICLK	section 14.
0008 7044h	ICU	Interrupt Request Register 068	IR068	8	8	2 ICLK	section 14.
0008 7045h	ICU	Interrupt Request Register 069	IR069	8	8	2 ICLK	section 14.
0008 7046h	ICU	Interrupt Request Register 070	IR070	8	8	2 ICLK	section 14.
0008 7047h	ICU	Interrupt Request Register 071	IR071	8	8	2 ICLK	section 14.
0008 7058h	ICU	Interrupt Request Register 088	IR088	8	8	2 ICLK	section 14.
0008 7059h	ICU	Interrupt Request Register 089	IR089	8	8	2 ICLK	section 14.
0008 7062h	ICU	Interrupt Request Register 098	IR098	8	8	2 ICLK	section 14.
0008 7063h	ICU	Interrupt Request Register 099	IR099	8	8	2 ICLK	section 14.
0008 7064h	ICU	Interrupt Request Register 100	IR100	8	8	2 ICLK	section 14.
0008 7065h	ICU	Interrupt Request Register 101	IR101	8	8	2 ICLK	section 14.
0008 7066h	ICU	Interrupt Request Register 102	IR102	8	8	2 ICLK	section 14.
0008 7067h	ICU	Interrupt Request Register 103	IR103	8	8	2 ICLK	section 14.
0008 7068h	ICU	Interrupt Request Register 104	IR104	8	8	2 ICLK	section 14.
0008 7069h	ICU	Interrupt Request Register 105	IR105	8	8	2 ICLK	section 14.
0008 706Ah	ICU	Interrupt Request Register 106	IR106	8	8	2 ICLK	section 14.
0008 706Bh	ICU	Interrupt Request Register 107	IR107	8	8	2 ICLK	section 14.
0008 706Ch	ICU	Interrupt Request Register 108	IR108	8	8	2 ICLK	section 14.
0008 706Dh	ICU	Interrupt Request Register 109	IR109	8	8	2 ICLK	section 14.
0008 706Eh	ICU	Interrupt Request Register 110	IR110	8	8	2 ICLK	section 14.
0008 706Fh	ICU	Interrupt Request Register 111	IR111	8	8	2 ICLK	section 14.
0008 7070h	ICU	Interrupt Request Register 112	IR112	8	8	2 ICLK	section 14.
0008 7071h	ICU	Interrupt Request Register 113	IR113	8	8	2 ICLK	section 14.
0008 7072h	ICU	Interrupt Request Register 114	IR114	8	8	2 ICLK	section 14.
0008 7073h	ICU	Interrupt Request Register 115	IR115	8	8	2 ICLK	section 14.
0008 7074h	ICU	Interrupt Request Register 116	IR116	8	8	2 ICLK	section 14.
0008 7075h	ICU	Interrupt Request Register 117	IR117	8	8	2 ICLK	section 14.
0008 7076h	ICU	Interrupt Request Register 118	IR118	8	8	2 ICLK	section 14.
0008 7077h	ICU	Interrupt Request Register 119	IR119	8	8	2 ICLK	section 14.
0008 7078h	ICU	Interrupt Request Register 120	IR120	8	8	2 ICLK	section 14.
0008 7079h	ICU	Interrupt Request Register 121	IR121	8	8	2 ICLK	section 14.
0008 707Ah	ICU	Interrupt Request Register 122	IR122	8	8	2 ICLK	section 14.
0008 707Bh	ICU	Interrupt Request Register 123	IR123	8	8	2 ICLK	section 14.
0008 707Ch	ICU	Interrupt Request Register 124	IR124	8	8	2 ICLK	section 14.
0008 707Dh	ICU	Interrupt Request Register 125	IR125	8	8	2 ICLK	section 14.
0008 707Eh	ICU	Interrupt Request Register 126	IR126	8	8	2 ICLK	section 14.
0008 707Fh	ICU	Interrupt Request Register 127	IR127	8	8	2 ICLK	section 14.
0008 7080h	ICU	Interrupt Request Register 128	IR128	8	8	2 ICLK	section 14.
0008 7081h	ICU	Interrupt Request Register 129	IR129	8	8	2 ICLK	section 14.
0008 7082h	ICU	Interrupt Request Register 130	IR130	8	8	2 ICLK	section 14.
0008 7083h	ICU	Interrupt Request Register 131	IR131	8	8	2 ICLK	section 14.
0008 7084h	ICU	Interrupt Request Register 132	IR132	8	8	2 ICLK	section 14.
0008 7085h	ICU	Interrupt Request Register 133	IR133	8	8	2 ICLK	section 14.
0008 7086h	ICU	Interrupt Request Register 134	IR134	8	8	2 ICLK	section 14.
0008 7087h	ICU	Interrupt Request Register 135	IR135	8	8	2 ICLK	section 14.
0008 7088h	ICU	Interrupt Request Register 136	IR136	8	8	2 ICLK	section 14.
0008 7089h	ICU	Interrupt Request Register 137	IR137	8	8	2 ICLK	section 14.
0008 708Ah	ICU	Interrupt Request Register 138	IR138	8	8	2 ICLK	section 14.
0008 708Bh	ICU	Interrupt Request Register 139	IR139	8	8	2 ICLK	section 14.
0008 708Ch	ICU	Interrupt Request Register 140	IR140	8	8	2 ICLK	section 14.

Table 5.1 List of I/O Registers (Address Order) (4/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Reference Section
0008 708Dh	ICU	Interrupt Request Register 141	IR141	8	8	2 ICLK	section 14.
0008 708Eh	ICU	Interrupt Request Register 142	IR142	8	8	2 ICLK	section 14.
0008 708Fh	ICU	Interrupt Request Register 143	IR143	8	8	2 ICLK	section 14.
0008 7090h	ICU	Interrupt Request Register 144	IR144	8	8	2 ICLK	section 14.
0008 7091h	ICU	Interrupt Request Register 145	IR145	8	8	2 ICLK	section 14.
0008 7092h	ICU	Interrupt Request Register 146	IR146	8	8	2 ICLK	section 14.
0008 7095h	ICU	Interrupt Request Register 149	IR149	8	8	2 ICLK	section 14.
0008 7096h	ICU	Interrupt Request Register 150	IR150	8	8	2 ICLK	section 14.
0008 7097h	ICU	Interrupt Request Register 151	IR151	8	8	2 ICLK	section 14.
0008 7098h	ICU	Interrupt Request Register 152	IR152	8	8	2 ICLK	section 14.
0008 7099h	ICU	Interrupt Request Register 153	IR153	8	8	2 ICLK	section 14.
0008 709Fh	ICU	Interrupt Request Register 159	IR159	8	8	2 ICLK	section 14.
0008 70A0h	ICU	Interrupt Request Register 160	IR160	8	8	2 ICLK	section 14.
0008 70A1h	ICU	Interrupt Request Register 161	IR161	8	8	2 ICLK	section 14.
0008 70A2h	ICU	Interrupt Request Register 162	IR162	8	8	2 ICLK	section 14.
0008 70A3h	ICU	Interrupt Request Register 163	IR163	8	8	2 ICLK	section 14.
0008 70A4h	ICU	Interrupt Request Register 164	IR164	8	8	2 ICLK	section 14.
0008 70A5h	ICU	Interrupt Request Register 165	IR165	8	8	2 ICLK	section 14.
0008 70A8h	ICU	Interrupt Request Register 168	IR168	8	8	2 ICLK	section 14.
0008 70A9h	ICU	Interrupt Request Register 169	IR169	8	8	2 ICLK	section 14.
0008 70AAh	ICU	Interrupt Request Register 170	IR170	8	8	2 ICLK	section 14.
0008 70ABh	ICU	Interrupt Request Register 171	IR171	8	8	2 ICLK	section 14.
0008 70ACh	ICU	Interrupt Request Register 172	IR172	8	8	2 ICLK	section 14.
0008 70ADh	ICU	Interrupt Request Register 173	IR173	8	8	2 ICLK	section 14.
0008 70AEh	ICU	Interrupt Request Register 174	IR174	8	8	2 ICLK	section 14.
0008 70AFh	ICU	Interrupt Request Register 175	IR175	8	8	2 ICLK	section 14.
0008 70B0h	ICU	Interrupt Request Register 176	IR176	8	8	2 ICLK	section 14.
0008 70B1h	ICU	Interrupt Request Register 177	IR177	8	8	2 ICLK	section 14.
0008 70B2h	ICU	Interrupt Request Register 178	IR178	8	8	2 ICLK	section 14.
0008 70B3h	ICU	Interrupt Request Register 179	IR179	8	8	2 ICLK	section 14.
0008 70B4h	ICU	Interrupt Request Register 180	IR180	8	8	2 ICLK	section 14.
0008 70B5h	ICU	Interrupt Request Register 181	IR181	8	8	2 ICLK	section 14.
0008 70B6h	ICU	Interrupt Request Register 182	IR182	8	8	2 ICLK	section 14.
0008 70B7h	ICU	Interrupt Request Register 183	IR183	8	8	2 ICLK	section 14.
0008 70B8h	ICU	Interrupt Request Register 184	IR184	8	8	2 ICLK	section 14.
0008 70B9h	ICU	Interrupt Request Register 185	IR185	8	8	2 ICLK	section 14.
0008 70BAh	ICU	Interrupt Request Register 186	IR186	8	8	2 ICLK	section 14.
0008 70BBh	ICU	Interrupt Request Register 187	IR187	8	8	2 ICLK	section 14.
0008 70BCh	ICU	Interrupt Request Register 188	IR188	8	8	2 ICLK	section 14.
0008 70BDh	ICU	Interrupt Request Register 189	IR189	8	8	2 ICLK	section 14.
0008 70BEh	ICU	Interrupt Request Register 190	IR190	8	8	2 ICLK	section 14.
0008 70BFh	ICU	Interrupt Request Register 191	IR191	8	8	2 ICLK	section 14.
0008 70C0h	ICU	Interrupt Request Register 192	IR192	8	8	2 ICLK	section 14.
0008 70C1h	ICU	Interrupt Request Register 193	IR193	8	8	2 ICLK	section 14.
0008 70C2h	ICU	Interrupt Request Register 194	IR194	8	8	2 ICLK	section 14.
0008 70C3h	ICU	Interrupt Request Register 195	IR195	8	8	2 ICLK	section 14.
0008 70C4h	ICU	Interrupt Request Register 196	IR196	8	8	2 ICLK	section 14.
0008 70C5h	ICU	Interrupt Request Register 197	IR197	8	8	2 ICLK	section 14.
0008 70CAh	ICU	Interrupt Request Register 202	IR202	8	8	2 ICLK	section 14.
0008 70CBh	ICU	Interrupt Request Register 203	IR203	8	8	2 ICLK	section 14.
0008 70CCh	ICU	Interrupt Request Register 204	IR204	8	8	2 ICLK	section 14.

Table 5.1 List of I/O Registers (Address Order) (5/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Reference Section
0008 70CDh	ICU	Interrupt Request Register 205	IR205	8	8	2 ICLK	section 14.
0008 70CEh	ICU	Interrupt Request Register 206	IR206	8	8	2 ICLK	section 14.
0008 70CFh	ICU	Interrupt Request Register 207	IR207	8	8	2 ICLK	section 14.
0008 70D0h	ICU	Interrupt Request Register 208	IR208	8	8	2 ICLK	section 14.
0008 70D1h	ICU	Interrupt Request Register 209	IR209	8	8	2 ICLK	section 14.
0008 70D2h	ICU	Interrupt Request Register 210	IR210	8	8	2 ICLK	section 14.
0008 70D3h	ICU	Interrupt Request Register 211	IR211	8	8	2 ICLK	section 14.
0008 70D4h	ICU	Interrupt Request Register 212	IR212	8	8	2 ICLK	section 14.
0008 70D5h	ICU	Interrupt Request Register 213	IR213	8	8	2 ICLK	section 14.
0008 70D6h	ICU	Interrupt Request Register 214	IR214	8	8	2 ICLK	section 14.
0008 70D7h	ICU	Interrupt Request Register 215	IR215	8	8	2 ICLK	section 14.
0008 70D8h	ICU	Interrupt Request Register 216	IR216	8	8	2 ICLK	section 14.
0008 70D9h	ICU	Interrupt Request Register 217	IR217	8	8	2 ICLK	section 14.
0008 70DAh	ICU	Interrupt Request Register 218	IR218	8	8	2 ICLK	section 14.
0008 70DBh	ICU	Interrupt Request Register 219	IR219	8	8	2 ICLK	section 14.
0008 70DCh	ICU	Interrupt Request Register 220	IR220	8	8	2 ICLK	section 14.
0008 70DDh	ICU	Interrupt Request Register 221	IR221	8	8	2 ICLK	section 14.
0008 70DEh	ICU	Interrupt Request Register 222	IR222	8	8	2 ICLK	section 14.
0008 70DFh	ICU	Interrupt Request Register 223	IR223	8	8	2 ICLK	section 14.
0008 70E0h	ICU	Interrupt Request Register 224	IR224	8	8	2 ICLK	section 14.
0008 70E1h	ICU	Interrupt Request Register 225	IR225	8	8	2 ICLK	section 14.
0008 70E2h	ICU	Interrupt Request Register 226	IR226	8	8	2 ICLK	section 14.
0008 70E3h	ICU	Interrupt Request Register 227	IR227	8	8	2 ICLK	section 14.
0008 70E4h	ICU	Interrupt Request Register 228	IR228	8	8	2 ICLK	section 14.
0008 70E5h	ICU	Interrupt Request Register 229	IR229	8	8	2 ICLK	section 14.
0008 70E6h	ICU	Interrupt Request Register 230	IR230	8	8	2 ICLK	section 14.
0008 70E7h	ICU	Interrupt Request Register 231	IR231	8	8	2 ICLK	section 14.
0008 70E8h	ICU	Interrupt Request Register 232	IR232	8	8	2 ICLK	section 14.
0008 70E9h	ICU	Interrupt Request Register 233	IR233	8	8	2 ICLK	section 14.
0008 70EAh	ICU	Interrupt Request Register 234	IR234	8	8	2 ICLK	section 14.
0008 70EBh	ICU	Interrupt Request Register 235	IR235	8	8	2 ICLK	section 14.
0008 70ECh	ICU	Interrupt Request Register 236	IR236	8	8	2 ICLK	section 14.
0008 70EDh	ICU	Interrupt Request Register 237	IR237	8	8	2 ICLK	section 14.
0008 70EEh	ICU	Interrupt Request Register 238	IR238	8	8	2 ICLK	section 14.
0008 70EFh	ICU	Interrupt Request Register 239	IR239	8	8	2 ICLK	section 14.
0008 70F0h	ICU	Interrupt Request Register 240	IR240	8	8	2 ICLK	section 14.
0008 70F1h	ICU	Interrupt Request Register 241	IR241	8	8	2 ICLK	section 14.
0008 70F2h	ICU	Interrupt Request Register 242	IR242	8	8	2 ICLK	section 14.
0008 70F3h	ICU	Interrupt Request Register 243	IR243	8	8	2 ICLK	section 14.
0008 70F4h	ICU	Interrupt Request Register 244	IR244	8	8	2 ICLK	section 14.
0008 70F6h	ICU	Interrupt Request Register 246	IR246	8	8	2 ICLK	section 14.
0008 70F7h	ICU	Interrupt Request Register 247	IR247	8	8	2 ICLK	section 14.
0008 70F8h	ICU	Interrupt Request Register 248	IR248	8	8	2 ICLK	section 14.
0008 70F9h	ICU	Interrupt Request Register 249	IR249	8	8	2 ICLK	section 14.
0008 70FAh	ICU	Interrupt Request Register 250	IR250	8	8	2 ICLK	section 14.
0008 70FBh	ICU	Interrupt Request Register 251	IR251	8	8	2 ICLK	section 14.
0008 70FCh	ICU	Interrupt Request Register 252	IR252	8	8	2 ICLK	section 14.
0008 70FDh	ICU	Interrupt Request Register 253	IR253	8	8	2 ICLK	section 14.
0008 711Bh	ICU	DTC Transfer Request Enable Register 027	DTCER027	8	8	2 ICLK	section 14.
0008 711Ch	ICU	DTC Transfer Request Enable Register 028	DTCER028	8	8	2 ICLK	section 14.
0008 711Dh	ICU	DTC Transfer Request Enable Register 029	DTCER029	8	8	2 ICLK	section 14.

Table 5.1 List of I/O Registers (Address Order) (6/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Reference Section
0008 711Eh	ICU	DTC Transfer Request Enable Register 030	DTCER030	8	8	2 ICLK	section 14.
0008 711Fh	ICU	DTC Transfer Request Enable Register 031	DTCER031	8	8	2 ICLK	section 14.
0008 712Dh	ICU	DTC Transfer Request Enable Register 045	DTCER045	8	8	2 ICLK	section 14.
0008 712Eh	ICU	DTC Transfer Request Enable Register 046	DTCER046	8	8	2 ICLK	section 14.
0008 7130h	ICU	DTC Transfer Request Enable Register 048	DTCER048	8	8	2 ICLK	section 14.
0008 7131h	ICU	DTC Transfer Request Enable Register 049	DTCER049	8	8	2 ICLK	section 14.
0008 7132h	ICU	DTC Transfer Request Enable Register 050	DTCER050	8	8	2 ICLK	section 14.
0008 7133h	ICU	DTC Transfer Request Enable Register 051	DTCER051	8	8	2 ICLK	section 14.
0008 7135h	ICU	DTC Transfer Request Enable Register 053	DTCER053	8	8	2 ICLK	section 14.
0008 7136h	ICU	DTC Transfer Request Enable Register 054	DTCER054	8	8	2 ICLK	section 14.
0008 7137h	ICU	DTC Transfer Request Enable Register 055	DTCER055	8	8	2 ICLK	section 14.
0008 7138h	ICU	DTC Transfer Request Enable Register 056	DTCER056	8	8	2 ICLK	section 14.
0008 713Bh	ICU	DTC Transfer Request Enable Register 059	DTCER059	8	8	2 ICLK	section 14.
0008 7140h	ICU	DTC Transfer Request Enable Register 064	DTCER064	8	8	2 ICLK	section 14.
0008 7141h	ICU	DTC Transfer Request Enable Register 065	DTCER065	8	8	2 ICLK	section 14.
0008 7142h	ICU	DTC Transfer Request Enable Register 066	DTCER066	8	8	2 ICLK	section 14.
0008 7143h	ICU	DTC Transfer Request Enable Register 067	DTCER067	8	8	2 ICLK	section 14.
0008 7144h	ICU	DTC Transfer Request Enable Register 068	DTCER068	8	8	2 ICLK	section 14.
0008 7145h	ICU	DTC Transfer Request Enable Register 069	DTCER069	8	8	2 ICLK	section 14.
0008 7146h	ICU	DTC Transfer Request Enable Register 070	DTCER070	8	8	2 ICLK	section 14.
0008 7147h	ICU	DTC Transfer Request Enable Register 071	DTCER071	8	8	2 ICLK	section 14.
0008 7162h	ICU	DTC Transfer Request Enable Register 098	DTCER098	8	8	2 ICLK	section 14.
0008 7163h	ICU	DTC Transfer Request Enable Register 099	DTCER099	8	8	2 ICLK	section 14.
0008 7164h	ICU	DTC Transfer Request Enable Register 100	DTCER100	8	8	2 ICLK	section 14.
0008 7165h	ICU	DTC Transfer Request Enable Register 101	DTCER101	8	8	2 ICLK	section 14.
0008 7166h	ICU	DTC Transfer Request Enable Register 102	DTCER102	8	8	2 ICLK	section 14.
0008 7167h	ICU	DTC Transfer Request Enable Register 103	DTCER103	8	8	2 ICLK	section 14.
0008 7168h	ICU	DTC Transfer Request Enable Register 104	DTCER104	8	8	2 ICLK	section 14.
0008 7169h	ICU	DTC Transfer Request Enable Register 105	DTCER105	8	8	2 ICLK	section 14.
0008 716Ah	ICU	DTC Transfer Request Enable Register 106	DTCER106	8	8	2 ICLK	section 14.
0008 716Bh	ICU	DTC Transfer Request Enable Register 107	DTCER107	8	8	2 ICLK	section 14.
0008 716Ch	ICU	DTC Transfer Request Enable Register 108	DTCER108	8	8	2 ICLK	section 14.
0008 716Dh	ICU	DTC Transfer Request Enable Register 109	DTCER109	8	8	2 ICLK	section 14.
0008 716Eh	ICU	DTC Transfer Request Enable Register 110	DTCER110	8	8	2 ICLK	section 14.
0008 716Fh	ICU	DTC Transfer Request Enable Register 111	DTCER111	8	8	2 ICLK	section 14.
0008 7170h	ICU	DTC Transfer Request Enable Register 112	DTCER112	8	8	2 ICLK	section 14.
0008 7171h	ICU	DTC Transfer Request Enable Register 113	DTCER113	8	8	2 ICLK	section 14.
0008 7172h	ICU	DTC Transfer Request Enable Register 114	DTCER114	8	8	2 ICLK	section 14.
0008 7173h	ICU	DTC Transfer Request Enable Register 115	DTCER115	8	8	2 ICLK	section 14.
0008 7174h	ICU	DTC Transfer Request Enable Register 116	DTCER116	8	8	2 ICLK	section 14.
0008 7175h	ICU	DTC Transfer Request Enable Register 117	DTCER117	8	8	2 ICLK	section 14.
0008 7179h	ICU	DTC Transfer Request Enable Register 121	DTCER121	8	8	2 ICLK	section 14.
0008 717Ah	ICU	DTC Transfer Request Enable Register 122	DTCER122	8	8	2 ICLK	section 14.
0008 717Dh	ICU	DTC Transfer Request Enable Register 125	DTCER125	8	8	2 ICLK	section 14.
0008 717Eh	ICU	DTC Transfer Request Enable Register 126	DTCER126	8	8	2 ICLK	section 14.
0008 7181h	ICU	DTC Transfer Request Enable Register 129	DTCER129	8	8	2 ICLK	section 14.
0008 7182h	ICU	DTC Transfer Request Enable Register 130	DTCER130	8	8	2 ICLK	section 14.
0008 7183h	ICU	DTC Transfer Request Enable Register 131	DTCER131	8	8	2 ICLK	section 14.
0008 7184h	ICU	DTC Transfer Request Enable Register 132	DTCER132	8	8	2 ICLK	section 14.
0008 7186h	ICU	DTC Transfer Request Enable Register 134	DTCER134	8	8	2 ICLK	section 14.
0008 7187h	ICU	DTC Transfer Request Enable Register 135	DTCER135	8	8	2 ICLK	section 14.

Table 5.1 List of I/O Registers (Address Order) (7/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Reference Section
0008 7188h	ICU	DTC Transfer Request Enable Register 136	DTCER136	8	8	2 ICLK	section 14.
0008 7189h	ICU	DTC Transfer Request Enable Register 137	DTCER137	8	8	2 ICLK	section 14.
0008 718Ah	ICU	DTC Transfer Request Enable Register 138	DTCER138	8	8	2 ICLK	section 14.
0008 718Bh	ICU	DTC Transfer Request Enable Register 139	DTCER139	8	8	2 ICLK	section 14.
0008 718Ch	ICU	DTC Transfer Request Enable Register 140	DTCER140	8	8	2 ICLK	section 14.
0008 718Dh	ICU	DTC Transfer Request Enable Register 141	DTCER141	8	8	2 ICLK	section 14.
0008 718Eh	ICU	DTC Transfer Request Enable Register 142	DTCER142	8	8	2 ICLK	section 14.
0008 718Fh	ICU	DTC Transfer Request Enable Register 143	DTCER143	8	8	2 ICLK	section 14.
0008 7190h	ICU	DTC Transfer Request Enable Register 144	DTCER144	8	8	2 ICLK	section 14.
0008 7191h	ICU	DTC Transfer Request Enable Register 145	DTCER145	8	8	2 ICLK	section 14.
0008 7195h	ICU	DTC Transfer Request Enable Register 149	DTCER149	8	8	2 ICLK	section 14.
0008 7196h	ICU	DTC Transfer Request Enable Register 150	DTCER150	8	8	2 ICLK	section 14.
0008 7197h	ICU	DTC Transfer Request Enable Register 151	DTCER151	8	8	2 ICLK	section 14.
0008 7198h	ICU	DTC Transfer Request Enable Register 152	DTCER152	8	8	2 ICLK	section 14.
0008 7199h	ICU	DTC Transfer Request Enable Register 153	DTCER153	8	8	2 ICLK	section 14.
0008 719Fh	ICU	DTC Transfer Request Enable Register 159	DTCER159	8	8	2 ICLK	section 14.
0008 71A0h	ICU	DTC Transfer Request Enable Register 160	DTCER160	8	8	2 ICLK	section 14.
0008 71A1h	ICU	DTC Transfer Request Enable Register 161	DTCER161	8	8	2 ICLK	section 14.
0008 71A2h	ICU	DTC Transfer Request Enable Register 162	DTCER162	8	8	2 ICLK	section 14.
0008 71ADh	ICU	DTC Transfer Request Enable Register 173	DTCER173	8	8	2 ICLK	section 14.
0008 71AEh	ICU	DTC Transfer Request Enable Register 174	DTCER174	8	8	2 ICLK	section 14.
0008 71AFh	ICU	DTC Transfer Request Enable Register 175	DTCER175	8	8	2 ICLK	section 14.
0008 71B1h	ICU	DTC Transfer Request Enable Register 177	DTCER177	8	8	2 ICLK	section 14.
0008 71B2h	ICU	DTC Transfer Request Enable Register 178	DTCER178	8	8	2 ICLK	section 14.
0008 71B4h	ICU	DTC Transfer Request Enable Register 180	DTCER180	8	8	2 ICLK	section 14.
0008 71B5h	ICU	DTC Transfer Request Enable Register 181	DTCER181	8	8	2 ICLK	section 14.
0008 71B7h	ICU	DTC Transfer Request Enable Register 183	DTCER183	8	8	2 ICLK	section 14.
0008 71B8h	ICU	DTC Transfer Request Enable Register 184	DTCER184	8	8	2 ICLK	section 14.
0008 71BAh	ICU	DTC Transfer Request Enable Register 186	DTCER186	8	8	2 ICLK	section 14.
0008 71BBh	ICU	DTC Transfer Request Enable Register 187	DTCER187	8	8	2 ICLK	section 14.
0008 71BDh	ICU	DTC Transfer Request Enable Register 189	DTCER189	8	8	2 ICLK	section 14.
0008 71BEh	ICU	DTC Transfer Request Enable Register 190	DTCER190	8	8	2 ICLK	section 14.
0008 71C0h	ICU	DTC Transfer Request Enable Register 192	DTCER192	8	8	2 ICLK	section 14.
0008 71C1h	ICU	DTC Transfer Request Enable Register 193	DTCER193	8	8	2 ICLK	section 14.
0008 71C3h	ICU	DTC Transfer Request Enable Register 195	DTCER195	8	8	2 ICLK	section 14.
0008 71C4h	ICU	DTC Transfer Request Enable Register 196	DTCER196	8	8	2 ICLK	section 14.
0008 71CBh	ICU	DTC Transfer Request Enable Register 203	DTCER203	8	8	2 ICLK	section 14.
0008 71CCh	ICU	DTC Transfer Request Enable Register 204	DTCER204	8	8	2 ICLK	section 14.
0008 71CDh	ICU	DTC Transfer Request Enable Register 205	DTCER205	8	8	2 ICLK	section 14.
0008 71CEh	ICU	DTC Transfer Request Enable Register 206	DTCER206	8	8	2 ICLK	section 14.
0008 71CFh	ICU	DTC Transfer Request Enable Register 207	DTCER207	8	8	2 ICLK	section 14.
0008 71D0h	ICU	DTC Transfer Request Enable Register 208	DTCER208	8	8	2 ICLK	section 14.
0008 71D1h	ICU	DTC Transfer Request Enable Register 209	DTCER209	8	8	2 ICLK	section 14.
0008 71D2h	ICU	DTC Transfer Request Enable Register 210	DTCER210	8	8	2 ICLK	section 14.
0008 71D4h	ICU	DTC Transfer Request Enable Register 212	DTCER212	8	8	2 ICLK	section 14.
0008 71D5h	ICU	DTC Transfer Request Enable Register 213	DTCER213	8	8	2 ICLK	section 14.
0008 71D6h	ICU	DTC Transfer Request Enable Register 214	DTCER214	8	8	2 ICLK	section 14.
0008 71D7h	ICU	DTC Transfer Request Enable Register 215	DTCER215	8	8	2 ICLK	section 14.
0008 71D8h	ICU	DTC Transfer Request Enable Register 216	DTCER216	8	8	2 ICLK	section 14.
0008 71D9h	ICU	DTC Transfer Request Enable Register 217	DTCER217	8	8	2 ICLK	section 14.
0008 71DBh	ICU	DTC Transfer Request Enable Register 219	DTCER219	8	8	2 ICLK	section 14.

Table 5.1 List of I/O Registers (Address Order) (8/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Reference Section
0008 71DCh	ICU	DTC Transfer Request Enable Register 220	DTCER220	8	8	2 ICLK	section 14.
0008 71DFh	ICU	DTC Transfer Request Enable Register 223	DTCER223	8	8	2 ICLK	section 14.
0008 71E0h	ICU	DTC Transfer Request Enable Register 224	DTCER224	8	8	2 ICLK	section 14.
0008 71E3h	ICU	DTC Transfer Request Enable Register 227	DTCER227	8	8	2 ICLK	section 14.
0008 71E4h	ICU	DTC Transfer Request Enable Register 228	DTCER228	8	8	2 ICLK	section 14.
0008 71E7h	ICU	DTC Transfer Request Enable Register 231	DTCER231	8	8	2 ICLK	section 14.
0008 71E8h	ICU	DTC Transfer Request Enable Register 232	DTCER232	8	8	2 ICLK	section 14.
0008 71EBh	ICU	DTC Transfer Request Enable Register 235	DTCER235	8	8	2 ICLK	section 14.
0008 71ECh	ICU	DTC Transfer Request Enable Register 236	DTCER236	8	8	2 ICLK	section 14.
0008 71EEh	ICU	DTC Transfer Request Enable Register 238	DTCER238	8	8	2 ICLK	section 14.
0008 71EFh	ICU	DTC Transfer Request Enable Register 239	DTCER239	8	8	2 ICLK	section 14.
0008 71F1h	ICU	DTC Transfer Request Enable Register 241	DTCER241	8	8	2 ICLK	section 14.
0008 71F2h	ICU	DTC Transfer Request Enable Register 242	DTCER242	8	8	2 ICLK	section 14.
0008 71F3h	ICU	DTC Transfer Request Enable Register 243	DTCER243	8	8	2 ICLK	section 14.
0008 71F4h	ICU	DTC Transfer Request Enable Register 244	DTCER244	8	8	2 ICLK	section 14.
0008 71F7h	ICU	DTC Transfer Request Enable Register 247	DTCER247	8	8	2 ICLK	section 14.
0008 71F8h	ICU	DTC Transfer Request Enable Register 248	DTCER248	8	8	2 ICLK	section 14.
0008 71FBh	ICU	DTC Transfer Request Enable Register 251	DTCER251	8	8	2 ICLK	section 14.
0008 71FCh	ICU	DTC Transfer Request Enable Register 252	DTCER252	8	8	2 ICLK	section 14.
0008 7202h	ICU	Interrupt Request Enable Register 02	IER02	8	8	2 ICLK	section 14.
0008 7203h	ICU	Interrupt Request Enable Register 03	IER03	8	8	2 ICLK	section 14.
0008 7204h	ICU	Interrupt Request Enable Register 04	IER04	8	8	2 ICLK	section 14.
0008 7205h	ICU	Interrupt Request Enable Register 05	IER05	8	8	2 ICLK	section 14.
0008 7206h	ICU	Interrupt Request Enable Register 06	IER06	8	8	2 ICLK	section 14.
0008 7207h	ICU	Interrupt Request Enable Register 07	IER07	8	8	2 ICLK	section 14.
0008 7208h	ICU	Interrupt Request Enable Register 08	IER08	8	8	2 ICLK	section 14.
0008 720Bh	ICU	Interrupt Request Enable Register 0B	IER0B	8	8	2 ICLK	section 14.
0008 720Ch	ICU	Interrupt Request Enable Register 0C	IER0C	8	8	2 ICLK	section 14.
0008 720Dh	ICU	Interrupt Request Enable Register 0D	IER0D	8	8	2 ICLK	section 14.
0008 720Eh	ICU	Interrupt Request Enable Register 0E	IER0E	8	8	2 ICLK	section 14.
0008 720Fh	ICU	Interrupt Request Enable Register 0F	IER0F	8	8	2 ICLK	section 14.
0008 7210h	ICU	Interrupt Request Enable Register 10	IER10	8	8	2 ICLK	section 14.
0008 7211h	ICU	Interrupt Request Enable Register 11	IER11	8	8	2 ICLK	section 14.
0008 7212h	ICU	Interrupt Request Enable Register 12	IER12	8	8	2 ICLK	section 14.
0008 7213h	ICU	Interrupt Request Enable Register 13	IER13	8	8	2 ICLK	section 14.
0008 7214h	ICU	Interrupt Request Enable Register 14	IER14	8	8	2 ICLK	section 14.
0008 7215h	ICU	Interrupt Request Enable Register 15	IER15	8	8	2 ICLK	section 14.
0008 7216h	ICU	Interrupt Request Enable Register 16	IER16	8	8	2 ICLK	section 14.
0008 7217h	ICU	Interrupt Request Enable Register 17	IER17	8	8	2 ICLK	section 14.
0008 7218h	ICU	Interrupt Request Enable Register 18	IER18	8	8	2 ICLK	section 14.
0008 7219h	ICU	Interrupt Request Enable Register 19	IER19	8	8	2 ICLK	section 14.
0008 721Ah	ICU	Interrupt Request Enable Register 1A	IER1A	8	8	2 ICLK	section 14.
0008 721Bh	ICU	Interrupt Request Enable Register 1B	IER1B	8	8	2 ICLK	section 14.
0008 721Ch	ICU	Interrupt Request Enable Register 1C	IER1C	8	8	2 ICLK	section 14.
0008 721Dh	ICU	Interrupt Request Enable Register 1D	IER1D	8	8	2 ICLK	section 14.
0008 721Eh	ICU	Interrupt Request Enable Register 1E	IER1E	8	8	2 ICLK	section 14.
0008 721Fh	ICU	Interrupt Request Enable Register 1F	IER1F	8	8	2 ICLK	section 14.
0008 72E0h	ICU	Software Interrupt Generation Register	SWINTR	8	8	2 ICLK	section 14.
0008 72F0h	ICU	Fast Interrupt Set Register	FIR	16	16	2 ICLK	section 14.
0008 7300h	ICU	Interrupt Source Priority Register 000	IPR000	8	8	2 ICLK	section 14.
0008 7302h	ICU	Interrupt Source Priority Register 002	IPR002	8	8	2 ICLK	section 14.

Table 5.1 List of I/O Registers (Address Order) (9/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Reference Section
0008 7303h	ICU	Interrupt Source Priority Register 003	IPR003	8	8	2 ICLK	section 14.
0008 7304h	ICU	Interrupt Source Priority Register 004	IPR004	8	8	2 ICLK	section 14.
0008 7305h	ICU	Interrupt Source Priority Register 005	IPR005	8	8	2 ICLK	section 14.
0008 7306h	ICU	Interrupt Source Priority Register 006	IPR006	8	8	2 ICLK	section 14.
0008 7307h	ICU	Interrupt Source Priority Register 007	IPR007	8	8	2 ICLK	section 14.
0008 7320h	ICU	Interrupt Source Priority Register 032	IPR032	8	8	2 ICLK	section 14.
0008 7321h	ICU	Interrupt Source Priority Register 033	IPR033	8	8	2 ICLK	section 14.
0008 7322h	ICU	Interrupt Source Priority Register 034	IPR034	8	8	2 ICLK	section 14.
0008 7328h	ICU	Interrupt Source Priority Register 040	IPR040	8	8	2 ICLK	section 14.
0008 7329h	ICU	Interrupt Source Priority Register 041	IPR041	8	8	2 ICLK	section 14.
0008 732Ch	ICU	Interrupt Source Priority Register 044	IPR044	8	8	2 ICLK	section 14.
0008 7330h	ICU	Interrupt Source Priority Register 048	IPR048	8	8	2 ICLK	section 14.
0008 7331h	ICU	Interrupt Source Priority Register 049	IPR049	8	8	2 ICLK	section 14.
0008 7332h	ICU	Interrupt Source Priority Register 050	IPR050	8	8	2 ICLK	section 14.
0008 7333h	ICU	Interrupt Source Priority Register 051	IPR051	8	8	2 ICLK	section 14.
0008 7334h	ICU	Interrupt Source Priority Register 052	IPR052	8	8	2 ICLK	section 14.
0008 7335h	ICU	Interrupt Source Priority Register 053	IPR053	8	8	2 ICLK	section 14.
0008 7336h	ICU	Interrupt Source Priority Register 054	IPR054	8	8	2 ICLK	section 14.
0008 7337h	ICU	Interrupt Source Priority Register 055	IPR055	8	8	2 ICLK	section 14.
0008 7338h	ICU	Interrupt Source Priority Register 056	IPR056	8	8	2 ICLK	section 14.
0008 7339h	ICU	Interrupt Source Priority Register 057	IPR057	8	8	2 ICLK	section 14.
0008 733Bh	ICU	Interrupt Source Priority Register 059	IPR059	8	8	2 ICLK	section 14.
0008 733Ch	ICU	Interrupt Source Priority Register 060	IPR060	8	8	2 ICLK	section 14.
0008 733Dh	ICU	Interrupt Source Priority Register 061	IPR061	8	8	2 ICLK	section 14.
0008 733Eh	ICU	Interrupt Source Priority Register 062	IPR062	8	8	2 ICLK	section 14.
0008 733Fh	ICU	Interrupt Source Priority Register 063	IPR063	8	8	2 ICLK	section 14.
0008 7340h	ICU	Interrupt Source Priority Register 064	IPR064	8	8	2 ICLK	section 14.
0008 7341h	ICU	Interrupt Source Priority Register 065	IPR065	8	8	2 ICLK	section 14.
0008 7342h	ICU	Interrupt Source Priority Register 066	IPR066	8	8	2 ICLK	section 14.
0008 7343h	ICU	Interrupt Source Priority Register 067	IPR067	8	8	2 ICLK	section 14.
0008 7344h	ICU	Interrupt Source Priority Register 068	IPR068	8	8	2 ICLK	section 14.
0008 7345h	ICU	Interrupt Source Priority Register 069	IPR069	8	8	2 ICLK	section 14.
0008 7346h	ICU	Interrupt Source Priority Register 070	IPR070	8	8	2 ICLK	section 14.
0008 7347h	ICU	Interrupt Source Priority Register 071	IPR071	8	8	2 ICLK	section 14.
0008 7358h	ICU	Interrupt Source Priority Register 088	IPR088	8	8	2 ICLK	section 14.
0008 7359h	ICU	Interrupt Source Priority Register 089	IPR089	8	8	2 ICLK	section 14.
0008 7362h	ICU	Interrupt Source Priority Register 098	IPR098	8	8	2 ICLK	section 14.
0008 7363h	ICU	Interrupt Source Priority Register 099	IPR099	8	8	2 ICLK	section 14.
0008 7364h	ICU	Interrupt Source Priority Register 100	IPR100	8	8	2 ICLK	section 14.
0008 7365h	ICU	Interrupt Source Priority Register 101	IPR101	8	8	2 ICLK	section 14.
0008 7366h	ICU	Interrupt Source Priority Register 102	IPR102	8	8	2 ICLK	section 14.
0008 7367h	ICU	Interrupt Source Priority Register 103	IPR103	8	8	2 ICLK	section 14.
0008 7368h	ICU	Interrupt Source Priority Register 104	IPR104	8	8	2 ICLK	section 14.
0008 7369h	ICU	Interrupt Source Priority Register 105	IPR105	8	8	2 ICLK	section 14.
0008 736Ah	ICU	Interrupt Source Priority Register 106	IPR106	8	8	2 ICLK	section 14.
0008 736Bh	ICU	Interrupt Source Priority Register 107	IPR107	8	8	2 ICLK	section 14.
0008 736Ch	ICU	Interrupt Source Priority Register 108	IPR108	8	8	2 ICLK	section 14.
0008 736Dh	ICU	Interrupt Source Priority Register 109	IPR109	8	8	2 ICLK	section 14.
0008 736Eh	ICU	Interrupt Source Priority Register 110	IPR110	8	8	2 ICLK	section 14.
0008 736Fh	ICU	Interrupt Source Priority Register 111	IPR111	8	8	2 ICLK	section 14.
0008 7370h	ICU	Interrupt Source Priority Register 112	IPR112	8	8	2 ICLK	section 14.

Table 5.1 List of I/O Registers (Address Order) (10/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Reference Section
0008 7371h	ICU	Interrupt Source Priority Register 113	IPR113	8	8	2 ICLK	section 14.
0008 7372h	ICU	Interrupt Source Priority Register 114	IPR114	8	8	2 ICLK	section 14.
0008 7376h	ICU	Interrupt Source Priority Register 118	IPR118	8	8	2 ICLK	section 14.
0008 7379h	ICU	Interrupt Source Priority Register 121	IPR121	8	8	2 ICLK	section 14.
0008 737Bh	ICU	Interrupt Source Priority Register 123	IPR123	8	8	2 ICLK	section 14.
0008 737Dh	ICU	Interrupt Source Priority Register 125	IPR125	8	8	2 ICLK	section 14.
0008 737Fh	ICU	Interrupt Source Priority Register 127	IPR127	8	8	2 ICLK	section 14.
0008 7381h	ICU	Interrupt Source Priority Register 129	IPR129	8	8	2 ICLK	section 14.
0008 7385h	ICU	Interrupt Source Priority Register 133	IPR133	8	8	2 ICLK	section 14.
0008 7386h	ICU	Interrupt Source Priority Register 134	IPR134	8	8	2 ICLK	section 14.
0008 738Ah	ICU	Interrupt Source Priority Register 138	IPR138	8	8	2 ICLK	section 14.
0008 738Bh	ICU	Interrupt Source Priority Register 139	IPR139	8	8	2 ICLK	section 14.
0008 738Eh	ICU	Interrupt Source Priority Register 142	IPR142	8	8	2 ICLK	section 14.
0008 7392h	ICU	Interrupt Source Priority Register 146	IPR146	8	8	2 ICLK	section 14.
0008 7395h	ICU	Interrupt Source Priority Register 149	IPR149	8	8	2 ICLK	section 14.
0008 7397h	ICU	Interrupt Source Priority Register 151	IPR151	8	8	2 ICLK	section 14.
0008 7399h	ICU	Interrupt Source Priority Register 153	IPR153	8	8	2 ICLK	section 14.
0008 739Fh	ICU	Interrupt Source Priority Register 159	IPR159	8	8	2 ICLK	section 14.
0008 73A3h	ICU	Interrupt Source Priority Register 163	IPR163	8	8	2 ICLK	section 14.
0008 73A8h	ICU	Interrupt Source Priority Register 168	IPR168	8	8	2 ICLK	section 14.
0008 73ADh	ICU	Interrupt Source Priority Register 173	IPR173	8	8	2 ICLK	section 14.
0008 73AEh	ICU	Interrupt Source Priority Register 174	IPR174	8	8	2 ICLK	section 14.
0008 73B1h	ICU	Interrupt Source Priority Register 177	IPR177	8	8	2 ICLK	section 14.
0008 73B4h	ICU	Interrupt Source Priority Register 180	IPR180	8	8	2 ICLK	section 14.
0008 73B7h	ICU	Interrupt Source Priority Register 183	IPR183	8	8	2 ICLK	section 14.
0008 73BAh	ICU	Interrupt Source Priority Register 186	IPR186	8	8	2 ICLK	section 14.
0008 73BDh	ICU	Interrupt Source Priority Register 189	IPR189	8	8	2 ICLK	section 14.
0008 73C0h	ICU	Interrupt Source Priority Register 192	IPR192	8	8	2 ICLK	section 14.
0008 73C3h	ICU	Interrupt Source Priority Register 195	IPR195	8	8	2 ICLK	section 14.
0008 73CAh	ICU	Interrupt Source Priority Register 202	IPR202	8	8	2 ICLK	section 14.
0008 73CBh	ICU	Interrupt Source Priority Register 203	IPR203	8	8	2 ICLK	section 14.
0008 73CCh	ICU	Interrupt Source Priority Register 204	IPR204	8	8	2 ICLK	section 14.
0008 73CDh	ICU	Interrupt Source Priority Register 205	IPR205	8	8	2 ICLK	section 14.
0008 73CEh	ICU	Interrupt Source Priority Register 206	IPR206	8	8	2 ICLK	section 14.
0008 73CFh	ICU	Interrupt Source Priority Register 207	IPR207	8	8	2 ICLK	section 14.
0008 73D0h	ICU	Interrupt Source Priority Register 208	IPR208	8	8	2 ICLK	section 14.
0008 73D1h	ICU	Interrupt Source Priority Register 209	IPR209	8	8	2 ICLK	section 14.
0008 73D2h	ICU	Interrupt Source Priority Register 210	IPR210	8	8	2 ICLK	section 14.
0008 73D3h	ICU	Interrupt Source Priority Register 211	IPR211	8	8	2 ICLK	section 14.
0008 73D4h	ICU	Interrupt Source Priority Register 212	IPR212	8	8	2 ICLK	section 14.
0008 73D5h	ICU	Interrupt Source Priority Register 213	IPR213	8	8	2 ICLK	section 14.
0008 73D6h	ICU	Interrupt Source Priority Register 214	IPR214	8	8	2 ICLK	section 14.
0008 73D7h	ICU	Interrupt Source Priority Register 215	IPR215	8	8	2 ICLK	section 14.
0008 73D8h	ICU	Interrupt Source Priority Register 216	IPR216	8	8	2 ICLK	section 14.
0008 73D9h	ICU	Interrupt Source Priority Register 217	IPR217	8	8	2 ICLK	section 14.
0008 73DAh	ICU	Interrupt Source Priority Register 218	IPR218	8	8	2 ICLK	section 14.
0008 73DEh	ICU	Interrupt Source Priority Register 222	IPR222	8	8	2 ICLK	section 14.
0008 73E2h	ICU	Interrupt Source Priority Register 226	IPR226	8	8	2 ICLK	section 14.
0008 73E6h	ICU	Interrupt Source Priority Register 230	IPR230	8	8	2 ICLK	section 14.
0008 73EAh	ICU	Interrupt Source Priority Register 234	IPR234	8	8	2 ICLK	section 14.
0008 73EEh	ICU	Interrupt Source Priority Register 238	IPR238	8	8	2 ICLK	section 14.

Table 5.1 List of I/O Registers (Address Order) (11/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Reference Section
0008 73EFh	ICU	Interrupt Source Priority Register 239	IPR239	8	8	2 ICLK	section 14.
0008 73F0h	ICU	Interrupt Source Priority Register 240	IPR240	8	8	2 ICLK	section 14.
0008 73F1h	ICU	Interrupt Source Priority Register 241	IPR241	8	8	2 ICLK	section 14.
0008 73F2h	ICU	Interrupt Source Priority Register 242	IPR242	8	8	2 ICLK	section 14.
0008 73F3h	ICU	Interrupt Source Priority Register 243	IPR243	8	8	2 ICLK	section 14.
0008 73F4h	ICU	Interrupt Source Priority Register 244	IPR244	8	8	2 ICLK	section 14.
0008 73F6h	ICU	Interrupt Source Priority Register 246	IPR246	8	8	2 ICLK	section 14.
0008 73F7h	ICU	Interrupt Source Priority Register 247	IPR247	8	8	2 ICLK	section 14.
0008 73F8h	ICU	Interrupt Source Priority Register 248	IPR248	8	8	2 ICLK	section 14.
0008 73F9h	ICU	Interrupt Source Priority Register 249	IPR249	8	8	2 ICLK	section 14.
0008 73FAh	ICU	Interrupt Source Priority Register 250	IPR250	8	8	2 ICLK	section 14.
0008 7500h	ICU	IRQ Control Register 0	IRQCR0	8	8	2 ICLK	section 14.
0008 7501h	ICU	IRQ Control Register 1	IRQCR1	8	8	2 ICLK	section 14.
0008 7502h	ICU	IRQ Control Register 2	IRQCR2	8	8	2 ICLK	section 14.
0008 7503h	ICU	IRQ Control Register 3	IRQCR3	8	8	2 ICLK	section 14.
0008 7504h	ICU	IRQ Control Register 4	IRQCR4	8	8	2 ICLK	section 14.
0008 7505h	ICU	IRQ Control Register 5	IRQCR5	8	8	2 ICLK	section 14.
0008 7506h	ICU	IRQ Control Register 6	IRQCR6	8	8	2 ICLK	section 14.
0008 7507h	ICU	IRQ Control Register 7	IRQCR7	8	8	2 ICLK	section 14.
0008 7510h	ICU	IRQ Pin Digital Filter Enable Register 0	IRQFLTE0	8	8	2 ICLK	section 14.
0008 7514h	ICU	IRQ Pin Digital Filter Setting Register 0	IRQFLTC0	16	16	2 ICLK	section 14.
0008 7580h	ICU	Non-Maskable Interrupt Status Register	NMISR	8	8	2 ICLK	section 14.
0008 7581h	ICU	Non-Maskable Interrupt Enable Register	NMIER	8	8	2 ICLK	section 14.
0008 7582h	ICU	Non-Maskable Interrupt Status Clear Register	NMICLR	8	8	2 ICLK	section 14.
0008 7583h	ICU	NMI Pin Interrupt Control Register	NMICR	8	8	2 ICLK	section 14.
0008 7590h	ICU	NMI Pin Digital Filter Enable Register	NMIFLTE	8	8	2 ICLK	section 14.
0008 7594h	ICU	NMI Pin Digital Filter Setting Register	NMIFLTC	8	8	2 ICLK	section 14.
0008 8000h	CMT	Compare Match Timer Start Register 0	CMSTR0	16	16	2 or 3 PCLKB	section 24.
0008 8002h	CMT0	Compare Match Timer Control Register	CMCR	16	16	2 or 3 PCLKB	section 24.
0008 8004h	CMT0	Compare Match Counter	CMCNT	16	16	2 or 3 PCLKB	section 24.
0008 8006h	CMT0	Compare Match Constant Register	CMCOR	16	16	2 or 3 PCLKB	section 24.
0008 8008h	CMT1	Compare Match Timer Control Register	CMCR	16	16	2 or 3 PCLKB	section 24.
0008 800Ah	CMT1	Compare Match Counter	CMCNT	16	16	2 or 3 PCLKB	section 24.
0008 800Ch	CMT1	Compare Match Constant Register	CMCOR	16	16	2 or 3 PCLKB	section 24.
0008 8010h	CMT	Compare Match Timer Start Register 1	CMSTR1	16	16	2 or 3 PCLKB	section 24.
0008 8012h	CMT2	Compare Match Timer Control Register	CMCR	16	16	2 or 3 PCLKB	section 24.
0008 8014h	CMT2	Compare Match Counter	CMCNT	16	16	2 or 3 PCLKB	section 24.
0008 8016h	CMT2	Compare Match Constant Register	CMCOR	16	16	2 or 3 PCLKB	section 24.
0008 8018h	CMT3	Compare Match Timer Control Register	CMCR	16	16	2 or 3 PCLKB	section 24.
0008 801Ah	CMT3	Compare Match Counter	CMCNT	16	16	2 or 3 PCLKB	section 24.
0008 801Ch	CMT3	Compare Match Constant Register	CMCOR	16	16	2 or 3 PCLKB	section 24.
0008 8030h	IWDT	IWDT Refresh Register	IWDTRR	8	8	2 or 3 PCLKB	section 25.
0008 8032h	IWDT	IWDT Control Register	IWDTCR	16	16	2 or 3 PCLKB	section 25.
0008 8034h	IWDT	IWDT Status Register	IWDTSR	16	16	2 or 3 PCLKB	section 25.
0008 8036h	IWDT	IWDT Reset Control Register	IWDTRCR	8	8	2 or 3 PCLKB	section 25.
0008 8038h	IWDT	IWDT Count Stop Control Register	IWDTCSTPR	8	8	2 or 3 PCLKB	section 25.
0008 80C0h	DA	D/A Data Register 0	DADR0	16	16	2 or 3 PCLKB	section 32.
0008 80C2h	DA	D/A Data Register 1	DADR1	16	16	2 or 3 PCLKB	section 32.
0008 80C4h	DA	D/A Control Register	DACR	8	8	2 or 3 PCLKB	section 32.
0008 80C5h	DA	DADRm Format Select Register	DADPR	8	8	2 or 3 PCLKB	section 32.
0008 80C6h	DA	D/A A/D Synchronous Start Control Register	DAADSCR	8	8	2 or 3 PCLKB	section 32.

Table 5.1 List of I/O Registers (Address Order) (12/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Reference Section
0008 8200h	TMR0	Timer Control Register	TCR	8	8	2 or 3 PCLKB	section 23.
0008 8201h	TMR1	Timer Control Register	TCR	8	8	2 or 3 PCLKB	section 23.
0008 8202h	TMR0	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB	section 23.
0008 8203h	TMR1	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB	section 23.
0008 8204h	TMR0	Time Constant Register A	TCORA	8	8	2 or 3 PCLKB	section 23.
0008 8205h	TMR1	Time Constant Register A	TCORA	8	8*1	2 or 3 PCLKB	section 23.
0008 8206h	TMR0	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB	section 23.
0008 8207h	TMR1	Time Constant Register B	TCORB	8	8*1	2 or 3 PCLKB	section 23.
0008 8208h	TMR0	Timer Counter	TCNT	8	8	2 or 3 PCLKB	section 23.
0008 8209h	TMR1	Timer Counter	TCNT	8	8*1	2 or 3 PCLKB	section 23.
0008 820Ah	TMR0	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB	section 23.
0008 820Bh	TMR1	Timer Counter Control Register	TCCR	8	8*1	2 or 3 PCLKB	section 23.
0008 8210h	TMR2	Timer Control Register	TCR	8	8	2 or 3 PCLKB	section 23.
0008 8211h	TMR3	Timer Control Register	TCR	8	8	2 or 3 PCLKB	section 23.
0008 8212h	TMR2	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB	section 23.
0008 8213h	TMR3	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB	section 23.
0008 8214h	TMR2	Time Constant Register A	TCORA	8	8	2 or 3 PCLKB	section 23.
0008 8215h	TMR3	Time Constant Register A	TCORA	8	8*1	2 or 3 PCLKB	section 23.
0008 8216h	TMR2	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB	section 23.
0008 8217h	TMR3	Time Constant Register B	TCORB	8	8*1	2 or 3 PCLKB	section 23.
0008 8218h	TMR2	Timer Counter	TCNT	8	8	2 or 3 PCLKB	section 23.
0008 8219h	TMR3	Timer Counter	TCNT	8	8*1	2 or 3 PCLKB	section 23.
0008 821Ah	TMR2	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB	section 23.
0008 821Bh	TMR3	Timer Counter Control Register	TCCR	8	8*1	2 or 3 PCLKB	section 23.
0008 8220h	TMR4	Timer Control Register	TCR	8	8	2 or 3 PCLKB	section 23.
0008 8221h	TMR5	Timer Control Register	TCR	8	8	2 or 3 PCLKB	section 23.
0008 8222h	TMR4	Timer Control / Status Register	TCSR	8	8	2 or 3 PCLKB	section 23.
0008 8223h	TMR5	Timer Control / Status Register	TCSR	8	8	2 or 3 PCLKB	section 23.
0008 8224h	TMR4	Time Constant Register A	TCORA	8	8	2 or 3 PCLKB	section 23.
0008 8225h	TMR5	Time Constant Register A	TCORA	8	8*1	2 or 3 PCLKB	section 23.
0008 8226h	TMR4	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB	section 23.
0008 8227h	TMR5	Time Constant Register B	TCORB	8	8*1	2 or 3 PCLKB	section 23.
0008 8228h	TMR4	Timer Counter	TCNT	8	8	2 or 3 PCLKB	section 23.
0008 8229h	TMR5	Timer Counter	TCNT	8	8*1	2 or 3 PCLKB	section 23.
0008 822Ah	TMR4	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB	section 23.
0008 822Bh	TMR5	Timer Counter Control Register	TCCR	8	8*1	2 or 3 PCLKB	section 23.
0008 8230h	TMR6	Timer Control Register	TCR	8	8	2 or 3 PCLKB	section 23.
0008 8231h	TMR7	Timer Control Register	TCR	8	8	2 or 3 PCLKB	section 23.
0008 8232h	TMR6	Timer Control / Status Register	TCSR	8	8	2 or 3 PCLKB	section 23.
0008 8233h	TMR7	Timer Control / Status Register	TCSR	8	8	2 or 3 PCLKB	section 23.
0008 8234h	TMR6	Time Constant Register A	TCORA	8	8	2 or 3 PCLKB	section 23.
0008 8235h	TMR7	Time Constant Register A	TCORA	8	8*1	2 or 3 PCLKB	section 23.
0008 8236h	TMR6	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB	section 23.
0008 8237h	TMR7	Time Constant Register B	TCORB	8	8*1	2 or 3 PCLKB	section 23.
0008 8238h	TMR6	Timer Counter	TCNT	8	8	2 or 3 PCLKB	section 23.
0008 8239h	TMR7	Timer Counter	TCNT	8	8*1	2 or 3 PCLKB	section 23.
0008 823Ah	TMR6	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB	section 23.
0008 823Bh	TMR7	Timer Counter Control Register	TCCR	8	8*1	2 or 3 PCLKB	section 23.
0008 8280h	CRC	CRC Control Register	CRCCR	8	8	2 or 3 PCLKB	section 30.
0008 8281h	CRC	CRC Data Input Register	CRCDIR	8	8	2 or 3 PCLKB	section 30.
0008 8282h	CRC	CRC Data Output Register	CRCDOR	16	16	2 or 3 PCLKB	section 30.

Table 5.1 List of I/O Registers (Address Order) (13/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Reference Section
0008 8300h	RIIC0	I²C-bus Control Register 1	ICCR1	8	8	2 or 3 PCLKB	section 27.
0008 8301h	RIIC0	I²C-bus Control Register 2	ICCR2	8	8	2 or 3 PCLKB	section 27.
0008 8302h	RIIC0	I²C-bus Mode Register 1	ICMR1	8	8	2 or 3 PCLKB	section 27.
0008 8303h	RIIC0	I²C-bus Mode Register 2	ICMR2	8	8	2 or 3 PCLKB	section 27.
0008 8304h	RIIC0	I²C-bus Mode Register 3	ICMR3	8	8	2 or 3 PCLKB	section 27.
0008 8305h	RIIC0	I²C-bus Function Enable Register	ICFER	8	8	2 or 3 PCLKB	section 27.
0008 8306h	RIIC0	I²C-bus Status Enable Register	ICSER	8	8	2 or 3 PCLKB	section 27.
0008 8307h	RIIC0	I²C-bus Interrupt Enable Register	ICIER	8	8	2 or 3 PCLKB	section 27.
0008 8308h	RIIC0	I²C-bus Status Register 1	ICSR1	8	8	2 or 3 PCLKB	section 27.
0008 8309h	RIIC0	I²C-bus Status Register 2	ICSR2	8	8	2 or 3 PCLKB	section 27.
0008 830Ah	RIIC0	Slave Address Register L0	SARL0	8	8	2 or 3 PCLKB	section 27.
0008 830Bh	RIIC0	Slave Address Register U0	SARU0	8	8	2 or 3 PCLKB	section 27.
0008 830Ch	RIIC0	Slave Address Register L1	SARL1	8	8	2 or 3 PCLKB	section 27.
0008 830Dh	RIIC0	Slave Address Register U1	SARU1	8	8	2 or 3 PCLKB	section 27.
0008 830Eh	RIIC0	Slave Address Register L2	SARL2	8	8	2 or 3 PCLKB	section 27.
0008 830Fh	RIIC0	Slave Address Register U2	SARU2	8	8	2 or 3 PCLKB	section 27.
0008 8310h	RIIC0	I²C-bus Bit Rate Low-Level Register	ICBRL	8	8	2 or 3 PCLKB	section 27.
0008 8311h	RIIC0	I²C-bus Bit Rate High-Level Register	ICBRH	8	8	2 or 3 PCLKB	section 27.
0008 8312h	RIIC0	I²C-bus Transmit Data Register	ICDRT	8	8	2 or 3 PCLKB	section 27.
0008 8313h	RIIC0	I²C-bus Receive Data Register	ICDRR	8	8	2 or 3 PCLKB	section 27.
0008 8380h	RSPI0	RSPI Control Register	SPCR	8	8	2 or 3 PCLKB	section 29.
0008 8381h	RSPI0	RSPI Slave Select Polarity Register	SSLP	8	8	2 or 3 PCLKB	section 29.
0008 8382h	RSPI0	RSPI Pin Control Register	SPPCR	8	8	2 or 3 PCLKB	section 29.
0008 8383h	RSPI0	RSPI Status Register	SPSR	8	8	2 or 3 PCLKB	section 29.
0008 8384h	RSPI0	RSPI Data Register	SPDR	32	16, 32	2 or 3 PCLKB	section 29.
0008 8388h	RSPI0	RSPI Sequence Control Register	SPSCR	8	8	2 or 3 PCLKB	section 29.
0008 8389h	RSPI0	RSPI Sequence Status Register	SPSSR	8	8	2 or 3 PCLKB	section 29.
0008 838Ah	RSPI0	RSPI Bit Rate Register	SPBR	8	8	2 or 3 PCLKB	section 29.
0008 838Bh	RSPI0	RSPI Data Control Register	SPDCR	8	8	2 or 3 PCLKB	section 29.
0008 838Ch	RSPI0	RSPI Clock Delay Register	SPCKD	8	8	2 or 3 PCLKB	section 29.
0008 838Dh	RSPI0	RSPI Slave Select Negation Delay Register	SSLND	8	8	2 or 3 PCLKB	section 29.
0008 838Eh	RSPI0	RSPI Next-Access Delay Register	SPND	8	8	2 or 3 PCLKB	section 29.
0008 838Fh	RSPI0	RSPI Control Register 2	SPCR2	8	8	2 or 3 PCLKB	section 29.
0008 8390h	RSPI0	RSPI Command Register 0	SPCMD0	16	16	2 or 3 PCLKB	section 29.
0008 8392h	RSPI0	RSPI Command Register 1	SPCMD1	16	16	2 or 3 PCLKB	section 29.
0008 8394h	RSPI0	RSPI Command Register 2	SPCMD2	16	16	2 or 3 PCLKB	section 29.
0008 8396h	RSPI0	RSPI Command Register 3	SPCMD3	16	16	2 or 3 PCLKB	section 29.
0008 8398h	RSPI0	RSPI Command Register 4	SPCMD4	16	16	2 or 3 PCLKB	section 29.
0008 839Ah	RSPI0	RSPI Command Register 5	SPCMD5	16	16	2 or 3 PCLKB	section 29.
0008 839Ch	RSPI0	RSPI Command Register 6	SPCMD6	16	16	2 or 3 PCLKB	section 29.
0008 839Eh	RSPI0	RSPI Command Register 7	SPCMD7	16	16	2 or 3 PCLKB	section 29.
0008 9000h	S12AD	A/D Control Register	ADCSR	16	16	2 or 3 PCLKB	section 31.
0008 9004h	S12AD	A/D Channel Select Register A0	ADANSA0	16	16	2 or 3 PCLKB	section 31.
0008 9006h	S12AD	A/D Channel Select Register A1	ADANSA1	16	16	2 or 3 PCLKB	section 31.
0008 9008h	S12AD	A/D-Converted Value Addition/Average Function Channel Select Register 0	ADADS0	16	16	2 or 3 PCLKB	section 31.
0008 900Ah	S12AD	A/D-Converted Value Addition/Average Function Channel Select Register 1	ADADS1	16	16	2 or 3 PCLKB	section 31.
0008 900Ch	S12AD	A/D-Converted Value Addition/Average Count Select Register	ADADC	8	8	2 or 3 PCLKB	section 31.
0008 900Eh	S12AD	A/D Control Extended Register	ADCER	16	16	2 or 3 PCLKB	section 31.
0008 9010h	S12AD	A/D Conversion Start Trigger Select Register	ADSTRGR	16	16	2 or 3 PCLKB	section 31.
0008 9014h	S12AD	A/D Channel Select Register B0	ADANSB0	16	16	2 or 3 PCLKB	section 31.

Table 5.1 List of I/O Registers (Address Order) (14/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Reference Section
0008 9016h	S12AD	A/D Channel Select Register B1	ADANSB1	16	16	2 or 3 PCLKB	section 31.
0008 9018h	S12AD	A/D Data Duplication Register	ADDBLDR	16	16	2 or 3 PCLKB	section 31.
0008 901Eh	S12AD	A/D Self-Diagnosis Data Register	ADRD	16	16	2 or 3 PCLKB	section 31.
0008 9020h	S12AD	A/D Data Register 0	ADDR0	16	16	2 or 3 PCLKB	section 31.
0008 9022h	S12AD	A/D Data Register 1	ADDR1	16	16	2 or 3 PCLKB	section 31.
0008 9024h	S12AD	A/D Data Register 2	ADDR2	16	16	2 or 3 PCLKB	section 31.
0008 9026h	S12AD	A/D Data Register 3	ADDR3	16	16	2 or 3 PCLKB	section 31.
0008 9040h	S12AD	A/D Data Register 16	ADDR16	16	16	2 or 3 PCLKB	section 31.
0008 907Ah	S12AD	A/D Disconnection Detection Control Register	ADDISCR	8	8	2 or 3 PCLKB	section 31.
0008 9080h	S12AD	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2 or 3 PCLKB	section 31.
0008 9084h	S12AD	A/D Data Duplication Register A	ADDBLDRA	16	16	2 or 3 PCLKB	section 31.
0008 9086h	S12AD	A/D Data Duplication Register B	ADDBLDRB	16	16	2 or 3 PCLKB	section 31.
0008 90D4h	S12AD	A/D Channel Select Register C0	ADANSC0	16	16	2 or 3 PCLKB	section 31.
0008 90D6h	S12AD	A/D Channel Select Register C1	ADANSC1	16	16	2 or 3 PCLKB	section 31.
0008 90D9h	S12AD	A/D Group C Trigger Select Register	ADGCTRGR	8	8	2 or 3 PCLKB	section 31.
0008 90DDh	S12AD	A/D Sampling State Register L	ADSSTRL	8	8	2 or 3 PCLKB	section 31.
0008 90E0h	S12AD	A/D Sampling State Register 0	ADSSTR0	8	8	2 or 3 PCLKB	section 31.
0008 90E1h	S12AD	A/D Sampling State Register 1	ADSSTR1	8	8	2 or 3 PCLKB	section 31.
0008 90E2h	S12AD	A/D Sampling State Register 2	ADSSTR2	8	8	2 or 3 PCLKB	section 31.
0008 90E3h	S12AD	A/D Sampling State Register 3	ADSSTR3	8	8	2 or 3 PCLKB	section 31.
0008 91A0h	S12AD	A/D Programmable Gain Amplifier Control Register	ADPGACR	16	16	2 or 3 PCLKB	section 31.
0008 91A2h	S12AD	A/D Programmable Gain Amplifier Gain Setting Register 0	ADPGAGS0	16	16	2 or 3 PCLKB	section 31.
0008 9200h	S12AD1	A/D Control Register	ADCSR	16	16	2 or 3 PCLKB	section 31.
0008 9204h	S12AD1	A/D Channel Select Register A0	ADANSA0	16	16	2 or 3 PCLKB	section 31.
0008 9206h	S12AD1	A/D Channel Select Register A1	ADANSA1	16	16	2 or 3 PCLKB	section 31.
0008 9208h	S12AD1	A/D-Converted Value Addition/Average Function Channel Select Register 0	ADADS0	16	16	2 or 3 PCLKB	section 31.
0008 920Ah	S12AD1	A/D-Converted Value Addition/Average Function Channel Select Register 1	ADADS1	16	16	2 or 3 PCLKB	section 31.
0008 920Ch	S12AD1	A/D-Converted Value Addition/Average Count Select Register	ADADC	8	8	2 or 3 PCLKB	section 31.
0008 920Eh	S12AD1	A/D Control Extended Register	ADCER	16	16	2 or 3 PCLKB	section 31.
0008 9210h	S12AD1	A/D Conversion Start Trigger Select Register	ADSTRGR	16	16	2 or 3 PCLKB	section 31.
0008 9214h	S12AD1	A/D Channel Select Register B0	ADANSB0	16	16	2 or 3 PCLKB	section 31.
0008 9216h	S12AD1	A/D Channel Select Register B1	ADANSB1	16	16	2 or 3 PCLKB	section 31.
0008 9218h	S12AD1	A/D Data Duplication Register	ADDBLDR	16	16	2 or 3 PCLKB	section 31.
0008 921Eh	S12AD1	A/D Self-Diagnosis Data Register	ADRD	16	16	2 or 3 PCLKB	section 31.
0008 9220h	S12AD1	A/D Data Register 0	ADDR0	16	16	2 or 3 PCLKB	section 31.
0008 9222h	S12AD1	A/D Data Register 1	ADDR1	16	16	2 or 3 PCLKB	section 31.
0008 9224h	S12AD1	A/D Data Register 2	ADDR2	16	16	2 or 3 PCLKB	section 31.
0008 9226h	S12AD1	A/D Data Register 3	ADDR3	16	16	2 or 3 PCLKB	section 31.
0008 9240h	S12AD1	A/D Data Register 16	ADDR16	16	16	2 or 3 PCLKB	section 31.
0008 9266h	S12AD1	A/D Sample-and-hold Circuit Control Register	ADSHCR	16	16	2 or 3 PCLKB	section 31.
0008 927Ah	S12AD1	A/D Disconnection Detection Control Register	ADDISCR	8	8	2 or 3 PCLKB	section 31.
0008 9280h	S12AD1	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2 or 3 PCLKB	section 31.
0008 9284h	S12AD1	A/D Data Duplication Register A	ADDBLDRA	16	16	2 or 3 PCLKB	section 31.
0008 9286h	S12AD1	A/D Data Duplication Register B	ADDBLDRB	16	16	2 or 3 PCLKB	section 31.
0008 92D4h	S12AD1	A/D Channel Select Register C0	ADANSC0	16	16	2 or 3 PCLKB	section 31.
0008 92D6h	S12AD1	A/D Channel Select Register C1	ADANSC1	16	16	2 or 3 PCLKB	section 31.
0008 92D9h	S12AD1	A/D Group C Trigger Select Register	ADGCTRGR	8	8	2 or 3 PCLKB	section 31.
0008 92DDh	S12AD1	A/D Sampling State Register L	ADSSTRL	8	8	2 or 3 PCLKB	section 31.
0008 92E0h	S12AD1	A/D Sampling State Register 0	ADSSTR0	8	8	2 or 3 PCLKB	section 31.
0008 92E1h	S12AD1	A/D Sampling State Register 1	ADSSTR1	8	8	2 or 3 PCLKB	section 31.

Table 5.1 List of I/O Registers (Address Order) (15/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Reference Section
0008 92E2h	S12AD1	A/D Sampling State Register 2	ADSSTR2	8	8	2 or 3 PCLKB	section 31.
0008 92E3h	S12AD1	A/D Sampling State Register 3	ADSSTR3	8	8	2 or 3 PCLKB	section 31.
0008 93A0h	S12AD1	A/D Programmable Gain Amplifier Control Register	ADPGACR	16	16	2 or 3 PCLKB	section 31.
0008 93A2h	S12AD1	A/D Programmable Gain Amplifier Gain Setting Register 0	ADPGAGS0	16	16	2 or 3 PCLKB	section 31.
0008 9400h	S12AD2	A/D Control Register	ADCSR	16	16	2 or 3 PCLKB	section 31.
0008 9404h	S12AD2	A/D Channel Select Register A0	ADANSA0	16	16	2 or 3 PCLKB	section 31.
0008 9408h	S12AD2	A/D-Converted Value Addition/Average Function Channel Select Register 0	ADADS0	16	16	2 or 3 PCLKB	section 31.
0008 940Ch	S12AD2	A/D-Converted Value Addition/Average Count Select Register	ADADC	8	8	2 or 3 PCLKB	section 31.
0008 940Eh	S12AD2	A/D Control Extended Register	ADCER	16	16	2 or 3 PCLKB	section 31.
0008 9410h	S12AD2	A/D Conversion Start Trigger Select Register	ADSTRGR	16	16	2 or 3 PCLKB	section 31.
0008 9412h	S12AD2	A/D Conversion Extended Input Control Register	ADEXICR	16	16	2 or 3 PCLKB	section 31.
0008 9414h	S12AD2	A/D Channel Select Register B0	ADANSB0	16	16	2 or 3 PCLKB	section 31.
0008 9418h	S12AD2	A/D Data Duplication Register	ADDBLDR	16	16	2 or 3 PCLKB	section 31.
0008 941Ch	S12AD2	A/D Internal Reference Voltage Data Register	ADOCDR	16	16	2 or 3 PCLKB	section 31.
0008 941Eh	S12AD2	A/D Self-Diagnosis Data Register	ADRD	16	16	2 or 3 PCLKB	section 31.
0008 9420h	S12AD2	A/D Data Register 0	ADDR0	16	16	2 or 3 PCLKB	section 31.
0008 9422h	S12AD2	A/D Data Register 1	ADDR1	16	16	2 or 3 PCLKB	section 31.
0008 9424h	S12AD2	A/D Data Register 2	ADDR2	16	16	2 or 3 PCLKB	section 31.
0008 9426h	S12AD2	A/D Data Register 3	ADDR3	16	16	2 or 3 PCLKB	section 31.
0008 9428h	S12AD2	A/D Data Register 4	ADDR4	16	16	2 or 3 PCLKB	section 31.
0008 942Ah	S12AD2	A/D Data Register 5	ADDR5	16	16	2 or 3 PCLKB	section 31.
0008 942Ch	S12AD2	A/D Data Register 6	ADDR6	16	16	2 or 3 PCLKB	section 31.
0008 942Eh	S12AD2	A/D Data Register 7	ADDR7	16	16	2 or 3 PCLKB	section 31.
0008 9430h	S12AD2	A/D Data Register 8	ADDR8	16	16	2 or 3 PCLKB	section 31.
0008 9432h	S12AD2	A/D Data Register 9	ADDR9	16	16	2 or 3 PCLKB	section 31.
0008 9434h	S12AD2	A/D Data Register 10	ADDR10	16	16	2 or 3 PCLKB	section 31.
0008 9436h	S12AD2	A/D Data Register 11	ADDR11	16	16	2 or 3 PCLKB	section 31.
0008 947Ah	S12AD2	A/D Disconnection Detection Control Register	ADDISCR	8	8	2 or 3 PCLKB	section 31.
0008 9480h	S12AD2	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2 or 3 PCLKB	section 31.
0008 9484h	S12AD2	A/D Data Duplication Register A	ADDBLDRA	16	16	2 or 3 PCLKB	section 31.
0008 9486h	S12AD2	A/D Data Duplication Register B	ADDBLDRB	16	16	2 or 3 PCLKB	section 31.
0008 94D4h	S12AD2	A/D Channel Select Register C0	ADANSC0	16	16	2 or 3 PCLKB	section 31.
0008 94D9h	S12AD2	A/D Group C Trigger Select Register	ADGCTRGR	8	8	2 or 3 PCLKB	section 31.
0008 94DFh	S12AD2	A/D Sampling State Register O	ADSSTRO	8	8	2 or 3 PCLKB	section 31.
0008 94E0h	S12AD2	A/D Sampling State Register 0	ADSSTR0	8	8	2 or 3 PCLKB	section 31.
0008 94E1h	S12AD2	A/D Sampling State Register 1	ADSSTR1	8	8	2 or 3 PCLKB	section 31.
0008 94E2h	S12AD2	A/D Sampling State Register 2	ADSSTR2	8	8	2 or 3 PCLKB	section 31.
0008 94E3h	S12AD2	A/D Sampling State Register 3	ADSSTR3	8	8	2 or 3 PCLKB	section 31.
0008 94E4h	S12AD2	A/D Sampling State Register 4	ADSSTR4	8	8	2 or 3 PCLKB	section 31.
0008 94E5h	S12AD2	A/D Sampling State Register 5	ADSSTR5	8	8	2 or 3 PCLKB	section 31.
0008 94E6h	S12AD2	A/D Sampling State Register 6	ADSSTR6	8	8	2 or 3 PCLKB	section 31.
0008 94E7h	S12AD2	A/D Sampling State Register 7	ADSSTR7	8	8	2 or 3 PCLKB	section 31.
0008 94E8h	S12AD2	A/D Sampling State Register 8	ADSSTR8	8	8	2 or 3 PCLKB	section 31.
0008 94E9h	S12AD2	A/D Sampling State Register 9	ADSSTR9	8	8	2 or 3 PCLKB	section 31.
0008 94EAh	S12AD2	A/D Sampling State Register 10	ADSSTR10	8	8	2 or 3 PCLKB	section 31.
0008 94EBh	S12AD2	A/D Sampling State Register 11	ADSSTR11	8	8	2 or 3 PCLKB	section 31.
0008 A020h	SCI1	Serial Mode Register	SMR	8	8	2 or 3 PCLKB	section 26.
0008 A021h	SCI1	Bit Rate Register	BRR	8	8	2 or 3 PCLKB	section 26.
0008 A022h	SCI1	Serial Control Register	SCR	8	8	2 or 3 PCLKB	section 26.
0008 A023h	SCI1	Transmit Data Register	TDR	8	8	2 or 3 PCLKB	section 26.

Table 5.1 List of I/O Registers (Address Order) (16/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Reference Section
0008 A024h	SCI1	Serial Status Register	SSR	8	8	2 or 3 PCLKB	section 26.
0008 A025h	SCI1	Receive Data Register	RDR	8	8	2 or 3 PCLKB	section 26.
0008 A026h	SMCI1	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB	section 26.
0008 A027h	SCI1	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB	section 26.
0008 A028h	SCI1	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB	section 26.
0008 A029h	SCI1	I2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB	section 26.
0008 A02Ah	SCI1	I2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB	section 26.
0008 A02Bh	SCI1	I2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB	section 26.
0008 A02Ch	SCI1	I2C Status Register	SISR	8	8	2 or 3 PCLKB	section 26.
0008 A02Dh	SCI1	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB	section 26.
0008 A02Eh	SCI1	Transmit Data Register HL	TDRHL	16	16	4 or 5 PCLKB	section 26.
0008 A02Eh	SCI1	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB	section 26.
0008 A02Fh	SCI1	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB	section 26.
0008 A030h	SCI1	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB	section 26.
0008 A030h	SCI1	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB	section 26.
0008 A031h	SCI1	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB	section 26.
0008 A032h	SCI1	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB	section 26.
0008 A0A0h	SCI5	Serial Mode Register	SMR	8	8	2 or 3 PCLKB	section 26.
0008 A0A1h	SCI5	Bit Rate Register	BRR	8	8	2 or 3 PCLKB	section 26.
0008 A0A2h	SCI5	Serial Control Register	SCR	8	8	2 or 3 PCLKB	section 26.
0008 A0A3h	SCI5	Transmit Data Register	TDR	8	8	2 or 3 PCLKB	section 26.
0008 A0A4h	SCI5	Serial Status Register	SSR	8	8	2 or 3 PCLKB	section 26.
0008 A0A5h	SCI5	Receive Data Register	RDR	8	8	2 or 3 PCLKB	section 26.
0008 A0A6h	SMCI5	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB	section 26.
0008 A0A7h	SCI5	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB	section 26.
0008 A0A8h	SCI5	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB	section 26.
0008 A0A9h	SCI5	I2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB	section 26.
0008 A0AAh	SCI5	I2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB	section 26.
0008 A0ABh	SCI5	I2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB	section 26.
0008 A0ACh	SCI5	I2C Status Register	SISR	8	8	2 or 3 PCLKB	section 26.
0008 A0ADh	SCI5	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB	section 26.
0008 A0AEh	SCI5	Transmit Data Register HL	TDRHL	16	16	4 or 5 PCLKB	section 26.
0008 A0AEh	SCI5	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB	section 26.
0008 A0AFh	SCI5	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB	section 26.
0008 A0B0h	SCI5	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB	section 26.
0008 A0B0h	SCI5	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB	section 26.
0008 A0B1h	SCI5	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB	section 26.
0008 A0B2h	SCI5	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB	section 26.
0008 A0C0h	SCI6	Serial Mode Register	SMR	8	8	2 or 3 PCLKB	section 26.
0008 A0C1h	SCI6	Bit Rate Register	BRR	8	8	2 or 3 PCLKB	section 26.
0008 A0C2h	SCI6	Serial Control Register	SCR	8	8	2 or 3 PCLKB	section 26.
0008 A0C3h	SCI6	Transmit Data Register	TDR	8	8	2 or 3 PCLKB	section 26.
0008 A0C4h	SCI6	Serial Status Register	SSR	8	8	2 or 3 PCLKB	section 26.
0008 A0C5h	SCI6	Receive Data Register	RDR	8	8	2 or 3 PCLKB	section 26.
0008 A0C6h	SMCI6	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB	section 26.
0008 A0C7h	SCI6	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB	section 26.
0008 A0C8h	SCI6	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB	section 26.
0008 A0C9h	SCI6	I2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB	section 26.
0008 A0CAh	SCI6	I2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB	section 26.
0008 A0CBh	SCI6	I2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB	section 26.
0008 A0CCh	SCI6	I2C Status Register	SISR	8	8	2 or 3 PCLKB	section 26.

Table 5.1 List of I/O Registers (Address Order) (17/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Reference Section
0008 A0CDh	SCI6	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB	section 26.
0008 A0CEh	SCI6	Transmit Data Register HL	TDRHL	16	16	4 or 5 PCLKB	section 26.
0008 A0CEh	SCI6	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB	section 26.
0008 A0CFh	SCI6	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB	section 26.
0008 A0D0h	SCI6	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB	section 26.
0008 A0D0h	SCI6	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB	section 26.
0008 A0D1h	SCI6	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB	section 26.
0008 A0D2h	SCI6	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB	section 26.
0008 A100h	SCI8	Serial Mode Register	SMR	8	8	2 or 3 PCLKB	section 26.
0008 A101h	SCI8	Bit Rate Register	BRR	8	8	2 or 3 PCLKB	section 26.
0008 A102h	SCI8	Serial Control Register	SCR	8	8	2 or 3 PCLKB	section 26.
0008 A103h	SCI8	Transmit Data Register	TDR	8	8	2 or 3 PCLKB	section 26.
0008 A104h	SCI8	Serial Status Register	SSR	8	8	2 or 3 PCLKB	section 26.
0008 A105h	SCI8	Receive Data Register	RDR	8	8	2 or 3 PCLKB	section 26.
0008 A106h	SMCI8	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB	section 26.
0008 A107h	SCI8	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB	section 26.
0008 A108h	SCI8	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB	section 26.
0008 A109h	SCI8	I^2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB	section 26.
0008 A10Ah	SCI8	I^2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB	section 26.
0008 A10Bh	SCI8	I^2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB	section 26.
0008 A10Ch	SCI8	I^2C Status Register	SISR	8	8	2 or 3 PCLKB	section 26.
0008 A10Dh	SCI8	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB	section 26.
0008 A10Eh	SCI8	Transmit Data Register HL	TDRHL	16	16	4 or 5 PCLKB	section 26.
0008 A10Eh	SCI8	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB	section 26.
0008 A10Fh	SCI8	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB	section 26.
0008 A110h	SCI8	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB	section 26.
0008 A110h	SCI8	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB	section 26.
0008 A111h	SCI8	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB	section 26.
0008 A112h	SCI8	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB	section 26.
0008 A120h	SCI9	Serial Mode Register	SMR	8	8	2 or 3 PCLKB	section 26.
0008 A121h	SCI9	Bit Rate Register	BRR	8	8	2 or 3 PCLKB	section 26.
0008 A122h	SCI9	Serial Control Register	SCR	8	8	2 or 3 PCLKB	section 26.
0008 A123h	SCI9	Transmit Data Register	TDR	8	8	2 or 3 PCLKB	section 26.
0008 A124h	SCI9	Serial Status Register	SSR	8	8	2 or 3 PCLKB	section 26.
0008 A125h	SCI9	Receive Data Register	RDR	8	8	2 or 3 PCLKB	section 26.
0008 A126h	SMCI9	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB	section 26.
0008 A127h	SCI9	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB	section 26.
0008 A128h	SCI9	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB	section 26.
0008 A129h	SCI9	I^2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB	section 26.
0008 A12Ah	SCI9	I^2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB	section 26.
0008 A12Bh	SCI9	I^2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB	section 26.
0008 A12Ch	SCI9	I^2C Status Register	SISR	8	8	2 or 3 PCLKB	section 26.
0008 A12Dh	SCI9	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB	section 26.
0008 A12Eh	SCI9	Transmit Data Register HL	TDRHL	16	16	4 or 5 PCLKB	section 26.
0008 A12Eh	SCI9	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB	section 26.
0008 A12Fh	SCI9	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB	section 26.
0008 A130h	SCI9	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB	section 26.
0008 A130h	SCI9	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB	section 26.
0008 A131h	SCI9	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB	section 26.
0008 A132h	SCI9	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB	section 26.
0008 B000h	CAC	CAC Control Register 0	CACR0	8	8	2 or 3 PCLKB	section 10.

Table 5.1 List of I/O Registers (Address Order) (18/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Reference Section
0008 B001h	CAC	CAC Control Register 1	CACR1	8	8	2 or 3 PCLKB	section 10.
0008 B002h	CAC	CAC Control Register 2	CACR2	8	8	2 or 3 PCLKB	section 10.
0008 B003h	CAC	CAC Interrupt Request Enable Register	CAICR	8	8	2 or 3 PCLKB	section 10.
0008 B004h	CAC	CAC Status Register	CASTR	8	8	2 or 3 PCLKB	section 10.
0008 B006h	CAC	CAC Upper-Limit Value Setting Register	CAULVR	16	16	2 or 3 PCLKB	section 10.
0008 B008h	CAC	CAC Lower-Limit Value Setting Register	CALLVR	16	16	2 or 3 PCLKB	section 10.
0008 B00Ah	CAC	CAC Counter Buffer Register	CACNTBR	16	16	2 or 3 PCLKB	section 10.
0008 B080h	DOC	DOC Control Register	DOCR	8	8	2 or 3 PCLKB	section 34.
0008 B082h	DOC	DOC Data Input Register	DODIR	16	16	2 or 3 PCLKB	section 34.
0008 B084h	DOC	DOC Data Setting Register	DODSR	16	16	2 or 3 PCLKB	section 34.
0008 C000h	PORT0	Port Direction Register	PDR	8	8	2 or 3 PCLKB	section 18.
0008 C001h	PORT1	Port Direction Register	PDR	8	8	2 or 3 PCLKB	section 18.
0008 C002h	PORT2	Port Direction Register	PDR	8	8	2 or 3 PCLKB	section 18.
0008 C003h	PORT3	Port Direction Register	PDR	8	8	2 or 3 PCLKB	section 18.
0008 C004h	PORT4	Port Direction Register	PDR	8	8	2 or 3 PCLKB	section 18.
0008 C005h	PORT5	Port Direction Register	PDR	8	8	2 or 3 PCLKB	section 18.
0008 C006h	PORT6	Port Direction Register	PDR	8	8	2 or 3 PCLKB	section 18.
0008 C007h	PORT7	Port Direction Register	PDR	8	8	2 or 3 PCLKB	section 18.
0008 C008h	PORT8	Port Direction Register	PDR	8	8	2 or 3 PCLKB	section 18.
0008 C009h	PORT9	Port Direction Register	PDR	8	8	2 or 3 PCLKB	section 18.
0008 C00Ah	PORTA	Port Direction Register	PDR	8	8	2 or 3 PCLKB	section 18.
0008 C00Bh	PORTB	Port Direction Register	PDR	8	8	2 or 3 PCLKB	section 18.
0008 C00Ch	PORTC	Port Direction Register	PDR	8	8	2 or 3 PCLKB	section 18.
0008 C00Dh	PORTD	Port Direction Register	PDR	8	8	2 or 3 PCLKB	section 18.
0008 C00Eh	PORTE	Port Direction Register	PDR	8	8	2 or 3 PCLKB	section 18.
0008 C00Fh	PORTF	Port Direction Register	PDR	8	8	2 or 3 PCLKB	section 18.
0008 C010h	PORTG	Port Direction Register	PDR	8	8	2 or 3 PCLKB	section 18.
0008 C020h	PORT0	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	section 18.
0008 C021h	PORT1	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	section 18.
0008 C022h	PORT2	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	section 18.
0008 C023h	PORT3	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	section 18.
0008 C024h	PORT4	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	section 18.
0008 C025h	PORT5	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	section 18.
0008 C026h	PORT6	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	section 18.
0008 C027h	PORT7	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	section 18.
0008 C028h	PORT8	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	section 18.
0008 C029h	PORT9	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	section 18.
0008 C02Ah	PORTA	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	section 18.
0008 C02Bh	PORTB	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	section 18.
0008 C02Ch	PORTC	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	section 18.
0008 C02Dh	PORTD	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	section 18.
0008 C02Eh	PORTE	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	section 18.
0008 C02Fh	PORTF	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	section 18.
0008 C030h	PORTG	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	section 18.
0008 C040h	PORT0	Port Input Data Register	PIDR	8	8	2 or 3 PCLKB	section 18.
0008 C041h	PORT1	Port Input Data Register	PIDR	8	8	2 or 3 PCLKB	section 18.
0008 C042h	PORT2	Port Input Data Register	PIDR	8	8	2 or 3 PCLKB	section 18.
0008 C043h	PORT3	Port Input Data Register	PIDR	8	8	2 or 3 PCLKB	section 18.
0008 C044h	PORT4	Port Input Data Register	PIDR	8	8	2 or 3 PCLKB	section 18.
0008 C045h	PORT5	Port Input Data Register	PIDR	8	8	2 or 3 PCLKB	section 18.
0008 C046h	PORT6	Port Input Data Register	PIDR	8	8	2 or 3 PCLKB	section 18.

Table 5.1 List of I/O Registers (Address Order) (19/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Reference Section
0008 C047h	PORT7	Port Input Data Register	PIDR	8	8	2 or 3 PCLKB	section 18.
0008 C048h	PORT8	Port Input Data Register	PIDR	8	8	2 or 3 PCLKB	section 18.
0008 C049h	PORT9	Port Input Data Register	PIDR	8	8	2 or 3 PCLKB	section 18.
0008 C04Ah	PORTA	Port Input Data Register	PIDR	8	8	2 or 3 PCLKB	section 18.
0008 C04Bh	PORTB	Port Input Data Register	PIDR	8	8	2 or 3 PCLKB	section 18.
0008 C04Ch	PORTC	Port Input Data Register	PIDR	8	8	2 or 3 PCLKB	section 18.
0008 C04Dh	PORTD	Port Input Data Register	PIDR	8	8	2 or 3 PCLKB	section 18.
0008 C04Eh	PORTE	Port Input Data Register	PIDR	8	8	2 or 3 PCLKB	section 18.
0008 C04Fh	PORTF	Port Input Data Register	PIDR	8	8	2 or 3 PCLKB	section 18.
0008 C050h	PORTG	Port Input Data Register	PIDR	8	8	2 or 3 PCLKB	section 18.
0008 C060h	PORT0	Port Mode Register	PMR	8	8	2 or 3 PCLKB	section 18.
0008 C061h	PORT1	Port Mode Register	PMR	8	8	2 or 3 PCLKB	section 18.
0008 C062h	PORT2	Port Mode Register	PMR	8	8	2 or 3 PCLKB	section 18.
0008 C063h	PORT3	Port Mode Register	PMR	8	8	2 or 3 PCLKB	section 18.
0008 C067h	PORT7	Port Mode Register	PMR	8	8	2 or 3 PCLKB	section 18.
0008 C068h	PORT8	Port Mode Register	PMR	8	8	2 or 3 PCLKB	section 18.
0008 C069h	PORT9	Port Mode Register	PMR	8	8	2 or 3 PCLKB	section 18.
0008 C06Ah	PORTA	Port Mode Register	PMR	8	8	2 or 3 PCLKB	section 18.
0008 C06Bh	PORTB	Port Mode Register	PMR	8	8	2 or 3 PCLKB	section 18.
0008 C06Ch	PORTC	Port Mode Register	PMR	8	8	2 or 3 PCLKB	section 18.
0008 C06Dh	PORTD	Port Mode Register	PMR	8	8	2 or 3 PCLKB	section 18.
0008 C06Eh	PORTE	Port Mode Register	PMR	8	8	2 or 3 PCLKB	section 18.
0008 C06Fh	PORTF	Port Mode Register	PMR	8	8	2 or 3 PCLKB	section 18.
0008 C070h	PORTG	Port Mode Register	PMR	8	8	2 or 3 PCLKB	section 18.
0008 C080h	PORT0	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	section 18.
0008 C082h	PORT1	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	section 18.
0008 C083h	PORT1	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	section 18.
0008 C084h	PORT2	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	section 18.
0008 C085h	PORT2	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	section 18.
0008 C086h	PORT3	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	section 18.
0008 C087h	PORT3	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	section 18.
0008 C08Eh	PORT7	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	section 18.
0008 C08Fh	PORT7	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	section 18.
0008 C090h	PORT8	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	section 18.
0008 C091h	PORT8	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	section 18.
0008 C092h	PORT9	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	section 18.
0008 C093h	PORT9	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	section 18.
0008 C094h	PORTA	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	section 18.
0008 C095h	PORTA	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	section 18.
0008 C096h	PORTB	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	section 18.
0008 C097h	PORTB	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	section 18.
0008 C098h	PORTC	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	section 18.
0008 C099h	PORTC	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	section 18.
0008 C09Ah	PORTD	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	section 18.
0008 C09Bh	PORTD	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	section 18.
0008 C09Ch	PORTE	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	section 18.
0008 C09Dh	PORTE	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	section 18.
0008 C09Eh	PORTF	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	section 18.
0008 C0A0h	PORTG	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	section 18.
0008 C0C0h	PORT0	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	section 18.
0008 C0C1h	PORT1	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	section 18.

Table 5.1 List of I/O Registers (Address Order) (20/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Reference Section
0008 C0C2h	PORT2	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	section 18.
0008 C0C3h	PORT3	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	section 18.
0008 C0C4h	PORT4	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	section 18.
0008 C0C5h	PORT5	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	section 18.
0008 C0C6h	PORT6	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	section 18.
0008 C0C7h	PORT7	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	section 18.
0008 C0C8h	PORT8	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	section 18.
0008 C0C9h	PORT9	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	section 18.
0008 C0CAh	PORTA	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	section 18.
0008 C0CBh	PORTB	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	section 18.
0008 C0CCh	PORTC	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	section 18.
0008 C0CDh	PORTD	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	section 18.
0008 C0CEh	PORTE	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	section 18.
0008 C0CFh	PORTF	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	section 18.
0008 C0D0h	PORTG	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	section 18.
0008 C0E0h	PORT0	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	section 18.
0008 C0E1h	PORT1	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	section 18.
0008 C0E2h	PORT2	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	section 18.
0008 C0E3h	PORT3	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	section 18.
0008 C0E7h	PORT7	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	section 18.
0008 C0E8h	PORT8	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	section 18.
0008 C0E9h	PORT9	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	section 18.
0008 C0EAh	PORTA	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	section 18.
0008 C0EBh	PORTB	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	section 18.
0008 C0ECh	PORTC	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	section 18.
0008 C0EDh	PORTD	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	section 18.
0008 C0EEh	PORTE	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	section 18.
0008 C0EFh	PORTF	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	section 18.
0008 C0F0h	PORTG	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	section 18.
0008 C11Fh	MPC	Write-Protect Register	PWPR	8	8	2 or 3 PCLKB	section 19.
0008 C140h	MPC	P00 Pin Function Control Register	P00PFS	8	8	2 or 3 PCLKB	section 19.
0008 C141h	MPC	P01 Pin Function Control Register	P01PFS	8	8	2 or 3 PCLKB	section 19.
0008 C142h	MPC	P02 Pin Function Control Register	P02PFS	8	8	2 or 3 PCLKB	section 19.
0008 C148h	MPC	P10 Pin Function Control Register	P10PFS	8	8	2 or 3 PCLKB	section 19.
0008 C149h	MPC	P11 Pin Function Control Register	P11PFS	8	8	2 or 3 PCLKB	section 19.
0008 C14Ah	MPC	P12 Pin Function Control Register	P12PFS	8	8	2 or 3 PCLKB	section 19.
0008 C14Bh	MPC	P13 Pin Function Control Register	P13PFS	8	8	2 or 3 PCLKB	section 19.
0008 C14Ch	MPC	P14 Pin Function Control Register	P14PFS	8	8	2 or 3 PCLKB	section 19.
0008 C14Dh	MPC	P15 Pin Function Control Register	P15PFS	8	8	2 or 3 PCLKB	section 19.
0008 C14Eh	MPC	P16 Pin Function Control Register	P16PFS	8	8	2 or 3 PCLKB	section 19.
0008 C14Fh	MPC	P17 Pin Function Control Register	P17PFS	8	8	2 or 3 PCLKB	section 19.
0008 C150h	MPC	P20 Pin Function Control Register	P20PFS	8	8	2 or 3 PCLKB	section 19.
0008 C151h	MPC	P21 Pin Function Control Register	P21PFS	8	8	2 or 3 PCLKB	section 19.
0008 C152h	MPC	P22 Pin Function Control Register	P22PFS	8	8	2 or 3 PCLKB	section 19.
0008 C153h	MPC	P23 Pin Function Control Register	P23PFS	8	8	2 or 3 PCLKB	section 19.
0008 C154h	MPC	P24 Pin Function Control Register	P24PFS	8	8	2 or 3 PCLKB	section 19.
0008 C155h	MPC	P25 Pin Function Control Register	P25PFS	8	8	2 or 3 PCLKB	section 19.
0008 C156h	MPC	P26 Pin Function Control Register	P26PFS	8	8	2 or 3 PCLKB	section 19.
0008 C157h	MPC	P27 Pin Function Control Register	P27PFS	8	8	2 or 3 PCLKB	section 19.
0008 C158h	MPC	P30 Pin Function Control Register	P30PFS	8	8	2 or 3 PCLKB	section 19.
0008 C159h	MPC	P31 Pin Function Control Register	P31PFS	8	8	2 or 3 PCLKB	section 19.

Table 5.1 List of I/O Registers (Address Order) (21/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Reference Section
0008 C15Ah	MPC	P32 Pin Function Control Register	P32PFS	8	8	2 or 3 PCLKB	section 19.
0008 C15Bh	MPC	P33 Pin Function Control Register	P33PFS	8	8	2 or 3 PCLKB	section 19.
0008 C15Ch	MPC	P34 Pin Function Control Register	P34PFS	8	8	2 or 3 PCLKB	section 19.
0008 C15Dh	MPC	P35 Pin Function Control Register	P35PFS	8	8	2 or 3 PCLKB	section 19.
0008 C160h	MPC	P40 Pin Function Control Register	P40PFS	8	8	2 or 3 PCLKB	section 19.
0008 C161h	MPC	P41 Pin Function Control Register	P41PFS	8	8	2 or 3 PCLKB	section 19.
0008 C162h	MPC	P42 Pin Function Control Register	P42PFS	8	8	2 or 3 PCLKB	section 19.
0008 C163h	MPC	P43 Pin Function Control Register	P43PFS	8	8	2 or 3 PCLKB	section 19.
0008 C164h	MPC	P44 Pin Function Control Register	P44PFS	8	8	2 or 3 PCLKB	section 19.
0008 C165h	MPC	P45 Pin Function Control Register	P45PFS	8	8	2 or 3 PCLKB	section 19.
0008 C166h	MPC	P46 Pin Function Control Register	P46PFS	8	8	2 or 3 PCLKB	section 19.
0008 C167h	MPC	P47 Pin Function Control Register	P47PFS	8	8	2 or 3 PCLKB	section 19.
0008 C168h	MPC	P50 Pin Function Control Register	P50PFS	8	8	2 or 3 PCLKB	section 19.
0008 C169h	MPC	P51 Pin Function Control Register	P51PFS	8	8	2 or 3 PCLKB	section 19.
0008 C16Ah	MPC	P52 Pin Function Control Register	P52PFS	8	8	2 or 3 PCLKB	section 19.
0008 C16Bh	MPC	P53 Pin Function Control Register	P53PFS	8	8	2 or 3 PCLKB	section 19.
0008 C16Ch	MPC	P54 Pin Function Control Register	P54PFS	8	8	2 or 3 PCLKB	section 19.
0008 C16Dh	MPC	P55 Pin Function Control Register	P55PFS	8	8	2 or 3 PCLKB	section 19.
0008 C170h	MPC	P60 Pin Function Control Register	P60PFS	8	8	2 or 3 PCLKB	section 19.
0008 C171h	MPC	P61 Pin Function Control Register	P61PFS	8	8	2 or 3 PCLKB	section 19.
0008 C172h	MPC	P62 Pin Function Control Register	P62PFS	8	8	2 or 3 PCLKB	section 19.
0008 C173h	MPC	P63 Pin Function Control Register	P63PFS	8	8	2 or 3 PCLKB	section 19.
0008 C174h	MPC	P64 Pin Function Control Register	P64PFS	8	8	2 or 3 PCLKB	section 19.
0008 C175h	MPC	P65 Pin Function Control Register	P65PFS	8	8	2 or 3 PCLKB	section 19.
0008 C178h	MPC	P70 Pin Function Control Register	P70PFS	8	8	2 or 3 PCLKB	section 19.
0008 C179h	MPC	P71 Pin Function Control Register	P71PFS	8	8	2 or 3 PCLKB	section 19.
0008 C17Ah	MPC	P72 Pin Function Control Register	P72PFS	8	8	2 or 3 PCLKB	section 19.
0008 C17Bh	MPC	P73 Pin Function Control Register	P73PFS	8	8	2 or 3 PCLKB	section 19.
0008 C17Ch	MPC	P74 Pin Function Control Register	P74PFS	8	8	2 or 3 PCLKB	section 19.
0008 C17Dh	MPC	P75 Pin Function Control Register	P75PFS	8	8	2 or 3 PCLKB	section 19.
0008 C17Eh	MPC	P76 Pin Function Control Register	P76PFS	8	8	2 or 3 PCLKB	section 19.
0008 C180h	MPC	P80 Pin Function Control Register	P80PFS	8	8	2 or 3 PCLKB	section 19.
0008 C181h	MPC	P81 Pin Function Control Register	P81PFS	8	8	2 or 3 PCLKB	section 19.
0008 C182h	MPC	P82 Pin Function Control Register	P82PFS	8	8	2 or 3 PCLKB	section 19.
0008 C183h	MPC	P83 Pin Function Control Register	P83PFS	8	8	2 or 3 PCLKB	section 19.
0008 C184h	MPC	P84 Pin Function Control Register	P84PFS	8	8	2 or 3 PCLKB	section 19.
0008 C188h	MPC	P90 Pin Function Control Register	P90PFS	8	8	2 or 3 PCLKB	section 19.
0008 C189h	MPC	P91 Pin Function Control Register	P91PFS	8	8	2 or 3 PCLKB	section 19.
0008 C18Ah	MPC	P92 Pin Function Control Register	P92PFS	8	8	2 or 3 PCLKB	section 19.
0008 C18Bh	MPC	P93 Pin Function Control Register	P93PFS	8	8	2 or 3 PCLKB	section 19.
0008 C18Ch	MPC	P94 Pin Function Control Register	P94PFS	8	8	2 or 3 PCLKB	section 19.
0008 C18Dh	MPC	P95 Pin Function Control Register	P95PFS	8	8	2 or 3 PCLKB	section 19.
0008 C18Eh	MPC	P96 Pin Function Control Register	P96PFS	8	8	2 or 3 PCLKB	section 19.
0008 C190h	MPC	PA0 Pin Function Control Register	PA0PFS	8	8	2 or 3 PCLKB	section 19.
0008 C191h	MPC	PA1 Pin Function Control Register	PA1PFS	8	8	2 or 3 PCLKB	section 19.
0008 C192h	MPC	PA2 Pin Function Control Register	PA2PFS	8	8	2 or 3 PCLKB	section 19.
0008 C193h	MPC	PA3 Pin Function Control Register	PA3PFS	8	8	2 or 3 PCLKB	section 19.
0008 C194h	MPC	PA4 Pin Function Control Register	PA4PFS	8	8	2 or 3 PCLKB	section 19.
0008 C195h	MPC	PA5 Pin Function Control Register	PA5PFS	8	8	2 or 3 PCLKB	section 19.
0008 C196h	MPC	PA6 Pin Function Control Register	PA6PFS	8	8	2 or 3 PCLKB	section 19.
0008 C197h	MPC	PA7 Pin Function Control Register	PA7PFS	8	8	2 or 3 PCLKB	section 19.

Table 5.1 List of I/O Registers (Address Order) (22/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Reference Section
0008 C198h	MPC	PB0 Pin Function Control Register	PB0PFS	8	8	2 or 3 PCLKB	section 19.
0008 C199h	MPC	PB1 Pin Function Control Register	PB1PFS	8	8	2 or 3 PCLKB	section 19.
0008 C19Ah	MPC	PB2 Pin Function Control Register	PB2PFS	8	8	2 or 3 PCLKB	section 19.
0008 C19Bh	MPC	PB3 Pin Function Control Register	PB3PFS	8	8	2 or 3 PCLKB	section 19.
0008 C19Ch	MPC	PB4 Pin Function Control Register	PB4PFS	8	8	2 or 3 PCLKB	section 19.
0008 C19Dh	MPC	PB5 Pin Function Control Register	PB5PFS	8	8	2 or 3 PCLKB	section 19.
0008 C19Eh	MPC	PB6 Pin Function Control Register	PB6PFS	8	8	2 or 3 PCLKB	section 19.
0008 C19Fh	MPC	PB7 Pin Function Control Register	PB7PFS	8	8	2 or 3 PCLKB	section 19.
0008 C1A0h	MPC	PC0 Pin Function Control Register	PC0PFS	8	8	2 or 3 PCLKB	section 19.
0008 C1A1h	MPC	PC1 Pin Function Control Register	PC1PFS	8	8	2 or 3 PCLKB	section 19.
0008 C1A2h	MPC	PC2 Pin Function Control Register	PC2PFS	8	8	2 or 3 PCLKB	section 19.
0008 C1A3h	MPC	PC3 Pin Function Control Register	PC3PFS	8	8	2 or 3 PCLKB	section 19.
0008 C1A4h	MPC	PC4 Pin Function Control Register	PC4PFS	8	8	2 or 3 PCLKB	section 19.
0008 C1A5h	MPC	PC5 Pin Function Control Register	PC5PFS	8	8	2 or 3 PCLKB	section 19.
0008 C1A6h	MPC	PC6 Pin Function Control Register	PC6PFS	8	8	2 or 3 PCLKB	section 19.
0008 C1A8h	MPC	PD0 Pin Function Control Register	PD0PFS	8	8	2 or 3 PCLKB	section 19.
0008 C1A9h	MPC	PD1 Pin Function Control Register	PD1PFS	8	8	2 or 3 PCLKB	section 19.
0008 C1AAh	MPC	PD2 Pin Function Control Register	PD2PFS	8	8	2 or 3 PCLKB	section 19.
0008 C1ABh	MPC	PD3 Pin Function Control Register	PD3PFS	8	8	2 or 3 PCLKB	section 19.
0008 C1ACh	MPC	PD4 Pin Function Control Register	PD4PFS	8	8	2 or 3 PCLKB	section 19.
0008 C1ADh	MPC	PD5 Pin Function Control Register	PD5PFS	8	8	2 or 3 PCLKB	section 19.
0008 C1AEh	MPC	PD6 Pin Function Control Register	PD6PFS	8	8	2 or 3 PCLKB	section 19.
0008 C1AFh	MPC	PD7 Pin Function Control Register	PD7PFS	8	8	2 or 3 PCLKB	section 19.
0008 C1B0h	MPC	PE0 Pin Function Control Register	PE0PFS	8	8	2 or 3 PCLKB	section 19.
0008 C1B1h	MPC	PE1 Pin Function Control Register	PE1PFS	8	8	2 or 3 PCLKB	section 19.
0008 C1B2h	MPC	PE2 Pin Function Control Register	PE2PFS	8	8	2 or 3 PCLKB	section 19.
0008 C1B3h	MPC	PE3 Pin Function Control Register	PE3PFS	8	8	2 or 3 PCLKB	section 19.
0008 C1B4h	MPC	PE4 Pin Function Control Register	PE4PFS	8	8	2 or 3 PCLKB	section 19.
0008 C1B5h	MPC	PE5 Pin Function Control Register	PE5PFS	8	8	2 or 3 PCLKB	section 19.
0008 C1B6h	MPC	PE6 Pin Function Control Register	PE6PFS	8	8	2 or 3 PCLKB	section 19.
0008 C1B8h	MPC	PF0 Pin Function Control Register	PF0PFS	8	8	2 or 3 PCLKB	section 19.
0008 C1B9h	MPC	PF1 Pin Function Control Register	PF1PFS	8	8	2 or 3 PCLKB	section 19.
0008 C1BAh	MPC	PF2 Pin Function Control Register	PF2PFS	8	8	2 or 3 PCLKB	section 19.
0008 C1BBh	MPC	PF3 Pin Function Control Register	PF3PFS	8	8	2 or 3 PCLKB	section 19.
0008 C1C0h	MPC	PG0 Pin Function Control Register	PG0PFS	8	8	2 or 3 PCLKB	section 19.
0008 C1C1h	MPC	PG1 Pin Function Control Register	PG1PFS	8	8	2 or 3 PCLKB	section 19.
0008 C1C2h	MPC	PG2 Pin Function Control Register	PG2PFS	8	8	2 or 3 PCLKB	section 19.
0008 C290h	SYSTEM	Reset Status Register 0	RSTSR0	8	8	4 or 5 PCLKB	section 6.
0008 C291h	SYSTEM	Reset Status Register 1	RSTSR1	8	8	4 or 5 PCLKB	section 6.
0008 C293h	SYSTEM	Main Clock Oscillator Forced Oscillation Control Register	MOFCR	8	8	4 or 5 PCLKB	section 9.
0008 C297h	SYSTEM	Voltage Monitoring Circuit Control Register	LVCMPCR	8	8	4 or 5 PCLKB	section 8.
0008 C298h	SYSTEM	Voltage Detection Level Select Register	LVDLVLR	8	8	4 or 5 PCLKB	section 8.
0008 C29Ah	SYSTEM	Voltage Monitoring 1 Circuit Control Register 0	LVD1CR0	8	8	4 or 5 PCLKB	section 8.
0008 C29Bh	SYSTEM	Voltage Monitoring 2 Circuit Control Register 0	LVD2CR0	8	8	4 or 5 PCLKB	section 8.
0008 C4C0h	POE	Input Level Control/Status Register 1	ICSR1	16	8, 16	2 or 3 PCLKB	section 21.
0008 C4C2h	POE	Output Level Control/Status Register 1	OCSR1	16	8, 16	2 or 3 PCLKB	section 21.
0008 C4C4h	POE	Input Level Control/Status Register 2	ICSR2	16	8, 16	2 or 3 PCLKB	section 21.
0008 C4C6h	POE	Output Level Control/Status Register 2	OCSR2	16	8, 16	2 or 3 PCLKB	section 21.
0008 C4C8h	POE	Input Level Control/Status Register 3	ICSR3	16	8, 16	2 or 3 PCLKB	section 21.
0008 C4CAh	POE	Software Port Output Enable Register	SPOER	8	8	2 or 3 PCLKB	section 21.
0008 C4CBh	POE	Port Output Enable Control Register 1	POECR1	8	8	2 or 3 PCLKB	section 21.

Table 5.1 List of I/O Registers (Address Order) (23/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Reference Section
0008 C4CCh	POE	Port Output Enable Control Register 2	POECR2	16	16	2 or 3 PCLKB	section 21.
0008 C4CEh	POE	Port Output Enable Control Register 3	POECR3	16	16	2 or 3 PCLKB	section 21.
0008 C4D0h	POE	Port Output Enable Control Register 4	POECR4	16	16	2 or 3 PCLKB	section 21.
0008 C4D2h	POE	Port Output Enable Control Register 5	POECR5	16	16	2 or 3 PCLKB	section 21.
0008 C4D4h	POE	Port Output Enable Control Register 6	POECR6	16	16	2 or 3 PCLKB	section 21.
0008 C4D6h	POE	Input Level Control/Status Register 4	ICSR4	16	8, 16	2 or 3 PCLKB	section 21.
0008 C4D8h	POE	Input Level Control/Status Register 5	ICSR5	16	8, 16	2 or 3 PCLKB	section 21.
0008 C4DAh	POE	Active Level Setting Register 1	ALR1	16	8, 16	2 or 3 PCLKB	section 21.
0008 C4DCh	POE	Input Level Control/Status Register 6	ICSR6	16	16	2 or 3 PCLKB	section 21.
0008 C4DEh	POE	Active Level Setting Register 2	ALR2	16	8, 16	2 or 3 PCLKB	section 21.
0008 C4E0h	POE	Input Level Control/Status Register 7	ICSR7	16	8, 16	2 or 3 PCLKB	section 21.
0008 C4E2h	POE	Port Output Enable Control Register 7	POECR7	16	16	2 or 3 PCLKB	section 21.
0008 C4E4h	POE	Port Output Enable Control Register 8	POECR8	16	16	2 or 3 PCLKB	section 21.
0008 C4E6h	POE	Port Output Enable Comparator Output Detection Flag Register	POECMPFR	16	16	2 or 3 PCLKB	section 21.
0008 C4E8h	POE	Port Output Enable Comparator Request Select Register	POECMPSEL	16	16	2 or 3 PCLKB	section 21.
0008 C4EAh	POE	Output Level Control/Status Register 3	OCSR3	16	8, 16	2 or 3 PCLKB	section 21.
0008 C4ECh	POE	Active Level Setting Register 3	ALR3	16	8, 16	2 or 3 PCLKB	section 21.
0008 C4F0h	POE	Port Mode Mask Control Register 0	PMMCR0	8	8	2 or 3 PCLKB	section 21.
0008 C4F2h	POE	Port Mode Mask Control Register 1	PMMCR1	16	16	2 or 3 PCLKB	section 21.
0008 C4F4h	POE	Port Mode Mask Control Register 2	PMMCR2	16	16	2 or 3 PCLKB	section 21.
0008 C4F6h	POE	Port Mode Mask Control Register 3	PMMCR3	16	16	2 or 3 PCLKB	section 21.
0008 C4F8h	POE	Port Output Enable Comparator Request Extended Selection Register 0	POECMPEX0	8	8	2 or 3 PCLKB	section 21.
0008 C4F9h	POE	Port Output Enable Comparator Request Extended Selection Register 1	POECMPEX1	8	8	2 or 3 PCLKB	section 21.
0008 C4FAh	POE	Port Output Enable Comparator Request Extended Selection Register 2	POECMPEX2	8	8	2 or 3 PCLKB	section 21.
0008 C4FBh	POE	Port Output Enable Comparator Request Extended Selection Register 3	POECMPEX3	8	8	2 or 3 PCLKB	section 21.
0008 C4FCh	POE	Port Output Enable Comparator Request Extended Selection Register 4	POECMPEX4	8	8	2 or 3 PCLKB	section 21.
0008 C4FDh	POE	Port Output Enable Comparator Request Extended Selection Register 5	POECMPEX5	8	8	2 or 3 PCLKB	section 21.
000A 0C80h	CMPC0	Comparator Control Register 0	CMPCTL	8	8	1 or 2 PCLKB	section 33.
000A 0C84h	CMPC0	Comparator Input Select Register 0	CMPSEL0	8	8	1 or 2 PCLKB	section 33.
000A 0C88h	CMPC0	Comparator Reference Voltage Select Register 0	CMPSEL1	8	8	1 or 2 PCLKB	section 33.
000A 0C8Ch	CMPC0	Comparator Output Monitor Register 0	CMPMON	8	8	1 or 2 PCLKB	section 33.
000A 0C90h	CMPC0	Comparator External Output Enable Register 0	CMPIOC	8	8	1 or 2 PCLKB	section 33.
000A 0CA0h	CMPC1	Comparator Control Register 1	CMPCTL	8	8	1 or 2 PCLKB	section 33.
000A 0CA4h	CMPC1	Comparator Input Select Register 1	CMPSEL0	8	8	1 or 2 PCLKB	section 33.
000A 0CA8h	CMPC1	Comparator Reference Voltage Select Register 1	CMPSEL1	8	8	1 or 2 PCLKB	section 33.
000A 0CACh	CMPC1	Comparator Output Monitor Register 1	CMPMON	8	8	1 or 2 PCLKB	section 33.
000A 0CB0h	CMPC1	Comparator External Output Enable Register 1	CMPIOC	8	8	1 or 2 PCLKB	section 33.
000A 0CC0h	CMPC2	Comparator Control Register 2	CMPCTL	8	8	1 or 2 PCLKB	section 33.
000A 0CC4h	CMPC2	Comparator Input Select Register 2	CMPSEL0	8	8	1 or 2 PCLKB	section 33.
000A 0CC8h	CMPC2	Comparator Reference Voltage Select Register 2	CMPSEL1	8	8	1 or 2 PCLKB	section 33.
000A 0CCCh	CMPC2	Comparator Output Monitor Register 2	CMPMON	8	8	1 or 2 PCLKB	section 33.
000A 0CD0h	CMPC2	Comparator External Output Enable Register 2	CMPIOC	8	8	1 or 2 PCLKB	section 33.
000A 0CE0h	CMPC3	Comparator Control Register 3	CMPCTL	8	8	1 or 2 PCLKB	section 33.
000A 0CE4h	CMPC3	Comparator Input Select Register 3	CMPSEL0	8	8	1 or 2 PCLKB	section 33.
000A 0CE8h	CMPC3	Comparator Reference Voltage Select Register 3	CMPSEL1	8	8	1 or 2 PCLKB	section 33.
000A 0CECh	CMPC3	Comparator Output Monitor Register 3	CMPMON	8	8	1 or 2 PCLKB	section 33.
000A 0CF0h	CMPC3	Comparator External Output Enable Register 3	CMPIOC	8	8	1 or 2 PCLKB	section 33.

Table 5.1 List of I/O Registers (Address Order) (24/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Reference Section
000A 8300h	RSCAN0	Bit Configuration Register L	CFGL	16	16	2 or 3 PCLKB	section 28.
000A 8302h	RSCAN0	Bit Configuration Register H	CFGH	16	16	2 or 3 PCLKB	section 28.
000A 8304h	RSCAN0	Control Register L	CTRL	16	16	2 or 3 PCLKB	section 28.
000A 8306h	RSCAN0	Control Register H	CTRH	16	16	2 or 3 PCLKB	section 28.
000A 8308h	RSCAN0	Status Register L	STSL	16	16	2 or 3 PCLKB	section 28.
000A 830Ah	RSCAN0	Status Register H	STSH	16	16	2 or 3 PCLKB	section 28.
000A 830Ch	RSCAN0	Error Flag Register L	ERFLL	16	16	2 or 3 PCLKB	section 28.
000A 830Eh	RSCAN0	Error Flag Register H	ERFLH	16	16	2 or 3 PCLKB	section 28.
000A 8322h	RSCAN	Global Configuration Register L	GCFGL	16	16	2 or 3 PCLKB	section 28.
000A 8324h	RSCAN	Global Configuration Register H	GCFGH	16	16	2 or 3 PCLKB	section 28.
000A 8326h	RSCAN	Global Control Register L	GCTRL	16	16	2 or 3 PCLKB	section 28.
000A 8328h	RSCAN	Global Control Register H	GCTRH	16	16	2 or 3 PCLKB	section 28.
000A 832Ah	RSCAN	Global Status Register	GSTS	16	16	2 or 3 PCLKB	section 28.
000A 832Ch	RSCAN	Global Error Flag Register	GERFLL	8	8	1 or 2 PCLKB	section 28.
000A 832Eh	RSCAN	Timestamp Register	GTSC	16	16	2 or 3 PCLKB	section 28.
000A 8330h	RSCAN	Receive Rule Number Configuration Register	GAFLCFG	16	16	2 or 3 PCLKB	section 28.
000A 8332h	RSCAN	Receive Buffer Number Configuration Register	RMNB	16	16	2 or 3 PCLKB	section 28.
000A 8334h	RSCAN	Receive Buffer Receive Complete Flag Register	RMND0	16	16	2 or 3 PCLKB	section 28.
000A 8338h	RSCAN	Receive FIFO Control Register 0	RFCC0	16	16	2 or 3 PCLKB	section 28.
000A 833Ah	RSCAN	Receive FIFO Control Register 1	RFCC1	16	16	2 or 3 PCLKB	section 28.
000A 8340h	RSCAN	Receive FIFO Status Register 0	RFSTS0	16	16	2 or 3 PCLKB	section 28.
000A 8342h	RSCAN	Receive FIFO Status Register 1	RFSTS1	16	16	2 or 3 PCLKB	section 28.
000A 8348h	RSCAN	Receive FIFO Pointer Control Register 0	RFPCTR0	16	16	2 or 3 PCLKB	section 28.
000A 834Ah	RSCAN	Receive FIFO Pointer Control Register 1	RFPCTR1	16	16	2 or 3 PCLKB	section 28.
000A 8350h	RSCAN0	Transmit/Receive FIFO Control Register 0L	CFCCL0	16	16	2 or 3 PCLKB	section 28.
000A 8352h	RSCAN0	Transmit/Receive FIFO Control Register 0H	CFCCH0	16	16	2 or 3 PCLKB	section 28.
000A 8358h	RSCAN0	Transmit/Receive FIFO Status Register 0	CFSTS0	16	16	2 or 3 PCLKB	section 28.
000A 835Ch	RSCAN0	Transmit/Receive FIFO Pointer Control Register 0	CFPCTR0	16	16	2 or 3 PCLKB	section 28.
000A 8360h	RSCAN	Receive FIFO Message Lost Status Register	RFMSTS	8	8	1 or 2 PCLKB	section 28.
000A 8361h	RSCAN0	Transmit/Receive FIFO Message Lost Status Register	CFMSTS	8	8	1 or 2 PCLKB	section 28.
000A 8362h	RSCAN	Receive FIFO Interrupt Status Register	RFISTS	8	8	1 or 2 PCLKB	section 28.
000A 8363h	RSCAN	Transmit/Receive FIFO Receive Interrupt Status Register	CFISTS	8	8	1 or 2 PCLKB	section 28.
000A 8364h	RSCAN0	Transmit Buffer Control Register 0	TMC0	8	8	1 or 2 PCLKB	section 28.
000A 8365h	RSCAN0	Transmit Buffer Control Register 1	TMC1	8	8	1 or 2 PCLKB	section 28.
000A 8366h	RSCAN0	Transmit Buffer Control Register 2	TMC2	8	8	1 or 2 PCLKB	section 28.
000A 8367h	RSCAN0	Transmit Buffer Control Register 3	TMC3	8	8	1 or 2 PCLKB	section 28.
000A 836Ch	RSCAN0	Transmit Buffer Status Register 0	TMSTS0	8	8	1 or 2 PCLKB	section 28.
000A 836Dh	RSCAN0	Transmit Buffer Status Register 1	TMSTS1	8	8	1 or 2 PCLKB	section 28.
000A 836Eh	RSCAN0	Transmit Buffer Status Register 2	TMSTS2	8	8	1 or 2 PCLKB	section 28.
000A 836Fh	RSCAN0	Transmit Buffer Status Register 3	TMSTS3	8	8	1 or 2 PCLKB	section 28.
000A 8374h	RSCAN0	Transmit Buffer Transmit Request Status Register	TMTRSTS	16	16	2 or 3 PCLKB	section 28.
000A 8376h	RSCAN0	Transmit Buffer Transmit Complete Status Register	TMTCSTS	16	16	2 or 3 PCLKB	section 28.
000A 8378h	RSCAN0	Transmit Buffer Transmit Abort Status Register	TMTASTS	16	16	2 or 3 PCLKB	section 28.
000A 837Ah	RSCAN0	Transmit Buffer Interrupt Enable Register	TMIEC	16	16	2 or 3 PCLKB	section 28.
000A 837Ch	RSCAN0	Transmit History Buffer Control Register	THLCC0	16	16	2 or 3 PCLKB	section 28.
000A 8380h	RSCAN0	Transmit History Buffer Status Register	THLSTS0	16	16	2 or 3 PCLKB	section 28.
000A 8384h	RSCAN0	Transmit History Buffer Pointer Control Register	THLPCTR0	16	16	2 or 3 PCLKB	section 28.
000A 8388h	RSCAN	Global Transmit Interrupt Status Register	GTINTSTS	16	16	2 or 3 PCLKB	section 28.
000A 838Ah	RSCAN	Global RAM Window Control Register	GRWCR	16	16	2 or 3 PCLKB	section 28.
000A 838Ch	RSCAN	Global Test Configuration Register	GTSTCFG	16	16	2 or 3 PCLKB	section 28.
000A 838Eh	RSCAN	Global Test Control Register	GTSTCTRL	8	8	1 or 2 PCLKB	section 28.

Table 5.1 List of I/O Registers (Address Order) (25/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Reference Section
000A 8394h	RSCAN	Global Test Protection Unlock Register	GLOCKK	16	16	2 or 3 PCLKB	section 28.
000A 83A0h	RSCAN	Receive Rule Entry Register 0AL	GAFLIDL0	16	16	2 or 3 PCLKB	section 28.
000A 83A0h	RSCAN	Receive Buffer Register 0AL	RMIDL0	16	16	2 or 3 PCLKB	section 28.
000A 83A2h	RSCAN	Receive Rule Entry Register 0AH	GAFLIDH0	16	16	2 or 3 PCLKB	section 28.
000A 83A2h	RSCAN	Receive Buffer Register 0AH	RMIDH0	16	16	2 or 3 PCLKB	section 28.
000A 83A4h	RSCAN	Receive Rule Entry Register 0BL	GAFLML0	16	16	2 or 3 PCLKB	section 28.
000A 83A4h	RSCAN	Receive Buffer Register 0BL	RMTS0	16	16	2 or 3 PCLKB	section 28.
000A 83A6h	RSCAN	Receive Rule Entry Register 0BH	GAFLMH0	16	16	2 or 3 PCLKB	section 28.
000A 83A6h	RSCAN	Receive Buffer Register 0BH	RMPTR0	16	16	2 or 3 PCLKB	section 28.
000A 83A8h	RSCAN	Receive Rule Entry Register 0CL	GAFLPL0	16	16	2 or 3 PCLKB	section 28.
000A 83A8h	RSCAN	Receive Buffer Register 0CL	RMDF00	16	16	2 or 3 PCLKB	section 28.
000A 83AAh	RSCAN	Receive Rule Entry Register 0CH	GAFLPH0	16	16	2 or 3 PCLKB	section 28.
000A 83AAh	RSCAN	Receive Buffer Register 0CH	RMDF10	16	16	2 or 3 PCLKB	section 28.
000A 83ACh	RSCAN	Receive Rule Entry Register 1AL	GAFLIDL1	16	16	2 or 3 PCLKB	section 28.
000A 83ACh	RSCAN	Receive Buffer Register 0DL	RMDF20	16	16	2 or 3 PCLKB	section 28.
000A 83AEh	RSCAN	Receive Rule Entry Register 1AH	GAFLIDH1	16	16	2 or 3 PCLKB	section 28.
000A 83AEh	RSCAN	Receive Buffer Register 0DH	RMDF30	16	16	2 or 3 PCLKB	section 28.
000A 83B0h	RSCAN	Receive Rule Entry Register 1BL	GAFLML1	16	16	2 or 3 PCLKB	section 28.
000A 83B0h	RSCAN	Receive Buffer Register 1AL	RMIDL1	16	16	2 or 3 PCLKB	section 28.
000A 83B2h	RSCAN	Receive Rule Entry Register 1BH	GAFLMH1	16	16	2 or 3 PCLKB	section 28.
000A 83B2h	RSCAN	Receive Buffer Register 1AH	RMIDH1	16	16	2 or 3 PCLKB	section 28.
000A 83B4h	RSCAN	Receive Rule Entry Register 1CL	GAFLPL1	16	16	2 or 3 PCLKB	section 28.
000A 83B4h	RSCAN	Receive Buffer Register 1BL	RMTS1	16	16	2 or 3 PCLKB	section 28.
000A 83B6h	RSCAN	Receive Rule Entry Register 1CH	GAFLPH1	16	16	2 or 3 PCLKB	section 28.
000A 83B6h	RSCAN	Receive Buffer Register 1BH	RMPTR1	16	16	2 or 3 PCLKB	section 28.
000A 83B8h	RSCAN	Receive Rule Entry Register 2AL	GAFLIDL2	16	16	2 or 3 PCLKB	section 28.
000A 83B8h	RSCAN	Receive Buffer Register 1CL	RMDF01	16	16	2 or 3 PCLKB	section 28.
000A 83BAh	RSCAN	Receive Rule Entry Register 2AH	GAFLIDH2	16	16	2 or 3 PCLKB	section 28.
000A 83BAh	RSCAN	Receive Buffer Register 1CH	RMDF11	16	16	2 or 3 PCLKB	section 28.
000A 83BCh	RSCAN	Receive Rule Entry Register 2BL	GAFLML2	16	16	2 or 3 PCLKB	section 28.
000A 83BCh	RSCAN	Receive Buffer Register 1DL	RMDF21	16	16	2 or 3 PCLKB	section 28.
000A 83BEh	RSCAN	Receive Rule Entry Register 2BH	GAFLMH2	16	16	2 or 3 PCLKB	section 28.
000A 83BEh	RSCAN	Receive Buffer Register 1DH	RMDF31	16	16	2 or 3 PCLKB	section 28.
000A 83C0h	RSCAN	Receive Rule Entry Register 2CL	GAFLPL2	16	16	2 or 3 PCLKB	section 28.
000A 83C0h	RSCAN	Receive Buffer Register 2AL	RMIDL2	16	16	2 or 3 PCLKB	section 28.
000A 83C2h	RSCAN	Receive Rule Entry Register 2CH	GAFLPH2	16	16	2 or 3 PCLKB	section 28.
000A 83C2h	RSCAN	Receive Buffer Register 2AH	RMIDH2	16	16	2 or 3 PCLKB	section 28.
000A 83C4h	RSCAN	Receive Rule Entry Register 3AL	GAFLIDL3	16	16	2 or 3 PCLKB	section 28.
000A 83C4h	RSCAN	Receive Buffer Register 2BL	RMTS2	16	16	2 or 3 PCLKB	section 28.
000A 83C6h	RSCAN	Receive Rule Entry Register 3AH	GAFLIDH3	16	16	2 or 3 PCLKB	section 28.
000A 83C6h	RSCAN	Receive Buffer Register 2BH	RMPTR2	16	16	2 or 3 PCLKB	section 28.
000A 83C8h	RSCAN	Receive Rule Entry Register 3BL	GAFLML3	16	16	2 or 3 PCLKB	section 28.
000A 83C8h	RSCAN	Receive Buffer Register 2CL	RMDF02	16	16	2 or 3 PCLKB	section 28.
000A 83CAh	RSCAN	Receive Rule Entry Register 3BH	GAFLMH3	16	16	2 or 3 PCLKB	section 28.
000A 83CAh	RSCAN	Receive Buffer Register 2CH	RMDF12	16	16	2 or 3 PCLKB	section 28.
000A 83CCh	RSCAN	Receive Rule Entry Register 3CL	GAFLPL3	16	16	2 or 3 PCLKB	section 28.
000A 83CCh	RSCAN	Receive Buffer Register 2DL	RMDF22	16	16	2 or 3 PCLKB	section 28.
000A 83CEh	RSCAN	Receive Rule Entry Register 3CH	GAFLPH3	16	16	2 or 3 PCLKB	section 28.
000A 83CEh	RSCAN	Receive Buffer Register 2DH	RMDF32	16	16	2 or 3 PCLKB	section 28.
000A 83D0h	RSCAN	Receive Rule Entry Register 4AL	GAFLIDL4	16	16	2 or 3 PCLKB	section 28.
000A 83D0h	RSCAN	Receive Buffer Register 3AL	RMIDL3	16	16	2 or 3 PCLKB	section 28.

Table 5.1 List of I/O Registers (Address Order) (26/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Reference Section
000A 83D2h	RSCAN	Receive Rule Entry Register 4AH	GAFLIDH4	16	16	2 or 3 PCLKB	section 28.
000A 83D2h	RSCAN	Receive Buffer Register 3AH	RMIDH3	16	16	2 or 3 PCLKB	section 28.
000A 83D4h	RSCAN	Receive Rule Entry Register 4BL	GAFLML4	16	16	2 or 3 PCLKB	section 28.
000A 83D4h	RSCAN	Receive Buffer Register 3BL	RMTS3	16	16	2 or 3 PCLKB	section 28.
000A 83D6h	RSCAN	Receive Rule Entry Register 4BH	GAFLMH4	16	16	2 or 3 PCLKB	section 28.
000A 83D6h	RSCAN	Receive Buffer Register 3BH	RMPTR3	16	16	2 or 3 PCLKB	section 28.
000A 83D8h	RSCAN	Receive Rule Entry Register 4CL	GAFLPL4	16	16	2 or 3 PCLKB	section 28.
000A 83D8h	RSCAN	Receive Buffer Register 3CL	RMDF03	16	16	2 or 3 PCLKB	section 28.
000A 83DAh	RSCAN	Receive Rule Entry Register 4CH	GAFLPH4	16	16	2 or 3 PCLKB	section 28.
000A 83DAh	RSCAN	Receive Buffer Register 3CH	RMDF13	16	16	2 or 3 PCLKB	section 28.
000A 83DCh	RSCAN	Receive Rule Entry Register 5AL	GAFLIDL5	16	16	2 or 3 PCLKB	section 28.
000A 83DCh	RSCAN	Receive Buffer Register 3DL	RMDF23	16	16	2 or 3 PCLKB	section 28.
000A 83DEh	RSCAN	Receive Rule Entry Register 5AH	GAFLIDH5	16	16	2 or 3 PCLKB	section 28.
000A 83DEh	RSCAN	Receive Buffer Register 3DH	RMDF33	16	16	2 or 3 PCLKB	section 28.
000A 83E0h	RSCAN	Receive Rule Entry Register 5BL	GAFLML5	16	16	2 or 3 PCLKB	section 28.
000A 83E0h	RSCAN	Receive Buffer Register 4AL	RMIDL4	16	16	2 or 3 PCLKB	section 28.
000A 83E2h	RSCAN	Receive Rule Entry Register 5BH	GAFLMH5	16	16	2 or 3 PCLKB	section 28.
000A 83E2h	RSCAN	Receive Buffer Register 4AH	RMIDH4	16	16	2 or 3 PCLKB	section 28.
000A 83E4h	RSCAN	Receive Rule Entry Register 5CL	GAFLPL5	16	16	2 or 3 PCLKB	section 28.
000A 83E4h	RSCAN	Receive Buffer Register 4BL	RMTS4	16	16	2 or 3 PCLKB	section 28.
000A 83E6h	RSCAN	Receive Rule Entry Register 5CH	GAFLPH5	16	16	2 or 3 PCLKB	section 28.
000A 83E6h	RSCAN	Receive Buffer Register 4BH	RMPTR4	16	16	2 or 3 PCLKB	section 28.
000A 83E8h	RSCAN	Receive Rule Entry Register 6AL	GAFLIDL6	16	16	2 or 3 PCLKB	section 28.
000A 83E8h	RSCAN	Receive Buffer Register 4CL	RMDF04	16	16	2 or 3 PCLKB	section 28.
000A 83EAh	RSCAN	Receive Rule Entry Register 6AH	GAFLIDH6	16	16	2 or 3 PCLKB	section 28.
000A 83EAh	RSCAN	Receive Buffer Register 4CH	RMDF14	16	16	2 or 3 PCLKB	section 28.
000A 83ECh	RSCAN	Receive Rule Entry Register 6BL	GAFLML6	16	16	2 or 3 PCLKB	section 28.
000A 83ECh	RSCAN	Receive Buffer Register 4DL	RMDF24	16	16	2 or 3 PCLKB	section 28.
000A 83EEh	RSCAN	Receive Rule Entry Register 6BH	GAFLMH6	16	16	2 or 3 PCLKB	section 28.
000A 83EEh	RSCAN	Receive Buffer Register 4DH	RMDF34	16	16	2 or 3 PCLKB	section 28.
000A 83F0h	RSCAN	Receive Rule Entry Register 6CL	GAFLPL6	16	16	2 or 3 PCLKB	section 28.
000A 83F0h	RSCAN	Receive Buffer Register 5AL	RMIDL5	16	16	2 or 3 PCLKB	section 28.
000A 83F2h	RSCAN	Receive Rule Entry Register 6CH	GAFLPH6	16	16	2 or 3 PCLKB	section 28.
000A 83F2h	RSCAN	Receive Buffer Register 5AH	RMIDH5	16	16	2 or 3 PCLKB	section 28.
000A 83F4h	RSCAN	Receive Rule Entry Register 7AL	GAFLIDL7	16	16	2 or 3 PCLKB	section 28.
000A 83F4h	RSCAN	Receive Buffer Register 5BL	RMTS5	16	16	2 or 3 PCLKB	section 28.
000A 83F6h	RSCAN	Receive Rule Entry Register 7AH	GAFLIDH7	16	16	2 or 3 PCLKB	section 28.
000A 83F6h	RSCAN	Receive Buffer Register 5BH	RMPTR5	16	16	2 or 3 PCLKB	section 28.
000A 83F8h	RSCAN	Receive Rule Entry Register 7BL	GAFLML7	16	16	2 or 3 PCLKB	section 28.
000A 83F8h	RSCAN	Receive Buffer Register 5CL	RMDF05	16	16	2 or 3 PCLKB	section 28.
000A 83FAh	RSCAN	Receive Rule Entry Register 7BH	GAFLMH7	16	16	2 or 3 PCLKB	section 28.
000A 83FAh	RSCAN	Receive Buffer Register 5CH	RMDF15	16	16	2 or 3 PCLKB	section 28.
000A 83FCh	RSCAN	Receive Rule Entry Register 7CL	GAFLPL7	16	16	2 or 3 PCLKB	section 28.
000A 83FCh	RSCAN	Receive Buffer Register 5DL	RMDF25	16	16	2 or 3 PCLKB	section 28.
000A 83FEh	RSCAN	Receive Rule Entry Register 7CH	GAFLPH7	16	16	2 or 3 PCLKB	section 28.
000A 83FEh	RSCAN	Receive Buffer Register 5DH	RMDF35	16	16	2 or 3 PCLKB	section 28.
000A 8400h	RSCAN	Receive Rule Entry Register 8AL	GAFLIDL8	16	16	2 or 3 PCLKB	section 28.
000A 8400h	RSCAN	Receive Buffer Register 6AL	RMIDL6	16	16	2 or 3 PCLKB	section 28.
000A 8402h	RSCAN	Receive Rule Entry Register 8AH	GAFLIDH8	16	16	2 or 3 PCLKB	section 28.
000A 8402h	RSCAN	Receive Buffer Register 6AH	RMIDH6	16	16	2 or 3 PCLKB	section 28.
000A 8404h	RSCAN	Receive Rule Entry Register 8BL	GAFLML8	16	16	2 or 3 PCLKB	section 28.

Table 5.1 List of I/O Registers (Address Order) (27/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Reference Section
000A 8404h	RSCAN	Receive Buffer Register 6BL	RMTS6	16	16	2 or 3 PCLKB	section 28.
000A 8406h	RSCAN	Receive Rule Entry Register 8BH	GAFLMH8	16	16	2 or 3 PCLKB	section 28.
000A 8406h	RSCAN	Receive Buffer Register 6BH	RMPTR6	16	16	2 or 3 PCLKB	section 28.
000A 8408h	RSCAN	Receive Rule Entry Register 8CL	GAFLPL8	16	16	2 or 3 PCLKB	section 28.
000A 8408h	RSCAN	Receive Buffer Register 6CL	RMDF06	16	16	2 or 3 PCLKB	section 28.
000A 840Ah	RSCAN	Receive Rule Entry Register 8CH	GAFLPH8	16	16	2 or 3 PCLKB	section 28.
000A 840Ah	RSCAN	Receive Buffer Register 6CH	RMDF16	16	16	2 or 3 PCLKB	section 28.
000A 840Ch	RSCAN	Receive Rule Entry Register 9AL	GAFLIDL9	16	16	2 or 3 PCLKB	section 28.
000A 840Ch	RSCAN	Receive Buffer Register 6DL	RMDF26	16	16	2 or 3 PCLKB	section 28.
000A 840Eh	RSCAN	Receive Rule Entry Register 9AH	GAFLIDH9	16	16	2 or 3 PCLKB	section 28.
000A 840Eh	RSCAN	Receive Buffer Register 6DH	RMDF36	16	16	2 or 3 PCLKB	section 28.
000A 8410h	RSCAN	Receive Rule Entry Register 9BL	GAFLML9	16	16	2 or 3 PCLKB	section 28.
000A 8410h	RSCAN	Receive Buffer Register 7AL	RMIDL7	16	16	2 or 3 PCLKB	section 28.
000A 8412h	RSCAN	Receive Rule Entry Register 9BH	GAFLMH9	16	16	2 or 3 PCLKB	section 28.
000A 8412h	RSCAN	Receive Buffer Register 7AH	RMIDH7	16	16	2 or 3 PCLKB	section 28.
000A 8414h	RSCAN	Receive Rule Entry Register 9CL	GAFLPL9	16	16	2 or 3 PCLKB	section 28.
000A 8414h	RSCAN	Receive Buffer Register 7BL	RMTS7	16	16	2 or 3 PCLKB	section 28.
000A 8416h	RSCAN	Receive Rule Entry Register 9CH	GAFLPH9	16	16	2 or 3 PCLKB	section 28.
000A 8416h	RSCAN	Receive Buffer Register 7BH	RMPTR7	16	16	2 or 3 PCLKB	section 28.
000A 8418h	RSCAN	Receive Rule Entry Register 10AL	GAFLIDL10	16	16	2 or 3 PCLKB	section 28.
000A 8418h	RSCAN	Receive Buffer Register 7CL	RMDF07	16	16	2 or 3 PCLKB	section 28.
000A 841Ah	RSCAN	Receive Rule Entry Register 10AH	GAFLIDH10	16	16	2 or 3 PCLKB	section 28.
000A 841Ah	RSCAN	Receive Buffer Register 7CH	RMDF17	16	16	2 or 3 PCLKB	section 28.
000A 841Ch	RSCAN	Receive Rule Entry Register 10BL	GAFLML10	16	16	2 or 3 PCLKB	section 28.
000A 841Ch	RSCAN	Receive Buffer Register 7DL	RMDF27	16	16	2 or 3 PCLKB	section 28.
000A 841Eh	RSCAN	Receive Rule Entry Register 10BH	GAFLMH10	16	16	2 or 3 PCLKB	section 28.
000A 841Eh	RSCAN	Receive Buffer Register 7DH	RMDF37	16	16	2 or 3 PCLKB	section 28.
000A 8420h	RSCAN	Receive Rule Entry Register 10CL	GAFLPL10	16	16	2 or 3 PCLKB	section 28.
000A 8420h	RSCAN	Receive Buffer Register 8AL	RMIDL8	16	16	2 or 3 PCLKB	section 28.
000A 8422h	RSCAN	Receive Rule Entry Register 10CH	GAFLPH10	16	16	2 or 3 PCLKB	section 28.
000A 8422h	RSCAN	Receive Buffer Register 8AH	RMIDH8	16	16	2 or 3 PCLKB	section 28.
000A 8424h	RSCAN	Receive Rule Entry Register 11AL	GAFLIDL11	16	16	2 or 3 PCLKB	section 28.
000A 8424h	RSCAN	Receive Buffer Register 8BL	RMTS8	16	16	2 or 3 PCLKB	section 28.
000A 8426h	RSCAN	Receive Rule Entry Register 11AH	GAFLIDH11	16	16	2 or 3 PCLKB	section 28.
000A 8426h	RSCAN	Receive Buffer Register 8BH	RMPTR8	16	16	2 or 3 PCLKB	section 28.
000A 8428h	RSCAN	Receive Rule Entry Register 11BL	GAFLML11	16	16	2 or 3 PCLKB	section 28.
000A 8428h	RSCAN	Receive Buffer Register 8CL	RMDF08	16	16	2 or 3 PCLKB	section 28.
000A 842Ah	RSCAN	Receive Rule Entry Register 11BH	GAFLMH11	16	16	2 or 3 PCLKB	section 28.
000A 842Ah	RSCAN	Receive Buffer Register 8CH	RMDF18	16	16	2 or 3 PCLKB	section 28.
000A 842Ch	RSCAN	Receive Rule Entry Register 11CL	GAFLPL11	16	16	2 or 3 PCLKB	section 28.
000A 842Ch	RSCAN	Receive Buffer Register 8DL	RMDF28	16	16	2 or 3 PCLKB	section 28.
000A 842Eh	RSCAN	Receive Rule Entry Register 11CH	GAFLPH11	16	16	2 or 3 PCLKB	section 28.
000A 842Eh	RSCAN	Receive Buffer Register 8DH	RMDF38	16	16	2 or 3 PCLKB	section 28.
000A 8430h	RSCAN	Receive Rule Entry Register 12AL	GAFLIDL12	16	16	2 or 3 PCLKB	section 28.
000A 8430h	RSCAN	Receive Buffer Register 9AL	RMIDL9	16	16	2 or 3 PCLKB	section 28.
000A 8432h	RSCAN	Receive Rule Entry Register 12AH	GAFLIDH12	16	16	2 or 3 PCLKB	section 28.
000A 8432h	RSCAN	Receive Buffer Register 9AH	RMIDH9	16	16	2 or 3 PCLKB	section 28.
000A 8434h	RSCAN	Receive Rule Entry Register 12BL	GAFLML12	16	16	2 or 3 PCLKB	section 28.
000A 8434h	RSCAN	Receive Buffer Register 9BL	RMTS9	16	16	2 or 3 PCLKB	section 28.
000A 8436h	RSCAN	Receive Rule Entry Register 12BH	GAFLMH12	16	16	2 or 3 PCLKB	section 28.
000A 8436h	RSCAN	Receive Buffer Register 9BH	RMPTR9	16	16	2 or 3 PCLKB	section 28.

Table 5.1 List of I/O Registers (Address Order) (28/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Reference Section
000A 8438h	RSCAN	Receive Rule Entry Register 12CL	GAFLPL12	16	16	2 or 3 PCLKB	section 28.
000A 8438h	RSCAN	Receive Buffer Register 9CL	RMDF09	16	16	2 or 3 PCLKB	section 28.
000A 843Ah	RSCAN	Receive Rule Entry Register 12CH	GAFLPH12	16	16	2 or 3 PCLKB	section 28.
000A 843Ah	RSCAN	Receive Buffer Register 9CH	RMDF19	16	16	2 or 3 PCLKB	section 28.
000A 843Ch	RSCAN	Receive Rule Entry Register 13AL	GAFLIDL13	16	16	2 or 3 PCLKB	section 28.
000A 843Ch	RSCAN	Receive Buffer Register 9DL	RMDF29	16	16	2 or 3 PCLKB	section 28.
000A 843Eh	RSCAN	Receive Rule Entry Register 13AH	GAFLIDH13	16	16	2 or 3 PCLKB	section 28.
000A 843Eh	RSCAN	Receive Buffer Register 9DH	RMDF39	16	16	2 or 3 PCLKB	section 28.
000A 8440h	RSCAN	Receive Rule Entry Register 13BL	GAFLML13	16	16	2 or 3 PCLKB	section 28.
000A 8440h	RSCAN	Receive Buffer Register 10AL	RMIDL10	16	16	2 or 3 PCLKB	section 28.
000A 8442h	RSCAN	Receive Rule Entry Register 13BH	GAFLMH13	16	16	2 or 3 PCLKB	section 28.
000A 8442h	RSCAN	Receive Buffer Register 10AH	RMIDH10	16	16	2 or 3 PCLKB	section 28.
000A 8444h	RSCAN	Receive Rule Entry Register 13CL	GAFLPL13	16	16	2 or 3 PCLKB	section 28.
000A 8444h	RSCAN	Receive Buffer Register 10BL	RMTS10	16	16	2 or 3 PCLKB	section 28.
000A 8446h	RSCAN	Receive Rule Entry Register 13CH	GAFLPH13	16	16	2 or 3 PCLKB	section 28.
000A 8446h	RSCAN	Receive Buffer Register 10BH	RMPTR10	16	16	2 or 3 PCLKB	section 28.
000A 8448h	RSCAN	Receive Rule Entry Register 14AL	GAFLIDL14	16	16	2 or 3 PCLKB	section 28.
000A 8448h	RSCAN	Receive Buffer Register 10CL	RMDF010	16	16	2 or 3 PCLKB	section 28.
000A 844Ah	RSCAN	Receive Rule Entry Register 14AH	GAFLIDH14	16	16	2 or 3 PCLKB	section 28.
000A 844Ah	RSCAN	Receive Buffer Register 10CH	RMDF110	16	16	2 or 3 PCLKB	section 28.
000A 844Ch	RSCAN	Receive Rule Entry Register 14BL	GAFLML14	16	16	2 or 3 PCLKB	section 28.
000A 844Ch	RSCAN	Receive Buffer Register 10DL	RMDF210	16	16	2 or 3 PCLKB	section 28.
000A 844Eh	RSCAN	Receive Rule Entry Register 14BH	GAFLMH14	16	16	2 or 3 PCLKB	section 28.
000A 844Eh	RSCAN	Receive Buffer Register 10DH	RMDF310	16	16	2 or 3 PCLKB	section 28.
000A 8450h	RSCAN	Receive Rule Entry Register 14CL	GAFLPL14	16	16	2 or 3 PCLKB	section 28.
000A 8450h	RSCAN	Receive Buffer Register 11AL	RMIDL11	16	16	2 or 3 PCLKB	section 28.
000A 8452h	RSCAN	Receive Rule Entry Register 14CH	GAFLPH14	16	16	2 or 3 PCLKB	section 28.
000A 8452h	RSCAN	Receive Buffer Register 11AH	RMIDH11	16	16	2 or 3 PCLKB	section 28.
000A 8454h	RSCAN	Receive Rule Entry Register 15AL	GAFLIDL15	16	16	2 or 3 PCLKB	section 28.
000A 8454h	RSCAN	Receive Buffer Register 11BL	RMTS11	16	16	2 or 3 PCLKB	section 28.
000A 8456h	RSCAN	Receive Rule Entry Register 15AH	GAFLIDH15	16	16	2 or 3 PCLKB	section 28.
000A 8456h	RSCAN	Receive Buffer Register 11BH	RMPTR11	16	16	2 or 3 PCLKB	section 28.
000A 8458h	RSCAN	Receive Rule Entry Register 15BL	GAFLML15	16	16	2 or 3 PCLKB	section 28.
000A 8458h	RSCAN	Receive Buffer Register 11CL	RMDF011	16	16	2 or 3 PCLKB	section 28.
000A 845Ah	RSCAN	Receive Rule Entry Register 15BH	GAFLMH15	16	16	2 or 3 PCLKB	section 28.
000A 845Ah	RSCAN	Receive Buffer Register 11CH	RMDF111	16	16	2 or 3 PCLKB	section 28.
000A 845Ch	RSCAN	Receive Rule Entry Register 15CL	GAFLPL15	16	16	2 or 3 PCLKB	section 28.
000A 845Ch	RSCAN	Receive Buffer Register 11DL	RMDF211	16	16	2 or 3 PCLKB	section 28.
000A 845Eh	RSCAN	Receive Rule Entry Register 15CH	GAFLPH15	16	16	2 or 3 PCLKB	section 28.
000A 845Eh	RSCAN	Receive Buffer Register 11DH	RMDF311	16	16	2 or 3 PCLKB	section 28.
000A 8460h	RSCAN	Receive Buffer Register 12AL	RMIDL12	16	16	2 or 3 PCLKB	section 28.
000A 8462h	RSCAN	Receive Buffer Register 12AH	RMIDH12	16	16	2 or 3 PCLKB	section 28.
000A 8464h	RSCAN	Receive Buffer Register 12BL	RMTS12	16	16	2 or 3 PCLKB	section 28.
000A 8466h	RSCAN	Receive Buffer Register 12BH	RMPTR12	16	16	2 or 3 PCLKB	section 28.
000A 8468h	RSCAN	Receive Buffer Register 12CL	RMDF012	16	16	2 or 3 PCLKB	section 28.
000A 846Ah	RSCAN	Receive Buffer Register 12CH	RMDF112	16	16	2 or 3 PCLKB	section 28.
000A 846Ch	RSCAN	Receive Buffer Register 12DL	RMDF212	16	16	2 or 3 PCLKB	section 28.
000A 846Eh	RSCAN	Receive Buffer Register 12DH	RMDF312	16	16	2 or 3 PCLKB	section 28.
000A 8470h	RSCAN	Receive Buffer Register 13AL	RMIDL13	16	16	2 or 3 PCLKB	section 28.
000A 8472h	RSCAN	Receive Buffer Register 13AH	RMIDH13	16	16	2 or 3 PCLKB	section 28.
000A 8474h	RSCAN	Receive Buffer Register 13BL	RMTS13	16	16	2 or 3 PCLKB	section 28.

Table 5.1 List of I/O Registers (Address Order) (29/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Reference Section
000A 8476h	RSCAN	Receive Buffer Register 13BH	RMPTR13	16	16	2 or 3 PCLKB	section 28.
000A 8478h	RSCAN	Receive Buffer Register 13CL	RMDF013	16	16	2 or 3 PCLKB	section 28.
000A 847Ah	RSCAN	Receive Buffer Register 13CH	RMDF113	16	16	2 or 3 PCLKB	section 28.
000A 847Ch	RSCAN	Receive Buffer Register 13DL	RMDF213	16	16	2 or 3 PCLKB	section 28.
000A 847Eh	RSCAN	Receive Buffer Register 13DH	RMDF313	16	16	2 or 3 PCLKB	section 28.
000A 8480h	RSCAN	Receive Buffer Register 14AL	RMIDL14	16	16	2 or 3 PCLKB	section 28.
000A 8482h	RSCAN	Receive Buffer Register 14AH	RMIDH14	16	16	2 or 3 PCLKB	section 28.
000A 8484h	RSCAN	Receive Buffer Register 14BL	RMTS14	16	16	2 or 3 PCLKB	section 28.
000A 8486h	RSCAN	Receive Buffer Register 14BH	RMPTR14	16	16	2 or 3 PCLKB	section 28.
000A 8488h	RSCAN	Receive Buffer Register 14CL	RMDF014	16	16	2 or 3 PCLKB	section 28.
000A 848Ah	RSCAN	Receive Buffer Register 14CH	RMDF114	16	16	2 or 3 PCLKB	section 28.
000A 848Ch	RSCAN	Receive Buffer Register 14DL	RMDF214	16	16	2 or 3 PCLKB	section 28.
000A 848Eh	RSCAN	Receive Buffer Register 14DH	RMDF314	16	16	2 or 3 PCLKB	section 28.
000A 8490h	RSCAN	Receive Buffer Register 15AL	RMIDL15	16	16	2 or 3 PCLKB	section 28.
000A 8492h	RSCAN	Receive Buffer Register 15AH	RMIDH15	16	16	2 or 3 PCLKB	section 28.
000A 8494h	RSCAN	Receive Buffer Register 15BL	RMTS15	16	16	2 or 3 PCLKB	section 28.
000A 8496h	RSCAN	Receive Buffer Register 15BH	RMPTR15	16	16	2 or 3 PCLKB	section 28.
000A 8498h	RSCAN	Receive Buffer Register 15CL	RMDF015	16	16	2 or 3 PCLKB	section 28.
000A 849Ah	RSCAN	Receive Buffer Register 15CH	RMDF115	16	16	2 or 3 PCLKB	section 28.
000A 849Ch	RSCAN	Receive Buffer Register 15DL	RMDF215	16	16	2 or 3 PCLKB	section 28.
000A 849Eh	RSCAN	Receive Buffer Register 15DH	RMDF315	16	16	2 or 3 PCLKB	section 28.
000A 8580h to 000A 859Fh	RSCAN	RAM Test Register 0 to 15	RPGACC0 to 15	16	16	2 or 3 PCLKB	section 28.
000A 85A0h	RSCAN	Receive FIFO Access Register 0AL	RFIDL0	16	16	2 or 3 PCLKB	section 28.
000A 85A0h	RSCAN	RAM Test Register 16	RPGACC16	16	16	2 or 3 PCLKB	section 28.
000A 85A2h	RSCAN	Receive FIFO Access Register 0AH	RFIDH0	16	16	2 or 3 PCLKB	section 28.
000A 85A2h	RSCAN	RAM Test Register 17	RPGACC17	16	16	2 or 3 PCLKB	section 28.
000A 85A4h	RSCAN	Receive FIFO Access Register 0BL	RFTS0	16	16	2 or 3 PCLKB	section 28.
000A 85A4h	RSCAN	RAM Test Register 18	RPGACC18	16	16	2 or 3 PCLKB	section 28.
000A 85A6h	RSCAN	Receive FIFO Access Register 0BH	RFPTR0	16	16	2 or 3 PCLKB	section 28.
000A 85A6h	RSCAN	RAM Test Register 19	RPGACC19	16	16	2 or 3 PCLKB	section 28.
000A 85A8h	RSCAN	Receive FIFO Access Register 0CL	RFDF00	16	16	2 or 3 PCLKB	section 28.
000A 85A8h	RSCAN	RAM Test Register 20	RPGACC20	16	16	2 or 3 PCLKB	section 28.
000A 85AAh	RSCAN	Receive FIFO Access Register 0CH	RFDF10	16	16	2 or 3 PCLKB	section 28.
000A 85AAh	RSCAN	RAM Test Register 21	RPGACC21	16	16	2 or 3 PCLKB	section 28.
000A 85ACh	RSCAN	Receive FIFO Access Register 0DL	RFDF20	16	16	2 or 3 PCLKB	section 28.
000A 85ACh	RSCAN	RAM Test Register 22	RPGACC22	16	16	2 or 3 PCLKB	section 28.
000A 85AEh	RSCAN	Receive FIFO Access Register 0DH	RFDF30	16	16	2 or 3 PCLKB	section 28.
000A 85AEh	RSCAN	RAM Test Register 23	RPGACC23	16	16	2 or 3 PCLKB	section 28.
000A 85B0h	RSCAN	Receive FIFO Access Register 1AL	RFIDL1	16	16	2 or 3 PCLKB	section 28.
000A 85B0h	RSCAN	RAM Test Register 24	RPGACC24	16	16	2 or 3 PCLKB	section 28.
000A 85B2h	RSCAN	Receive FIFO Access Register 1AH	RFIDH1	16	16	2 or 3 PCLKB	section 28.
000A 85B2h	RSCAN	RAM Test Register 25	RPGACC25	16	16	2 or 3 PCLKB	section 28.
000A 85B4h	RSCAN	Receive FIFO Access Register 1BL	RFTS1	16	16	2 or 3 PCLKB	section 28.
000A 85B4h	RSCAN	RAM Test Register 26	RPGACC26	16	16	2 or 3 PCLKB	section 28.
000A 85B6h	RSCAN	Receive FIFO Access Register 1BH	RFPTR1	16	16	2 or 3 PCLKB	section 28.
000A 85B6h	RSCAN	RAM Test Register 27	RPGACC27	16	16	2 or 3 PCLKB	section 28.
000A 85B8h	RSCAN	Receive FIFO Access Register 1CL	RFDF01	16	16	2 or 3 PCLKB	section 28.
000A 85B8h	RSCAN	RAM Test Register 28	RPGACC28	16	16	2 or 3 PCLKB	section 28.
000A 85BAh	RSCAN	Receive FIFO Access Register 1CH	RFDF11	16	16	2 or 3 PCLKB	section 28.
000A 85BAh	RSCAN	RAM Test Register 29	RPGACC29	16	16	2 or 3 PCLKB	section 28.

Table 5.1 List of I/O Registers (Address Order) (30/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Reference Section
000A 85BCh	RSCAN	Receive FIFO Access Register 1DL	RFDF21	16	16	2 or 3 PCLKB	section 28.
000A 85BCh	RSCAN	RAM Test Register 30	RPGACC30	16	16	2 or 3 PCLKB	section 28.
000A 85BEh	RSCAN	Receive FIFO Access Register 1DH	RFDF31	16	16	2 or 3 PCLKB	section 28.
000A 85BEh	RSCAN	RAM Test Register 31	RPGACC31	16	16	2 or 3 PCLKB	section 28.
000A 85C0h to 000A 85DEh	RSCAN	RAM Test Register 32 to 47	RPGACC32 to 47	16	16	2 or 3 PCLKB	section 28.
000A 85E0h	RSCAN0	Transmit/Receive FIFO Access Register 0AL	CFIDL0	16	16	2 or 3 PCLKB	section 28.
000A 85E0h	RSCAN	RAM Test Register 48	RPGACC48	16	16	2 or 3 PCLKB	section 28.
000A 85E2h	RSCAN0	Transmit/Receive FIFO Access Register 0AH	CFIDH0	16	16	2 or 3 PCLKB	section 28.
000A 85E2h	RSCAN	RAM Test Register 49	RPGACC49	16	16	2 or 3 PCLKB	section 28.
000A 85E4h	RSCAN0	Transmit/Receive FIFO Access Register 0BL	CFTS0	16	16	2 or 3 PCLKB	section 28.
000A 85E4h	RSCAN	RAM Test Register 50	RPGACC50	16	16	2 or 3 PCLKB	section 28.
000A 85E6h	RSCAN0	Transmit/Receive FIFO Access Register 0BH	CFPTR0	16	16	2 or 3 PCLKB	section 28.
000A 85E6h	RSCAN	RAM Test Register 51	RPGACC51	16	16	2 or 3 PCLKB	section 28.
000A 85E8h	RSCAN0	Transmit/Receive FIFO Access Register 0CL	CFDF00	16	16	2 or 3 PCLKB	section 28.
000A 85E8h	RSCAN	RAM Test Register 52	RPGACC52	16	16	2 or 3 PCLKB	section 28.
000A 85EAh	RSCAN0	Transmit/Receive FIFO Access Register 0CH	CFDF10	16	16	2 or 3 PCLKB	section 28.
000A 85EAh	RSCAN	RAM Test Register 53	RPGACC53	16	16	2 or 3 PCLKB	section 28.
000A 85ECh	RSCAN0	Transmit/Receive FIFO Access Register 0DL	CFDF20	16	16	2 or 3 PCLKB	section 28.
000A 85ECh	RSCAN	RAM Test Register 54	RPGACC54	16	16	2 or 3 PCLKB	section 28.
000A 85EEh	RSCAN0	Transmit/Receive FIFO Access Register 0DH	CFDF30	16	16	2 or 3 PCLKB	section 28.
000A 85EEh	RSCAN	RAM Test Register 55	RPGACC55	16	16	2 or 3 PCLKB	section 28.
000A 85F0h to 000A 85FEh	RSCAN	RAM Test Register 56 to 63	RPGACC56 to 63	16	16	2 or 3 PCLKB	section 28.
000A 8600h	RSCAN0	Transmit Buffer Register 0AL	TMIDL0	16	16	2 or 3 PCLKB	section 28.
000A 8600h	RSCAN	RAM Test Register 64	RPGACC64	16	16	2 or 3 PCLKB	section 28.
000A 8602h	RSCAN0	Transmit Buffer Register 0AH	TMIDH0	16	16	2 or 3 PCLKB	section 28.
000A 8602h	RSCAN	RAM Test Register 65	RPGACC65	16	16	2 or 3 PCLKB	section 28.
000A 8604h	RSCAN	RAM Test Register 66	RPGACC66	16	16	2 or 3 PCLKB	section 28.
000A 8606h	RSCAN0	Transmit Buffer Register 0BH	TMPTR0	16	16	2 or 3 PCLKB	section 28.
000A 8606h	RSCAN	RAM Test Register 67	RPGACC67	16	16	2 or 3 PCLKB	section 28.
000A 8608h	RSCAN0	Transmit Buffer Register 0CL	TMDF00	16	16	2 or 3 PCLKB	section 28.
000A 8608h	RSCAN	RAM Test Register 68	RPGACC68	16	16	2 or 3 PCLKB	section 28.
000A 860Ah	RSCAN0	Transmit Buffer Register 0CH	TMDF10	16	16	2 or 3 PCLKB	section 28.
000A 860Ah	RSCAN	RAM Test Register 69	RPGACC69	16	16	2 or 3 PCLKB	section 28.
000A 860Ch	RSCAN0	Transmit Buffer Register 0DL	TMDF20	16	16	2 or 3 PCLKB	section 28.
000A 860Ch	RSCAN	RAM Test Register 70	RPGACC70	16	16	2 or 3 PCLKB	section 28.
000A 860Eh	RSCAN0	Transmit Buffer Register 0DH	TMDF30	16	16	2 or 3 PCLKB	section 28.
000A 860Eh	RSCAN	RAM Test Register 71	RPGACC71	16	16	2 or 3 PCLKB	section 28.
000A 8610h	RSCAN0	Transmit Buffer Register 1AL	TMIDL1	16	16	2 or 3 PCLKB	section 28.
000A 8610h	RSCAN	RAM Test Register 72	RPGACC72	16	16	2 or 3 PCLKB	section 28.
000A 8612h	RSCAN0	Transmit Buffer Register 1AH	TMIDH1	16	16	2 or 3 PCLKB	section 28.
000A 8612h	RSCAN	RAM Test Register 73	RPGACC73	16	16	2 or 3 PCLKB	section 28.
000A 8614h	RSCAN	RAM Test Register 74	RPGACC74	16	16	2 or 3 PCLKB	section 28.
000A 8616h	RSCAN0	Transmit Buffer Register 1BH	TMPTR1	16	16	2 or 3 PCLKB	section 28.
000A 8616h	RSCAN	RAM Test Register 75	RPGACC75	16	16	2 or 3 PCLKB	section 28.
000A 8618h	RSCAN0	Transmit Buffer Register 1CL	TMDF01	16	16	2 or 3 PCLKB	section 28.
000A 8618h	RSCAN	RAM Test Register 76	RPGACC76	16	16	2 or 3 PCLKB	section 28.
000A 861Ah	RSCAN0	Transmit Buffer Register 1CH	TMDF11	16	16	2 or 3 PCLKB	section 28.
000A 861Ah	RSCAN	RAM Test Register 77	RPGACC77	16	16	2 or 3 PCLKB	section 28.
000A 861Ch	RSCAN0	Transmit Buffer Register 1DL	TMDF21	16	16	2 or 3 PCLKB	section 28.

Table 5.1 List of I/O Registers (Address Order) (31/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Reference Section
000A 861Ch	RSCAN	RAM Test Register 78	RPGACC78	16	16	2 or 3 PCLKB	section 28.
000A 861Eh	RSCAN0	Transmit Buffer Register 1DH	TMDF31	16	16	2 or 3 PCLKB	section 28.
000A 861Eh	RSCAN	RAM Test Register 79	RPGACC79	16	16	2 or 3 PCLKB	section 28.
000A 8620h	RSCAN0	Transmit Buffer Register 2AL	TMIDL2	16	16	2 or 3 PCLKB	section 28.
000A 8620h	RSCAN	RAM Test Register 80	RPGACC80	16	16	2 or 3 PCLKB	section 28.
000A 8622h	RSCAN0	Transmit Buffer Register 2AH	TMIDH2	16	16	2 or 3 PCLKB	section 28.
000A 8622h	RSCAN	RAM Test Register 81	RPGACC81	16	16	2 or 3 PCLKB	section 28.
000A 8624h	RSCAN	RAM Test Register 82	RPGACC82	16	16	2 or 3 PCLKB	section 28.
000A 8626h	RSCAN0	Transmit Buffer Register 2BH	TMPTR2	16	16	2 or 3 PCLKB	section 28.
000A 8626h	RSCAN	RAM Test Register 83	RPGACC83	16	16	2 or 3 PCLKB	section 28.
000A 8628h	RSCAN0	Transmit Buffer Register 2CL	TMDF02	16	16	2 or 3 PCLKB	section 28.
000A 8628h	RSCAN	RAM Test Register 84	RPGACC84	16	16	2 or 3 PCLKB	section 28.
000A 862Ah	RSCAN0	Transmit Buffer Register 2CH	TMDF12	16	16	2 or 3 PCLKB	section 28.
000A 862Ah	RSCAN	RAM Test Register 85	RPGACC85	16	16	2 or 3 PCLKB	section 28.
000A 862Ch	RSCAN0	Transmit Buffer Register 2DL	TMDF22	16	16	2 or 3 PCLKB	section 28.
000A 862Ch	RSCAN	RAM Test Register 86	RPGACC86	16	16	2 or 3 PCLKB	section 28.
000A 862Eh	RSCAN0	Transmit Buffer Register 2DH	TMDF32	16	16	2 or 3 PCLKB	section 28.
000A 862Eh	RSCAN	RAM Test Register 87	RPGACC87	16	16	2 or 3 PCLKB	section 28.
000A 8630h	RSCAN0	Transmit Buffer Register 3AL	TMIDL3	16	16	2 or 3 PCLKB	section 28.
000A 8630h	RSCAN	RAM Test Register 88	RPGACC88	16	16	2 or 3 PCLKB	section 28.
000A 8632h	RSCAN0	Transmit Buffer Register 3AH	TMIDH3	16	16	2 or 3 PCLKB	section 28.
000A 8632h	RSCAN	RAM Test Register 89	RPGACC89	16	16	2 or 3 PCLKB	section 28.
000A 8634h	RSCAN	RAM Test Register 90	RPGACC90	16	16	2 or 3 PCLKB	section 28.
000A 8636h	RSCAN0	Transmit Buffer Register 3BH	TMPTR3	16	16	2 or 3 PCLKB	section 28.
000A 8636h	RSCAN	RAM Test Register 91	RPGACC91	16	16	2 or 3 PCLKB	section 28.
000A 8638h	RSCAN0	Transmit Buffer Register 3CL	TMDF03	16	16	2 or 3 PCLKB	section 28.
000A 8638h	RSCAN	RAM Test Register 92	RPGACC92	16	16	2 or 3 PCLKB	section 28.
000A 863Ah	RSCAN0	Transmit Buffer Register 3CH	TMDF13	16	16	2 or 3 PCLKB	section 28.
000A 863Ah	RSCAN	RAM Test Register 93	RPGACC93	16	16	2 or 3 PCLKB	section 28.
000A 863Ch	RSCAN0	Transmit Buffer Register 3DL	TMDF23	16	16	2 or 3 PCLKB	section 28.
000A 863Ch	RSCAN	RAM Test Register 94	RPGACC94	16	16	2 or 3 PCLKB	section 28.
000A 863Eh	RSCAN0	Transmit Buffer Register 3DH	TMDF33	16	16	2 or 3 PCLKB	section 28.
000A 863Eh	RSCAN	RAM Test Register 95	RPGACC95	16	16	2 or 3 PCLKB	section 28.
000A 8640h to 000A 867Eh	RSCAN	RAM Test Register 96 to 127	RPGACC96 to 127	16	16	2 or 3 PCLKB	section 28.
000A 8680h	RSCAN0	Transmit History Buffer Access Register	THLACC0	16	16	2 or 3 PCLKB	section 28.
000C 1200h	MTU3	Timer Control Register	TCR	8	8, 16, 32	4 or 5 PCLKA	section 20.
000C 1201h	MTU4	Timer Control Register	TCR	8	8	4 or 5 PCLKA	section 20.
000C 1202h	MTU3	Timer Mode Register 1	TMDR1	8	8, 16	4 or 5 PCLKA	section 20.
000C 1203h	MTU4	Timer Mode Register 1	TMDR1	8	8	4 or 5 PCLKA	section 20.
000C 1204h	MTU3	Timer I/O Control Register H	TIORH	8	8, 16, 32	4 or 5 PCLKA	section 20.
000C 1205h	MTU3	Timer I/O Control Register L	TIORL	8	8	4 or 5 PCLKA	section 20.
000C 1206h	MTU4	Timer I/O Control Register H	TIORH	8	8, 16	4 or 5 PCLKA	section 20.
000C 1207h	MTU4	Timer I/O Control Register L	TIORL	8	8	4 or 5 PCLKA	section 20.
000C 1208h	MTU3	Timer Interrupt Enable Register	TIER	8	8, 16	4 or 5 PCLKA	section 20.
000C 1209h	MTU4	Timer Interrupt Enable Register	TIER	8	8	4 or 5 PCLKA	section 20.
000C 120Ah	MTU	Timer Output Master Enable Register A	TOERA	8	8	4 or 5 PCLKA	section 20.
000C 120Dh	MTU	Timer Gate Control Register	TGCRA	8	8	4 or 5 PCLKA	section 20.
000C 120Eh	MTU	Timer Output Control Register 1A	TOCR1A	8	8, 16	4 or 5 PCLKA	section 20.
000C 120Fh	MTU	Timer Output Control Register 2A	TOCR2A	8	8	4 or 5 PCLKA	section 20.
000C 1210h	MTU3	Timer Counter	TCNT	16	16, 32	4 or 5 PCLKA	section 20.

Table 5.1 List of I/O Registers (Address Order) (32/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Reference Section
000C 1212h	MTU4	Timer Counter	TCNT	16	16	4 or 5 PCLKA	section 20.
000C 1214h	MTU	Timer Period Data Register A	TCDRA	16	16, 32	4 or 5 PCLKA	section 20.
000C 1216h	MTU	Timer Dead Time Data Register A	TDDRA	16	16	4 or 5 PCLKA	section 20.
000C 1218h	MTU3	Timer General Register A	TGRA	16	16, 32	4 or 5 PCLKA	section 20.
000C 121Ah	MTU3	Timer General Register B	TGRB	16	16	4 or 5 PCLKA	section 20.
000C 121Ch	MTU4	Timer General Register A	TGRA	16	16, 32	4 or 5 PCLKA	section 20.
000C 121Eh	MTU4	Timer General Register B	TGRB	16	16	4 or 5 PCLKA	section 20.
000C 1220h	MTU	Timer Subcounters A	TCNTSA	16	16, 32	4 or 5 PCLKA	section 20.
000C 1222h	MTU	Timer Period Buffer Register A	TCBRA	16	16	4 or 5 PCLKA	section 20.
000C 1224h	MTU3	Timer General Register C	TGRC	16	16, 32	4 or 5 PCLKA	section 20.
000C 1226h	MTU3	Timer General Register D	TGRD	16	16	4 or 5 PCLKA	section 20.
000C 1228h	MTU4	Timer General Register C	TGRC	16	16, 32	4 or 5 PCLKA	section 20.
000C 122Ah	MTU4	Timer General Register D	TGRD	16	16	4 or 5 PCLKA	section 20.
000C 122Ch	MTU3	Timer Status Register	TSR	8	8, 16	4 or 5 PCLKA	section 20.
000C 122Dh	MTU4	Timer Status Register	TSR	8	8	4 or 5 PCLKA	section 20.
000C 1230h	MTU	Timer Interrupt Skipping Set Register 1A	TITCR1A	8	8, 16	4 or 5 PCLKA	section 20.
000C 1231h	MTU	Timer Interrupt Skipping Counters 1A	TITCNT1A	8	8	4 or 5 PCLKA	section 20.
000C 1232h	MTU	Timer Buffer Transfer Set Register A	TBTERA	8	8	4 or 5 PCLKA	section 20.
000C 1234h	MTU	Timer Dead Time Enable Register A	TDERA	8	8	4 or 5 PCLKA	section 20.
000C 1236h	MTU	Timer Output Level Buffer Register A	TOLBRA	8	8	4 or 5 PCLKA	section 20.
000C 1238h	MTU3	Timer Buffer Operation Transfer Mode Register	TBTM	8	8, 16	4 or 5 PCLKA	section 20.
000C 1239h	MTU4	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	4 or 5 PCLKA	section 20.
000C 123Ah	MTU	Timer Interrupt Skipping Mode Register A	TITMRA	8	8	4 or 5 PCLKA	section 20.
000C 123Bh	MTU	Timer Interrupt Skipping Set Register 2A	TITCR2A	8	8	4 or 5 PCLKA	section 20.
000C 123Ch	MTU	Timer Interrupt Skipping Counters 2A	TITCNT2A	8	8	4 or 5 PCLKA	section 20.
000C 1240h	MTU4	Timer A/D Converter Start Request Control Register	TADCR	16	16	4 or 5 PCLKA	section 20.
000C 1244h	MTU4	Timer A/D Converter Start Request Cycle Set Register A	TADCORA	16	16, 32	4 or 5 PCLKA	section 20.
000C 1246h	MTU4	Timer A/D Converter Start Request Cycle Set Register B	TADCORB	16	16	4 or 5 PCLKA	section 20.
000C 1248h	MTU4	Timer A/D Converter Start Request Cycle Set Buffer Register A	TADCOBRA	16	16, 32	4 or 5 PCLKA	section 20.
000C 124Ah	MTU4	Timer A/D Converter Start Request Cycle Set Buffer Register B	TADCOBRB	16	16	4 or 5 PCLKA	section 20.
000C 124Ch	MTU3	Timer Control Register 2	TCR2	8	8	4 or 5 PCLKA	section 20.
000C 124Dh	MTU4	Timer Control Register 2	TCR2	8	8	4 or 5 PCLKA	section 20.
000C 1260h	MTU	Timer Waveform Control Register A	TWCRA	8	8	4 or 5 PCLKA	section 20.
000C 1270h	MTU	Timer Mode Register 2A	TMDR2A	8	8	4 or 5 PCLKA	section 20.
000C 1272h	MTU3	Timer General Register E	TGRE	16	16	4 or 5 PCLKA	section 20.
000C 1274h	MTU4	Timer General Register E	TGRE	16	16	4 or 5 PCLKA	section 20.
000C 1276h	MTU4	Timer General Register F	TGRF	16	16	4 or 5 PCLKA	section 20.
000C 1280h	MTU	Timer Start Register A	TSTRA	8	8, 16	4 or 5 PCLKA	section 20.
000C 1281h	MTU	Timer Synchronous Register A	TSYRA	8	8	4 or 5 PCLKA	section 20.
000C 1282h	MTU	Timer Counter Synchronous Start Register	TCSYSTR	8	8	4 or 5 PCLKA	section 20.
000C 1284h	MTU	Timer Read/Write Enable Register A	TRWERA	8	8	4 or 5 PCLKA	section 20.
000C 1290h	MTU0	Noise Filter Control Register 0	NFCR0	8	8	4 or 5 PCLKA	section 20.
000C 1291h	MTU1	Noise Filter Control Register 1	NFCR1	8	8	4 or 5 PCLKA	section 20.
000C 1292h	MTU2	Noise Filter Control Register 2	NFCR2	8	8	4 or 5 PCLKA	section 20.
000C 1293h	MTU3	Noise Filter Control Register 3	NFCR3	8	8	4 or 5 PCLKA	section 20.
000C 1294h	MTU4	Noise Filter Control Register 4	NFCR4	8	8	4 or 5 PCLKA	section 20.
000C 1296h	MTU9	Noise Filter Control Register 9	NFCR9	8	8	4 or 5 PCLKA	section 20.
000C 1299h	MTU0	Noise Filter Control Register C	NFCRC	8	8	4 or 5 PCLKA	section 20.
000C 1300h	MTU0	Timer Control Register	TCR	8	8, 16, 32	4 or 5 PCLKA	section 20.
000C 1301h	MTU0	Timer Mode Register 1	TMDR1	8	8	4 or 5 PCLKA	section 20.

Table 5.1 List of I/O Registers (Address Order) (33/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Reference Section
000C 1302h	MTU0	Timer I/O Control Register H	TIORH	8	8, 16	4 or 5 PCLKA	section 20.
000C 1303h	MTU0	Timer I/O Control Register L	TIORL	8	8	4 or 5 PCLKA	section 20.
000C 1304h	MTU0	Timer Interrupt Enable Register	TIER	8	8, 16, 32	4 or 5 PCLKA	section 20.
000C 1306h	MTU0	Timer Counter	TCNT	16	16	4 or 5 PCLKA	section 20.
000C 1308h	MTU0	Timer General Register A	TGRA	16	16, 32	4 or 5 PCLKA	section 20.
000C 130Ah	MTU0	Timer General Register B	TGRB	16	16	4 or 5 PCLKA	section 20.
000C 130Ch	MTU0	Timer General Register C	TGRC	16	16, 32	4 or 5 PCLKA	section 20.
000C 130Eh	MTU0	Timer General Register D	TGRD	16	16	4 or 5 PCLKA	section 20.
000C 1320h	MTU0	Timer General Register E	TGRE	16	16, 32	4 or 5 PCLKA	section 20.
000C 1322h	MTU0	Timer General Register F	TGRF	16	16	4 or 5 PCLKA	section 20.
000C 1324h	MTU0	Timer Interrupt Enable Register 2	TIER2	8	8, 16	4 or 5 PCLKA	section 20.
000C 1326h	MTU0	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	4 or 5 PCLKA	section 20.
000C 1328h	MTU0	Timer Control Register 2	TCR2	8	8	4 or 5 PCLKA	section 20.
000C 1380h	MTU1	Timer Control Register	TCR	8	8, 16	4 or 5 PCLKA	section 20.
000C 1381h	MTU1	Timer Mode Register 1	TMDR1	8	8	4 or 5 PCLKA	section 20.
000C 1382h	MTU1	Timer I/O Control Register	TIOR	8	8	4 or 5 PCLKA	section 20.
000C 1384h	MTU1	Timer Interrupt Enable Register	TIER	8	8, 16, 32	4 or 5 PCLKA	section 20.
000C 1385h	MTU1	Timer Status Register	TSR	8	8	4 or 5 PCLKA	section 20.
000C 1386h	MTU1	Timer Counter	TCNT	16	16	4 or 5 PCLKA	section 20.
000C 1388h	MTU1	Timer General Register A	TGRA	16	16, 32	4 or 5 PCLKA	section 20.
000C 138Ah	MTU1	Timer General Register B	TGRB	16	16	4 or 5 PCLKA	section 20.
000C 1390h	MTU1	Timer Input Capture Control Register	TICCR	8	8	4 or 5 PCLKA	section 20.
000C 1391h	MTU1	Timer Mode Register 3	TMDR3	8	8	4 or 5 PCLKA	section 20.
000C 1394h	MTU1	Timer Control Register 2	TCR2	8	8	4 or 5 PCLKA	section 20.
000C 13A0h	MTU1	Timer Longword Counter	TCNTLW	32	32	4 or 5 PCLKA	section 20.
000C 13A4h	MTU1	Timer Longword General Register	TGRALW	32	32	4 or 5 PCLKA	section 20.
000C 13A8h	MTU1	Timer Longword General Register	TGRBLW	32	32	4 or 5 PCLKA	section 20.
000C 1400h	MTU2	Timer Control Register	TCR	8	8, 16	4 or 5 PCLKA	section 20.
000C 1401h	MTU2	Timer Mode Register 1	TMDR1	8	8	4 or 5 PCLKA	section 20.
000C 1402h	MTU2	Timer I/O Control Register	TIOR	8	8	4 or 5 PCLKA	section 20.
000C 1404h	MTU2	Timer Interrupt Enable Register	TIER	8	8, 16, 32	4 or 5 PCLKA	section 20.
000C 1405h	MTU2	Timer Status Register	TSR	8	8	4 or 5 PCLKA	section 20.
000C 1406h	MTU2	Timer Counter	TCNT	16	16	4 or 5 PCLKA	section 20.
000C 1408h	MTU2	Timer General Register A	TGRA	16	16, 32	4 or 5 PCLKA	section 20.
000C 140Ah	MTU2	Timer General Register B	TGRB	16	16	4 or 5 PCLKA	section 20.
000C 140Ch	MTU2	Timer Control Register 2	TCR2	8	8	4 or 5 PCLKA	section 20.
000C 1580h	MTU9	Timer Control Register	TCR	8	8, 16, 32	4 or 5 PCLKA	section 20.
000C 1581h	MTU9	Timer Mode Register 1	TMDR1	8	8	4 or 5 PCLKA	section 20.
000C 1582h	MTU9	Timer I/O Control Register H	TIORH	8	8, 16	4 or 5 PCLKA	section 20.
000C 1583h	MTU9	Timer I/O Control Register L	TIORL	8	8	4 or 5 PCLKA	section 20.
000C 1584h	MTU9	Timer Interrupt Enable Register	TIER	8	8, 16, 32	4 or 5 PCLKA	section 20.
000C 1586h	MTU9	Timer Counter	TCNT	16	16	4 or 5 PCLKA	section 20.
000C 1588h	MTU9	Timer General Register A	TGRA	16	16, 32	4 or 5 PCLKA	section 20.
000C 158Ah	MTU9	Timer General Register B	TGRB	16	16	4 or 5 PCLKA	section 20.
000C 158Ch	MTU9	Timer General Register C	TGRC	16	16, 32	4 or 5 PCLKA	section 20.
000C 158Eh	MTU9	Timer General Register D	TGRD	16	16	4 or 5 PCLKA	section 20.
000C 15A0h	MTU9	Timer General Register E	TGRE	16	16, 32	4 or 5 PCLKA	section 20.
000C 15A2h	MTU9	Timer General Register F	TGRF	16	16	4 or 5 PCLKA	section 20.
000C 15A4h	MTU9	Timer Interrupt Enable Register 2	TIER2	8	8, 16	4 or 5 PCLKA	section 20.
000C 15A6h	MTU9	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	4 or 5 PCLKA	section 20.
000C 15A8h	MTU9	Timer Control Register 2	TCR2	8	8	4 or 5 PCLKA	section 20.

Table 5.1 List of I/O Registers (Address Order) (34/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Reference Section
000C 1A00h	MTU6	Timer Control Register	TCR	8	8, 16, 32	4 or 5 PCLKA	section 20.
000C 1A01h	MTU7	Timer Control Register	TCR	8	8	4 or 5 PCLKA	section 20.
000C 1A02h	MTU6	Timer Mode Register 1	TMDR1	8	8, 16	4 or 5 PCLKA	section 20.
000C 1A03h	MTU7	Timer Mode Register 1	TMDR1	8	8	4 or 5 PCLKA	section 20.
000C 1A04h	MTU6	Timer I/O Control Register H	TIORH	8	8, 16, 32	4 or 5 PCLKA	section 20.
000C 1A05h	MTU6	Timer I/O Control Register L	TIORL	8	8	4 or 5 PCLKA	section 20.
000C 1A06h	MTU7	Timer I/O Control Register H	TIORH	8	8, 16	4 or 5 PCLKA	section 20.
000C 1A07h	MTU7	Timer I/O Control Register L	TIORL	8	8	4 or 5 PCLKA	section 20.
000C 1A08h	MTU6	Timer Interrupt Enable Register	TIER	8	8, 16	4 or 5 PCLKA	section 20.
000C 1A09h	MTU7	Timer Interrupt Enable Register	TIER	8	8	4 or 5 PCLKA	section 20.
000C 1A0Ah	MTU	Timer Output Master Enable Register B	TOERB	8	8	4 or 5 PCLKA	section 20.
000C 1A0Dh	MTU	Timer Gate Control Register	TGCRB	8	8	4 or 5 PCLKA	section 20.
000C 1A0Eh	MTU	Timer Output Control Register 1B	TOCR1B	8	8, 16	4 or 5 PCLKA	section 20.
000C 1A0Fh	MTU	Timer Output Control Register 2B	TOCR2B	8	8	4 or 5 PCLKA	section 20.
000C 1A10h	MTU6	Timer Counter	TCNT	16	16, 32	4 or 5 PCLKA	section 20.
000C 1A12h	MTU7	Timer Counter	TCNT	16	16	4 or 5 PCLKA	section 20.
000C 1A14h	MTU	Timer Period Data Register B	TCDRB	16	16, 32	4 or 5 PCLKA	section 20.
000C 1A16h	MTU	Timer Dead Time Data Register B	TDDRB	16	16	4 or 5 PCLKA	section 20.
000C 1A18h	MTU6	Timer General Register A	TGRA	16	16, 32	4 or 5 PCLKA	section 20.
000C 1A1Ah	MTU6	Timer General Register B	TGRB	16	16	4 or 5 PCLKA	section 20.
000C 1A1Ch	MTU7	Timer General Register A	TGRA	16	16, 32	4 or 5 PCLKA	section 20.
000C 1A1Eh	MTU7	Timer General Register B	TGRB	16	16	4 or 5 PCLKA	section 20.
000C 1A20h	MTU	Timer Subcounters B	TCNTSB	16	16, 32	4 or 5 PCLKA	section 20.
000C 1A22h	MTU	Timer Period Buffer Register B	TCBRB	16	16	4 or 5 PCLKA	section 20.
000C 1A24h	MTU6	Timer General Register C	TGRC	16	16, 32	4 or 5 PCLKA	section 20.
000C 1A26h	MTU6	Timer General Register D	TGRD	16	16	4 or 5 PCLKA	section 20.
000C 1A28h	MTU7	Timer General Register C	TGRC	16	16, 32	4 or 5 PCLKA	section 20.
000C 1A2Ah	MTU7	Timer General Register D	TGRD	16	16	4 or 5 PCLKA	section 20.
000C 1A2Ch	MTU6	Timer Status Register	TSR	8	8, 16	4 or 5 PCLKA	section 20.
000C 1A2Dh	MTU7	Timer Status Register	TSR	8	8	4 or 5 PCLKA	section 20.
000C 1A30h	MTU	Timer Interrupt Skipping Set Register 1B	TITCR1B	8	8, 16	4 or 5 PCLKA	section 20.
000C 1A31h	MTU	Timer Interrupt Skipping Counters 1B	TITCNT1B	8	8	4 or 5 PCLKA	section 20.
000C 1A32h	MTU	Timer Buffer Transfer Set Register B	TBTERB	8	8	4 or 5 PCLKA	section 20.
000C 1A34h	MTU	Timer Dead Time Enable Register B	TDERB	8	8	4 or 5 PCLKA	section 20.
000C 1A36h	MTU	Timer Output Level Buffer Register B	TOLBRB	8	8	4 or 5 PCLKA	section 20.
000C 1A38h	MTU6	Timer Buffer Operation Transfer Mode Register	TBTM	8	8, 16	4 or 5 PCLKA	section 20.
000C 1A39h	MTU7	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	4 or 5 PCLKA	section 20.
000C 1A3Ah	MTU	Timer Interrupt Skipping Mode Register B	TITMRB	8	8	4 or 5 PCLKA	section 20.
000C 1A3Bh	MTU	Timer Interrupt Skipping Set Register 2B	TITCR2B	8	8	4 or 5 PCLKA	section 20.
000C 1A3Ch	MTU	Timer Interrupt Skipping Counters 2B	TITCNT2B	8	8	4 or 5 PCLKA	section 20.
000C 1A40h	MTU7	Timer A/D Converter Start Request Control Register	TADCR	16	16	4 or 5 PCLKA	section 20.
000C 1A44h	MTU7	Timer A/D Converter Start Request Cycle Set Register A	TADCORA	16	16, 32	4 or 5 PCLKA	section 20.
000C 1A46h	MTU7	Timer A/D Converter Start Request Cycle Set Register B	TADCORB	16	16	4 or 5 PCLKA	section 20.
000C 1A48h	MTU7	Timer A/D Converter Start Request Cycle Set Buffer Register A	TADCOBRA	16	16, 32	4 or 5 PCLKA	section 20.
000C 1A4Ah	MTU7	Timer A/D Converter Start Request Cycle Set Buffer Register B	TADCOBRB	16	16	4 or 5 PCLKA	section 20.
000C 1A4Ch	MTU6	Timer Control Register 2	TCR2	8	8	4 or 5 PCLKA	section 20.
000C 1A4Dh	MTU7	Timer Control Register 2	TCR2	8	8	4 or 5 PCLKA	section 20.
000C 1A50h	MTU6	Timer Synchronous Clear Register	TSYCR	8	8	4 or 5 PCLKA	section 20.
000C 1A60h	MTU	Timer Waveform Control Register B	TWCRB	8	8	4 or 5 PCLKA	section 20.
000C 1A70h	MTU	Timer Mode Register 2B	TMDR2B	8	8	4 or 5 PCLKA	section 20.

Table 5.1 List of I/O Registers (Address Order) (35/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Reference Section
000C 1A72h	MTU6	Timer General Register E	TGRE	16	16	4 or 5 PCLKA	section 20.
000C 1A74h	MTU7	Timer General Register E	TGRE	16	16	4 or 5 PCLKA	section 20.
000C 1A76h	MTU7	Timer General Register F	TGRF	16	16	4 or 5 PCLKA	section 20.
000C 1A80h	MTU	Timer Start Register B	TSTRB	8	8, 16	4 or 5 PCLKA	section 20.
000C 1A81h	MTU	Timer Synchronous Register B	TSYRB	8	8	4 or 5 PCLKA	section 20.
000C 1A84h	MTU	Timer Read/Write Enable Register B	TRWERB	8	8	4 or 5 PCLKA	section 20.
000C 1A93h	MTU6	Noise Filter Control Register 6	NFCR6	8	8	4 or 5 PCLKA	section 20.
000C 1A94h	MTU7	Noise Filter Control Register 7	NFCR7	8	8	4 or 5 PCLKA	section 20.
000C 1A95h	MTU5	Noise Filter Control Register 5	NFCR5	8	8	4 or 5 PCLKA	section 20.
000C 1C80h	MTU5	Timer Counter U	TCNTU	16	16, 32	4 or 5 PCLKA	section 20.
000C 1C82h	MTU5	Timer General Register U	TGRU	16	16	4 or 5 PCLKA	section 20.
000C 1C84h	MTU5	Timer Control Register U	TCRU	8	8	4 or 5 PCLKA	section 20.
000C 1C85h	MTU5	Timer Control Register 2U	TCR2U	8	8	4 or 5 PCLKA	section 20.
000C 1C86h	MTU5	Timer I/O Control Register U	TIORU	8	8	4 or 5 PCLKA	section 20.
000C 1C90h	MTU5	Timer Counter V	TCNTV	16	16, 32	4 or 5 PCLKA	section 20.
000C 1C92h	MTU5	Timer General Register V	TGRV	16	16	4 or 5 PCLKA	section 20.
000C 1C94h	MTU5	Timer Control Register V	TCRV	8	8	4 or 5 PCLKA	section 20.
000C 1C95h	MTU5	Timer Control Register 2V	TCR2V	8	8	4 or 5 PCLKA	section 20.
000C 1C96h	MTU5	Timer I/O Control Register V	TIORV	8	8	4 or 5 PCLKA	section 20.
000C 1CA0h	MTU5	Timer Counter W	TCNTW	16	16, 32	4 or 5 PCLKA	section 20.
000C 1CA2h	MTU5	Timer General Register W	TGRW	16	16	4 or 5 PCLKA	section 20.
000C 1CA4h	MTU5	Timer Control Register W	TCRW	8	8	4 or 5 PCLKA	section 20.
000C 1CA5h	MTU5	Timer Control Register 2W	TCR2W	8	8	4 or 5 PCLKA	section 20.
000C 1CA6h	MTU5	Timer I/O Control Register W	TIORW	8	8	4 or 5 PCLKA	section 20.
000C 1CB2h	MTU5	Timer Interrupt Enable Register	TIER	8	8	4 or 5 PCLKA	section 20.
000C 1CB4h	MTU5	Timer Start Register	TSTR	8	8	4 or 5 PCLKA	section 20.
000C 1CB6h	MTU5	Timer Compare Match Clear Register	TCNTCMPCLR	8	8	4 or 5 PCLKA	section 20.
000C 1D30h	MTU	A/D Conversion Start Request Select Register 0	TADSTRGR0	8	8	4 or 5 PCLKA	section 20.
000C 1D32h	MTU	A/D Conversion Start Request Select Register 1	TADSTRGR1	8	8	4 or 5 PCLKA	section 20.
000C 2000h	GPT	General PWM Timer Software Start Register	GTSTR	16	8, 16, 32	4 or 5 PCLKA	section 22.
000C 2002h	GPT	Noise Filter Control Register	NFCR	16	16, 32	4 or 5 PCLKA	section 22.
000C 2004h	GPT	General PWM Timer Hardware Source Start/Stop Control Register 0	GTHSCR	16	8, 16, 32	4 or 5 PCLKA	section 22.
000C 2006h	GPT	General PWM Timer Hardware Source Clear Control Register	GTHCCR	16	8, 16, 32	4 or 5 PCLKA	section 22.
000C 2008h	GPT	General PWM Timer Hardware Start Source Select Register	GTHSSR	16	8, 16, 32	4 or 5 PCLKA	section 22.
000C 200Ah	GPT	General PWM Timer Hardware Stop/Clear Source Select Register	GTHPSR	16	8, 16, 32	4 or 5 PCLKA	section 22.
000C 200Ch	GPT	General PWM Timer Write-Protection Register	GTWP	16	8, 16, 32	4 or 5 PCLKA	section 22.
000C 200Eh	GPT	General PWM Timer Sync Register	GTSYNC	16	8, 16, 32	4 or 5 PCLKA	section 22.
000C 2010h	GPT	General PWM Timer External Trigger Input Interrupt Register	GTETINT	16	8, 16, 32	4 or 5 PCLKA	section 22.
000C 2014h	GPT	General PWM Timer Buffer Operation Disable Register	GTBDR	16	8, 16, 32	4 or 5 PCLKA	section 22.
000C 2018h	GPT	General PWM Timer Start Write-Protection Register	GTSWP	16	8, 16, 32	4 or 5 PCLKA	section 22.
000C 201Ch	GPT	General PWM Timer Clearing Write-Protection Register	GTCWP	16	8, 16, 32	4 or 5 PCLKA	section 22.
000C 2020h	GPT	General PWM Timer Common Register Write-Protection Register	GTCMNWP	16	8, 16, 32	4 or 5 PCLKA	section 22.
000C 2024h	GPT	General PWM Timer Mode Register	GTMDR	16	8, 16, 32	4 or 5 PCLKA	section 22.
000C 2028h	GPT	General PWM Timer External Clock Noise Filter Control Register	GTECNFCR	32	8, 16, 32	4 or 5 PCLKA	section 22.
000C 202Ch	GPT	General PWM Timer A/D Conversion Start Request Signal Monitor Register	GTADSMR	32	8, 16, 32	4 or 5 PCLKA	section 22.
000C 2100h	GPT0	General PWM Timer I/O Control Register	GTIOR	16	8, 16, 32	4 or 5 PCLKA	section 22.
000C 2102h	GPT0	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	8, 16, 32	4 or 5 PCLKA	section 22.

Table 5.1 List of I/O Registers (Address Order) (36/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Reference Section
000C 2104h	GPT0	General PWM Timer Control Register	GTCR	16	8, 16, 32	4 or 5 PCLKA	section 22.
000C 2106h	GPT0	General PWM Timer Buffer Enable Register	GTBER	16	8, 16, 32	4 or 5 PCLKA	section 22.
000C 2108h	GPT0	General PWM Timer Count Direction Register	GTUDC	16	8, 16, 32	4 or 5 PCLKA	section 22.
000C 210Ah	GPT0	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	GTITC	16	8, 16, 32	4 or 5 PCLKA	section 22.
000C 210Ch	GPT0	General PWM Timer Status Register	GTST	16	8, 16, 32	4 or 5 PCLKA	section 22.
000C 210Eh	GPT0	General PWM Timer Counter	GTCNT	16	16	4 or 5 PCLKA	section 22.
000C 2110h	GPT0	General PWM Timer Compare Capture Register A	GTCCRA	16	16, 32	4 or 5 PCLKA	section 22.
000C 2112h	GPT0	General PWM Timer Compare Capture Register B	GTCCRB	16	16, 32	4 or 5 PCLKA	section 22.
000C 2114h	GPT0	General PWM Timer Compare Capture Register C	GTCCRC	16	16, 32	4 or 5 PCLKA	section 22.
000C 2116h	GPT0	General PWM Timer Compare Capture Register D	GTCCRD	16	16, 32	4 or 5 PCLKA	section 22.
000C 2118h	GPT0	General PWM Timer Compare Capture Register E	GTCCRE	16	16, 32	4 or 5 PCLKA	section 22.
000C 211Ah	GPT0	General PWM Timer Compare Capture Register F	GTCCRF	16	16, 32	4 or 5 PCLKA	section 22.
000C 211Ch	GPT0	General PWM Timer Period Setting Register	GTPR	16	16, 32	4 or 5 PCLKA	section 22.
000C 211Eh	GPT0	General PWM Timer Period Setting Buffer Register	GTPBR	16	16, 32	4 or 5 PCLKA	section 22.
000C 2120h	GPT0	General PWM Timer Period Setting Double Buffer Register	GTPDBR	16	16, 32	4 or 5 PCLKA	section 22.
000C 2124h	GPT0	A/D Converter Start Request Timing Register A	GTADTRA	16	16, 32	4 or 5 PCLKA	section 22.
000C 2126h	GPT0	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16, 32	4 or 5 PCLKA	section 22.
000C 2128h	GPT0	A/D Converter Start Request Timing Double Buffer Register A	GTADTDBRA	16	16, 32	4 or 5 PCLKA	section 22.
000C 212Ch	GPT0	A/D Converter Start Request Timing Register B	GTADTRB	16	16, 32	4 or 5 PCLKA	section 22.
000C 212Eh	GPT0	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16, 32	4 or 5 PCLKA	section 22.
000C 2130h	GPT0	A/D Converter Start Request Timing Double Buffer Register B	GTADTDBRB	16	16, 32	4 or 5 PCLKA	section 22.
000C 2134h	GPT0	General PWM Timer Output Negate Control Register	GTONCR	16	16, 32	4 or 5 PCLKA	section 22.
000C 2136h	GPT0	General PWM Timer Dead Time Control Register	GTDTCR	16	16, 32	4 or 5 PCLKA	section 22.
000C 2138h	GPT0	General PWM Timer Dead Time Value Register U	GTDVU	16	16, 32	4 or 5 PCLKA	section 22.
000C 213Ah	GPT0	General PWM Timer Dead Time Value Register D	GTDVD	16	16, 32	4 or 5 PCLKA	section 22.
000C 213Ch	GPT0	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16, 32	4 or 5 PCLKA	section 22.
000C 213Eh	GPT0	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16, 32	4 or 5 PCLKA	section 22.
000C 2140h	GPT0	General PWM Timer Output Protection Function Status Register	GTSOS	16	16, 32	4 or 5 PCLKA	section 22.
000C 2142h	GPT0	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16, 32	4 or 5 PCLKA	section 22.
000C 2180h	GPT1	General PWM Timer I/O Control Register	GTIOR	16	8, 16, 32	4 or 5 PCLKA	section 22.
000C 2182h	GPT1	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	8, 16, 32	4 or 5 PCLKA	section 22.
000C 2184h	GPT1	General PWM Timer Control Register	GTCR	16	8, 16, 32	4 or 5 PCLKA	section 22.
000C 2186h	GPT1	General PWM Timer Buffer Enable Register	GTBER	16	8, 16, 32	4 or 5 PCLKA	section 22.
000C 2188h	GPT1	General PWM Timer Count Direction Register	GTUDC	16	8, 16, 32	4 or 5 PCLKA	section 22.
000C 218Ah	GPT1	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	GTITC	16	8, 16, 32	4 or 5 PCLKA	section 22.
000C 218Ch	GPT1	General PWM Timer Status Register	GTST	16	8, 16, 32	4 or 5 PCLKA	section 22.
000C 218Eh	GPT1	General PWM Timer Counter	GTCNT	16	16	4 or 5 PCLKA	section 22.
000C 2190h	GPT1	General PWM Timer Compare Capture Register A	GTCCRA	16	16, 32	4 or 5 PCLKA	section 22.
000C 2192h	GPT1	General PWM Timer Compare Capture Register B	GTCCRB	16	16, 32	4 or 5 PCLKA	section 22.
000C 2194h	GPT1	General PWM Timer Compare Capture Register C	GTCCRC	16	16, 32	4 or 5 PCLKA	section 22.
000C 2196h	GPT1	General PWM Timer Compare Capture Register D	GTCCRD	16	16, 32	4 or 5 PCLKA	section 22.
000C 2198h	GPT1	General PWM Timer Compare Capture Register E	GTCCRE	16	16, 32	4 or 5 PCLKA	section 22.
000C 219Ah	GPT1	General PWM Timer Compare Capture Register F	GTCCRF	16	16, 32	4 or 5 PCLKA	section 22.
000C 219Ch	GPT1	General PWM Timer Period Setting Register	GTPR	16	16, 32	4 or 5 PCLKA	section 22.
000C 219Eh	GPT1	General PWM Timer Period Setting Buffer Register	GTPBR	16	16, 32	4 or 5 PCLKA	section 22.
000C 21A0h	GPT1	General PWM Timer Period Setting Double Buffer Register	GTPDBR	16	16, 32	4 or 5 PCLKA	section 22.
000C 21A4h	GPT1	A/D Converter Start Request Timing Register A	GTADTRA	16	16, 32	4 or 5 PCLKA	section 22.
000C 21A6h	GPT1	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16, 32	4 or 5 PCLKA	section 22.

Table 5.1 List of I/O Registers (Address Order) (37/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Reference Section
000C 21A8h	GPT1	A/D Converter Start Request Timing Double Buffer Register A	GTADTDBRA	16	16, 32	4 or 5 PCLKA	section 22.
000C 21ACh	GPT1	A/D Converter Start Request Timing Register B	GTADTRB	16	16, 32	4 or 5 PCLKA	section 22.
000C 21AEh	GPT1	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16, 32	4 or 5 PCLKA	section 22.
000C 21B0h	GPT1	A/D Converter Start Request Timing Double Buffer Register B	GTADTDBRB	16	16, 32	4 or 5 PCLKA	section 22.
000C 21B4h	GPT1	General PWM Timer Output Negate Control Register	GTONCR	16	16, 32	4 or 5 PCLKA	section 22.
000C 21B6h	GPT1	General PWM Timer Dead Time Control Register	GTDTCR	16	16, 32	4 or 5 PCLKA	section 22.
000C 21B8h	GPT1	General PWM Timer Dead Time Value Register U	GTDVU	16	16, 32	4 or 5 PCLKA	section 22.
000C 21BAh	GPT1	General PWM Timer Dead Time Value Register D	GTDVD	16	16, 32	4 or 5 PCLKA	section 22.
000C 21BCh	GPT1	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16, 32	4 or 5 PCLKA	section 22.
000C 21BEh	GPT1	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16, 32	4 or 5 PCLKA	section 22.
000C 21C0h	GPT1	General PWM Timer Output Protection Function Status Register	GTSOS	16	16, 32	4 or 5 PCLKA	section 22.
000C 21C2h	GPT1	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16, 32	4 or 5 PCLKA	section 22.
000C 2200h	GPT2	General PWM Timer I/O Control Register	GTIOR	16	8, 16, 32	4 or 5 PCLKA	section 22.
000C 2202h	GPT2	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	8, 16, 32	4 or 5 PCLKA	section 22.
000C 2204h	GPT2	General PWM Timer Control Register	GTCR	16	8, 16, 32	4 or 5 PCLKA	section 22.
000C 2206h	GPT2	General PWM Timer Buffer Enable Register	GTBER	16	8, 16, 32	4 or 5 PCLKA	section 22.
000C 2208h	GPT2	General PWM Timer Count Direction Register	GTUDC	16	8, 16, 32	4 or 5 PCLKA	section 22.
000C 220Ah	GPT2	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	GTITC	16	8, 16, 32	4 or 5 PCLKA	section 22.
000C 220Ch	GPT2	General PWM Timer Status Register	GTST	16	8, 16, 32	4 or 5 PCLKA	section 22.
000C 220Eh	GPT2	General PWM Timer Counter	GTCNT	16	16	4 or 5 PCLKA	section 22.
000C 2210h	GPT2	General PWM Timer Compare Capture Register A	GTCCRA	16	16, 32	4 or 5 PCLKA	section 22.
000C 2212h	GPT2	General PWM Timer Compare Capture Register B	GTCCRB	16	16, 32	4 or 5 PCLKA	section 22.
000C 2214h	GPT2	General PWM Timer Compare Capture Register C	GTCCRC	16	16, 32	4 or 5 PCLKA	section 22.
000C 2216h	GPT2	General PWM Timer Compare Capture Register D	GTCCRD	16	16, 32	4 or 5 PCLKA	section 22.
000C 2218h	GPT2	General PWM Timer Compare Capture Register E	GTCCRE	16	16, 32	4 or 5 PCLKA	section 22.
000C 221Ah	GPT2	General PWM Timer Compare Capture Register F	GTCCRF	16	16, 32	4 or 5 PCLKA	section 22.
000C 221Ch	GPT2	General PWM Timer Period Setting Register	GTPR	16	16, 32	4 or 5 PCLKA	section 22.
000C 221Eh	GPT2	General PWM Timer Period Setting Buffer Register	GTPBR	16	16, 32	4 or 5 PCLKA	section 22.
000C 2220h	GPT2	General PWM Timer Period Setting Double Buffer Register	GTPDBR	16	16, 32	4 or 5 PCLKA	section 22.
000C 2224h	GPT2	A/D Converter Start Request Timing Register A	GTADTRA	16	16, 32	4 or 5 PCLKA	section 22.
000C 2226h	GPT2	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16, 32	4 or 5 PCLKA	section 22.
000C 2228h	GPT2	A/D Converter Start Request Timing Double Buffer Register A	GTADTDBRA	16	16, 32	4 or 5 PCLKA	section 22.
000C 222Ch	GPT2	A/D Converter Start Request Timing Register B	GTADTRB	16	16, 32	4 or 5 PCLKA	section 22.
000C 222Eh	GPT2	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16, 32	4 or 5 PCLKA	section 22.
000C 2230h	GPT2	A/D Converter Start Request Timing Double Buffer Register B	GTADTDBRB	16	16, 32	4 or 5 PCLKA	section 22.
000C 2234h	GPT2	General PWM Timer Output Negate Control Register	GTONCR	16	16, 32	4 or 5 PCLKA	section 22.
000C 2236h	GPT2	General PWM Timer Dead Time Control Register	GTDTCR	16	16, 32	4 or 5 PCLKA	section 22.
000C 2238h	GPT2	General PWM Timer Dead Time Value Register U	GTDVU	16	16, 32	4 or 5 PCLKA	section 22.
000C 223Ah	GPT2	General PWM Timer Dead Time Value Register D	GTDVD	16	16, 32	4 or 5 PCLKA	section 22.
000C 223Ch	GPT2	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16, 32	4 or 5 PCLKA	section 22.
000C 223Eh	GPT2	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16, 32	4 or 5 PCLKA	section 22.
000C 2240h	GPT2	General PWM Timer Output Protection Function Status Register	GTSOS	16	16, 32	4 or 5 PCLKA	section 22.
000C 2242h	GPT2	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16, 32	4 or 5 PCLKA	section 22.
000C 2280h	GPT3	General PWM Timer I/O Control Register	GTIOR	16	8, 16, 32	4 or 5 PCLKA	section 22.
000C 2282h	GPT3	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	8, 16, 32	4 or 5 PCLKA	section 22.
000C 2284h	GPT3	General PWM Timer Control Register	GTCR	16	8, 16, 32	4 or 5 PCLKA	section 22.

Table 5.1 List of I/O Registers (Address Order) (38/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Reference Section
000C 2286h	GPT3	General PWM Timer Buffer Enable Register	GTBER	16	8, 16, 32	4 or 5 PCLKA	section 22.
000C 2288h	GPT3	General PWM Timer Count Direction Register	GTUDC	16	8, 16, 32	4 or 5 PCLKA	section 22.
000C 228Ah	GPT3	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	GTITC	16	8, 16, 32	4 or 5 PCLKA	section 22.
000C 228Ch	GPT3	General PWM Timer Status Register	GTST	16	8, 16, 32	4 or 5 PCLKA	section 22.
000C 228Eh	GPT3	General PWM Timer Counter	GTCNT	16	16	4 or 5 PCLKA	section 22.
000C 2290h	GPT3	General PWM Timer Compare Capture Register A	GTCCRA	16	16, 32	4 or 5 PCLKA	section 22.
000C 2292h	GPT3	General PWM Timer Compare Capture Register B	GTCCRB	16	16, 32	4 or 5 PCLKA	section 22.
000C 2294h	GPT3	General PWM Timer Compare Capture Register C	GTCCRC	16	16, 32	4 or 5 PCLKA	section 22.
000C 2296h	GPT3	General PWM Timer Compare Capture Register D	GTCCRD	16	16, 32	4 or 5 PCLKA	section 22.
000C 2298h	GPT3	General PWM Timer Compare Capture Register E	GTCCRE	16	16, 32	4 or 5 PCLKA	section 22.
000C 229Ah	GPT3	General PWM Timer Compare Capture Register F	GTCCRF	16	16, 32	4 or 5 PCLKA	section 22.
000C 229Ch	GPT3	General PWM Timer Period Setting Register	GTPR	16	16, 32	4 or 5 PCLKA	section 22.
000C 229Eh	GPT3	General PWM Timer Period Setting Buffer Register	GTPBR	16	16, 32	4 or 5 PCLKA	section 22.
000C 22A0h	GPT3	General PWM Timer Period Setting Double Buffer Register	GTPDBR	16	16, 32	4 or 5 PCLKA	section 22.
000C 22A4h	GPT3	A/D Converter Start Request Timing Register A	GTADTRA	16	16, 32	4 or 5 PCLKA	section 22.
000C 22A6h	GPT3	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16, 32	4 or 5 PCLKA	section 22.
000C 22A8h	GPT3	A/D Converter Start Request Timing Double Buffer Register A	GTADTDBRA	16	16, 32	4 or 5 PCLKA	section 22.
000C 22ACh	GPT3	A/D Converter Start Request Timing Register B	GTADTRB	16	16, 32	4 or 5 PCLKA	section 22.
000C 22AEh	GPT3	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16, 32	4 or 5 PCLKA	section 22.
000C 22B0h	GPT3	A/D Converter Start Request Timing Double Buffer Register B	GTADTDBRB	16	16, 32	4 or 5 PCLKA	section 22.
000C 22B4h	GPT3	General PWM Timer Output Negate Control Register	GTONCR	16	16, 32	4 or 5 PCLKA	section 22.
000C 22B6h	GPT3	General PWM Timer Dead Time Control Register	GTDTCR	16	16, 32	4 or 5 PCLKA	section 22.
000C 22B8h	GPT3	General PWM Timer Dead Time Value Register U	GTDVU	16	16, 32	4 or 5 PCLKA	section 22.
000C 22BAh	GPT3	General PWM Timer Dead Time Value Register D	GTDVD	16	16, 32	4 or 5 PCLKA	section 22.
000C 22BCh	GPT3	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16, 32	4 or 5 PCLKA	section 22.
000C 22BEh	GPT3	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16, 32	4 or 5 PCLKA	section 22.
000C 22C0h	GPT3	General PWM Timer Output Protection Function Status Register	GTSOS	16	16, 32	4 or 5 PCLKA	section 22.
000C 22C2h	GPT3	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16, 32	4 or 5 PCLKA	section 22.
000C 2300h	GPT01	General PWM Timer Longword Counter	GTCNTLW	32	32	4 or 5 PCLKA	section 22.
000C 2304h	GPT01	General PWM Timer Longword Compare Capture Register A	GTCCRALW	32	32	4 or 5 PCLKA	section 22.
000C 2308h	GPT01	General PWM Timer Longword Compare Capture Register B	GTCCRBLW	32	32	4 or 5 PCLKA	section 22.
000C 230Ch	GPT01	General PWM Timer Longword Compare Capture Register C	GTCCRCLW	32	32	4 or 5 PCLKA	section 22.
000C 2310h	GPT01	General PWM Timer Longword Compare Capture Register D	GTCCRDLW	32	32	4 or 5 PCLKA	section 22.
000C 2314h	GPT01	General PWM Timer Longword Compare Capture Register E	GTCCRELW	32	32	4 or 5 PCLKA	section 22.
000C 2318h	GPT01	General PWM Timer Longword Compare Capture Register F	GTCCRFLW	32	32	4 or 5 PCLKA	section 22.
000C 231Ch	GPT01	General PWM Timer Longword Period Setting Register	GTPRLW	32	32	4 or 5 PCLKA	section 22.
000C 2320h	GPT01	General PWM Timer Longword Period Setting Buffer Register	GTPBRLW	32	32	4 or 5 PCLKA	section 22.
000C 2324h	GPT01	General PWM Timer Longword Period Setting Double Buffer Register	GTPDBRLW	32	32	4 or 5 PCLKA	section 22.
000C 2328h	GPT01	Longword A/D Converter Start Request Timing Register A	GTADTRALW	32	32	4 or 5 PCLKA	section 22.
000C 232Ch	GPT01	Longword A/D Converter Start Request Timing Buffer Register A	GTADTBRALW	32	32	4 or 5 PCLKA	section 22.
000C 2330h	GPT01	Longword A/D Converter Start Request Timing Double Buffer Register A	GTADTDBRALW	32	32	4 or 5 PCLKA	section 22.
000C 2334h	GPT01	Longword A/D Converter Start Request Timing Register B	GTADTRBLW	32	32	4 or 5 PCLKA	section 22.

Table 5.1 List of I/O Registers (Address Order) (39/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Reference Section
000C 2338h	GPT01	Longword A/D Converter Start Request Timing Buffer Register B	GTADTBRBLW	32	32	4 or 5 PCLKA	section 22.
000C 233Ch	GPT01	Longword A/D Converter Start Request Timing Double Buffer Register B	GTADTDBRBLW	32	32	4 or 5 PCLKA	section 22.
000C 2340h	GPT01	General PWM Timer Longword Dead Time Value Register U	GTDVULW	32	32	4 or 5 PCLKA	section 22.
000C 2344h	GPT01	General PWM Timer Longword Dead Time Value Register D	GTDVDLW	32	32	4 or 5 PCLKA	section 22.
000C 2348h	GPT01	General PWM Timer Longword Dead Time Buffer Register U	GTDBULW	32	32	4 or 5 PCLKA	section 22.
000C 234Ch	GPT01	General PWM Timer Longword Dead Time Buffer Register D	GTDBDLW	32	32	4 or 5 PCLKA	section 22.
000C 2380h	GPT23	General PWM Timer Longword Counter	GTCNTLW	32	32	4 or 5 PCLKA	section 22.
000C 2384h	GPT23	General PWM Timer Longword Compare Capture Register A	GTCCRALW	32	32	4 or 5 PCLKA	section 22.
000C 2388h	GPT23	General PWM Timer Longword Compare Capture Register B	GTCCRBLW	32	32	4 or 5 PCLKA	section 22.
000C 238Ch	GPT23	General PWM Timer Longword Compare Capture Register C	GTCCRCLW	32	32	4 or 5 PCLKA	section 22.
000C 2390h	GPT23	General PWM Timer Longword Compare Capture Register D	GTCCRDLW	32	32	4 or 5 PCLKA	section 22.
000C 2394h	GPT23	General PWM Timer Longword Compare Capture Register E	GTCCRELW	32	32	4 or 5 PCLKA	section 22.
000C 2398h	GPT23	General PWM Timer Longword Compare Capture Register F	GTCCRFLW	32	32	4 or 5 PCLKA	section 22.
000C 239Ch	GPT23	General PWM Timer Longword Period Setting Register	GTPRLW	32	32	4 or 5 PCLKA	section 22.
000C 23A0h	GPT23	General PWM Timer Longword Period Setting Buffer Register	GTPBRLW	32	32	4 or 5 PCLKA	section 22.
000C 23A4h	GPT23	General PWM Timer Longword Period Setting Double Buffer Register	GTPDBRLW	32	32	4 or 5 PCLKA	section 22.
000C 23A8h	GPT23	Longword A/D Converter Start Request Timing Register A	GTADTRALW	32	32	4 or 5 PCLKA	section 22.
000C 23ACh	GPT23	Longword A/D Converter Start Request Timing Buffer Register A	GTADTBRALW	32	32	4 or 5 PCLKA	section 22.
000C 23B0h	GPT23	Longword A/D Converter Start Request Timing Double Buffer Register A	GTADTDBRALW	32	32	4 or 5 PCLKA	section 22.
000C 23B4h	GPT23	Longword A/D Converter Start Request Timing Register B	GTADTRBLW	32	32	4 or 5 PCLKA	section 22.
000C 23B8h	GPT23	Longword A/D Converter Start Request Timing Buffer Register B	GTADTBRBLW	32	32	4 or 5 PCLKA	section 22.
000C 23BCh	GPT23	Longword A/D Converter Start Request Timing Double Buffer Register B	GTADTDBRBLW	32	32	4 or 5 PCLKA	section 22.
000C 23C0h	GPT23	General PWM Timer Longword Dead Time Value Register U	GTDVULW	32	32	4 or 5 PCLKA	section 22.
000C 23C4h	GPT23	General PWM Timer Longword Dead Time Value Register D	GTDVDLW	32	32	4 or 5 PCLKA	section 22.
000C 23C8h	GPT23	General PWM Timer Longword Dead Time Buffer Register U	GTDBULW	32	32	4 or 5 PCLKA	section 22.
000C 23CCh	GPT23	General PWM Timer Longword Dead Time Buffer Register D	GTDBDLW	32	32	4 or 5 PCLKA	section 22.
000D 0000h	SCI11	Serial Mode Register	SMR	8	8	3 or 4 PCLKA	section 26.
000D 0001h	SCI11	Bit Rate Register	BRR	8	8	3 or 4 PCLKA	section 26.
000D 0002h	SCI11	Serial Control Register	SCR	8	8	3 or 4 PCLKA	section 26.
000D 0003h	SCI11	Transmit Data Register	TDR	8	8	3 or 4 PCLKA	section 26.
000D 0004h	SCI11	Serial Status Register	SSR	8	8	3 or 4 PCLKA	section 26.
000D 0005h	SCI11	Receive Data Register	RDR	8	8	3 or 4 PCLKA	section 26.
000D 0006h	SMCI11	Smart Card Mode Register	SCMR	8	8	3 or 4 PCLKA	section 26.
000D 0007h	SCI11	Serial Extended Mode Register	SEMR	8	8	3 or 4 PCLKA	section 26.
000D 0008h	SCI11	Noise Filter Setting Register	SNFR	8	8	3 or 4 PCLKA	section 26.
000D 0009h	SCI11	I^2C Mode Register 1	SIMR1	8	8	3 or 4 PCLKA	section 26.
000D 000Ah	SCI11	I^2C Mode Register 2	SIMR2	8	8	3 or 4 PCLKA	section 26.
000D 000Bh	SCI11	I^2C Mode Register 3	SIMR3	8	8	3 or 4 PCLKA	section 26.
000D 000Ch	SCI11	I^2C Status Register	SISR	8	8	3 or 4 PCLKA	section 26.
000D 000Dh	SCI11	SPI Mode Register	SPMR	8	8	3 or 4 PCLKA	section 26.
000D 000Eh	SCI11	Transmit Data Register HL	TDRHL	16	16	5 or 6 PCLKA	section 26.

Table 5.1 List of I/O Registers (Address Order) (40/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Reference Section
000D 000Eh	SCI11	Transmit Data Register H	TDRH	8	8	3 or 4 PCLKA	section 26.
000D 000Fh	SCI11	Transmit Data Register L	TDRL	8	8	3 or 4 PCLKA	section 26.
000D 0010h	SCI11	Receive Data Register HL	RDRHL	16	16	5 or 6 PCLKA	section 26.
000D 0010h	SCI11	Receive Data Register H	RDRH	8	8	3 or 4 PCLKA	section 26.
000D 0011h	SCI11	Receive Data Register L	RDRL	8	8	3 or 4 PCLKA	section 26.
000D 0012h	SCI11	Modulation Duty Register	MDDR	8	8	3 or 4 PCLKA	section 26.
007F C090h	FLASH	E2 DataFlash Control Register	DFLCTL	8	8	2 or 3 FCLK	section 36.
007F C100h	FLASH	Flash P/E Mode Control Register	FPMCR	8	8	2 or 3 FCLK	section 36.
007F C104h	FLASH	Flash Area Select Register	FASR	8	8	2 or 3 FCLK	section 36.
007F C108h	FLASH	Flash Processing Start Address Register L	FSARL	16	16	2 or 3 FCLK	section 36.
007F C110h	FLASH	Flash Processing Start Address Register H	FSARH	16	16	2 or 3 FCLK	section 36.
007F C114h	FLASH	Flash Control Register	FCR	8	8	2 or 3 FCLK	section 36.
007F C118h	FLASH	Flash Processing End Address Register L	FEARL	16	16	2 or 3 FCLK	section 36.
007F C120h	FLASH	Flash Processing End Address Register H	FEARH	16	16	2 or 3 FCLK	section 36.
007F C124h	FLASH	Flash Reset Register	FRESETR	8	8	2 or 3 FCLK	section 36.
007F C12Ch	FLASH	Flash Status Register 1	FSTATR1	8	8	2 or 3 FCLK	section 36.
007F C130h	FLASH	Flash Write Buffer 0 Register	FWB0	16	16	2 or 3 FCLK	section 36.
007F C138h	FLASH	Flash Write Buffer 1 Register	FWB1	16	16	2 or 3 FCLK	section 36.
007F C140h	FLASH	Flash Write Buffer 2 Register	FWB2	16	16	2 or 3 FCLK	section 36.
007F C144h	FLASH	Flash Write Buffer 3 Register	FWB3	16	16	2 or 3 FCLK	section 36.
007F C180h	FLASH	Protection Unlock Register	FPR	8	8	2 or 3 FCLK	section 36.
007F C184h	FLASH	Protection Unlock Status Register	FPSR	8	8	2 or 3 FCLK	section 36.
007F C1C0h	FLASH	Flash Start-Up Setting Monitor Register	FSCMR	16	16	2 or 3 FCLK	section 36.
007F C1C8h	FLASH	Flash Access Window Start Address Monitor Register	FAWSMR	16	16	2 or 3 FCLK	section 36.
007F C1D0h	FLASH	Flash Access Window End Address Monitor Register	FAWEMR	16	16	2 or 3 FCLK	section 36.
007F C1D8h	FLASH	Flash Initial Setting Register	FISR	8	8	2 or 3 FCLK	section 36.
007F C1DCh	FLASH	Flash Extra Area Control Register	FEXCR	8	8	2 or 3 FCLK	section 36.
007F C1E0h	FLASH	Flash Error Address Monitor Register L	FEAML	16	16	2 or 3 FCLK	section 36.
007F C1E8h	FLASH	Flash Error Address Monitor Register H	FEAMH	16	16	2 or 3 FCLK	section 36.
007F C1F0h	FLASH	Flash Status Register 0	FSTATR0	8	8	2 or 3 FCLK	section 36.
007F C350h	FLASHCONST	Unique ID Register 0	UIDR0	32	32	2 or 3 FCLK	section 36.
007F C354h	FLASHCONST	Unique ID Register 1	UIDR1	32	32	2 or 3 FCLK	section 36.
007F C358h	FLASHCONST	Unique ID Register 2	UIDR2	32	32	2 or 3 FCLK	section 36.
007F C35Ch	FLASHCONST	Unique ID Register 3	UIDR3	32	32	2 or 3 FCLK	section 36.
007F FFB2h	FLASH	Flash P/E Mode Entry Register	FENTRYR	16	16	2 or 3 FCLK	section 36.

Note 1. Odd addresses cannot be accessed in 16-bit units. When accessing a register in 16-bit units, access the address of the TMR0, TMR2, TMR4, or TMR6 register. Table 23.5 lists register allocation for 16-bit access.

6. Resets

6.1 Overview

The following resets are implemented: RES# pin reset, power-on reset, voltage monitoring 0 reset, voltage monitoring 1 reset, voltage monitoring 2 reset, independent watchdog timer reset, and software reset.
Table 6.1 lists the reset names and sources.

Table 6.1 Reset Names and Sources

Reset Name	Source
RES# pin reset	Voltage input to the RES# pin is driven low.
Power-on reset	VCC rises (voltage monitored: VPOR)*1
Voltage monitoring 0 reset	VCC falls (voltage monitored: Vdet0)*1
Voltage monitoring 1 reset	VCC falls (voltage monitored: Vdet1)*1
Voltage monitoring 2 reset	VCC falls (voltage monitored: Vdet2)*1
Independent watchdog timer reset	The independent watchdog timer underflows, or a refresh error occurs.
Software reset	Register setting

Note 1. For the voltages to be monitored (VPOR, Vdet0, Vdet1, and Vdet2), see section 8, Voltage Detection Circuit (LVDAb) and section 37, Electrical Characteristics.

The internal state and pins are initialized by a reset.
Table 6.2 lists the reset targets to be initialized.

Table 6.2 Targets Initialized by Each Reset Source

Target to be Initialized	Reset Source						
	RES# Pin Reset	Power-On Reset	Voltage Monitoring 0 Reset	Independent Watchdog Timer Reset	Voltage Monitoring 1 Reset	Voltage Monitoring 2 Reset	Software Reset
The power-on reset detect flag (RSTSR0.PORF)	○	—	—	—	—	—	—
Register related to the cold start/warm start determination flag (RSTSR1.CWSF)	—*1	○	—	—	—	—	—
Voltage monitoring 0 reset detect flag (RSTSR0.LVD0RF)	○	○	—	—	—	—	—
The independent watchdog timer reset detect flag (RSTSR2.IWDTRF)	○	○	○	—	—	—	—
Registers related to the independent watchdog timer (IWDTRR, IWDTCR, IWDTSR, IWDTRCR, IWDTCSTPR, ILOCOCR)	○	○	○	—	—	—	—
The voltage monitoring 1 reset detect flag (RSTSR0.LVD1RF)	○	○	○	○	—	—	—
Registers related to voltage monitor function 1 (LVD1CR0, LVCMPCR.LVD1E, LVDLVLR.LVD1LVL[3:0])	○	○	○	○	—	—	—
(LVD1CR1, LVD1SR)	○	○	○	○	—	—	—
The voltage monitoring 2 reset detect flag (RSTSR0.LVD2RF)	○	○	○	○	○	—	—
Registers related to voltage monitor function 2 (LVD2CR0, LVD2E, LVDLVLR.LVD2LVL[1:0])	○	○	○	○	○	—	—
(LVD2CR1, LVD2SR)	○	○	○	○	○	—	—
The software reset detect flag (RSTSR2.SWRF)	○	○	○	○	○	○	—
Registers other than the above, CPU, and internal state	○	○	○	○	○	○	○

○: Targets to be initialized, —: No change occurs.
Note 1. Initialized at a power-on.

When a reset is canceled, the reset exception handling starts. For the reset exception handling, see section 13, Exception Handling.
Table 6.3 lists the pin related to the reset.

Table 6.3 Pin Related to Reset

Pin Name	I/O	Function
RES#	Input	Reset pin

6.2 Register Descriptions

6.2.1 Reset Status Register 0 (RSTSR0)

Address(es): 0008 C290h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	LVD2RF	LVD1RF	LVD0RF	PORF
Value after reset:	0	0	0	0	0*1	0*1	0*1	0*1

Bit	Symbol	Bit Name	Description	R/W
b0	PORF	Power-On Reset Detect Flag	0: Power-on reset not detected. 1: Power-on reset detected.	R(/W) *2
b1	LVD0RF	Voltage Monitoring 0 Reset Detect Flag	0: Voltage monitoring 0 reset not detected. 1: Voltage monitoring 0 reset detected.	R(/W) *2
b2	LVD1RF	Voltage Monitoring 1 Reset Detect Flag	0: Voltage monitoring 1 reset not detected. 1: Voltage monitoring 1 reset detected.	R(/W) *2
b3	LVD2RF	Voltage Monitoring 2 Reset Detect Flag	0: Voltage monitoring 2 reset not detected. 1: Voltage monitoring 2 reset detected.	R(/W) *2
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The value after reset depends on the reset source.
Note 2. Only 0 can be written to clear the flag.

PORF Flag (Power-On Reset Detect Flag)

The PORF flag indicates that a power-on reset has occurred.
[Setting condition]

- When a power-on reset occurs.

[Clearing conditions]

- When resets shown in Table 6.2 occur.
- When PORF is read as 1 and then 0 is written to PORF.

LVD0RF Flag (Voltage Monitoring 0 Reset Detect Flag)

The LVD0RF flag indicates that VCC voltage has fallen below Vdet0.
[Setting condition]

- When Vdet0-level VCC voltage is detected.

[Clearing conditions]

- When resets listed in Table 6.2 occur.
- When LVD0RF is read as 1 and then 0 is written to LVD0RF.

LVD1RF Flag (Voltage Monitoring 1 Reset Detect Flag)

The LVD1RF flag indicates that VCC voltage has fallen below Vdet1.
[Setting condition]

- When Vdet1-level VCC voltage is detected.

[Clearing conditions]

- When a reset listed in Table 6.2 occurs.
- When LVD1RF is read as 1 and then 0 is written to LVD1RF.

LVD2RF Flag (Voltage Monitoring 2 Reset Detect Flag)

The LVD2RF flag indicates that VCC voltage has fallen below Vdet2.

[Setting condition]

- When Vdet2-level VCC voltage is detected.

[Clearing conditions]

- When a reset listed in Table 6.2 occurs.
- When LVD2RF is read as 1 and then 0 is written to LVD2RF.

6.2.2 Reset Status Register 1 (RSTSR1)

Address(es): 0008 C291h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CWSF
Value after reset:	0	0	0	0	0	0	0	0/1*1

Bit	Symbol	Bit Name	Description	R/W
b0	CWSF	Cold/Warm Start Determination Flag	0: Cold start 1: Warm start	R(/W) *2
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The value after reset depends on the reset source.
Note 2. Only 1 can be written to set the flag.

RSTSR1 determines whether a power-on reset has caused the reset processing (cold start) or a reset signal input during operation has caused the reset processing (warm start).

CWSF Flag (Cold/Warm Start Determination Flag)

The CWSF flag indicates the type of reset processing: cold start or warm start.

The CWSF flag is initialized at a power-on.

[Setting condition]

- When 1 is written through programming; it is not set to 0 even when 0 is written.

[Clearing condition]

- When a reset listed in Table 6.2 occurs.

6.2.3 Reset Status Register 2 (RSTSR2)

Address(es): 0008 00C0h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SWRF	—	IWDTRF
Value after reset:	0	0	0	0	0	0*1	0	0*1

Bit	Symbol	Bit Name	Description	R/W
b0	IWDTRF	Independent Watchdog Timer Reset Detect Flag	0: Independent watchdog timer reset not detected. 1: Independent watchdog timer reset detected.	R(/W) *2
b1	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b2	SWRF	Software Reset Detect Flag	0: Software reset not detected. 1: Software reset detected.	R(/W) *2
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The value after reset depends on the reset source.
Note 2. Only 0 can be written to clear the flag.

IWDTRF Flag (Independent Watchdog Timer Reset Detect Flag)

The IWDTRF flag indicates that an independent watchdog timer reset has occurred.

[Setting condition]

- When an independent watchdog timer reset occurs.

[Clearing conditions]

- When a reset listed in Table 6.2 occurs.
- When IWDTRF is read as 1 and then 0 is written to IWDTRF.

SWRF Flag (Software Reset Detect Flag)

The SWRF flag indicates that a software reset has occurred.

[Setting condition]

- When a software reset occurs.

[Clearing conditions]

- When a reset listed in Table 6.2 occurs.
- When SWRF is read as 1 and then 0 is written to SWRF.

6.2.4 Software Reset Register (SWRR)

Address(es): 0008 00C2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SWRR[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	SWRR[15:0]	Software Reset	Writing A501h resets the LSI. These bits are read as 0000h.	R/W

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

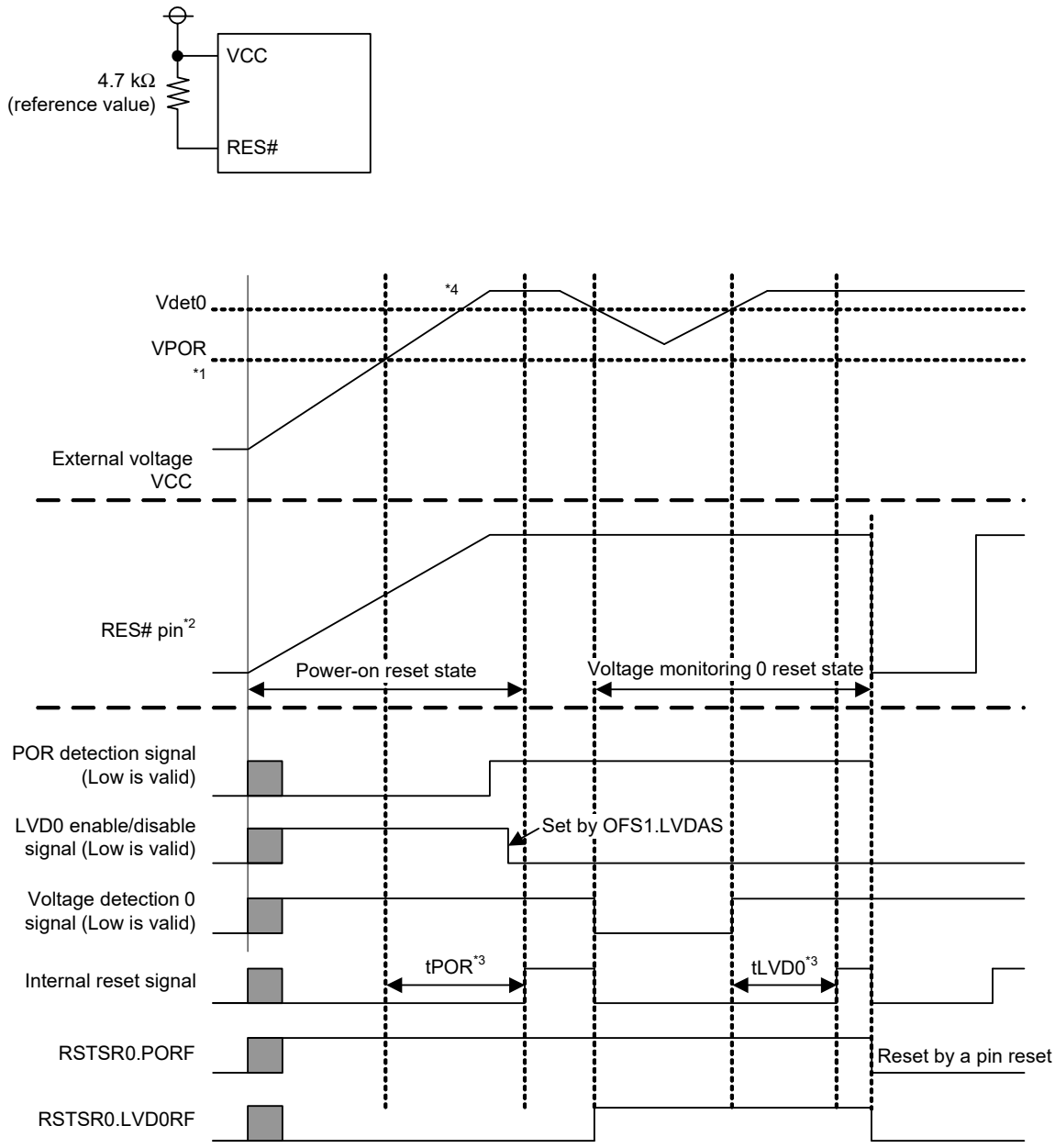
6.3 Operation

6.3.1 RES# Pin Reset

This is a reset generated by the RES# pin.
When the RES# pin is driven low, all the processing in progress is aborted and the LSI enters a reset state.
In order to unfailingly reset the LSI, the RES# pin should be held low for the specified power supply stabilization time at a power-on.
When the RES# pin is driven high from low, the internal reset is canceled after the post-RES# cancellation wait time (tRESWT) has elapsed, and then the CPU starts the reset exception handling.
For details, see section 37, Electrical Characteristics.

6.3.2 Power-On Reset and Voltage Monitoring 0 Reset

The power-on reset is an internal reset generated by the power-on reset circuit. A power-on reset is generated when power is supplied to the RES# pin while it is connected to VCC via a resistor. When connecting a capacitor to the RES# pin, also ensure that the voltage on the RES# pin is always at least VIH. For details on VIH, refer to section 37, Electrical Characteristics. After VCC has exceeded VPOR and the specified period (power-on reset time) has elapsed, the internal reset is canceled and the CPU starts the reset exception handling. The power-on reset time is a stabilization period for the external power supply and the MCU circuit. After a power-on reset has been generated, the PORF flag in RSTSR0 is set to 1. The PORF flag is initialized by RES# pin reset.
The voltage monitoring 0 reset is an internal reset generated by the voltage monitoring circuit. If the voltage detection circuit 0 start bit (LVDAS) in option function select register 1 (OFS1) is 0 (voltage monitoring 0 reset is enabled after a reset) and VCC falls below Vdet0, the RSTSR0.LVD0RF flag becomes 1 and the voltage detection circuit generates voltage monitoring 0 reset. Clear the OFS1.LVDAS bit to 0 if the voltage monitoring 0 reset is to be used.
Release from the voltage monitoring 0 reset state occurs when VCC rises above Vdet0 and the LVD0 reset time (tLVD0) elapses, and then the CPU starts the reset exception handling.
Figure 6.1 shows operations during a power-on reset and voltage monitoring 0 reset.
For details on voltage monitoring 0 reset, refer to section 8, Voltage Detection Circuit (LVDAb).



Note: For details on the electrical characteristics, see the Electrical Characteristics section.
Note 1. Vdet0 indicates the detection level for a voltage monitoring 0 reset and VPOR indicates the detection level for a power-on reset.
Note 2. Ensure that the voltage on the RES# pin is always at least VIH.
Note 3. tPOR indicates the period of a power-on reset and tLVD0 indicates the period of a voltage monitoring 0 reset.
Note 4. At the time the power-supply voltage rises, VCC must rise to at least the minimum guaranteed voltage before release from the POR reset state.

Figure 6.1 Operation Examples During a Power-On Reset and Voltage Monitoring 0 Reset

6.3.3 Voltage Monitoring 1 Reset and Voltage Monitoring 2 Reset

The voltage monitoring 1 reset and voltage monitoring 2 reset are internal resets generated by the voltage monitoring circuit.

When the voltage monitoring 1 interrupt/reset enable bit (LVD1RIE) is set to 1 (enabling generation of a reset or interrupt by the voltage detection circuit) and the voltage monitoring 1 circuit mode select bit (LVD1RI) is set to 1 (selecting generation of a reset in response to detection of a low voltage) in the voltage monitoring 1 circuit control register 0 (LVD1CR0), the RSTSR0.LVD1RF flag is set to 1 and the voltage-detection circuit generates a voltage monitoring 1 reset if VCC falls to or below Vdet1.

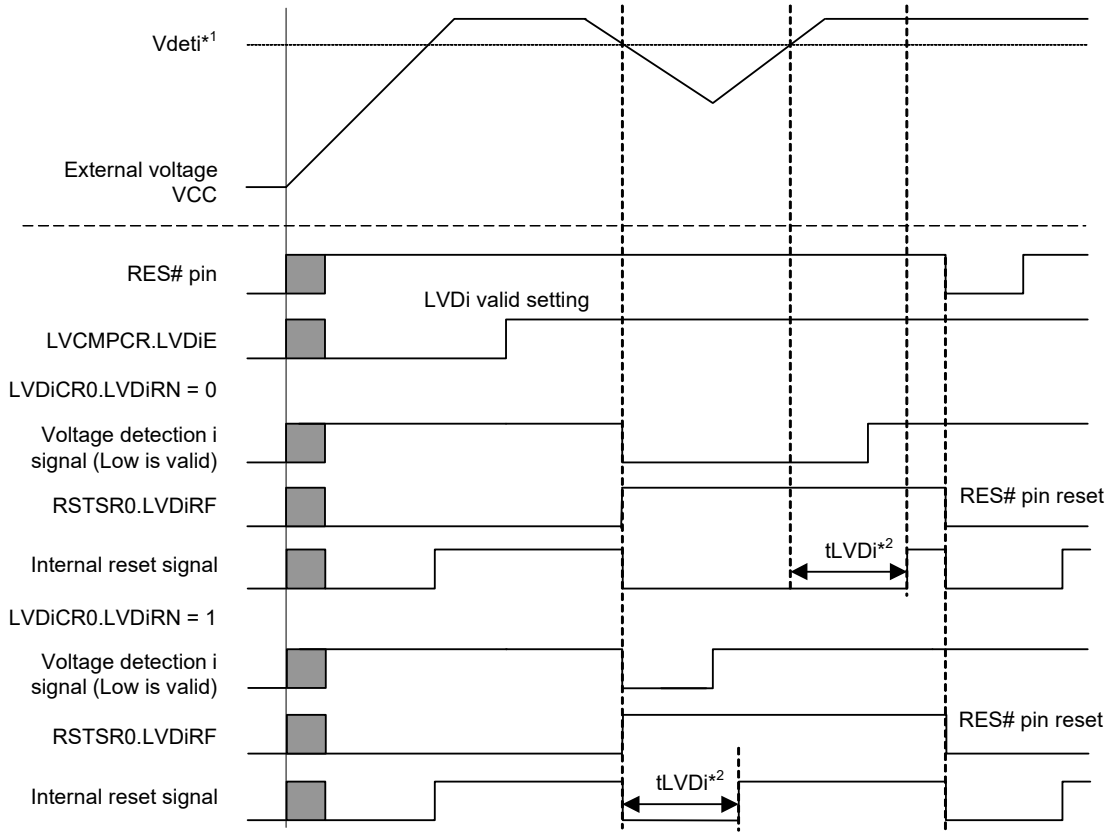
Likewise, when the voltage monitoring 2 interrupt/reset enable bit (LVD2RIE) is set to 1 (enabling generation of a reset or interrupt by the voltage detection circuit) and the voltage monitoring 2 circuit mode select bit (LVD2RI) is set to 1 (selecting generation of a reset in response to detection of a low voltage) in voltage monitoring 2 circuit control register 0 (LVD2CR0), the RSTSR0.LVD2RF flag is set to 1 and the voltage detection circuit generates a voltage monitoring 2 reset if VCC falls to or below Vdet2.

Timing for release from the voltage monitoring 1 reset state is selectable with the voltage monitoring 1 reset negation select bit (LVD1RN) in the LVD1CR0 register. When the LVD1CR0.LVD1RN bit is 0 and VCC has fallen to or below Vdet1, the CPU is released from the internal reset state and starts reset exception handling once the voltage monitoring 1 reset time (tLVD1) has elapsed after VCC has risen above Vdet1. When the LVD1CR0.LVD1RN bit is 1 and VCC has fallen to or below Vdet1, the CPU is released from the internal reset state and starts reset exception handling once the voltage monitoring 1 reset time (tLVD1) has elapsed.

Likewise, timing for release from the voltage monitoring 2 reset state is selectable by setting the voltage monitoring 2 reset negation select bit (LVD2RN) in the LVD2CR0 register. Detection levels Vdet1 and Vdet2 can be changed by settings in the voltage detection level select register (LVDLVLR).

Figure 6.2 shows examples of operations during voltage monitoring 1 and 2 resets.

For details on the voltage monitoring 1 reset and voltage monitoring 2 reset, refer to section 8, Voltage Detection Circuit (LVDAb).



Note: For details on the electrical characteristics, see the Electrical Characteristics section.
Note 1. Vdeti shows a detection level of voltage monitoring 1 reset and voltage monitoring 2 reset. (i = 1, 2)
Note 2. tLVDi shows a time for voltage monitoring 1 reset and voltage monitoring 2 reset. (i = 1, 2)

Figure 6.2 Operation Examples During Voltage Monitoring 1 Reset and Voltage Monitoring 2 Reset

6.3.4 Independent Watchdog Timer Reset

Independent watchdog timer reset is an internal reset generated by the independent watchdog timer.
Output of the independent watchdog timer reset from the independent watchdog timer can be selected by setting the IWDT reset control register (IWDTRCR) and option function select register 0 (OFS0).
When output of the independent watchdog timer reset is selected, an independent watchdog timer reset is generated if the independent watchdog timer underflows, or if data is written outside the refresh-permitted period. When the internal reset time (tRESW2) has elapsed after the independent watchdog timer reset has been generated, the internal reset is canceled and the CPU starts the reset exception handling.
For details on the independent watchdog timer reset, see section 25, Independent Watchdog Timer (IWDTa).

6.3.5 Software Reset

The software reset is an internal reset generated by the software reset circuit.
When A501h is written to SWRR, a software reset is generated. When the internal reset time (tRESW2) has elapsed after the software reset is generated, the internal reset is canceled and the CPU starts the reset exception handling.

6.3.6 Determination of Cold/Warm Start

By reading the CWSF flag in RSTSR1, the type of reset processing caused can be identified; that is, whether a power-on reset has caused the reset processing (cold start) or a reset signal input during operation has caused the reset processing (warm start).

The CWSF flag in RSTSR1 is set to 0 when a power-on reset occurs (cold start); otherwise the flag is not set to 0. The flag is set to 1 when 1 is written to it through programming; it is not set to 0 even when 0 is written.

Figure 6.3 shows an example of cold/warm start determination operation.

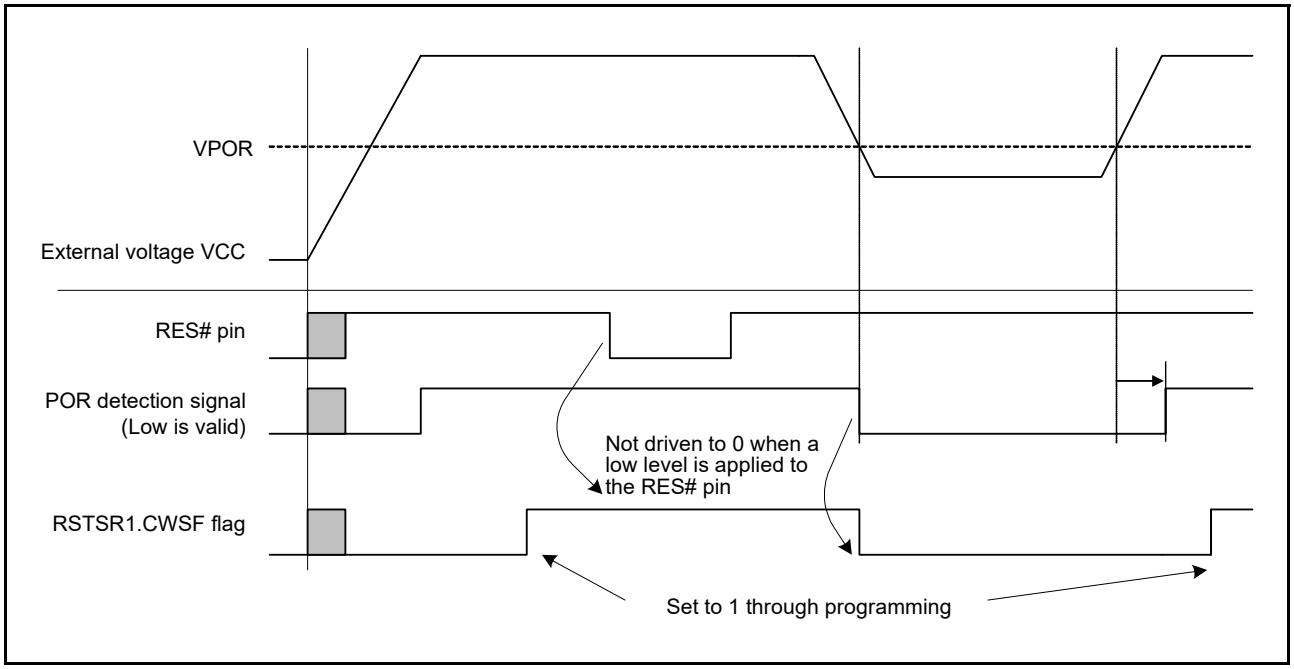


Figure 6.3 Example of Cold/Warm Start Determination Operation

6.3.7 Determination of Reset Generation Source

Reading RSTSR0 and RSTSR2 determines which reset was used to execute the reset exception handling.
Figure 6.4 shows an example of the flow to identify a reset generation source.

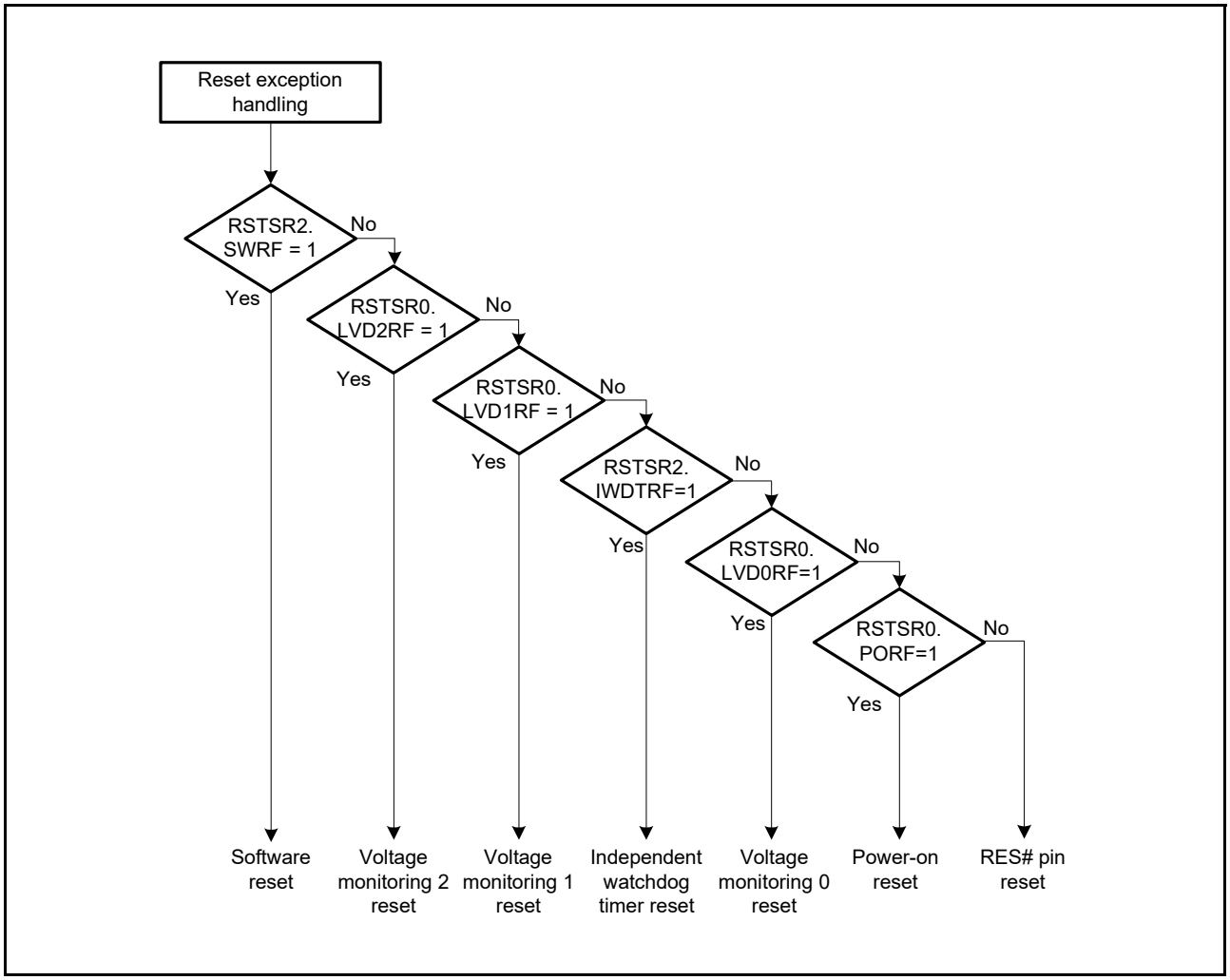


Figure 6.4 Example of Reset Generation Source Determination Flow

7. Option-Setting Memory

7.1 Overview

Option-setting memory refers to a set of registers that are provided for selecting the state of the microcontroller after a reset. The option-setting memory is allocated in the ROM.

Figure 7.1 shows the option-setting memory area.

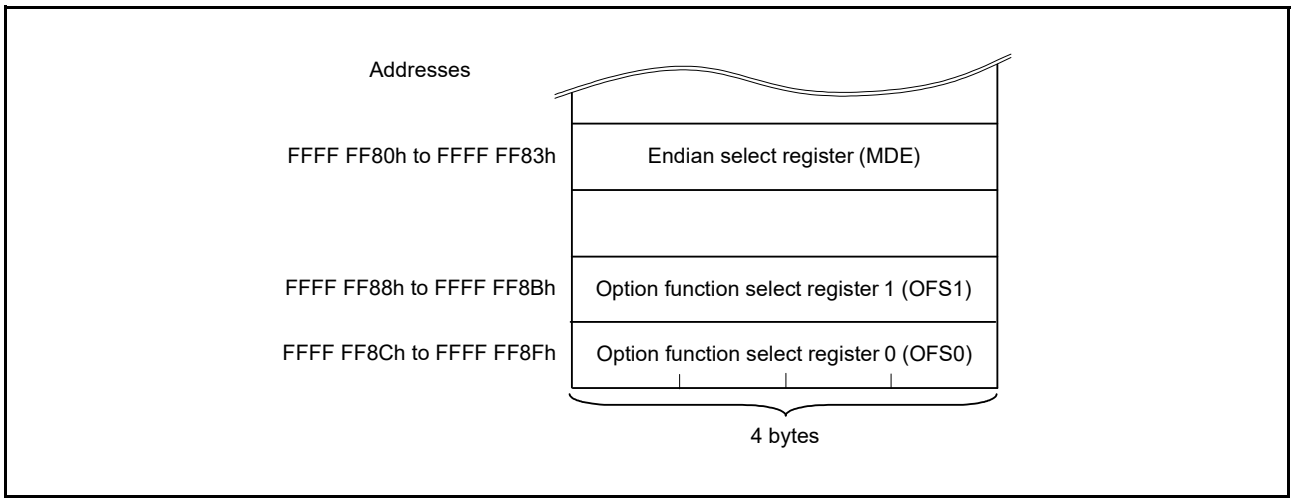


Figure 7.1 Option-Setting Memory Area

7.2 Register Descriptions

7.2.1 Option Function Select Register 0 (OFS0)

Address(es): FFFF FF8Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	The value set by the user*1															

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	—	IWDTSLCSTP	—	IWDTRSTIRQS	IWDTRPSS[1:0]		IWDTRPES[1:0]		IWDTCKS[3:0]				IWDTTOPS[1:0]		IWDTSTRT	—
	The value set by the user*1															

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	When reading, this bit returns the value written by the user. The write value should be 1.	R
b1	IWDTSTRT	IWDT Start Mode Select	0: IWDT is automatically activated in auto-start mode after a reset 1: IWDT is halted after a reset	R
b3, b2	IWDTTOPS[1:0]	IWDT Timeout Period Select	b3 b2 0 0: 128 cycles (007Fh) 0 1: 512 cycles (01FFh) 1 0: 1024 cycles (03FFh) 1 1: 2048 cycles (07FFh)	R
b7 to b4	IWDTCKS[3:0]	IWDT Clock Frequency Division Ratio Select	b7 b4 0 0 0 0: No division 0 0 1 0: Divide-by-16 0 0 1 1: Divide-by-32 0 1 0 0: Divide-by-64 1 1 1 1: Divide-by-128 0 1 0 1: Divide-by-256 Settings other than above are prohibited.	R
b9, b8	IWDTRPES[1:0]	IWDT Window End Position Select	b9 b8 0 0: 75% 0 1: 50% 1 0: 25% 1 1: 0% (No window end position setting)	R
b11, b10	IWDTRPSS[1:0]	IWDT Window Start Position Select	b11 b10 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100% (No window start position setting)	R
b12	IWDTRSTIRQS	IWDT Reset Interrupt Request Select	0: Non-maskable interrupt request is enabled 1: Reset is enabled	R
b13	—	Reserved	When reading, this bit returns the value written by the user. The write value should be 1.	R
b14	IWDTSLCSTP	IWDT Sleep Mode Count Stop Control	0: Counting stop is disabled 1: Counting stop is enabled when entering sleep, software standby, or deep sleep mode	R
b31 to b15	—	Reserved	When reading, these bits return the value written by the user. The write value should be 1.	R

Note 1. The value of the blank product is FFFF FFFFh. It is set to the written value after written by the user.

The OFS0 register is allocated in the ROM. Set this register at the same time as writing the program. After writing to the OFS0 register once, do not write to it again.
When erasing the block including the OFS0 register, the OFS0 register value becomes FFFF FFFFh.

The setting in the OFS0 register is ignored in boot mode, and this register functions similarly when it is set to FFFF FFFFh.

IWDTSTRT Bit (IWDT Start Mode Select)

This bit selects the mode in which the IWDT is activated after a reset (stopped state or activated in auto-start mode). When activated in auto-start mode, the OFS0 register setting for the IWDT is effective.

IWDTTOPS[1:0] Bits (IWDT Timeout Period Select)

These bits select the timeout period, i.e. the time it takes for the down-counter to underflow, as 128, 512, 1024, or 2048 cycles of the frequency-divided clock set by the IWDTCKS[3:0] bits. The time (number of IWDT-dedicated clock cycles) it takes to underflow after a refresh operation is determined by the combination of the IWDTCKS[3:0] bits and IWDTTOPS[1:0] bits.

For details, see section 25, Independent Watchdog Timer (IWDTa).

IWDTCKS[3:0] Bits (IWDT Clock Frequency Division Ratio Select)

These bits select, from 1/1, 1/16, 1/32, 1/64, 1/128, and 1/256, the division ratio of the prescaler to divide the frequency of the IWDT-dedicated clock. Using the setting of these bits together with the IWDTTOPS[1:0] bit setting, the IWDT counting period can be set from 128 to 524288 IWDT-dedicated clock cycles.

For details, see section 25, Independent Watchdog Timer (IWDTa).

IWDTRPES[1:0] Bits (IWDT Window End Position Select)

These bits select the position of the end of the window for the down-counter as 0%, 25%, 50%, or 75% of the value being counted by the counter. The value of the window end position must be smaller than the value of the window start position (window start position > window end position). If the value for the window end position is greater than the value for the window start position, only the value for the window start position is effective.

The counter values corresponding to the settings for the start and end positions of the window in the IWDTRPSS[1:0] and IWDTRPES[1:0] bits vary with the setting of the IWDTTOPS[1:0] bits.

For details, refer to section 25, Independent Watchdog Timer (IWDTa).

IWDTRPSS[1:0] Bits (IWDT Window Start Position Select)

These bits select the position where the window for the down-counter starts as 25%, 50%, 75%, or 100% of the value being counted (the point at which counting starts is 100% and the point at which an underflow occurs is 0%). The interval between the positions where the window starts and ends becomes the period in which refreshing is possible, and refreshing is not possible outside this period.

For details, refer to section 25, Independent Watchdog Timer (IWDTa).

IWDTRSTIRQS Bit (IWDT Reset Interrupt Request Select)

The setting of this bit selects the operation on an underflow of the down-counter or generation of a refresh error. Either an independent watchdog timer reset or a non-maskable interrupt request is selectable.

For details, refer to section 25, Independent Watchdog Timer (IWDTa).

IWDTSLCSTP Bit (IWDT Sleep Mode Count Stop Control)

This bit selects whether to stop counting when entering sleep, software standby, or deep sleep mode.

For details, see section 25, Independent Watchdog Timer (IWDTa).

7.2.2 Option Function Select Register 1 (OFS1)

Address(es): FFFF FF88h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	The value set by the user*1															

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	HOCO EN	—	—	—	—	—	LVDAS	VDSEL[1:0]	
Value after reset:	The value set by the user*1															

Bit	Symbol	Bit Name	Description	R/W
b1, b0	VDSEL[1:0]	Voltage Detection 0 Level Select	b1 b0 0 0: 3.84 V is selected 0 1: 2.82 V is selected 1 0: 2.51 V is selected Settings other than above are prohibited when the voltage detection 0 circuit is used.	R
b2	LVDAS	Voltage Detection 0 Circuit Start	0: Voltage monitoring 0 reset is enabled after a reset 1: Voltage monitoring 0 reset is disabled after a reset	R
b7 to b3	—	Reserved	When reading, these bits return the value written by the user. The write value should be 1.	R
b8	HOCOEN	HOCO Oscillation Enable	0: HOCO oscillation is enabled after a reset 1: HOCO oscillation is disabled after a reset	R
b31 to b9	—	Reserved	When reading, these bits return the value written by the user. The write value should be 1.	R

Note 1. The value of the blank product is FFFF FFFFh. It is set to the written value after written by the user.

The OFS1 register is allocated in the ROM. Set this register at the same time as writing the program. After writing, do not write additions to this register.
When erasing the block including the OFS1 register, the OFS1 register value becomes FFFF FFFFh.
The setting in the OFS1 register is ignored in boot mode, and this register functions similarly when it is set to FFFF FFFFh.

VDSEL[1:0] Bits (Voltage Detection 0 Level Select)

These bits select the voltage detection level to be monitored by the voltage detection 0 circuit.

LVDAS Bit (Voltage Detection 0 Circuit Start)

This bit selects whether the voltage monitoring 0 reset is enabled or disabled after a reset.
The Vdet0 voltage to be monitored by the voltage detection 0 circuit is selected by the VDSEL[1:0] bits.

HOCOEN Bit (HOCO Oscillation Enable)

This bit selects whether the HOCO oscillation is effective or not after a reset.
Setting the HOCOEN bit to 0 allows the HOCO oscillation to be started before the CPU starts operation, and therefore reduces the wait time for oscillation stabilization.
Note that even if the HOCOEN bit is set to 0, the system clock source is not switched to HOCO. The system clock source is switched to HOCO only by modifying the clock source select bits (SCKCR3.CKSEL[2:0]) from the CPU.
Also, when the HOCOEN bit is set to 0, the HOCO oscillation stabilization time (tHOCO) is secured by hardware, so the clock with the accuracy of the HOCO oscillation frequency (fHOCO) shown in Electrical Characteristics is supplied after release from the CPU reset state.

7.2.3 Endian Select Register (MDE)

Address(es): FFFF FF80h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	The value set by the user*1															

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	—	—	—	—	—	—	—	—	—	—	—	—	—	MDE[2:0]		
	The value set by the user*1															

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	MDE[2:0]	Endian Select	b2 b0 0 0 0: Big endian 1 1 1: Little endian Settings other than above are prohibited.	R
b31 to b3	—	Reserved	When reading, these bits return the value written by the user. The write value should be 1.	R

Note 1. The value of the blank product is FFFF FFFFh. It is set to the written value after written by the user.

The MDE register selects the endian for the CPU.MDE is allocated in the ROM. Set the register at the same time as writing the program. After writing to the register once, do not write to it again.
When erasing the block including the MDE register, the MDE register value becomes FFFF FFFFh.

MDE[2:0] Bits (Endian Select)

These bits select little endian or big endian for the CPU.

7.3 Usage Note

7.3.1 Setting Example of Option-Setting Memory

Since the option-setting memory is allocated in the ROM, values cannot be written by executing instructions. Write appropriate values when writing the program. An example of the settings is shown below.

- To set ffff fff8h in the OFS0 register
  .org 0ffff ff8ch
  .lword 0ffffff8h

Note: Programming formats vary depending on the compiler. Refer to the compiler manual for details.

8. Voltage Detection Circuit (LVDAb)

The voltage detection circuit (LVD) monitors the voltage level input to the VCC pin using a program.

8.1 Overview

In voltage detection 0, the detection voltage can be selected from three levels using option function select register 1 (OFS1).
In voltage detection 1, the detection voltage can be selected from nine levels using the voltage detection level select register (LVDLVLR).
In voltage detection 2, the detection voltage can be selected from four levels using the LVDLVLR register.
Voltage monitoring 0 reset, voltage monitoring 1 reset/interrupt, and voltage monitoring 2 reset/interrupt can be used.
Table 8.1 lists the specifications of the voltage detection circuit. Figure 8.1 is a block diagram of the voltage detection circuit. Figure 8.2 is a block diagram of the voltage monitoring 1 interrupt/reset circuit. Figure 8.3 is a block diagram of the voltage monitoring 2 interrupt/reset circuit.

Table 8.1 LVD Specifications

Item		Voltage Monitoring 0	Voltage Monitoring 1	Voltage Monitoring 2
VCC monitoring	Monitored voltage	Vdet0	Vdet1	Vdet2
	Detection target	Voltage drops past Vdet0	When voltage rises above or drops below Vdet1	When voltage rises above or drops below Vdet2
	Detection voltage	Voltage selectable from 3 levels using OFS1	Voltage selectable from 9 levels using the LVDLVLR.LVD1LVL[3:0] bits	Voltage selectable from 4 levels using the LVDLVLR.LVD2LVL[1:0] bits
	Monitoring flag	Not available	LVD1SR.LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR.LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2
			LVD1SR.LVD1DET flag: Vdet1 passage detection	LVD2SR.LVD2DET flag: Vdet2 passage detection
Process upon voltage detection	Reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset
		Reset when Vdet0 > VCC CPU restart after specified time with VCC > Vdet0	Reset when Vdet1 > VCC CPU restart timing selectable: after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC CPU restart timing selectable: after specified time with VCC > Vdet2 or after specified time with Vdet2 > VCC
	Interrupt	Not available	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt
			Non-maskable or maskable interrupt is selectable	Non-maskable or maskable interrupt is selectable
			Interrupt request issued when Vdet1 > VCC and VCC > Vdet1 or either	Interrupt request issued when Vdet2 > VCC and VCC > Vdet2 or either

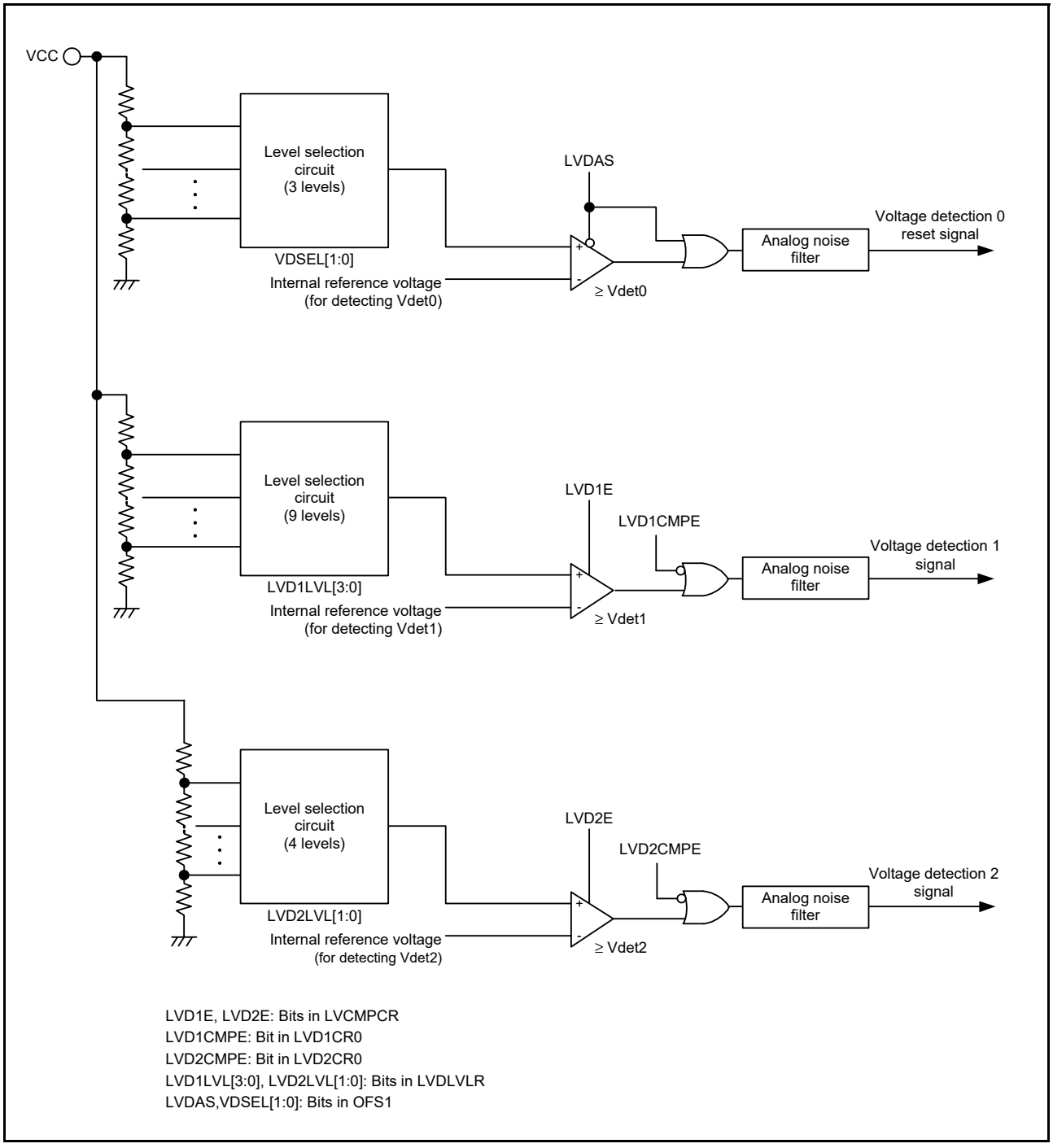


Figure 8.1 Block Diagram of the LVD

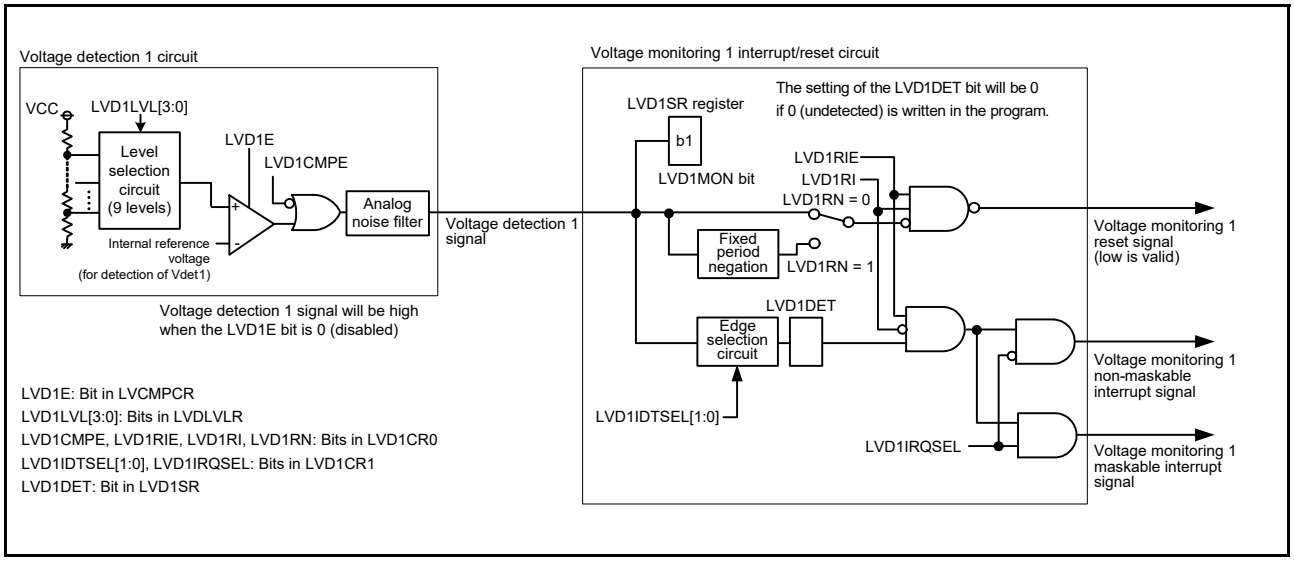


Figure 8.2 Block Diagram of Voltage Monitoring 1 Interrupt/Reset Circuit

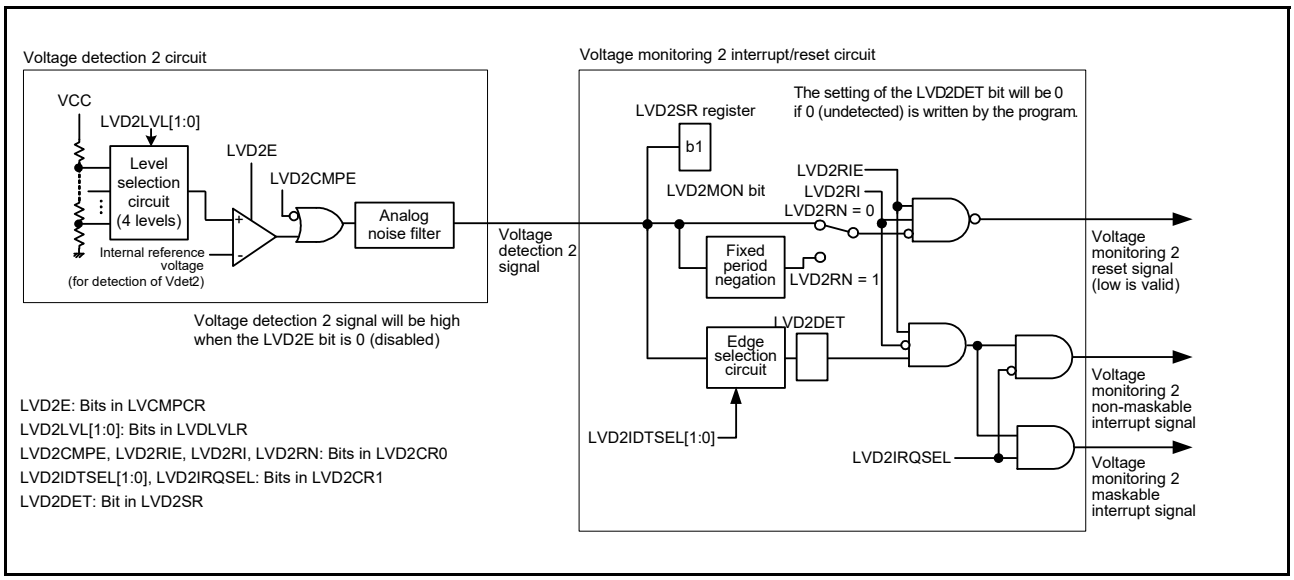


Figure 8.3 Block Diagram of Voltage Monitoring 2 Interrupt/Reset Circuit

8.2 Register Descriptions

8.2.1 Voltage Monitoring 1 Circuit Control Register 1 (LVD1CR1)

Address(es): 0008 00E0h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	LVD1IRQSEL	LVD1IDTSEL[1:0]	
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b1, b0	LVD1IDTSEL[1:0]	Voltage Monitoring 1 Interrupt Generation Condition Select	b1 b0 0 0: When VCC ≥ Vdet1 (rise) is detected 0 1: When VCC < Vdet1 (drop) is detected 1 0: When drop and rise are detected 1 1: Setting prohibited	R/W
b2	LVD1IRQSEL	Voltage Monitoring 1 Interrupt Type Select	0: Non-maskable interrupt 1: Maskable interrupt	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

8.2.2 Voltage Monitoring 1 Circuit Status Register (LVD1SR)

Address(es): 0008 00E1h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	LVD1MON	LVD1DET
Value after reset:	0	0	0	0	0	0	1	0

Bit	Symbol	Bit Name	Description	R/W
b0	LVD1DET	Voltage Monitoring 1 Voltage Change Detection Flag	0: Not detected 1: Vdet1 passage detection	R/(W) *1
b1	LVD1MON	Voltage Monitoring 1 Signal Monitor Flag	0: VCC < Vdet1 1: VCC ≥ Vdet1 or LVD1MON circuit is disabled	R
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.
Note 1. Only 0 can be written to this bit. After writing 0 to this bit, it takes two system clock cycles for the bit to be read as 0.

LVD1DET Flag (Voltage Monitoring 1 Voltage Change Detection Flag)

The LVD1DET flag is enabled when the LVCMPCR.LVD1E bit is 1 (voltage detection 1 circuit enabled) and the LVD1CR0.LVD1CMPE bit is 1 (voltage monitoring 1 circuit comparison result output enabled).
The LVD1DET flag should be set to 0 after LVD1CR0.LVD1RIE is set to 0 (disabled). LVD1CR0.LVD1RIE can be set to 1 (enabled) again after a period of two or more cycles of PCLKB has elapsed.
With read access to an I/O register which access cycle number is defined by PCLKB, two or more cycles of PCLKB may have to be secured as waiting time.

LVD1MON Flag (Voltage Monitoring 1 Signal Monitor Flag)

The LVD1MON flag is enabled when the LVCMPCR.LVD1E bit is 1 (voltage detection 1 circuit enabled) and the LVD1CR0.LVD1CMPE bit is 1 (voltage monitoring 1 circuit comparison result output enabled).

8.2.3 Voltage Monitoring 2 Circuit Control Register 1 (LVD2CR1)

Address(es): 0008 00E2h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	LVD2IRQSEL	LVD2IDTSEL [1:0]	
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b1, b0	LVD2IDTSEL [1:0]	Voltage Monitoring 2 Interrupt Generation Condition Select	b1 b0 0 0: When VCC ≥ Vdet2 (rise) is detected 0 1: When VCC < Vdet2 (drop) is detected 1 0: When drop and rise are detected 1 1: Setting prohibited	R/W
b2	LVD2IRQSEL	Voltage Monitoring 2 Interrupt Type Select	0: Non-maskable interrupt 1: Maskable interrupt	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

8.2.4 Voltage Monitoring 2 Circuit Status Register (LVD2SR)

Address(es): 0008 00E3h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	LVD2MON	LVD2DET
Value after reset:	0	0	0	0	0	0	1	0

Bit	Symbol	Bit Name	Description	R/W
b0	LVD2DET	Voltage Monitoring 2 Voltage Change Detection Flag	0: Not detected 1: Vdet2 passage detection	R/(W) *1
b1	LVD2MON	Voltage Monitoring 2 Signal Monitor Flag	0: VCC < Vdet2 1: VCC ≥ Vdet2 or LVD2MON is disabled	R
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.
Note 1. Only 0 can be written to this bit. After writing 0 to this bit, it takes two system clock cycles for the bit to be read as 0.

LVD2DET Flag (Voltage Monitoring 2 Voltage Change Detection Flag)

The LVD2DET flag is enabled when the LVCMPCR.LVD2E bit is 1 (voltage detection 2 circuit enabled) and the LVD2CR0.LVD2CMPE bit is 1 (voltage monitoring 2 circuit comparison result output enabled).
The LVD2DET flag should be set to 0 after LVD2CR0.LVD2RIE is set to 0 (disabled). LVD2CR0.LVD2RIE can be set to 1 (enabled) again after a period of two or more cycles of PCLKB has elapsed.
With read access to an I/O register which access cycle number is defined by PCLKB, two or more cycles of PCLKB may have to be secured as waiting time.

LVD2MON Flag (Voltage Monitoring 2 Signal Monitor Flag)

The LVD2MON flag is enabled when the LVCMPCR.LVD2E bit is 1 (voltage detection 2 circuit enabled) and the LVD2CR0.LVD2CMPE bit is 1 (voltage monitoring 2 circuit comparison result output enabled).

8.2.5 Voltage Monitoring Circuit Control Register (LVCMPCR)

Address(es): 0008 C297h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	LVD2E	LVD1E	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5	LVD1E	Voltage Detection 1 Enable	0: Voltage detection 1 circuit disabled 1: Voltage detection 1 circuit enabled	R/W
b6	LVD2E	Voltage Detection 2 Enable	0: Voltage detection 2 circuit disabled 1: Voltage detection 2 circuit enabled	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

LVD1E Bit (Voltage Detection 1 Enable)

When using voltage detection 1 interrupt/reset or the LVD1SR.LVD1MON flag, set the LVD1E bit to 1. The voltage detection 1 circuit starts once $Td_{(E-A)}$ passes after the LVD1E bit value is changed from 0 to 1.

LVD2E Bit (Voltage Detection 2 Enable)

When using voltage detection 2 interrupt/reset or the LVD2SR.LVD2MON flag, set the LVD2E bit to 1. The voltage detection 2 circuit starts once $Td_{(E-A)}$ passes after the LVD2E bit value is changed from 0 to 1.

8.2.6 Voltage Detection Level Select Register (LVDLVLR)

Address(es): 0008 C298h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	LVD2LVL[1:0]		LVD1LVL[3:0]			
Value after reset:	0	0	0	0	0	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	LVD1LVL[3:0]	Voltage Detection 1 Level Select (Standard voltage during drop in voltage)	b3 b0 0 0 0 0: 4.29 V 0 0 0 1: 4.14 V 0 0 1 0: 4.02 V 0 0 1 1: 3.84 V 0 1 0 0: 3.10 V 0 1 0 1: 3.00 V 0 1 1 0: 2.90 V 0 1 1 1: 2.79 V 1 0 0 0: 2.68 V Settings other than those listed above are prohibited.	R/W
b5, b4	LVD2LVL[1:0]	Voltage Detection 2 Level Select (Standard voltage during drop in voltage)	b5 b4 0 0: 4.29V 0 1: 4.14V 1 0: 4.02V 1 1: 3.84V	R/W
b7, b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

When changing the LVDLVLR register, first set the LVCMPCR.LVD1E and LVCMPCR.LVD2E bits to 0 (voltage detection n circuit disabled) (n = 1, 2).

When a setting is made so that the voltage detection level range set by the LVD1LVL[3:0] bits overlaps with the range set by the LVD2LVL[1:0] bits, it cannot be specified which of LVD1 and LVD2 is used for voltage detection. For details on the voltage detection level range, refer to section 37, Electrical Characteristics.

8.2.7 Voltage Monitoring 1 Circuit Control Register 0 (LVD1CR0)

Address(es): 0008 C29Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	LVD1RN	LVD1RI	—	—	—	LVD1CMPE	—	LVD1RIE
Value after reset:	1	0	0	0	X	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b0	LVD1RIE	Voltage Monitoring 1 Interrupt/Reset Enable	0: Disabled 1: Enabled	R/W
b1	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b2	LVD1CMPE	Voltage Monitoring 1 Circuit Comparison Result Output Enable	0: Voltage monitoring 1 circuit comparison results output disabled 1: Voltage monitoring 1 circuit comparison results output enabled	R/W
b3	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b5, b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	LVD1RI	Voltage Monitoring 1 Circuit Mode Select	0: Voltage monitoring 1 interrupt occurs when the voltage passes Vdet1 1: Voltage monitoring 1 reset occurs when the voltage falls below Vdet1	R/W
b7	LVD1RN	Voltage Monitoring 1 Reset Negation Select	0: Negation follows a stabilization time (tLVD1) after VCC > Vdet1 is detected. 1: Negation follows a stabilization time (tLVD1) after assertion of the voltage monitoring 1 reset.	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

LVD1RIE Bit (Voltage Monitoring 1 Interrupt/Reset Enable)

The LVD1RIE bit is enabled when the LVCMPCR.LVD1E bit is set to 1 (voltage detection 1 circuit enabled) and the LVD1CMPE bit is set to 1 (voltage monitoring 1 circuit comparison results output enabled).

Ensure that neither a voltage monitoring 1 reset nor a voltage monitoring 1 non-maskable interrupt is generated during programming or erasure of the flash memory.

LVD1RN Bit (Voltage Monitoring 1 Reset Negation Select)

If the LVD1RN bit is to be set to 1 (negation follows a stabilization time after assertion of the voltage monitoring 1 reset), set the LOCOCR.LCSTP bit to 0 (LOCO is operating). Furthermore, if a transition to software standby mode, the only possible value for the LVD1RN bit is 0 (negation follows a stabilization time after VCC > Vdet1 is detected). Do not set the LVD1RN bit to 1 (negation follows a stabilization time after assertion of the voltage monitoring 1 reset).

8.2.8 Voltage Monitoring 2 Circuit Control Register 0 (LVD2CR0)

Address(es): 0008 C29Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	LVD2RN	LVD2RI	—	—	—	LVD2CMPE	—	LVD2RIE
Value after reset:	1	0	0	0	X	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b0	LVD2RIE	Voltage Monitoring 2 Interrupt/Reset Enable	0: Disabled 1: Enabled	R/W
b1	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b2	LVD2CMPE	Voltage Monitoring 2 Circuit Comparison Result Output Enable	0: Voltage monitoring 2 circuit comparison results output disabled 1: Voltage monitoring 2 circuit comparison results output enabled	R/W
b3	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b5, b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	LVD2RI	Voltage Monitoring 2 Circuit Mode Select	0: Voltage monitoring 2 interrupt during Vdet2 passage 1: Voltage monitoring 2 reset enabled when the voltage falls to and below Vdet2	R/W
b7	LVD2RN	Voltage Monitoring 2 Reset Negation Select	0: Negation follows a stabilization time (tLVD2) after VCC > Vdet2 is detected. 1: Negation follows a stabilization time (tLVD2) after assertion of the voltage monitoring 2 reset.	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

LVD2RIE Bit (Voltage Monitoring 2 Interrupt/Reset Enable)

The LVD2RIE bit is enabled when the LVCMPCR.LVD2E bit is set to 1 (voltage detection 2 circuit enabled) and the LVD2CMPE bit is set to 1 (voltage monitoring 2 circuit comparison results output enabled).

Ensure that neither a voltage monitoring 2 reset nor a voltage monitoring 2 non-maskable interrupt is generated during programming or erasure of the flash memory.

LVD2RN Bit (Voltage Monitoring 2 Reset Negation Select)

If the LVD2RN bit is to be set to 1 (negation follows a stabilization time after assertion of the voltage monitoring 2 reset), set the LOCOCR.LCSTP bit to 0 (LOCO is operating). Furthermore, if a transition to software standby mode, the only possible value for the LVD2RN bit is 0 (negation follows a stabilization time after VCC > Vdet2 is detected). Do not set the LVD2RN bit to 1 (negation follows a stabilization time after assertion of the voltage monitoring 2 reset).

8.3 VCC Input Voltage Monitor

8.3.1 Monitoring Vdet0

Monitoring Vdet0 is not possible.

8.3.2 Monitoring Vdet1

After making the following settings, the LVD1SR.LVD1MON flag can be used to monitor the results of comparison by voltage monitor 1.

(1) Specify the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits (voltage detection 1 level select).
(2) Set the LVCMPCR.LVD1E bit to 1 (voltage detection 1 circuit enabled).
(3) After waiting for $Td_{(E-A)}$, set the LVD1CR0.LVD1CMPE bit to 1 (voltage monitoring 1 circuit comparison results output enabled).

8.3.3 Monitoring Vdet2

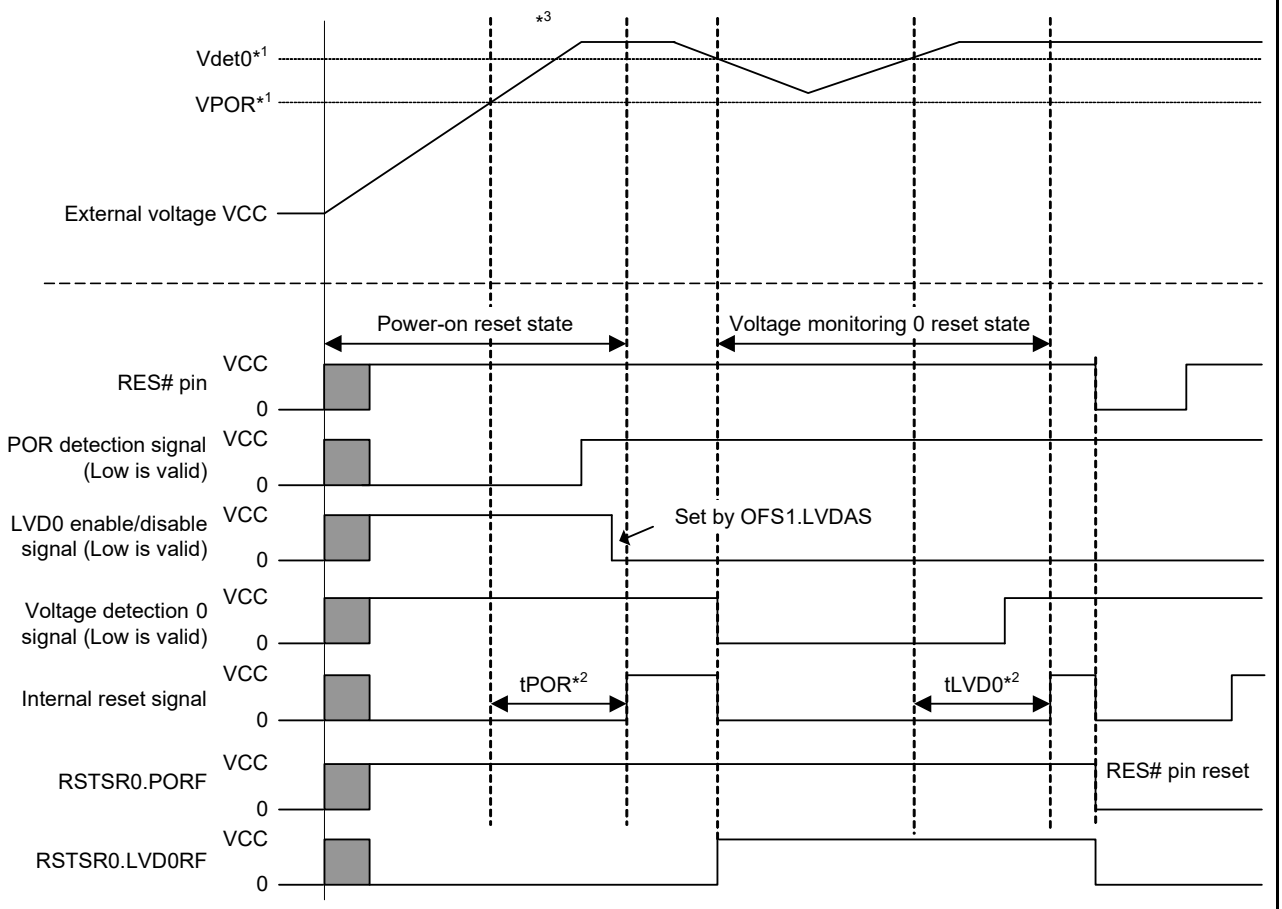
After making the following settings, the LVD2SR.LVD2MON flag can be used to monitor the results of comparison by voltage monitor 2.

(1) Specify the detection voltage by setting the LVDLVLR.LVD2LVL[1:0] bits (voltage detection 2 level select).
(2) Set the LVCMPCR.LVD2E bit to 1 (voltage detection 2 circuit enabled).
(3) After waiting for $Td_{(E-A)}$, set the LVD2CR0.LVD2CMPE bit to 1 (voltage monitoring 2 circuit comparison results output enabled).

8.4 Reset from Voltage Monitor 0

When using the reset from voltage monitor 0, clear the voltage detection 0 circuit start bit (OFS1.LVDAS) to 0 (enabling the voltage monitor 0 reset after a reset).

Figure 8.4 shows an example of operations for a voltage monitoring 0 reset.



Note: For details on the electrical characteristics, see the Electrical Characteristics section.
Note 1. Vdet0 indicates the detection level for a voltage monitoring 0 reset and VPOR indicates the detection level for a power-on reset.
Note 2. tPOR indicates the period of a power-on reset and tLVD0 indicates the period of a voltage monitoring 0 reset.
Note 3. At the time the power-supply voltage rises, VCC must rise to at least the minimum guaranteed voltage before release from the POR reset state.

Figure 8.4 Example of Voltage Monitoring 0 Reset Operation

8.5 Interrupt and Reset from Voltage Monitoring 1

Table 8.2 shows the procedures for setting bits related to the voltage monitoring 1 interrupt and voltage monitoring 1 reset. Table 8.3 shows the procedures for stopping bits related to the voltage monitoring 1 interrupt and voltage monitoring 1 reset. Figure 8.5 shows an example of operations for a voltage monitoring 1 interrupt. For the operation of the voltage monitoring 1 reset, see Figure 6.2 in section 6, Resets.

Table 8.2 Procedures for Setting Bits Related to the Voltage Monitoring 1 Interrupt and Voltage Monitoring 1 Reset

Step	Voltage Monitoring 1 Interrupt	Voltage Monitoring 1 Reset
1*1	Select the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits.	
2*1	Set the LVD1CR0.LVD1RI bit to 0 (voltage monitoring 1 interrupt).	Set the LVD1CR0.LVD1RI bit to 1 (voltage monitoring 1 reset). Select the type of reset negation by setting the LVD1CR0.LVD1RN bit.
3	Select the timing of interrupt requests by setting the LVD1CR1.LVD1IDTSEL[1:0] bits. Select the type of interrupt by setting the LVD1CR1.LVD1IRQSEL bit.	—
4	—	Set the LVD1CR0.LVD1RIE bit to 1 (voltage monitoring 1 interrupt/reset enabled).
5*1	Set the LVCMPCR.LVD1E bit to 1 (voltage detection 1 circuit enabled).	
6*1	Wait for at least $Td_{(E-A)}$.	
7	Set the LVD1CR0.LVD1CMPE bit to 1 (voltage monitoring 1 circuit comparison results output enabled).	
8	Set the LVD1SR.LVD1DET bit to 0.	—
9	Set the LVD1CR0.LVD1RIE bit to 1 (voltage monitoring 1 interrupt/reset enabled).	—

Note 1. Steps 1, 2, 5, and 6 are not required if operation is with the setting to select the voltage monitoring 1 interrupt (LVD1CR0.LVD1RI = 0) and operation can be restarted by simply changing the settings of the LVD1CR1.LVD1IRQSEL and LVD1IDTSEL[1:0] bits after monitoring is stopped or if restarting is in a case where the settings related to the voltage-detection circuit were not changed after monitoring was stopped. When changes are to be made and operation is with the setting to select the voltage monitoring 1 reset (LVD1CR0.LVD1RI = 1), proceed through all steps from 1 to 9.

Table 8.3 Procedures for Stopping Bits Related to the Voltage Monitoring 1 Interrupt and Voltage Monitoring 1 Reset

Step	Voltage Monitoring 1 Interrupt	Voltage Monitoring 1 Reset
1	Set the LVD1CR0.LVD1RIE bit to 0 (voltage monitoring 1 interrupt/reset disabled).	—
2	Set the LVD1CR0.LVD1CMPE bit to 0 (voltage monitoring 1 circuit comparison results output disabled).	
3*1	Set the LVCMPCR.LVD1E bit to 0 (voltage detection 1 circuit disabled).	
4	—	Set the LVD1CR0.LVD1RIE bit to 0 (voltage monitoring 1 interrupt/reset disabled).
5	Modify settings of bits related to the voltage detection circuit registers other than LVCMPCR.LVD1E, LVD1CR0.LVD1RIE, and LVD1CR0.LVD1CMPE.	

Note 1. Step 3 is not required if operation is with the setting to select the voltage monitoring 1 interrupt (LVD1CR0.LVD1RI = 0) and operation can be restarted by simply changing the settings of the LVD1CR1.LVD1IRQSEL and LVD1IDTSEL[1:0] bits after monitoring is stopped or if restarting is in a case where the settings related to the voltage-detection circuit were not changed after monitoring was stopped. When changes are to be made and operation is with the setting to select the voltage monitoring 1 reset (LVD1CR0.LVD1RI = 1), proceed through all steps from 1 to 5.

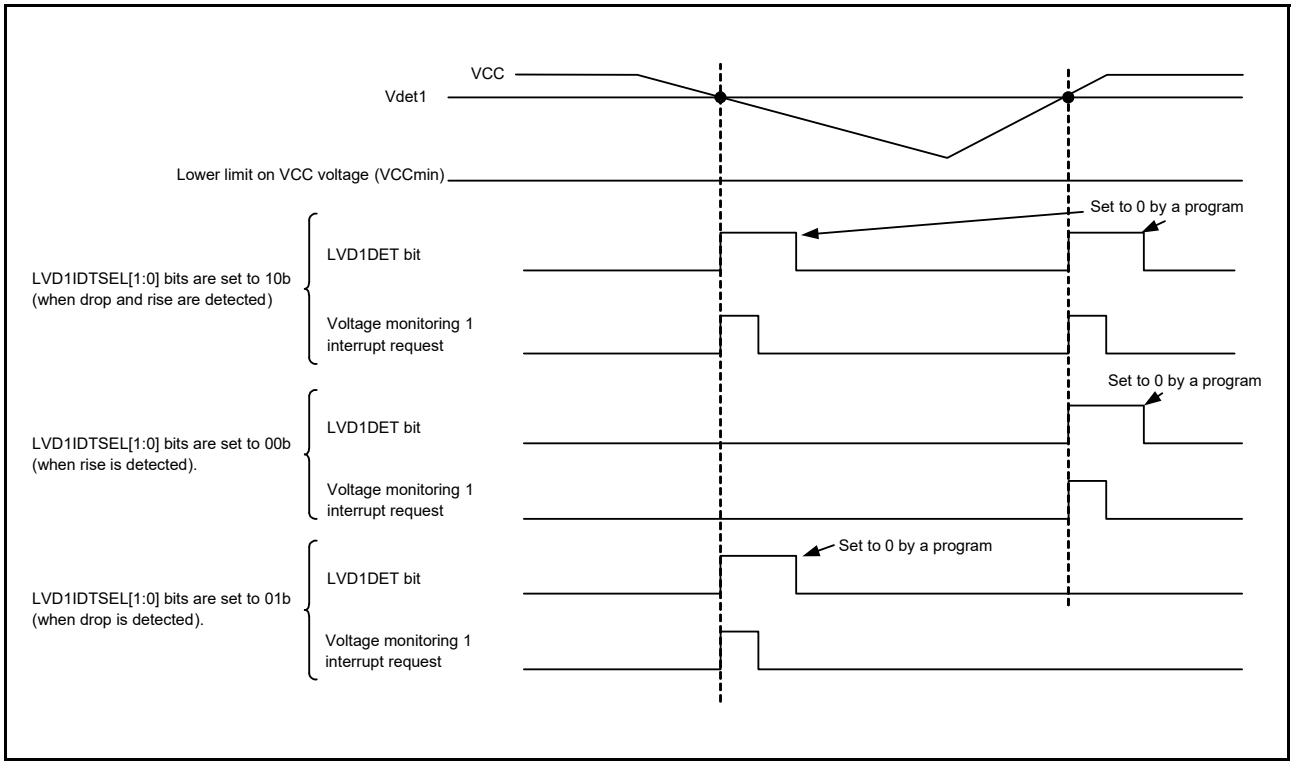


Figure 8.5 Example of Voltage Monitoring 1 Interrupt Operation

8.6 Interrupt and Reset from Voltage Monitoring 2

Table 8.4 shows the procedures for setting bits related to the voltage monitoring 2 interrupt and voltage monitoring 2 reset. Table 8.5 shows the procedure for stopping bits related to the voltage monitoring 2 interrupt and voltage monitoring 2 reset. Figure 8.6 shows an example of operations for a voltage monitoring 2 interrupt. For the operation of the voltage monitoring 2 reset, see Figure 6.2 in section 6, Resets.

Table 8.4 Procedures for Setting Bits Related to the Voltage Monitoring 2 Interrupt and Voltage Monitoring 2 Reset

Step	Voltage Monitoring 2 Interrupt	Voltage Monitoring 2 Reset
1*1	Select the detection voltage by setting the LVDLVLR.LVD2LVL[1:0] bits.	
2*1	Set the LVD2CR0.LVD2RI bit to 0 (voltage monitoring 2 interrupt).	Set the LVD2CR0.LVD2RI bit to 1 (voltage monitoring 2 reset). Select the type of reset negation by setting the LVD2CR0.LVD2RN bit.
3	Select the timing of interrupt requests by setting the LVD2CR1.LVD2IDTSEL[1:0] bits. Select the type of interrupt by setting the LVD2CR1.LVD2IRQSEL bit.	—
4	—	Set the LVD2CR0.LVD2RIE bit to 1 (voltage monitoring 2 interrupt/reset enabled).
5*1	Set the LVCMPCR.LVD2E bit to 1 (voltage detection 2 circuit enabled).	
6*1	Wait for at least $Td_{(E-A)}$.	
7	Set the LVD2CR0.LVD2CMPE bit to 1 (voltage monitoring 2 circuit comparison results output enabled).	
8	Set the LVD2SR.LVD2DET bit to 0.	—
9	Set the LVD2CR0.LVD2RIE bit to 1 (voltage monitoring 2 interrupt/reset enabled)	—

Note 1. Steps 1, 2, 5, and 6 are not required if operation is with the setting to select the voltage monitoring 2 interrupt (LVD2CR0.LVD2RI = 0) and operation can be restarted by simply changing the settings of the LVD2CR1.LVD2IRQSEL and LVD2IDTSEL[1:0] bits after monitoring is stopped or if restarting is in a case where the settings related to the voltage-detection circuit were not changed after monitoring was stopped. When changes are to be made and operation is with the setting to select the voltage monitoring 2 reset (LVD2CR0.LVD2RI = 1), proceed through all steps from 1 to 9.

Table 8.5 Procedures for Stopping Bits Related to the Voltage Monitoring 2 Interrupt and Voltage Monitoring 2 Reset

Step	Voltage Monitoring 2 Interrupt	Voltage Monitoring 2 Reset
1	Set the LVD2CR0.LVD2RIE bit to 0 (voltage monitoring 2 interrupt/reset disabled).	—
2	Set the LVD2CR0.LVD2CMPE bit to 0 (voltage monitoring 2 circuit comparison results output disabled).	
3*1	Set the LVCMPCR.LVD2E bit to 0 (voltage monitoring 2 circuit disabled).	
4	—	Set the LVD2CR0.LVD2RIE bit to 0 (voltage monitoring 2 interrupt/reset disabled).
5	Modify settings of bits related to the voltage detection circuit registers other than LVCMPCR.LVD2E, LVD2CR0.LVD2RIE, and LVD2CR0.LVD2CMPE.	

Note 1. Step 3 is not required if operation is with the setting to select the voltage monitoring 2 interrupt (LVD2CR0.LVD2RI = 0) and operation can be restarted by simply changing the settings of the LVD2CR1.LVD2IRQSEL and LVD2IDTSEL[1:0] bits after monitoring is stopped or if restarting is in a case where the settings related to the voltage-detection circuit were not changed after monitoring was stopped. When changes are to be made and operation is with the setting to select the voltage monitoring 2 reset (LVD2CR0.LVD2RI = 1), proceed through all steps from 1 to 5.

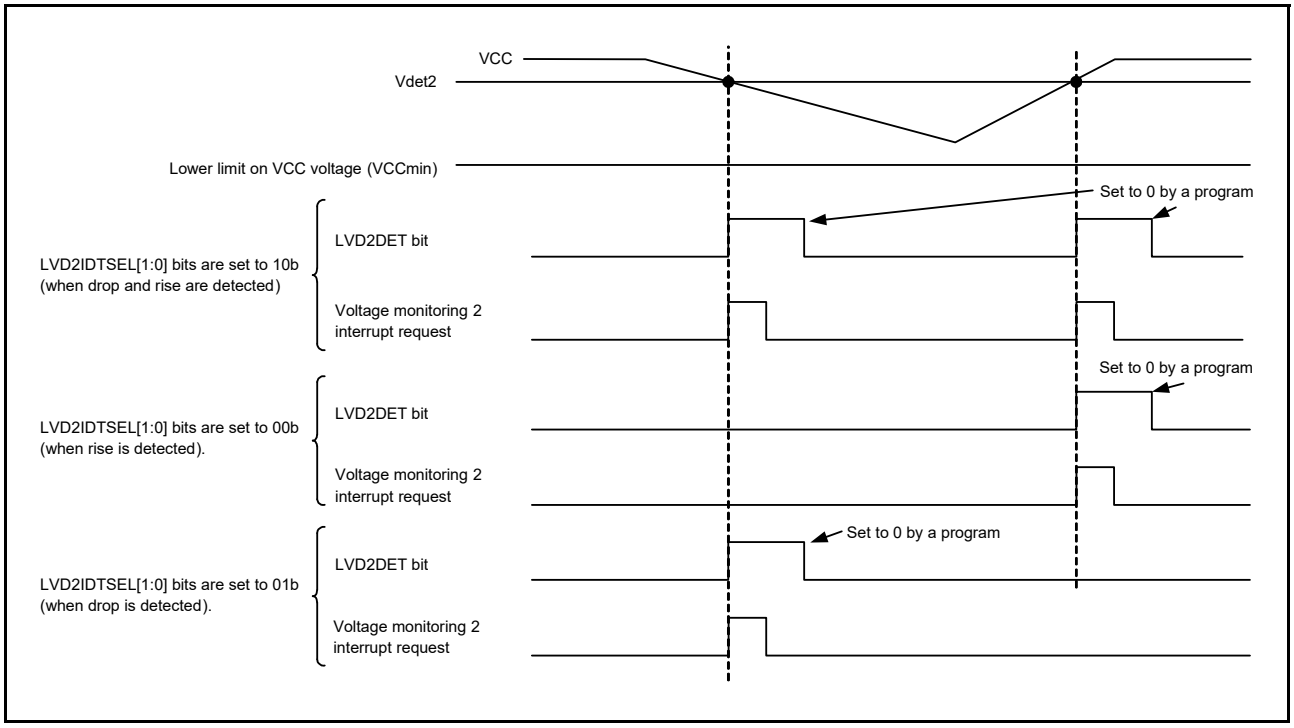


Figure 8.6 Example of Voltage Monitoring 2 Interrupt Operation

9. Clock Generation Circuit

9.1 Overview

This MCU incorporates a clock generation circuit.
Table 9.1 lists the specifications of the clock generation circuit. Figure 9.1 shows a block diagram of the clock generation circuit.

Table 9.1 Specifications of Clock Generation Circuit

Item	Specification
Uses	• Generates the system clock (ICLK) to be supplied to the CPU, DTC, ROM, and RAM. • Generates the peripheral module clocks (PCLKA, PCLKB, and PCLKD) to be supplied to peripheral modules. The peripheral module clock PCLKA is the operating clock for the MTU, GPT, and SCI11, the peripheral module clock PCLKD is for the S12AD, and PCLKB is for other modules. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the IWDT-dedicated low-speed clock (IWDTCLK) to be supplied to the IWDT. • Generates the CAN clock (CANMCLK) to be supplied to the RSCAN
Operating frequencies*1	• ICLK: 80 MHz (max) • PCLKA: 80 MHz (max) • PCLKB: 40 MHz (max) • PCLKD: 40 MHz (max) • FCLK: 1 to 32 MHz (ROM) • CACCLK: Same frequency as each oscillator • IWDTCLK: 15 kHz • CANMCLK: 20 MHz (max)
Main clock oscillator	• Resonator frequency: 1 to 20 MHz • External clock input frequency: 20 MHz (max) • Connectable resonator or additional circuit: ceramic resonator, crystal • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When a main clock oscillation stop is detected, the system clock source is switched to LOCO and MTU and GPT pin output is stopped. • Drive capacity switching function
PLL circuit	• Input clock source: Main clock and HOCO (32 MHz) clock divided by 4 • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 to 12.5 MHz • Frequency multiplication ratio: Selectable from 4 to 15.5 (increments of 0.5) • VCO oscillation frequency: 40 to 80 MHz
High-speed on-chip oscillator (HOCO)	Oscillation frequency: 32 and 64 MHz
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 4 MHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 15 kHz

Note 1. The maximum operating frequency in high-speed operating mode. For the maximum operating frequency in the other operating modes, refer to section 11.2.5, Operating Power Control Register (OPCCR).

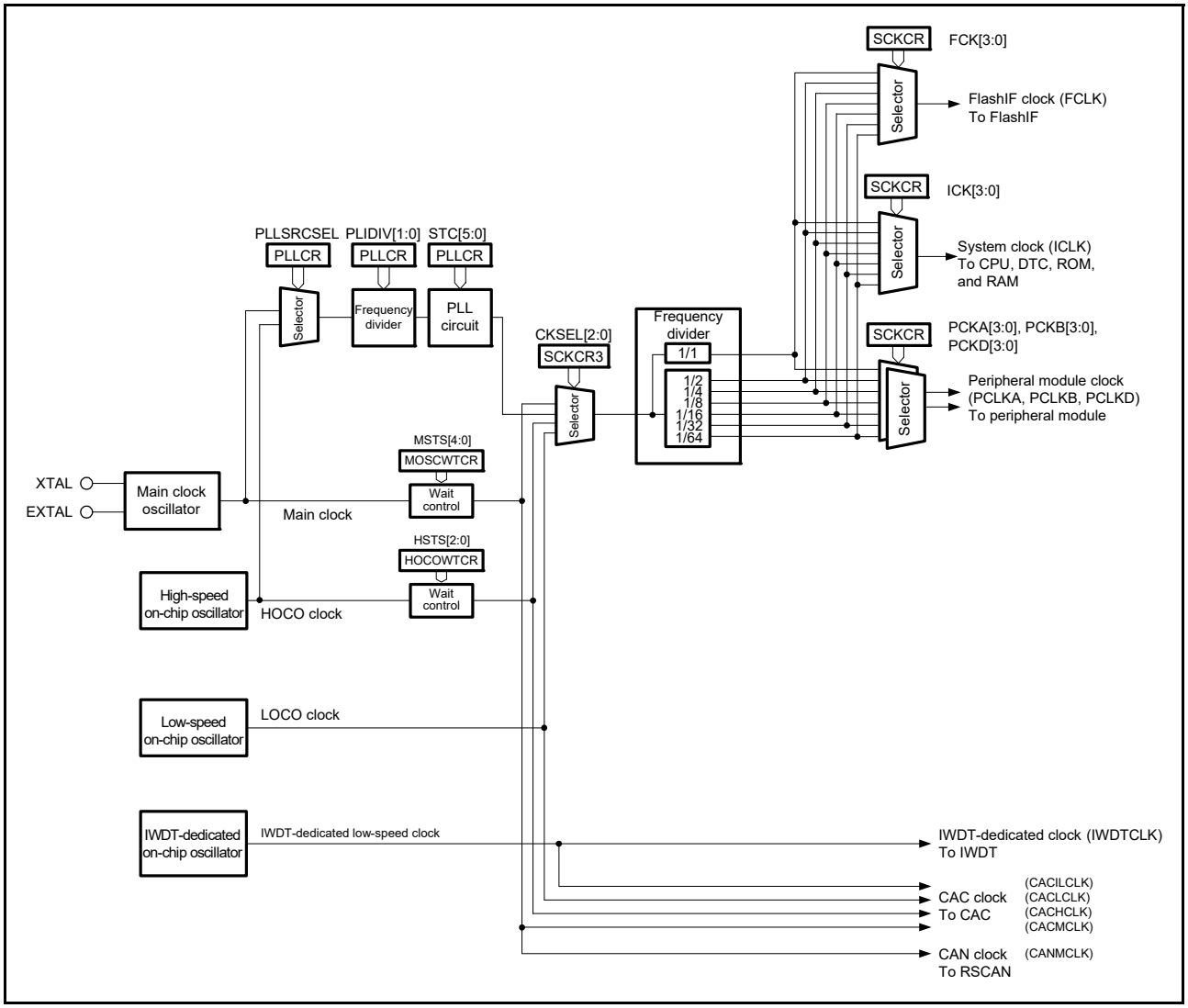


Figure 9.1 Block Diagram of Clock Generation Circuit

Table 9.2 lists the I/O pins of the clock generation circuit.

Table 9.2 I/O Pins of Clock Generation Circuit

Pin Name	I/O	Description
XTAL	Output	These pins are used to connect a crystal. The EXTAL pin can also be used to input an external clock. For details, refer to section 9.3.2, External Clock Input.
EXTAL	Input	

9.2 Register Descriptions

9.2.1 System Clock Control Register (SCKCR)

Address(es): 0008 0020h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	FCK[3:0]				ICK[3:0]				—	—	—	—	—	—	—	—
Value after reset:	0	0	1	1	0	0	1	1	0	0	0	0	0	0	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PCKA[3:0]				PCKB[3:0]				—	—	—	—	PCKD[3:0]			
Value after reset:	0	0	1	1	0	0	1	1	0	0	0	0	0	0	1	1

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	PCKD[3:0] *2	Peripheral Module Clock D (PCLKD) Select	b3 b0 0 0 0 0: ×1 0 0 0 1: ×1/2 0 0 1 0: ×1/4 0 0 1 1: ×1/8 0 1 0 0: ×1/16 0 1 0 1: ×1/32 0 1 1 0: ×1/64 Settings other than above are prohibited.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b11 to b8	PCKB[3:0] *2	Peripheral Module Clock B (PCLKB) Select	b11 b8 0 0 0 0: ×1 0 0 0 1: ×1/2 0 0 1 0: ×1/4 0 0 1 1: ×1/8 0 1 0 0: ×1/16 0 1 0 1: ×1/32 0 1 1 0: ×1/64 Settings other than above are prohibited.	R/W
b15 to b12	PCKA[3:0] *2	Peripheral Module Clock A (PCLKA) Select	b15 b12 0 0 0 0: ×1 0 0 0 1: ×1/2 0 0 1 0: ×1/4 0 0 1 1: ×1/8 0 1 0 0: ×1/16 0 1 0 1: ×1/32 0 1 1 0: ×1/64 Settings other than above are prohibited.	R/W
b19 to b16	—	Reserved	Set the same value as the set value of the PCKB[3:0] bits.	R/W
b23 to b20	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b27 to b24	ICK[3:0] *1, *3	System Clock (ICLK) Select	b27 b24 0 0 0 0: ×1 0 0 0 1: ×1/2 0 0 1 0: ×1/4 0 0 1 1: ×1/8 0 1 0 0: ×1/16 0 1 0 1: ×1/32 0 1 1 0: ×1/64 Settings other than above are prohibited.	R/W

Bit	Symbol	Bit Name	Description	R/W
b31 to b28	FCK[3:0]*2	FlashIF Clock (FCLK) Select	b31 b28 0 0 0 0: ×1 0 0 0 1: ×1/2 0 0 1 0: ×1/4 0 0 1 1: ×1/8 0 1 0 0: ×1/16 0 1 0 1: ×1/32 0 1 1 0: ×1/64 Settings other than above are prohibited.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
Note 1. Do not set the frequency of ICLK higher than 32 MHz when a clock of frequency higher than 32 MHz is selected by the SCKCR3.CKSEL[2:0] bits and MEMWAIT.MEMWAIT [1:0] = 00b.
Note 2. Do not set the frequency higher than the system clock (ICLK).
Note 3. Do not set the frequency of ICLK higher than 64 MHz when a clock of frequency higher than 32 MHz is selected by the SCKCR3.CKSEL[2:0] bits and MEMWAIT.MEMWAIT[1:0] = 01b.

This register cannot be rewritten while the flash memory is being programmed or erased.
When an instruction for writing to SCKCR or SCKCR3 is to follow writing to the SCKCR register, do so in accord with the procedure below.

1. Write to the SCKCR register.
2. Confirm that the value has actually been written to the SCKCR register.
3. Proceed to the next step.

PCKD[3:0] Bits (Peripheral Module Clock D (PCLKD) Select)

These bits select the frequency of peripheral module clock D (PCLKD).

PCKB[3:0] Bits (Peripheral Module Clock B (PCLKB) Select)

These bits select the frequency of peripheral module clock B (PCLKB).

PCKA[3:0] Bits (Peripheral Module Clock A (PCLKA) Select)

These bits select the frequency of peripheral module clock A (PCLKA).

ICK[3:0] Bits (System Clock (ICLK) Select)

These bits select the frequency of the system clock (ICLK).

FCK[3:0] Bits (FlashIF Clock (FCLK) Select)

These bits select the frequency of the FlashIF clock (FCLK).

9.2.2 System Clock Control Register 3 (SCKCR3)

Address(es): 0008 0026h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	CKSEL[2:0]			—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b10 to b8	CKSEL[2:0] *1, *2	Clock Source Select	b10 b8 0 0 0: LOCO 0 0 1: HOCO 0 1 0: Main clock oscillator 1 0 0: PLL circuit Settings other than above are prohibited.	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
Note 1. Do not set the frequency of the system clock (ICLK) higher than 32 MHz, which is selected by the settings of SCKCR.ICK[3:0] and SCKCR3.CKSEL[2:0], when the MEMWAIT.MEMWAIT[1:0] = 00b.
Note 2. Do not set the frequency of the system clock (ICLK) higher than 64 MHz, which is selected by the settings of SCKCR.ICK[3:0] and SCKCR3.CKSEL[2:0], when the MEMWAIT.MEMWAIT[1:0] = 01b.

This register cannot be rewritten while the flash memory is being programmed or erased.

CKSEL[2:0] Bits (Clock Source Select)

These bits select the source of the system clock (ICLK), peripheral module clock (PCLKA, PCLKB, and PCLKD), FlashIF clock (FCLK), from low-speed on-chip oscillator (LOCO), high-speed on-chip oscillator (HOCO), the main clock oscillator, and the PLL circuit.
Transitions to clock sources which are not in operation are prohibited.

9.2.3 PLL Control Register (PLLCR)

Address(es): 0008 0028h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	STC[5:0]						—	—	—	—	—	PLLSRCSEL	PLIDIV[1:0]	
Value after reset:	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	PLIDIV[1:0]	PLL Input Frequency Division Ratio Select	b1 b0 0 0: ×1 0 1: ×1/2 1 0: ×1/4 1 1: Setting prohibited	R/W
b2	PLLSRCSEL	PLL Clock Source Selection	0: The main clock oscillator is selected. 1: HOCO is selected	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13 to b8	STC[5:0]	Frequency Multiplication Factor Select	b13 b8 0 0 0 1 1 1: ×4 0 0 1 0 0 0: ×4.5 0 0 1 0 0 1: ×5 0 0 1 0 1 0: ×5.5 0 0 1 0 1 1: ×6 0 0 1 1 0 0: ×6.5 0 0 1 1 0 1: ×7 0 0 1 1 1 0: ×7.5 0 0 1 1 1 1: ×8 0 1 0 0 0 0: ×8.5 0 1 0 0 0 1: ×9 0 1 0 0 1 0: ×9.5 0 1 0 0 1 1: ×10 0 1 0 1 0 0: ×10.5 0 1 0 1 0 1: ×11 0 1 0 1 1 0: ×11.5 0 1 0 1 1 1: ×12 0 1 1 0 0 0: ×12.5 0 1 1 0 0 1: ×13 0 1 1 0 1 0: ×13.5 0 1 1 0 1 1: ×14 0 1 1 1 0 0: ×14.5 0 1 1 1 0 1: ×15 0 1 1 1 1 0: ×15.5 Settings other than above are prohibited.	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Writing to the PLLCR is prohibited when the PLLCR2.PLLEN bit is 0 (PLL is operating).

PLIDIV[1:0] Bits (PLL Input Frequency Division Ratio Select)

These bits select the frequency division ratio of the PLL clock source.
Set these bits so that the frequency of PLL input signal is within the range of 4 MHz to 12.5 MHz.

PLLSRCSEL Bit (PLL Clock Source Selection)

This bit selects a clock source for PLL.
When the HOCO is selected for a clock source, set the HOCO frequency setting bit (HOCOCR2.HCFRQ[1:0]) in the high-speed on-chip oscillator control register 2 to 00b (the frequency is selected to 32 MHz), and set the oscillation frequency of the HOCO clock to 32 MHz. Set the PLIDIV[1:0] bits to 10b so that the input frequency of the clock source

is divided by 4. Set the PLLCR.STC[5:0] bits to 010011b so that the frequency is multiplied by 10.

STC[5:0] Bits (Frequency Multiplication Factor Select)

These bits select the frequency multiplication factor of the PLL circuit.
Set these bits so that the PLL oscillation frequency is within the range of 40 MHz to 80 MHz.

9.2.4 PLL Control Register 2 (PLLCR2)

Address(es): 0008 002Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	PLLEN
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	PLLEN	PLL Stop Control	0: PLL is operating. 1: PLL is stopped.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

PLLEN Bit (PLL Stop Control)

This bit runs or stops the PLL circuit.
The PLL clock source is selectable as the main clock oscillator and HOCO.
Selecting the main clock oscillator as the PLL clock source with the PLLCR.PLLSRCSEL bit requires setting the main clock oscillator wait control register (MOSCWTCR).
After setting the PLLEN bit to 0 (PLL is operating), confirm that the OSCOVFSR.PLOVF bit is 1 before switching the system clock to the PLL clock.
That is, a fixed time for stabilization is required after the setting for PLL operation. A fixed time is also required for oscillation to stop after the setting to stop PLL operation. Accordingly, take note of the following limitations when starting and stopping PLL operation.
The following notes apply when selecting the main clock oscillator as the PLL clock source.

- After stopping the PLL, confirm that the OSCOVFSR.PLOVF bit is 0 before restarting the PLL.
- Confirm that the PLL is operating and that the OSCOVFSR.PLOVF bit is 1 before stopping the PLL.
- Regardless of whether or not it is selected as the system clock, confirm that the OSCOVFSR.PLOVF bit is 1 before executing a WAIT instruction to place the MCU in software standby mode.
- After stopping the PLL, confirm that the OSCOVFSR.PLOVF bit is 0 and execute a WAIT instruction before entering software standby mode.

When the PLL clock is selected by the SCKCR3.CKSEL[2:0] bits, do not set the PLLEN bit (PLL is stopped) to 1.

9.2.5 Main Clock Oscillator Control Register (MOSCCR)

Address(es): 0008 0032h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	MOSTP
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	MOSTP	Main Clock Oscillator Stop	0: Main clock oscillator is operating. 1: Main clock oscillator is stopped.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Set this register after setting up the main clock oscillator wait control register.

MOSTP Bit (Main Clock Oscillator Stop)

This bit runs or stops the main clock oscillator.
After setting the MOSTP bit to 0 (main clock oscillator is operating), read the OSCOVFSR.MOOVF bit to confirm that is has become 1, and then use the main clock.
For the main clock oscillator, a fixed time is required for oscillation to become stable after the settings for operation have been made. Furthermore, a fixed time is required for oscillation to actually stop after the settings to stop oscillation have been made. Accordingly, take note of the following limitations when starting and stopping operation.

- After stopping the main clock oscillator, confirm that the OSCOVFSR.MOOVF bit is 0 before restarting the main clock oscillator.
- Confirm that the main clock oscillator is operating and that the OSCOVFSR.MOOVF bit is 1 before stopping the main clock oscillator.
- Regardless of whether or not it is selected as the system clock, confirm that the OSCOVFSR.MOOVF bit is 1 and execute a WAIT instruction in order to operate the main clock oscillator and place the MCU in software standby mode.
- After stopping the main clock oscillator, confirm that the OSCOVFSR.MOOVF bit is 0 and execute a WAIT instruction before entering software standby mode.

Do not set the MOSTP bit to 1 when one of the following condition is met.

- When the main clock is selected as the clock source for the system clock (the SCKCR3.CKSEL[2:0] bits are 010b)
- When MOSC is selected as the clock source for PLL (the PLLCR.PLLSRCSEL bit is 0) and the PLL clock is selected as the clock source for the system clock (the SCKCR3.CKSEL[2:0] bits are 100b)
- When MOSC is selected as the clock source for PLL (the PLLCR.PLLSRCSEL bit is 0) and PLL is operating (the PLLCR2.PLLEN bit is 0)

9.2.6 Low-Speed On-Chip Oscillator Control Register (LOCOCR)

Address(es): 0008 0034h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	LCSTP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	LCSTP	LOCO Stop	0: LOCO is operating. 1: LOCO is stopped.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

LCSTP Bit (LOCO Stop)

This bit runs or stops the LOCO.

After the setting of the LCSTP bit has been changed so that the LOCO operates, only start using the LOCO clock after the LOCO clock oscillation stabilization time (t_{LOCO}) has elapsed.

That is, a fixed time for stabilization of oscillation is required after the setting for LOCO operation. A fixed time is also required for oscillation to stop after the setting to stop the oscillator. Accordingly, take note of the following limitations when starting and stopping the oscillator.

- When restarting the LOCO after it has been stopped, allow at least five cycles of the LOCO as an interval over which it is still stopped.
- Ensure that oscillation by the LOCO is stable when making the setting to stop the LOCO.
- Regardless of whether or not it is selected as the system clock, ensure that oscillation by the LOCO is stable before executing a WAIT instruction to place the chip on software standby.
- When a transition to software standby mode is to follow the setting to stop the LOCO, wait for at least three cycles of the LOCO after the setting to stop the LOCO and before executing the WAIT instruction.

While the LOCO is selected by the SCKCR3.CKSEL[2:0] bits, do not set the LCSTP bit to 1 (LOCO is stopped).

9.2.7 IWDT-Dedicated On-Chip Oscillator Control Register (ILOCOCR)

Address(es): 0008 0035h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	ILCSTP
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	ILCSTP	IWDT-Dedicated On-Chip Oscillator Stop	0: IWDT-dedicated on-chip oscillator is operating. 1: IWDT-dedicated on-chip oscillator is stopped.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

When the IWDT start mode select bit in option function select register 0 (OFS0.IWDTSTRT) is 0 (IWDT is operating), the setting of this register is invalid; it is valid only when the OFS0.IWDTSTRT bit is set to 1 (IWDT is stopped). The ILCSTP bit cannot be changed from 0 (IWDT-dedicated on-chip oscillator is operating) to 1 (IWDT-dedicated on-chip oscillator is stopped) while ILOCOCR is valid.

ILCSTP Bit (IWDT-Dedicated On-Chip Oscillator Stop)

This bit runs or stops the IWDT-dedicated on-chip oscillator.

After the setting of the ILCSTP bit has been changed so that the IWDT-dedicated on-chip oscillator operates, supply of the clock is started the MCU internally after a fixed time corresponding to the IWDT-dedicated clock oscillation stabilization time (t_{ILOCO}) has elapsed.

If the IWDT-dedicated clock is to be used, only start using the oscillator after this wait time has elapsed.

Ensure that oscillation by the IWDT-dedicated on-chip oscillator is stable before executing a WAIT instruction to place the chip on software standby mode.

9.2.8 High-Speed On-Chip Oscillator Control Register (HOCOCR)

Address(es): 0008 0036h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	HCSTP
Value after reset:	0	0	0	0	0	0	0	0/1*1

Bit	Symbol	Bit Name	Description	R/W
b0	HCSTP	HOCO Stop	0: HOCO is operating. 1: HOCO is stopped.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
Note 1. The HCSTP bit value after a reset is 0 when the HOCO oscillation enable bit in option function select register 1 (OFS1.HOCOEN) is 0. The HCSTP bit value after a reset is 1 when the OFS1.HOCOEN bit is 1.

Set the high-speed on-chip wait control register before setting this register.

HCSTP Bit (HOCO Stop)

This bit runs or stops the HOCO.
When changing the HCSTP bit from 1 to 0 (i.e. changing the HOCO clock from stopped to operating), confirm that the OSCOVFSR.HCOVF flag is 1 before switching the system clock to the HOCO clock.
That is, a fixed time for stabilization of oscillation is required after the setting for HOCO operation. A fixed time is also required for oscillation to stop after the setting to stop the oscillator. Accordingly, take note of the following limitations when starting and stopping the oscillator.

- After stopping the HOCO, confirm that the OSCOVFSR.HCOVF flag is 0 before restarting the HOCO.
- Confirm that the HOCO is operating and that the OSCOVFSR.HCOVF flag is 1 before stopping the HOCO.
- Regardless of whether or not it is selected as the system clock, confirm that the OSCOVFSR.HCOVF flag is 1 before executing a WAIT instruction to place the MCU in software standby mode.
- After stopping the HOCO, confirm that the OSCOVFSR.HCOVF flag is 0 and execute a WAIT instruction before entering software standby mode.

While the HOCO is selected by the SCKCR3.CKSEL[2:0] bits, do not set the HCSTP bit to 1 (HOCO is stopped).
Writing 1 to the HCSTP bit (the HOCO is stopped) is prohibited when the HOCO is selected as the clock source for PLL (the PLLCR.PLLSRCSEL bit is 1) and the PLL clock is selected as the clock source for the system clock (the SCKCR3.CKSEL[2:0] bits are 100b), and the HOCO is selected as the clock source for PLL (the PLLCR.PLLSRCSEL bit is 1) and while the PLL is operating (the PLLCR2.PLLEN bit is 0).

9.2.9 High-Speed On-Chip Oscillator Control Register 2 (HOCOCR2)

Address(es): 0008 0037h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	HCFRQ[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	HCFRQ[1:0]	HOCO Frequency Setting	b1 b0 0 0: 32 MHz 1 1: 64 MHz Settings other than above are prohibited.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Writing to the HOCOCR2 register is prohibited when the HOCOCR.HCSTP bit is 0 (HOCO is operating).

HCFRQ[1:0] Bits (HOCO Frequency Setting)

These bits set the frequency of the HOCO. When setting the HCFREQ[1:0] bits to 00b and the HOCO frequency to 32 MHz, set the HOCOWTCR.HSTS[2:0] bits to 101b. When setting the HCFREQ[1:0] bits to 11b and the HOCO frequency to 64 MHz, set the HOCOWTCR.HSTS[2:0] bits to 110b.

9.2.10 High-Speed On-Chip Oscillator Wait Control Register (HOCOWTCR)

Address(es): 0008 00A5h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	HSTS[2:0]		
Value after reset:	0	0	0	0	0	1	0	1

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	HSTS[2:0]	High-Speed On-Chip Oscillator Oscillation Stabilization Wait Time	b2 b0 1 0 1: Wait time = 142 cycles (When the HOCO oscillation frequency is set to 32 MHz) 1 1 0: Wait time = 270 cycles (When the HOCO oscillation frequency is set to 64 MHz) Settings other than above are prohibited.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC2 bit to 1 (write enabled) before rewriting this register.

The HOCOWTCR register can be rewritten under the following cases. Otherwise, do not rewrite this register.

- When the HOCOCR.HCSTP bit is set to 0 (operating), and the OSCOVFSR.HCOVF flag is read and confirmed to be 1.
- When the HOCOCR.HCSTP bit is set to 1 (stopped), and the OSCOVFSR.HCOVF flag is read and confirmed to be 0.

HSTS[2:0] Bits (High-Speed On-Chip Oscillator Oscillation Stabilization Wait Time)

These bits are used to select the oscillation stabilization wait time of the HOCO when setting HOCO operation (the HOCOCR.HCSTP bit to 0) and when canceling software standby mode.

When the HOCOCR2.HCFREQ[1:0] bits are set to 00b and the HOCO oscillation frequency is set to 32 MHz, set the HSTS[2:0] bits to 101b. When the HOCOCR2.HCFREQ[1:0] bits are set to 11b and the HOCO oscillation frequency is set to 64 MHz, set the HSTS[2:0] bits to 110b.

Supply of the HOCO clock is started to the MCU internally after the number of LOCO cycles set by the HSTS[2:0] bits has been counted. Counting of LOCO cycles proceeds regardless of the setting of the LOCOCR.LOSTP bit and hardware automatically controls running and stopping the LOCO.

The clock is not supplied to the MCU internally until counting is completed.

After counting is completed, supply of the clock is started to the MCU internally and the OSCOVFSR.HCOVF flag is set to 1.

9.2.11 Oscillation Stabilization Flag Register (OSCOVFSR)

Address(es): 0008 003Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	HCOVF	PLOVF	—	MOOVF
Value after reset:	0	0	0	0	0/1*1	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	MOOVF	Main Clock Oscillation Stabilization Flag	0: Main clock is stopped 1: Oscillation is stable and the clock can be used as the system clock*2	R
b1	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b2	PLOVF	PLL Clock Oscillation Stabilization Flag	0: PLL is stopped or not stabilized 1: Oscillation is stable and the clock can be used as the system clock	R
b3	HCOVF	HOCO Clock Oscillation Stabilization Flag	0: HOCO is stopped or not stabilized 1: Oscillation is stable and the clock can be used as the system clock*2	R
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The HCOVF value after a reset is 1 when the HOCO oscillation enable bit in option function selection register 1 (OFS1.HOCOEN) is 0. The HCOVF value after a reset is 0 when the OFS1.HOCOEN bit is 1.
Note 2. When an appropriate value is set in the wait control register for each oscillator. If a set value (wait time) is not adequate, clock supply starts before oscillation becomes stable.

The OSCOVFSR register monitors whether oscillation of each oscillator has become stable.
If a wait control register is provided for each oscillator, specify a wait time that is longer than or equal to the stabilization time of the corresponding oscillation circuit.

MOOVF Flag (Main Clock Oscillation Stabilization Flag)

This flag indicates whether oscillation of the main clock is stable.
[Setting condition]

- After the MOSCCR.MOSTP bit is set to 0 (main clock oscillator is operating) when the MOSTP bit is 1 (main clock oscillator is stopped), the corresponding time set in the MOSCWTCR register has elapsed and supply of the main clock is started to the MCU internally.

[Clearing condition]

- After the MOSCCR.MOSTP bit is set to 1, the processing to stop the oscillation of the main clock oscillator is completed.

PLOVF Flag (PLL Clock Oscillation Stabilization Flag)

This flag indicates whether oscillation of the PLL clock is stable.
[Setting condition]
After the PLLCR2.PLLEN is set to 0 (PLL is operating) when the PLLEN bit is 1 (PLL is stopped), the MOOVF flag becomes 1, the PLL clock oscillation stabilization time (t_{PLL}) has elapsed, and supply of the PLL clock is started to the MCU internally.
However, if oscillation by the PLL clock source selected in the PLLCR.PLLSRCSEL bit is not stable when the PLLEN bit is set to 0, counting by the LOCO clock counter proceeds after the oscillation of the PLL clock source has become stable.
[Clearing condition]
After the PLLCR2.PLLEN bit is set to 1, the processing to stop the oscillation of the PLL is completed.

HCOVF Flag (HOCO Clock Oscillation Stabilization Flag)

This flag indicates whether oscillation of the HOCO clock is stable.

[Setting condition]

- After the HOCOCR.HCSTP bit is set to 0 (HOCO is operating) when the HCSTP bit is 1 (HOCO is stopped), supply of the HOCO clock is started to the MCU internally.

[Clearing condition]

- After the HOCOCR.HCSTP bit is set to 1, the processing to stop the oscillation of the HOCO is completed.

9.2.12 Oscillation Stop Detection Control Register (OSTDCR)

Address(es): 0008 0040h

	b7	b6	b5	b4	b3	b2	b1	b0
	OSTDE	—	—	—	—	—	—	OSTDIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	OSTDIE	Oscillation Stop Detection Interrupt Enable	0: The oscillation stop detection interrupt is disabled. Oscillation stop detection is not notified to the POE. 1: The oscillation stop detection interrupt is enabled. Oscillation stop detection is notified to the POE.	R/W
b6 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	OSTDE	Oscillation Stop Detection Function Enable	0: Oscillation stop detection function is disabled. 1: Oscillation stop detection function is enabled.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

OSTDIE Bit (Oscillation Stop Detection Interrupt Enable)

If the oscillation stop detection flag in the oscillation stop detection status register (OSTDSR.OSTDF) requires clearing, do this after setting the OSTDIE bit to 0. Wait for at least two cycles of PCLKB before again setting the OSTDIE bit to 1. According to the number of cycles for access to read a given I/O register, wait time longer than two cycles of PCLKB may have to be secured.

OSTDE Bit (Oscillation Stop Detection Function Enable)

This bit enables or disables the oscillation stop detection function.

When the OSTDE bit is 1 (oscillation stop detection function enabled), the LOCO stop bit (LOCOCR.LCSTP) is set to 0 and the LOCO operation is started. The LOCO cannot be stopped while the oscillation stop detection function is enabled; writing 1 (LOCO is stopped) to the LOCOCR.LCSTP bit is invalid.

When the oscillation stop detection flag in the oscillation stop detection status register (OSTDSR.OSTDF) is 1 (main clock oscillation stop has been detected), writing 0 to the OSTDE bit is invalid.

When the OSTDE bit is 1, a transition cannot be made to software standby mode. To make a transition to software standby mode, execute the WAIT instruction with the OSTDE bit being 0.

9.2.13 Oscillation Stop Detection Status Register (OSTDSR)

Address(es): 0008 0041h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	OSTDF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	OSTDF	Oscillation Stop Detection Flag	0: The main clock oscillation stop has not been detected. 1: The main clock oscillation stop has been detected.	R/(W) *1
b7 to b1	—	Reserved	These bits are read as 0 and cannot be modified.	R

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
Note 1. This bit can only be set to 0.

OSTDF Flag (Oscillation Stop Detection Flag)

This bit is a flag to indicate the main clock status. When the OSTDF flag is 1, it indicates that the main clock oscillation stop has been detected.

Once the main clock oscillation stop is detected, the OSTDF flag is not set to 0 even though the main clock oscillation is restarted. The OSTDF flag is set to 0 by reading 1 from the bit and then writing 0. At least three ICLK cycles of wait time is necessary between writing 0 to the OSTDF flag and reading the OSTDF flag as 0. If the OSTDF flag is set to 0 while the main clock oscillation is stopped, the OSTDF flag becomes 0 and then returns to 1.

When the main clock oscillator (010b) or PLL (100b) is selected by the clock source select bits in system clock control register 3 (SCKCR3.CKSEL[2:0]), the OSTDF flag cannot be modified to 0. The OSTDF flag should be set to 0 after switching the clock source to a source other than the main clock oscillator and the PLL.

[Setting condition]

- The main clock oscillation is stopped with the OSTDCR.OSTDE bit being 1 (oscillation stop detection function enabled).

[Clearing condition]

- 1 is read and then 0 is written when the SCKCR3.CKSEL[2:0] bits are neither 010b nor 100b.

9.2.14 Main Clock Oscillator Wait Control Register (MOSCWTCR)

Address(es): 0008 00A2h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	MSTS[4:0]				
Value after reset:	0	0	0	0	0	1	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	MSTS[4:0]	Main Clock Oscillator Wait Time	b4 b0 0 0 0 0 0: Wait time = 2 cycles (0.5 µs) 0 0 0 0 1: Wait time = 1024 cycles (256 µs) 0 0 0 1 0: Wait time = 2048 cycles (512 µs) 0 0 0 1 1: Wait time = 4096 cycles (1.024 ms) 0 0 1 0 0: Wait time = 8192 cycles (2.048 ms) 0 0 1 0 1: Wait time = 16384 cycles (4.096 ms) 0 0 1 1 0: Wait time = 32768 cycles (8.192 ms) 0 0 1 1 1: Wait time = 65536 cycles (16.384 ms) Settings other than above are prohibited. Wait time when LOCO = 4.0 MHz (0.25 µs, TYP.)	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

MSTS[4:0] Bits (Main Clock Oscillator Wait Time)

Set these bits to select the oscillation stabilization wait time of the main clock oscillator.

Set the main clock oscillation stabilization time to longer than or equal to the stabilization time recommended by the oscillator manufacturer. When the main clock is externally input, set these bits to 00000b because the oscillation stabilization time is not required.

The wait time set by the MSTS[4:0] bits is counted using the LOCO clock. The LOCO automatically oscillates when necessary, regardless of the value of the LOCOCR.LCSTP bit.

After the set wait time has elapsed, supply of the main clock is started to the MCU internally and the OSCOVFSR.MOOVF flag becomes 1. If the set wait time is short, supply of the main clock is started before oscillation of the clock becomes stable.

Only rewrite the MOSCWTCR register when the MOSCCR.MOSTP bit is 1 and the OSCOVFSR.MOOVF flag is 0. Do not rewrite this register under any other conditions.

9.2.15 Main Clock Oscillator Forced Oscillation Control Register (MOFCR)

Address(es): 0008 C293h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	MOSEL	MODRV21	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5	MODRV21	Main Clock Oscillator Drive Capability Switch	0: 1 MHz or higher and lower than 10 MHz 1: 10 MHz to 20 MHz	R/W
b6	MOSEL	Main Clock Oscillator Switch	0: Resonator 1: External oscillator input	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

MODRV21 Bit (Main Clock Oscillator Drive Capability Switch)

These bits select the drive capability of the main clock oscillator.

MOSEL Bit (Main Clock Oscillator Switch)

This bit selects the oscillation source of the main clock oscillator.

9.2.16 Memory Wait Cycle Setting Register (MEMWAIT)

Address(es): 0008 0031h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	MEMWAIT[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	MEMWAIT[1:0]	Memory Wait Cycle Setting*1, *2	b1 b0 0 0: No wait states 0 1: Wait states (ICLK ≤ 64 MHz) 1 0: Wait states (ICLK ≤ 80 MHz) Settings other than above are prohibited.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
Note 1. Do not select the MEMWAIT[1:0] bits = 00b (no wait states) when a clock of frequency higher than 32 MHz is selected as the system clock (ICLK) by the SCKCR.ICK[3:0] or SCKCR3.CKSEL[2:0] bits. When a clock of frequency is lower than 32 MHz is selected as the ICLK, it is not necessary to set the MEMWAIT[1:0] bits to 01b (wait states (ICLK ≤ 64 MHz)).
Note 2. Do not select the MEMWAIT[1:0] bits = 01b (wait states (ICLK ≤ 64 MHz)) when a clock of frequency higher than 64 MHz is selected as the system clock (ICLK) by the SCKCR.ICK[3:0] or SCKCR3.CKSEL[2:0] bits. When a clock of frequency is lower than 64 MHz is selected as the ICLK, it is not necessary to set the MEMWAIT[1:0] bits to 10b (wait states (ICLK ≤ 80 MHz)).

The MEMWAIT register is used to control the wait cycle of the ROM. If a clock with a frequency higher than 32 MHz is set as the system clock (ICLK), set this register to insert a wait at times of ROM access. When ROM cache is operating and an instruction hits the cache so that the data are supplied from the ROM cache, the wait according to the setting of the register is not inserted. The ROM cache is disabled after release from the reset state. For setting the operation of the ROM cache, refer to section 36.4.24, ROM Cache Enable Register (ROMCE).

MEMWAIT[1:0] Bits (Memory Wait Cycle Setting)

These bits are used to set the wait cycle of the ROM.
These bits are set to “no wait states” immediately after a reset.
When selecting a clock of frequency higher than 32 MHz as the system clock (ICLK), set the MEMWAIT[1:0] bits to 01b (wait states (ICLK ≤ 64 MHz)) or 10b (wait states (ICLK ≤ 80 MHz)).
When setting the MEMWAIT[1:0] bits to 01b (wait states (ICLK ≤ 64 MHz)) or 10b (wait states (ICLK ≤ 80 MHz)), make sure that high-speed operating mode is selected. After the MEMWAIT[1:0] bits are set to the set value, change the system clock to a clock of frequency higher than 32 MHz.
When setting the MEMWAIT[1:0] bits to 00b (no wait states), make sure that the frequency of the system clock (ICLK) is 32 MHz or lower. When changing the operating power control state, make sure that the value of the MEMWAIT[1:0] bits are changed to 00b.
Table 9.3 lists the restrictions on setting the MEMWAIT[1:0] bits, and Figure 9.2 and Figure 9.3 show the procedure for changing the MEMWAIT[1:0] bits.

Table 9.3 Restrictions on Setting the MEMWAIT[1:0] Bits

	Operating Power Control State			
	High-Speed Operating Mode			Middle-Speed Operating Mode
MEMWAIT[1:0] Bits	ICLK ≤ 32 MHz	32 MHz < ICLK ≤ 64 MHz	64 MHz < ICLK ≤ 80 MHz	
00b	Can be set	Cannot be set	Cannot be set	Can be set
01b	Can be set	Can be set	Cannot be set	Cannot be set
10b	Can be set	Can be set	Can be set	Cannot be set
Other than above	Cannot be set			

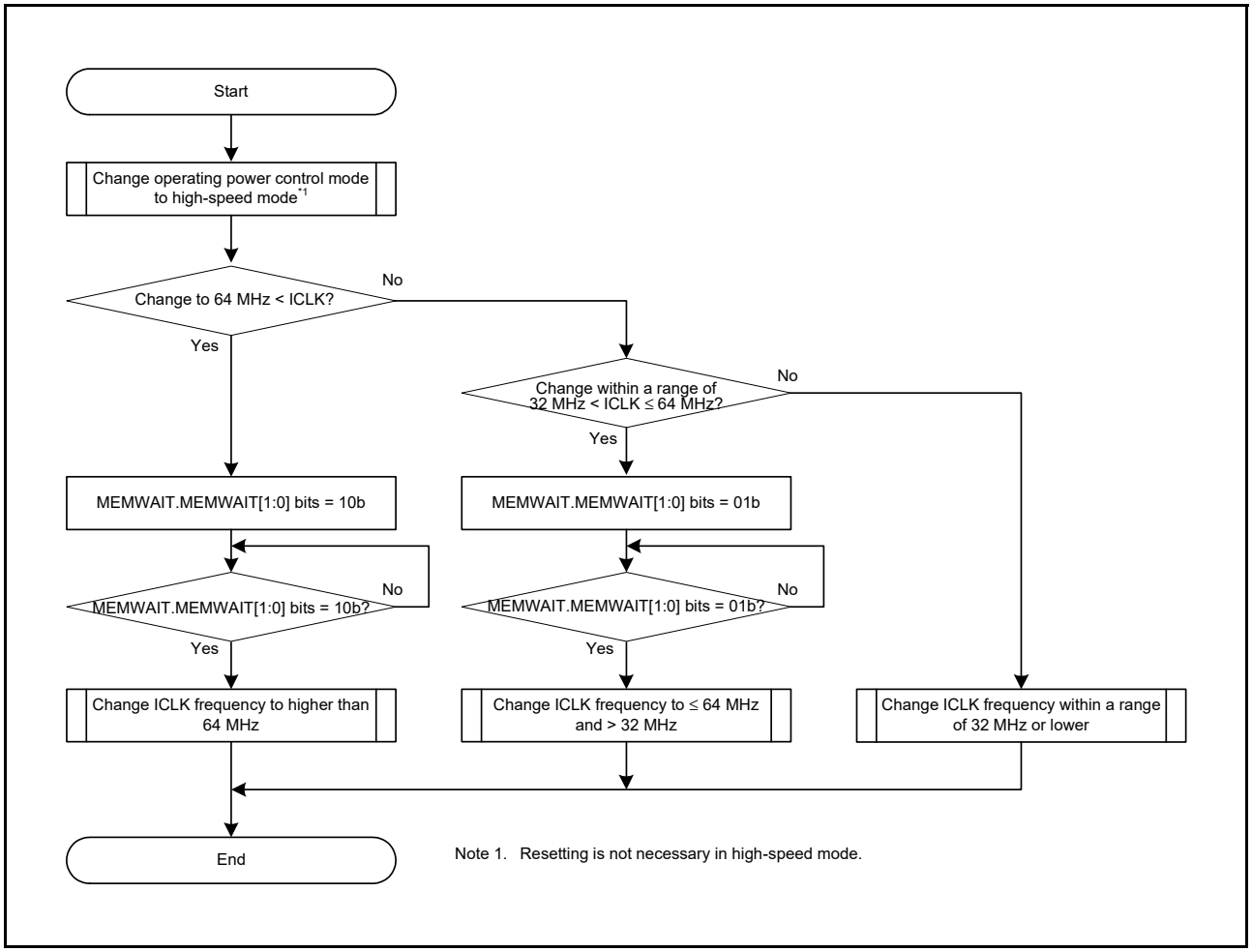


Figure 9.2 Example of Setting Procedure When Changing the Current ICLK Frequency to a Higher Frequency

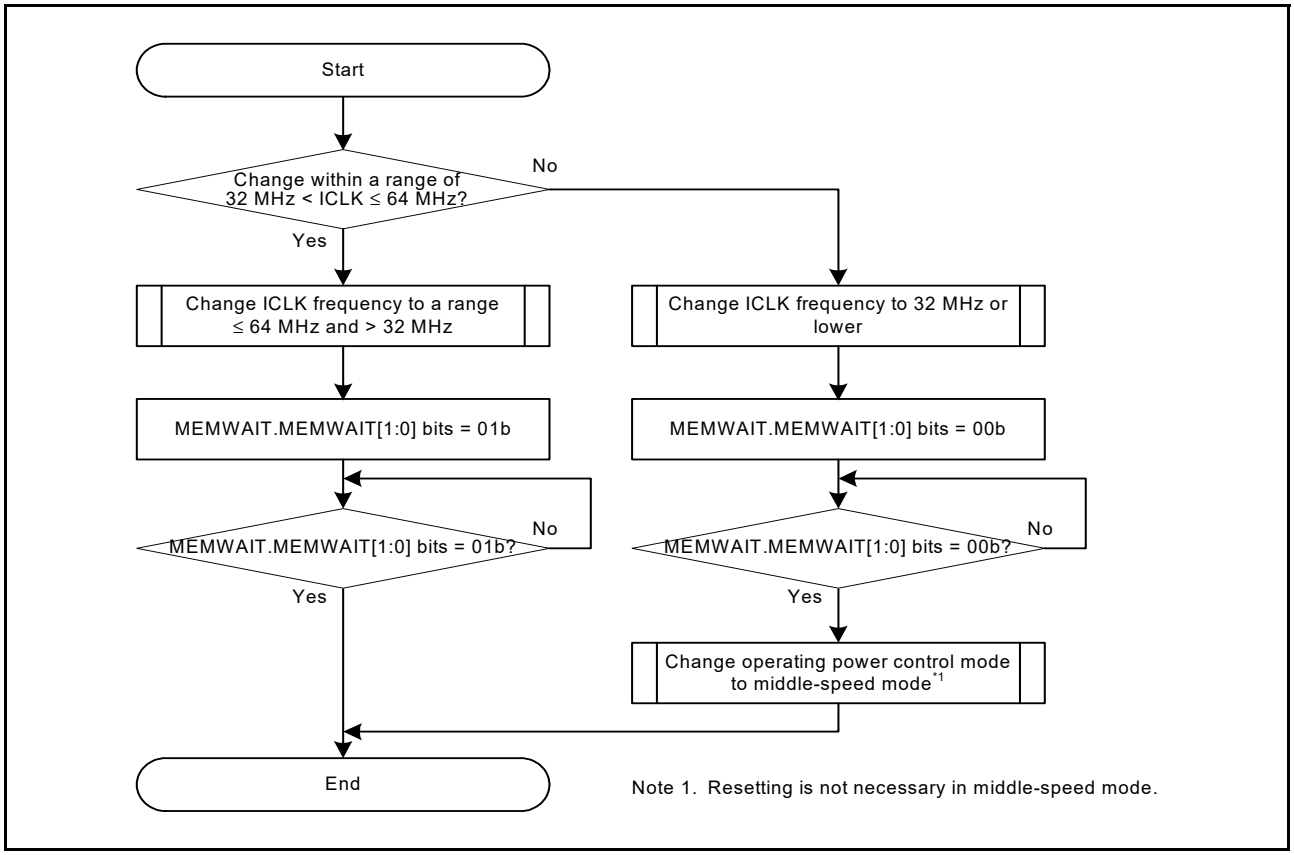


Figure 9.3 Example of Setting Procedure When Changing the Current ICLK Frequency to a Lower Frequency

9.3 Main Clock Oscillator

There are two ways of supplying the clock signal from the main clock oscillator: connecting an oscillator or the input of an external clock signal.

9.3.1 Connecting a Crystal

Figure 9.4 shows an example of connecting a crystal.
A damping resistor (R_d) should be added, if necessary. Since the resistor values vary depending on the resonator and the oscillation drive capability, use values recommended by the resonator manufacturer. If use of an external feedback resistor (R_f) is directed by the resonator manufacturer, insert an R_f between EXTAL and XTAL by following the instruction.
When connecting a resonator to supply the clock, the frequency of the resonator should be in the frequency range of the resonator for the main clock oscillator described in Table 9.1.

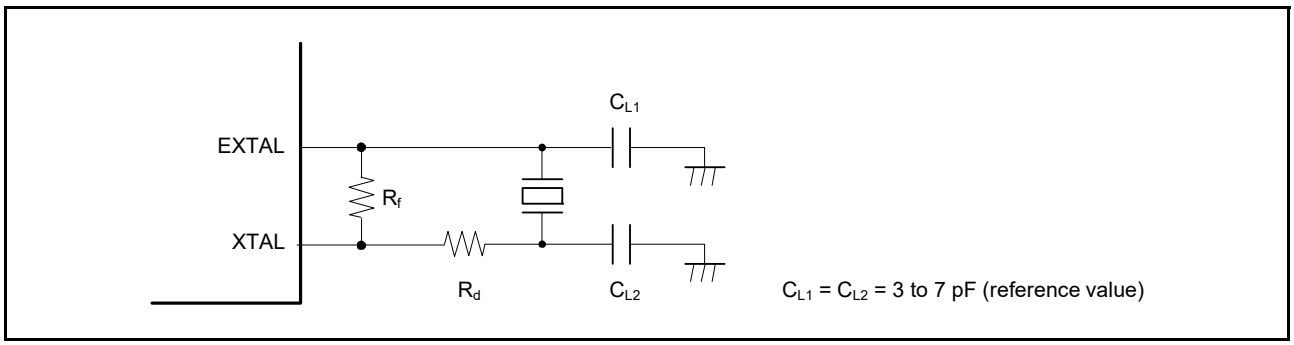


Figure 9.4 Example of Crystal Connection

Table 9.4 Damping Resistance (Reference Values)

Frequency (MHz)	2	8	16	20
R_d (Ω)	0	0	0	0

Figure 9.5 shows an equivalent circuit of the crystal. Use a crystal that has the characteristics shown in Table 9.5 as a reference.

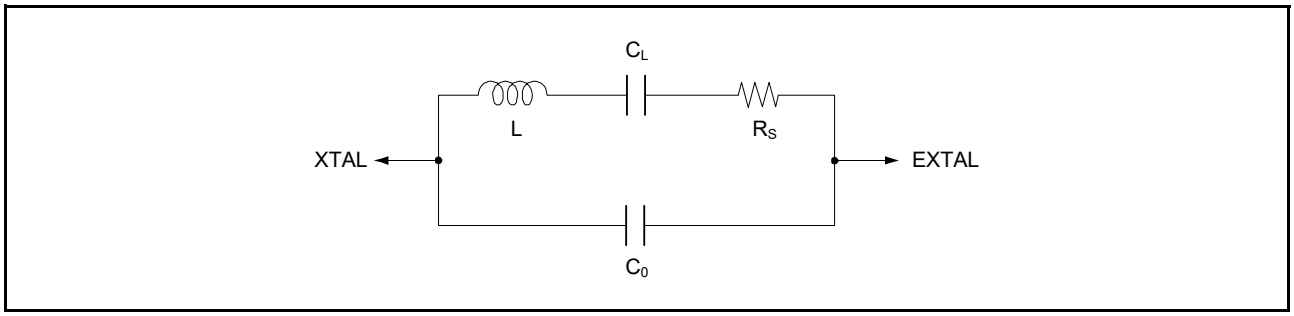


Figure 9.5 Equivalent Circuit of Crystal

Table 9.5 Crystal Characteristics (Reference Values)

Frequency (MHz)	8	12	16
R_S max (Ω)	200	120	56
C_0 max (pF)	1.3	1.3	1.4

9.3.2 External Clock Input

Figure 9.6 shows connection of an external clock. Set the MOFCR.MOSEL bit to 1 if operation is to be driven by an external clock. In this case, the XTAL pin will be in the Hi-Z state.

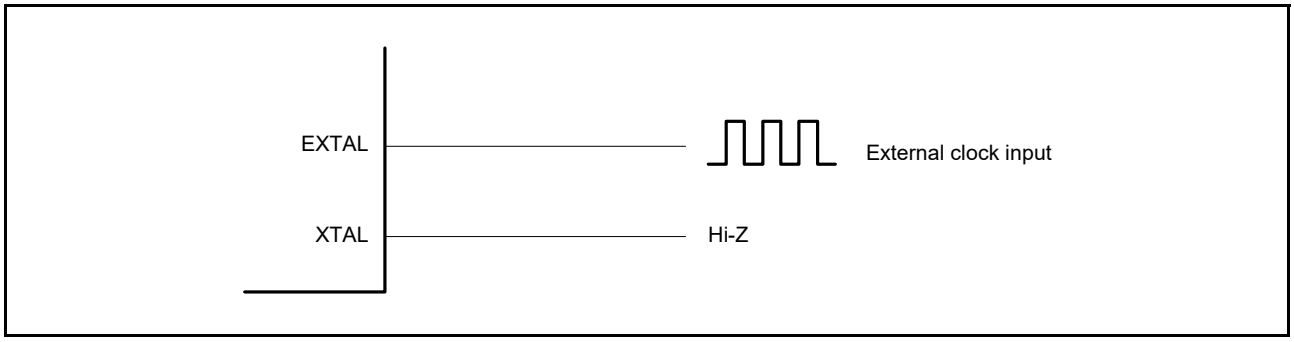


Figure 9.6 Connection Example of External Clock

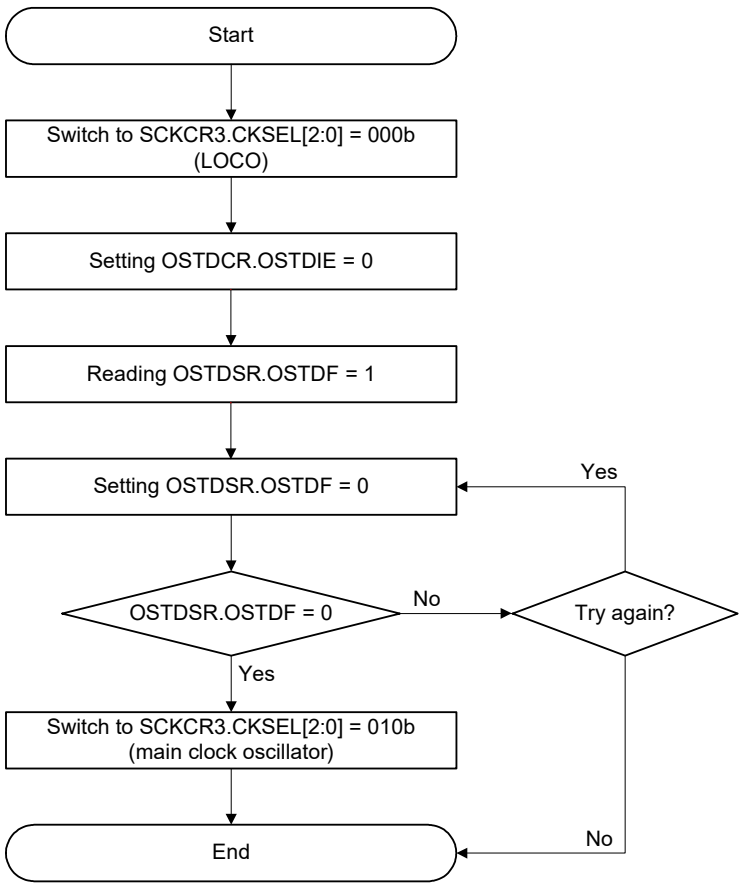
9.3.3 Notes on the External Clock Input

The frequency of the external clock input can only be changed while the main clock oscillator is stopped. Do not change the frequency of the external clock input while the setting of the main clock oscillator stop bit (MOSCCR.MOSTP) is 0 (main clock oscillator is operating).

9.4 Oscillation Stop Detection Function

9.4.1 Oscillation Stop Detection and Operation after Detection

The oscillation stop detection function is used to detect the main clock oscillator stop and to supply LOCO clock pulses from the low-speed on-chip oscillator as the system clock source instead of the main clock.
When the HOCO is selected as the clock source for the PLL and the PLL clock is selected as the system clock, the system clock is not switched to the LOCO even if stopping of the main clock is detected.
An oscillation stop detection interrupt request can be generated when an oscillation stop is detected. In addition, the MTU and GPT output can forcedly be stopped on the detection. For details, refer to section 20, Multi-Function Timer Pulse Unit 3 (MTU3d), section 21, Port Output Enable 3 (POE3A), and section 22, General PWM Timer (GPTB).
In the MCU, the main clock oscillation stop is detected when the input clock remains to be 0 or 1 for a certain period, for example, due to a malfunction of the main clock oscillator (refer to section 37, Electrical Characteristics).
When an oscillation stop is detected, the main clock selected by the clock source select bits (SCKCR3.CKSEL[2:0]) is switched to the LOCO clock by the corresponding selectors in the former stage. Therefore, if an oscillation stop is detected with the main clock selected as the system clock source, the system clock source is switched to the LOCO clock without a change of CKSEL[2:0].
If an oscillation stop is detected while the PLL clock is selected by the clock source select bits (SCKCR3.CKSEL[2:0]) in system clock control register 3, the SCKCR3.CKSEL[2:0] bit value does not change and the PLL clock remains the system clock source. However, the frequency becomes a free-running oscillation frequency.
Switching between the main clock and LOCO clock is controlled by the oscillation stop detection flag (OSTDSR.OSTDF). The clock source is switched to the LOCO clock when the OSTDF flag is 1, and is switched to the main clock again when the OSTDF flag is set to 0. At this time, if the main clock or PLL clock is selected with the CKSEL[2:0] bits, the OSTDF flag cannot be set to 0. To switch the clock source to the main clock or PLL clock again after the oscillation stop detection, set the CKSEL[2:0] bits to a clock source other than the main clock or PLL clock and set the OSTDF flag to 0. After that, check that the OSTDF flag is not 1, and then set the CKSEL[2:0] bits to the main clock or PLL clock after the specified oscillation stabilization time has elapsed.
After a reset is released, the main clock oscillator is stopped and the oscillation stop detection function is disabled. To enable the oscillation stop detection function, activate the main clock oscillator and write 1 to the oscillation stop detection function enable bit (OSTDCR.OSTDE) after a specified oscillation stabilization time has elapsed.
The oscillation stop detection function is provided against the main clock stop by an external cause. Therefore, the oscillation stop detection function should be disabled before the main clock oscillator is stopped by the software or a transition is made to software standby mode.
When the system clock with the main clock selected as the system clock source, the CAC main clock (CACMCLK), and CAN clock (CANMCLK) are selected, these clocks are switched to the LOCO clock by the detection of oscillation stop.
The system clock (ICLK) frequency during the LOCO clock operation is specified by the LOCO oscillation frequency and the division ratio set by the system clock (ICLK) select bits (SCKCR.ICK[3:0]).
When the PLL clock is selected as the system clock source, these clocks operate at the PLL free-running frequency by the oscillation stop detection.



Note: On return from the oscillation-stopped state, the factor responsible for stopping the main clock oscillation circuit must be removed on the user system to allow the return of oscillation.

Figure 9.7 Flow of Recovery from Detection of Oscillator Stop

9.4.2 Oscillation Stop Detection Interrupts

The stop of the main clock oscillator is notified to the port output enable (POE) if the oscillation-stop detection flag (OSTDSR.OSTDF) becomes 1 while the oscillation-stop detection interrupt enable bit (OSTDCR.OSTDIE) is 1 (oscillation stop detection interrupt enabled). On accepting the notification of the oscillation stop, the POE sets the oscillation stop detection flag in input level control/status register 6 (ICSR6.OSTSTF) to 1. After the oscillation stop is detected, wait for at least 10 cycles of PCLKB before writing to this ICSR6.OSTSTF flag. When the OSTDSR.OSTDF flag requires clearing, do so setting the oscillation stop detection interrupt enable bit (OSTDCR.OSTDIE) to 0. Wait for at least two cycles of PCLKB clock before again setting the OSTDCR.OSTDIE bit to 1. According to the number of cycles for access to read a given I/O register, wait time longer than two cycles of PCLKB may have to be secured.
The oscillation stop detection interrupt is a non-maskable interrupt. Since non-maskable interrupts are disabled in the initial state after a reset release, enable the non-maskable interrupts by the software before using oscillation stop detection interrupts. For details, refer to section 14, Interrupt Controller (ICUb).
When the PLL detects an oscillation stop and is running at its own oscillation frequency, this indicates the occurrence of some system failure. An emergency measure should be taken to handle the failure.

9.5 PLL Circuit

The PLL circuit has a function to multiply the frequency from the oscillator.

9.6 Internal Clock

Clock sources of internal clock signals are the main clock, HOCO clock, LOCO clock, PLL clock, and dedicated low-speed clock for the IWDT. The internal clocks listed below are produced from these sources.

(1) Operating clock of the CPU, DTC, ROM, and RAM: System clock (ICLK)
(2) Operating clock of peripheral modules: Peripheral module clock (PCLKA, PCLKB, and PCLKD)
(3) Operating clock of the FlashIF: FlashIF clock (FCLK)
(4) Operating clock for the CAN: CAN clock (CANMCLK)
(5) Operating clock for the CAC: CAC clock (CACCLK)
(6) Operating clock for the IWDT: IWDT-dedicated low-speed clock (IWDTCLK)

Frequencies of the internal clocks are set by the combinations of the division ratios selected by the FCK[3:0], ICK[3:0], PCKA[3:0], PCKB[3:0], and PCKD[3:0] bits in the SCKCR register, the clock source selected by the SCKCR3.CKSEL[2:0] bits, the multiplier and divisor for the frequency of the PLL circuit set by the STC[5:0] and PLIDIV[1:0] bits in the PLLCR register and the HOCOCR2.HCFRQ[1:0] bits. If the value of any of these bits is changed, subsequent operation will be at the frequency determined by the new value.

9.6.1 System Clock

The system clock (ICLK) is used as the operating clock of the CPU, DTC, ROM, and RAM.
The ICLK frequency is set by using the SCKCR.ICK[3:0] bits, the SCKCR3.CKSEL[2:0] bits, the STC[5:0] and PLIDIV[1:0] bits in the PLLCR register, and the HOCOCR2.HCFRQ[1:0] bits.

9.6.2 Peripheral Module Clock

The peripheral module clocks (PCLKA, PCLKB, and PCLKD) are the operating clocks for use by peripheral modules.
The frequencies of the PCLKA, PCLKB, and PCLKD are set by using the PCKA[3:0], PCKB[3:0], and PCKD[3:0] bits in the SCKCR register, the SCKCR3.CKSEL[2:0] bits, the STC[5:0] and PLIDIV[1:0] bits in the PLLCR register, and the HOCOCR2.HCFRQ[1:0] bits.
The peripheral module clock used as the operating clock is PCLKD for S12AD, and PCLKA and PCLKB are for other modules.

9.6.3 FlashIF Clock

The FlashIF clock (FCLK) is used as the operating clock of the FlashIF.
The FCLK frequency is set by using the SCKCR.FCK[3:0] bits, the SCKCR3.CKSEL[2:0] bits, and the STC[5:0] and PLIDIV[1:0] bits in the PLLCR register, and the HOCOCR2.HCFRQ[1:0] bits.

9.6.4 CAN Clock

The CAN clock (CANMCLK) is an operating clock for the CAN module.
CANMCLK is generated by the main clock oscillator.

9.6.5 CAC Clock

The CAC clock (CACCLK) is an operating clock for the CAC module.
The CACCLK clocks include CACMCLK which is generated by the main clock oscillator, CACHCLK which is generated by the high-speed on-chip oscillator, CACLCLK which is generated by the low-speed on-chip oscillator, and CACILCLK which is generated by the IWDT-dedicated on-chip oscillator.

9.6.6 IWDT-Dedicated Clock

The IWDT-dedicated clock (IWDTCLK) is the operating clock for the IWDT.
IWDTCLK is internally generated by the IWDT-dedicated on-chip oscillator.

9.7 Usage Notes

9.7.1 Notes on Clock Generation Circuit

(1) The frequencies of the system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, and PCLKD), and FlashIF clock (FCLK) supplied to each module can be selected by the SCKCR register. Each frequency should meet the following:
Select each frequency that is within the operation guaranteed range of clock cycle time (t_{cyc}) specified in AC characteristics of electrical characteristics.
The frequencies must not exceed the ranges listed in Table 9.1.
The peripheral modules operate on the PCLKA, PCLKB, and PCLKD. Note therefore that the operating speed of modules such as the timer and SCI varies before and after the frequency is changed.

(2) The relationship of frequencies of the system clock (ICLK), peripheral module clocks A, B, and D (PCLKA, PCLKB, and PCLKD), and FlashIF clock (FCLK) must be set as follows.
ICLK:FCLK = N:1 (N is an integer)
ICLK:PCLKA, PCLKB, and PCLKD = N:1 (N is an integer)

(3) To secure the processing after the clock frequency is changed, modify the pertinent clock control register to change the frequency, and then read the value from the register, and then perform the subsequent processing.

9.7.2 Notes on Resonator

Since various resonator characteristics relate closely to the user's board design, adequate evaluation is required on the user side before use, referencing the resonator connection example shown in this section. The circuit constants for the resonator depend on the resonator to be used and the stray capacitance of the mounting circuit. Therefore, the circuit constants should be determined in full consultation with the resonator manufacturer. The voltage to be applied between the resonator pins must be within the absolute maximum rating.

9.7.3 Notes on Board Design

When using a crystal, place the resonator and its load capacitors as close to the XTAL and EXTAL pins as possible. Other signal lines should be routed away from the oscillation circuit as shown in Figure 9.8 to prevent electromagnetic induction from interfering with correct oscillation.

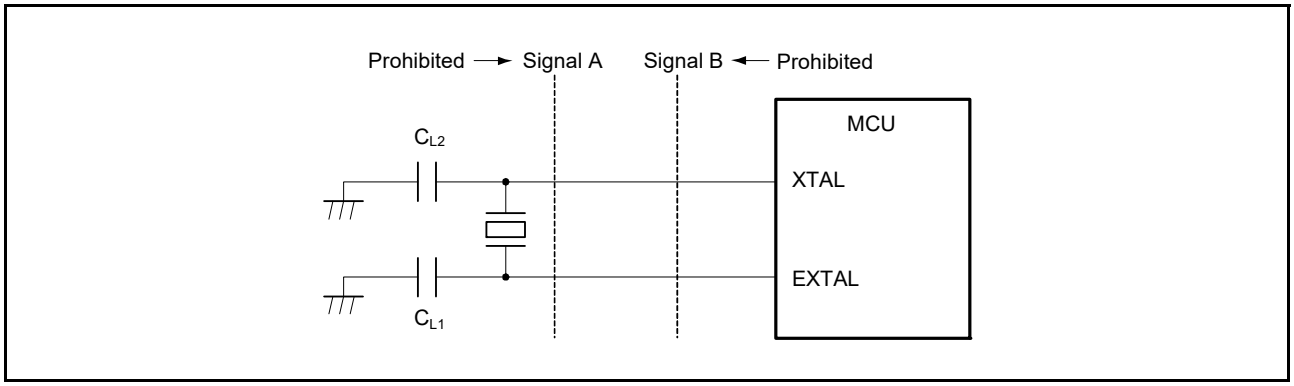


Figure 9.8 Notes on Board Design for Oscillation Circuit

10. Clock Frequency Accuracy Measurement Circuit (CAC)

10.1 Overview

The clock frequency accuracy measurement circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock to be used as a measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range.
When measurement is completed or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated.
Table 10.1 lists the specifications of the CAC and Figure 10.1 shows a block diagram of the CAC.

Table 10.1 CAC Specifications

Item	Description
Measurement target clocks	The frequency of the following clocks can be measured. • Main clock • HOCO clock • LOCO clock • IWDTCLK clock • Peripheral module clock B (PCLKB)
Measurement reference clocks	• External clock input to the CACREF pin • Main clock • HOCO clock • LOCO clock • IWDTCLK clock • Peripheral module clock B (PCLKB)
Selectable function	Digital filter function
Interrupt sources	• Measurement end interrupt • Frequency error interrupt • Overflow interrupt
Low power consumption function	Module stop state can be set.

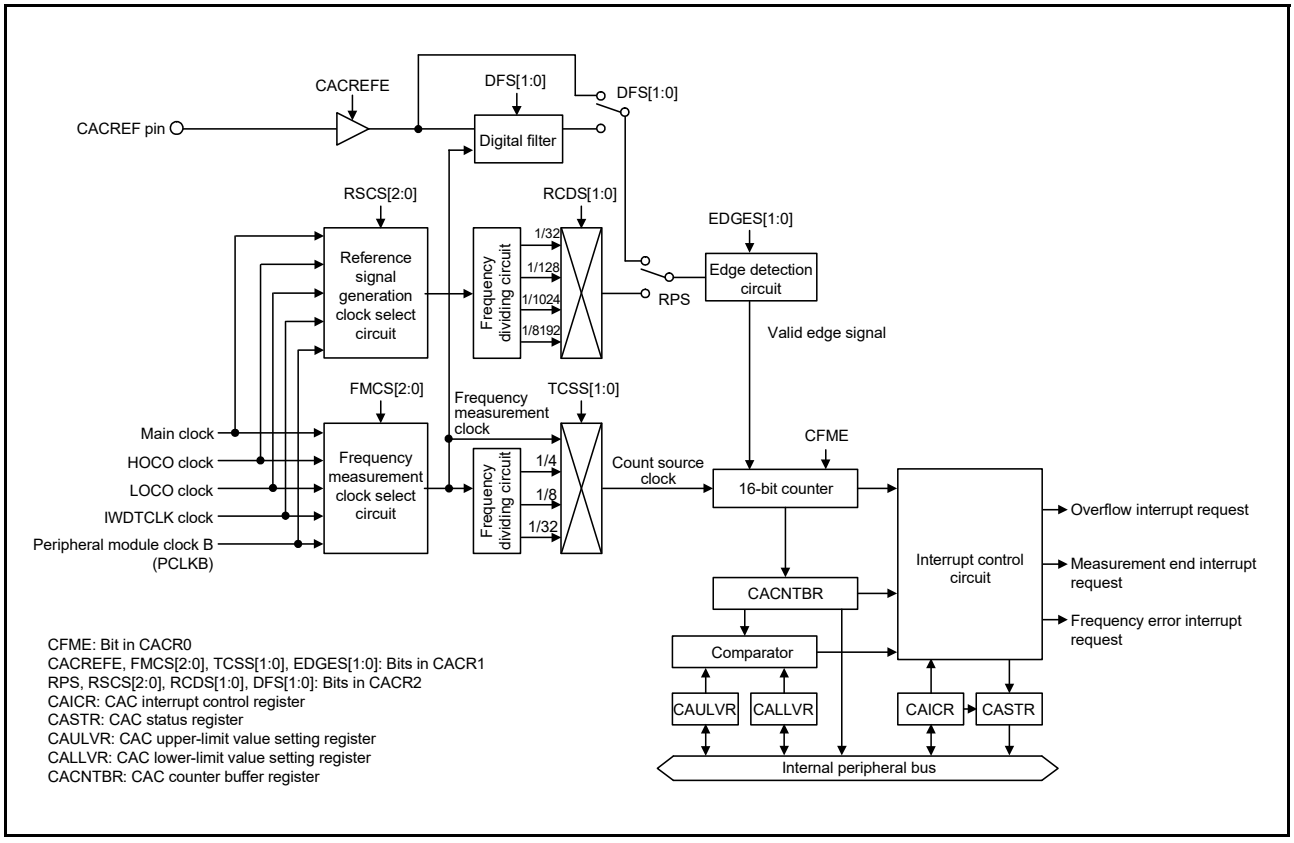


Figure 10.1 CAC Block Diagram

Table 10.2 shows the pin configuration of the CAC.

Table 10.2 Pin Configuration of CAC

Pin Name	I/O	Function
CACREF	Input	Measurement reference clock input pin

10.2 Register Descriptions

10.2.1 CAC Control Register 0 (CACR0)

Address(es): 0008 B000h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CFME
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CFME	Clock Frequency Measurement Enable	0: Clock frequency measurement is disabled. 1: Clock frequency measurement is enabled.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CFME Bit (Clock Frequency Measurement Enable)

This bit specifies whether clock frequency measurement is enabled or disabled.

When rewriting this bit, more time is required than other bits for the new value to be reflected in the register. Further write access to this bit are ignored until the current write access is reflected in the register. Read the bit to confirm that the rewrite has been reflected in the register.

10.2.2 CAC Control Register 1 (CACR1)

Address(es): 0008 B001h

	b7	b6	b5	b4	b3	b2	b1	b0
	EDGES[1:0]		TCSS[1:0]		FMCS[2:0]			CACREFE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CACREFE	CACREF Pin Input Enable	0: CACREF pin input is disabled. 1: CACREF pin input is enabled.	R/W
b3 to b1	FMCS[2:0]	Measurement Target Clock Select	b3 b1 0 0 0: Main clock 0 1 0: HOCO clock 0 1 1: LOCO clock 1 0 0: IWDTCLK clock 1 0 1: Peripheral module clock B (PCLKB) Settings other than above are prohibited.	R/W
b5, b4	TCSS[1:0]	Timer Count Clock Source Select	b5 b4 0 0: No division 0 1: ×1/4 clock 1 0: ×1/8 clock 1 1: ×1/32 clock	R/W
b7, b6	EDGES[1:0]	Valid Edge Select	b7 b6 0 0: Rising edge 0 1: Falling edge 1 0: Both rising and falling edges 1 1: Setting prohibited	R/W

Note 1. Set the CACR1 register when the CACR0.CFME bit is 0.

CACREFE Bit (CACREF Pin Input Enable)

This bit specifies whether the CACREF pin input is enabled or disabled.

FMCS[2:0]Bits (Measurement Target Clock Select)

These bits select the measurement target clock whose frequency is to be measured.

TCSS[1:0] Bits (Timer Count Clock Source Select)

These bits select the count clock source for the clock frequency accuracy measurement circuit.

EDGES[1:0]Bits (Valid Edge Select)

These bits select the valid edge for the reference signal.

10.2.3 CAC Control Register 2 (CACR2)

Address(es): 0008 B002h

	b7	b6	b5	b4	b3	b2	b1	b0
	DFS[1:0]		RCDS[1:0]		RSCS[2:0]			RPS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	RPS	Reference Signal Select	0: CACREF pin input 1: Internal clock (internally generated signal)	R/W
b3 to b1	RSCS[2:0]	Measurement Reference Clock Select	b3 b1 0 0 0: Main clock 0 1 0: HOCO clock 0 1 1: LOCO clock 1 0 0: IWDTCLK clock 1 0 1: Peripheral module clock B (PCLKB) Settings other than above are prohibited.	R/W
b5, b4	RCDS[1:0]	Measurement Reference Clock Frequency Division Ration Select	b5 b4 0 0: ×1/32 clock 0 1: ×1/128 clock 1 0: ×1/1024 clock 1 1: ×1/8192 clock	R/W
b7, b6	DFS[1:0]	Digital Filter Select	b7 b6 0 0: Digital filtering is disabled. 0 1: The sampling clock for the digital filter is the frequency measuring clock. 1 0: The sampling clock for the digital filter is the frequency measuring clock divided by 4. 1 1: The sampling clock for the digital filter is the frequency measuring clock divided by 16.	R/W

Note 1. Set the CACR2 register when the CACR0.CFME bit is 0.

RPS Bit (Reference Signal Select)

This bit selects whether to use the CACREF pin input or an internal clock (internally generated signal) as the reference signal.

RSCS[2:0]Bits (Measurement Reference Clock Select)

These bits select the clock source for generating the measurement reference clock.

RCDS[1:0]Bits (Measurement Reference Clock Frequency Division Ration Select)

These bits select the frequency division ratio of the measurement reference clock.

DFS[1:0]Bits (Digital Filter Select)

The setting of these bits enables or disables the digital filter and selects its sampling clock.

10.2.4 CAC Interrupt Request Enable Register (CAICR)

Address(es): 0008 B003h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	OVFFCL	MENDFCL	FERRFCL	—	OVFIE	MENDIE	FERRIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	FERRIE	Frequency Error Interrupt Request Enable	0: Frequency error interrupt request is disabled. 1: Frequency error interrupt request is enabled.	R/W
b1	MENDIE	Measurement End Interrupt Request Enable	0: Measurement end interrupt request is disabled. 1: Measurement end interrupt request is enabled.	R/W
b2	OVFIE	Overflow Interrupt Request Enable	0: Overflow interrupt request is disabled. 1: Overflow interrupt request is enabled.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	FERRFCL	FERRF Clear	When 1 is written to this bit, the CASTR.FERRF flag is cleared. This bit is read as 0.	R/W
b5	MENDFCL	MENDF Clear	When 1 is written to this bit, the CASTR.MENDF flag is cleared. This bit is read as 0.	R/W
b6	OVFFCL	OVFF Clear	When 1 is written to this bit, the CASTR.OVFF flag is cleared. This bit is read as 0.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

FERRIE Bit (Frequency Error Interrupt Request Enable)

This bit specifies whether the frequency error interrupt request is enabled or disabled.

MENDIE Bit (Measurement End Interrupt Request Enable)

This bit specifies whether the measurement end interrupt request is enabled or disabled.

OVFIE Bit (Overflow Interrupt Request Enable)

This bit specifies whether the overflow interrupt request is enabled or disabled.

FERRFCL Bit (FERRF Clear)

Setting this bit to 1 clears the CASTR.FERRF flag.

MENDFCL Bit (MENDF Clear)

Setting this bit to 1 clears the CASTR.MENDF flag.

OVFFCL Bit (OVFF Clear)

Setting this bit to 1 clears the CASTR.OVFF flag.

10.2.5 CAC Status Register (CASTR)

Address(es): 0008 B004h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	OVFF	MENDF	FERRF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	FERRF	Frequency Error Flag	0: The clock frequency is within the range corresponding to the settings. 1: The clock frequency has deviated beyond the range corresponding to the settings (frequency error).	R
b1	MENDF	Measurement End Flag	0: Measurement is in progress. 1: Measurement has ended.	R
b2	OVFF	Overflow Flag	0: The counter has not overflowed. 1: The counter has overflowed.	R
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

FERRF Flag (Frequency Error Flag)

This flag indicates deviation of the clock frequency from the set value (frequency error).

[Setting condition]

- The clock frequency is outside of the setting range.

[Clearing condition]

- 1 is written to the CAICR.FERRFCL bit.

MENDF Flag (Measurement End Flag)

This flag indicates the end of measurement.

[Setting condition]

- Measurement has finished.

[Clearing condition]

- 1 is written to the CAICR.MENDFCL bit.

OVFF Flag (Overflow Flag)

This flag indicates that the counter has overflowed.

[Setting condition]

- The counter has overflowed.

[Clearing condition]

- 1 is written to the CAICR.OVFFCL bit.

10.2.6 CAC Upper-Limit Value Setting Register (CAULVR)

Address(es): 0008 B006h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CAULVR is a 16-bit readable/writable register that specifies the upper-limit value of the counter used for measuring the frequency. When the frequency rises above the value specified in this register, a frequency error is detected.
Write to this register when the CACR0.CFME bit is 0.
The counter value held in CACNTBR can vary with the difference between the phases of the digital filter and edge-detection circuit on the one hand and the signal on the CACREF pin on the other, so ensure that this setting allows an adequate margin.

10.2.7 CAC Lower-Limit Value Setting Register (CALLVR)

Address(es): 0008 B008h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CALLVR is a 16-bit readable/writable register that specifies the lower-limit value of the counter used for measuring the frequency. When the frequency falls below the value specified in this register, a frequency error is detected.
Write to this register when the CACR0.CFME bit is 0.
The counter value held in CACNTBR can vary with the difference between the phases of the digital filter and edge-detection circuit on the one hand and the signal on the CACREF pin on the other, so ensure that this setting allows an adequate margin.

10.2.8 CAC Counter Buffer Register (CACNTBR)

Address(es): 0008 B00Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CACNTBR is a 16-bit read-only register that retains the counter value at the time a valid reference signal edge is input.

10.3 Operation

10.3.1 Measuring Clock Frequency

The clock frequency accuracy measurement circuit measures the clock frequency using the CACREF pin input or the internal clock as a reference. Figure 10.2 shows an operating example of the clock frequency accuracy measurement circuit.

The clock frequency accuracy measurement circuit operates as shown below when measuring the clock frequency.

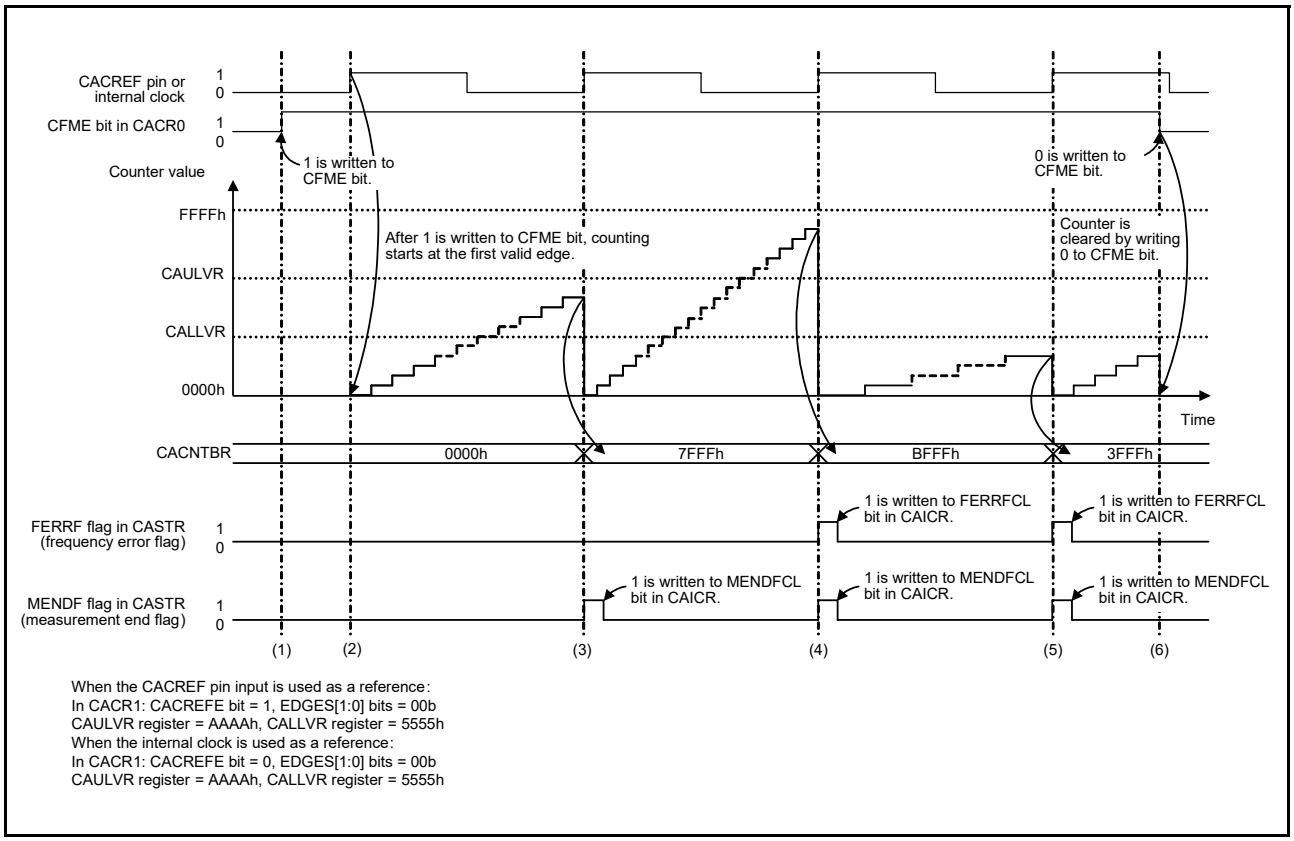


Figure 10.2 Operating Example of Clock Frequency Accuracy Measurement Circuit

(1) When the CACREF pin input is used as a reference (CACR1.CACREFE bit = 1), clock frequency measurement is enabled by writing 1 to the CACR0.CFME bit while the CACR2.RPS bit is 0 and the CACR1.CACREFE bit is 1. On the other hand, when the internal clock is used as a reference (CACR1.CACREFE bit = 0), clock frequency measurement is enabled by writing 1 to the CACR0.CFME bit while the CACR2.RPS bit is 1.

(2) When the CACREF pin input is used as a reference, the timer starts up-counting if the valid edge selected by the CACR1.EDGES[1:0] bits is input from the CACREF pin after 1 is written to the CFME bit. The valid edge is a rising edge (CACR1.EDGES[1:0] = 00b) in Figure 10.2.
When the internal clock is used as a reference, the timer starts up-counting if the valid edge selected by the CACR1.EDGES[1:0] bits is input based on the clock source selected by the CACR2.RSCS[2:0] bits after 1 is written to the CFME bit. The valid edge is a rising edge (CACR1.EDGES[1:0] = 00b) in Figure 10.2.

(3) When the next valid edge is input, the counter value is transferred in CACNTBR and compared with the values of CAULVR and CALLVR. If both CACNTBR ≤ CAULVR and CACNTBR ≥ CALLVR are satisfied, only the MENDF flag in CASTR is set to 1 because the clock frequency is correct. If the MENDIE bit in CAICR is 1, a measurement end interrupt is generated.

(4) When the next valid edge is input, the counter value is transferred in CACNTBR and compared with the values of CAULVR and CALLVR. In the case of CACNTBR > CAULVR, the FERRF flag in CASTR is set to 1 because the

clock frequency is erroneous. If the FERRIE bit in CAICR is 1, a frequency error interrupt is generated. Also, the MENDF flag in CASTR is set to 1. If the MENDIE bit in CAICR is 1, a measurement end interrupt is generated.

(5) When the next valid edge is input, the counter value is transferred in CACNTBR and compared with the values of CAULVR and CALLVR. In the case of CACNTBR < CALLVR, the FERRF flag in CASTR is set to 1 because the clock frequency is erroneous. If the FERRIE bit in CAICR is 1, a frequency error interrupt is generated. Also, the MENDF flag in CASTR is set to 1. If the MENDIE bit in CAICR is 1, a measurement end interrupt is generated.

(6) While the CFME bit in CACR0 is 1, the counter value is transferred in CACNTBR and compared with the values of CAULVR and CALLVR every time a valid edge is input. Writing 0 to the CFME bit in CACR0 clears the counter and stops up-counting.

10.3.2 Digital Filtering of Signals on the CACREF Pin

The CACREF pin has a digital filter. Levels on the target pin for sampling are conveyed to the internal circuitry after matching three consecutive times at the selected sampling interval and the same level continues to be conveyed internally until the level on the pin again matches three consecutive times.

Enabling and disabling of the digital filter and its sampling clock are selectable.

The counter value transferred in CACNTBR may be in error by up to one cycle of the sampling clock due to the difference between the phases of the digital filter and the signal input to the CACREF pin.

When a frequency dividing clock is selected as a count source clock, the counter value error is obtained by the following formula:

Counter value error = (One cycle of the count source clock) / (One cycle of the sampling clock)

10.4 Interrupt Requests

The CAC generates three types of interrupt request: frequency error interrupt, measurement end interrupt, and overflow interrupt. When an interrupt source is generated, the corresponding status flag becomes 1. Table 10.3 lists details on the interrupt requests of the clock frequency accuracy measurement circuit.

Table 10.3 Interrupt Requests of Clock Frequency Accuracy Measurement Circuit

Interrupt Request	Interrupt Enable Bit	Status Flag	Interrupt Source
Frequency error interrupt	CAICR.FERRIE	CASTR.FERRF	The result of comparing CACNTBR to CAULVR and CALLVR is either CACNTBR > CAULVR or CACNTBR < CALLVR.
Measurement end interrupt	CAICR.MENDIE	CASTR.MENDF	A valid edge is input from the CACREF pin. Note however that a measurement end interrupt does not occur at the first valid edge after writing 1 to the CACR0.CFME bit.
Overflow interrupt	CAICR.OVFIE	CASTR.OVFF	The counter has overflowed.

10.5 Usage Notes

10.5.1 Module Stop Function Setting

CAC operation can be disabled or enabled using module stop control register C (MSTPCRC). The initial setting is for the CAC to be halted. Register access is enabled by releasing the module stop state. For details, refer to section 11, Low Power Consumption.

11. Low Power Consumption

11.1 Overview

This MCU has several functions for reducing power consumption, by setting clock dividers, stopping modules, changing to low power consumption mode in normal operation, and changing to operating power control mode.
Table 11.1 lists the specifications of low power consumption functions, and Table 11.2 lists the conditions to change to low power consumption modes, states of the CPU and peripheral modules, and the method for exiting each mode.
After a reset, this MCU returns to normal mode, but modules except the DTC, and RAM are stopped.

Table 11.1 Specifications of Low Power Consumption Functions

Item	Specification
Clock divider functions	The frequency division ratio can be set independently for the system clock (ICLK), high speed peripheral module clock (PCLKA), peripheral module clock (PCLKB), S12AD clock (PCLKD), and FlashIF clock (FCLK).*1
Module stop function	Each peripheral module can be stopped independently by the module stop control register.
Function for transition to low power consumption mode	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.
Low power consumption modes	• Sleep mode • Deep sleep mode • Software standby mode
Operating power control modes	• Power consumption can be reduced in normal operation, sleep mode, and deep sleep mode by selecting an appropriate operating power control mode according to the operating frequency and operating voltage. • Two operating power control modes are available High-speed operating mode Middle-speed operating mode

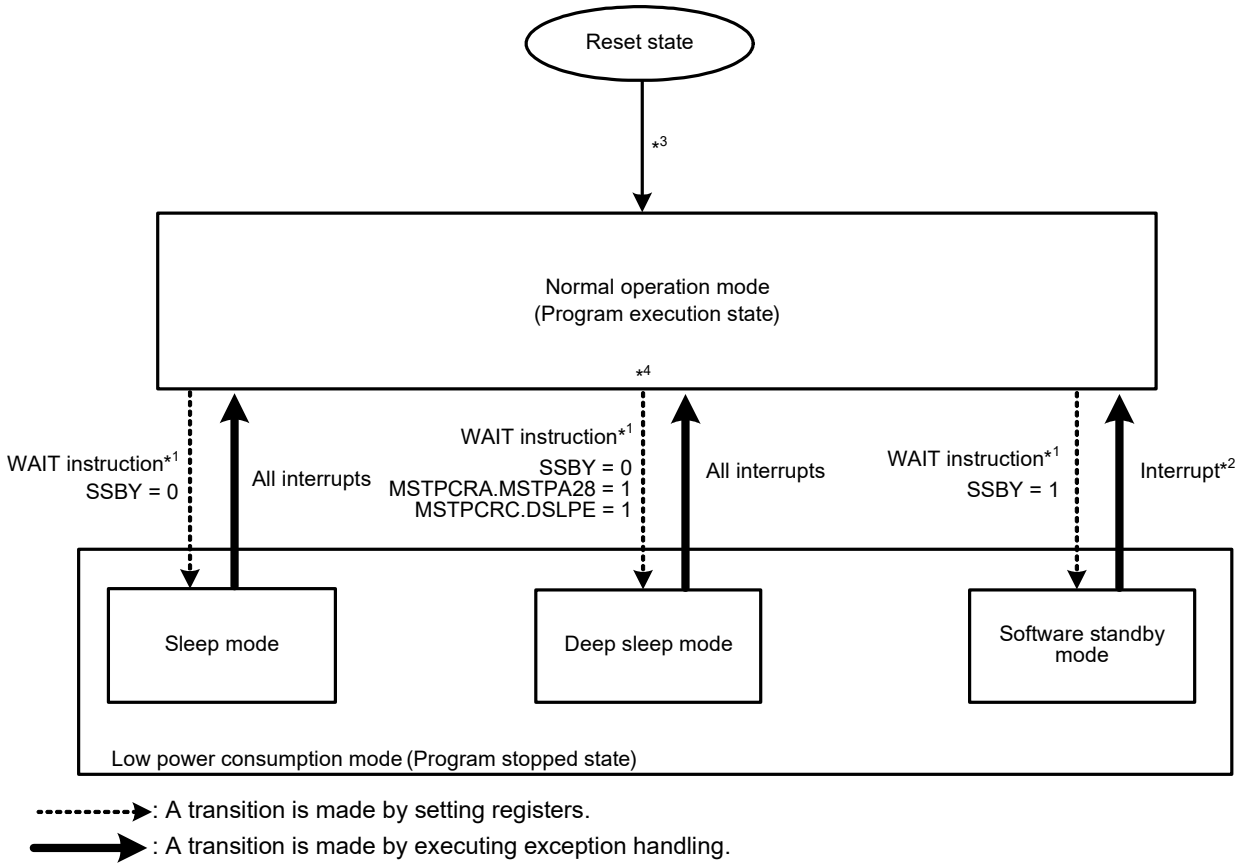
Note 1. For details, refer to section 9, Clock Generation Circuit.

Table 11.2 Operating Conditions of Each Power Consumption Mode

	Sleep Mode	Deep Sleep Mode	Software Standby Mode
Entry trigger	Control register + instruction	Control register + instruction	Control register + instruction
Exit trigger	Interrupt	Interrupt	Interrupt*1
After exiting from each mode, CPU begins from*2	Interrupt handling	Interrupt handling	Interrupt handling
Main clock oscillator	Operating possible	Operating possible	Stopped
High-speed on-chip oscillator	Operating possible	Operating possible	Stopped
Low-speed on-chip oscillator	Operating possible	Operating possible	Stopped
IWDT-dedicated on-chip oscillator	Operating possible*3	Operating possible*3	Operating possible*3
PLL	Operating possible	Operating possible	Stopped
CPU	Stopped (Retained)	Stopped (Retained)	Stopped (Retained)
RAM0 (0000 0000h to 0000 7FFFh)	Operating possible (Retained)	Stopped (Retained)	Stopped (Retained)
DTC	Operating possible*5	Stopped (Retained)	Stopped (Retained)
Flash memory	Operating	Stopped (Retained)	Stopped (Retained)
Independent watchdog timer (IWDT)	Operating possible*3	Operating possible*3	Operating possible*3
Voltage detection circuit (LVD)	Operating possible	Operating possible	Operating possible
Power-on reset circuit	Operating	Operating	Operating
Peripheral modules	Operating possible	Operating possible	Stopped (Retained)*4
I/O ports	Operating	Operating	Retained
Comparator C	Operating possible	Operating possible	Operating possible*6

“Operating possible” means that operating or stopped can be controlled by the register setting.
“Stopped (Retained)” means that internal register values are retained and internal operations are suspended.

Note 1. “Interrupts” here indicates an external pin interrupt (the NMI or IRQ0 to IRQ7) or any of peripheral interrupts (the IWDT, and voltage monitoring interrupts).
Note 2. This does not include a RES# pin reset, power-on reset, voltage monitoring reset, or independent watchdog-timer reset. One of these reset sources initiate transition to reset state.
Note 3. Operating or stopping is selected by setting the IWDT sleep mode count stop control bit (IWDTSLCSTP) in option function select register 0 (OFS0) in IWDT auto-start mode. In any mode other than IWDT auto-start mode, operating or stopping is selected by the setting of the sleep mode count stop control bit (SLCSTP) in the IWDT count stop control register (IWDTCSTPR).
Note 4. The peripheral logic states are retained.
Note 5. During sleep mode, do not write to the system control related registers (indicated by ‘SYSTEM’ in the Module Symbol column in Table 5.1, List of I/O Registers (Address Order).
Note 6. Using the digital filter function is prohibited. Operation for outputting the comparison result to the COMPn pin is possible.



Note 1. If an interrupt is accepted while entering low power consumption mode, the transition to the program stop state is exited and the interrupt exception handling is executed.
Note 2. “Interrupts” here indicates an external pin interrupt (the NMI or IRQ0 to IRQ7) or any of peripheral interrupts (the IWDT and voltage monitoring interrupts).
Note 3. The LOCO is the clock source following a transition from the reset state to normal mode.
Note 4. Makes a transition from sleep mode, deep sleep mode, or software standby mode to normal operating mode by an interrupt.
For deep sleep mode and software standby mode, the clock source after exiting is the same as that of the clock before entering software standby mode.

Transition to the reset state is made at any state instantly after a RES# pin reset, power on reset, voltage monitoring reset, IWDT reset, or software reset is generated.

Figure 11.1 Mode Transitions

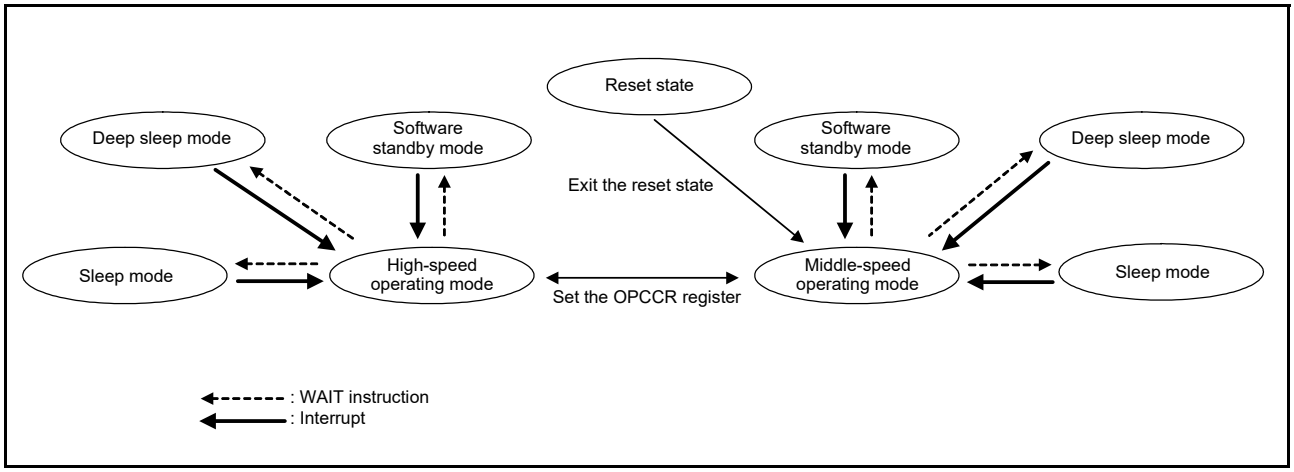


Figure 11.2 Operating Modes

- It is possible to return from sleep mode to the previous operating state used before entering sleep mode.
- After exiting the reset state, operation starts in middle-speed operating mode.

11.2 Register Descriptions

11.2.1 Standby Control Register (SBYCR)

Address(es): 0008 000Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SSBY	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b13 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b14	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b15	SSBY	Software Standby	0: Set entry to sleep mode or deep sleep mode after the WAIT instruction is executed 1: Set entry to software standby mode after the WAIT instruction is executed	R/W

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

SSBY Bit (Software Standby)

The SSBY bit specifies the transition destination after the WAIT instruction is executed.
When the SSBY bit is set to 1, the MCU enters software standby mode after execution of the WAIT instruction. When the MCU returns to normal mode after an interrupt has triggered and exits from software standby mode, the SSBY bit remains 1. The SSBY bit can be cleared by writing 0 to the SSBY bit.

When the oscillation stop detection function enable bit (OSTDCR.OSTDE) in the oscillation stop detection control register is 1, the set value of the SSBY bit is invalid. Even if the SSBY bit is 1, the MCU will enter sleep mode or deep sleep mode after execution of the WAIT instruction.

11.2.2 Module Stop Control Register A (MSTPCRA)

Address(es): 0008 0010h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	MSTPA28	—	—	—	—	MSTPA23	—	—	—	MSTPA19	—	MSTPA17	MSTPA16
Value after reset:	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MSTPA15	MSTPA14	—	—	—	—	MSTPA9	—	MSTPA7	—	MSTPA5	MSTPA4	MSTPA3	MSTPA2	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b1, b0	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b2	MSTPA2	8-bit Timer 7 and 6 (Unit 3) Module Stop	Target module: TMR7, TMR6 0: This module clock is enabled 1: This module clock is disabled	R/W
b3	MSTPA3	8-bit Timer 5 and 4 (Unit 2) Module Stop	Target module: TMR5, TMR4 0: This module clock is enabled 1: This module clock is disabled	R/W
b4	MSTPA4	8-bit Timer 3 and 2 (Unit 1) Module Stop	Target module: TMR3, TMR2 0: This module clock is enabled 1: This module clock is disabled	R/W
b5	MSTPA5	8-bit Timer 1 and 0 (Unit 0) Module Stop	Target module: TMR1, TMR0 0: This module clock is enabled 1: This module clock is disabled	R/W
b6	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b7	MSTPA7	General PWM Timer Module Stop	Target module: GPT 0: This module clock is enabled 1: This module clock is disabled	R/W
b8	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b9	MSTPA9	Multifunction Timer Pulse Unit 3 Module Stop	Target module: MTU 0: This module clock is enabled 1: This module clock is disabled	R/W
b13 to b10	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b14	MSTPA14	Compare Match Timer 1 (Unit 1) Module Stop	Target module: CMT unit 1 (CMT2, CMT3) 0: This module clock is enabled 1: This module clock is disabled	R/W
b15	MSTPA15	Compare Match Timer (Unit 0) Module Stop	Target module: CMT unit 0 (CMT0, CMT1) 0: This module clock is enabled 1: This module clock is disabled	R/W
b16	MSTPA16	12-Bit A/D Converter 1 Module Stop	Target module: S12AD1 0: This module clock is enabled 1: This module clock is disabled	R/W
b17	MSTPA17	12-Bit A/D Converter Module Stop	Target module: S12AD 0: This module clock is enabled 1: This module clock is disabled	R/W
b18	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b19	MSTPA19	8-Bit D/A Converter Module Stop	Target module: DA 0: This module clock is enabled 1: This module clock is disabled	R/W
b22 to b20	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b23	MSTPA23	12-Bit A/D Converter 2 Module Stop	Target module: S12AD2 0: This module clock is enabled 1: This module clock is disabled	R/W

Bit	Symbol	Bit Name	Description	R/W
b27 to b24	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b28	MSTPA28	Data Transfer Controller Module Stop	Target module: DTC 0: This module clock is enabled 1: This module clock is disabled	R/W
b31 to b29	—	Reserved	These bits are read as 1. The write value should be 1.	R/W

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

11.2.3 Module Stop Control Register B (MSTPCRB)

Address(es): 0008 0014h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	MSTPB30	—	—	—	MSTPB26	MSTPB25	—	MSTPB23	—	MSTPB21	—	—	—	MSTPB17	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	MSTPB10	—	—	—	MSTPB6	—	—	—	—	—	MSTPB0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b0	MSTPB0	RSCAN Module Stop*1	Target module: RSCAN 0: This module clock is enabled 1: This module clock is disabled	R/W
b5 to b1	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b6	MSTPB6	DOC Module Stop	Target module: DOC 0: This module clock is enabled 1: This module clock is disabled	R/W
b9 to b7	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b10	MSTPB10	Comparator C Module Stop	Target module: Comparator C 0: This module clock is enabled 1: This module clock is disabled	R/W
b16 to b11	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b17	MSTPB17	Serial Peripheral Interface 0 Module Stop	Target module: RSPI0 0: This module clock is enabled 1: This module clock is disabled	R/W
b20 to b18	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b21	MSTPB21	I^2C Bus Interface 0 Module Stop	Target module: RIIC0 0: This module clock is enabled 1: This module clock is disabled	R/W
b22	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b23	MSTPB23	CRC Calculator Module Stop	Target module: CRC 0: This module clock is enabled 1: This module clock is disabled	R/W
b24	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b25	MSTPB25	Serial Communication Interface 6 Module Stop	Target module: SCI6 0: This module clock is enabled 1: This module clock is disabled	R/W
b26	MSTPB26	Serial Communication Interface 5 Module Stop	Target module: SCI5 0: This module clock is enabled 1: This module clock is disabled	R/W
b29 to b27	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b30	MSTPB30	Serial Communication Interface 1 Module Stop	Target module: SCI1 0: This module clock is enabled 1: This module clock is disabled	R/W
b31	—	Reserved	This bit is read as 1. The write value should be 1.	R/W

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.
Note 1. Rewrite this bit while the oscillation of the clock to be controlled by this bit is stable. When entering software standby mode after overwriting this bit, wait 2 cycles of CANMCLK after overwriting, and execute a WAIT instruction.

11.2.4 Module Stop Control Register C (MSTPCRC)

Address(es): 0008 0018h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	DSLPE	—	—	—	MSTPC27	MSTPC26	—	MSTPC24	—	—	—	—	MSTPC19	—	—	—
Value after reset:	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MSTPC0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	MSTPC0	RAM0 Module Stop*1	Target module: RAM0 (0000 0000h to 0000 7FFFh) 0: RAM0 operating 1: RAM0 stopped	R/W
b15 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b18 to b16	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b19	MSTPC19	Clock Frequency Accuracy Measurement Circuit Module Stop*2	Target module: CAC 0: This module clock is enabled 1: This module clock is disabled	R/W
b23 to b20	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b24	MSTPC24	Serial Communication Interface 11 Module Stop	Target module: SCI11 0: This module clock is enabled 1: This module clock is disabled	R/W
b25	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b26	MSTPC26	Serial Communication Interface 9 Module Stop	Target module: SCI9 0: This module clock is enabled 1: This module clock is disabled	R/W
b27	MSTPC27	Serial Communication Interface 8 Module Stop	Target module: SCI8 0: This module clock is enabled 1: This module clock is disabled	R/W
b30 to b28	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b31	DSLPE	Deep Sleep Mode Enable	0: Deep sleep mode is disabled 1: Deep sleep mode is enabled	R/W

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

Note 1. The corresponding MSTPC0 bit should not be set to 1 during access to the RAM. The corresponding RAM should not be accessed while the MSTPC0 bit is 1.

Note 2. The MSTPC19 bit should be rewritten while the oscillation of the clock to be controlled by this bit is stable. For entering software standby mode after rewriting this bit, wait for two cycles of the slowest clock among the clocks output by the oscillators actually oscillating and execute the WAIT instruction.

DSLPE Bit (Deep Sleep Mode Enable)

The DSLPE bit enables or disables a transition to deep sleep mode.

When the CPU executes the WAIT instruction with the DSLPE bit set to 1 and the SBYCR.SSBY and MSTPCRA.MSTPA28 bits meet specified conditions, the MCU enters deep sleep mode. For details, refer to section 11.6.2, Deep Sleep Mode.

11.2.5 Operating Power Control Register (OPCCR)

Address(es): 0008 00A0h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	OPCMTSF	—	OPCM[2:0]		
Value after reset:	0	0	0	0	0	0	1	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	OPCM[2:0]	Operating Power Control Mode Select	b2 b0 0 0 0: High-speed operating mode 0 1 0: Middle-speed operating mode Settings other than above are prohibited.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	OPCMTSF	Operating Power Control Mode Transition Status Flag	0: Transition completed 1: During transition	R
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

The OPCCR register is used to reduce power consumption in normal operating mode, sleep mode, and deep sleep mode. Power consumption can be reduced according to the operating frequency and operating voltage to be used by the OPCCR setting.

The OPCCR register cannot be rewritten under the following conditions:

- When the OPCCR.OPCMTSF flag is 1 (during transition)
- Time period from WAIT instruction execution for a sleep mode transition, until exit from sleep mode to normal operation
- Time period from WAIT instruction execution for a deep sleep mode transition, until exit from deep sleep mode to normal operation

The OPCCR register cannot be rewritten while the flash memory is being programmed or erased (P/E).
For the procedures of changing operating power control modes, refer to Function in section 11.5, Function for Lower Operating Power Consumption.
During sleep mode or mode transitions, do not write to the registers related to system control (indicated by 'SYSTEM' in the Module Symbol column in Table 5.1, List of I/O Registers (Address Order)).

OPCM[2:0] Bits (Operating Power Control Mode Select)

The OPCM[2:0] bits select operating power control mode in normal operating mode, sleep mode, and deep sleep mode. Table 11.3 shows the relationship between operating power control modes, the OPCM[2:0] bit settings, and the operating frequency and voltage ranges.

OPCMTSF Flag (Operating Power Control Mode Transition Status Flag)

This flag indicates the switching control state during and after operating power mode transition.
This flag becomes 1 when the value of the OPCM[2:0] bits is rewritten, and 0 when mode transition is completed. Read this flag and confirm that it is 0 before proceeding to the next processing. Only rewrite the OPCM[2:0] bits when this flag is 0.

Table 11.3 Operating Frequency and Voltage Ranges in Operating Power Control Modes

Operating Power Control Mode	OPCM [2:0] Bits	Operating Voltage Range	Operating Frequency Range					
			Flash Memory Read Frequency					Flash Memory Programming/ Erasure Frequency
			ICLK	FCLK	PCLKD	PCLKB	PCLKA	FCLK
High-speed operating mode	000b	2.7 to 5.5 V	Up to 80 MHz	Up to 32 MHz	Up to 40 MHz	Up to 40 MHz	Up to 80 MHz	1 to 32 MHz
Middle-speed operating mode	010b	2.7 to 5.5 V	Up to 12 MHz	Up to 12 MHz	Up to 12 MHz	Up to 12 MHz	Up to 12 MHz	1 to 12 MHz

Note: When using the FCLK at lower than 4 MHz during programming or erasing the flash memory, the frequency can be set to 1, 2, or 3 MHz.

Each operating power control mode is described below.

- High-Speed Operating Mode
  The maximum operating frequency during FLASH read is 80 MHz for ICLK and PCLKA; 40 MHz for PCLKB and PCLKD; 32 MHz for FCLK.
  During FLASH programming/erasure, the operating frequency range is 1 to 32 MHz.

Note: When using the FCLK at lower than 4 MHz during programming or erasing the flash memory, the frequency can be set to 1, 2, or 3 MHz.

- Middle-Speed Operating Mode
  As compared to high-speed operating mode, this mode reduces power consumption for low-speed operation.
  The maximum operating frequency during FLASH read is 12 MHz for ICLK, FCLK, PCLKA, PCLKB, and PCLKD.
  During FLASH programming/erasure, the operating frequency range is 1 to 12 MHz.
  The power consumption of this mode is lower than that of high speed mode under the same conditions.
  After a reset is canceled, operation is started from this mode.

Note: When using the FCLK at lower than 4 MHz during programming or erasing the flash memory, the frequency can be set to 1, 2, or 3 MHz.

11.3 Reducing Power Consumption by Switching Clock Signals

The clock frequency can change by setting the SCKCR.FCK[3:0], ICK[3:0], PCKA[3:0], PCKB[3:0], and PCKD[3:0] bits. The CPU, DTC, ROM, and RAM clocks can be set by the ICK[3:0] bits. The peripheral module clocks can be set by the PCKA[3:0], PCKB[3:0], and PCKD[3:0] bits.
The flash memory clock can be set by the FCK[3:0] bits.
For details, refer to section 9, Clock Generation Circuit.

11.4 Module Stop Function

The module stop function can be set for each on-chip peripheral module.
When the MSTPmi bit (m = A to C; i = 0 to 31) in MSTPCRA to MSTPCRC is set to 1, the specified module stops operating and enters the module stop state, but the CPU continues to operate independently. When the corresponding MSTPmi bit is set to 0, the module exits the module state and restarts operating at the end of the bus cycle. The internal states of modules are retained in the module stop state.
After a reset is canceled, all modules other than the DTC, and on-chip RAM are in the module stop state. Basically the registers in the module stop state cannot be read or written. However, note that data may be written to these registers if write access is made immediately after the setting of the module stop state. To avoid this, always write to the module stop registers after confirming that the last register setting is done.

11.5 Function for Lower Operating Power Consumption

By selecting an appropriate operating power control mode according to the operating frequency and operating voltage, power consumption can be reduced in normal mode, sleep mode, and deep sleep mode.

11.5.1 Setting Operating Power Control Mode

Examples of the procedures for switching operating power control modes are shown below:

(1) Switching from Normal Power Consumption Mode to Low Power Consumption Mode

- From high-speed operating mode to middle-speed operating mode

(High-speed operation in high-speed operating mode)
↓
Set the frequency of each clock to lower than the maximum operating frequency for middle-speed operating mode
↓
Confirm that the OPCCR.OPCMTSF flag is 0 (transition completed)
↓
Set the OPCCR.OPCM[2:0] bits to 010b (middle-speed operating mode)
↓
Confirm that the OPCCR.OPCMTSF flag is 0 (transition completed)
↓
(Middle-speed operation in middle-speed operating mode)

(2) Switching from Low Power Consumption Mode to Normal Power Consumption Mode

- From middle-speed operating mode to high-speed operating mode

Middle-speed operation in middle-speed operating mode
↓
Confirm that the OPCCR.OPCMTSF flag is 0 (transition completed)
↓
Set the OPCCR.OPCM[2:0] bit to 0 (high-speed operating mode)
↓
Confirm that the OPCCR.OPCMTSF flag is 0 (transition completed)
↓
Set the frequency of each clock to lower than the maximum operating frequency for high-speed operating mode
↓
High-speed operation in high-speed operating mode

11.6 Low Power Consumption Modes

11.6.1 Sleep Mode

11.6.1.1 Entry to Sleep Mode

When the WAIT instruction is executed while the SBYCR.SSBY bit is 0, the CPU enters sleep mode. In sleep mode, the CPU stops operating but the contents of its internal registers are retained. Other peripheral functions do not stop.
Counting by the IWDT stops if a transition to sleep mode is made while the IWDT is being used in auto-start mode and the OFS0.IWDTSLCSTP bit is 1. In the same way, counting by the IWDT stops if a transition to sleep mode is made while the IWDT is being used in register start mode and the IWDTCSTPR.SLCSTP bit is 1.
Furthermore, counting by the IWDT continues if a transition to sleep mode is made while the IWDT is being used in auto-start mode and the OFS0.IWDTSLCSTP bit is 0 (counting by the IWDT continues through transitions to low power consumption modes). In the same way, counting by the IWDT continues if a transition to sleep mode is made while the IWDT is being used in register start mode and the IWDTCSTPR.SLCSTP bit is 0.
To use sleep mode, make the following settings and then execute a WAIT instruction.

(1) Set the PSW.I bit*1 of the CPU to 0.
(2) Set the interrupt request destination*2 to be used for exit from sleep mode.
(3) Set the priority*3 of the interrupt to be used for exit from sleep mode to a level higher than the setting of the PSW.IPL[3:0] bits*1 of the CPU.
(4) Set the IERm.IENj bit*3 to 1 for the interrupt.
(5) Read the I/O register that is written last and confirm that the written value has been reflected.
(6) Execute the WAIT instruction (this automatically sets the I bit*1 in the PSW of the CPU to 1).

Note 1. For details, refer to section 2, CPU.
Note 2. For details, refer to section 14.4.3, Selecting Interrupt Request Destinations.
Note 3. For details, refer to section 14, Interrupt Controller (ICUb).

11.6.1.2 Exit from Sleep Mode

Exit from sleep mode is initiated by any interrupt, a RES# pin reset, a power-on reset, a voltage monitoring reset, or a reset caused by an IWDT underflow.

- Initiated by an interrupt
  An interrupt initiates exit from sleep mode and the interrupt exception handling starts. If a maskable interrupt has been masked by the CPU (the priority level*1 of the interrupt has been set to a value lower than that of the PSW.IPL[3:0] bits*2 of the CPU), sleep mode is not exited.
- Initiated by a RES# pin reset
  When the RES# pin is driven low, the MCU enters the reset state. When the RES# pin is driven high after the reset signal is input for a predetermined time period, the CPU starts the reset exception handling.
- Initiated by a power-on reset
  A power-on reset asserts a reset to the MCU.
  When a power-on reset is negated by a rise in the supply voltage, the CPU starts the reset exception handling.
- Initiated by a voltage monitoring reset
  A voltage monitoring reset asserts a reset to the MCU.
  When a voltage monitoring reset is negated by a rise in the supply voltage, the CPU starts the reset exception handling.
- Initiated by an independent watchdog timer reset
  An internal reset generated by an IWDT underflow asserts a reset to the MCU. However, when IWDT counting is stopped in sleep mode by setting OFS0.IWDTSTRT = 0 and OFS0.IWDTSLCSTP = 1, or OFS0.IWDTSTRT = 1 and IWDTCSTPR.SLCSTP = 1, the IWDT is stopped in sleep mode and sleep mode is not exited by the independent watchdog timer reset.

Note 1. For details, refer to section 14, Interrupt Controller (ICUb).
Note 2. For details, refer to section 2, CPU.

11.6.2 Deep Sleep Mode

11.6.2.1 Entry to Deep Sleep Mode

When a WAIT instruction is executed with the MSTPCRC.DSLPE bit set to 1, the MSTPCRA.MSTPA28 bit set to 1, and the SBYCR.SSBY bit cleared to 0, a transition to deep sleep mode is made.*1
In deep sleep mode, the CPU and the DTC, ROM, and RAM clocks stop. Peripheral functions do not stop.
Counting by the IWDT stops if a transition to deep sleep mode is made while the IWDT is being used in auto-start mode and the OFS0.IWDTSLCSTP bit is 1. In the same way, counting by the IWDT stops if a transition to deep sleep mode is made while the IWDT is being used in register start mode and the IWDTCSTPR.SLCSTP bit is 1.
Furthermore, counting by the IWDT continues if a transition to deep sleep mode is made while the IWDT is being used in auto-start mode and the OFS0.IWDTSLCSTP bit is 0 (counting by the IWDT continues through transitions to low power consumption modes). In the same way, counting by the IWDT continues if a transition to deep sleep mode is made while the IWDT is being used in register start mode and the IWDTCSTPR.SLCSTP bit is 0.

To use deep sleep mode, make the following settings and then execute a WAIT instruction.

(1) Set the PSW.I bit*2 of the CPU to 0.
(2) Set the interrupt request destination*3 to be used for exit from deep sleep mode.
(3) Set the priority*4 of the interrupt to be used for exit from deep sleep mode to a level higher than the setting of the PSW.IPL[3:0] bits*2 of the CPU.
(4) Set the IERm.IENj bit*4 to 1 for the interrupt.
(5) Read the I/O register that is written last and confirm that the written value has been reflected.
(6) Execute a WAIT instruction (executing a WAIT instruction causes automatic setting of the PSW.I bit*2 of the CPU to 1).

Note 1. Transition to deep sleep mode might not be possible, depending on the operating state of the DTC. Before setting the MSTPCRA.MSTPA28 bit to 1, set the DTCST.DTCST bit of the DTC to 0 to avoid activating the DTC.
Note 2. For details, refer to section 2, CPU.
Note 3. For details, refer to section 14.4.3, Selecting Interrupt Request Destinations.
Note 4. For details, refer to section 14, Interrupt Controller (ICUb).

11.6.2.2 Exit from Deep Sleep Mode

Exit from deep sleep mode is initiated by any interrupt, a RES# pin reset, a power-on reset, a voltage monitoring reset, or a reset caused by an IWDT underflow.

- Initiated by an interrupt
  An interrupt initiates exit from deep sleep mode and the interrupt exception handling starts. If a maskable interrupt has been masked by the CPU (the priority level*1 of the interrupt has been set to a value lower than that of the PSW.IPL[3:0] bits*2 of the CPU), deep sleep mode is not exited.
- Initiated by the RES# pin reset
  When the RES# pin is driven low, the MCU enters the reset state. When the RES# pin is driven high after the reset signal is input for a predetermined time period, the CPU starts the reset exception handling.
- Initiated by a power-on reset
  A power-on reset asserts a reset to the MCU.
  When a power-on reset is negated by a rise in the supply voltage, the CPU starts the reset exception handling.
- Initiated by a voltage monitoring reset
  A voltage monitoring reset asserts a reset to the MCU.
  When a voltage monitoring reset is negated by a rise in the supply voltage, the CPU starts the reset exception handling.
- Initiated by the independent watchdog timer
  An internal reset generated by an IWDT underflow asserts a reset to the MCU. However, when IWDT counting is stopped in deep sleep mode by setting OFS0.IWDTSTRT = 0 and OFS0.IWDTSLCSTP = 1, or OFS0.IWDTSTRT = 1 and IWDTCSTPR.SLCSTP = 1, the IWDT is stopped in deep sleep mode and deep sleep mode is not exited by the independent watchdog timer reset.

Note 1. For details, refer to section 14, Interrupt Controller (ICUb).
Note 2. For details, refer to section 2, CPU.

11.6.3 Software Standby Mode

11.6.3.1 Entry to Software Standby Mode

When a WAIT instruction is executed with the SBYCR.SSBY bit set to 1, a transition to software standby mode is made. In this mode, the CPU, on-chip peripheral functions stop. However, the contents of the CPU internal registers, RAM data, the states of on-chip peripheral functions, the I/O ports are retained. Software standby mode allows significant reduction in power consumption because the oscillator stops in this mode.
Set the DTCST.DTCST bit of the DTC to 0 before executing the WAIT instruction.
Counting by the IWDT stops if a transition to software standby mode is made while the IWDT is being used in auto-start mode and the OFS0.IWDTSLCSTP bit is 1. In the same way, counting by the IWDT stops if a transition to software standby mode is made while the IWDT is being used in register start mode and the IWDTCSTPR.SLCSTP bit is 1.

Furthermore, counting by the IWDT continues if a transition to software standby mode is made while the IWDT is being used in auto-start mode and the OFS0.IWDTSLCSTP bit is 0 (counting by the IWDT continues through transitions to low power consumption modes). In the same way, counting by the IWDT continues if a transition to software standby mode is made while the IWDT is being used in register start mode and the IWDTCSTPR.SLCSTP bit is 0.
To use software standby mode, make the following settings and then execute a WAIT instruction.

(1) Set the PSW.I bit*1 of the CPU to 0.
(2) Set the interrupt request destination*2 to be used for recovery from software standby mode to the CPU.
(3) Set the priority*3 of the interrupt to be used for recovery from software standby mode to a level higher than the setting of the PSW.IPL[3:0] bits*1 of the CPU.
(4) Set the IERm.IENj bit*3 to 1 for the interrupt.
(5) Read the I/O register that is written last and confirm that the written value has been reflected.
(6) Execute a WAIT instruction (executing a WAIT instruction causes automatic setting of the PSW.I bit*1 of the CPU to 1).

Note 1. For details, refer to section 2, CPU.
Note 2. For details, refer to section 14.4.3, Selecting Interrupt Request Destinations.
Note 3. For details, refer to section 14, Interrupt Controller (ICUb).

11.6.3.2 Exit from Software Standby Mode

Exit from software standby mode is initiated by an external pin interrupt (the NMI or IRQ0 to IRQ7), peripheral function interrupts (the IWDT, and voltage monitoring), a RES# pin reset, a power-on reset, a voltage monitoring reset, or an independent watchdog timer reset. When any trigger which initiates exit from software standby mode is asserted, the oscillators which were operating before entry to software standby mode restart operation. After the oscillation of all these oscillators has been stabilized, operation returns from software standby mode.

- Initiated by an interrupt
  When an interrupt request from among the NMI, IRQ0 to IRQ7, IWDT, voltage monitoring interrupts is generated, each of the oscillators which was operating before the transition to software standby mode resumes oscillation. After the oscillation stabilization wait time of each oscillator set by the MOSCWTCR.MSTS[4:0] bits has elapsed, the MCU exits software standby mode and interrupt exception processing starts.
- Initiated by a RES# pin reset
  Clock oscillation starts when the low level is applied to the RES# pin. Clock supply for the MCU starts at the same time. Keep the level on the RES# pin low over the time required for oscillation of the clocks to become stable. Reset exception processing starts when the high level is applied to the RES# pin.
- Initiated by a power-on reset
  A power-on reset asserts a reset to the MCU.
  When a power-on reset is negated by a rise in the supply voltage, the CPU starts the reset exception handling.
- Initiated by a voltage monitoring reset
  A voltage monitoring reset asserts a reset to the MCU.
  When a voltage monitoring reset is negated by a rise in the supply voltage, the CPU starts the reset exception handling.
- Initiated by an independent watchdog timer reset
  An internal reset generated by an IWDT underflow asserts a reset to the MCU.
  Note that the independent watchdog timer is stopped in software standby mode due to the register settings (OFS0.IWDTSTRT = 0 and OFS0.IWDTSLCSTP = 1, or OFS0.IWDTSTRT = 1 and IWDTCSTPR.SLCSTP = 1) in software standby mode. In that case, exit from software standby mode by the independent watchdog timer reset cannot be done.

11.6.3.3 Example of Software Standby Mode Application

Figure 11.3 shows an example of entry to software standby mode by the falling edge of the IRQn pin, and exit from software standby mode by the rising edge of the IRQn pin.
In this example, an IRQn interrupt is accepted with the IRQCRi.IRQMD[1:0] bits of the ICU set to 01b (falling edge), and then the IRQCRi.IRQMD[1:0] bits are set to 10b (rising edge). After that, the SBYCR.SSBY bit is set to 1 and the WAIT instruction is executed. Thus entry to software standby mode is completed. After that, exit from software standby mode is initiated by the rising edge of the IRQn pin.
To exit software standby mode, settings of the interrupt controller (ICU) are also necessary. For details, refer to section 14, Interrupt Controller (ICUb).

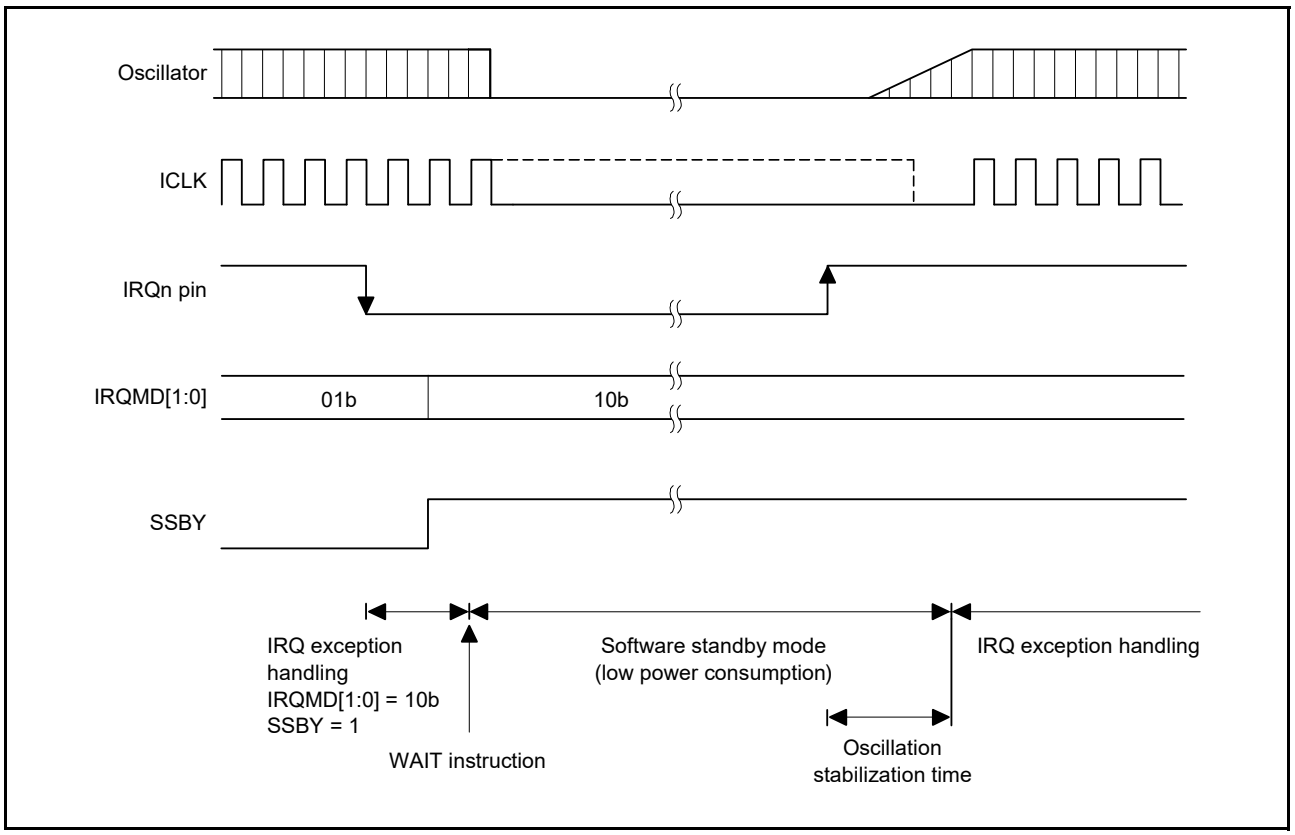


Figure 11.3 Example of Software Standby Mode Application

11.7 Usage Notes

11.7.1 I/O Port States

I/O port states are retained in software standby mode. Therefore, the supply current is not reduced if output signals are high level.

11.7.2 Module Stop State of DTC

Before setting the MSTPCRA.MSTPA28 bit to 1, set the DTCST.DTCST bit of the DTC to 0 to avoid activating the DTC.
For details, refer to section 17, Data Transfer Controller (DTCa).

11.7.3 On-Chip Peripheral Module Interrupts

Interrupts do not operate in the module stop state. Therefore, if the module stop state is made after an interrupt request is generated, a CPU interrupt source or a DTC startup source cannot be cleared. For this reason, disable interrupts before entering the module stop state.

11.7.4 Write Access to MSTPCRA, MSTPCRB, and MSTPCRC

Write accesses to MSTPCRA, MSTPCRB, and MSTPCRC should be made only by the CPU.

11.7.5 Timing of WAIT Instructions

The WAIT instruction is executed before completion of the preceding register write. The WAIT instruction being executed before the register setting is modified may cause unintended operation. To avoid this, always execute the WAIT instruction after confirming that the last register setting is done.

11.7.6 Rewrite the Register by DTC in Sleep Mode

Depending on the settings of the OFS0.IWDTSLCSTP bit and IWDTCSTPR.SLCSTP bit, the IWDT may also stop in sleep mode. To avoid this, do not set up the DTC to rewrite any registers related to the IWDT in sleep mode.

12. Register Write Protection Function

The register write protection function protects important registers from being overwritten for in case a program runs out of control. The registers to be protected are set with the protect register (PRCR).

Table 12.1 lists the association between the PRCR bits and the registers to be protected.

Table 12.1 Association between PRCR Bits and Registers to be Protected

PRCR Bit	Register to be Protected
PRC0	• Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, MOSCCR, LOCOCR, ILOCOCR, HOCOCR, HOCOCR2, OSTDCR, OSTDSR, MEMWAIT
PRC1	• Register related to the operating modes: SYSCR1 • Registers related to low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, OPCCR • Registers related to the clock generation circuit: MOFCR, MOSCWTCR • Software reset register: SWRR
PRC2	• Register related to the clock generation circuit: HOCOWTCR
PRC3	• Registers related to the LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR

12.1 Register Descriptions

12.1.1 Protect Register (PRCR)

Address(es): 0008 03FEh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PRKEY[7:0]								—	—	—	—	PRC3	PRC2	PRC1	PRC0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect Bit 0	Enables writing to the registers related to the clock generation circuit. 0: Write disabled 1: Write enabled	R/W
b1	PRC1	Protect Bit 1	Enables writing to the registers related to operating modes, low power consumption functions, the clock generation circuit, and software reset. 0: Write disabled 1: Write enabled	R/W
b2	PRC2	Protect Bit 2	Enables writing to the registers related to the clock generation circuit. 0: Write disabled 1: Write enabled	R/W
b3	PRC3	Protect Bit 3	Enables writing to the registers related to the LVD. 0: Write disabled 1: Write enabled	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	PRKEY[7:0]	PRC Key Code	These bits control permission and prohibition of writing to the PRCR register. To modify the PRCR register, write A5h to the 8 higher-order bits and the desired value to the 8 lower-order bits as a 16-bit unit.	R/W*1

Note 1. Write data is not retained.

PRCi Bits (Protect Bit i) (i = 0 to 3)

These bits enable or disable writing to the corresponding registers to be protected.

Setting the PRCi bits to 1 and 0 enable and disable writing to the corresponding registers to be protected, respectively.

13. Exception Handling

13.1 Exception Events

During execution of a program by the CPU, the occurrence of a certain event may cause execution of that program to be suspended and execution of another program to be started. Such kinds of events are called exception events.
The RXv2 CPU supports eight types of exceptions. The types of exception events are shown in Figure 13.1.
The occurrence of an exception causes the processor mode to shift to supervisor mode.

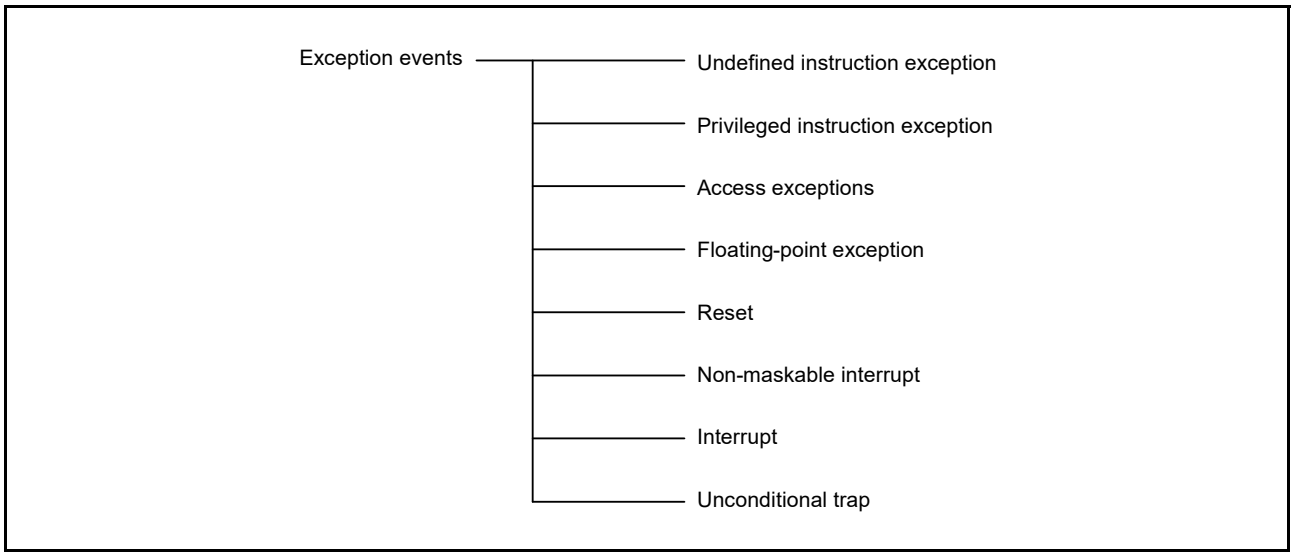


Figure 13.1 Types of Exception Events

13.1.1 Undefined Instruction Exception

An undefined instruction exception occurs when execution of an undefined instruction (an instruction not implemented) is detected.

13.1.2 Privileged Instruction Exception

A privileged instruction exception occurs when execution of a privileged instruction is detected in user mode. Privileged instructions can be executed only in supervisor mode.

13.1.3 Access Exceptions

An access exception occurs when an error is detected in access to memory by the CPU. If the memory-protection unit detects an instruction memory-protection error, an instruction-access exception occurs, and if the unit detects a data memory protection error, an operand-access exception occurs.

13.1.4 Floating-Point Exception

Floating-point exceptions include the five exception events (overflow, underflow, inexact, division-by-zero, and invalid operation) specified in the IEEE754 standard and another floating-point exception that is generated on detection of unimplemented processing. The exception handling of floating-point exceptions is prohibited when the EX, EU, EZ, EO, or EV bit in FPSW is 0.

13.1.5 Reset

A reset is generated by input of a reset signal to the CPU. This has the highest priority of any exception and is always accepted.

13.1.6 Non-Maskable Interrupt

The non-maskable interrupt is generated by input of a non-maskable interrupt signal to the CPU and is only used when a fatal fault is considered to have occurred in the system. Never use the non-maskable interrupt with an attempt to return to the program that was being executed at the time of interrupt generation after the exception handling routine is ended.

13.1.7 Interrupt

Interrupts are generated by the input of interrupt signals to the CPU. A fast interrupt can be selected as the interrupt with the highest priority. In the case of the fast interrupt, hardware pre-processing and hardware post-processing are handled fast. The priority level of the fast interrupt is 15 (the highest). The exception handling of interrupts is masked when the I bit in PSW is 0.

13.1.8 Unconditional Trap

An unconditional trap is generated when the INT or BRK instruction is executed.

13.2 Exception Handling Procedure

In the exception handling, part of the processing is handled automatically by hardware and part of it is handled by a program (exception handling routine) that has been written by the user. Figure 13.2 shows the processing procedure when an exception other than a reset is accepted.

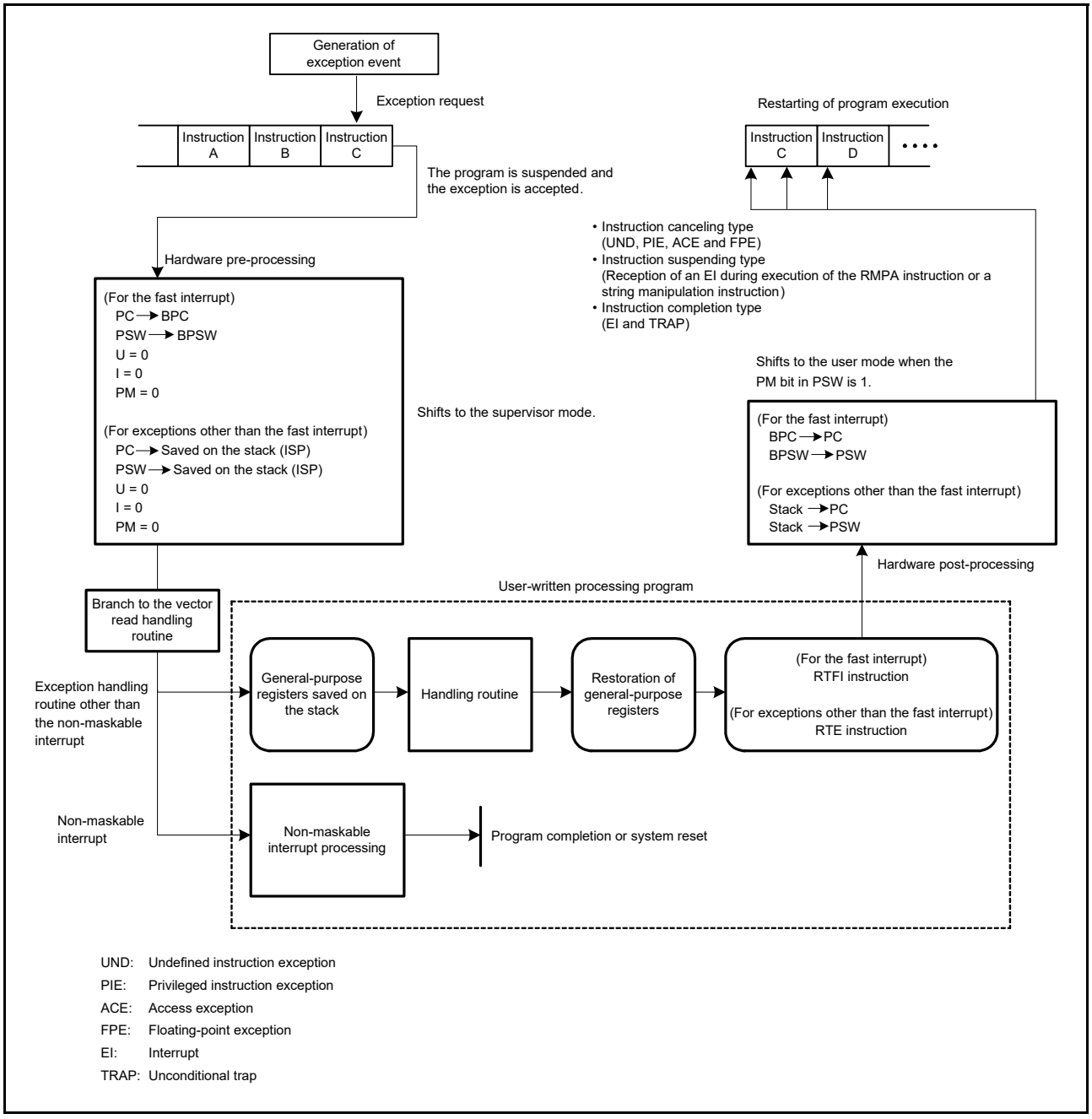


Figure 13.2 Outline of Exception Handling Procedure

When an exception is accepted, hardware processing by the RXv2 CPU is followed by access to the vector to acquire the address of the branch destination. In the vector, a vector address is allocated to each exception, and the branch destination address of the exception handling routine is written to each vector address.
Hardware pre-processing by the RXv2 CPU handles saving of the contents of the program counter (PC) and processor status word (PSW). In the case of a fast interrupt, the contents are saved in the backup PC (BPC) and the backup PSW (BPSW), respectively. In the case of exceptions other than a fast interrupt, the contents are saved in the stack area.
General purpose registers and control registers other than the PC and PSW that are to be used within the exception handling routine must be saved on the stack by a user program at the start of the exception handling routine.
On completion of processing by an exception handling routine, registers saved on the stack are restored and the RTE instruction is executed to restore execution from the exception handling routine to the original program. For return from a fast interrupt, the RTFI instruction is used instead. In the case of a non-maskable interrupt, however, finish the program or reset the system without returning to the original program.
Hardware post-processing by the RXv2 CPU handles restoration of the contents of PC and PSW. In the case of a fast interrupt, the values of BPC and BPSW are restored to PC and PSW, respectively. In the case of exceptions other than a fast interrupt, the values are restored from the stack to PC and PSW.

13.3 Acceptance of Exception Events

When an exception occurs, the CPU suspends the execution of the program and processing branches to the exception handling routine.

13.3.1 Acceptance Timing and Saved PC Value

Table 13.1 lists the timing of acceptance and the program counter (PC) value to be saved for each exception event.

Table 13.1 Acceptance Timing and Saved PC Value

Exception Event		Type of Handling	Acceptance Timing	Value Saved in BPC or on the Stack
Undefined instruction exception		Instruction canceling type	During instruction execution	PC value of the instruction that generated the exception
Privileged instruction exception		Instruction canceling type	During instruction execution	PC value of the instruction that generated the exception
Access exception		Instruction canceling type	During instruction execution	PC value of the instruction that generated the exception
Floating-point exception		Instruction canceling type	During instruction execution	PC value of the instruction that generated the exception
Reset		Instruction abandonment type	Any machine cycle	None
Non-maskable interrupt	During execution of the RMPA, SCMPU, SMOVB, SMOVF, SMOVU, SSTR, SUNTIL, and SWHILE instructions	Instruction suspending type	During instruction execution	PC value of the instruction being executed
	Other than above	Instruction completion type	At the next break between instructions	PC value of the next instruction
Interrupt	During execution of the RMPA, SCMPU, SMOVB, SMOVF, SMOVU, SSTR, SUNTIL, and SWHILE instructions	Instruction suspending type	During instruction execution	PC value of the instruction being executed
	Other than above	Instruction completion type	At the next break between instructions	PC value of the next instruction
Unconditional trap		Instruction completion type	At the next break between instructions	PC value of the next instruction

13.3.2 Vector and Site for Saving the Values in the PC and PSW

The vector for each type of exception and the site for saving the values of the program counter (PC) and processor status word (PSW) are listed in Table 13.2. The addresses where the exception vector table and interrupt vector table start must be set. For details, see section 2.6, Vector Table.

Table 13.2 Vector and Site for Saving the Values in the PC and PSW

Exception		Vector	Site for Saving the Values in the PC and PSW
Undefined instruction exception		Exception vector table (EXTB)	Stack
Privileged instruction exception		Exception vector table (EXTB)	Stack
Access exception		Exception vector table (EXTB)	Stack
Floating-point exception		Exception vector table (EXTB)	Stack
Reset		Exception vector table (EXTB)	Nowhere
Non-maskable interrupt		Exception vector table (EXTB)	Stack
Interrupt	Fast interrupt	FINTV	BPC and BPSW
	Other than above	Interrupt vector table (INTB)	Stack
Unconditional trap		Interrupt vector table (INTB)	Stack

13.4 Hardware Processing for Accepting and Returning from Exceptions

This section describes the hardware processing for accepting and returning from exceptions other than a reset.

(1) Hardware Pre-Processing for Accepting an Exception

(a) Saving PSW

- For a fast interrupt
  PSW → BPSW
- For exceptions other than a fast interrupt
  PSW → Stack

Note: The values in FPSW are not saved by hardware pre-processing. Therefore, if floating-point instructions are to be used within an exception handling routine, the user must save these values on the stack within the exception handling routine.

(b) Updating PM, U, and I Bits in PSW

I: Set to 0
U: Set to 0
PM: Set to 0

(c) Saving PC

- For a fast interrupt
  PC → BPC
- For exceptions other than a fast interrupt
  PC → Stack

(d) Setting Branch Destination Address of Exception Handling Routine in PC

Processing is shifted to the exception handling routine by acquiring the vector corresponding to the exception and then branching accordingly.

(2) Hardware Post-Processing for Execution of RTE and RTFI Instructions

(a) Restoring PSW

- For a fast interrupt
  BPSW → PSW
- For exceptions other than a fast interrupt
  Stack → PSW

(b) Restoring PC

- For a fast interrupt
  BPC → PC
- For exceptions other than a fast interrupt
  Stack → PC

13.5 Hardware Pre-Processing

The hardware pre-processing from reception of each exception request to execution of the associated exception handling routine are explained below.

13.5.1 Undefined Instruction Exception

1. The value of the processor status word (PSW) is saved on the stack (ISP).
2. The processor mode select bit (PM), the stack pointer select bit (U), and the interrupt enable bit (I) in PSW are cleared to 0.
3. The value of the program counter (PC) is saved on the stack (ISP).
4. The vector is fetched from the value of EXTB + address 0000 005Ch.
5. The fetched vector is set to the PC and processing branches to the exception handling routine.

13.5.2 Privileged Instruction Exception

1. The value in the processor status word (PSW) is saved on the stack (ISP).
2. The processor mode select bit (PM), the stack pointer select bit (U), and the interrupt enable bit (I) in PSW are cleared to 0.
3. The value of the program counter (PC) is saved on the stack (ISP).
4. The vector is fetched from the value of EXTB + address 0000 0050h.
5. The fetched vector is set to the PC and processing branches to the exception handling routine.

13.5.3 Access Exceptions

1. The value in the processor status word (PSW) is saved on the stack (ISP).
2. The processor mode select bit (PM), the stack pointer select bit (U), and the interrupt enable bit (I) in PSW are cleared to 0.
3. The value of the program counter (PC) is saved on the stack (ISP).
4. The vector is fetched from the value of EXTB + address 0000 0054h.
5. The fetched vector is set to the PC and processing branches to the exception handling routine.

13.5.4 Floating-Point Exception

1. The value in the processor status word (PSW) is saved on the stack (ISP).
2. The processor mode select bit (PM), the stack pointer select bit (U), and the interrupt enable bit (I) in PSW are cleared to 0.
3. The value of the program counter (PC) is saved on the stack (ISP).
4. The vector is fetched from the value of EXTB + address 0000 0064h.
5. The fetched vector is set to the PC and processing branches to the exception handling routine.

13.5.5 Reset

1. The control registers are initialized.
2. The vector is fetched from address FFFF FFFCh.
3. The fetched vector is set to the PC.

13.5.6 Non-Maskable Interrupt

1. The value of the processor status word (PSW) is saved on the stack (ISP).
2. The processor mode select bit (PM), the stack pointer select bit (U), and the interrupt enable bit (I) in PSW are cleared to 0.
3. If the interrupt was generated during the execution of an RMPA, SCMPU, SMOVB, SMOVF, SMOVU, SSTR, SUNTIL, or SWHILE instruction, the value of the program counter (PC) for that instruction is saved on the stack (ISP). For other instructions, the PC value of the next instruction is saved.
4. The processor interrupt priority level bits (IPL[3:0]) in PSW are set to Fh.
5. The vector is fetched from the value of EXTB + address 0000 0078h.
6. The fetched vector is set to the PC and processing branches to the exception handling routine.

13.5.7 Interrupt

1. The value of the processor status word (PSW) is saved on the stack (ISP) or, for the fast interrupt, in the backup PSW (BPSW).
2. The processor mode select bit (PM), the stack pointer select bit (U), and the interrupt enable bit (I) in PSW are cleared to 0.
3. If the interrupt was generated during the execution of an RMPA, SCMPU, SMOVB, SMOVF, SMOVU, SSTR, SUNTIL, or SWHILE instruction, the value of the program counter (PC) for that instruction is saved. For other instructions, the PC value of the next instruction is saved. Saving of the PC is in the backup PC (BPC) for fast interrupts.
4. The processor interrupt priority level bits (IPL[3:0]) in PSW indicate the interrupt priority level of the interrupt.
5. The vector for an interrupt source other than the fast interrupt is fetched from the interrupt vector table. For the fast interrupt, the address is fetched from the fast interrupt vector register (FINTV).
6. The fetched vector is set to the PC and processing branches to the exception handling routine.

13.5.8 Unconditional Trap

1. The value in the processor status word (PSW) is saved on the stack (ISP).
2. The processor mode select bit (PM), the stack pointer select bit (U), and the interrupt enable bit (I) in PSW are cleared to 0.
3. The value of the program counter (PC) for the next instruction is saved on the stack (ISP).
4. For the INT instruction, the value at the vector corresponding to the INT instruction number is fetched from the interrupt vector table.
   For the BRK instruction, the value at the vector from the start address is fetched from the interrupt vector table.
5. The fetched vector is set to the PC and processing branches to the exception handling routine.

13.6 Return from Exception Handling Routine

Executing the instruction listed in Table 13.3 at the end of the corresponding exception handling routine restores the values of the program counter (PC) and processor status word (PSW) that were saved on the stack or in the control registers (BPC and BPSW) immediately before the exception handling sequence.

Table 13.3 Return from Exception Handling Routine

Exception		Instruction for Return
Undefined instruction exception		RTE
Privileged instruction exception		RTE
Access exception		RTE
Floating-point exception		RTE
Reset		Return is impossible
Non-maskable interrupt		Prohibited
Interrupt	Fast interrupt	RTFI
	Other than above	RTE
Unconditional trap		RTE

13.7 Priority of Exception Events

The priority of exception events is listed in Table 13.4. When multiple exceptions are generated at the same time, the exception with the highest priority is accepted first.

Table 13.4 Priority of Exception Events

Priority		Exception Event
High	1	Reset
↑	2	Non-maskable interrupt
	3	Interrupt
	4	Instruction access exception
	5	Undefined instruction exception Privileged instruction exception
	6	Unconditional trap
	7	Operand access exception
Low	8	Floating-point exception

14. Interrupt Controller (ICUb)

14.1 Overview

The interrupt controller receives interrupt requests from peripheral modules and external pins, and generates an interrupt request to the CPU and a transfer request to the DTC.

Table 14.1 lists the specifications of the interrupt controller, and Figure 14.1 shows a block diagram of the interrupt controller.

Table 14.1 Specifications of Interrupt Controller

Item		Description
Interrupts	Peripheral function interrupts	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection Edge detection or level detection is fixed for each source of connected peripheral modules.
	External pin interrupts	• Interrupts from pins IRQ0 to IRQ7 • Number of sources: 8 • Interrupt detection: Low level/falling edge/rising edge/rising and falling edges One of these detection methods can be set for each source. • Digital filter function: Supported
	Software interrupt	• Interrupt generated by writing to a register • One interrupt source
	Interrupt priority	Specified by registers.
	Fast interrupt function	Faster interrupt processing of the CPU can be set only for a single interrupt source.
	DTC control	Interrupt sources can be used to start the DTC.*1
Non-maskable interrupts	NMI pin interrupt	• Interrupt from the NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter function: Supported
	Oscillation stop detection interrupt	Interrupt on detection of oscillation having stopped
	IWDT underflow/ refresh error	Interrupt on an underflow of the down counter or occurrence of a refresh error
	Voltage monitoring 1 interrupt	Voltage monitoring interrupt of voltage monitoring circuit 1 (LVD1)
	Voltage monitoring 2 interrupt	Voltage monitoring interrupt of voltage monitoring circuit 2 (LVD2)
Return from power-down modes		• Sleep mode, deep sleep mode: Return is initiated by non-maskable interrupts or any other interrupt source. • Software standby mode: Return is initiated by non-maskable interrupts, IRQ0 to IRQ7 interrupts.

Note 1. For the DTC trigger, refer to Table 14.3, Interrupt Vector Table.

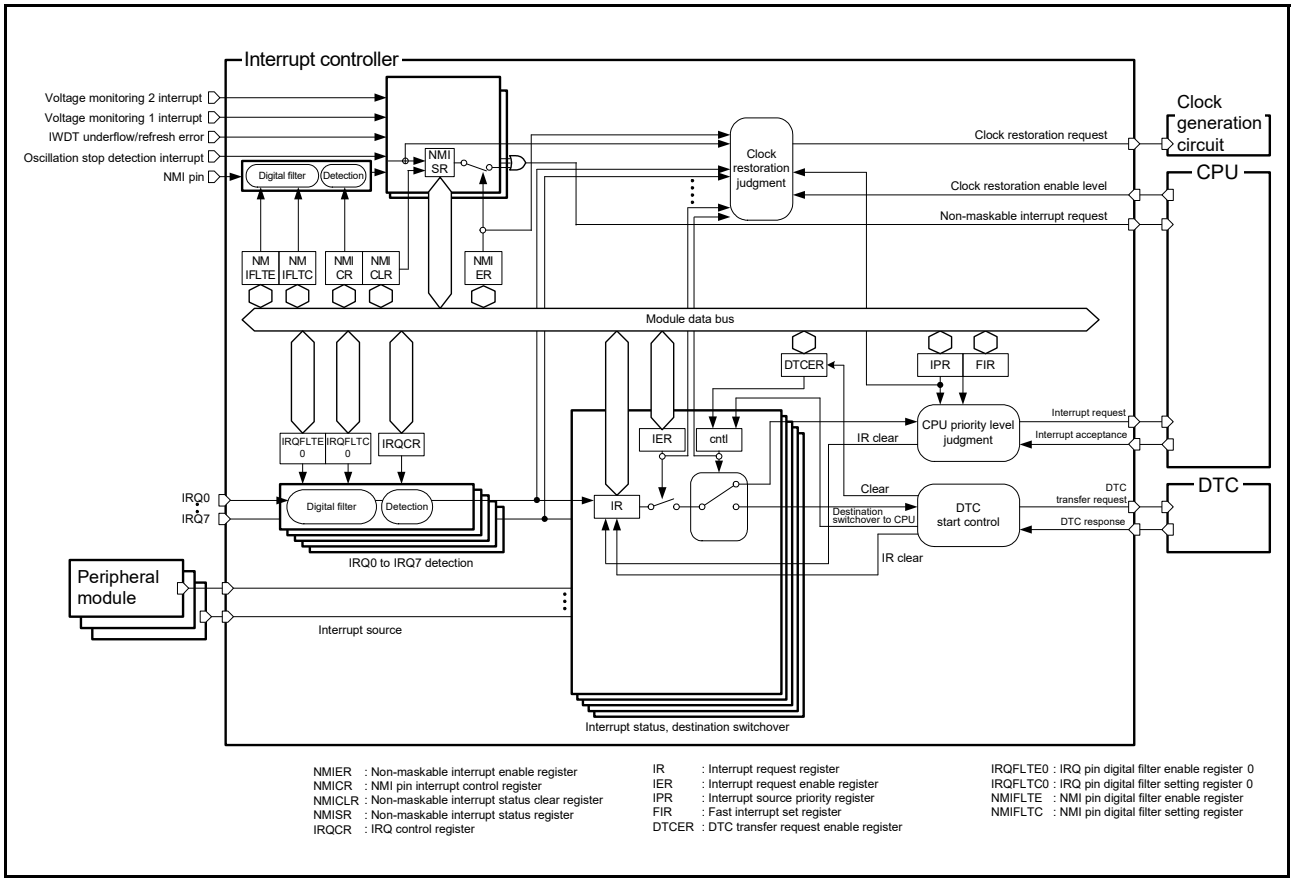


Figure 14.1 Block Diagram of Interrupt Controller

Table 14.2 lists the input/output pins of the interrupt controller.

Table 14.2 Pin Configuration of Interrupt Controller

Pin Name	I/O	Description
NMI	Input	Non-maskable interrupt request pin
IRQ0 to IRQ7	Input	External interrupt request pins

14.2 Register Descriptions

14.2.1 Interrupt Request Register n (IRn) (n = interrupt vector number)

Address(es): 0008 7010h to 0008 70FFh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	IR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	IR	Interrupt Status Flag	0: No interrupt request is generated 1: An interrupt request is generated	R/(W) *1
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. For an edge detection interrupt, only 0 can be written to this bit; do not write 1.
For a level detection interrupt, neither 0 nor 1 can be written.

IRn is provided for each interrupt source, where “n” indicates the interrupt vector number.
For the correspondence between interrupt sources and interrupt vector numbers, see Table 14.3, Interrupt Vector Table.

IR Flag (Interrupt Status Flag)

This flag is the status flag of an individual interrupt request. This flag is set to 1 when the corresponding interrupt request is generated. To detect an interrupt request, the interrupt request output should be enabled by the corresponding peripheral module interrupt enable bit.
There are two interrupt request detection methods: edge detection and level detection. For interrupts from peripheral modules, either edge detection or level detection is determined per interrupt source. For interrupts from IRQi (i = 0 to 7) pins, edge detection or level detection is selected by setting the corresponding IRQCRi.IRQMD[1:0] bits. For detection of the various interrupt sources, see Table 14.3, Interrupt Vector Table.

(1) Edge detection

[Setting condition]

- The flag is set to 1 in response to the generation of an interrupt request from the corresponding peripheral module or IRQi pin. For interrupt generation by the various peripheral modules, refer to the sections describing the modules.

[Clearing conditions]

- The flag is cleared to 0 when the interrupt request destination accepts the interrupt request.
- The IR flag is cleared to 0 by writing 0 to it. Note, however, that writing 0 to the IR flag is prohibited if the destination of the interrupt request is the DTC.

(2) Level detection

[Setting condition]

- The flag remains set to 1 while an interrupt request is being sent from the corresponding peripheral module or IRQi pin. For interrupt generation by the various peripheral modules, refer to the sections describing the modules.

[Clearing condition]

- The flag is cleared to 0 when the source of the interrupt request is cleared (it is not cleared when the interrupt request destination accepts the interrupt request). For clearing interrupts from the various peripheral modules, refer to the sections describing the modules.

When level detection has been selected for an IRQi pin, the interrupt request is withdrawn by driving the IRQi pin high.
Do not write 0 or 1 to the IR flag while level detection is selected.

14.2.2 Interrupt Request Enable Register m (IERm) (m = 02h to 1Fh)

Address(es): 0008 7202h to 0008 721Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	IEN0	Interrupt Request Enable 0	0: Interrupt request is disabled 1: Interrupt request is enabled	R/W
b1	IEN1	Interrupt Request Enable 1		R/W
b2	IEN2	Interrupt Request Enable 2		R/W
b3	IEN3	Interrupt Request Enable 3		R/W
b4	IEN4	Interrupt Request Enable 4		R/W
b5	IEN5	Interrupt Request Enable 5		R/W
b6	IEN6	Interrupt Request Enable 6		R/W
b7	IEN7	Interrupt Request Enable 7		R/W

Note: Write 0 to the bit that corresponds to the vector number for reservation. These bits are read as 0.

IENj Bit (Interrupt Request Enable j) (j = 0 to 7)

When an IENj bit is 1, the corresponding interrupt request will be output to the destination selected for the request.
When an IENj bit is 0, the corresponding interrupt request will not be output to the destination selected for the request.
The setting of an IENj bit does not affect the IRn.IR flag (n = interrupt vector number). Even if the corresponding IENj bit is 0, the IR flag value changes according to the descriptions in section 14.2.1, Interrupt Request Register n (IRn) (n = interrupt vector number).
The IERm.IENj bit is set for each request source (vector number).
For the correspondence between interrupt sources and IERm.IENj bits, see Table 14.3, Interrupt Vector Table.
For the procedure for setting IERm.IENj bits during the selection of destinations for interrupt requests, refer to section 14.4.3, Selecting Interrupt Request Destinations.

14.2.3 Interrupt Source Priority Register n (IPRn) (n = interrupt vector number)

Address(es): 0008 7300h to 0008 73FFh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	IPR[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	IPR[3:0]	Interrupt Priority Level Select	b3 b0 0 0 0 0: Level 0 (interrupt disabled)*1 0 0 0 1: Level 1 0 0 1 0: Level 2 0 0 1 1: Level 3 0 1 0 0: Level 4 0 1 0 1: Level 5 0 1 1 0: Level 6 0 1 1 1: Level 7 1 0 0 0: Level 8 1 0 0 1: Level 9 1 0 1 0: Level 10 1 0 1 1: Level 11 1 1 0 0: Level 12 1 1 0 1: Level 13 1 1 1 0: Level 14 1 1 1 1: Level 15 (highest)	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. When the interrupt is specified as a fast interrupt, it can be issued even if the priority level is level 0.

For the correspondence between interrupt sources and IPRn registers, see Table 14.3, Interrupt Vector Table.

IPR[3:0] Bits (Interrupt Priority Level Select)

These bits specify the priority level of the corresponding interrupt source.

Priority levels specified by the IPR[3:0] bits are used only to determine the priority of interrupt requests to be transferred to the CPU, and do not affect transfer requests to the DTC.

The CPU accepts only interrupt requests higher than the priority level specified by the IPL[3:0] bits in PSW, and handles accepted interrupts.

If two or more interrupt requests are generated at the same time, their priority levels are compared with the value of the IPR[3:0] bits. If interrupt requests of the same priority level are generated at the same time, an interrupt source with a smaller vector number takes precedence.

These bits should be written to while an interrupt request is disabled (IERm.IENj bit = 0 (m = 02h to 1Fh, j = 0 to 7)).

14.2.4 Fast Interrupt Set Register (FIR)

Address(es): 0008 72F0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	FIEN	—	—	—	—	—	—	—	FVCT[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	FVCT[7:0]	Fast Interrupt Vector Number	Specify the vector number of an interrupt source to be a fast interrupt.	R/W
b14 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	FIEN	Fast Interrupt Enable	0: Fast interrupt is disabled 1: Fast interrupt is enabled	R/W

The fast interrupt function based on the FIR register setting is applicable only to interrupts to the CPU. It will not affect any transfer request to the DTC.
Before writing to this register, be sure to disable interrupt requests (IERm.IENj bit = 0 (m = 02h to 1Fh, j = 0 to 7)).

FVCT[7:0] Bits (Fast Interrupt Vector Number)

The FVCT[7:0] bits specify the vector number of an interrupt source that uses the fast interrupt function.

FIEN Bit (Fast Interrupt Enable)

This bit enables the fast interrupt.
Setting this bit to 1 makes the interrupt request of the vector number specified by the FVCT[7:0] bits a fast interrupt.
When an interrupt request of the vector number specified by the FVCT[7:0] bits is generated and the interrupt request destination is the CPU while the FIEN bit is 1, the interrupt request is output to the CPU as a fast interrupt regardless of the setting of the IPRn register (n = interrupt vector number). When using the fast interrupt for returning from the software standby mode, see section 14.6.2, Return from Software Standby Mode.
If the setting of the IERm.IENj bit has disabled interrupt requests from the interrupt source with the vector number in this register, fast interrupt requests are not output to the CPU.
For settable vector numbers, see Table 14.3, Interrupt Vector Table.
Do not write any reserved vector numbers to the FVCT[7:0] bits.

For details on the fast interrupt, see section 13, Exception Handling, and section 14.4.6, Fast Interrupt.

14.2.5 Software Interrupt Generation Register (SWINTR)

Address(es): 0008 72E0h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	SWINT
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SWINT	Software Interrupt Generation	This bit is read as 0. Writing 1 issues a software interrupt request. Writing 0 to this bit has no effect.	R/(W) *1
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only 1 can be written.

SWINT Bit (Software Interrupt Generation)

When 1 is written to the SWINT bit, the interrupt request register 027 (IR027) is set to 1.

If 1 is written to the SWINT bit when the DTC transfer request enable register 027 (DTCER027) is set to 0, an interrupt to the CPU is generated.

If 1 is written to the SWINT bit when the DTC transfer request enable register 027 (DTCER027) is set to 1, a DTC transfer request is issued.

14.2.6 DTC Transfer Request Enable Register n (DTCERn) (n = interrupt vector number)

Address(es): 0008 711Bh to 0008 71FFh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DTCE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DTCE	DTC Transfer Request Enable	0: The corresponding interrupt source is not selected as the DTC trigger. 1: The corresponding interrupt source is selected as the DTC trigger.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

See Table 14.3, Interrupt Vector Table, for the interrupt sources that are selectable as the DTC trigger.

DTCE Bit (DTC Transfer Request Enable)

When the DTCE bit is set to 1, the corresponding interrupt source is selected as the DTC trigger.

[Setting condition]

- When 1 is written to the DTCE bit

[Clearing conditions]

- When the specified number of transfers is completed (for the chain transfer, the number of transfers for the last chain transfer is completed)
- When 0 is written to the DTCE bit

14.2.7 IRQ Control Register i (IRQCRi) (i = 0 to 7)

Address(es): 0008 7500h to 0008 7507h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	IRQMD[1:0]		—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b3, b2	IRQMD[1:0]	IRQ Detection Sense Select	b3 b2 0 0: Low level 0 1: Falling edge 1 0: Rising edge 1 1: Rising and falling edges	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Only change the settings of this register while the corresponding interrupt request enable bit is prohibiting the interrupt request (IENj bit in IERm (m = 02h to 1Fh, j = 0 to 7) is 0). After changing the setting, clear the IR flag in IRn before setting the interrupt enable bit. However, when the change is to the low level, the IR flag does not require clearing.

IRQMD[1:0] Bits (IRQ Detection Sense Select)

These bits select the interrupt detection sensing method of IRQi pin.

For the external pin interrupt detection setting, see section 14.4.8, External Pin Interrupts.

14.2.8 IRQ Pin Digital Filter Enable Register 0 (IRQFLTE0)

Address(es): 0008 7510h

	b7	b6	b5	b4	b3	b2	b1	b0
	FLTEN7	FLTEN6	FLTEN5	FLTEN4	FLTEN3	FLTEN2	FLTEN1	FLTEN0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	FLTEN0	IRQ0 Digital Filter Enable	0: Digital filter is disabled 1: Digital filter is enabled	R/W
b1	FLTEN1	IRQ1 Digital Filter Enable		R/W
b2	FLTEN2	IRQ2 Digital Filter Enable		R/W
b3	FLTEN3	IRQ3 Digital Filter Enable		R/W
b4	FLTEN4	IRQ4 Digital Filter Enable		R/W
b5	FLTEN5	IRQ5 Digital Filter Enable		R/W
b6	FLTEN6	IRQ6 Digital Filter Enable		R/W
b7	FLTEN7	IRQ7 Digital Filter Enable		R/W

FLTENi Bit (IRQi Digital Filter Enable) (i = 0 to 7)

This bit enables the digital filter used for the IRQi pin.

The digital filter is enabled when the FLTENi bit is 1, and disabled when the FLTENi bit is 0.

The IRQi pin level is sampled at the sampling clock cycle specified with the IRQFLTC0.FCLKSELi[1:0] bits. When the sampled level matches three times, the output level from the digital filter changes.

For details of the digital filter, see section 14.4.7, Digital Filter.

14.2.9 IRQ Pin Digital Filter Setting Register 0 (IRQFLTC0)

Address(es): 0008 7514h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	FCLKSEL7[1:0]		FCLKSEL6[1:0]		FCLKSEL5[1:0]		FCLKSEL4[1:0]		FCLKSEL3[1:0]		FCLKSEL2[1:0]		FCLKSEL1[1:0]		FCLKSEL0[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	FCLKSEL0[1:0]	IRQ0 Digital Filter Sampling Clock	0 0: PCLK 0 1: PCLK/8 1 0: PCLK/32 1 1: PCLK/64	R/W
b3, b2	FCLKSEL1[1:0]	IRQ1 Digital Filter Sampling Clock		R/W
b5, b4	FCLKSEL2[1:0]	IRQ2 Digital Filter Sampling Clock		R/W
b7, b6	FCLKSEL3[1:0]	IRQ3 Digital Filter Sampling Clock		R/W
b9, b8	FCLKSEL4[1:0]	IRQ4 Digital Filter Sampling Clock		R/W
b11, b10	FCLKSEL5[1:0]	IRQ5 Digital Filter Sampling Clock		R/W
b13, b12	FCLKSEL6[1:0]	IRQ6 Digital Filter Sampling Clock		R/W
b15, b14	FCLKSEL7[1:0]	IRQ7 Digital Filter Sampling Clock		R/W

FCLKSELi[1:0] Bits (IRQi Digital Filter Sampling Clock) (i = 0 to 7)

These bits select the cycle of the digital filter sampling clock for the IRQi pin.

The sampling clock cycle can be selected from among the PCLK (every cycle), PCLK/8 (once every eight cycles), PCLK/32 (once every 32 cycles), and PCLK/64 (once every 64 cycles).

For details of the digital filter, see section 14.4.7, Digital Filter.

14.2.10 Non-Maskable Interrupt Status Register (NMISR)

Address(es): 0008 7580h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	LVD2ST	LVD1ST	IWDTST	—	OSTST	NMIST
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	NMIST	NMI Status Flag	0: NMI pin interrupt is not requested 1: NMI pin interrupt is requested	R
b1	OSTST	Oscillation Stop Detection Interrupt Status Flag	0: Oscillation stop detection interrupt is not requested 1: Oscillation stop detection interrupt is requested	R
b2	—	Reserved	This bit is read as 0. Writing to this bit has no effect.	R
b3	IWDTST	IWDT Underflow/Refresh Error Status Flag	0: IWDT underflow/refresh error interrupt is not requested 1: IWDT underflow/refresh error interrupt is requested	R
b4	LVD1ST	Voltage Monitoring 1 Interrupt Status Flag	0: Voltage monitoring 1 interrupt is not requested 1: Voltage monitoring 1 interrupt is requested	R
b5	LVD2ST	Voltage Monitoring 2 Interrupt Status Flag	0: Voltage monitoring 2 interrupt is not requested 1: Voltage monitoring 2 interrupt is requested	R
b7, b6	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R

The NMISR register monitors the status of a non-maskable interrupt source. Writing to the NMISR register is ignored. The setting in the non-maskable interrupt enable register (NMIER) does not affect the status flags in NMISR.
Before the end of the non-maskable interrupt handler, read the NMISR register and confirm the generation status of other non-maskable interrupts. Be sure to confirm that all of the bits in the NMISR register are set to 0 before the end of the handler.

NMIST Flag (NMI Status Flag)

This flag indicates the NMI pin interrupt request.
The NMIST flag is read-only, and cleared by the NMICLR.NMICLR bit.
[Setting condition]

- When an edge specified by the NMICR.NMIMD bit is input to the NMI pin

[Clearing condition]

- When 1 is written to the NMICLR.NMICLR bit

OSTST Flag (Oscillation Stop Detection Interrupt Status Flag)

This flag indicates the oscillation stop detection interrupt request.
The OSTST flag is read-only, and cleared by the NMICLR.OSTCLR bit.
[Setting condition]

- When the oscillation stop detection interrupt is generated

[Clearing condition]

- When 1 is written to the NMICLR.OSTCLR bit

IWDTST Flag (IWDT Underflow/Refresh Error Status Flag)

This flag indicates the IWDT underflow/refresh error interrupt request.
The IWDTST flag is read-only, and cleared by the NMICLR.IWDTCLR bit.
[Setting condition]

- When the IWDT underflow/refresh error interrupt is generated while this interrupt is enabled at its source.

[Clearing condition]

- When 1 is written to the NMICLR.IWDTCLR bit

LVD1ST Flag (Voltage Monitoring 1 Interrupt Status Flag)

This flag indicates the request for voltage monitoring 1 interrupt.
The LVD1ST flag is read-only, and cleared by the NMICLR.LVD1CLR bit.

[Setting condition]

- When the voltage monitoring 1 interrupt is generated while this interrupt is enabled at its source.

[Clearing condition]

- When 1 is written to the NMICLR.LVD1CLR bit

LVD2ST Flag (Voltage Monitoring 2 Interrupt Status Flag)

This flag indicates the request for voltage monitoring 2 interrupt.
The LVD2ST flag is read-only, and cleared by the NMICLR.LVD2CLR bit.

[Setting condition]

- When the voltage monitoring 2 interrupt is generated while this interrupt is enabled at its source.

[Clearing condition]

- When 1 is written to the NMICLR.LVD2CLR bit

14.2.11 Non-Maskable Interrupt Enable Register (NMIER)

Address(es): 0008 7581h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	LVD2EN	LVD1EN	IWDTEN	—	OSTEN	NMIEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	NMIEN	NMI Pin Interrupt Enable	0: NMI pin interrupt is disabled 1: NMI pin interrupt is enabled	R/(W) *1
b1	OSTEN	Oscillation Stop Detection Interrupt Enable	0: Oscillation stop detection interrupt is disabled 1: Oscillation stop detection interrupt is enabled	R/(W) *1
b2	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b3	IWDTEN	IWDT Underflow/Refresh Error Enable	0: IWDT underflow/refresh error interrupt is disabled 1: IWDT underflow/refresh error interrupt is enabled	R/(W) *1
b4	LVD1EN	Voltage Monitoring 1 Interrupt Enable	0: Voltage monitoring 1 interrupt is disabled 1: Voltage monitoring 1 interrupt is enabled	R/(W) *1
b5	LVD2EN	Voltage Monitoring 2 Interrupt Enable	0: Voltage monitoring 2 interrupt is disabled 1: Voltage monitoring 2 interrupt is enabled	R/(W) *1
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. A 1 can be written to this bit only once, and subsequent write accesses are no longer enabled.

NMIEN Bit (NMI Pin Interrupt Enable)

This bit enables the NMI pin interrupt.

A 1 can be written to this bit only once, and subsequent write accesses are no longer enabled.

Writing 0 to this bit is disabled.

OSTEN Bit (Oscillation Stop Detection Interrupt Enable)

This bit enables the oscillation stop detection interrupt.

A 1 can be written to this bit only once, and subsequent write accesses are no longer enabled.

Writing 0 to this bit is disabled.

IWDTEN Bit (IWDT Underflow/Refresh Error Enable)

This bit enables the IWDT underflow/refresh error interrupt.

A 1 can be written to this bit only once, and subsequent write accesses are no longer enabled.

Writing 0 to this bit is disabled.

LVD1EN Bit (Voltage Monitoring 1 Interrupt Enable)

This bit enables the voltage monitoring 1 interrupt.

A 1 can be written to this bit only once, and subsequent write accesses are no longer enabled.

Writing 0 to this bit is disabled.

LVD2EN Bit (Voltage Monitoring 2 Interrupt Enable)

This bit enables the voltage monitoring 2 interrupt.

A 1 can be written to this bit only once, and subsequent write accesses are no longer enabled.

Writing 0 to this bit is disabled.

14.2.12 Non-Maskable Interrupt Status Clear Register (NMICLR)

Address(es): 0008 7582h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	LVD2CLR	LVD1CLR	IWDTCLR	—	OSTCLR	NMICLR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	NMICLR	NMI Clear	This bit is read as 0. Writing 1 to this bit clears the NMISR.NMIST flag. Writing 0 to this bit has no effect.	R/(W) *1
b1	OSTCLR	OST Clear	This bit is read as 0. Writing 1 to this bit clears the NMISR.OSTST flag. Writing 0 to this bit has no effect.	R/(W) *1
b2	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b3	IWDTCLR	IWDT Clear	This bit is read as 0. Writing 1 to this bit clears the NMISR.IWDTST flag. Writing 0 to this bit has no effect.	R/(W) *1
b4	LVD1CLR	LVD1 Clear	This bit is read as 0. Writing 1 to this bit clears the NMISR.LVD1ST flag. Writing 0 to this bit has no effect.	R/(W) *1
b5	LVD2CLR	LVD2 Clear	This bit is read as 0. Writing 1 to this bit clears the NMISR.LVD2ST flag. Writing 0 to this bit has no effect.	R/(W) *1
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only 1 can be written to this bit.

NMICLR Bit (NMI Clear)

Writing 1 to the NMICLR bit clears the NMISR.NMIST flag. This bit is read as 0.

OSTCLR Bit (OST Clear)

Writing 1 to the OSTCLR bit clears the NMISR.OSTST flag. This bit is read as 0.

IWDTCLR Bit (IWDT Clear)

Writing 1 to the IWDTCLR bit clears the NMISR.IWDTST flag. This bit is read as 0.

LVD1CLR Bit (LVD1 Clear)

Writing 1 to the LVD1CLR bit clears the NMISR.LVD1ST flag. This bit is read as 0.

LVD2CLR Bit (LVD2 Clear)

Writing 1 to the LVD2CLR bit clears the NMISR.LVD2ST flag. This bit is read as 0.

14.2.13 NMI Pin Interrupt Control Register (NMICR)

Address(es): 0008 7583h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	NMIMD	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b3	NMIMD	NMI Detection Set	0: Falling edge 1: Rising edge	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Change the setting of the NMICR register before the NMI pin interrupt is enabled (before setting the NMIER.NMIEN bit to 1).

NMIMD Bit (NMI Detection Set)

This bit specifies the detection edge of the NMI pin interrupt.

14.2.14 NMI Pin Digital Filter Enable Register (NMIFLTE)

Address(es): 0008 7590h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	NFLTEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	NFLTEN	NMI Digital Filter Enable	0: Digital filter is disabled 1: Digital filter is enabled	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

NFLTEN Bit (NMI Digital Filter Enable)

This bit enables the digital filter used for the NMI pin interrupt.

The digital filter is enabled when the NFLTEN bit is 1, and disabled when the NFLTEN bit is 0.

The NMI pin level is sampled at the sampling clock cycle specified with the NMIFLTC.NFCLKSEL[1:0] bits. When the sampled level matches three times, the output level from the digital filter changes.

For details of the digital filter, see section 14.4.7, Digital Filter.

14.2.15 NMI Pin Digital Filter Setting Register (NMIFLTC)

Address(es): 0008 7594h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	NFCLKSEL[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	NFCLKSEL[1:0]	NMI Digital Filter Sampling Clock	b1 b0 0 0: PCLK 0 1: PCLK/8 1 0: PCLK/32 1 1: PCLK/64	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

NFCLKSEL[1:0] Bits (NMI Digital Filter Sampling Clock)

These bits select the cycle of the digital filter sampling clock for the NMI pin interrupt.

The sampling clock cycle can be selected from among the PCLK (every cycle), PCLK/8 (once every eight cycles), PCLK/32 (once every 32 cycles), and PCLK/64 (once every 64 cycles).

For details of the digital filter, see section 14.4.7, Digital Filter.

14.3 Vector Table

There are two types of interrupts detected by the interrupt controller: maskable interrupts and non-maskable interrupts. When the CPU accepts an interrupt or non-maskable interrupt, it acquires a 4-byte vector address from the vector table.

14.3.1 Interrupt Vector Table

The interrupt vector table is placed in the 1024-byte range (4 bytes × 256 sources) beginning at the address specified in the interrupt table register (INTB) of the CPU. Write a value to the INTB register before enabling interrupts. The value written to the INTB register should be a multiple of 4.
Executing an INT instruction or BRK instruction leads to the generation of an unconditional trap. The same range of memory as shown in Table 14.3, Interrupt Vector Table, is used for the vectors for unconditional traps. The vector for BRK instructions is vector 0 while the vector numbers for INT instructions are specifiable as numbers in the range from 0 to 255.
Table 14.3 lists details of the interrupt vectors. Details of the headings in Table 14.3 are listed below.

Item	Description
Source of interrupt request generation	Name of the source for generation of the interrupt request
Name	Name of the interrupt
Vector no.	Vector number for the interrupt
Vector address offset	Value of the offset from the base address for the vector table
Form of interrupt detection	“Edge” or “level” as the method for detection of the interrupt
CPU interrupt	“✓” in this column indicates usability as a CPU interrupt.
Start the DTC	“✓” in this column indicates usability as a request for DTC transfer.
sstb return	“✓” in this column indicates usability as a request for return from software-standby mode.
IER	Name of the IER register and bit corresponding to the vector number
IPR	Name of the IPR register corresponding to the interrupt source
DTCER	Name of the DTCER register corresponding to the DTC trigger

Table 14.3 Interrupt Vector Table (1/6)

Source of Interrupt Request Generation	Name	Vector No.*1	Vector Address Offset	Form of Interrupt Detection	CPU	DTC	sstb Return	IER	IPR	DTCER
—	For an unconditional trap	0	0000h	—	N/A	N/A	N/A	—	—	—
—	For an unconditional trap	1	0004h	—	N/A	N/A	N/A	—	—	—
—	For an unconditional trap	2	0008h	—	N/A	N/A	N/A	—	—	—
—	For an unconditional trap	3	000Ch	—	N/A	N/A	N/A	—	—	—
—	For an unconditional trap	4	0010h	—	N/A	N/A	N/A	—	—	—
—	For an unconditional trap	5	0014h	—	N/A	N/A	N/A	—	—	—
—	For an unconditional trap	6	0018h	—	N/A	N/A	N/A	—	—	—
—	For an unconditional trap	7	001Ch	—	N/A	N/A	N/A	—	—	—
—	For an unconditional trap	8	0020h	—	N/A	N/A	N/A	—	—	—
—	For an unconditional trap	9	0024h	—	N/A	N/A	N/A	—	—	—
—	For an unconditional trap	10	0028h	—	N/A	N/A	N/A	—	—	—
—	For an unconditional trap	11	002Ch	—	N/A	N/A	N/A	—	—	—
—	For an unconditional trap	12	0030h	—	N/A	N/A	N/A	—	—	—
—	For an unconditional trap	13	0034h	—	N/A	N/A	N/A	—	—	—
—	For an unconditional trap	14	0038h	—	N/A	N/A	N/A	—	—	—
—	For an unconditional trap	15	003Ch	—	N/A	N/A	N/A	—	—	—
BSC	BUSERR	16	0040h	Level	✓	N/A	N/A	IER02.IEN0	IPR000	—
—	Reserved	17	0044h	—	N/A	N/A	N/A	—	—	—
—	Reserved	18	0048h	—	N/A	N/A	N/A	—	—	—
—	Reserved	19	004Ch	—	N/A	N/A	N/A	—	—	—
—	Reserved	20	0050h	—	N/A	N/A	N/A	—	—	—
—	Reserved	21	0054h	—	N/A	N/A	N/A	—	—	—
—	Reserved	22	0058h	—	N/A	N/A	N/A	—	—	—
FCU	FRDYI	23	005Ch	Edge	✓	N/A	N/A	IER02.IEN7	IPR002	—
—	Reserved	24	0060h	—	N/A	N/A	N/A	—	—	—
—	Reserved	25	0064h	—	N/A	N/A	N/A	—	—	—
—	Reserved	26	0068h	—	N/A	N/A	N/A	—	—	—
ICU	SWINT	27	006Ch	Edge	✓	✓	N/A	IER03.IEN3	IPR003	DTCER027
CMT0	CMI0	28	0070h	Edge	✓	✓	N/A	IER03.IEN4	IPR004	DTCER028
CMT1	CMI1	29	0074h	Edge	✓	✓	N/A	IER03.IEN5	IPR005	DTCER029
CMT2	CMI2	30	0078h	Edge	✓	✓	N/A	IER03.IEN6	IPR006	DTCER030
CMT3	CMI3	31	007Ch	Edge	✓	✓	N/A	IER03.IEN7	IPR007	DTCER031
CAC	FERRF	32	0080h	Level	✓	N/A	N/A	IER04.IEN0	IPR032	—
	MENDF	33	0084h	Level	✓	N/A	N/A	IER04.IEN1	IPR033	—
	OVFF	34	0088h	Level	✓	N/A	N/A	IER04.IEN2	IPR034	—
—	Reserved	35	008Ch	—	N/A	N/A	N/A	—	—	—
—	Reserved	36	0090h	—	N/A	N/A	N/A	—	—	—
—	Reserved	37	0094h	—	N/A	N/A	N/A	—	—	—
—	Reserved	38	0098h	—	N/A	N/A	N/A	—	—	—
—	Reserved	39	009Ch	—	N/A	N/A	N/A	—	—	—
GPT	ETGIN	40	00A0h	Edge	✓	N/A	N/A	IER05.IEN0	IPR040	—
	ETGIP	41	00A4h	Edge	✓	N/A	N/A	IER05.IEN1	IPR041	—
—	Reserved	42	00A8h	—	N/A	N/A	N/A	—	—	—
—	Reserved	43	00ACh	—	N/A	N/A	N/A	—	—	—
RSPI0	SPEI0	44	00B0h	Level	✓	N/A	N/A	IER05.IEN4	IPR044	—
	SPRI0	45	00B4h	Edge	✓	✓	N/A	IER05.IEN5		DTCER045
	SPTI0	46	00B8h	Edge	✓	✓	N/A	IER05.IEN6		DTCER046
	SPII0	47	00BCh	Level	✓	N/A	N/A	IER05.IEN7		—

Table 14.3 Interrupt Vector Table (2/6)

Source of Interrupt Request Generation	Name	Vector No.*1	Vector Address Offset	Form of Interrupt Detection	CPU	DTC	sstb Return	IER	IPR	DTCER
GPT0	GTCIA0	48	00C0h	Edge	✓	✓	N/A	IER06.IEN0	IPR048	DTCER048
	GTCIB0	49	00C4h	Edge	✓	✓	N/A	IER06.IEN1	IPR049	DTCER049
	GTCIC0	50	00C8h	Edge	✓	✓	N/A	IER06.IEN2	IPR050	DTCER050
	GTCID0	51	00CCh	Edge	✓	✓	N/A	IER06.IEN3	IPR051	DTCER051
	GDTE0	52	00D0h	Edge	✓	N/A	N/A	IER06.IEN4	IPR052	—
	GTCIE0	53	00D4h	Edge	✓	✓	N/A	IER06.IEN5	IPR053	DTCER053
	GTCIF0	54	00D8h	Edge	✓	✓	N/A	IER06.IEN6	IPR054	DTCER054
	GTCIV0	55	00DCh	Edge	✓	✓	N/A	IER06.IEN7	IPR055	DTCER055
	GTCIU0	56	00E0h	Edge	✓	✓	N/A	IER07.IEN0	IPR056	DTCER056
DOC	DOPCF	57	00E4h	Level	✓	N/A	N/A	IER07.IEN1	IPR057	—
—	Reserved	58	00E8h	—	N/A	N/A	N/A	—	—	—
RSCAN	COMFRXINT	59	00ECh	Edge	✓	✓	N/A	IER07.IEN3	IPR059	DTCER059
	RXFINT	60	00F0h	Level	✓	N/A	N/A	IER07.IEN4	IPR060	—
	TXINT	61	00F4h	Level	✓	N/A	N/A	IER07.IEN5	IPR061	—
	CHERRINT	62	00F8h	Level	✓	N/A	N/A	IER07.IEN6	IPR062	—
	GLERRINT	63	00FCh	Level	✓	N/A	N/A	IER07.IEN7	IPR063	—
ICU	IRQ0	64	0100h	Edge/Level	✓	✓	✓	IER08.IEN0	IPR064	DTCER064
	IRQ1	65	0104h	Edge/Level	✓	✓	✓	IER08.IEN1	IPR065	DTCER065
	IRQ2	66	0108h	Edge/Level	✓	✓	✓	IER08.IEN2	IPR066	DTCER066
	IRQ3	67	010Ch	Edge/Level	✓	✓	✓	IER08.IEN3	IPR067	DTCER067
	IRQ4	68	0110h	Edge/Level	✓	✓	✓	IER08.IEN4	IPR068	DTCER068
	IRQ5	69	0114h	Edge/Level	✓	✓	✓	IER08.IEN5	IPR069	DTCER069
	IRQ6	70	0118h	Edge/Level	✓	✓	✓	IER08.IEN6	IPR070	DTCER070
	IRQ7	71	011Ch	Edge/Level	✓	✓	✓	IER08.IEN7	IPR071	DTCER071
—	Reserved	72	0120h	—	N/A	N/A	N/A	—	—	—
—	Reserved	73	0124h	—	N/A	N/A	N/A	—	—	—
—	Reserved	74	0128h	—	N/A	N/A	N/A	—	—	—
—	Reserved	75	012Ch	—	N/A	N/A	N/A	—	—	—
—	Reserved	76	0130h	—	N/A	N/A	N/A	—	—	—
—	Reserved	77	0134h	—	N/A	N/A	N/A	—	—	—
—	Reserved	78	0138h	—	N/A	N/A	N/A	—	—	—
—	Reserved	79	013Ch	—	N/A	N/A	N/A	—	—	—
—	Reserved	80	0140h	—	N/A	N/A	N/A	—	—	—
—	Reserved	81	0144h	—	N/A	N/A	N/A	—	—	—
—	Reserved	82	0148h	—	N/A	N/A	N/A	—	—	—
—	Reserved	83	014Ch	—	N/A	N/A	N/A	—	—	—
—	Reserved	84	0150h	—	N/A	N/A	N/A	—	—	—
—	Reserved	85	0154h	—	N/A	N/A	N/A	—	—	—
—	Reserved	86	0158h	—	N/A	N/A	N/A	—	—	—
—	Reserved	87	015Ch	—	N/A	N/A	N/A	—	—	—
LVD	LVD1	88	0160h	Edge	✓	N/A	✓	IER0B.IEN0	IPR088	—
	LVD2	89	0164h	Edge	✓	N/A	✓	IER0B.IEN1	IPR089	—
—	Reserved	90	0168h	—	N/A	N/A	N/A	—	—	—
—	Reserved	91	016Ch	—	N/A	N/A	N/A	—	—	—
—	Reserved	92	0170h	—	N/A	N/A	N/A	—	—	—
—	Reserved	93	0174h	—	N/A	N/A	N/A	—	—	—
—	Reserved	94	0178h	—	N/A	N/A	N/A	—	—	—
—	Reserved	95	017Ch	—	N/A	N/A	N/A	—	—	—
—	Reserved	96	0180h	—	N/A	N/A	N/A	—	—	—
—	Reserved	97	0184h	—	N/A	N/A	N/A	—	—	—

Table 14.3 Interrupt Vector Table (3/6)

Source of Interrupt Request Generation	Name	Vector No.*1	Vector Address Offset	Form of Interrupt Detection	CPU	DTC	sstb Return	IER	IPR	DTCER
GPT1	GTCIA1	98	0188h	Edge	✓	✓	N/A	IER0C.IEN2	IPR098	DTCER098
	GTCIB1	99	018Ch	Edge	✓	✓	N/A	IER0C.IEN3	IPR099	DTCER099
	GTCIC1	100	0190h	Edge	✓	✓	N/A	IER0C.IEN4	IPR100	DTCER100
	GTCID1	101	0194h	Edge	✓	✓	N/A	IER0C.IEN5	IPR101	DTCER101
S12AD	S12ADI	102	0198h	Edge	✓	✓	N/A	IER0C.IEN6	IPR102	DTCER102
	GBADI	103	019Ch	Edge	✓	✓	N/A	IER0C.IEN7	IPR103	DTCER103
	GCADI	104	01A0h	Edge	✓	✓	N/A	IER0D.IEN0	IPR104	DTCER104
S12AD1	S12ADI1	105	01A4h	Edge	✓	✓	N/A	IER0D.IEN1	IPR105	DTCER105
	GBADI1	106	01A8h	Edge	✓	✓	N/A	IER0D.IEN2	IPR106	DTCER106
	GCADI1	107	01ACh	Edge	✓	✓	N/A	IER0D.IEN3	IPR107	DTCER107
CMPC0	CMPC0	108	01B0h	Edge	✓	✓	N/A	IER0D.IEN4	IPR108	DTCER108
CMPC1	CMPC1	109	01B4h	Edge	✓	✓	N/A	IER0D.IEN5	IPR109	DTCER109
CMPC2	CMPC2	110	01B8h	Edge	✓	✓	N/A	IER0D.IEN6	IPR110	DTCER110
S12AD2	S12ADI2	111	01BCh	Edge	✓	✓	N/A	IER0D.IEN7	IPR111	DTCER111
	GBADI2	112	01C0h	Edge	✓	✓	N/A	IER0E.IEN0	IPR112	DTCER112
	GCADI2	113	01C4h	Edge	✓	✓	N/A	IER0E.IEN1	IPR113	DTCER113
MTU0	TGIA0	114	01C8h	Edge	✓	✓	N/A	IER0E.IEN2	IPR114	DTCER114
	TGIB0	115	01CCh	Edge	✓	✓	N/A	IER0E.IEN3		DTCER115
	TGIC0	116	01D0h	Edge	✓	✓	N/A	IER0E.IEN4		DTCER116
	TGID0	117	01D4h	Edge	✓	✓	N/A	IER0E.IEN5		DTCER117
	TCIV0	118	01D8h	Edge	✓	N/A	N/A	IER0E.IEN6	IPR118	—
	TGIE0	119	01DCh	Edge	✓	N/A	N/A	IER0E.IEN7		—
	TGIF0	120	01E0h	Edge	✓	N/A	N/A	IER0F.IEN0		—
MTU1	TGIA1	121	01E4h	Edge	✓	✓	N/A	IER0F.IEN1	IPR121	DTCER121
	TGIB1	122	01E8h	Edge	✓	✓	N/A	IER0F.IEN2		DTCER122
	TCIV1	123	01ECh	Edge	✓	N/A	N/A	IER0F.IEN3	IPR123	—
	TCIU1	124	01F0h	Edge	✓	N/A	N/A	IER0F.IEN4		—
MTU2	TGIA2	125	01F4h	Edge	✓	✓	N/A	IER0F.IEN5	IPR125	DTCER125
	TGIB2	126	01F8h	Edge	✓	✓	N/A	IER0F.IEN6		DTCER126
	TCIV2	127	01FCh	Edge	✓	N/A	N/A	IER0F.IEN7	IPR127	—
	TCIU2	128	0200h	Edge	✓	N/A	N/A	IER10.IEN0		—
MTU3	TGIA3	129	0204h	Edge	✓	✓	N/A	IER10.IEN1	IPR129	DTCER129
	TGIB3	130	0208h	Edge	✓	✓	N/A	IER10.IEN2		DTCER130
	TGIC3	131	020Ch	Edge	✓	✓	N/A	IER10.IEN3		DTCER131
	TGID3	132	0210h	Edge	✓	✓	N/A	IER10.IEN4		DTCER132
	TCIV3	133	0214h	Edge	✓	N/A	N/A	IER10.IEN5	IPR133	—
MTU4	TGIA4	134	0218h	Edge	✓	✓	N/A	IER10.IEN6	IPR134	DTCER134
	TGIB4	135	021Ch	Edge	✓	✓	N/A	IER10.IEN7		DTCER135
	TGIC4	136	0220h	Edge	✓	✓	N/A	IER11.IEN0		DTCER136
	TGID4	137	0224h	Edge	✓	✓	N/A	IER11.IEN1		DTCER137
	TCIV4	138	0228h	Edge	✓	✓	N/A	IER11.IEN2	IPR138	DTCER138
MTU5	TGIU5	139	022Ch	Edge	✓	✓	N/A	IER11.IEN3	IPR139	DTCER139
	TGIV5	140	0230h	Edge	✓	✓	N/A	IER11.IEN4		DTCER140
	TGIW5	141	0234h	Edge	✓	✓	N/A	IER11.IEN5		DTCER141
MTU6	TGIA6	142	0238h	Edge	✓	✓	N/A	IER11.IEN6	IPR142	DTCER142
	TGIB6	143	023Ch	Edge	✓	✓	N/A	IER11.IEN7		DTCER143
	TGIC6	144	0240h	Edge	✓	✓	N/A	IER12.IEN0		DTCER144
	TGID6	145	0244h	Edge	✓	✓	N/A	IER12.IEN1		DTCER145
	TCIV6	146	0248h	Edge	✓	N/A	N/A	IER12.IEN2	IPR146	—
—	Reserved	147	024Ch	—	N/A	N/A	N/A	—	—	—
—	Reserved	148	0250h	—	N/A	N/A	N/A	—	—	—

Table 14.3 Interrupt Vector Table (4/6)

Source of Interrupt Request Generation	Name	Vector No.*1	Vector Address Offset	Form of Interrupt Detection	CPU	DTC	sstb Return	IER	IPR	DTCER
MTU7	TGIA7	149	0254h	Edge	✓	✓	N/A	IER12.IEN5	IPR149	DTCER149
	TGIB7	150	0258h	Edge	✓	✓	N/A	IER12.IEN6		DTCER150
	TGIC7	151	025Ch	Edge	✓	✓	N/A	IER12.IEN7	IPR151	DTCER151
	TGID7	152	0260h	Edge	✓	✓	N/A	IER13.IEN0		DTCER152
	TCIV7	153	0264h	Edge	✓	✓	N/A	IER13.IEN1	IPR153	DTCER153
—	Reserved	154	0268h	—	N/A	N/A	N/A	—	—	—
—	Reserved	155	026Ch	—	N/A	N/A	N/A	—	—	—
—	Reserved	156	0270h	—	N/A	N/A	N/A	—	—	—
—	Reserved	157	0274h	—	N/A	N/A	N/A	—	—	—
—	Reserved	158	0278h	—	N/A	N/A	N/A	—	—	—
MTU9	TGIA9	159	027Ch	Edge	✓	✓	N/A	IER13.IEN7	IPR159	DTCER159
	TGIB9	160	0280h	Edge	✓	✓	N/A	IER14.IEN0		DTCER160
	TGIC9	161	0284h	Edge	✓	✓	N/A	IER14.IEN1		DTCER161
	TGID9	162	0288h	Edge	✓	✓	N/A	IER14.IEN2		DTCER162
	TCIV9	163	028Ch	Edge	✓	N/A	N/A	IER14.IEN3	IPR163	—
	TGIE9	164	0290h	Edge	✓	N/A	N/A	IER14.IEN4		—
	TGIF9	165	0294h	Edge	✓	N/A	N/A	IER14.IEN5		—
—	Reserved	166	0298h	—	N/A	N/A	N/A	—	—	—
—	Reserved	167	029Ch	—	N/A	N/A	N/A	—	—	—
POE	OEI1	168	02A0h	Level	✓	N/A	N/A	IER15.IEN0	IPR168	—
	OEI2	169	02A4h	Level	✓	N/A	N/A	IER15.IEN1		—
	OEI3	170	02A8h	Level	✓	N/A	N/A	IER15.IEN2		—
	OEI4	171	02ACh	Level	✓	N/A	N/A	IER15.IEN3		—
	OEI5	172	02B0h	Level	✓	N/A	N/A	IER15.IEN4		—
CMPC3	CMPC3	173	02B4h	Edge	✓	✓	N/A	IER15.IEN5	IPR173	DTCER173
TMR0	CMIA0	174	02B8h	Edge	✓	✓	N/A	IER15.IEN6	IPR174	DTCER174
	CMIB0	175	02BCh	Edge	✓	✓	N/A	IER15.IEN7		DTCER175
	OVI0	176	02C0h	Edge	✓	N/A	N/A	IER16.IEN0		—
TMR1	CMIA1	177	02C4h	Edge	✓	✓	N/A	IER16.IEN1	IPR177	DTCER177
	CMIB1	178	02C8h	Edge	✓	✓	N/A	IER16.IEN2		DTCER178
	OVI1	179	02CCh	Edge	✓	N/A	N/A	IER16.IEN3		—
TMR2	CMIA2	180	02D0h	Edge	✓	✓	N/A	IER16.IEN4	IPR180	DTCER180
	CMIB2	181	02D4h	Edge	✓	✓	N/A	IER16.IEN5		DTCER181
	OVI2	182	02D8h	Edge	✓	N/A	N/A	IER16.IEN6		—
TMR3	CMIA3	183	02DCh	Edge	✓	✓	N/A	IER16.IEN7	IPR183	DTCER183
	CMIB3	184	02E0h	Edge	✓	✓	N/A	IER17.IEN0		DTCER184
	OVI3	185	02E4h	Edge	✓	N/A	N/A	IER17.IEN1		—
TMR4	CMIA4	186	02E8h	Edge	✓	✓	N/A	IER17.IEN2	IPR186	DTCER186
	CMIB4	187	02ECh	Edge	✓	✓	N/A	IER17.IEN3		DTCER187
	OVI4	188	02F0h	Edge	✓	N/A	N/A	IER17.IEN4		—
TMR5	CMIA5	189	02F4h	Edge	✓	✓	N/A	IER17.IEN5	IPR189	DTCER189
	CMIB5	190	02F8h	Edge	✓	✓	N/A	IER17.IEN6		DTCER190
	OVI5	191	02FCh	Edge	✓	N/A	N/A	IER17.IEN7		—
TMR6	CMIA6	192	0300h	Edge	✓	✓	N/A	IER18.IEN0	IPR192	DTCER192
	CMIB6	193	0304h	Edge	✓	✓	N/A	IER18.IEN1		DTCER193
	OVI6	194	0308h	Edge	✓	N/A	N/A	IER18.IEN2		—
TMR7	CMIA7	195	030Ch	Edge	✓	✓	N/A	IER18.IEN3	IPR195	DTCER195
	CMIB7	196	0310h	Edge	✓	✓	N/A	IER18.IEN4		DTCER196
	OVI7	197	0314h	Edge	✓	N/A	N/A	IER18.IEN5		—
—	Reserved	198	0318h	—	N/A	N/A	N/A	—	—	—
—	Reserved	199	031Ch	—	N/A	N/A	N/A	—	—	—

Table 14.3 Interrupt Vector Table (5/6)

Source of Interrupt Request Generation	Name	Vector No.*1	Vector Address Offset	Form of Interrupt Detection	CPU	DTC	sstb Return	IER	IPR	DTCER
—	Reserved	200	0320h	—	N/A	N/A	N/A	—	—	—
—	Reserved	201	0324h	—	N/A	N/A	N/A	—	—	—
GPT1	GDTE1	202	0328h	Edge	✓	N/A	N/A	IER19.IEN2	IPR202	—
	GTCIE1	203	032Ch	Edge	✓	✓	N/A	IER19.IEN3	IPR203	DTCER203
	GTCIF1	204	0330h	Edge	✓	✓	N/A	IER19.IEN4	IPR204	DTCER204
	GTCIV1	205	0334h	Edge	✓	✓	N/A	IER19.IEN5	IPR205	DTCER205
	GTCIU1	206	0338h	Edge	✓	✓	N/A	IER19.IEN6	IPR206	DTCER206
GPT2	GTCIA2	207	033Ch	Edge	✓	✓	N/A	IER19.IEN7	IPR207	DTCER207
	GTCIB2	208	0340h	Edge	✓	✓	N/A	IER1A.IEN0	IPR208	DTCER208
	GTCIC2	209	0344h	Edge	✓	✓	N/A	IER1A.IEN1	IPR209	DTCER209
	GTCID2	210	0348h	Edge	✓	✓	N/A	IER1A.IEN2	IPR210	DTCER210
	GDTE2	211	034Ch	Edge	✓	N/A	N/A	IER1A.IEN3	IPR211	—
	GTCIE2	212	0350h	Edge	✓	✓	N/A	IER1A.IEN4	IPR212	DTCER212
	GTCIF2	213	0354h	Edge	✓	✓	N/A	IER1A.IEN5	IPR213	DTCER213
	GTCIV2	214	0358h	Edge	✓	✓	N/A	IER1A.IEN6	IPR214	DTCER214
	GTCIU2	215	035Ch	Edge	✓	✓	N/A	IER1A.IEN7	IPR215	DTCER215
GPT3	GTCIA3	216	0360h	Edge	✓	✓	N/A	IER1B.IEN0	IPR216	DTCER216
	GTCIB3	217	0364h	Edge	✓	✓	N/A	IER1B.IEN1	IPR217	DTCER217
SCI1	ERI1	218	0368h	Level	✓	N/A	N/A	IER1B.IEN2	IPR218	—
	RXI1	219	036Ch	Edge	✓	✓	N/A	IER1B.IEN3		DTCER219
	TXI1	220	0370h	Edge	✓	✓	N/A	IER1B.IEN4		DTCER220
	TEI1	221	0374h	Level	✓	N/A	N/A	IER1B.IEN5		—
SCI5	ERI5	222	0378h	Level	✓	N/A	N/A	IER1B.IEN6	IPR222	—
	RXI5	223	037Ch	Edge	✓	✓	N/A	IER1B.IEN7		DTCER223
	TXI5	224	0380h	Edge	✓	✓	N/A	IER1C.IEN0		DTCER224
	TEI5	225	0384h	Level	✓	N/A	N/A	IER1C.IEN1		—
SCI6	ERI6	226	0388h	Level	✓	N/A	N/A	IER1C.IEN2	IPR226	—
	RXI6	227	038Ch	Edge	✓	✓	N/A	IER1C.IEN3		DTCER227
	TXI6	228	0390h	Edge	✓	✓	N/A	IER1C.IEN4		DTCER228
	TEI6	229	0394h	Level	✓	N/A	N/A	IER1C.IEN5		—
SCI8	ERI8	230	0398h	Level	✓	N/A	N/A	IER1C.IEN6	IPR230	—
	RXI8	231	039Ch	Edge	✓	✓	N/A	IER1C.IEN7		DTCER231
	TXI8	232	03A0h	Edge	✓	✓	N/A	IER1D.IEN0		DTCER232
	TEI8	233	03A4h	Level	✓	N/A	N/A	IER1D.IEN1		—
SCI9	ERI9	234	03A8h	Level	✓	N/A	N/A	IER1D.IEN2	IPR234	—
	RXI9	235	03ACh	Edge	✓	✓	N/A	IER1D.IEN3		DTCER235
	TXI9	236	03B0h	Edge	✓	✓	N/A	IER1D.IEN4		DTCER236
	TEI9	237	03B4h	Level	✓	N/A	N/A	IER1D.IEN5		—
GPT3	GTCIC3	238	03B8h	Edge	✓	✓	N/A	IER1D.IEN6	IPR238	DTCER238
	GTCID3	239	03BCh	Edge	✓	✓	N/A	IER1D.IEN7	IPR239	DTCER239
	GDTE3	240	03C0h	Edge	✓	N/A	N/A	IER1E.IEN0	IPR240	—
	GTCIE3	241	03C4h	Edge	✓	✓	N/A	IER1E.IEN1	IPR241	DTCER241
	GTCIF3	242	03C8h	Edge	✓	✓	N/A	IER1E.IEN2	IPR242	DTCER242
	GTCIV3	243	03CCh	Edge	✓	✓	N/A	IER1E.IEN3	IPR243	DTCER243
	GTCIU3	244	03D0h	Edge	✓	✓	N/A	IER1E.IEN4	IPR244	DTCER244
—	Reserved	245	03D4h	—	N/A	N/A	N/A	—	—	—
RIIC0	EEI0	246	03D8h	Level	✓	N/A	N/A	IER1E.IEN6	IPR246	—
	RXI0	247	03DCh	Edge	✓	✓	N/A	IER1E.IEN7	IPR247	DTCER247
	TXI0	248	03E0h	Edge	✓	✓	N/A	IER1F.IEN0	IPR248	DTCER248
	TEI0	249	03E4h	Level	✓	N/A	N/A	IER1F.IEN1	IPR249	—

Table 14.3 Interrupt Vector Table (6/6)

Source of Interrupt Request Generation	Name	Vector No.*1	Vector Address Offset	Form of Interrupt Detection	CPU	DTC	sstb Return	IER	IPR	DTCER
SCI11	ERI11	250	03E8h	Level	✓	N/A	N/A	IER1F.IEN2	IPR250	—
	RXI11	251	03ECh	Edge	✓	✓	N/A	IER1F.IEN3		DTCER251
	TXI11	252	03F0h	Edge	✓	✓	N/A	IER1F.IEN4		DTCER252
	TEI11	253	03F4h	Level	✓	N/A	N/A	IER1F.IEN5		—
—	Reserved	254	03F8h	—	N/A	N/A	N/A	—	—	—
—	Reserved	255	03FCh	—	N/A	N/A	N/A	—	—	—

Note 1. An interrupt source with a smaller vector number takes precedence.

14.3.2 Fast Interrupt Vector Table

The address of the entry in the interrupt vector table that corresponds to the vector number of the fast interrupt is placed in the fast interrupt vector register (FINTV) of the CPU.

14.3.3 Non-maskable Interrupt Vector Area

Non-maskable interrupts use the vector area in the exception vector table.
The exception vector table is allocated to the 128-byte area (4 bytes × 32 sources) beginning with the address set in the EXTB register in the CPU. Set a multiple of 4 in the EXTB register.

14.4 Interrupt Operation

The interrupt controller performs the following processing.

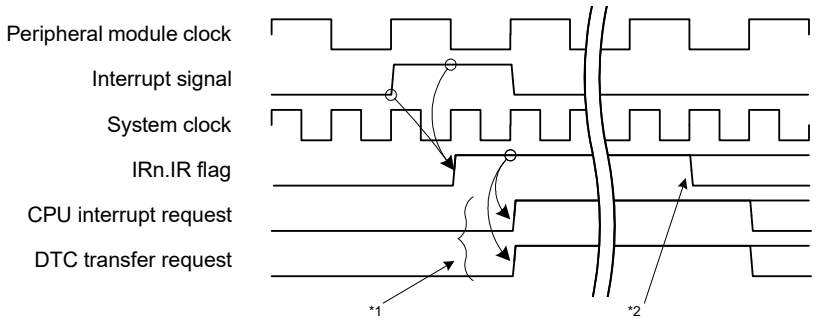
- Detecting interrupts
- Enabling and disabling interrupts
- Selecting interrupt request destinations (CPU interrupt or DTC trigger)
- Determining priority

14.4.1 Detecting Interrupts

Interrupt requests are detected in either of two ways: the detection of edges of the interrupt signal or the detection of a level of the interrupt signal.
Edge detection or level detection is selected for the IRQi pins (i = 0 to 7) as external interrupt requests by the setting of the IRQMD[1:0] bits in IRQCRi.
For interrupts from peripheral modules, either edge detection or level detection is determined per interrupt source.
For the correspondence between interrupt sources and methods of detection, see Table 14.3, Interrupt Vector Table.

14.4.1.1 Operation of Status Flags for Edge-Detected Interrupts

Figure 14.2 shows the operation of the IR flag in IRn (n = interrupt vector number) in the case of edge detection of an interrupt from a peripheral module or on an external pin.
The IR flag in IRn is set to 1 immediately after the transition of the interrupt signal due to generation of the interrupt. If the CPU is the request destination for the interrupt, the IR flag is automatically cleared to 0 on acceptance of the interrupt. If the DTC is the request destination for the interrupt, the IRn.IR flag operation differs according to the DTC transfer settings and transfer count. For details, see Table 14.4, Operation When Starting the DTC.



Note 1. One of the following requests is issued: CPU interrupt request, DTC transfer request. For details of the setting, see section 14.4.3, Selecting Interrupt Request Destinations.
Note 2. When the CPU interrupt request is specified, this flag is set to 0 on acceptance of a CPU interrupt. For the timing of 0 setting at the DTC transfer request, see Table 14.4, Operation When Starting the DTC.

Figure 14.2 IRn.IR Flag Operation for Edge Detection Interrupts

Figure 14.3 to Figure 14.5 show the interrupt signals of the interrupt controller. Note that the timings of the interrupts with interrupt vector numbers 64 to 95 are different from those of other interrupts. For the IRQ pin interrupts with interrupt vector numbers 64 to 79, “internal delay + 2 PCLK cycles” of delay is added after the IRQ pin input. For the interrupts with interrupt vector numbers 80 to 95, “2 PCLK cycles” of delay is added.

If an interrupt signal is generated every clock cycle, the subsequent interrupts cannot be detected; secure two or more clock cycles of the system clock between issuance of continuous interrupt requests.

While the IRn.IR flag is 1 after an interrupt request is generated, the interrupt request that is generated again will be ignored.*1
Figure 14.3 shows the timing for IRn.IR flag re-setting.

Note 1. When the transmission or reception interrupt of the SCI, RSPI, RIIC, or RSCAN is generated with the IRn.IR flag being 1, the interrupt request is retained. After the IRn.IR flag is cleared to 0, the IRn.IR flag is set to 1 again by the retained request. For details, see descriptions of the interrupts in section 26, Serial Communications Interface (SCIg), section 27, I2C-bus Interface (RIICa), and section 29, Serial Peripheral Interface (RSPIb).

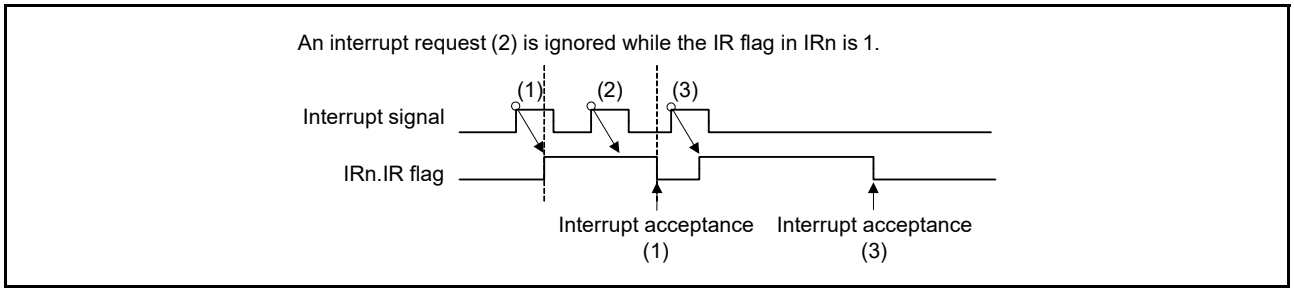


Figure 14.3 Timing for IRn.IR Flag Re-Setting

If an interrupt is disabled after the IRn.IR flag is set to 1 (output of the interrupt request is disabled by the interrupt enable bit of the relevant peripheral module), the IRn.IR flag is not affected but retains its state. Figure 14.4 shows operation when the interrupt is disabled.

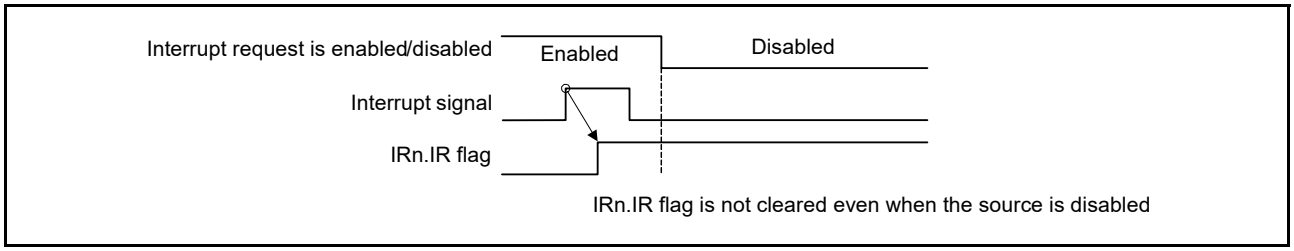


Figure 14.4 Relationship between IRn.IR Flag Operation and Disabling of Interrupt Request

14.4.1.2 Operation of Status Flags for Level-Detected Interrupts

Figure 14.5 shows the operation of the interrupt status flag (IR flag) in IRn (n = interrupt vector number) in the case of level detection of an interrupt from a peripheral module or an external pin.
The IR flag in IRn remains set to 1 as long as the interrupt signal is asserted. To clear the IRn.IR flag to 0, clear the interrupt request in the source generating the interrupt. Confirm that the interrupt request flag in the source generating the interrupt has been cleared to 0 and that the IRn.IR flag has been cleared to 0, and then complete the interrupt handling.

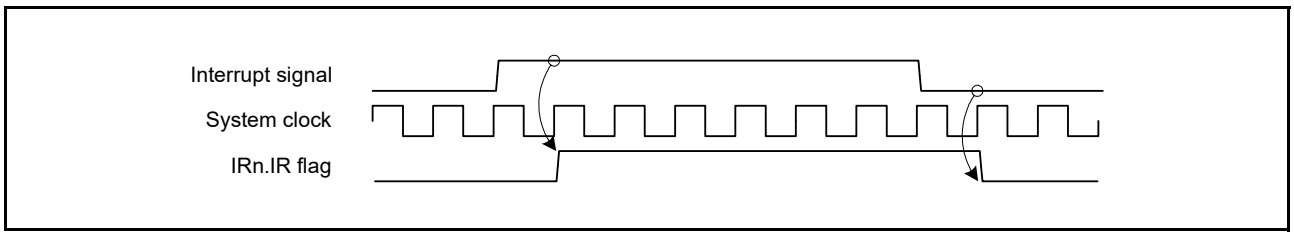


Figure 14.5 IRn.IR Flag Operation for Level Detection Interrupts

Figure 14.6 shows the procedure for handling level detection interrupts.

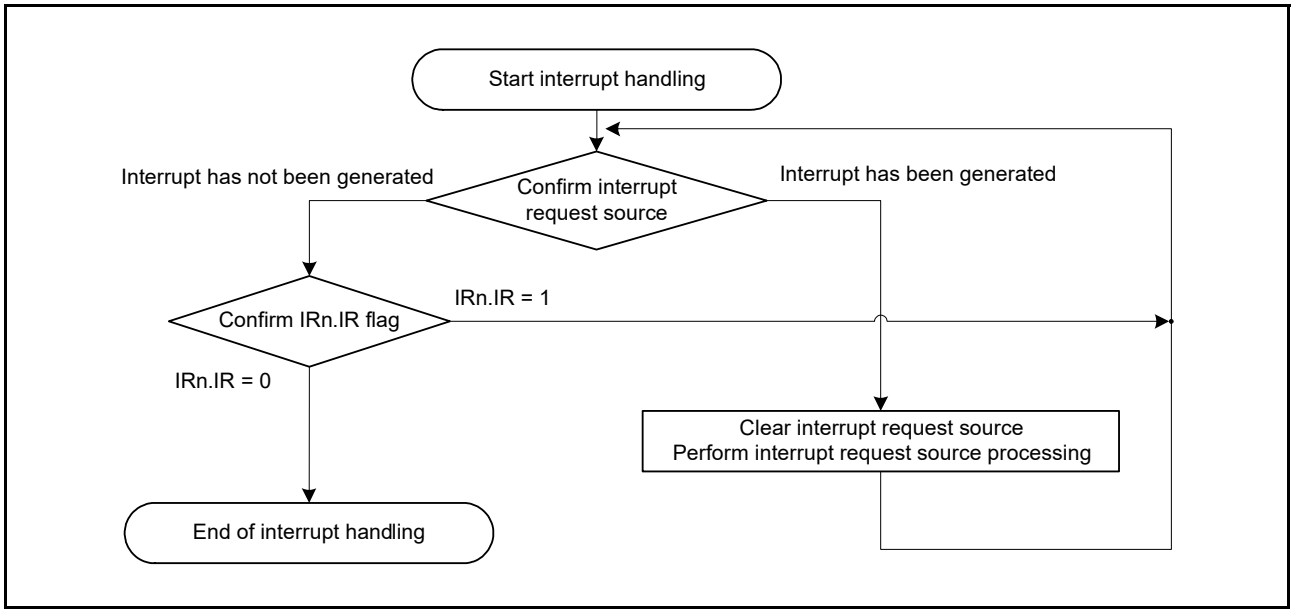


Figure 14.6 Procedure for Handling Level Detection Interrupts

14.4.2 Enabling and Disabling Interrupt Sources

Enabling requests from a given interrupt source requires the following settings.

1. In the case of interrupt requests from peripheral modules, setting the interrupt enable bit for the peripheral module to permit the output of interrupt requests from the source
2. Enabling of the interrupt by the IERm.IENj bit (m = 02h to 1Fh, j = 0 to 7)

When an interrupt request that is enabled at the corresponding source is generated, the corresponding IRn.IR flag (n = interrupt vector number) is set to 1.
Setting the IERm.IENj bit to enable an interrupt request allows the interrupt request for which the corresponding IRn.IR is 1 to be output to the interrupt request destination. Setting the IERm.IENj bit to disable an interrupt request suspends the output of the interrupt request for which the corresponding IRn.IR is 1.
The IRn.IR flag is not affected by the IERm.IENj bit.

Use the following procedure to disable interrupt requests.

1. Set the IERm.IENj bit to disable interrupt requests.
2. Set the peripheral module interrupt output enable bit to disable the output. Read the last written register and confirm that writing is completed.
3. Check the IRn.IR flag, and clear the IRn.IR flag if necessary.*1

Note 1. To disable the transmission or reception interrupt of the SCI, RSPI, or RIIC from the enabled state, clear the IRn.IR flag to 0 using the above procedure. For details, see descriptions of the interrupts in section 26, Serial Communications Interface (SCIg), section 27, I^2C-bus Interface (RIICa), and section 29, Serial Peripheral Interface (RSPIb).

14.4.3 Selecting Interrupt Request Destinations

Possible settings for the request destination of each interrupt are fixed. That is, settings for request destination other than those indicated in Table 14.3, Interrupt Vector Table, are not possible. Do not make an interrupt request destination setting that is not indicated by a "✓" in Table 14.3.
If the DTC is selected as the destination for requests from an IRQi pin (i = 0 to 7), be sure to set the IRQMD[1:0] bits in IRQCRi for that interrupt to select edge detection.
The following describes how to specify the destinations of interrupt requests.

(1) DTC Trigger

Make the following settings for each source while the IERm.IENj bit (m = 02h to 1Fh, j = 0 to 7) is 0.

1. Set the DTC transfer request enable bit in the DTC transfer request enable register (DTCERn.DTCE (n = interrupt vector number)) for the pertinent source to 1.

After making the above settings, set the IERm.IENj bit to 1.
In addition, set the DTC module start bit (DTCST.DTCST) to 1. The order of making settings for each interrupt and enabling the DTC module start bit does not matter.
For the DTC setting procedure, refer to section 17.5, DTC Setting Procedure, in section 17, Data Transfer Controller (DTCa).

(2) CPU Interrupt Request

If the interrupt request destination is the DTC, the interrupt request is sent to the CPU. Set the IERm.IENj bit (m = 02h to 1Fh, j = 0 to 7) to 1 while the DTC trigger settings described above are in place.

Table 14.4 shows operation when the DTC is the request destination.

Table 14.4 Operation When Starting the DTC

Interrupt Request Destination	DISEL *1	Remaining Number of Transfer Operations	Operation per Request	IR*2	Interrupt Request Destination after Transfer
DTC*3	1	≠ 0	DTC transfer → CPU interrupt	Cleared on interrupt acceptance by the CPU	DTC
		= 0	DTC transfer → CPU interrupt	Cleared on interrupt acceptance by the CPU	The DTCERn.DTCE bit is cleared and the CPU becomes the destination.
	0	≠ 0	DTC transfer	Cleared at the start of DTC data transfer after reading DTC transfer information	DTC
		= 0	DTC transfer → CPU interrupt	Cleared on interrupt acceptance by the CPU	The DTCERn.DTCE bit is cleared and the CPU becomes the destination.

Note 1. DISEL for the DTC is set by the DTC.MRB.DISEL bit.
Note 2. When the IRn.IR flag is 1, an interrupt request (DTC transfer request) that is generated again will be ignored.
Note 3. For chain transfer, DTC transfer continues until the last chain transfer ends. Whether a CPU interrupt is generated at the end of chain transfer, the IRn.IR flag clear timing, and the interrupt request destination after transfer are determined by the state of DISEL and the remaining transfer count at the end of chain transfer. For the chain transfer, see Table 17.3, Chain Transfer Conditions in section 17, Data Transfer Controller (DTCa).

The request destination for an interrupt should be changed while the IERm.IENj bit is 0.

When a source is to be changed to an interrupt request or the DTC transfer information is to be changed while a transfer is not complete (i.e. while the DTCERn.DTCE bit (n = interrupt vector number) has not been cleared) after the settings described under (1) DTC Trigger have been made, follow the procedure below.

1. For both the source to be withdrawn and the source that will have a new trigger, clear the IENj bits in IERm to 0.
2. Check the state of transfer by the DTC. If transfer is in progress, wait for its completion.
3. Make the settings described under (1) DTC Trigger.

14.4.4 Determining Priority

Interrupt priority is determined for each interrupt request destination.
The priority for each interrupt request destination is determined as follows.

(1) Determining Priority when the CPU is the Request Destination of the Interrupt

A source selected for the fast interrupt has the highest priority. After that, an interrupt source with a larger value of the interrupt priority level select bits (IPR[3:0]) in IPRn takes priority. If interrupts with the same priority level are generated by multiple sources, the source with the smallest vector number takes precedence.

(2) Determining Priority when the DTC is the Request Destination of the Interrupt

The IPR[3:0] bits in IPRn (n = interrupt vector number) have no effect. An interrupt source with a smaller vector number takes precedence.

14.4.5 Multiple Interrupts

To enable multiple interrupts of the CPU, set the PSW.I bit to 1 (interrupt enabled) in the handling routine of accepted interrupts.
The PSW.IPL[3:0] bits immediately after processing branches to the interrupt handling routine are set to the same value as the interrupt priority level of the accepted interrupt request. If an interrupt request which has an interrupt level higher than that of the PSW.IPL[3:0] bits is generated at this time, this interrupt request (for multiple interrupts) is accepted.
If the interrupt priority level of the accepted interrupt request is 15 (fast interrupt or interrupt when IPR[3:0] are set to 1111b), multiple interrupts are not generated.

14.4.6 Fast Interrupt

The fast interrupt is an interrupt for executing a faster interrupt response by the CPU, so only one of the interrupt sources can be assigned.
The interrupt priority level of the fast interrupt is 15 (highest) regardless of the setting of the IPR[3:0] bits in IPRn (n = interrupt vector number). In addition, the fast interrupt is accepted with precedence over other interrupt sources with level 15. However, when the value of the PSW.IPL[3:0] bits are 1111b (priority level 15), even the fast interrupt cannot be accepted.
To assign an interrupt source to the fast interrupt, specify the vector number of the source in the FIR.FVCT[7:0] bits, and set the FIR.FIEN bit to 1 (fast interrupt is enabled).
For details on the fast interrupt, see section 2, CPU and section 13, Exception Handling.

14.4.7 Digital Filter

The digital filter function is provided for the external interrupt request IRQi pins (i = 0 to 7) and NMI pin interrupt.
The digital filter samples input signals at the filter sampling clock (PCLK) and removes the pulses of which length is less than three sampling cycles.
To use the digital filter for the IRQi pin, set the sampling clock cycle (PCLK, PCLK/8, PCLK/32, or PCLK/64) with the IRQFLTC0.FCLKSELi[1:0] bits and set the IRQFLTE0.FLTENi bit to 1 (digital filter enabled).
To use the digital filter for the NMI pin, set the sampling clock cycle (PCLK, PCLK/8, PCLK/32, or PCLK/64) with the NMIFLTC.NFCLKSEL[1:0] bits and set the NMIFLTE.NFLTEN bit to 1 (digital filter enabled).
Figure 14.7 shows an example of digital filter operation.

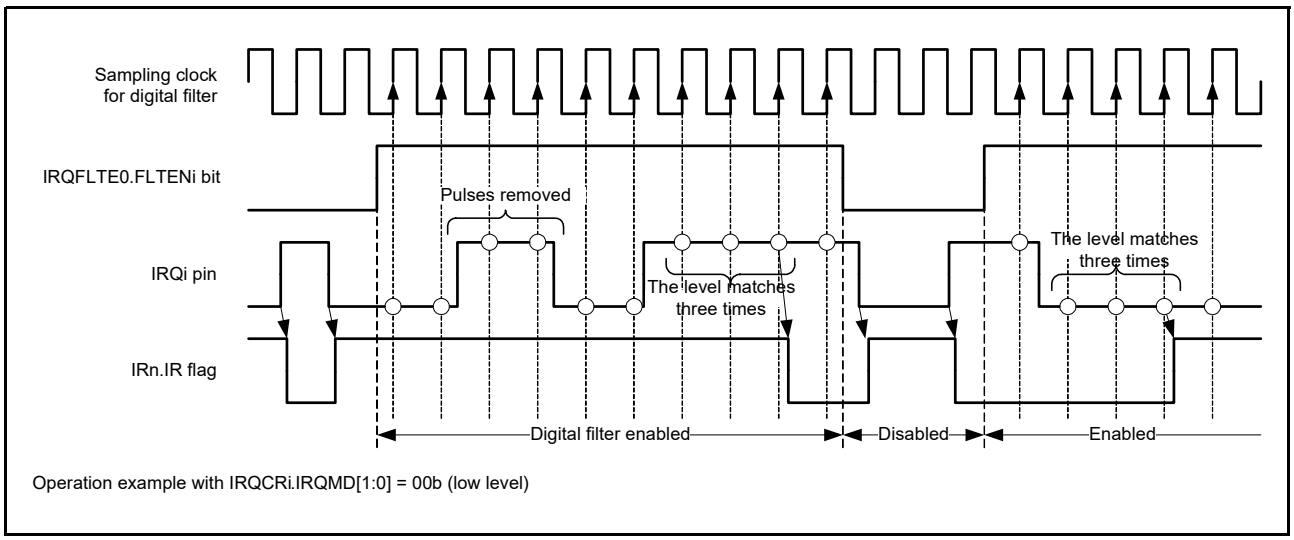


Figure 14.7 Digital Filter Operation Example

Before software standby mode is entered, set the IRQFLTE0.FLTENi and NMIFLTE.NFLTEN bits to 0 (digital filter disabled). To use the digital filter again after return from software standby mode, set the IRQFLTE0.FLTENi or NMIFLTE.NFLTEN bit to 1 (digital filter enabled).

14.4.8 External Pin Interrupts

The procedure for using the signal on an external pin as an interrupt is as follows.

1. Clear the IERm.IENj bit (m = 02h to 1Fh, j = 0 to 7) to 0 (interrupt request disabled).
2. Clear the IRQFLTE0.FLTENi bit (i = 0 to 7) to 0 (digital filter disabled).*1
3. Set the digital filter sampling clock with the IRQFLTC0.FCLKSELi[1:0] bits.*1
4. Make or confirm the I/O port settings.
5. Set the method of detection for the interrupt in the IRQCRi.IRQMD[1:0] bits.
6. Clear the corresponding IRn.IR flag (n = interrupt vector number) to 0 (if edge detection is in use).
7. Set the IRQFLTE0.FLTENi bit to 1 (digital filter enabled).*1
8. If the interrupt is to be used for DTC trigger, set the DTCERn.DTCE bit. The interrupt will be a CPU interrupt if the setting not is made.
9. Set the IERm.IENj bit to 1 (interrupt request enabled).

Note 1. To use the digital filter function, settings must be made beforehand.

14.5 Non-maskable Interrupt Operation

There are six types of non-maskable interrupt: the NMI pin interrupt, oscillation stop detection interrupt, IWDT underflow/refresh error, voltage monitoring 1 interrupt, and voltage monitoring 2 interrupt. Non-maskable interrupts are only usable as interrupts for the CPU; that is, they are not capable of DTC trigger. Non-maskable interrupts take precedence over all interrupts, including the fast interrupt.
Non-maskable interrupt requests are accepted regardless of the states of the I (interrupt enable) bit and IPL[3:0] (processor interrupt priority level) bits in the PSW of the CPU. The current states of the non-maskable interrupts can be checked in the non-maskable interrupt status register (NMISR).
Confirm that all bits in the NMISR have returned to 0 from within the handler for the non-maskable interrupt, before ending the handler.
Non-maskable interrupts are disabled by default. If a system is to use non-maskable interrupts, the following procedure must be followed at the beginning of program processing.

Non-maskable interrupt usage procedure:

1. Set the stack pointer (SP).
2. To use the NMI pin, clear the NMIFLTE.NFLTEN bit to 0 (digital filter disabled).*1
3. To use the NMI pin, set the digital filter sampling clock with the NMIFLTC.NFCLKSEL[1:0] bits.*1
4. To use the NMI pin, set the NMI pin detection sense with the NMICR.NMIMD bit.
5. To use the NMI pin, write 1 to the NMICLR.NMICLR bit to clear the NMISR.NMIST flag to 0.
6. To use the NMI pin, set the NMIFLTE.NFLTEN bit to 1 (digital filter enabled).*1
7. Enable the non-maskable interrupt by writing 1 to the corresponding bit in the non-maskable interrupt enable register (NMIER).

Note 1. To use the digital filter function, settings must be made beforehand.

After 1 is written to the NMIER register, subsequent write access to the NMIEN bit in NMIER is ignored. The NMI interrupt cannot be disabled. It can be disabled only by a reset.
For the flow of non-maskable interrupt processing, see section 13, Exception Handling.
Writing 1 to the NMICLR.NMICLR bit clears the NMI status flag (NMISR.NMIST) to 0.
Writing 1 to the NMICLR.OSTCLR bit clears the oscillation stop detection interrupt status flag (NMISR.OSTST) to 0.
Writing 1 to the NMICLR.IWDTCLR bit clears the IWDT underflow/refresh error status flag (NMISR.IWDTST) to 0.
Writing 1 to the NMICLR.LVD1CLR bit clears the voltage monitoring 1 interrupt status flag (NMISR.LVD1ST) to 0.
Writing 1 to the NMICLR.LVD2CLR bit clears the voltage monitoring 2 interrupt status flag (NMISR.LVD2ST) to 0.

14.6 Return from Power-Down States

The interrupt sources that can be used to return operation from sleep mode, deep sleep mode, or software standby mode are listed in Table 14.3, Interrupt Vector Table.
For details, refer to section 11, Low Power Consumption. The following describes how to use an interrupt to return operation from each low power consumption mode.

14.6.1 Return from Sleep Mode or Deep Sleep Mode

If the interrupt controller is to return operation from sleep mode in response to an interrupt or non-maskable interrupt, make the following settings for the interrupt.

- Interrupts

1. Select the CPU as the interrupt request destination.
2. Use the IENj bit in IERm (m = 02h to 1Fh, j = 0 to 7) to enable the given interrupt request.
3. Set a priority level higher than that set by the IPL[3:0] bits in the PSW of CPU.

- Non-maskable interrupts

Use the NMIER register to enable the given interrupt request.

14.6.2 Return from Software Standby Mode

The interrupt controller can return operation from a non-maskable interrupt or an interrupt that enables the return from the software standby mode.
The conditions for the return are listed below.

- Interrupts

1. Select the interrupt source that enables the return from the software standby mode.
2. Select the CPU as the interrupt request destination.
3. Use the IENj bit in IERm (m = 02h to 1Fh, j = 0 to 7) to enable the given interrupt request.
4. Set a priority level higher than that set by the IPL[3:0] bits in the PSW of CPU.
   (For the interrupt source specified as a fast interrupt, as well as setting the fast interrupt set register (FIR), the interrupt priority level (IPRn (n = interrupt vector number)) should be set above the level set by IPL in the PSW of the CPU.)

Interrupt requests through the IRQ pins that do not satisfy the above conditions are not detected while the clock is stopped in software standby mode.

- Non-maskable interrupts

Use the NMIER register to enable the given interrupt request.

- Procedure to make a transition to/from software standby mode

1. Before software standby mode is entered, disable the digital filter for the interrupt source as a return target (IRQFLTE0.FLTENi = 0, NMIFLTE.NFLTEN = 0).
2. To use the digital filter again after return from software standby mode, enable the digital filter (IRQFLTE0.FLTENi = 1, NMIFLTE.NFLTEN = 1).

14.7 Usage Note

14.7.1 Note on WAIT Instruction Used with Non-Maskable Interrupt

Before executing the WAIT instruction, check to see that all the status flags in NMISR are 0.

15. Buses

15.1 Overview

Table 15.1 lists the bus specifications, Figure 15.1 shows the bus configuration, and Table 15.2 lists the addresses assigned for each bus.

Table 15.1 Bus Specifications

Bus Type		Description
CPU bus	Instruction bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
	Operand bus	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
Memory bus	Memory bus 1	• Connected to RAM
	Memory bus 2	• Connected to ROM
Internal main bus	Internal main bus 1	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)
	Internal main bus 2	• Connected to the DTC • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
Internal peripheral bus	Internal peripheral bus 1	• Connected to peripheral modules (DTC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)
	Internal peripheral bus 2	• Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, and 4) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 3	• Connected to peripheral modules (RSCAN, CMPC) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 4	• Connected to peripheral modules (MTU, GPT, SCI11) • Operates in synchronization with the peripheral-module clock (PCLKA)
	Internal peripheral bus 6	• Connected to the flash control module and E2 DataFlash • Operates in synchronization with the FlashIF clock (FCLK)

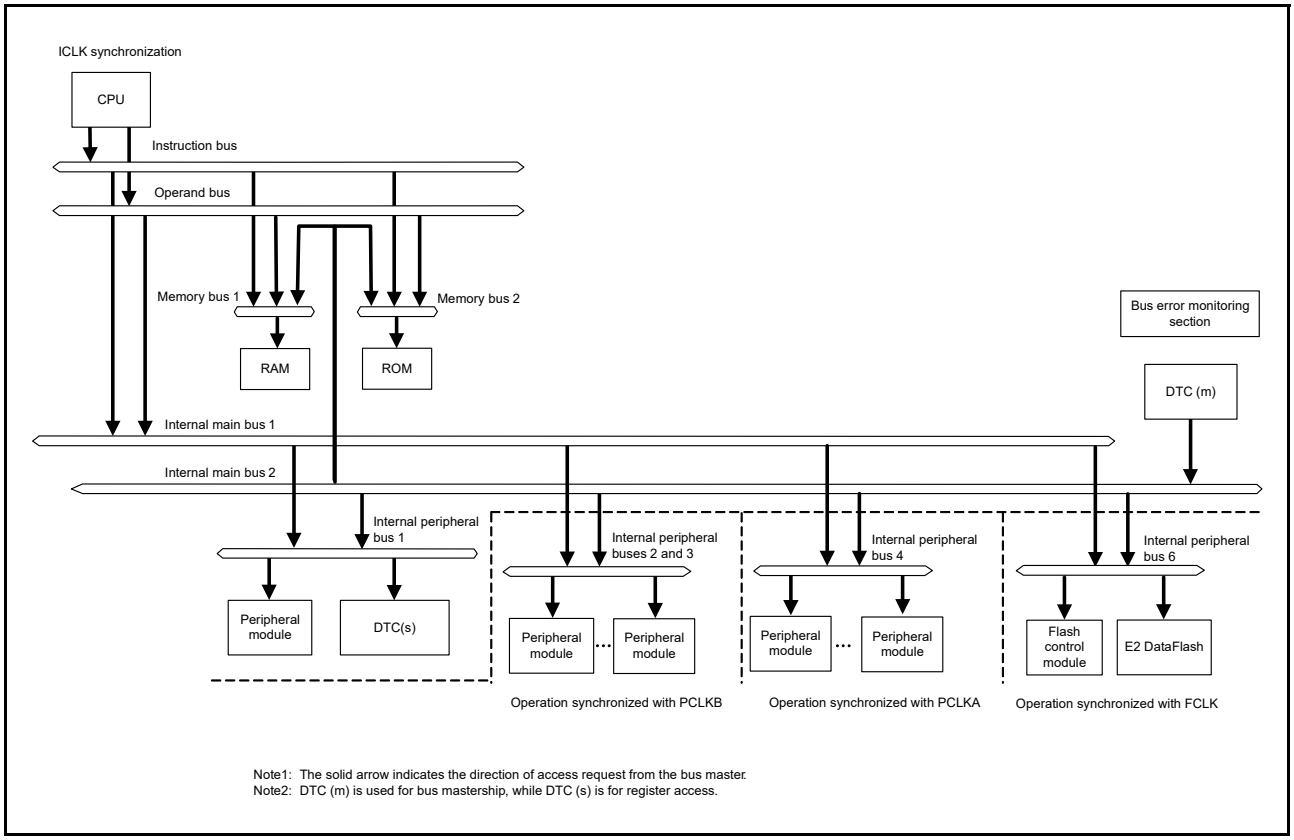


Figure 15.1 Bus Configuration

Table 15.2 Addresses Assigned for Each Bus

Address	Bus	Area
0000 0000h to 0000 7FFFh	Memory bus 1	RAM
0000 8000h to 0007 FFFFh		Reserved area
0008 0000h to 0008 7FFFh	Internal peripheral bus 1	Peripheral I/O registers
0008 8000h to 0009 FFFFh	Internal peripheral bus 2	
000A 0000h to 000B FFFFh	Internal peripheral bus 3	
000C 0000h to 000D FFFFh	Internal peripheral bus 4	
000E 0000h to 000F FFFFh	Reserved area	Reserved area
0010 0000h to 00FF FFFFh	Internal peripheral bus 6	Flash control module, E2 DataFlash
0100 0000h to 7FFF FFFFh	Reserved area	Reserved area
8000 0000h to FFFF FFFFh	Memory bus 2	ROM (for reading only)

15.2 Description of Buses

15.2.1 CPU Buses

The CPU buses consist of the instruction and operand buses, which are connected to internal main bus 1. As the names suggest, the instruction bus is used to fetch instructions for the CPU, while the operand bus is used for operand access. The instruction bus is 64 bits while the operand bus is 32 bits.
Connection of the instruction and operand buses to RAM and ROM provides the CPU with direct access to these areas, i.e. access is not via internal main bus 1. However, only reading is possible in direct access to ROM by the CPU; programming and erasure are handled via an internal peripheral bus.
Bus requests for instruction fetching and operand access are arbitrated through internal main bus 1. The order of priority is operand access then instruction fetching.
If instruction fetching and operand access are requested for different buses (memory bus 1, memory bus 2, and internal main bus 1), the bus-access operations can proceed simultaneously. For example, parallel access to ROM and RAM.

15.2.2 Memory Buses

The memory buses consist of memory bus 1 and memory bus 2. RAM is connected to memory bus 1 and ROM is connected to memory bus 2. The memory buses are 64 bits. Requests for bus mastership from the CPU buses (instruction fetching and operand) and internal main bus 2 are arbitrated through memory buses 1 and 2.
The priority order of the buses can be set using the memory bus 1 (RAM) priority control bits (BPRA[1:0]) and memory bus 2 (ROM) priority control bits (BPRO[1:0]) in the bus priority control register (BUSPRI) for the corresponding memory buses. When the priority order is fixed, internal main bus 2 has priority over the CPU bus (operand over instruction fetching). When the priority order is toggled, a bus has a lower priority when the request of that bus is accepted.

15.2.3 Internal Main Buses

The internal main buses consist of a bus for use by the CPU (internal main bus 1) and a bus for use by the other bus-master modules, i.e. the DTC (internal main bus 2).
Bus requests for instruction fetching and operand access are arbitrated through internal main bus 1. The order of priority is operand access then instruction fetching.
If the CPU and another bus master are requesting access to different buses (on-chip memory, internal peripheral buses 1 to 4, 6), the respective bus-access operations can proceed simultaneously.
However, when the CPU executes the XCHG instruction, requests for bus access from masters other than the CPU are not accepted until data transfer for the XCHG instruction is completed regardless of the bus priority control register (BUSPRI) setting. Furthermore, requests for bus access from masters other than the DTC are not accepted during reading and writing-back of transfer control information for the DTC.

Table 15.3 Order of Priority for Bus Masters

Priority	Internal main buses	Bus Master
High ↑ Low	2	DTC
	1	CPU

Note: The above applies when the priority order of the buses is fixed.
The priority order of internal main bus 1 and another bus (internal main bus 2) can be toggled by the bus priority control register (BUSPRI) (round-robin method).

15.2.4 Internal Peripheral Buses

Connection of peripheral modules to the internal peripheral buses is as described in Table 15.4.

Table 15.4 Connection of Peripheral Modules to the Internal Peripheral Buses

Type of Bus	Peripheral Modules
Internal peripheral bus 1	DTC, interrupt controller, and bus error monitoring section
Internal peripheral bus 2	Peripheral modules other than those connected to internal peripheral buses 1, 3, and 4
Internal peripheral bus 3	RSCAN, CMPC
Internal peripheral bus 4	MTU, GPT, SCI11
Internal peripheral bus 6	Flash control module, E2 DataFlash

Requests for bus mastership from the CPU (internal main bus 1) and other bus masters (internal main bus 2) are arbitrated through internal peripheral buses 1 to 4, and 6.
The priority order of two internal main buses can be set using the bus priority control register (BUSPRI). The priority order can be set with the internal peripheral bus 1 priority control bits (BUSPRI.BPIB[1:0]), internal peripheral bus 2 and 3 priority control bits (BUSPRI.BPGB[1:0]), internal peripheral bus 4 priority control bits (BUSPRI.BPHB[1:0]), and internal peripheral bus 6 priority control bits (BUSPRI.BPFB[1:0]) for the corresponding internal peripheral buses.
When the priority order is fixed, internal main bus 2 has priority over internal main bus 1. When the priority order is toggled, a bus has a lower priority when the request of that bus is accepted (round-robin method).
The order of accepting requests may change depending on the BUSPRI setting (Refer to Figure 15.2).

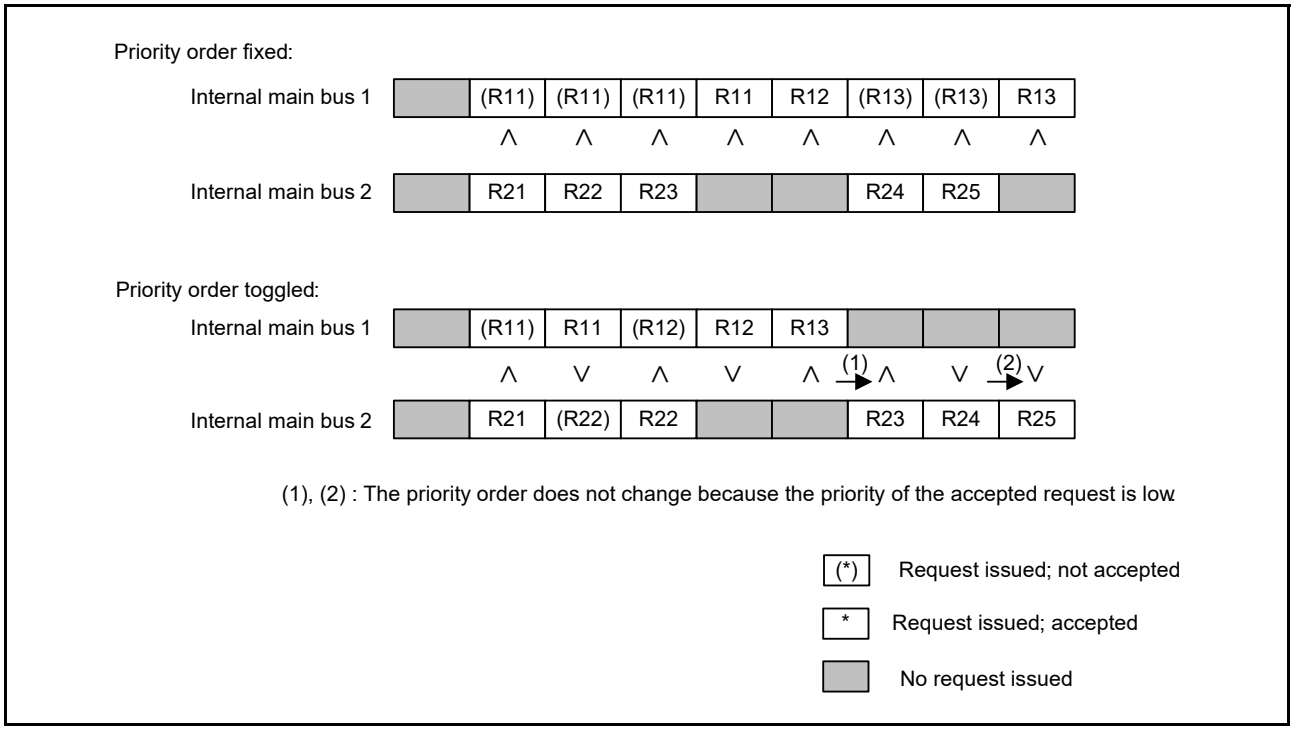


Figure 15.2 Priority Order between Internal Peripheral Bus Accesses

15.2.5 Write Buffer Function (Internal Peripheral Bus)

The internal peripheral bus has the write buffer function, which allows the next round of bus access to start, before the current write access is completed, in write access. However, if the following round of bus access is from the same bus master but to the different internal peripheral bus, it is suspended until the bus operations already in progress are completed. When read access to the internal memory is scheduled after the write access to the internal peripheral bus from the CPU, the following round of bus access can be started before the current bus operation is completed and thus the order of accesses may be changed (Refer to Figure 15.3).

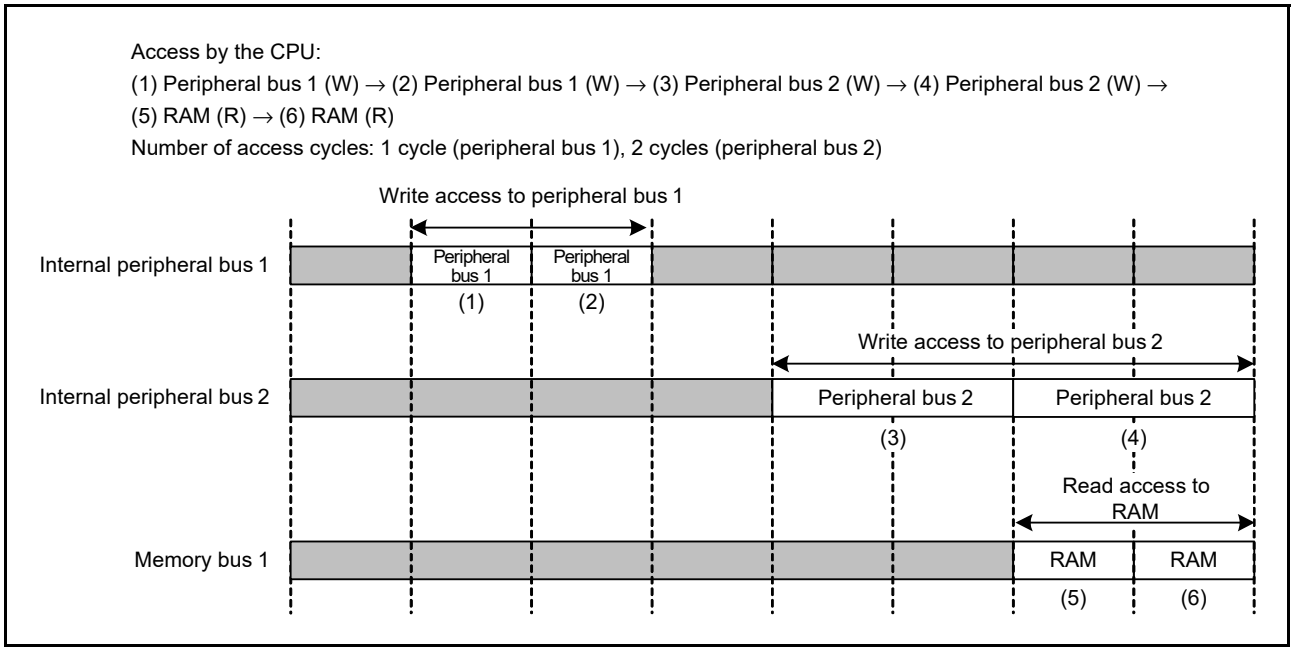


Figure 15.3 Write Buffer Function

15.2.6 Parallel Operation

Parallel operation is possible when different bus-master modules are requesting access to different slave modules. For example, if the CPU is fetching an instruction from ROM and an operand from RAM, the DTC is able to handle transfer between peripheral buses at the same time.

An example of parallel operations is shown in Figure 15.4. In this example, the CPU is able to employ the instruction and operand buses for simultaneous access to ROM and RAM, respectively. Furthermore, the DTC simultaneously employs internal main bus 2 for access to peripheral buses during access to RAM and ROM by the CPU.

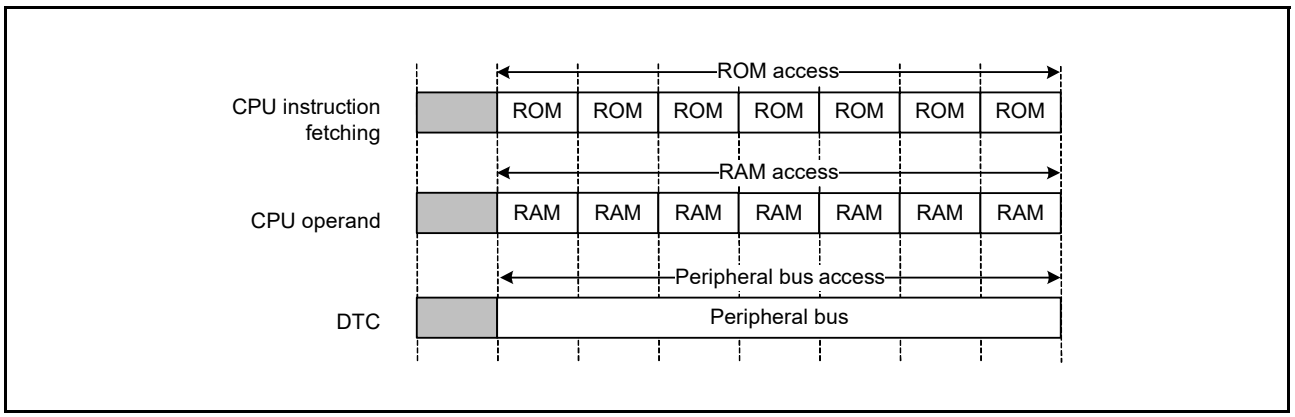


Figure 15.4 Example of Parallel Operations

15.2.7 Restrictions

(1) Prohibition of Access that Spans Areas of Address Space

Single access that spans two areas of the address space is prohibited, and operation of such an access is not guaranteed. Setting must be made so that two areas are not accessed at the same time by a single word or longword access.

(2) Restrictions in Relation to RMPA and String-Manipulation Instructions

(a) The allocation of data to be handled by RMPA or string-manipulation instructions to I/O registers is prohibited, and operation is not guaranteed if this restriction is not observed.

15.3 Register Descriptions

15.3.1 Bus Error Status Clear Register (BERCLR)

Address(es): 0008 1300h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	STSCLR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	STSCLR	Status Clear	0: Invalid 1: Bus error status register cleared	(W)*1
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only writing 1 is effective; i.e. writing 0 has no effect.

STSCLR Bit (Status Clear)

Writing 1 to this bit clears the bus error status registers 1 and 2 (BERSR1 and BERSR2).
Writing 0 has no effect. It is read as 0.

15.3.2 Bus Error Monitoring Enable Register (BEREN)

Address(es): 0008 1304h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	TOEN	IGAEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	IGAEN	Illegal Address Access Detection Enable	0: Illegal address access detection is disabled. 1: Illegal address access detection is enabled.	R/W
b1	TOEN	Timeout Detection Enable*1, *2	0: Bus timeout detection is disabled. 1: Bus timeout detection is enabled.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. When detection is disabled (the TOEN bit is cleared to 0), bus access can cause the bus to freeze.
Note 2. Do not clear the TOEN bit to 0 (bus timeout detection disabled) while timeout errors are being detected.

15.3.3 Bus Error Status Register 1 (BERSR1)

Address(es): 0008 1308h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	MST[2:0]			—	—	TO	IA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	IA	Illegal Address Access	0: Illegal address access not made 1: Illegal address access made	R
b1	TO	Timeout	0: Timeout not generated 1: Timeout generated	R
b3, b2	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R
b6 to b4	MST[2:0]	Bus Master Code	b6 b4 0 0 0: CPU 0 0 1: Reserved 0 1 0: Reserved 0 1 1: DTC 1 0 0: Reserved 1 0 1: Reserved 1 1 0: Reserved 1 1 1: Reserved	R
b7	—	Reserved	This bit is read as 0. Writing to this bit has no effect.	R

MST[2:0] Bits (Bus Master Code)

These bits indicate the bus master that accessed a bus when a bus error occurred.

15.3.4 Bus Error Status Register 2 (BERSR2)

Address(es): 0008 130Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ADDR[12:0]													—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R
b15 to b3	ADDR[12:0]	Bus Error Occurrence Address	The upper 13 bits of an address that was accessed when a bus error occurred (in units of 512 Kbytes).	R

15.3.5 Bus Priority Control Register (BUSPRI)

Address(es): 0008 1310h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	BPFB[1:0]		BPHB[1:0]		BPGB[1:0]		BPIB[1:0]		BPRO[1:0]		BPRA[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	BPRA[1:0]	Memory Bus 1 (RAM) Priority Control	b1 b0 0 0: The order of priority is fixed. 0 1: The order of priority is toggled. 1 0: Setting prohibited 1 1: Setting prohibited	R(/W) *1
b3, b2	BPRO[1:0]	Memory Bus 2 (ROM) Priority Control	b3 b2 0 0: The order of priority is fixed. 0 1: The order of priority is toggled. 1 0: Setting prohibited 1 1: Setting prohibited	R(/W) *1
b5, b4	BPIB[1:0]	Internal Peripheral Bus 1 Priority Control	b5 b4 0 0: The order of priority is fixed. 0 1: The order of priority is toggled. 1 0: Setting prohibited 1 1: Setting prohibited	R(/W) *1
b7, b6	BPGB[1:0]	Internal Peripheral Bus 2 and 3 Priority Control	b7 b6 0 0: The order of priority is fixed. 0 1: The order of priority is toggled. 1 0: Setting prohibited 1 1: Setting prohibited	R(/W) *1
b9, b8	BPHB[1:0]	Internal Peripheral Bus 4 Priority Control	b9 b8 0 0: The order of priority is fixed. 0 1: The order of priority is toggled. 1 0: Setting prohibited 1 1: Setting prohibited	R(/W) *1
b11, b10	BPFB[1:0]	Internal Peripheral Bus 6 Priority Control	b11 b10 0 0: The order of priority is fixed. 0 1: The order of priority is toggled. 1 0: Setting prohibited 1 1: Setting prohibited	R(/W) *1
b15 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. These bits can be written to only once while the DTC are written to more than one time, the operation is not guaranteed.

BPRA[1:0] Bits (Memory Bus 1 (RAM) Priority Control)

These bits specify the priority order for memory bus 1 (RAM).

When the priority order is fixed, internal main bus 2 has priority over internal main bus 1.

When the priority order is toggled, a bus has a lower priority when the request of that bus is accepted.

BPRO[1:0] Bits (Memory Bus 2 (ROM) Priority Control)

These bits specify the priority order for memory bus 2 (ROM).

When the priority order is fixed, internal main bus 2 has priority over internal main bus 1.

When the priority order is toggled, a bus has a lower priority when the request of that bus is accepted.

BPIB[1:0] Bits (Internal Peripheral Bus 1 Priority Control)

These bits specify the priority order for internal peripheral bus 1.

When the priority order is fixed, internal main bus 2 has priority over internal main bus 1.

When the priority order is toggled, a bus has a lower priority when the request of that bus is accepted.

BPGB[1:0] Bits (Internal Peripheral Bus 2 and 3 Priority Control)

These bits specify the priority order for internal peripheral buses 2 and 3.
When the priority order is fixed, internal main bus 2 has priority over internal main bus 1.
When the priority order is toggled, a bus has a lower priority when the request of that bus is accepted.

BPHB[1:0] Bits (Internal Peripheral Bus 4 Priority Control)

These bits specify the priority order for internal peripheral bus 4.
When the priority order is fixed, internal main bus 2 has priority over internal main bus 1.
When the priority order is toggled, a bus has a lower priority when the request of that bus is accepted.

BPFB[1:0] Bits (Internal Peripheral Bus 6 Priority Control)

These bits specify the priority order for internal peripheral bus 6.
When the priority order is fixed, internal main bus 2 has priority over internal main bus 1.
When the priority order is toggled, a bus has a lower priority when the request of that bus is accepted.

15.4 Bus Error Monitoring Section

The bus error monitoring section monitors the individual areas for bus errors, and when a bus error occurs, the error is indicated to the bus master.

15.4.1 Types of Bus Error

There are two types of bus error: illegal address access and timeout.
Illegal address access is the detection of illegal access to an area, and time-out is the detection of a bus-access operation not being completed within 768 cycles.

15.4.1.1 Illegal Address Access

When the illegal address access detection enable bit (IGAEN) in the bus error monitoring enable register (BEREN) is set to 1, access of the following types leads to illegal address access errors.

- Access to illegal address ranges
  The address ranges where access will lead to illegal address access errors are indicated in Table 15.5.

15.4.1.2 Timeout

When the timeout detection enable bit (TOEN) in the bus error monitoring enable register (BEREN) is set to 1, bus access that is not completed within 768 cycles leads to a timeout error.

- Internal peripheral buses (2 and 3): Bus access is not completed within 768 peripheral module clock (PCLKB) cycles from the start of the access. In this MCU, a timeout error does not occur.
  Once a timeout error occurs, accesses from the bus master are rejected for 256 PCLKB cycles.
- Internal peripheral buses (4): Bus access is not completed within 768 peripheral module clock (PCLKA) cycles from the start of the access.
  Once a timeout error occurs, accesses from the bus master are rejected for 256 PCLKA cycles.
- Internal peripheral bus (6): Bus access is not completed within 768 FlashIF clock (FCLK) cycles from the start of the access.
  Once a timeout error occurs, accesses from the bus master are rejected for 256 FCLK cycles. In this MCU, a timeout error does not occur.

15.4.2 Operations When a Bus Error Occurs

When a bus error occurs, the error is indicated to the CPU. Operation is not guaranteed when a bus error occurs.

- Bus error indication to the CPU
  An interrupt is generated. The IERn register in the ICU can specify whether to generate an interrupt in the case of a bus error.

15.4.3 Conditions Leading to Bus Errors

Table 15.5 lists the types of bus errors for each area in the respective address space.
If an illegal address access error or timeout is detected when no bus error has occurred (bus error status register n (BERSRn; n = 1 or 2) is cleared), the detected error is reflected on the BERSRn. Once a bus error occurs, no subsequent bus errors are reflected on the register unless the register is cleared.
If bus errors are simultaneously caused by two or more bus masters, error information of only one bus master is reflected. Once a bus error occurs, the status is retained until BERSRn is cleared.

Table 15.5 Types of Bus Errors

Address	Type of Area	Type of Error
		Illegal Address Access
0000 0000h to 0007 FFFFh	Memory bus 1	—
0008 0000h to 0008 7FFFh	Internal peripheral bus 1	—
0008 8000h to 0009 FFFFh	Internal peripheral bus 2	Δ
000A 0000h to 000B FFFFh	Internal peripheral bus 3	Δ
000C 0000h to 000D FFFFh	Internal peripheral bus 4	Δ
000E 0000h to 000F FFFFh	Reserved area	—
0010 0000h to 00FF FFFFh	Internal peripheral bus 6	Δ
0100 0000h to 0FFF FFFFh	Reserved area	—
1000 0000h to 7FFF FFFFh	Reserved area	○
8000 0000h to FFFF FFFFh	Memory bus 2	—

—: A bus error does not result.
Δ: A bus error may or may not result.
○: A bus error results.
Note: The capacity of the RAM and ROM differs depending on the product. For details, see section 35, RAM, section 36, Flash Memory.

15.5 Interrupt

15.5.1 Interrupt Source

An illegal address access error or detection of a timeout leads to a bus error signal for the interrupt controller.

Table 15.6 Interrupt Source

Name	Interrupt Source	DTC Activation
BUSERR	Illegal address access error or timeout	Not possible

16. Memory-Protection Unit (MPU)

16.1 Overview

The RXv2 CPU incorporates a memory-protection unit that checks the addresses of CPU access to the overall address space (0000 0000h to FFFF FFFFh).

Access-control information can be set for up to eight regions, and permission for access to each region is in accord with this information. The default response to the detection of access to a region where permission has not been set is the generation of a memory-protection error.

The supported access-control information for the individual regions consists of permission to read, permission to write, and permission to execute. This access-control information is effective when the processor mode of the CPU is user mode. Memory protection is not applied when the CPU is in supervisor mode.

Table 16.1 lists the specifications of the memory-protection unit, and Figure 16.1 shows a block diagram of the memory-protection unit.

Table 16.1 Specifications of Memory Protection

Specifictaions	Description
Region to be covered by memory protection and processor mode	0000 0000h to FFFF FFFFh (in user mode) No memory protection in supervisor mode
Number of regions	8
Page size (smallest unit of protection)	16 bytes
Specifying addresses of individual regions	Setting the page numbers where regions start and end
Setting to make memory protection effective or ineffective in individual regions	A V (valid) bit in each region-n end page number register (REPAGEn) makes the settings effective or ineffective for the corresponding region (n = 0 to 7).
Access-control information settings for individual regions	Instruction execution: Permission to execute Operand access: Permission to read, permission to write
Start of memory-protection operations	After the memory-protection unit has been enabled, access monitoring starting up with the transition to user mode.
Memory-protection error processing	Generation of access exceptions
Addresses where memory-protection errors are generated	Address in instruction execution: The PC value is preserved on the stack. Address in operand access: The address is stored in the data memory-protection error address register (MPDEA).
Determining the reasons for memory-protection errors	The memory-protection error status register (MPESTS) holds indicators of the reason.
Background region setting	Access-control information can be set for the background region (the whole address space).
Processing where regions overlap	The access-control information for access to an overlap between regions is the logical OR of the attributes for the given regions, and permission is given priority.

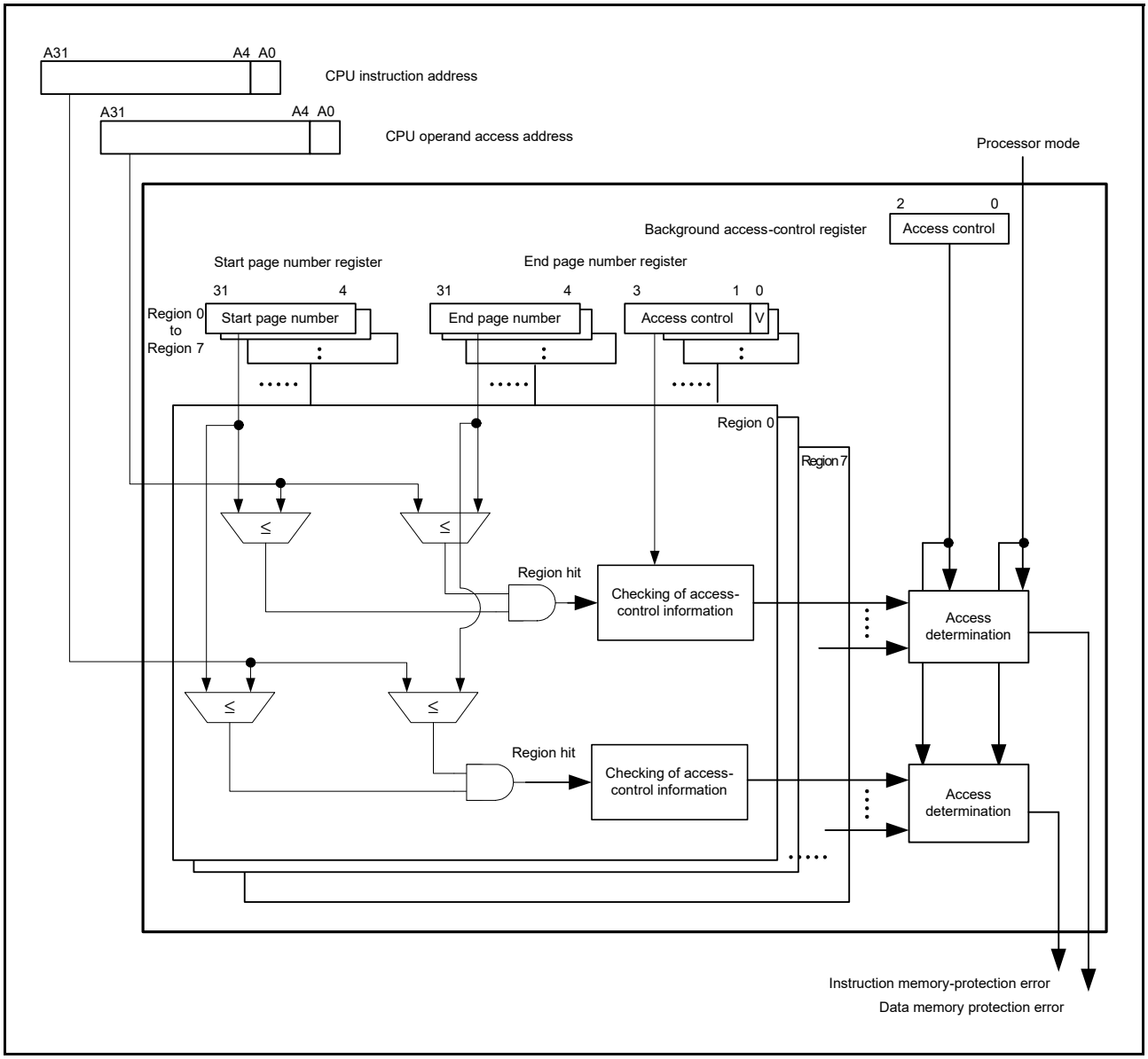


Figure 16.1 Block Diagram of the Memory-Protection Unit

16.1.1 Types of Access Control

There are three types of access control information: permission for instruction execution, permission to read operands, and permission to write operands. Violations of these types of access control are only detected when programs are running in user mode. Violations are not detected when programs are running in supervisor mode.

16.1.2 Regions for Access Control

Up to eight regions for access control are definable. Settings of the range of memory for each access-control region are made in the corresponding region-n start page number register (RSPAGEn) and region-n end page number register (REPAGEn), where n = 0 to 7.
The minimum unit for control of access is the “page”, by which the address space is divided into 16-byte units. The 28 higher-order bits ([31:4]) of the address [31:0] bits correspond to the page number.
The REPAGEn register specifies the access-control information for each area and whether the area is enabled or not.

16.1.3 Background Region

“Background region” refers to the whole address space (0000 0000h to FFFF FFFFh). Access-control information for the background region is set in the background-region access-control register (MPBAC). In contrast to the access-control information for the eight individual regions, protection information for the background region is effective as long as memory protection is enabled (the MPEN bit in the MPEN register is 1).

16.1.4 Overlap between Regions

In cases of overlap between multiple regions, the access-control information becomes the logical OR of the access-control bits for the overlapping regions (including the background region), with permission given priority.

16.1.5 Instructions and Data that Span Regions

Operations in response to the detection of memory-protection errors when instructions or data span regions for which different access-control settings have been made are undefined. Ensure that instructions and data do not span regions for which different access-control settings have been made.

16.2 Register Descriptions

16.2.1 Region-n Start Page Number Register (RSPAGEn) (n = 0 to 7)

Address(es): RSPAGE0 0008 6400h, RSPAGE1 0008 6408h, RSPAGE2 0008 6410h, RSPAGE3 0008 6418h, RSPAGE4 0008 6420h, RSPAGE5 0008 6428h, RSPAGE6 0008 6430h, RSPAGE7 0008 6438h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	RSPN[27:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RSPN[27:0]												—	—	—	—
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Function	R/W
b3 to b0	—	Reserved	The read value is 0. The write value should always be 0	R/W
b31 to b4	RSPN[27:0]	Region-Start Page Number	Page number where the region starts, for use in region determination	R/W

RSPN[27:0] Bits (Region-Start Page Number)

These bits specify the page number where the region starts.

16.2.2 Region-n End Page Number Register (REPAGEn) (n = 0 to 7)

Address(es): REPAGE0 0008 6404h, REPAGE1 0008 640Ch, REPAGE2 0008 6414h, REPAGE3 0008 641Ch, REPAGE4 0008 6424h, REPAGE5 0008 642Ch, REPAGE6 0008 6434h, REPAGE7 0008 643Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	REPN[27:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	REPN[27:0]												UAC[2:0]			V
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Function	R/W
b0	V	Valid Bit	0: Region setting invalid 1: Region setting valid	R/W
b3 to b1	UAC[2:0]	Access Control Bits in User Mode	b3 0: Reading prohibited 1: Reading permitted b2 0: Writing prohibited 1: Writing permitted b1 0: Execution prohibited 1: Execution permitted	R/W
b31 to b4	REPN[27:0]	Region-End Page Number	Page number where the region ends, for use in region determination	R/W

V Bit (Valid Bit)

This bit enables or disables the settings for the corresponding region.
This bit is cleared to 0 when the region invalidation operation register (MPOPI) invalidates all access-controlled areas.

UAC[2:0] Bits (Access Control Bits in User Mode)

These bits specify the access control in user mode.

REPN[27:0] Bits (Region-End Page Number)

These bits specify the page number where the region ends.
Specify a value that is greater than or equal to the page number where the corresponding region starts. The page specified by the region-end page number is part of the target region for memory protection.

16.2.3 Memory-Protection Enable Register (MPEN)

Address(es): 0008 6500h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MPEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	MPEN	Memory-Protection Enable	1: The memory protection is enabled 0: The memory protection is disabled	R/W
b31 to b1	—	Reserved	The read value is 0. The write value should always be 0	R/W

MPEN Bit (Memory-Protection Enable)

This bit enables or disables the memory protection.

After 1 has been written to this bit, address checking for memory protection by the CPU starts on the execution of a branch instruction (RTE or RTFI) that shifts operation to the user mode.

16.2.4 Background Access Control Register (MPBAC)

Address(es): 0008 6504h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	UBAC[2:0]			—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	The read value is 0. The write value should always be 0	R/W
b3 to b1	UBAC[2:0]	Background Access Control Bits in User Mode	b3 0: Reading prohibited 1: Reading permitted b2 0: Writing prohibited 1: Writing permitted b1 0: Execution prohibited 1: Execution permitted	R/W
b31 to b4	—	Reserved	The read value is 0. The write value should always be 0	R/W

UBAC[2:0] Bits (Background Access Control Bits in User Mode)

These bits specify the background access control in user mode.

16.2.5 Memory-Protection Error Status-Clearing Register (MPECLR)

Address(es): 0008 6508h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CLR	Error Status-Clearing	[Reading] 0: Fixed value for reading [Writing] 0: Nothing is done. 1: The DRW, DMPER and IMPER bits in MPESTS are cleared to 0	R/W
b31 to b1	—	Reserved	The read value is 0. The write value should always be 0	R/W

CLR Bit (Error Status-Clearing)

This bit clears the data read/write bit (DRW), the data memory-protection error generation bit (DMPER), and the instruction memory-protection error generation bit (IMPER) in the memory-protection error status register (MPESTS) to 0.

16.2.6 Memory-Protection Error Status Register (MPESTS)

Address(es): 0008 650Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	DRW	DMPER	IMPER
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMPER	Instruction Memory-Protection Error Generation	0: No instruction memory-protection error was generated 1: Instruction memory-protection error was generated	R
b1	DMPER	Data Memory-Protection Error Generation	0: No data memory-protection error was generated 1: Data memory-protection error was generated	R
b2	DRW	Data Read/Write	0: Data were read 1: Data were written	R
b31 to b3	—	Reserved	The read value is 0. The write value should always be 0	R/W

IMPER Bit (Instruction Memory-Protection Error Generation)

This bit indicates the state of memory-protection error generation by instruction execution.

Setting the error status-clearing bit (CLR) in the memory-protection error status-clearing register (MPECLR) to 1 clears this bit to 0.

DMPER Bit (Data Memory-Protection Error Generation)

This bit indicates the state of memory-protection error generation by operand access.

Setting the error status-clearing bit (CLR) in the memory-protection error status-clearing register (MPECLR) to 1 clears this bit to 0.

DRW Bit (Data Read/Write)

For a memory-protection error produced by operand access, this bit indicates the read/write attribute of the access operation. This bit is only valid when the DMPER bit is 1.

Setting the error status-clearing bit (CLR) in the memory-protection error status-clearing register (MPECLR) to 1 clears this bit to 0.

16.2.7 Data Memory-Protection Error Address Register (MPDEA)

Address(es): 0008 6514h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	DEA[31:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DEA[31:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Function	R/W
b31 to b0	DEA[31:0]	Data Memory-Protection Error Address	Data memory-protection error address	R

DEA[31:0] Bits (Data Memory-Protection Error Address)

These bits retain the address for which operand access generated a memory-protection error.

16.2.8 Region Search Address Register (MPSA)

Address(es): 0008 6520h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	SA[31:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SA[31:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Function	R/W
b31 to b0	SA[31:0]	Region Search Address	Address for region searching	R/W

SA[31:0] Bits (Region Search Address)

These bits specify the address for use in comparison with region-start addresses in the region-n start page number registers (RSPAGEn) and region-end addresses in the region-n end page number registers (REPAGEn).

16.2.9 Region Search Operation Register (MPOPS)

Address(es): 0008 6524h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	S
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	S	Region Search Operation	[Reading] 0: Fixed value for reading [Writing] 0: Nothing is done. 1: A region-search operation proceeds	R/W
b15 to b1	—	Reserved	The read value is 0. The write value should always be 0	R/W

S Bit (Region Search Operation)

Setting this bit to 1 makes the memory-protection unit perform a region-search operation. The address specified in the region search address register (MPSA) is compared with the address information for individual regions to search for a hitting region.

The result of searching is stored in the data-hit region bits (HITD[7:0]) of the data-hit region register (MHITD). Moreover, the logical OR of the respective access control bits for hitting regions is stored in the data-hit region access control bits (UHACD[2:0]) in user mode.

16.2.10 Region Invalidation Operation Register (MPOPI)

Address(es): 0008 6526h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	INV
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INV	Region Invalidate Start	[Reading] 0: Fixed value for reading [Writing] 0: Nothing is done 1: All access-controlled areas are invalidated	R/W
b15 to b1	—	Reserved	The read value is 0. The write value should always be 0	R/W

INV Bit (Region Invalidate Start)

Setting this bit to 1 clears the valid (V) bits in all of the region-n end page number registers (REPAGEn) to 0. After a V bit is cleared to 0, all settings other than background access-control settings are invalid.

16.2.11 Instruction-Hit Region Register (MHITI)

Address(es): 0008 6528h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	HITI[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	UHACI[2:0]			—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	The read value is 0. The write value should always be 0	R/W
b3 to b1	UHACI[2:0]	Instruction-Hit Region Access Control Bits in User Mode	b3 0: Reading prohibited 1: Read permitted b2 0: Writing prohibited 1: Writing permitted b1 0: Execution prohibited 1: Execution is permitted	R
b15 to b4	—	Reserved	The read value is 0. The write value should always be 0	R/W
b23 to b16	HITI[7:0]	Instruction-Hit Region	When the instruction memory-protection error generation bit (MPESTS.IMPER) = 1, [b23:b16] = 0000 0000b indicates that attempted access to the background region led to an instruction memory-protection error. Other than above b23 0: Instruction memory-protection error was not generated in region 7 1: Instruction memory-protection error was generated in region 7 b22 0: Instruction memory-protection error was not generated in region 6 1: Instruction memory-protection error was generated in region 6 b21 0: Instruction memory-protection error was not generated in region 5 1: Instruction memory-protection error was generated in region 5 b20 0: Instruction memory-protection error was not generated in region 4 1: Instruction memory-protection error was generated in region 4 b19 0: Instruction memory-protection error was not generated in region 3 1: Instruction memory-protection error was generated in region 3 b18 0: Instruction memory-protection error was not generated in region 2 1: Instruction memory-protection error was generated in region 2 b17 0: Instruction memory-protection error was not generated in region 1 1: Instruction memory-protection error was generated in region 1 b16 0: Instruction memory-protection error was not generated in region 0 1: Instruction memory-protection error was generated in region 0	R
b31 to b24	—	Reserved	The read value is 0. The write value should always be 0	R/W

UHACI[2:0] Bits (Instruction-Hit Region Access Control Bits in User Mode)

These bits hold the user-mode access control bits (REPAGEn.UAC[2:0]) for the region where the instruction memory-protection error was generated.

If the error was generated in an overlap between regions, the value stored here is the logical OR of the user-mode access control bits for the corresponding regions (including the background region).

HITI[7:0] Bits (Instruction-Hit Region)

These bits indicate the region where an instruction memory-protection error was generated. These bits are set to 0000 0000b in response to the generation of an instruction memory-protection error in the background region.

16.2.12 Data-Hit Region Register (MHITD)

Address(es): 0008 652Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	HITD[7:0]							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	UHACD[2:0]			—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	The read value is 0. The write value should always be 0	R/W
b3 to b1	UHACD[2:0]	Data-Hit Region Access Control Bits in User Mode	b3 0: Reading prohibited 1: Reading permitted b2 0: Writing prohibited 1: Writing permitted b1 0: Execution prohibited 1: Execution permitted	R
b15 to b4	—	Reserved	The read value is 0. The write value should always be 0	R/W
b23 to b16	HITD[7:0]	Data-Hit Region	When the data memory-protection error generation bit (MPESTS.DMPER) = 1, [b23:b16] = 0000 0000b indicates that attempted access to the background region led to a data memory-protection error Other than above b23 0: Neither a data memory-protection error nor a search hit was generated in region 7 1: A data memory-protection error or search hit was generated in region 7 b22 0: Neither a data memory-protection error nor a search hit was generated in region 6 1: A data memory-protection error or search hit was generated in region 6 b21 0: Neither a data memory-protection error nor a search hit was generated in region 5 1: A data memory-protection error or search hit was generated in region 5 b20 0: Neither a data memory-protection error nor a search hit was generated in region 4 1: A data memory-protection error or search hit was generated in region 4 b19 0: Neither a data memory-protection error nor a search hit was generated in region 3 1: A data memory-protection error or search hit was generated in region 3 b18 0: Neither a data memory-protection error nor a search hit was generated in region 2 1: A data memory-protection error or search hit was generated in region 2 b17 0: Neither a data memory-protection error nor a search hit was generated in region 1 1: A data memory-protection error or search hit was generated in region 1 b16 0: Neither a data memory-protection error nor a search hit was generated in region 0 1: A data memory-protection error or search hit was generated in region 0	R

Bit	Symbol	Bit Name	Function	R/W
b31 to b24	—	Reserved	The read value is 0. The write value should always be 0	R/W

UHACD[2:0] Bits (Data-Hit Region Access Control Bits in User Mode)

These bits hold the user-mode access control bits (REPAGEn.UAC[2:0]) that have been set for the region where a data memory-protection error was generated or the region that produced a hit in region searching.
When an error is generated in an overlap between regions or a hit was generated in region searching, the value stored here is the logical OR of the user-mode access control bits for the corresponding regions (including the background region).

HITD[7:0] Bits (Data-Hit Region)

These bits indicate the region where a data memory-protection error was generated or the region that produced a hit in a region search. These bits are set to 0000 0000b for a data memory-protection error generated in the background region.

Note: When access to a register of memory protection unit in user mode generates a data memory-protection error, the value in this register is cleared to 0000 0000h.

16.3 Functions

16.3.1 Memory Protection

Memory protection means monitoring, in accord with the access-control information that has been set for the individual access-control regions and the background region, whether or not access by programs running in user mode violates the access-control settings. The memory-protection unit notifies the CPU of access-control violations (or memory-protection errors) when they are detected, causing the CPU to start access-exception processing.
Memory protection is enabled by setting the memory-protection enable (MPEN) bit in the memory-protection enable (MPEN) register to 1.
An instruction memory-protection error is generated on detection of an instruction-execution violation and a data memory-protection error is generated on detection of an operand-access reading or writing violation. Operand access that leads to a data memory-protection error is not actually executed.

16.3.2 Region Search

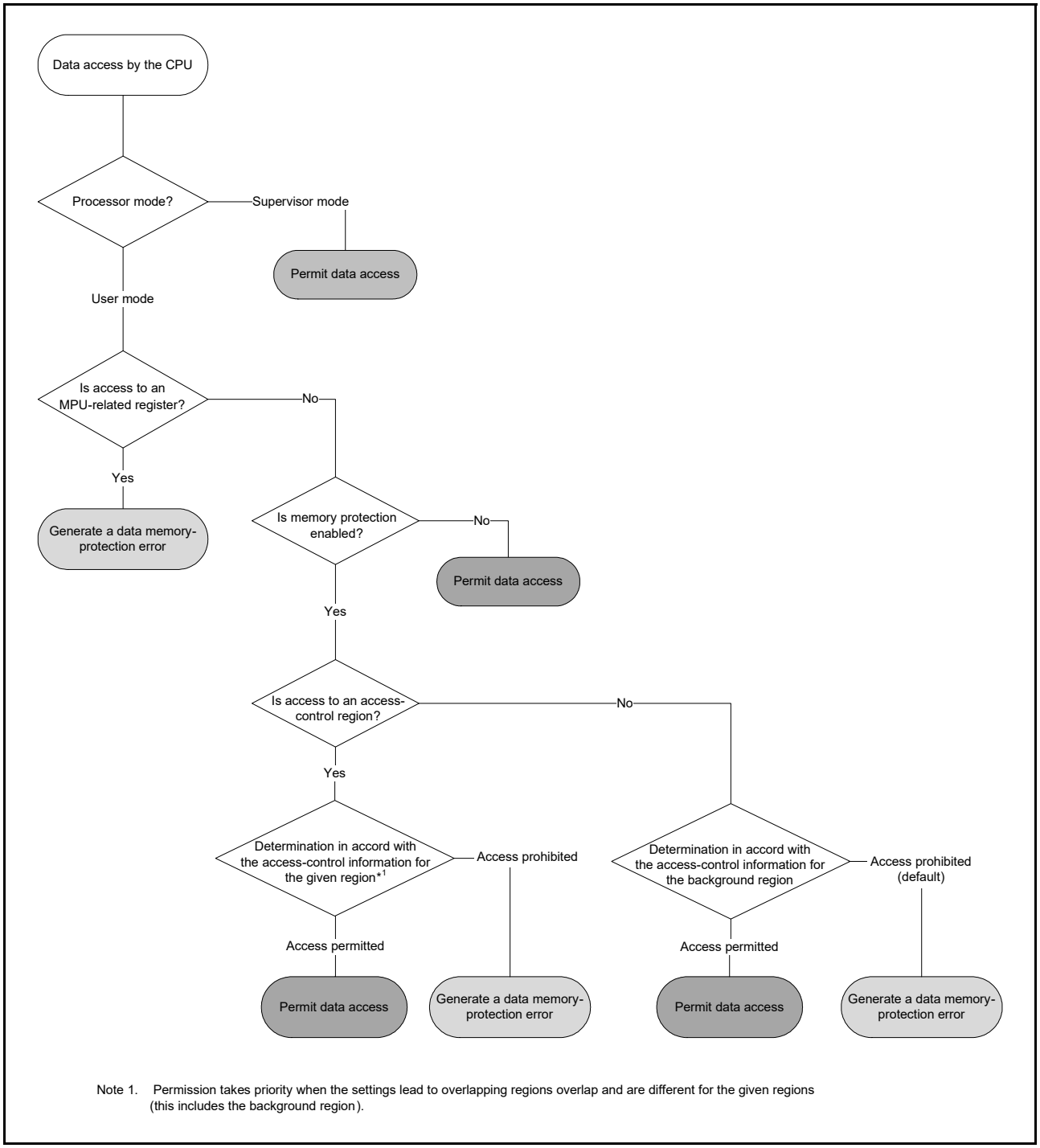
Region search means enquiry as to which of the eight specified access regions was “hit” and how the access-control information (permission to execute, to read, and to write) is set.
When the region search operation (S) bit in the region-search operation (MPOP) register is set to 1, the address specified in the region search address (MPSA) register is compared with the addresses for the individual regions. After a region search is executed, the data-hit region register (MHITD) indicates the logical OR of the access-control information for the region which was “hit” and for the other regions.

16.3.3 Protection of Registers Related to the Memory-Protection Unit

Registers related to the memory-protection unit are not accessible through means of access other than operand access by the CPU (i.e. by instruction fetching or DMA). Attempted access to registers related to the memory-protection unit in user mode through operand access by the CPU leads to a data memory-protection error regardless of whether or not memory protection is in effect at the given location.

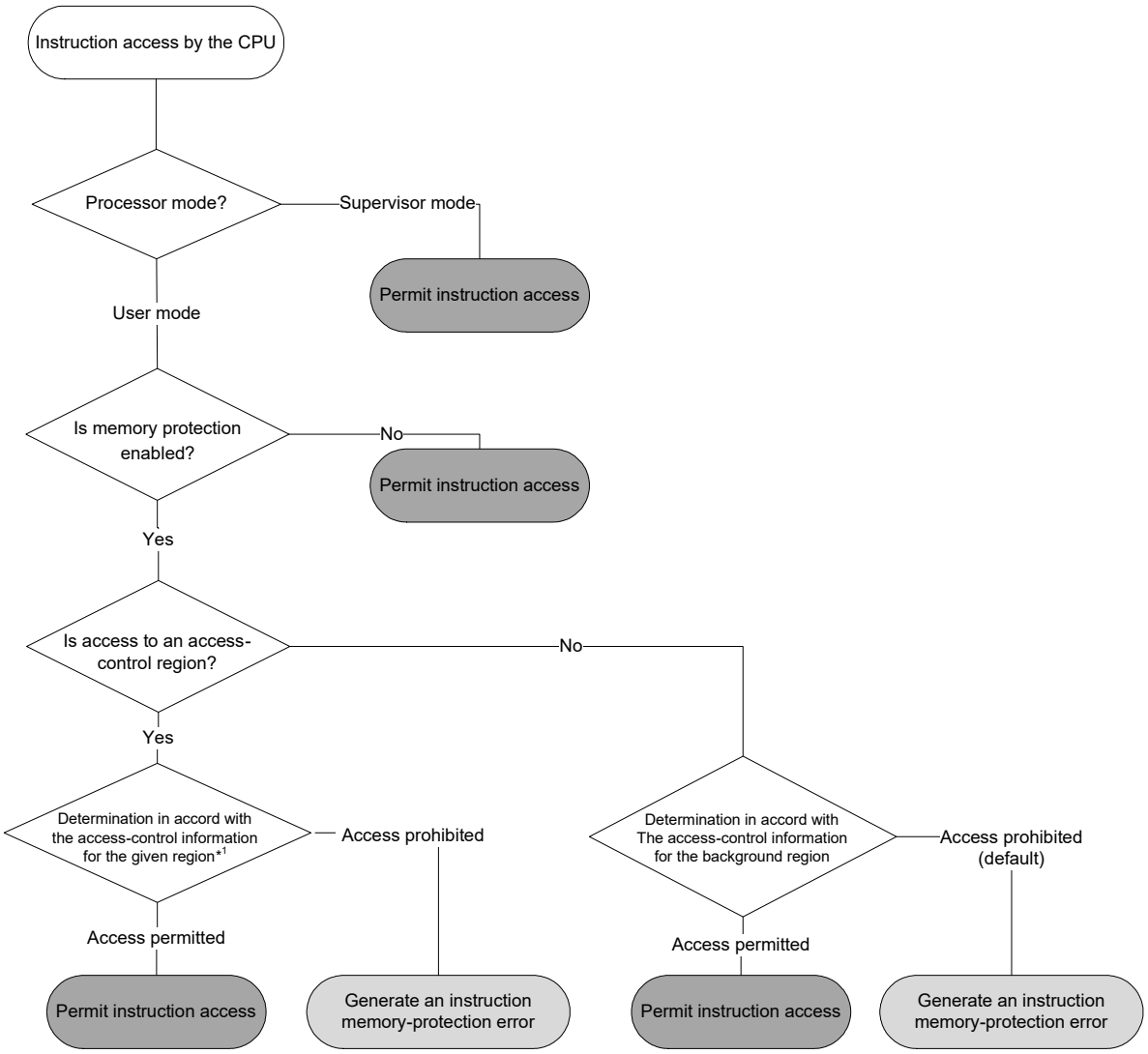
16.3.4 Flow for Determination of Access by the Memory-Protection Function

Figure 16.2 shows the flow of determination in the case of data access and Figure 16.3 shows the flow of determination in the case of instruction access.



Note 1. Permission takes priority when the settings lead to overlapping regions overlap and are different for the given regions (this includes the background region).

Figure 16.2 Flow of Determination for Data Access



Note 1. Permission takes priority when the settings lead to overlapping regions overlap and are not the same for the given regions (this includes the background region).

Figure 16.3 Flow of Determination for Instruction Access

16.4 Procedures for Using Memory Protection

16.4.1 Setting Access-Control Information

Access-control information for the various regions is set in supervisor mode.
Settings for up to eight access-control regions are made in the region-n start page number registers (RSPAGEn) and region-n end page number registers (REPAGEn), where n = 0 to 7.
Settings for the background access-control region are made in the background access-control register (MPBAC).

16.4.2 Enabling Memory Protection

Setting the memory-protection enable (MPEN) bit in the memory-protection enable (MPEN) register to 1 while operation is in supervisor mode enables memory protection.

16.4.3 Transition to User Mode

After updating the registers related to the memory-protection unit, please be sure to read any of these registers and check that the settings have been made and execute an operation using the value read before the transition to user mode.
Either of the methods below can be used for the transition from supervisor mode to user mode.

- Set the processor mode setting (PM) bit in the copy of the processor status word (PSW) saved in the stack area to 1 (the setting for user mode) and then execute an RTE instruction.
- Set the PM bit in the backup processor status word (BPSW) to 1 and then execute an RTFI instruction.

Note: Using an MVTC or POPC instruction to write to the PSW.PM bit is invalid. Use an RTE or RTFI instruction to update the value of the PSW.PM bit.

The memory-protection unit starts checking instruction-execution access and operand access by the CPU on the transition to user mode.

16.4.4 Processing in Response to Memory-Protection Errors

The CPU starts access-exception processing on detection of a violation of protection set up by the access-control information (i.e. a memory-protection error). For details on CPU operations in access-exception processing, refer to section 13, Exception Handling.
To determine whether an instruction memory-protection error or data memory-protection error has been generated, check the values of the instruction memory-protection error generation (IMPER) and data memory-protection error generation (DMPER) bits in the memory-protection error status register (MPESTS) from within the exception-processing routine.
After confirming the type of error, clear the memory-protection error status register (MPESTS) by writing 1 to the status clearing (MPE) bit in the memory-protection error status clearing register (MPECLR).

(1) When a data memory-protection error is generated

Access-exception processing by the CPU saves the address of the instruction that led to the memory-protection error on the stack. Furthermore, the address of the operand for which access led to a memory-protection error is stored in the data memory-protection error address register (MPDEA) and the region information for the region where the memory-protection error was generated is stored in the data-hit region register (MHITD).

- Violations of access control in access to valid regions 0 to 7

The data-hit region bits (MHITD.HITD[7:0]) with the same region number as the region where the error occurred is set to 1. In user mode, the logical “or” of the region access-control information for the location where the error occurred is set in the data-hit region access-control bits (MHITD.UHACD[2:0]).

- Violations of access control for the background region, besides access to outside valid regions 0 to 7

The data-hit region bits (MHITD.HITD[7:0]) are set to 0000 0000b. In user mode, the access-control information for the background region is set in the data-hit region access-control bits (MHITD.UHACD[2:0]).

Referring to this information can pinpoint the sources of errors.

(2) When an instruction memory-protection error is generated

Access-exception processing by the CPU saves the address of the instruction that led to the memory-protection error on the stack. Furthermore, the region information for the region where the memory-protection error was generated is stored in the instruction-hit region register (MHITI).

- Violations of access control in access to valid regions 0 to 7

The instruction-hit region bit (MHITD.HITI[7:0]) with the same region number as the region where the error occurred is set to 1. In user mode, the logical “or” of the region access-control information for the location where the error occurred is set in the instruction-hit region access-control bits (MHITI.UHACI[2:0]).

- Violations of access control for the background region, besides access to outside valid regions 0 to 7

The instruction-hit region bits (MHITI.HITI[7:0]) are set to 0000 0000b. In user mode, the access-control information for the background region is set in the instruction-hit region access-control bits (MHITI.UHACI[2:0]).

Referring to this information can pinpoint the sources of errors.

17. Data Transfer Controller (DTCa)

This MCU incorporates a data transfer controller (DTC).
The DTC is triggered by an interrupt request to perform data transfers.

17.1 Overview

Table 17.1 lists the specifications of the DTC, and Figure 17.1 shows a block diagram of the DTC.

Table 17.1 DTC Specifications

Item	Description
Number of transfer channels	• The same number as all interrupt sources that can start the DTC transfer.
Transfer modes	• Normal transfer mode A single transfer request leads to a single data transfer. • Repeat transfer mode A single transfer request leads to a single data transfer. The transfer address is returned to the transfer start address after the number of data transfers corresponding to “repeat size”. The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 × 32 bits, 1024 bytes. • Block transfer mode A single transfer request leads to the transfer of a single block. The maximum block size is 256 × 32 bits = 1024 bytes.
Chain transfer	• Multiple types of data transfers can sequentially be executed in response to a single request. • Either “performed only when the transfer counter becomes 0” or “every time” can be selected.
Transfer space	• In short-address mode: 16 Mbytes (Areas from 0000 0000h to 007F FFFFh and FF80 0000h to FFFF FFFFh except reserved areas) • In full-address mode: 4 Gbytes (Area from 0000 0000h to FFFF FFFFh except reserved areas)
Data transfer units	• Single data: 1 byte (8 bits), 1 word (16 bits), 1 longword (32 bits) • Single block size: 1 to 256 data
CPU interrupt source	• An interrupt request can be generated to the CPU on a request source for a data transfer. • An interrupt request can be generated to the CPU after a single data transfer. • An interrupt request can be generated to the CPU after data transfer of specified volume.
Read skip	Reading of the transfer information can be skipped when the same transfer is repeated.
Write-back skip	Write-back of the transferred data that is not updated can be skipped when the address of the transfer source or destination is fixed.
Low power consumption function	Module stop state can be set.

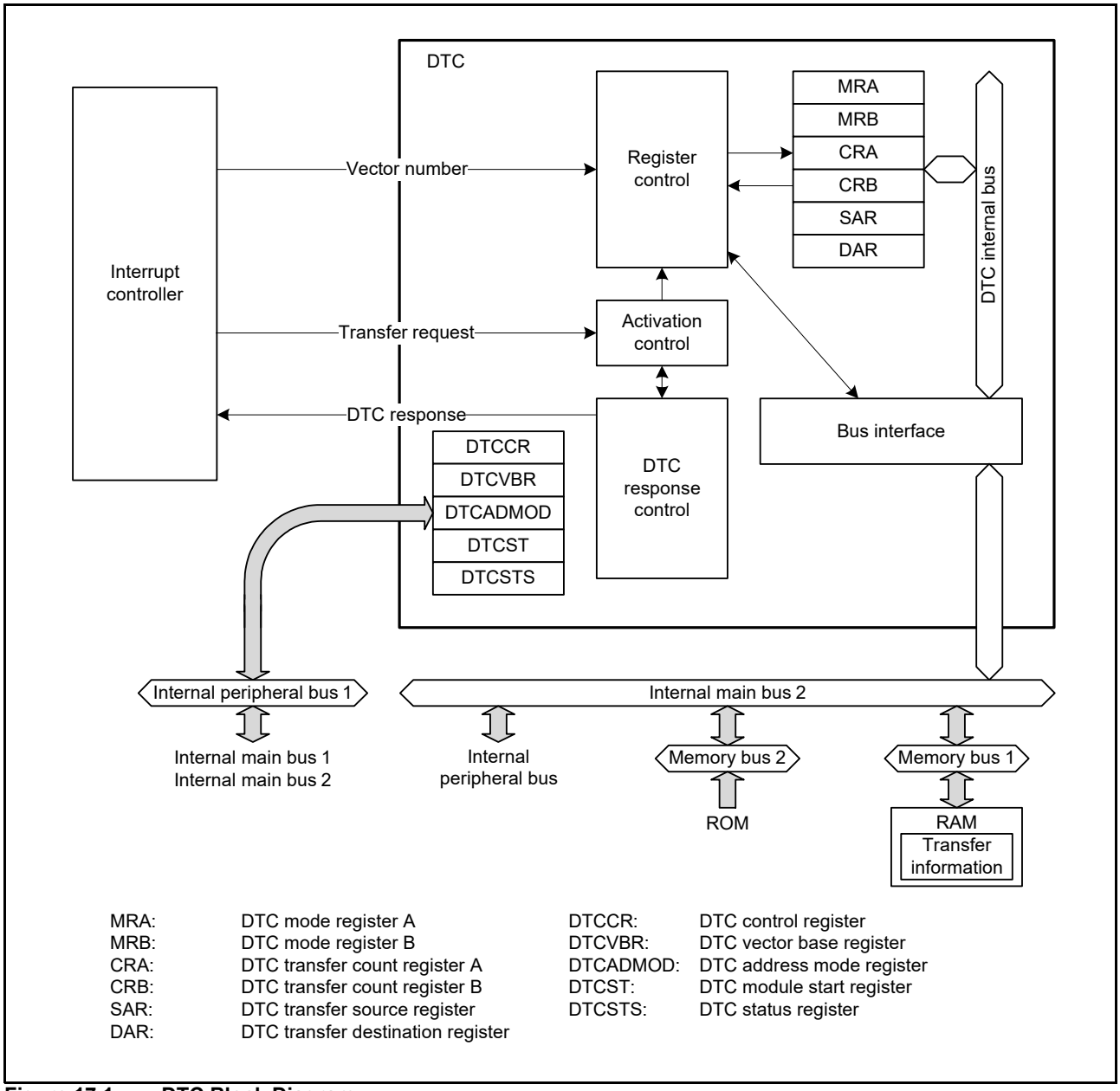


Figure 17.1 DTC Block Diagram

17.2 Register Descriptions

Registers MRA, MRB, SAR, DAR, CRA, and CRB are DTC internal registers, which cannot be directly accessed from the CPU. Values to be set in these DTC internal registers are placed in the RAM area as transfer information. When accepting a transfer request, the DTC reads the transfer information from the RAM area and sets it in the internal registers. After the data transfer ends, the values of the updated internal register are written back to the RAM area as transfer information.

17.2.1 DTC Mode Register A (MRA)

Address(es): (inaccessible directly from the CPU)

	b7	b6	b5	b4	b3	b2	b1	b0
	MD[1:0]		SZ[1:0]		SM[1:0]		—	—
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b1, b0	—	Reserved	Set these bits to 0.	—
b3, b2	SM[1:0]	Transfer Source Address Addressing Mode	b3 b2 0 0: The address in the SAR register is fixed. (write-back to SAR is skipped.) 0 1: The address in the SAR register is fixed. (write-back to SAR is skipped.) 1 0: The SAR value is incremented after a data transfer. (+1 when the SZ[1:0] bits are 00b, +2 when 01b, +4 when 10b) 1 1: The SAR value is decremented after a data transfer. (–1 when the SZ[1:0] bits are 00b, –2 when 01b, –4 when 10b)	—
b5, b4	SZ[1:0]	DTC Data Transfer Size	b5 b4 0 0: Byte (8-bit) transfer 0 1: Word (16-bit) transfer 1 0: Longword (32-bit) transfer 1 1: Setting prohibited	—
b7, b6	MD[1:0]	DTC Transfer Mode Select	b7 b6 0 0: Normal transfer mode 0 1: Repeat transfer mode 1 0: Block transfer mode 1 1: Setting prohibited	—

MRA register is used to select the DTC operating mode and cannot be accessed directly from the CPU.

17.2.2 DTC Mode Register B (MRB)

Address(es): (inaccessible directly from the CPU)

	b7	b6	b5	b4	b3	b2	b1	b0
	CHNE	CHNS	DISEL	DTS	DM[1:0]		—	—
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b1, b0	—	Reserved	Set these bits to 0.	—
b3, b2	DM[1:0]	Transfer Destination Address Addressing Mode	b3 b2 0 0: The address in the DAR register is fixed. (Write-back to DAR is skipped.) 0 1: The address in the DAR register is fixed. (Write-back to DAR is skipped.) 1 0: The DAR value is incremented after data transfer. (+1 when the MRA.SZ[1:0] bits are 00b, +2 when 01b, +4 when 10b) 1 1: The DAR value is decremented after data transfer. (–1 when the SZ[1:0] bits are 00b, –2 when 01b, –4 when 10b)	—
b4	DTS	DTC Transfer Mode Select	0: Transfer destination side is repeat area or block area. 1: Transfer source side is repeat area or block area.	—
b5	DISEL	DTC Interrupt Select	0: An interrupt request to the CPU is generated on completion of the specified number of data transfers. 1: An interrupt request to the CPU is generated for each data transfer.	—
b6	CHNS	DTC Chain Transfer Select	0: Chain transfer is performed on completion of each transfer. 1: Chain transfer is performed only when the transfer counter is changed from 1 to 0 or 1 to CRAH.	—
b7	CHNE	DTC Chain Transfer Enable	0: Chain transfer is disabled. 1: Chain transfer is enabled.	—

MRB register is used to select the DTC operating mode and cannot be accessed directly from the CPU.

DTS Bit (DTC Transfer Mode Select)

The DTS bit specifies the side (transfer source or destination) to be a repeat area or block area in repeat transfer mode or block transfer mode.

CHNS Bit (DTC Chain Transfer Select)

The CHNS bit selects the chain transfer condition.

When the CHNE bit is 0, setting of the CHNS bit is ignored. For details on the conditions to select the chain transfer, refer to Table 17.3, Chain Transfer Conditions.

When the next transfer is chain transfer, completion of the specified number of transfers is not determined, the interrupt status flag for the request source is not cleared, and an interrupt request to the CPU is not generated.

CHNE Bit (DTC Chain Transfer Enable)

The CHNE bit enables or disables chain transfer.

The chain transfer condition is selected by the CHNS bit.

For details of chain transfer, refer to section 17.4.6, Chain Transfer.

17.2.3 DTC Transfer Source Register (SAR)

Address(es): (inaccessible directly from the CPU)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

SAR register is used to set the transfer source start address.
In full-address mode, 32 bits are valid.
In short-address mode, lower 24 bits are valid and upper 8 bits (b31 to b24) are ignored. The address of this register is extended by the value specified by b23.
SAR register cannot be accessed directly from the CPU.

17.2.4 DTC Transfer Destination Register (DAR)

Address(es): (inaccessible directly from the CPU)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

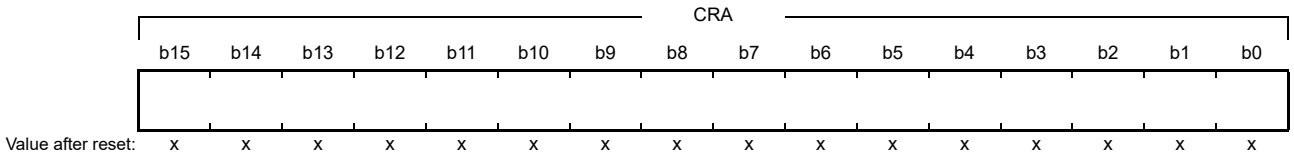
x: Undefined

DAR register is used to set the transfer destination start address.
In full-address mode, 32 bits are valid.
In short-address mode, lower 24 bits are valid and upper 8 bits (b31 to b24) are ignored. The address of this register is extended by the value specified by b23.
DAR register cannot be accessed directly from the CPU.

17.2.5 DTC Transfer Count Register A (CRA)

- Normal transfer mode

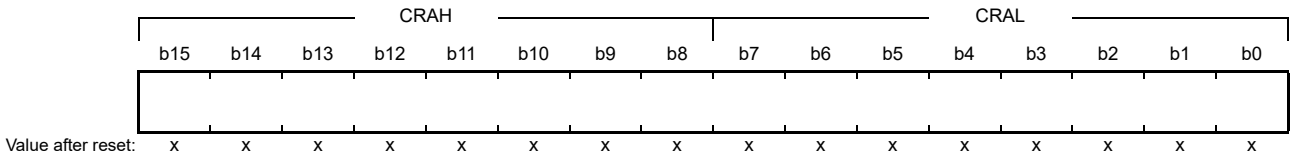
Address(es): (inaccessible directly from the CPU)



x: Undefined

- Repeat transfer mode/block transfer mode

Address(es): (inaccessible directly from the CPU)



x: Undefined

Symbol	Register Name	Description	R/W
CRAL	Transfer Counter A Lower Register	Set transfer count. This register functions as a transfer counter during data transfer.	—
CRAH	Transfer Counter A Upper Register	Set transfer count. This register functions as a reload register during data transfer.	—

Note: The function depends on transfer mode.
Note: Set CRAH and CRAL to the same value in repeat transfer mode and block transfer mode.

This register is for counting the number of transfers and cannot be accessed directly from the CPU.

(1) Normal transfer mode (MRA.MD[1:0] bits = 00b)

CRA register functions as a 16-bit transfer counter in normal transfer mode.
The transfer count is 1, 65535, and 65536 when the set value is 0001h, FFFFh, and 0000h, respectively.
The CRA value is decremented (–1) at each data transfer.

(2) Repeat transfer mode (MRA.MD[1:0] bits = 01b)

The CRAH register retains the transfer count and the CRAL register functions as an 8-bit transfer counter.
The transfer count is 1, 255, and 256 when the set value is 01h, FFh, and 00h, respectively.
The CRAL value is decremented (–1) at each data transfer. When it reaches 00h, the CRAH value is reloaded to the CRAL register.

(3) Block transfer mode (MRA.MD[1:0] bits = 10b)

The CRAH register retains the block size and the CRAL register functions as an 8-bit block size counter.
The transfer count is 1, 255, and 256 when the set value is 01h, FFh, and 00h, respectively.
The CRAL value is decremented (–1) at each data transfer. When it reaches 00h, the CRAH value is reloaded to the CRAL register.

17.2.6 DTC Transfer Count Register B (CRB)

Address(es): (inaccessible directly from the CPU)

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

CRB register is used to set the block transfer count for block transfer mode and cannot be accessed directly from the CPU.
The transfer count is 1, 65535, and 65536 when the set value is 0001h, FFFFh, and 0000h, respectively.
The CRB value is decremented (–1) when the final data of a single block size is transferred.
When normal transfer mode or repeat transfer mode is selected, this register is not used and the set value is ignored.

17.2.7 DTC Control Register (DTCCR)

Address(es): DTC.DTCCR 0008 2400h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	RRS	—	—	—	—
Value after reset:	0	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b3	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b4	RRS	DTC Transfer Information Read Skip Enable	0: Transfer information read is not skipped. 1: Transfer information read is skipped when vector numbers match.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

DTCCR register is used to control the DTC operation.

RRS Bit (DTC Transfer Information Read Skip Enable)

The DTC vector number is compared with the vector number in the previous data transfer.
When these vector numbers match and the RRS bit is set to 1, DTC data transfer is performed without reading the transferred information. However, when the previous transfer was chain transfer, the transferred information is read regardless of the value of the RRS bit.
Furthermore, when the transfer counter (CRA register) became 0 during the previous normal transfer and when the transfer counter (CRB register) became 0 during the previous block transfer, the transferred information is read regardless of the RRS bit value.

17.2.8 DTC Vector Base Register (DTCVBR)

Address(es): DTC.DTCVBR 0008 2404h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The DTCVBR register is used to set the base address for calculating the address to which the DTC vector is allocated. Writing to the upper 4 bits (b31 to b28) is ignored, and the address of this register is extended by the value specified by b27. The lower 10 bits are reserved and the values are fixed to 0. Write 0 to the lower 10 bits if necessary.
It can be set in the range of 0000 0000h to 07FF FC00h and F800 0000h to FFFF FC00h in 1-Kbyte units.

17.2.9 DTC Address Mode Register (DTCADMOD)

Address(es): DTC.DTCADMOD 0008 2408h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	SHORT
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SHORT	Short-Address Mode Set	0: Full-address mode 1: Short-address mode	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

DTCADMOD register is used to specify the area accessible by the DTC.

SHORT Bit (Short-Address Mode Set)

This bit is used to select address mode of registers SAR and DAR.
Full-address mode allows the DTC to access to a 4-Gbyte space (0000 0000h to FFFF FFFFh).
Short-address mode allows the DTC to access to a 16-Mbyte space (0000 0000h to 007F FFFFh and FF80 0000h to FFFF FFFFh).

17.2.10 DTC Module Start Register (DTCST)

Address(es): DTC.DTCST 0008 240Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DTCST
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DTCST	DTC Module Start	0: DTC module stop 1: DTC module start	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

DTCST Bit (DTC Module Start)

Set the DTCST bit to 1 to enable the DTC to accept transfer requests. When this bit is set to 0, transfer requests are no longer accepted.

If this bit is set to 0 during data transfer, the accepted transfer request is active until the processing is completed.

Set the DTCST bit to 0 before making a transition to the module stop state, deep sleep mode, or software standby mode.

Set the DTCST bit to 1 to resume the data transfer after returning from the module stop state, deep sleep mode, or software standby mode.

For details on transitions to the module stop state, deep sleep mode, and software standby mode, refer to section 17.8, Low Power Consumption Function, and section 11, Low Power Consumption.

17.2.11 DTC Status Register (DTCSTS)

Address(es): DTC.DTCSTS 0008 240Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ACT	—	—	—	—	—	—	—	VECN[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	VECN[7:0]	DTC Active Vector Number Monitoring Flag	These bits indicate the vector number for the request source when data transfer is in progress. The value is only valid if data transfer is in progress (the value of the ACT flag is 1).	R
b14 to b8	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R
b15	ACT	DTC Active Flag	0: Data transfer is not in progress. 1: Data transfer is in progress.	R

VECN[7:0] Flags (DTC Active Vector Number Monitoring Flag)

While data transfer is in progress, these bits indicate the vector number corresponding to the request source for the transfer.

When the DTCSTS register is read, the value of the VECN[7:0] flags is valid if the value of the ACT flag was 1 (data transfer is in progress) and invalid if the value of the ACT flag was 0 (data transfer is not in progress).

For the correspondence between the DTC request sources and the vector addresses, refer to section 14.3.1, Interrupt Vector Table in section 14, Interrupt Controller (ICUb).

ACT Flag (DTC Active Flag)

This flag indicates the state of data transfer operation.

[Setting condition]

- When the data transfer is started by a transfer request.

[Clearing condition]

- When the data transfer is completed in response to a transfer request.

17.3 Request Sources

The DTC data transfer is triggered by an interrupt request. Setting the ICU.DTCERn.DTCE bit (n = interrupt vector number) to 1 selects the corresponding interrupt request as a request source for the DTC.
For the correspondence between the DTC request sources and the vector addresses, refer to section 14.3.1, Interrupt Vector Table in section 14, Interrupt Controller (ICUb). For request by software, refer to section 14.2.5, Software Interrupt Generation Register (SWINTR) in section 14, Interrupt Controller (ICUb).
Once the DTC has accepted a transfer request, it does not accept another transfer request until transfer for that single request is completed, regardless of the priority of the requests.
When multiple transfer requests are generated during data transfer by the DTC, the request with the highest priority on completion of the current transfer is accepted. When multiple transfer requests are generated while the DTCST.DTCST bit is 0 (DTC module stop), the request with the highest priority at the moment when the bit is subsequently set to 1 (DTC module start) is accepted.

The DTC performs the following operations at the start of a single data transfer (or the last of the consecutive transfers in the case of a chain transfer).

- On completion of a specified number of data transfer, the ICU.DTCERn.DTCE bit is set to 0 and an interrupt is requested to the CPU.
- If the MRB.DISEL bit is 1, an interrupt is requested to the CPU on completion of data transfer.
- For the other transfers, the interrupt status flag of the request source is set to 0 at the start of data transfer.

17.3.1 Allocating Transfer Information and DTC Vector Table

The DTC reads the start address of the transfer information corresponding to each request source from the vector table and reads the transfer information starting at that address.
The vector table should be located so that the lower 10 bits of the base address (start address) are 0. Use the DTC vector base register (DTCVBR) to set the base address of the DTC vector table.
Transfer information is allocated in the RAM area. The start address of the transfer information n with vector number n should be allocated at DTCVBR + 4n.
Transfer information should be aligned on a 4-byte boundary. The size of a transfer information is 12 bytes in short-address mode or 16 bytes in full-address mode. Use the DTCADMOD.SHORT bit to select short-address mode (SHORT bit = 1) or full-address mode (SHORT bit = 0).
Figure 17.2 shows the relationship between the DTC vector table and transfer information.
Figure 17.3 shows the allocation of transfer information in the RAM area. The lower addresses vary according to the endian of the corresponding allocation area. For details, refer to section 17.9.2, Allocating Transfer Information.

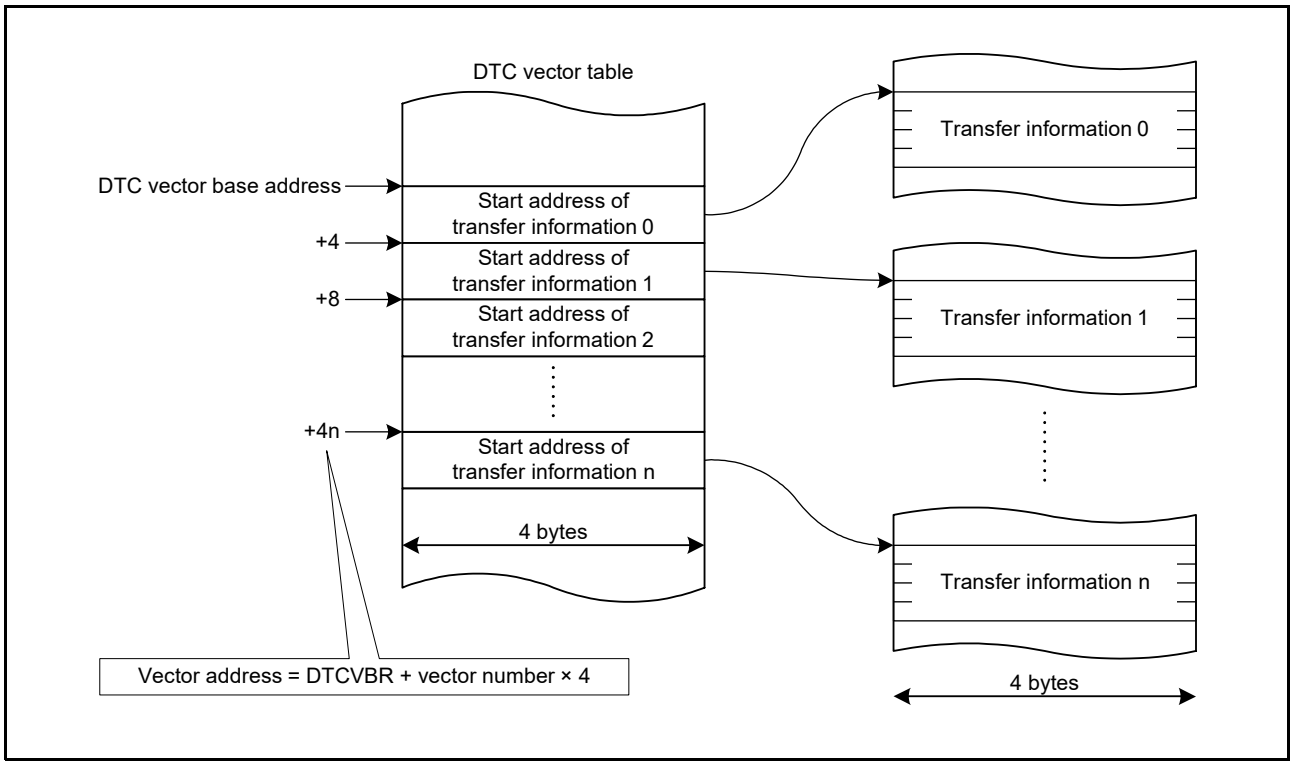


Figure 17.2 DTC Vector Table and Transfer Information

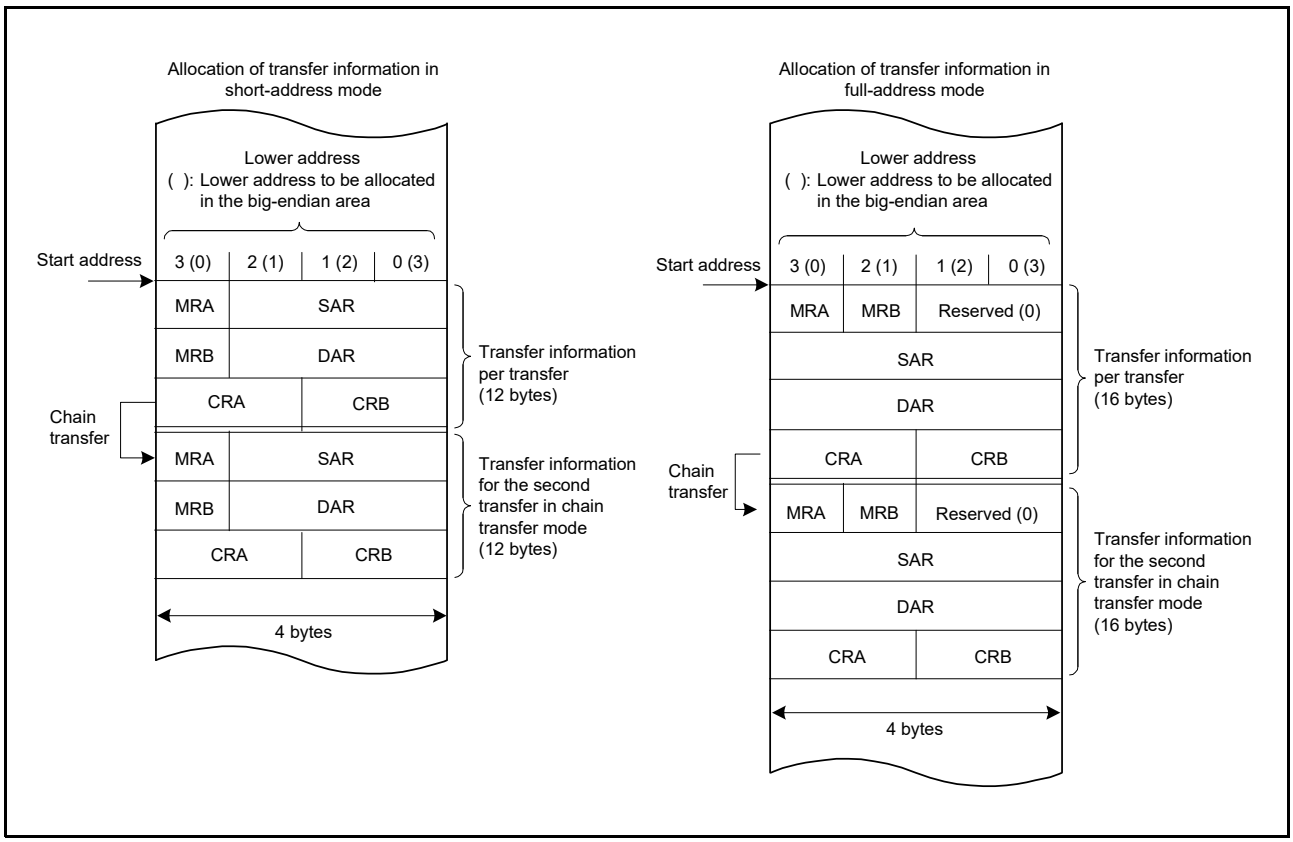


Figure 17.3 Allocation of Transfer Information in the RAM Area

17.4 Operation

The DTC transfers data in accordance with the transfer information. Storage of the transfer information in the RAM area is required before DTC operation.

When the DTC accepts a transfer request, it reads the DTC vector corresponding to the vector number. Next, the DTC reads transfer information from the address pointed by the DTC vector, transfers data, and then writes back the transfer information after the data transfer. Allocating transfer information in the RAM area allows data transfer of arbitrary number of channels.

There are three transfer modes: normal transfer mode, repeat transfer mode, and block transfer mode.

Set a transfer source address in the SAR register and a transfer destination address in the DAR register. The SAR and DAR registers are updated after the transfer according to the respective settings (increment, decrement, or fixed).

Table 17.2 lists transfer modes of the DTC.

Table 17.2 Transfer Modes of the DTC

Transfer Mode	Data Size Transferred on Single Transfer Request	Increment/Decrement of Memory Address	Settable Transfer Count
Normal transfer mode	1 byte/1 word/1 longword	Incremented/decremented by 1, 2, or 4 or address fixed	1 to 65536
Repeat transfer mode*1	1 byte/1 word/1 longword	Incremented/decremented by 1, 2, or 4 or address fixed	1 to 256*3
Block transfer mode*2	Block size specified in CRAH (1 to 256 bytes/1 to 256 words/1 to 256 longwords)	Incremented/decremented by 1, 2, or 4 or address fixed	1 to 65536

Note 1. Set transfer source or transfer destination in the repeat area.
Note 2. Set transfer source or transfer destination in the block area.
Note 3. After data transfer of the specified count, the initial state is restored and the operation is continued (repeated).

Setting the MRB.CHNE bit to 1 allows multiple transfers (chain transfer) on a single transfer request. The setting in combination with the MRB.CHNS bit enables a chain transfer when the specified number of data transfers is completed.

Figure 17.4 shows the operation flowchart of the DTC. Table 17.3 lists chain transfer conditions.

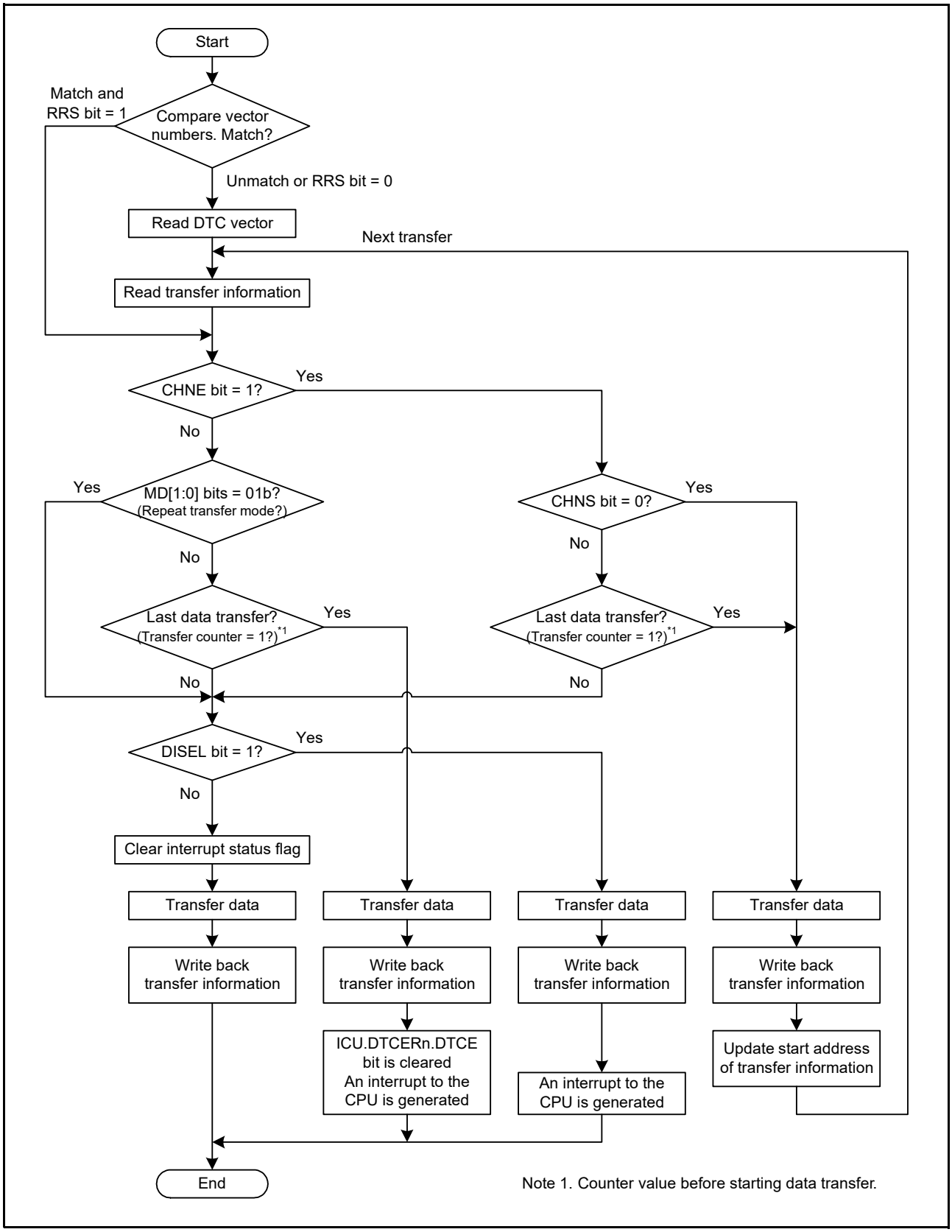


Figure 17.4 Operation Flowchart of the DTC

Table 17.3 Chain Transfer Conditions

First Transfer				Second Transfer*3				
CHNE Bit	CHNS Bit	DISEL Bit	Transfer Counter*1,*2	CHNE Bit	CHNS Bit	DISEL Bit	Transfer Counter*1,*2	Data Transfer
0	—	0	Other than (1 → 0)	—	—	—	—	Ends after the first transfer
0	—	0	(1 → 0)	—	—	—	—	Ends after the first transfer with an interrupt request to the CPU
0	—	1	—	—	—	—	—	
1	0	—	—	0	—	0	Other than (1 → 0)	Ends after the second transfer
				0	—	0	(1 → 0)	Ends after the second transfer with an interrupt request to the CPU
				0	—	1	—	
1	1	0	Other than (1 → ∗)	—	—	—	—	Ends after the first transfer
1	1	—	(1 → ∗)	0	—	0	Other than (1 → 0)	Ends after the second transfer
				0	—	0	(1 → 0)	Ends after the second transfer with an interrupt request to the CPU
				0	—	1	—	
1	1	1	Other than (1 → ∗)	—	—	—	—	Ends after the first transfer with an interrupt request to the CPU

Note 1. The transfer counters used depend on transfer modes as follows:
Normal transfer mode: CRA register
Repeat transfer mode: CRAL register
Block transfer mode: CRB register

Note 2. On completion of data transfer, the counters operate as follows:
1 → 0 in normal and block transfer modes
1 → CRAH in repeat transfer mode
(1 → ∗) in the table indicates both of the two operations above.

Note 3. Chain transfer can be selected for the second or subsequent transfers. The condition combination of “second transfer and the CHNE bit is 1” is omitted.

17.4.1 Transfer Information Read Skip Function

Reading of DTC vector and transfer information can be skipped by the setting of the DTCCR.RRS bit.

When a DTC transfer request is accepted, the current DTC vector number is compared with the DTC vector number in the previous data transfer. When these vector numbers match and the RRS bit is 1, the DTC does not read the DTC vector and transfer information, and transfers data according to the transfer information remained in the DTC.

However, when the previous transfer was chain transfer, the DTC vector and transfer information are read. Furthermore, when the transfer counter (CRA register) became 0 during the previous normal transfer and when the transfer counter (CRB register) became 0 during the previous block transfer, transfer information is read regardless of the value of the RRS bit. Figure 17.13 shows an example of transfer information read skip.

When updating the vector table and transfer information, set the RRS bit to 0, update the vector table and transfer information, and then set the RRS bit to 1. Setting the RRS bit to 0 discards the vector numbers retained in the DTC. The updated DTC vector table and transfer information are read in the next data transfer.

17.4.2 Transfer Information Write-Back Skip Function

When the MRA.SM[1:0] bits or the MRB.DM[1:0] bits are set to “address is fixed” (00b or 01b), a part of transfer information is not written back. This function is performed independently of the setting of short-address mode or full-address mode.

Table 17.4 lists transfer information write-back skip conditions and applicable registers. The CRA and CRB registers are written back independently of the setting of short-address mode or full-address mode.

Furthermore, in full-address mode, write-back of registers MRA and MRB is skipped.

Table 17.4 Transfer Information Write-Back Skip Conditions and Applicable Registers

MRA.SM[1:0] Bits		**MRB.DM[1:0] Bits**			
b3	b2	b3	b2	**SAR Register**	**DAR Register**
0	0	0	0	Skip	Skip
0	0	0	1		
0	1	0	0		
0	1	0	1		
0	0	1	0	Skip	Write-back
0	0	1	1		
0	1	1	0		
0	1	1	1		
1	0	0	0	Write-back	Skip
1	0	0	1		
1	1	0	0		
1	1	0	1		
1	0	1	0	Write-back	Write-back
1	0	1	1		
1	1	1	0		
1	1	1	1		

17.4.3 Normal Transfer Mode

This mode allows 1-byte, 1-word, or 1-longword data transfer on a single transfer request. The transfer count can be set to 1 to 65536.

Transfer source addresses and transfer destination addresses can be set to increment, decrement, or fixed independently.

This mode enables an interrupt request to the CPU to be generated at the end of specified-count transfer.

Table 17.5 lists register functions in normal transfer mode, and Figure 17.5 shows the memory map of normal transfer mode.

Table 17.5 Register Functions in Normal Transfer Mode

Register	Description	Value Written Back by Writing Transfer Information
SAR	Transfer source address	Increment/decrement/fixed*1
DAR	Transfer destination address	Increment/decrement/fixed*1
CRA	Transfer counter A	CRA – 1
CRB	Transfer counter B	Not updated

Note 1. Write-back operation is skipped when address is fixed.

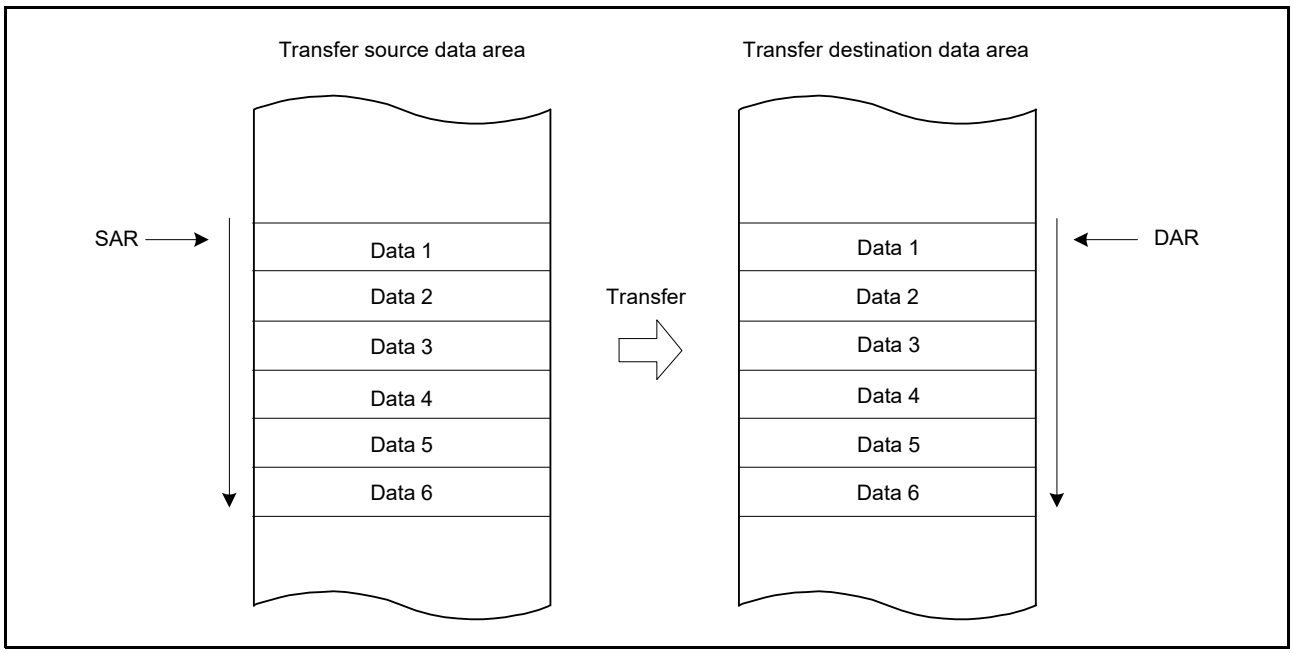


Figure 17.5 Memory Map of Normal Transfer Mode

17.4.4 Repeat Transfer Mode

This mode allows 1-byte, 1-word, or 1-longword data transfer on a single transfer request.
Specify either transfer source or transfer destination for the repeat area by the MRB.DTS bit. The transfer count can be set to 1 to 256. When the specified-count transfer is completed, the initial value of the address register specified in the transfer counter and the repeat area is restored and transfer is repeated. The other address register is incremented or decremented continuously or remains unchanged.
When the transfer counter CRAL is decreased to 00h in repeat transfer mode, the CRAL value is updated to the value set in the CRAH register. Thus the transfer counter does not become 00h, which disables an interrupt request to be generated to the CPU when the MRB.DISEL bit is set to 0 (an interrupt request to the CPU is generated on completion of the specified number of data transfers).
Table 17.6 lists the register functions in repeat transfer mode, and Figure 17.6 shows the memory map of repeat transfer mode.

Table 17.6 Register Functions in Repeat Transfer Mode

		Value Written Back by Writing Transfer Information		
			When CRAL = 1	
Register	**Description**	**When CRAL ≠ 1**	**When the MRB.DTS bit is 0**	**When the MRB.DTS bit is 1**
SAR	Transfer source address	Increment/decrement/fixed*1	Increment/decrement/fixed*1	SAR register initial value
DAR	Transfer destination address	Increment/decrement/fixed*1	DAR register initial value	Increment/decrement/fixed*1
CRAH	Retains initial value of transfer counter	CRAH	CRAH	
CRAL	Transfer counter A	CRAL – 1	CRAH	
CRB	Transfer counter B	Not updated	Not updated	

Note 1. Write-back operation is skipped when address is fixed.

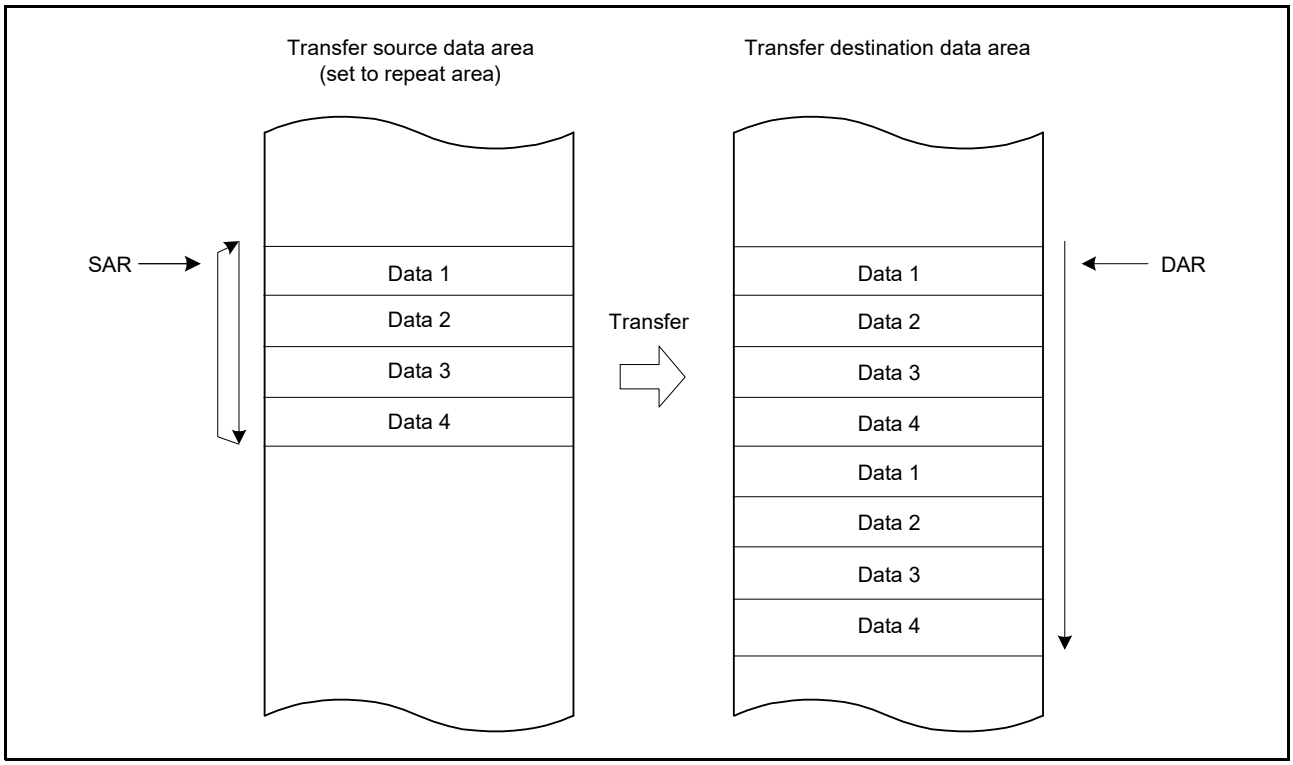


Figure 17.6 Memory Map of Repeat Transfer Mode (Transfer Source: Repeat Area)

17.4.5 Block Transfer Mode

This mode allows single-block data transfer on a single transfer request.
Specify either transfer source or transfer destination for the block area by the MRB.DTS bit. The block size can be set to 1 to 256 bytes, 1 to 256 words, or 1 to 256 longwords.
When transfer of the specified one block is completed, the initial values of the block size counter CRAL and the address register (the SAR register when the MRB.DTS bit is 1 or the DAR register when the DTS bit is 0) specified in the block area are restored. The other address register is incremented or decremented continuously or remains unchanged.
The transfer count (block count) can be set to 1 to 65536. This mode enables an interrupt request to the CPU to be generated at the end of specified-count block transfer.
Table 17.7 lists register functions in block transfer mode, and Figure 17.7 shows the memory map of block transfer mode.

Table 17.7 Register Functions in Block Transfer Mode

		Value Written Back by Writing Transfer Information	
Register	**Description**	**When MRB.DTS bit is 0**	**When MRB.DTS bit is 1**
SAR	Transfer source address	Increment/decrement/fixed*1	SAR register initial value
DAR	Transfer destination address	DAR register initial value	Increment/decrement/fixed*1
CRAH	Retains initial value of block size	CRAH	
CRAL	Block size counter	CRAH	
CRB	Block transfer counter	CRB – 1	

Note 1. Write-back operation is skipped when address is fixed.

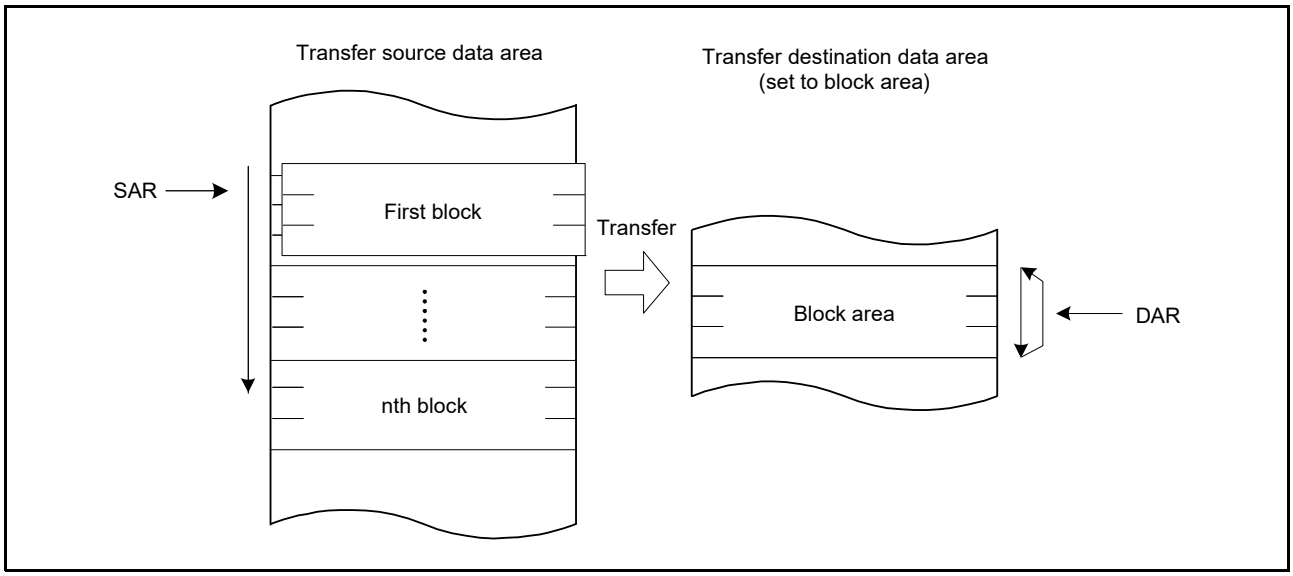


Figure 17.7 Memory Map of Block Transfer Mode (Transfer Destination: Block Area)

17.4.6 Chain Transfer

Setting the MRB.CHNE bit to 1 allows chain transfer to be performed continuously on a single transfer request. If the MRB.CHNE bit is 1 and the MRB.CHNS bit is 0, an interrupt request to the CPU is not generated when the specified number of data transfers is completed, or while the MRB.DISEL bit is 1 (an interrupt request to the CPU is generated for every data transfer). Data transfer has no effect on the interrupt status flag, which is the request source. The transfer information (SAR, DAR, CRA, CRB, MRA, and MRB) that define a data transfer can be specified independently of each other. Figure 17.8 shows chain transfer operation.

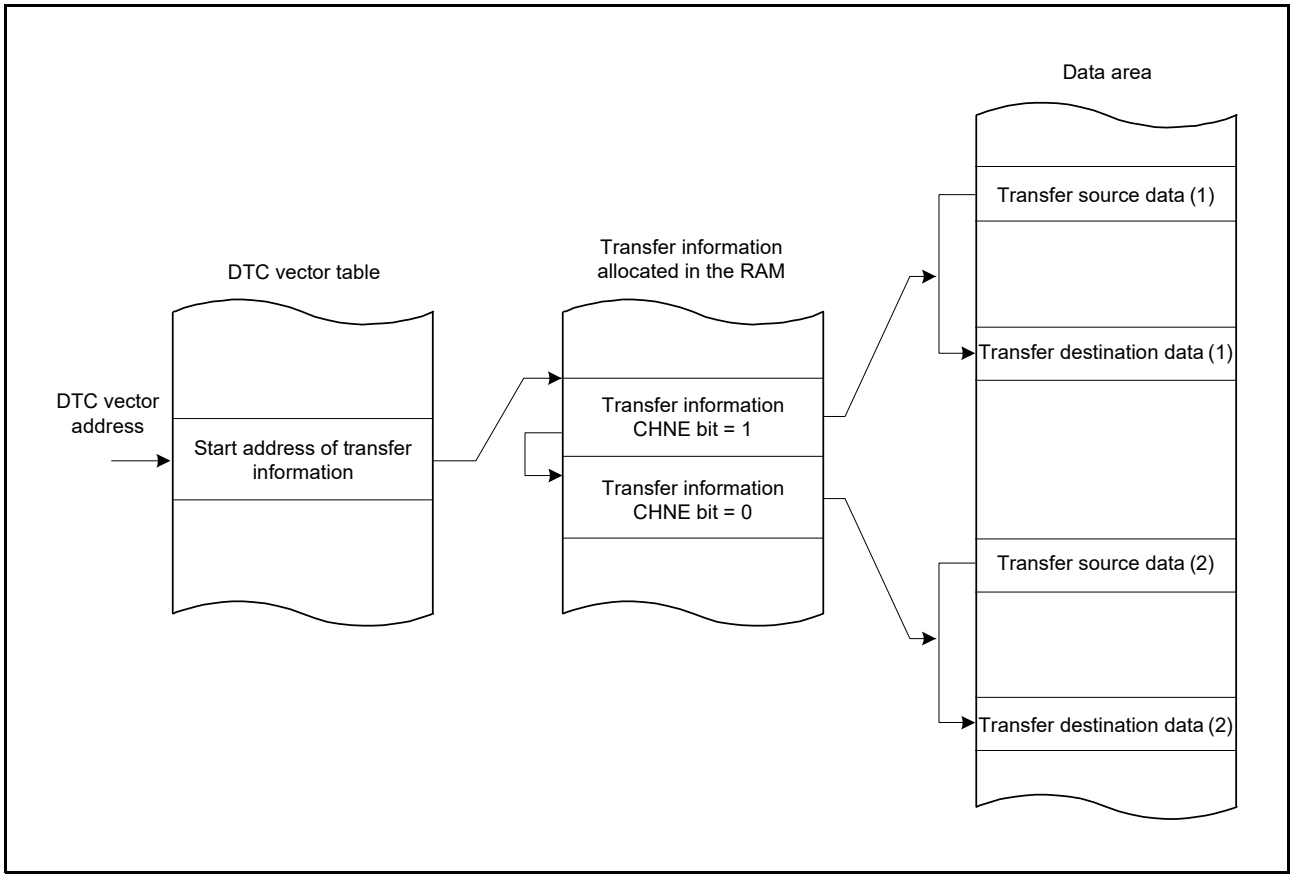


Figure 17.8 Chain Transfer Operation

If the MRB.CHNE bit is 1 and the CHNS bit is 1, chain transfer is performed only after completion of specified number of data transfers. In repeat transfer mode, chain transfer is performed after completion of specified number of data transfers.
For details on chain transfer conditions, refer to Table 17.3, Chain Transfer Conditions.

17.4.7 Operation Timing

Figure 17.9 to Figure 17.13 show examples of DTC operation timing.

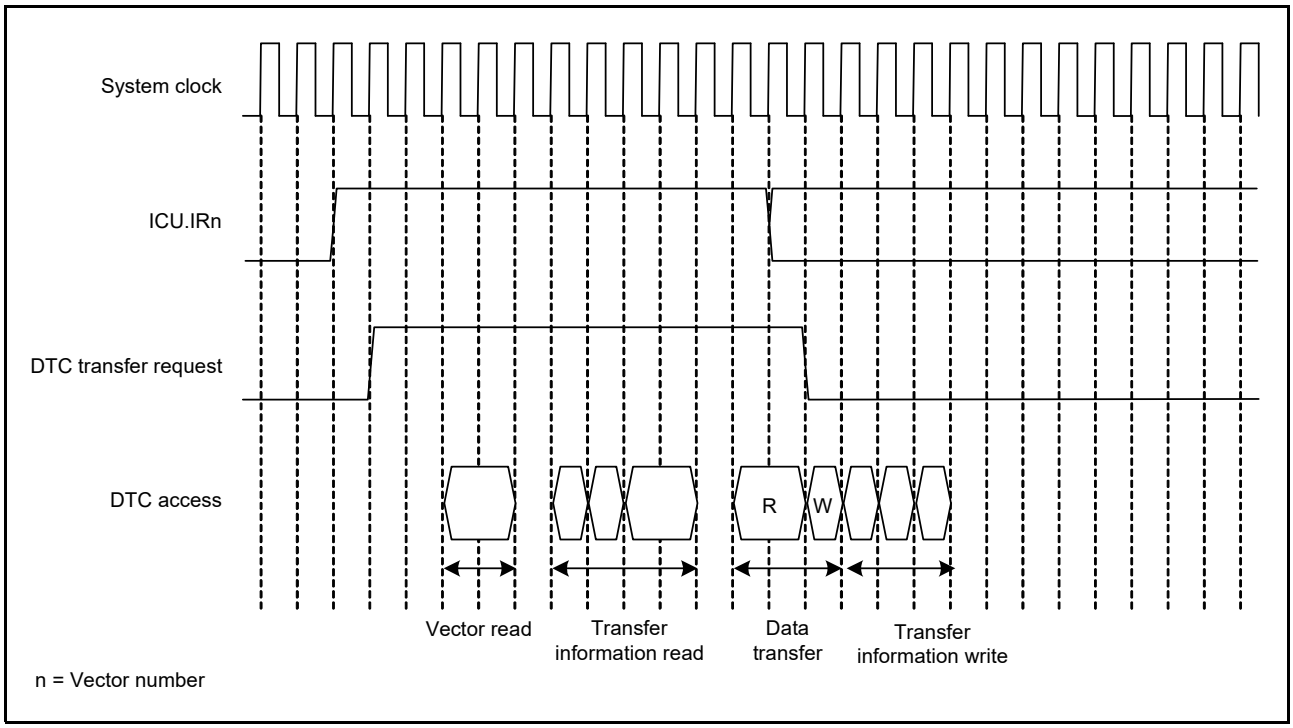


Figure 17.9 Example (1) of DTC Operation Timing (Short-Address Mode, Normal Transfer Mode, Repeat Transfer Mode)

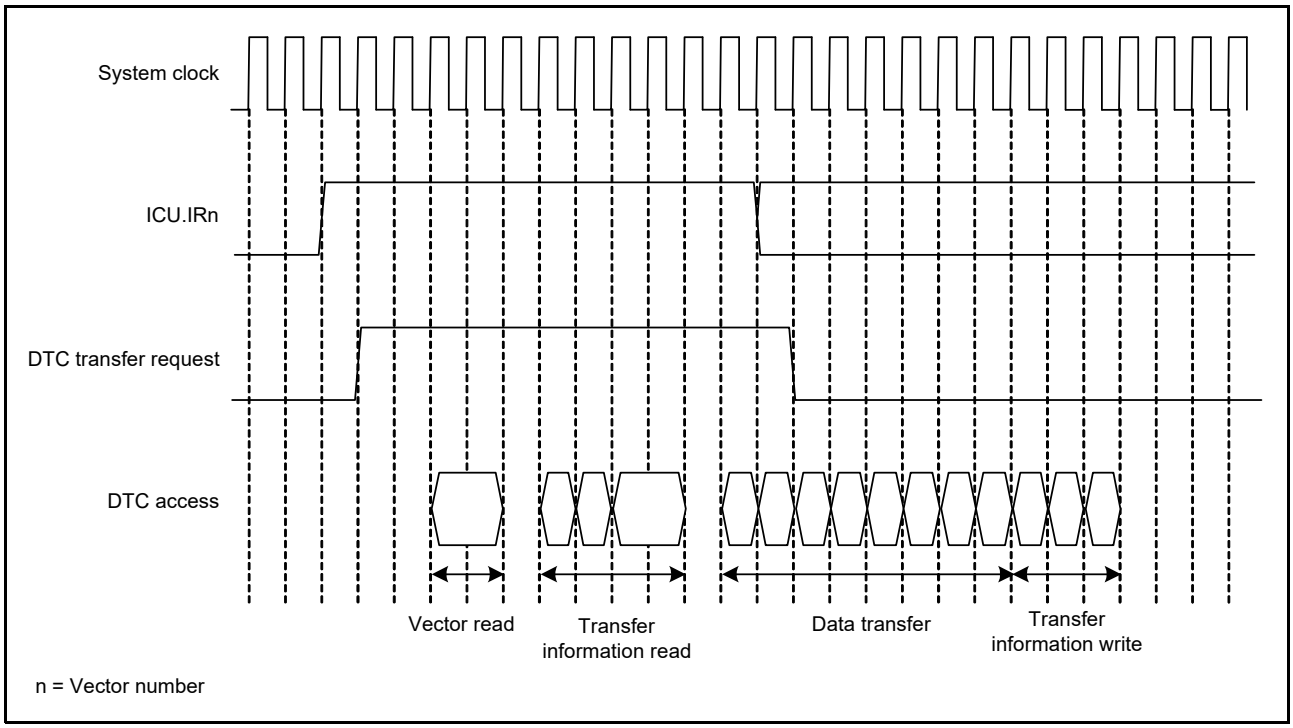


Figure 17.10 Example (2) of DTC Operation Timing (Short-Address Mode, Block Transfer Mode, Block Size = 4)

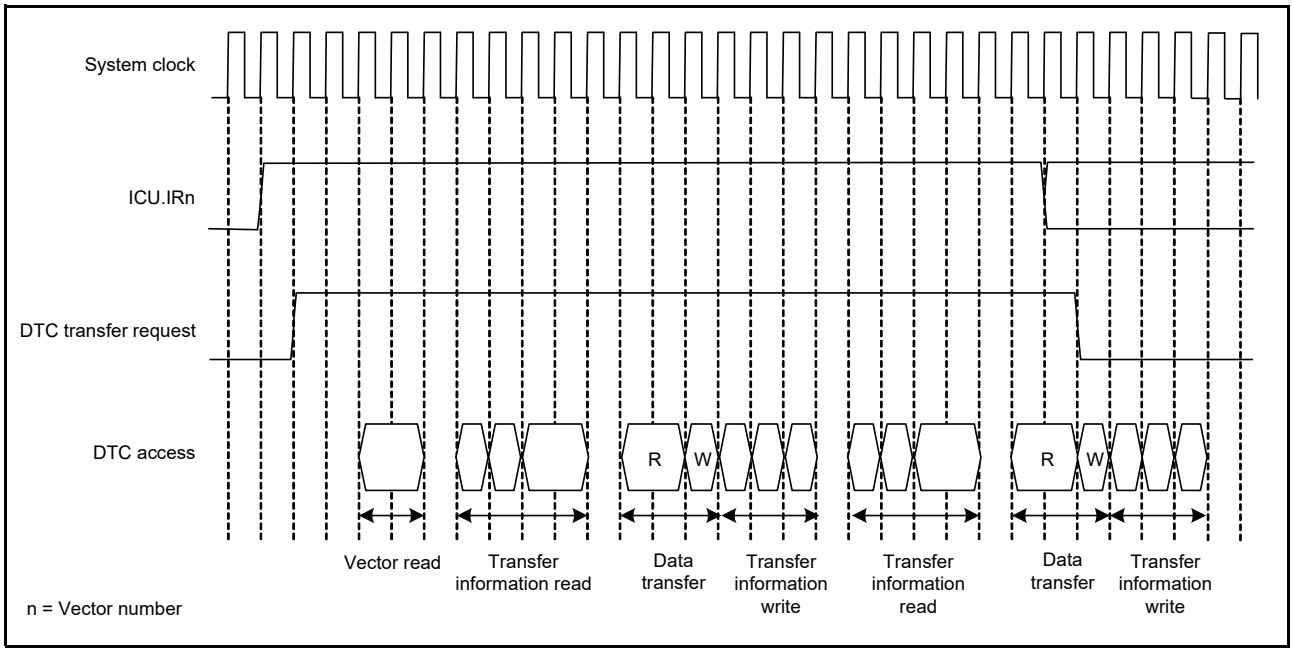


Figure 17.11 Example (3) of DTC Operation Timing (Short-Address Mode, Chain Transfer)

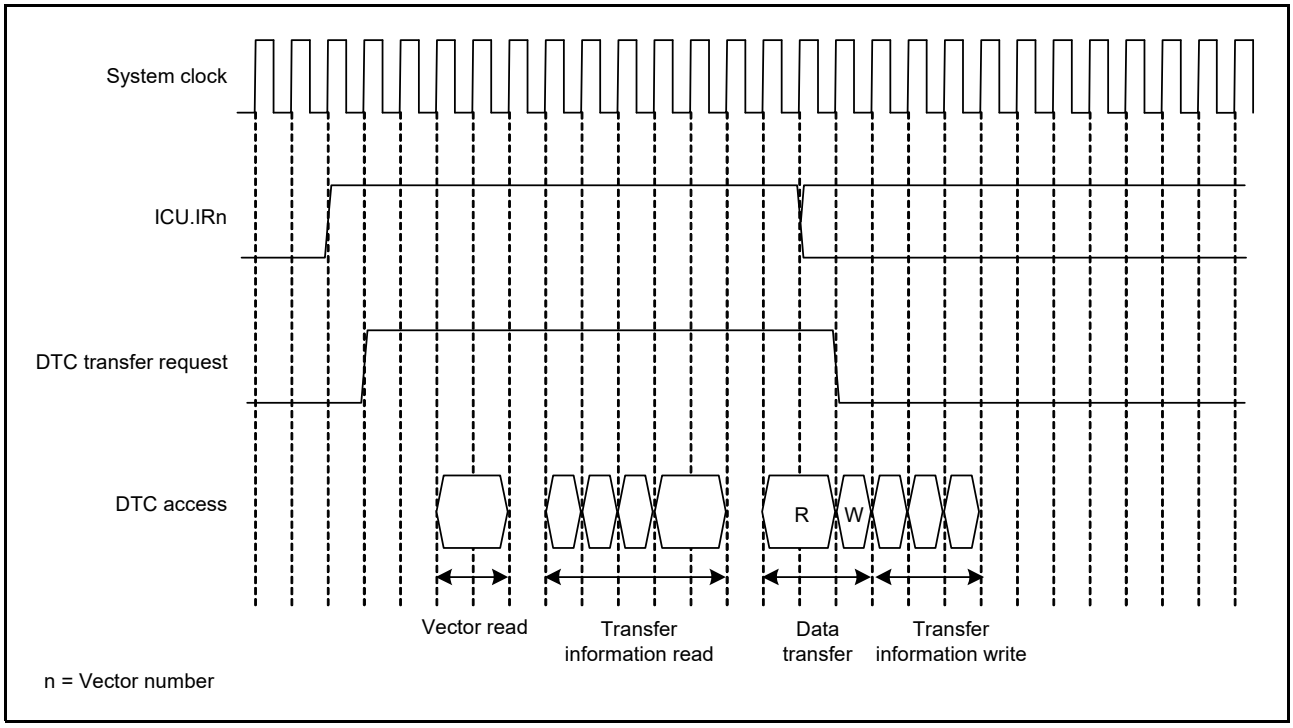
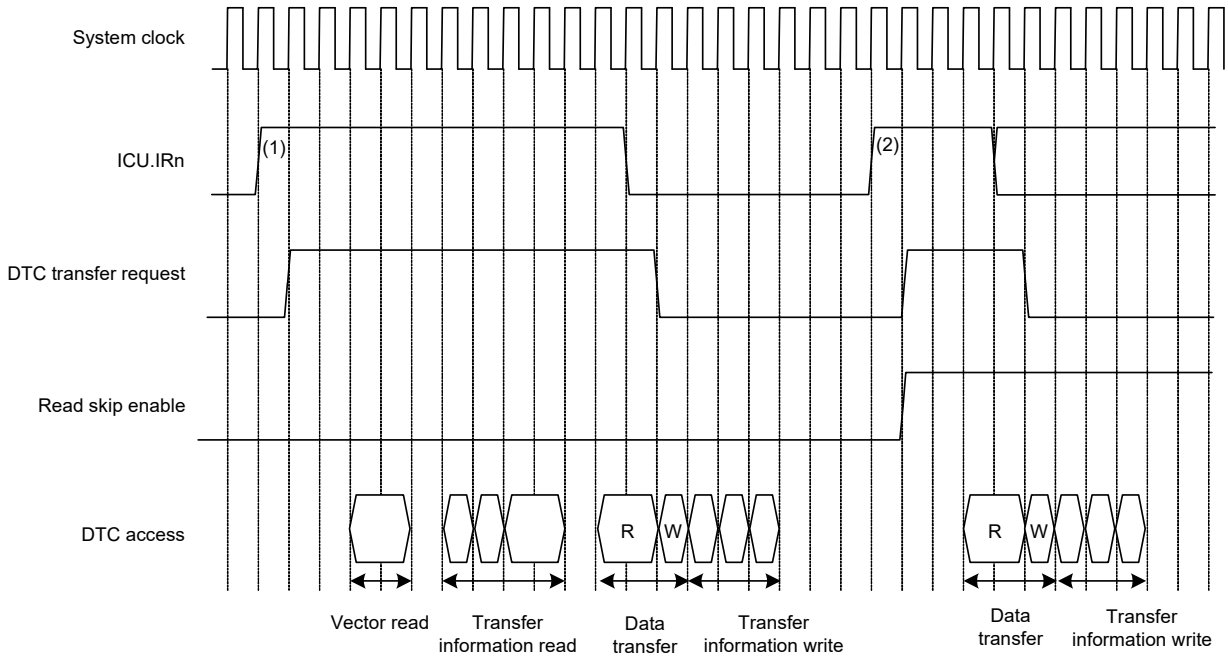


Figure 17.12 Example (4) of DTC Operation Timing (Full-Address Mode, Normal Transfer Mode, Repeat Transfer Mode)



n = Vector number

Note: When request sources (vector numbers) of (1) and (2) are the same and the DTCCR.RRS bit is 1, the transfer information read for request (2) is skipped.

Figure 17.13 Example of Operation When Transfer Information Read Skip is Executed (Vector, Transfer Information, and Transfer Destination Data on the RAM, and Transfer Source Data on the Peripheral Module)

17.4.8 Execution Cycles of the DTC

Table 17.8 lists the execution cycles of single data transfer of the DTC.
For the order of the execution states, refer to section 17.4.7, Operation Timing.

Table 17.8 Execution Cycles of the DTC

Transfer Mode	Vector Read		Transfer Information Read			Transfer Information Write			Data Transfer		Internal Operation	
									Read	Write		
Normal	Cv + 1	0*1	4 × Ci + 1*2	3 × Ci + 1*3	0*1	3 × Ci*4	2 × Ci*5	Ci*6	Cr + 1	Cw	2	0*1
Repeat									Cr + 1	Cw		
Block*7									P × Cr	P × Cw		

Note 1. When transfer information read is skipped
Note 2. In full-address mode
Note 3. In short-address mode
Note 4. When neither SAR nor DAR is set to address-fixed
Note 5. When SAR or DAR is set to address-fixed
Note 6. When SAR and DAR are set to address-fixed
Note 7. When the block size is 2 or more. If the block size is 1, the cycle number for normal transfer is applied.

P: Block size (initial settings of CRAH and CRAL)
Cv: Cycles for access to vector transfer information storage destination
Ci: Cycles for access to transfer information storage destination address
Cr: Cycles for access to data read destination
Cw: Cycles for access to data write destination
(The unit is system clocks (ICLK) for “+ 1” in the Vector Read, Transfer Information Read, and Data Transfer Read columns and “2” in the Internal Operation column.)
(Cv, Ci, Cr, and Cw vary depending on the corresponding access destination. For the number of cycles for respective access destinations, refer to section 35, RAM, section 36, Flash Memory, and section 5, I/O Registers.)

17.4.9 DTC Bus Mastership Release Timing

The DTC does not release the bus mastership during transfer information read and transfer information write. While transfer information is not read or written, bus arbitration is made according to the priority determined by the bus master arbitrator.
For bus arbitration, refer to section 15, Buses.

17.5 DTC Setting Procedure

Before using the DTC, set the DTC vector base register (DTCVBR).
Figure 17.14 shows the procedure to set the DTC.

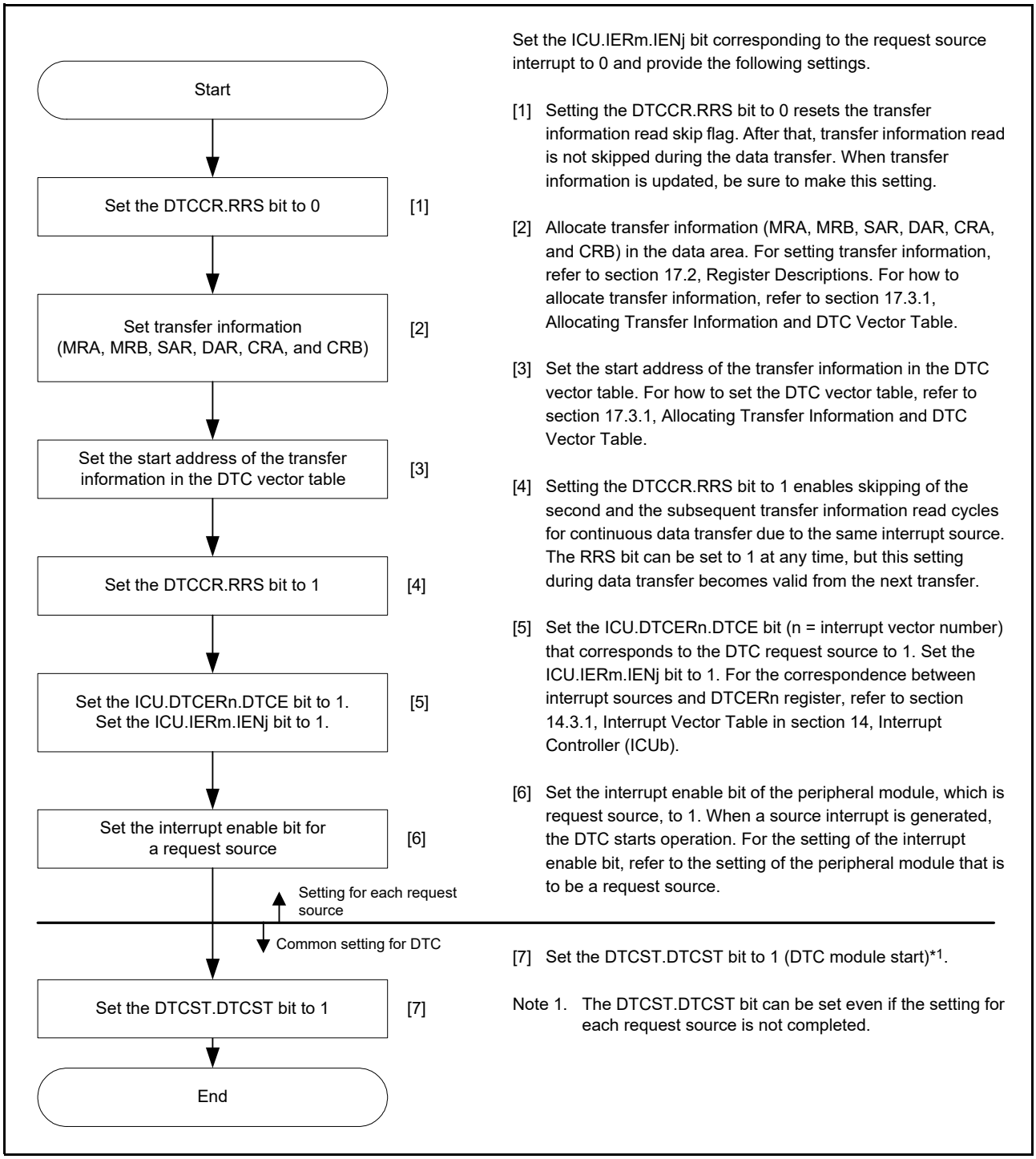


Figure 17.14 Procedure to Set the DTC

17.6 Examples of DTC Usage

17.6.1 Normal Transfer

As an example of DTC usage, its employment in the reception of 128 bytes of data by an SCI is described below.

(1) Transfer Information Setting

Set the MRA.MD[1:0] bits to 00b (normal transfer mode), the MRA.SZ[1:0] bits to 00b (byte transfer), and the MRA.SM[1:0] bits to 00b (source address is fixed). Set the MRB.CHNE bit to 0 (chain transfer is disabled), the MRB.DISEL bit to 0 (an interrupt request to the CPU is generated on completion of the specified number of data transfers), and the MRB.DM[1:0] bits to 10b (DAR is inclemented after data transfer). The MRB.DTS bit can be set to any value. Set the RDR register address of the SCI in the SAR register, the start address of the RAM area for data storage in the DAR register, and 128 (0080h) in the CRA register. The CRB register can be set to any value.

(2) DTC Vector Table Setting

The start address of the transfer information for the RXI interrupt is set in the vector table for the DTC.

(3) ICU Setting and DTC Module Activation

Set the corresponding ICU.DTCERn.DTCE bit to 1 and the ICU.IERm.IENj bit to 1.
Set the DTCST.DTCST bit to 1.

(4) SCI Setting

Enable the RXI interrupt by setting the SCR.RIE bit in the SCI to 1. If a reception error occurs during the SCI receive operation, further reception is not performed. Accordingly, make settings so that the CPU can accept receive error interrupts.

(5) DTC Transfer

Every time the reception of 1 byte by the SCI is completed, an RXI interrupt is generated to start the data transfer. The DTC transfers the received byte from the RDR of the SCI to RAM, after which the DAR register is incremented and the CRA register is decremented.

(6) Interrupt Handling

After 128 times of data transfers have been completed and the value in the CRA register becomes 0, an RXI interrupt request is output to the CPU. Complete the process in the handling routine for this interrupt.

17.6.2 Chain Transfer When the Counter is 0

The second data transfer is performed only when the transfer counter is set to 0 in the first data transfer, and the first data transfer information is repeatedly changed in the second data transfer. Repeating this chain transfer enables transfers to be repeated more than 256 times.
The following shows an example of configuring a 128-Kbyte input buffer to addresses 20 0000h to 21 FFFFh (where the input buffer is set so that its lower address starts with 0000h). Figure 17.15 shows a chain transfer when the counter is 0.

(1) Set normal transfer mode for input data for the first data transfer. Set the following:
Transfer source address: Fixed, the CRA register is 0000h (65,536 times), the MRB.CHNE bit is 1 (chain transfer is enabled), the MRB.CHNS bit is 1 (chain transfer is performed only when the transfer counter becomes 0), and the MRB.DISEL bit is 0 (an interrupt request to the CPU is generated on completion of the specified number of data transfers).
(2) Prepare the upper 8 bits (in this case, 21h and 20h) of the start address at every 65,536 times of the transfer destination address for the first data transfer in another area (such as ROM).
(3) For the second data transfer, set repeat transfer mode (source is repeat area) for rewriting the transfer destination address of the first data transfer. The transfer destination is the address where the upper 8 bits of the DAR register in the first transfer information is allocated. In this case, set the MRB.CHNE bit to 0 (chain transfer is disabled) and the MRB.DISEL bit to 0 (an interrupt request to the CPU is generated on completion of the specified number of data transfers). In this case, set the transfer counter to 2.
(4) When a transfer request is accepted, the first data transfer is executed. When transfer is executed 65,536 times and the transfer counter of the first data transfer becomes 0, the second data transfer is started and the upper 8 bits of the transfer destination address of the first data transfer is set to 21h. At this time, the lower 16 bits of the transfer destination address and the transfer counter of the first data transfer have become 0000h.
(5) In succession, when another transfer request is accepted, the first data transfer is executed. When transfer is executed 65,536 times and the transfer counter of the first data transfer becomes 0, the second data transfer is started and the upper 8 bits of the transfer destination address of the first data transfer is set to 20h. At this time, the lower 16 bits of the transfer destination address and the transfer counter of the first data transfer have become 0000h.
(6) Steps (4) and (5) above are repeated infinitely. Because the second data transfer is in repeat transfer mode, no interrupt request to the CPU is generated.

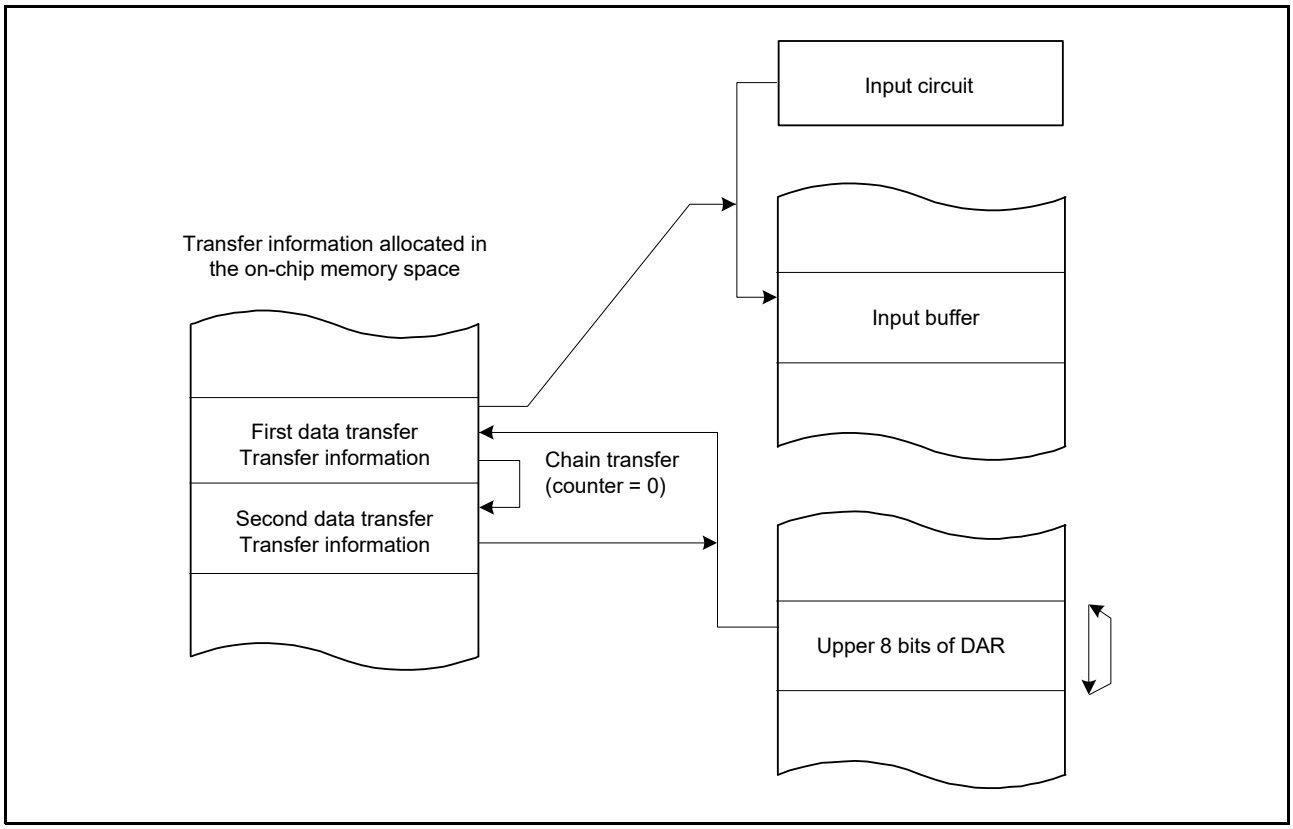


Figure 17.15 Chain Transfer When the Counter is 0

17.7 Interrupt Source

When the DTC has finished data transfer of specified count or when data transfer with the MRB.DISEL bit set to 1 (an interrupt request to the CPU is generated each time the data transfer is performed) has been completed, an interrupt to the CPU is generated by the DTC trigger source. Such interrupts to the CPU are controlled according to the PSW.I bit (interrupt enable) of the CPU, the PSW.IPL[3:0] bits (processor interrupt priority level), and the priority level of the interrupt controller.

17.8 Low Power Consumption Function

Before making a transition to the module stop state, deep sleep mode, or software standby mode, set the DTCST.DTCST bit to 0 (DTC module stop), and then perform the following.

(1) Module Stop Function

Writing 1 (transition to the module-stop state is made) to the MSTPCRA.MSTPA28 bit enables the module stop function of the DTC. If data transfer is in progress at the time 1 is written to the MSTPCRA.MSTPA28 bit, the transition to the module stop state proceeds after data transfer has ended. While the MSTPCRA.MSTPA28 bit is 1, accessing the DTC registers is prohibited.
Writing 0 (release from the module-stop state) to the MSTPCRA.MSTPA28 bit releases the DTC from the module stop state.

(2) Deep Sleep Mode

Make settings according to the procedure under section 11.6.2.1, Entry to Deep Sleep Mode, in section 11, Low Power Consumption.
If any data transfer is in progress at the time the WAIT instruction is executed, the transition to deep sleep mode follows the completion of the data transfer.
The DTC is released from the module stop state by writing 0 to the MSTPCRA.MSTPA28 bit following recovery from deep sleep mode.

(3) Software Standby Mode

Make settings according to the procedure under section 11.6.3.1, Entry to Software Standby Mode, in section 11, Low Power Consumption.
If any data transfer is in progress at the time the WAIT instruction is executed, the transition to software standby mode follows the completion of the data transfer.

(4) Notes on Low Power Consumption Function

For the WAIT instruction and the register setting procedure, refer to section 11.7.5, Timing of WAIT Instructions in section 11, Low Power Consumption.
To perform data transfer after returning from a low power consumption mode, set the DTCST.DTCST bit to 1 again.
To use a request that is generated in deep sleep mode or software standby mode as an interrupt request to the CPU but not as a DTC transfer request, specify the CPU as the interrupt request destination according to the description in section 14.4.3, Selecting Interrupt Request Destinations in section 14, Interrupt Controller (ICUb), and then execute the WAIT instruction.

17.9 Usage Notes

17.9.1 Start Address of Transfer Information

Set multiples of 4 for the start addresses of the transfer information to be specified in the DTC vector table. If any value other than a multiple of 4 is specified, access still proceeds with the lower 2 bits of the address regarded as 00b.

17.9.2 Allocating Transfer Information

Allocate transfer information in the memory area according to the endian of the area as shown in Figure 17.16.
For example, when writing CRA and CRB settings in 16-bit units in big endian, write the CRA setting to the address plus 8h (Ch) and the CRB setting to the address plus Ah (Eh). In little endian, write the CRB setting to the address plus 8h (Ch) and the CRA setting to the address plus Ah (Eh). When writing CRA and CRB settings in 32-bit units, allocate the CRA setting at the MSB side of the 32 bits and the CRB setting at the LSB side, and write the settings to the address plus 8h (Ch), regardless of endian.

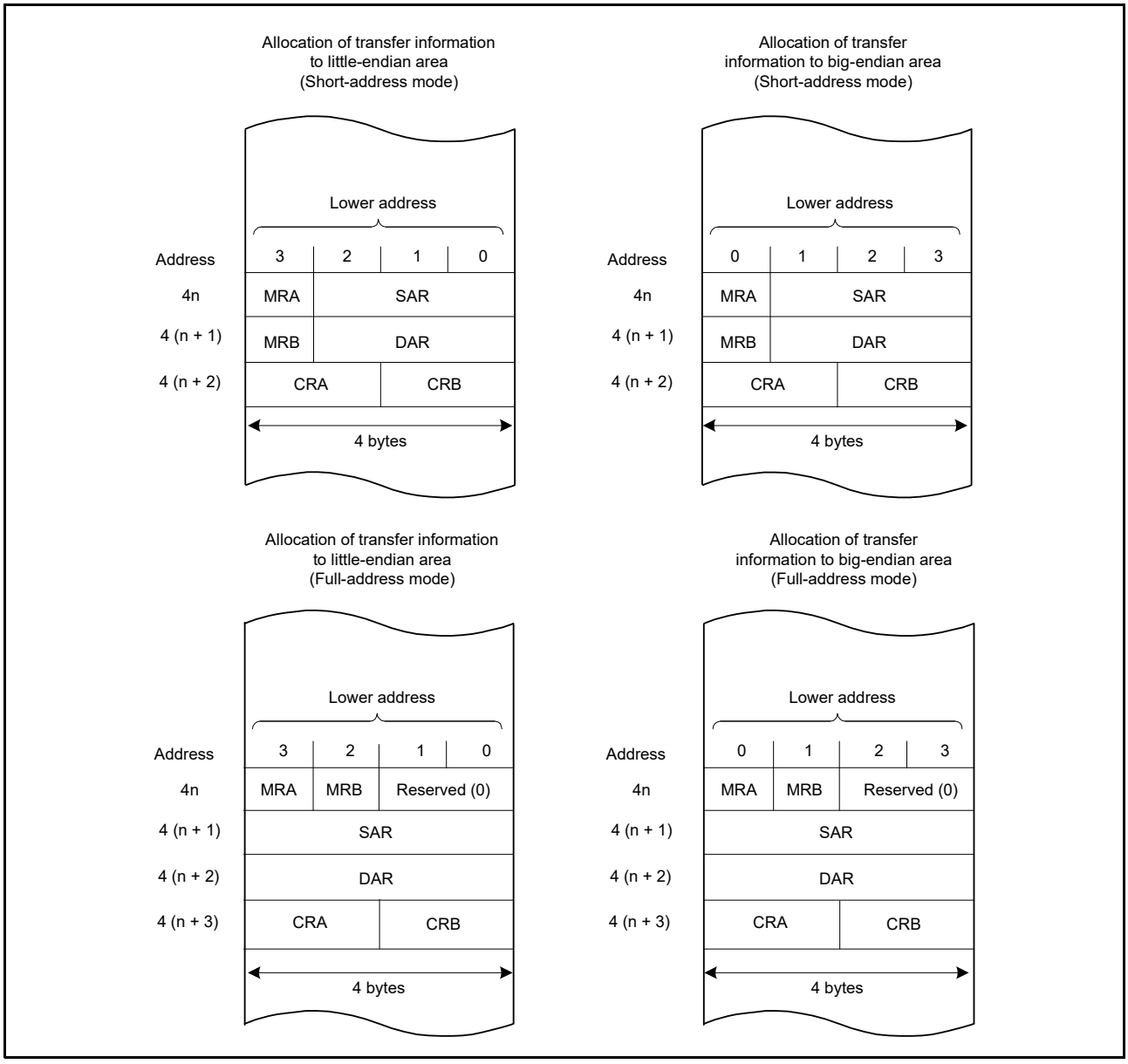


Figure 17.16 Allocation of Transfer Information

18. I/O Ports

18.1 Overview

The I/O ports function as a general I/O port, an I/O pin of a peripheral module, or an input pin for an interrupt.
Some of the pins are also configurable as an I/O pin of a peripheral module or an input pin for an interrupt. All pins function as input pins immediately after a reset, and pin functions are switched by register settings. The setting of each pin is specified by the registers for the corresponding I/O port and on-chip peripheral modules.
Each port has the port direction register (PDR) that selects input or output direction, the port output data register (PODR) that holds data for output, the port input data register (PIDR) that indicates the pin states, the open drain control register y (ODRy, y = 0, 1) that selects the output type of each pin, the pull-up control register (PCR) that controls on/off of the input pull-up MOS, the drive capacity control register (DSCR) that selects the drive capacity, and the port mode register (PMR) that specifies the pin function of each port.
For details on the PMR register, see section 19, Multi-Function Pin Controller (MPC).
The configuration of the I/O ports differs depending on the package. Table 18.1 lists the specifications of I/O ports, and Table 18.2 list the port functions.

Table 18.1 Specifications of I/O Ports

Port	Package		Package	
	144 Pins	Number of Pin	100 Pins	Number of Pin
PORT0	P00 to P02	3	P00 to P02	3
PORT1	P10 to P17	8	P10, P11	2
PORT2	P20 to P27	8	P20 to P24, P27	6
PORT3	P30 to P37	8	P30 to P33, P36, P37	6
PORT4	P40 to P47	8	P40 to P47	8
PORT5	P50 to P55	6	P52 to P55	4
PORT6	P60 to P65	6	P60 to P65	6
PORT7	P70 to P76	7	P70 to P76	7
PORT8	P80 to P84	5	P80 to P82	3
PORT9	P90 to P96	7	P90 to P96	7
PORTA	PA0 to PA7	8	PA0 to PA5	6
PORTB	PB0 to PB7	8	PB0 to PB7	8
PORTC	PC0 to PC6	7	—	—
PORTD	PD0 to PD7	8	PD0 to PD7	8
PORTE	PE0 to PE6	7	PE0 to PE5	6
PORTF	PF0 to PF3	4	—	—
PORTG	PG0 to PG2	3	—	—
	Total of Pins	111	Total of Pins	80

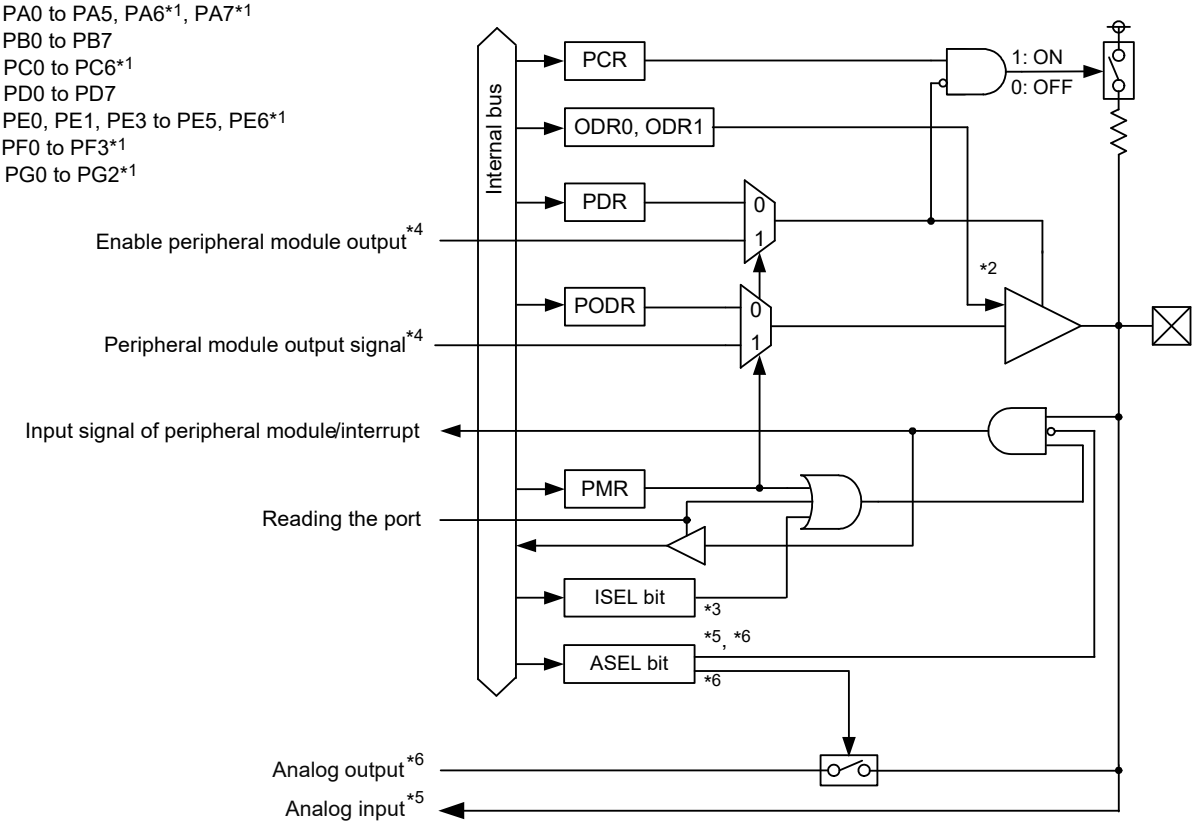
Table 18.2 Port Functions

Port	Pin	Input Pull-up	Open Drain Output	Drive Capacity Switching	High Current Pin	5-V Tolerant
PORT0	P00 to P02	○	○	○	—	—
PORT1	P10 to P17	○	○	○	—	—
PORT2	P20 to P27	○	○	○	—	—
PORT3	P30 to P35	○	○	○	—	—
	P36, P37	○	○	Fixed to normal output	—	—
PORT4	P40 to P47	○	—	Fixed to normal output	—	—
PORT5	P50 to P55	○	—	Fixed to normal output	—	—
PORT6	P60 to P65	○	—	Fixed to normal output	—	—
PORT7	P70	○	○	○	—	—
	P71 to P76	○	○	Fixed to high drive output	○	—
PORT8	P80, P82 to P84	○	○	○	—	—
	P81	○	○	Fixed to high drive output	○	—
PORT9	P90 to P95	○	○	Fixed to high drive output	○	—
	P96	○	○	○	—	—
PORTA	PA0 to PA3, PA5 to PA7	○	○	○	—	—
	PA4	○	○	○	—	—
PORTB	PB0, PB3	○	○	○	—	—
	PB1, PB2	○	○	Fixed to high drive output	—	○
	PB5	○	○	Fixed to high drive output	○	—
	PB4, PB6, PB7	○	○	○	—	—
PORTC	PC0 to PC6	○	○	○	—	—
PORTD	PD0, PD2	○	○	○	—	—
	PD3	○	○	Fixed to high drive output	○	—
	PD1, PD4 to PD7	○	○	○	—	—
PORTE	PE0, PE1, PE3 to PE6	○	○	○	—	—
	PE2	—	—	—	—	—
PORTF	PF0 to PF3	○	○	○	—	—
PORTG	PG0 to PG2	○	○	○	—	—

Specifying input pull-up, open-drain output, switching of drive capacity, or 5-V tolerance is available for other signals on pins that also function as general I/O pins.

18.2 I/O Port Configuration

Port 0: P00 to P02
Port 1: P10, P11, P12 to P17*1
Port 2: P20 to P24, P25*1, P26*1, P27
Port 3: P30 to P33, P34*1, P35*1
Port 4: P40 to P47
Port 5: P50*1, P51*1 to P55
Port 6: P60 to P65
Port 7: P70 to P76
Port 8: P80 to P82, P83*1, P84*1
Port 9: P90 to P96
Port A: PA0 to PA5, PA6*1, PA7*1
Port B: PB0 to PB7
Port C: PC0 to PC6*1
Port D: PD0 to PD7
Port E: PE0, PE1, PE3 to PE5, PE6*1
Port F: PF0 to PF3*1
Port G: PG0 to PG2*1



Note 1. Not provided on the 100-pin package
Note 2. Control signal for N-channel open-drain output
Note 3. An external interrupt function is multiplexed on this pin
Note 4. A peripheral module output is multiplexed on this pin
Note 5. An analog input function is multiplexed on this pin.
Note 6. An analog output function is multiplexed on this pin.

Figure 18.1 I/O Port Configuration (1)

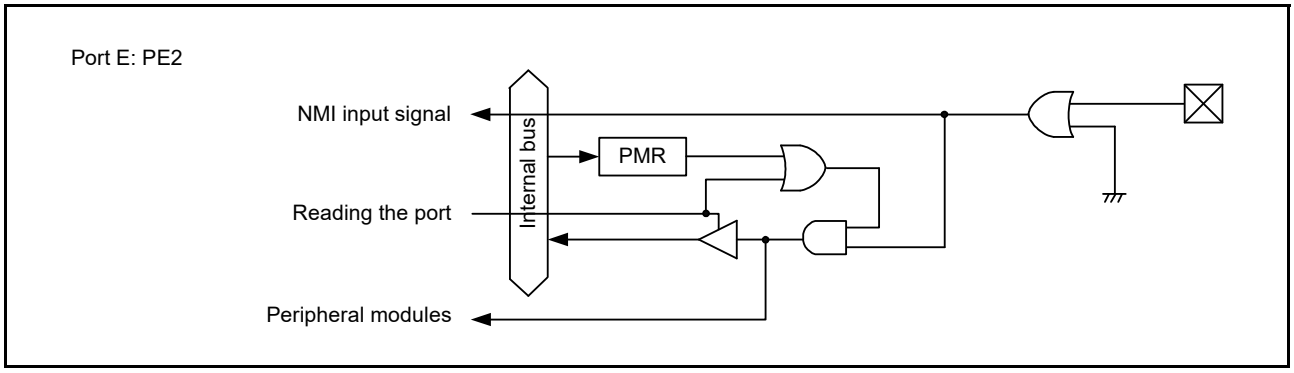
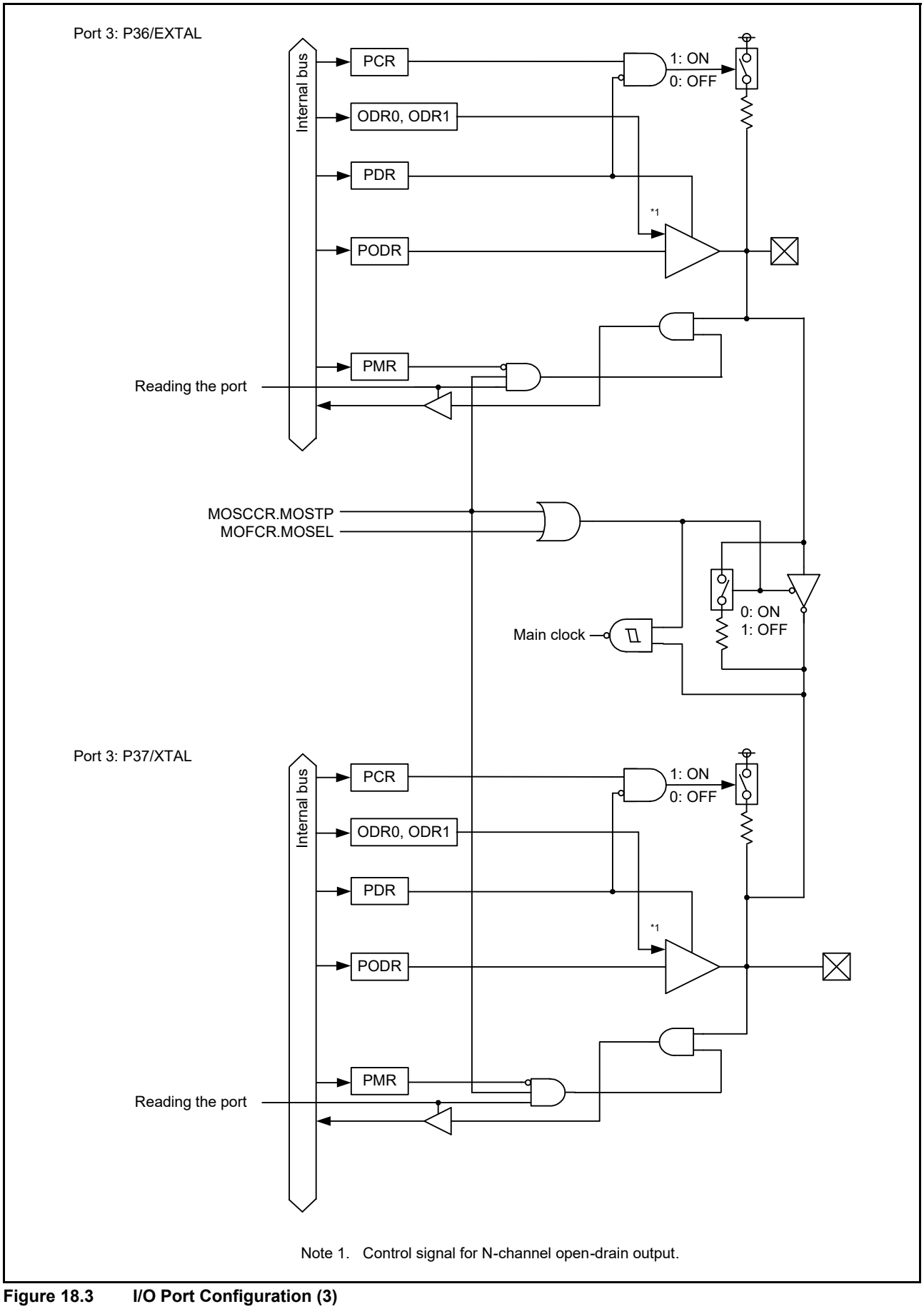


Figure 18.2 I/O Port Configuration (2)



Note 1. Control signal for N-channel open-drain output.

Figure 18.3 I/O Port Configuration (3)

18.3 Register Descriptions

18.3.1 Port Direction Register (PDR)

Address(es): PORT0.PDR 0008 C000h, PORT1.PDR 0008 C001h, PORT2.PDR 0008 C002h, PORT3.PDR 0008 C003h, PORT4.PDR 0008 C004h, PORT5.PDR 0008 C005h, PORT6.PDR 0008 C006h, PORT7.PDR 0008 C007h, PORT8.PDR 0008 C008h, PORT9.PDR 0008 C009h, PORTA.PDR 0008 C00Ah, PORTB.PDR 0008 C00Bh, PORTC.PDR 0008 C00Ch, PORTD.PDR 0008 C00Dh, PORTE.PDR 0008 C00Eh, PORTF.PDR 0008 C00Fh, PORTG.PDR 0008 C010h

	b7	b6	b5	b4	b3	b2	b1	b0
	B7	B6	B5	B4	B3	B2	B1	B0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	B0	Pm0 I/O Select	0: Input (Functions as an input pin.) 1: Output (Functions as an output pin.)	R/W
b1	B1	Pm1 I/O Select		R/W
b2	B2	Pm2 I/O Select		R/W
b3	B3	Pm3 I/O Select		R/W
b4	B4	Pm4 I/O Select		R/W
b5	B5	Pm5 I/O Select		R/W
b6	B6	Pm6 I/O Select		R/W
b7	B7	Pm7 I/O Select		R/W

m = 0 to 9, A to G

PDR is used to select the input or output direction for individual pins of the corresponding port m when the pins are configured as the general I/O pins.

Each bit of PORTm.PDR corresponds to each pin of port m; I/O direction can be specified in 1-bit units.

Write 1 (output) to each bit of PDR corresponding to port m that does not exist.

Each bit of PDR corresponding to port m that does not exist is reserved. Make settings according to the description in section 18.4, Initialization of the Port Direction Register (PDR).

The PORTE.PDR.B2 bit is reserved, because the PE2 pin is input only. A reserved bit is read as 0. The write value should be 0.

18.3.2 Port Output Data Register (PODR)

Address(es): PORT0.PODR 0008 C020h, PORT1.PODR 0008 C021h, PORT2.PODR 0008 C022h, PORT3.PODR 0008 C023h, PORT4.PODR 0008 C024h, PORT5.PODR 0008 C025h, PORT6.PODR 0008 C026h, PORT7.PODR 0008 C027h, PORT8.PODR 0008 C028h, PORT9.PODR 0008 C029h, PORTA.PODR 0008 C02Ah, PORTB.PODR 0008 C02Bh, PORTC.PODR 0008 C02Ch, PORTD.PODR 0008 C02Dh, PORTE.PODR 0008 C02Eh, PORTF.PODR 0008 C02Fh, PORTG.PODR 0008 C030h

	b7	b6	b5	b4	b3	b2	b1	b0
	B7	B6	B5	B4	B3	B2	B1	B0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	B0	Pm0 Output Data Store	Holds output data.	R/W
b1	B1	Pm1 Output Data Store		R/W
b2	B2	Pm2 Output Data Store		R/W
b3	B3	Pm3 Output Data Store		R/W
b4	B4	Pm4 Output Data Store		R/W
b5	B5	Pm5 Output Data Store		R/W
b6	B6	Pm6 Output Data Store		R/W
b7	B7	Pm7 Output Data Store		R/W

m = 0 to 9, A to G

PODR holds the data to be output from the pins used for general output ports.
The PORTE.PODR.B2 bit is reserved, because the PE2 pin is input only. The bit corresponding to a pin that does not exist is reserved. A reserved bit is read as 0. The write value should be 0.

18.3.3 Port Input Data Register (PIDR)

Address(es): PORT0.PIDR 0008 C040h, PORT1.PIDR 0008 C041h, PORT2.PIDR 0008 C042h, PORT3.PIDR 0008 C043h, PORT4.PIDR 0008 C044h, PORT5.PIDR 0008 C045h, PORT6.PIDR 0008 C046h, PORT7.PIDR 0008 C047h, PORT8.PIDR 0008 C048h, PORT9.PIDR 0008 C049h, PORTA.PIDR 0008 C04Ah, PORTB.PIDR 0008 C04Bh, PORTC.PIDR 0008 C04Ch, PORTD.PIDR 0008 C04Dh, PORTE.PIDR 0008 C04Eh, PORTF.PIDR 0008 C04Fh, PORTG.PIDR 0008 C050h

	b7	b6	b5	b4	b3	b2	b1	b0
	B7	B6	B5	B4	B3	B2	B1	B0
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b0	B0	Pm0	Indicates individual pin states of the corresponding port.	R
b1	B1	Pm1		R
b2	B2	Pm2		R
b3	B3	Pm3		R
b4	B4	Pm4		R
b5	B5	Pm5		R
b6	B6	Pm6		R
b7	B7	Pm7		R

m = 0 to 9, A to G

PIDR indicates individual pin states of port m.

The pin states of port m can be read with the PORTm.PIDR, regardless of the values of PORTm.PDR and PORTm.PMR.

The NMI pin state is reflected in the PE2 bit.

The bit corresponding to a pin that does not exist is reserved. A reserved bit is read as undefined, and cannot be modified.

Note: When using P36 and P37 as general I/O ports, set the MOSCCR.MOSTP bit to 1 (main clock oscillator is stopped) and the P36 and P37 control bits in the PORT3.PMR register to 0 (use pin as general I/O port).

18.3.4 Port Mode Register (PMR)

Address(es): PORT0.PMR 0008 C060h, PORT1.PMR 0008 C061h, PORT2.PMR 0008 C062h, PORT3.PMR 0008 C063h, PORT7.PMR 0008 C067h, PORT8.PMR 0008 C068h, PORT9.PMR 0008 C069h, PORTA.PMR 0008 C06Ah, PORTB.PMR 0008 C06Bh, PORTC.PMR 0008 C06Ch, PORTD.PMR 0008 C06Dh, PORTE.PMR 0008 C06Eh, PORTF.PMR 0008 C06Fh, PORTG.PMR 0008 C070h

	b7	b6	b5	b4	b3	b2	b1	b0
	B7	B6	B5	B4	B3	B2	B1	B0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	B0	Pm0 Pin Mode Control	0: Use pin as general I/O port. 1: Use pin as I/O port for peripheral functions.	R/W
b1	B1	Pm1 Pin Mode Control		R/W
b2	B2	Pm2 Pin Mode Control		R/W
b3	B3	Pm3 Pin Mode Control		R/W
b4	B4	Pm4 Pin Mode Control		R/W
b5	B5	Pm5 Pin Mode Control		R/W
b6	B6	Pm6 Pin Mode Control		R/W
b7	B7	Pm7 Pin Mode Control		R/W

m = 0 to 3, 7 to 9, A to G

Each bit of PORTm.PMR corresponds to each pin of port m; pin function can be specified in 1-bit units.
The bit corresponding to a pin that does not exist is reserved. A reserved bit is read as 0. The write value should be 0.

18.3.5 Open Drain Control Register 0 (ODR0)

Address(es): PORT0.ODR0 0008 C080h, PORT1.ODR0 0008 C082h, PORT2.ODR0 0008 C084h, PORT3.ODR0 0008 C086h, PORT7.ODR0 0008 C08Eh, PORT8.ODR0 0008 C090h, PORT9.ODR0 0008 C092h, PORTA.ODR0 0008 C094h, PORTB.ODR0 0008 C096h, PORTC.ODR0 0008 C098h, PORTD.ODR0 0008 C09Ah, PORTE.ODR0 0008 C09Ch, PORTF.ODR0 0008 C09Eh, PORTG.ODR0 0008 C0A0h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	B6	—	B4	—	B2	—	B0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	B0	Pm0 Output Type Select	0: CMOS output 1: N-channel open-drain	R/W
b1	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b2	B2	Pm1 Output Type Select	0: CMOS output 1: N-channel open-drain	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	B4	Pm2 Output Type Select	0: CMOS output 1: N-channel open-drain	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	B6	Pm3 Output Type Select	0: CMOS output 1: N-channel open-drain	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

m = 0 to 3, 7 to 9, A to G

The bits corresponding to a pin that does not exist or pins with no open-drain output allocation are reserved. A reserved bit is read as 0. The write value should be 0.

18.3.6 Open Drain Control Register 1 (ODR1)

Address(es): PORT1.ODR1 0008 C083h, PORT2.ODR1 0008 C085h, PORT3.ODR1 0008 C087h, PORT7.ODR1 0008 C08Fh, PORT8.ODR1 0008 C091h, PORT9.ODR1 0008 C093h, PORTA.ODR1 0008 C095h, PORTB.ODR1 0008 C097h, PORTC.ODR1 0008 C099h, PORTD.ODR1 0008 C09Bh, PORTE.ODR1 0008 C09Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	B6	—	B4	—	B2	—	B0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	B0	Pm4 Output Type Select	0: CMOS output 1: N-channel open-drain	R/W
b1	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b2	B2	Pm5 Output Type Select	0: CMOS output 1: N-channel open-drain	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	B4	Pm6 Output Type Select	0: CMOS output 1: N-channel open-drain	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	B6	Pm7 Output Type Select	0: CMOS output 1: N-channel open-drain	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

m = 1 to 3, 7 to 9, A to E

The bits corresponding to a pin that does not exist or pins with no open-drain output allocation are reserved. A reserved bit is read as 0. The write value should be 0.

18.3.7 Pull-Up Control Register (PCR)

Address(es): PORT0.PCR 0008 C0C0h, PORT1.PCR 0008 C0C1h, PORT2.PCR 0008 C0C2h, PORT3.PCR 0008 C0C3h, PORT4.PCR 0008 C0C4h, PORT5.PCR 0008 C0C5h, PORT6.PCR 0008 C0C6h, PORT7.PCR 0008 C0C7h, PORT8.PCR 0008 C0C8h, PORT9.PCR 0008 C0C9h, PORTA.PCR 0008 C0CAh, PORTB.PCR 0008 C0CBh, PORTC.PCR 0008 C0CCh, PORTD.PCR 0008 C0CDh, PORTE.PCR 0008 C0CEh, PORTF.PCR 0008 C0CFh, PORTG.PCR 0008 C0D0h

	b7	b6	b5	b4	b3	b2	b1	b0
	B7	B6	B5	B4	B3	B2	B1	B0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	B0	Pm0 Input Pull-Up Resistor Control	0: Disables an input pull-up resistor. 1: Enables an input pull-up resistor.	R/W
b1	B1	Pm1 Input Pull-Up Resistor Control		R/W
b2	B2	Pm2 Input Pull-Up Resistor Control		R/W
b3	B3	Pm3 Input Pull-Up Resistor Control		R/W
b4	B4	Pm4 Input Pull-Up Resistor Control		R/W
b5	B5	Pm5 Input Pull-Up Resistor Control		R/W
b6	B6	Pm6 Input Pull-Up Resistor Control		R/W
b7	B7	Pm7 Input Pull-Up Resistor Control		R/W

m = 0 to 9, A to G

While a pin is in the input state with the corresponding bit in PORTm.PCR set to 1, the pull-up resistor connected to the pin is enabled.

When a pin is used as a general port output pin, or a peripheral function output pin, the pull-up resistor for the pin is disabled regardless of the settings of the PCR register.

The pull-up resistor is also disabled in the reset state.

The PORTE.PCR.B2 bit is reserved. The bit corresponding to a pin that does not exist is also reserved. A reserved bit is read as 0. The write value should be 0.

18.3.8 Drive Capacity Control Register (DSCR)

Address(es): PORT0.DSCR 0008 C0E0h, PORT1.DSCR 0008 C0E1h, PORT2.DSCR 0008 C0E2h, PORT3.DSCR 0008 C0E3h, PORT7.DSCR 0008 C0E7h, PORT8.DSCR 0008 C0E8h, PORT9.DSCR 0008 C0E9h, PORTA.DSCR 0008 C0EAh, PORTB.DSCR 0008 C0EBh, PORTC.DSCR 0008 C0ECh, PORTD.DSCR 0008 C0EDh, PORTE.DSCR 0008 C0EEh, PORTF.DSCR 0008 C0EFh, PORTG.DSCR 0008 C0F0h

	b7	b6	b5	b4	b3	b2	b1	b0
	B7	B6	B5	B4	B3	B2	B1	B0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	B0	Pm0 Drive Capacity Control	0: Normal drive output 1: High-drive output	R/W
b1	B1	Pm1 Drive Capacity Control		R/W
b2	B2	Pm2 Drive Capacity Control		R/W
b3	B3	Pm3 Drive Capacity Control		R/W
b4	B4	Pm4 Drive Capacity Control		R/W
b5	B5	Pm5 Drive Capacity Control		R/W
b6	B6	Pm6 Drive Capacity Control		R/W
b7	B7	Pm7 Drive Capacity Control		R/W

m = 0 to 3, 7 to 9, A to G

When high-drive output is selected, switching noise increases compared to when normal output is selected. Carefully evaluate the effect of noise on the MCU caused by adjacent pins before selecting high-drive output.
A bit corresponding to a pin with a fixed drive capacity or one that does not exist, is reserved. A reserved bit is read as 0. The write value should be 0.

18.4 Initialization of the Port Direction Register (PDR)

Initialize reserved bits in the PDR register according to Table 18.3 and Table 18.4.

- The blank columns in Table 18.3 and Table 18.4 indicate the bits corresponding to the pins listed in Table 18.1, Specifications of I/O Ports.
  The corresponding bits should be set to 1 (output) or 0 (input) depending on the user system.
- The columns other than the blank columns in Table 18.3 and Table 18.4 indicate reserved bits.
  A reserved bit should be set to 0 (input) or 1 (output) according to Table 18.3 and Table 18.4.
  When setting a value to a reserved bit, access in byte units.

Table 18.3 PDR Register Settings in 144-Pin Packages

	PDR Register							
Port Symbol	**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
PORT0	0	0	0	0	0			
PORT1								
PORT2								
PORT3								
PORT4								
PORT5	0	0						
PORT6	0	0						
PORT7	0							
PORT8	0	0	0					
PORT9	0							
PORTA								
PORTB								
PORTC	0							
PORTD								
PORTE	0					0		
PORTF	0	0	0	0				
PORTG	0	0	0	0	0			

Table 18.4 PDR Register Settings in 100-Pin Packages

	PDR Register							
Port Symbol	**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
PORT0	0	0	0	0	0			
PORT1	1	1	1	1	1	1		
PORT2		1	1					
PORT3			1	1				
PORT4								
PORT5	0	0					1	1
PORT6	0	0						
PORT7	0							
PORT8	0	0	0	1	1			
PORT9	0							
PORTA	1	1						
PORTB								
PORTC	0	1	1	1	1	1	1	1
PORTD								
PORTE	0	1				0		
PORTF	0	0	0	0	1	1	1	1
PORTG	0	0	0	0	0	1	1	1

18.5 Handling of Unused Pins

The configuration of unused pins is listed in Table 18.5.

Table 18.5 Unused Pin Configuration

Pin Name	Description
MD	(Always used as mode pins)
RES#	Connect this pin to VCC via a pull-up resistor.
PE2/NMI	Connect this pin to VCC via a pull-up resistor.
P36/EXTAL	When the main clock is not used, set the MOSCCR.MOSTP bit to 1 (general port P36). When this pin is not used as port P36 either, it is configured in the same way as port 0 to 3, 7 to 9, A to G.
P37/XTAL	When the main clock is not used, set the MOSCCR.MOSTP bit to 1 (general port P37). When this pin is not used as port P37 either, it is configured in the same way as port 0 to 3, 7 to 9, A to G. When the external clock is input to the EXTAL pin, leave this pin open.
Ports 0 to 3, 7 to 9 Ports A to G	• If the direction setting is for input (PORTn.PDR = 0), the corresponding pin is connected to VCC (pulled up) via a resistor or to VSS (pulled down) via a resistor.*1 • If the direction setting is for output (PORTn.PDR = 1), the pin is released.*1, *2
Port 4 to 6	The corresponding pin is connected to an analog power supply (AVCC0/AVCC1/AVCC2) (pulled up) via resistor or to an analog ground (AVSS0/AVSS1/AVSS2) (pulled down) via resistor.
VREFH0	Connect this pin to AVCC0
VREFH1	Connect this pin to AVCC1
VREFH2	Connect this pin to AVCC2
VREFL0	Connect this pin to AVSS0
VREFL1	Connect this pin to AVSS1
VREFL2	Connect this pin to AVSS2
PGAVSS0	Connect this pin to AVSS0
PGAVSS1	Connect this pin to AVSS1

Note 1. Clear the PORTn.PMR bit, the PmnPFS.ISEL bit and the PmnPFS.ASEL bit to 0.
Note 2. In the case of release when the setting is for output, the port is an input over the period from release from the reset state to the pin becoming an output. Since the voltage on the pin is undefined while it is an input, this may lead to an increase in the current drawn.

19. Multi-Function Pin Controller (MPC)

19.1 Overview

The multi-function pin controller (MPC) is used to allocate input and output signals for peripheral modules and input interrupt signals to pins from among multiple ports.

Table 19.1 shows the allocation of pin functions to multiple pins. The symbols ○ and × in the table indicate whether the pins are or are not present on the given package. Allocating the same function to more than one pin is prohibited.

Table 19.1 Allocation of Pin Functions to Multiple Pins (1/9)

Module/Function	Channel	Pin Functions	Allocation Port	Package	
				144-pin	100-pin
Interrupt	IRQ0	IRQ0 (input)	P10	○	○
			P52	○	○
			PE5	○	○
	IRQ1	IRQ1 (input)	P11	○	○
			P53	○	○
			PA5	○	○
			PE4	○	○
	IRQ2	IRQ2 (input)	P00	○	○
			P54	○	○
			PD4	○	○
			PE3	○	○
	IRQ3	IRQ3 (input)	P55	○	○
			PB4	○	○
			PD5	○	○
			PE6	○	×
	IRQ4	IRQ4 (input)	P01	○	○
			P60	○	○
			P96	○	○
	IRQ5	IRQ5 (input)	P02	○	○
			P61	○	○
			P70	○	○
			PB6	○	○
			PD6	○	○
	IRQ6	IRQ6 (input)	P21	○	○
			P31	○	○
			P62	○	○
	IRQ7	IRQ7 (input)	P20	○	○
			P30	○	○
			P63	○	○
	NMI	NMI (input)	PE2	○	○

Table 19.1 Allocation of Pin Functions to Multiple Pins (2/9)

Module/Function	Channel	Pin Functions	Allocation Port	Package	
				144-pin	100-pin
Multi-function timer unit 3	MTU0	MTIOC0A (input/output)/MTIOC0A# (input/output)	P31	○	○
			PB3	○	○
		MTIOC0B (input/output)/MTIOC0B# (input/output)	P30	○	○
			PB2	○	○
		MTIOC0C (input/output)/MTIOC0C# (input/output)	PB1	○	○
		MTIOC0D (input/output)/MTIOC0D# (input/output)	PB0	○	○
	MTU1	MTIOC1A (input/output)/MTIOC1A# (input/output)	P27	○	○
			PA5	○	○
			PC6	○	×
		MTIOC1B (input/output)/MTIOC1B# (input/output)	PA4	○	○
			PC5	○	×
	MTU2	MTIOC2A (input/output)/MTIOC2A# (input/output)	PA3	○	○
		MTIOC2B (input/output)/MTIOC2B# (input/output)	PA2	○	○
	MTU3	MTIOC3A (input/output)/MTIOC3A# (input/output)	P11	○	○
			P33	○	○
		MTIOC3B (input/output)/MTIOC3B# (input/output)	P12	○	×
			P71	○	○
		MTIOC3C (input/output)/MTIOC3C# (input/output)	P32	○	○
		MTIOC3D (input/output)/MTIOC3D# (input/output)	P15	○	×
			P74	○	○
	MTU4	MTIOC4A (input/output)/MTIOC4A# (input/output)	P13	○	×
			P72	○	○
		MTIOC4B (input/output)/MTIOC4B# (input/output)	P14	○	×
			P73	○	○
		MTIOC4C (input/output)/MTIOC4C# (input/output)	P16	○	×
			P75	○	○
		MTIOC4D (input/output)/MTIOC4D# (input/output)	P17	○	×
			P76	○	○
	MTU5	MTIC5U (input)/MTIC5U# (input)	P24	○	○
			P82	○	○
		MTIC5V (input)/MTIC5V# (input)	P23	○	○
			P81	○	○
		MTIC5W (input)/MTIC5W# (input)	P22	○	○
			P80	○	○
	MTU6	MTIOC6A (input/output)/MTIOC6A# (input/output)	PA1	○	○
		MTIOC6B (input/output)/MTIOC6B# (input/output)	P95	○	○
		MTIOC6C (input/output)/MTIOC6C# (input/output)	PA0	○	○
		MTIOC6D (input/output)/MTIOC6D# (input/output)	P92	○	○

Table 19.1 Allocation of Pin Functions to Multiple Pins (3/9)

Module/Function	Channel	Pin Functions	Allocation Port	Package	
				144-pin	100-pin
Multi-function timer unit 3	MTU7	MTIOC7A (input/output)/MTIOC7A# (input/output)	P94	○	○
		MTIOC7B (input/output)/MTIOC7B# (input/output)	P93	○	○
		MTIOC7C (input/output)/MTIOC7C# (input/output)	P91	○	○
		MTIOC7D (input/output)/MTIOC7D# (input/output)	P90	○	○
	MTU9	MTIOC9A (input/output)/MTIOC9A# (input/output)	P21	○	○
			P26	○	×
			PD7	○	○
		MTIOC9B (input/output)/MTIOC9B# (input/output)	P10	○	○
			PE0	○	○
		MTIOC9C (input/output)/MTIOC9C# (input/output)	P20	○	○
			PD6	○	○
			P25	○	×
		MTIOC9D (input/output)/MTIOC9D# (input/output)	P02	○	○
			PE1	○	○
	MTU	MTCLKA (input)/MTCLKA# (input)	P21	○	○
			P33	○	○
		MTCLKB (input)/MTCLKB# (input)	P20	○	○
			P32	○	○
		MTCLKC (input)/MTCLKC# (input)	P11	○	○
			P31	○	○
			PE4	○	○
		MTCLKD (input)/MTCLKD# (input)	P10	○	○
			P30	○	○
			PE3	○	○
		ADSM0 (output)	PA7	○	×
			PB2	○	○
			PC2	○	×
		ADSM1 (output)	PA6	○	×
			PB1	○	○
			PC1	○	×
General PWM timer	GPT0	GTIOC0A (input/output)/GTIOC0A# (input/output)	P12	○	×
			P71	○	○
			PD2	○	○
		GTIOC0B (input/output)/GTIOC0B# (input/output)	P15	○	×
			P74	○	○
			PD1	○	○
	GPT1	GTIOC1A (input/output)/GTIOC1A# (input/output)	P13	○	×
			P72	○	○
			PD0	○	○
		GTIOC1B (input/output)/GTIOC1B# (input/output)	P16	○	×
			P75	○	○
			PB7	○	○

Table 19.1 Allocation of Pin Functions to Multiple Pins (4/9)

Module/Function	Channel	Pin Functions	Allocation Port	Package	
				144-pin	100-pin
General PWM timer	GPT2	GTIOC2A (input/output)/GTIOC2A# (input/output)	P14	○	×
			P73	○	○
			PB6	○	○
		GTIOC2B (input/output)/GTIOC2B# (input/output)	P17	○	×
			P76	○	○
			PB5	○	○
	GPT3	GTIOC3A (input/output)/GTIOC3A# (input/output)	PD7	○	○
		GTIOC3B (input/output)/GTIOC3B# (input/output)	PD6	○	○
	GPT	GTECLKA (input)	PD5	○	○
		GTECLKB (input)	PD4	○	○
		GTECLKC (input)	PD3	○	○
		GTECLKD (input)	PB4	○	○
		GTETRG (input)	PB4	○	○
			PG2	○	×
		GTADSM0 (output)	P35	○	×
			PA3	○	○
			PC2	○	×
		GTADSM1 (output)	P34	○	×
			PA2	○	○
			PC1	○	×
8-bit timer	TMR0	TMO0 (output)	P33	○	○
			P35	○	×
			PB0	○	○
			PD3	○	○
		TMCI0 (input)	PB1	○	○
			PD4	○	○
		TMRI0 (input)	PB2	○	○
			PD5	○	○
	TMR1	TMO1 (output)	PD6	○	○
			PF0	○	×
		TMCI1 (input)	PD2	○	○
			PE0	○	○
		TMRI1 (input)	PD7	○	○
	TMR2	TMO2 (output)	P23	○	○
			PA0	○	○
			PA7	○	×
			PD1	○	○
		TMCI2 (input)	P24	○	○
		TMRI2 (input)	P22	○	○
	TMR3	TMO3 (output)	P11	○	○
			PF2	○	×
		TMCI3 (input)	PA5	○	○
		TMRI3 (input)	P10	○	○

Table 19.1 Allocation of Pin Functions to Multiple Pins (5/9)

Module/Function	Channel	Pin Functions	Allocation Port	Package	
				144-pin	100-pin
8-bit timer	TMR4	TMO4 (output)	P22	○	○
			P34	○	×
			P82	○	○
			PA1	○	○
			PD2	○	○
		TMCI4 (input)	P21	○	○
			P81	○	○
		TMRI4 (input)	P20	○	○
			P80	○	○
	TMR5	TMO5 (output)	PE1	○	○
			PF1	○	×
		TMCI5 (input)	PE0	○	○
		TMRI5 (input)	PD7	○	○
	TMR6	TMO6 (output)	P24	○	○
			P32	○	○
			PA6	○	×
			PD0	○	○
		TMCI6 (input)	P30	○	○
			PD4	○	○
		TMRI6 (input)	P31	○	○
			PD5	○	○
	TMR7	TMO7 (output)	PA2	○	○
			PF3	○	×
		TMCI7 (input)	PA4	○	○
		TMRI7 (input)	PA3	○	○
CAN module	RSCAN0	CTXD0 (output)	PA0	○	○
			PF2	○	×
		CRXD0 (input)	PA1	○	○
			PF3	○	×
Port output enable 3	POE0	POE0# (input)	P70	○	○
	POE4	POE4# (input)	P96	○	○
	POE8	POE8# (input)	PB4	○	○
	POE10	POE10# (input)	PE2	○	○
			PE4	○	○
			PE6	○	×
	POE11	POE11# (input)	PE3	○	○
	POE12	POE12# (input)	P01	○	○
			P10	○	○

Table 19.1 Allocation of Pin Functions to Multiple Pins (6/9)

Module/Function	Channel	Pin Functions	Allocation Port	Package	
				144-pin	100-pin
Serial communications interface	SCI1	RXD1 (input)/SMISO1 (input/output)/SSCL1 (input/output)	PC3	○	×
			PD5	○	○
		TXD1 (output)/SMOSI1 (input/output)/SSDA1 (input/output)	PC4	○	×
			PD3	○	○
		SCK1 (input/output)	P25	○	×
			PD4	○	○
		CTS1# (input)/RTS1# (output)/SS1# (input)	P02	○	○
			P26	○	×
			PD6	○	○
	SCI5	RXD5 (input)/SMISO5 (input/output)/SSCL5 (input/output)	PB6	○	○
			PE0	○	○
		TXD5 (output)/SMOSI5 (input/output)/SSDA5 (input/output)	PB5	○	○
			PD7	○	○
		SCK5 (input/output)	PB7	○	○
			PD2	○	○
		CTS5# (input)/RTS5# (output)/SS5# (input)	PB4	○	○
			PE1	○	○
	SCI6	RXD6 (input)/SMISO6 (input/output)/SSCL6 (input/output)	P80	○	○
			PA5	○	○
			PB1	○	○
		TXD6 (output)/SMOSI6 (input/output)/SSDA6 (input/output)	P81	○	○
			PB0	○	○
			PB2	○	○
		SCK6 (input/output)	P82	○	○
			PA4	○	○
			PB3	○	○
		CTS6# (input)/RTS6# (output)/SS6# (input)	P10	○	○
			PA2	○	○
	SCI8	RXD8(input)/SMISO8 (input/output)/SSCL8 (input/output)	P83	○	×
			PC0	○	×
		TXD8 (output)/SMOSI8 (input/output)/SSDA8 (input/output)	P84	○	×
			PC1	○	×
		SCK8 (input/output)	PC2	○	×
		CTS8# (input)/RTS8# (output)/SS8# (input)	P35	○	×
			P96	○	×
	SCI9	RXD9 (input)/SMISO9 (input/output)/SSCL9 (input/output)	PG0	○	×
		TXD9 (output)/SMOSI9 (input/output)/SSDA9 (input/output)	PG1	○	×
		SCK9 (input/output)	PG2	○	×
		CTS9# (input)/RTS9# (output)/SS9# (input)	P34	○	×
			P70	○	×

Table 19.1 Allocation of Pin Functions to Multiple Pins (7/9)

Module/Function	Channel	Pin Functions	Allocation Port	Package	
				144-pin	100-pin
Serial communications interface	SCI11	RXD11 (input)/SMISO11 (input/output)/ SSCL11 (input/output)	PC6	○	×
			PD5	○	○
			PF1	○	×
		TXD11 (output)/SMOSI11 (input/output)/ SSDA11 (input/output)	PC5	○	×
			PD3	○	○
			PF0	○	×
		SCK11 (input/output)	PD4	○	○
			PF2	○	×
		CTS11# (input)/RTS11# (output)/SS11# (input)	PD6	○	○
			PF3	○	×
I^2C bus interface		SCL0 (input/output)	PB1	○	○
		SDA0 (input/output)	PB2	○	○
Serial peripheral interface		RSPCKA (input/output)	P24	○	○
			PA4	○	○
			PB3	○	○
			PD0	○	○
		MOSIA (input/output)	P23	○	○
			PB0	○	○
			PD2	○	○
		MISOA (input/output)	P22	○	○
			PA5	○	○
			PD1	○	○
		SSLA0 (input/output)	P30	○	○
			PA3	○	○
			PD6	○	○
		SSLA1 (output)	P31	○	○
			PA2	○	○
			PD7	○	○
		SSLA2 (output)	P32	○	○
			PA1	○	○
			PE0	○	○
		SSLA3 (output)	P33	○	○
			PA0	○	○
			PE1	○	○
12-bit A/D converter		AN000 (input)	P40	○	○
		AN001 (input)	P41	○	○
		AN002 (input)	P42	○	○
		AN003 (input)	P43	○	○
		AN016 (input)	P20	○	○
		AN100 (input)	P44	○	○
		AN101 (input)	P45	○	○
		AN102 (input)	P46	○	○
		AN103 (input)	P47	○	○
		AN116 (input)	P21	○	○

Table 19.1 Allocation of Pin Functions to Multiple Pins (8/9)

Module/Function	Channel	Pin Functions	Allocation Port	Package	
				144-pin	100-pin
12-bit A/D converter		AN200 (input)	P60	○	○
		AN201 (input)	P61	○	○
		AN202 (input)	P62	○	○
		AN203 (input)	P63	○	○
		AN204 (input)	P64	○	○
		AN205 (input)	P65	○	○
		AN206 (input)	P50	○	×
		AN207 (input)	P51	○	×
		AN208 (input)	P52	○	○
		AN209 (input)	P53	○	○
		AN210 (input)	P54	○	○
		AN211 (input)	P55	○	○
		ADTRG0# (input)	PA4	○	○
			P20	○	○
			PA1	○	○
		ADTRG1# (input)	P21	○	○
			PA5	○	○
		ADTRG2# (input)	P22	○	○
			PB0	○	○
		ADST0 (output)	P02	○	○
			P26	○	×
			PD6	○	○
		ADST1 (output)	P00	○	○
			P25	○	×
		ADST2 (output)	P01	○	○
			PC4	○	×
8-bit D/A converter		DA0	P24	○	○
		DA1	P23	○	○
Clock frequency accuracy measurement circuit		CACREF (input)	P23	○	○
			PB3	○	○
Comparator		COMP0 (output)	P24	○	○
			PF3	○	×
			PG2	○	×
		COMP1 (output)	P23	○	○
			PF2	○	×
			PG1	○	×
		COMP2 (output)	P22	○	○
			PF1	○	×
			PG0	○	×
		COMP3 (output)	P30	○	○
			PC0	○	×
			PF0	○	×
		CMPC00 (input)	P40	○	○
		CMPC01 (input)	P40	○	○

Table 19.1 Allocation of Pin Functions to Multiple Pins (9/9)

Module/Function	Channel	Pin Functions	Allocation Port	Package	
				144-pin	100-pin
Comparator		CMPC02 (input)	P45	○	○
		CMPC03 (input)	P45	○	○
		CMPC10 (input)	P44	○	○
		CMPC11 (input)	P44	○	○
		CMPC12 (input)	P46	○	○
		CMPC13 (input)	P46	○	○
		CMPC20 (input)	P45	○	○
		CMPC21 (input)	P45	○	○
		CMPC22 (input)	P40	○	○
		CMPC23 (input)	P40	○	○
		CMPC30 (input)	P46	○	○
		CMPC31 (input)	P46	○	○
		CMPC32 (input)	P44	○	○
		CMPC33 (input)	P44	○	○

19.2 Register Descriptions

Registers and bits for pins that are not present due to differences according to the package are reserved. Write the value after a reset when writing to such bits.

19.2.1 Write-Protect Register (PWPR)

Address(es): 0008 C11Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	B0WI	PFSWE	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	PFSWE	PFS Register Write Enable	0: Writing to the PFS register is disabled 1: Writing to the PFS register is enabled	R/W
b7	B0WI	PFSWE Bit Write Disable	0: Writing to the PFSWE bit is enabled 1: Writing to the PFSWE bit is disabled	R/W

PFSWE Bit (PFS Register Write Enable)

Writing to PmnPFS register is enabled only when the PFSWE bit is set to 1.
To set the PFSWE bit to 1, write 1 to the PFSWE bit after writing 0 to the B0WI bit.

B0WI Bit (PFSWE Bit Write Disable)

Writing to the PFSWE bit is enabled only when the B0WI bit is set to 0.

19.2.2 P0n Pin Function Control Register (P0nPFS) (n = 0 to 2)

Address(es): P00PFS 0008 C140h, P01PFS 0008 C141h, P02PFS 0008 C142h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	ISEL	—	PSEL[4:0]				
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	PSEL[4:0]	Pin Function Select	These bits select the peripheral function. For individual pin functions, see Table 19.2.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	ISEL	Interrupt Input Function Select	0: Not used as IRQn input pin 1: Used as IRQn input pin P00: IRQ2 (144-/100-pin) P01: IRQ4 (144-/100-pin) P02: IRQ5 (144-/100-pin)	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

The Pmn pin function control register (PmnPFS) selects the pin function.
Bits PSEL[4:0] select the peripheral function assigned to each port pin.
The ISEL bit is set when a pin is used as an IRQ input pin. This setting can be used with the combination of the peripheral function, though IRQn (external pin interrupt) of the same number should not be enabled by two or more pins. The ISEL bit to which IRQn is not specified is reserved.

Table 19.2 Register Settings for Input/Output Pin Function in 144-/100-pin

	Pin		
PSEL[4:0] Settings	P00	P01	P02
00000b (Initial value)	Hi-Z		
00001b	—	—	MTIOC9D
00011b	—	—	MTIOC9D#
00111b	—	POE12#	—
01001b	ADST1	ADST2	ADST0
01010b	—	—	CTS1# RTS1# SS1#

—: Do not specify this value.

19.2.3 P1n Pin Function Control Register (P1nPFS) (n = 0 to 7)

Address(es): P10PFS 0008 C148h, P11PFS 0008 C149h, P12PFS 0008 C14Ah, P13PFS 0008 C14Bh, P14PFS 0008 C14Ch, P15PFS 0008 C14Dh, P16PFS 0008 C14Eh, P17PFS 0008 C14Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	ISEL	—	PSEL[4:0]				
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	PSEL[4:0]	Pin Function Select	These bits select the peripheral function. For individual pin functions, see Table 19.3 and Table 19.4.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	ISEL	Interrupt Input Function Select	0: Not used as IRQn input pin 1: Used as IRQn input pin P10: IRQ0 (144-/100-pin) P11: IRQ1 (144-/100-pin)	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Table 19.3 Register Settings for Input/Output Pin Function in 144-pin

	Pin							
PSEL[4:0] Settings	**P10**	**P11**	**P12**	**P13**	**P14**	**P15**	**P16**	**P17**
00000b (Initial value)	Hi-Z							
00001b	MTIOC9B	MTIOC3A	MTIOC3B	MTIOC4A	MTIOC4B	MTIOC3D	MTIOC4C	MTIOC4D
00010b	MTCLKD	MTCLKC	—	—	—	—	—	—
00011b	MTIOC9B#	MTIOC3A#	MTIOC3B#	MTIOC4A#	MTIOC4B#	MTIOC3D#	MTIOC4C#	MTIOC4D#
00100b	MTCLKD#	MTCLKC#	—	—	—	—	—	—
00101b	TMRI3	TMO3	—	—	—	—	—	—
00111b	POE12#	—	—	—	—	—	—	—
01010b	CTS6# RTS6# SS6#	—	—	—	—	—	—	—
10100b	—	—	GTIOC0A	GTIOC1A	GTIOC2A	GTIOC0B	GTIOC1B	GTIOC2B
10110b	—	—	GTIOC0A#	GTIOC1A#	GTIOC2A#	GTIOC0B#	GTIOC1B#	GTIOC2B#

—: Do not specify this value.

Table 19.4 Register Settings for Input/Output Pin Function in 100-pin

	Pin	
PSEL[4:0] Settings	**P10**	**P11**
00000b (Initial value)	Hi-Z	
00001b	MTIOC9B	MTIOC3A
00010b	MTCLKD	MTCLKC
00011b	MTIOC9B#	MTIOC3A#
00100b	MTCLKD#	MTCLKC#
00101b	TMRI3	TMO3
00111b	POE12#	—
01010b	CTS6# RTS6# SS6#	—

—: Do not specify this value.

19.2.4 P2n Pin Function Control Register (P2nPFS) (n = 0 to 7)

Address(es): P20PFS 0008 C150h, P21PFS 0008 C151h, P22PFS 0008 C152h, P23PFS 0008 C153h, P24PFS 0008 C154h, P25PFS 0008 C155h, P26PFS 0008 C156h, P27PFS 0008 C157h

	b7	b6	b5	b4	b3	b2	b1	b0
	ASEL	ISEL	—	PSEL[4:0]				
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	PSEL[4:0]	Pin Function Select	These bits select the peripheral function. For individual pin functions, see Table 19.5 and Table 19.6.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	ISEL	Interrupt Input Function Select	0: Not used as IRQn input pin 1: Used as IRQn input pin P20: IRQ7 (144-/100-pin) P21: IRQ6 (144-/100-pin)	R/W
b7	ASEL	Analog Function Select	0: Used other than as analog pin 1: Used as analog pin P20: AN016, CVREFC0 (144-/100-pin) P21: AN116, CVREFC1 (144-/100-pin) P23: DA1 (144-/100-pin) P24: DA0 (144-/100-pin)	R/W

Table 19.5 Register Settings for Input/Output Pin Function in 144-pin

	Pin							
PSEL[4:0] Settings	**P20**	**P21**	**P22**	**P23**	**P24**	**P25**	**P26**	**P27**
00000b (Initial value)	Hi-Z							
00001b	MTIOC9C	MTIOC9A	MTIC5W	MTIC5V	MTIC5U	MTIOC9C	MTIOC9A	MTIOC1A
00010b	MTCLKB	MTCLKA	—	—	—	—	—	—
00011b	MTIOC9C#	MTIOC9A#	MTIC5W#	MTIC5V#	MTIC5U#	MTIOC9C#	MTIOC9A#	MTIOC1A#
00100b	MTCLKB#	MTCLKA#	—	—	—	—	—	—
00101b	TMRI4	TMCI4	TMRI2	TMO2	TMCI2	—	—	—
00110b	—	—	TMO4	—	TMO6	—	—	—
00111b	—	—	—	CACREF	—	—	—	—
01001b	ADTRG0#	ADTRG1#	ADTRG2#	—	—	ADST1	ADST0	—
01010b	—	—	—	—	—	SCK1	CTS1# RTS1# SS1#	—
01101b	—	—	MISOA	MOSIA	RSPCKA	—	—	—
10110b	—	—	COMP2	COMP1	COMP0	—	—	—

—: Do not specify this value.

Table 19.6 Register Settings for Input/Output Pin Function in 100-pin

	Pin					
PSEL[4:0] Settings	**P20**	**P21**	**P22**	**P23**	**P24**	**P27**
00000b (Initial value)	Hi-Z					
00001b	MTIOC9C	MTIOC9A	MTIC5W	MTIC5V	MTIC5U	MTIOC1A
00010b	MTCLKB	MTCLKA	—	—	—	—
00011b	MTIOC9C#	MTIOC9A#	MTIC5W#	MTIC5V#	MTIC5U#	MTIOC1A#
00100b	MTCLKB#	MTCLKA#	—	—	—	—
00101b	TMRI4	TMCI4	TMRI2	TMO2	TMCI2	—
00110b	—	—	TMO4	—	TMO6	—
00111b	—	—	—	CACREF	—	—
01001b	ADTRG0#	ADTRG1#	ADTRG2#	—	—	—
01101b	—	—	MISOA	MOSIA	RSPCKA	—
11110b	—	—	COMP2	COMP1	COMP0	—

—: Do not specify this value.

19.2.5 P3n Pin Function Control Register (P3nPFS) (n = 0 to 5)

Address(es): P30PFS 0008 C158h, P31PFS 0008 C159h, P32PFS 0008 C15Ah, P33PFS 0008 C15Bh, P34PFS 0008 C15Ch, P35PFS 0008 C15Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	ISEL	—	PSEL[4:0]				
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	PSEL[4:0]	Pin Function Select	These bits select the peripheral function. For individual pin functions, see Table 19.7 and Table 19.8.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	ISEL	Interrupt Input Function Select	0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ7 (144-/100-pin) P31: IRQ6 (144-/100-pin)	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Table 19.7 Register Settings for Input/Output Pin Function in 144-pin

	Pin					
PSEL[4:0] Settings	**P30**	**P31**	**P32**	**P33**	**P34**	**P35**
00000b (Initial value)	Hi-Z					
00001b	MTIOC0B	MTIOC0A	MTIOC3C	MTIOC3A	—	—
00010b	MTCLKD	MTCLKC	MTCLKB	MTCLKA	—	—
00011b	MTIOC0B#	MTIOC0A#	MTIOC3C#	MTIOC3A#	—	—
00100b	MTCLKD#	MTCLKC#	MTCLKB#	MTCLKA#	—	—
00101b	TMCI6	TMRI6	TMO6	TMO0	TMO4	TMO0
01010b	—	—	—	—	CTS9# RTS9# SS9#	CTS8# RST8# SS8#
01101b	SSLA0	SSLA1	SSLA2	SSLA3	—	—
10100b	—	—	—	—	GTADSM1	GTADSM0
11110b	COMP3	—	—	—	—	—

—: Do not specify this value.

Table 19.8 Register Settings for Input/Output Pin Function in 100-pin

	Pin			
PSEL[4:0] Settings	**P30**	**P31**	**P32**	**P33**
00000b (Initial value)	Hi-Z			
00001b	MTIOC0B	MTIOC0A	MTIOC3C	MTIOC3A
00010b	MTCLKD	MTCLKC	MTCLKB	MTCLKA
00011b	MTIOC0B#	MTIOC0A#	MTIOC3C#	MTIOC3A#
00100b	MTCLKD#	MTCLKC#	MTCLKB#	MTCLKA#
00101b	TMCI6	TMRI6	TMO6	TMO0
01101b	SSLA0	SSLA1	SSLA2	SSLA3
11110b	COMP3	—	—	—

—: Do not specify this value.

19.2.6 P4n Pin Function Control Register (P4nPFS) (n = 0 to 7)

Address(es): P40PFS 0008 C160h, P41PFS 0008 C161h, P42PFS 0008 C162h, P43PFS 0008 C163h, P44PFS 0008 C164h, P45PFS 0008 C165h, P46PFS 0008 C166h, P47PFS 0008 C167h

	b7	b6	b5	b4	b3	b2	b1	b0
	ASEL	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	ASEL	Analog Input Function Select	0: Not used as an analog pin 1: Used as an analog pin P40: AN000, CMPC00, CMPC01, CMPC22, CMPC23 (144-/100-pin) P41: AN001 (144-/100-pin) P42: AN002 (144-/100-pin) P43: AN003 (144-/100-pin) P44: AN100, CMPC10, CMPC11, CMPC32, CMPC33 (144-/100-pin) P45: AN101, CMPC02, CMPC03, CMPC20, CMPC21 (144-/100-pin) P46: AN102, CMPC12, CMPC13, CMPC30, CMPC31 (144-/100-pin) P47: AN103 (144-/100-pin)	R/W

The ASEL bit is set when a pin is used as an analog pin. The pin state cannot be read at this point.

19.2.7 P5n Pin Function Control Register (P5nPFS) (n = 0 to 5)

Address(es): P50PFS 0008 C168h, P51PFS 0008 C169h, P52PFS 0008 C16Ah, P53PFS 0008 C16Bh, P54PFS 0008 C16Ch, P55PFS 0008 C16Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	ASEL	ISEL	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	ISEL	Interrupt Input Function Select	0: Not used as IRQn input pin 1: Used as IRQn input pin P52: IRQ0 (144-/100-pin) P53: IRQ1 (144-/100-pin) P54: IRQ2 (144-/100-pin) P55: IRQ3 (144-/100-pin)	R/W
b7	ASEL	Analog Input Function Select	0: Not used as an analog pin 1: Used as an analog pin P50: AN206 (144-pin) P51: AN207 (144-pin) P52: AN208 (144-/100-pin) P53: AN209 (144-/100-pin) P54: AN210 (144-/100-pin) P55: AN211 (144-/100-pin)	R/W

The ASEL bit is set when a pin is used as an analog pin. The pin state cannot be read at this point.

19.2.8 P6n Pin Function Control Register (P6nPFS) (n = 0 to 5)

Address(es): P60PFS 0008 C170h, P61PFS 0008 C171h, P62PFS 0008 C172h, P63PFS 0008 C173h, P64PFS 0008 C174h, P65PFS 0008 C175h

	b7	b6	b5	b4	b3	b2	b1	b0
	ASEL	ISEL	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	ISEL	Interrupt Input Function Select	0: Not used as IRQn input pin 1: Used as IRQn input pin P60: IRQ4 (144-/100-pin) P61: IRQ5 (144-/100-pin) P62: IRQ6 (144-/100-pin) P63: IRQ7 (144-/100-pin)	R/W
b7	ASEL	Analog Input Function Select	0: Not used as an analog pin 1: Used as an analog pin P60: AN200 (144-/100-pin) P61: AN201 (144-/100-pin) P62: AN202 (144-/100-pin) P63: AN203 (144-/100-pin) P64: AN204 (144-/100-pin) P65: AN205 (144-/100-pin)	R/W

The ASEL bit is set when a pin is used as an analog pin. The pin state cannot be read at this point.

19.2.9 P7n Pin Function Control Register (P7nPFS) (n = 0 to 6)

Address(es): P70PFS 0008 C178h, P71PFS 0008 C179h, P72PFS 0008 C17Ah, P73PFS 0008 C17Bh, P74PFS 0008 C17Ch, P75PFS 0008 C17Dh, P76PFS 0008 C17Eh

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	PSEL[4:0]	Pin Function Select	These bits select the peripheral function. For individual pin functions, see Table 19.9 and Table 19.10.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	ISEL	Interrupt Input Function Select	0: Not used as IRQn input pin 1: Used as IRQn input pin P70: IRQ5 (144-/100-pin)	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Table 19.9 Register Settings for Input/Output Pin Function in 144-pin

	Pin						
PSEL[4:0] Settings	**P70**	**P71**	**P72**	**P73**	**P74**	**P75**	**P76**
00000b (Initial value)	Hi-Z						
00001b	—	MTIOC3B	MTIOC4A	MTIOC4B	MTIOC3D	MTIOC4C	MTIOC4D
00011b	—	MTIOC3B#	MTIOC4A#	MTIOC4B#	MTIOC3D#	MTIOC4C#	MTIOC4D#
00111b	POE0#	—	—	—	—	—	—
01010b	CTS9# RTS9# SS9#	—	—	—	—	—	—
10100b	—	GTIOC0A	GTIOC1A	GTIOC2A	GTIOC0B	GTIOC1B	GTIOC2B
10110b	—	GTIOC0A#	GTIOC1A#	GTIOC2A#	GTIOC0B#	GTIOC1B#	GTIOC2B#

—: Do not specify this value.

Table 19.10 Register Settings for Input/Output Pin Function in 100-pin

	Pin						
PSEL[4:0] Settings	**P70**	**P71**	**P72**	**P73**	**P74**	**P75**	**P76**
00000b (Initial value)	Hi-Z						
00001b	—	MTIOC3B	MTIOC4A	MTIOC4B	MTIOC3D	MTIOC4C	MTIOC4D
00011b	—	MTIOC3B#	MTIOC4A#	MTIOC4B#	MTIOC3D#	MTIOC4C#	MTIOC4D#
00111b	POE0#	—	—	—	—	—	—
10100b	—	GTIOC0A	GTIOC1A	GTIOC2A	GTIOC0B	GTIOC1B	GTIOC2B
10110b	—	GTIOC0A#	GTIOC1A#	GTIOC2A#	GTIOC0B#	GTIOC1B#	GTIOC2B#

—: Do not specify this value.

19.2.10 P8n Pin Function Control Register (P8nPFS) (n = 0 to 4)

Address(es): P80PFS 0008 C180h, P81PFS 0008 C181h, P82PFS 0008 C182h, P83PFS 0008 C183h, P84PFS 0008 C184h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	PSEL[4:0]				
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	PSEL[4:0]	Pin Function Select	These bits select the peripheral function. For individual pin functions, see Table 19.11 and Table 19.12.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Table 19.11 Register Settings for Input/Output Pin Function in 144-pin

	Pin				
PSEL[4:0] Settings	**P80**	**P81**	**P82**	**P83**	**P84**
00000b (Initial value)	Hi-Z				
00001b	MTIC5W	MTIC5V	MTIC5U	—	—
00011b	MTIC5W#	MTIC5V#	MTIC5U#	—	—
00101b	TMRI4	TMCI4	TMO4	—	—
01010b	RXD6 SMISO6 SSCL6	TXD6 SMOSI6 SSDA6	SCK6	RXD8 SMISO8 SSCL8	TXD8 SMOSI8 SSDA8

—: Do not specify this value.

Table 19.12 Register Settings for Input/Output Pin Function in 100-pin

	Pin		
PSEL[4:0] Settings	**P80**	**P81**	**P82**
00000b (Initial value)	Hi-Z		
00001b	MTIC5W	MTIC5V	MTIC5U
00011b	MTIC5W#	MTIC5V#	MTIC5U#
00101b	TMRI4	TMCI4	TMO4
01010b	RXD6 SMISO6 SSCL6	TXD6 SMOSI6 SSDA6	SCK6

19.2.11 P9n Pin Function Control Register (P9nPFS) (n = 0 to 6)

Address(es): P90PFS 0008 C188h, P91PFS 0008 C189h, P92PFS 0008 C18Ah, P93PFS 0008 C18Bh, P94PFS 0008 C18Ch, P95PFS 0008 C18Dh, P96PFS 0008 C18Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	ISEL	—	PSEL[4:0]				
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	PSEL[4:0]	Pin Function Select	These bits select the peripheral function. For individual pin functions, see Table 19.13 and Table 19.14.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	ISEL	Interrupt Input Function Select	0: Not used as IRQn input pin 1: Used as IRQn input pin P96: IRQ4 (144-/100-pin)	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Table 19.13 Register Settings for Input/Output Pin Function in 144-pin

	Pin						
PSEL[4:0] Settings	**P90**	**P91**	**P92**	**P93**	**P94**	**P95**	**P96**
00000b (Initial value)	Hi-Z						
00001b	MTIOC7D	MTIOC7C	MTIOC6D	MTIOC7B	MTIOC7A	MTIOC6B	—
00011b	MTIOC7D#	MTIOC7C#	MTIOC6D#	MTIOC7B#	MTIOC7A#	MTIOC6B#	—
00111b	—	—	—	—	—	—	POE4#
01010b	—	—	—	—	—	—	CTS8# RTS8# SS8#

—: Do not specify this value.

Table 19.14 Register Settings for Input/Output Pin Function in 100-pin

	Pin						
PSEL[4:0] Settings	**P90**	**P91**	**P92**	**P93**	**P94**	**P95**	**P96**
00000b (Initial value)	Hi-Z						
00001b	MTIOC7D	MTIOC7C	MTIOC6D	MTIOC7B	MTIOC7A	MTIOC6B	—
00011b	MTIOC7D#	MTIOC7C#	MTIOC6D#	MTIOC7B#	MTIOC7A#	MTIOC6B#	—
00111b	—	—	—	—	—	—	POE4#

—: Do not specify this value.

19.2.12 PAn Pin Function Control Register (PAnPFS) (n = 0 to 7)

Address(es): PA0PFS 0008 C190h, PA1PFS 0008 C191h, PA2PFS 0008 C192h, PA3PFS 0008 C193h, PA4PFS 0008 C194h, PA5PFS 0008 C195h, PA6PFS 0008 C196h, PA7PFS 0008 C197h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	ISEL	—	PSEL[4:0]				
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	PSEL[4:0]	Pin Function Select	These bits select the peripheral function. For individual pin functions, see Table 19.15 and Table 19.16.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	ISEL	Interrupt Input Function Select	0: Not used as IRQn input pin 1: Used as IRQn input pin PA5: IRQ1 (144-/100-pin)	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Table 19.15 Register Settings for Input/Output Pin Function in 144-pin

	Pin							
PSEL[4:0] Settings	PA0	PA1	PA2	PA3	PA4	PA5	PA6	PA7
00000b (Initial value)	Hi-Z							
00001b	MTIOC6C	MTIOC6A	MTIOC2B	MTIOC2A	MTIOC1B	MTIOC1A	—	—
00011b	MTIOC6C#	MTIOC6A#	MTIOC2B#	MTIOC2A#	MTIOC1B#	MTIOC1A#	—	—
00101b	TMO2	TMO4	TMO7	TMRI7	TMCI7	TMCI3	TMO6	TMO2
01001b	—	ADTRG0#	—	—	ADTRG0#	ADTRG1#	ADSM1	ADSM0
01010b	—	—	CTS6# RTS6# SS6#	—	SCK6	RXD6 SMISO6 SSCL6	—	—
01101b	SSLA3	SSLA2	SSLA1	SSLA0	RSPCKA	MISOA	—	—
10000b	CTXD0	CRXD0	—	—	—	—	—	—
10100b	—	—	GTADSM1	GTADSM0	—	—	—	—

—: Do not specify this value.

Table 19.16 Register Settings for Input/Output Pin Function in 100-pin

	Pin					
PSEL[4:0] Settings	PA0	PA1	PA2	PA3	PA4	PA5
00000b (Initial value)	Hi-Z					
00001b	MTIOC6C	MTIOC6A	MTIOC2B	MTIOC2A	MTIOC1B	MTIOC1A
00010b	MTIOC6C#	MTIOC6A#	MTIOC2B#	MTIOC2A#	MTIOC1B#	MTIOC1A#
00101b	TMO2	TMO4	TMO7	TMRI7	TMCI7	TMCI3
01001b	—	ADTRG0#	—	—	ADTRG0#	ADTRG1#
01010b	—	—	CTS6# RTS6# SS6#	—	SCK6	RXD6 SMISO6 SSCL6
01101b	SSLA3	SSLA2	SSLA1	SSLA0	RSPCKA	MISOA
10000b	CTXD0	CRXD0	—	—	—	—
10100b	—	—	GTADSM1	GTADSM0	—	—

—: Do not specify this value.

19.2.13 PBn Pin Function Control Register (PBnPFS) (n = 0 to 7)

Address(es): PB0PFS 0008 C198h, PB1PFS 0008 C199h, PB2PFS 0008 C19Ah, PB3PFS 0008 C19Bh, PB4PFS 0008 C19Ch, PB5PFS 0008 C19Dh, PB6PFS 0008 C19Eh, PB7PFS 0008 C19Fh

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	PSEL[4:0]	Pin Function Select	These bits select the peripheral function. For individual pin functions, see Table 19.17.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	ISEL	Interrupt Input Function Select	0: Not used as IRQn input pin 1: Used as IRQn input pin PB4: IRQ3 (144-/100-pin) PB6: IRQ5 (144-/100-pin)	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Table 19.17 Register Settings for Input/Output Pin Function in 144-/100-pin

	Pin							
PSEL[4:0] Settings	**PB0**	**PB1**	**PB2**	**PB3**	**PB4**	**PB5**	**PB6**	**PB7**
00000b (Initial value)	Hi-Z							
00001b	MTIOC0D	MTIOC0C	MTIOC0B	MTIOC0A	—	—	—	—
00011b	MTIOC0D#	MTIOC0C#	MTIOC0B#	MTIOC0A#	—	—	—	—
00101b	TMO0	TMCI0	TMRI0	—	—	—	—	—
00111b	—	—	—	CACREF	POE8#	—	—	—
01001b	ADTRG2#	ADSM1	ADSM0	—	—	—	—	—
01010b	TXD6 SMOSI6 SSDA6	RXD6 SMISO6 SSCL6	TXD6 SMOSI6 SSDA6	SCK6	CTS5# RTS5# SS5#	TXD5 SMOSI5 SSDA5	RXD5 SMISO5 SSCL5	SCK5
01101b	MOSIA	—	—	RSPCKA	—	—	—	—
01111b	—	SCL0	SDA0	—	—	—	—	—
10100b	—	—	—	—	GTETRG	GTIOC2B	GTIOC2A	GTIOC1B
10101b	—	—	—	—	GTECLKD	—	—	—
10110b	—	—	—	—	—	GTIOC2B#	GTIOC2A#	GTIOC1B#

—: Do not specify this value.

19.2.14 PCn Pin Function Control Register (PCnPFS) (n = 0 to 6)

Address(es): PC0PFS 0008 C1A0h, PC1PFS 0008 C1A1h, PC2PFS 0008 C1A2h, PC3PFS 0008 C1A3h, PC4PFS 0008 C1A4h, PC5PFS 0008 C1A5h, PC6PFS 0008 C1A6h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	PSEL[4:0]				
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	PSEL[4:0]	Pin Function Select	These bits select the peripheral function. For individual pin functions, see Table 19.18.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Table 19.18 Register Settings for Input/Output Pin Function in 144-pin

	Pin						
PSEL[4:0] Settings	**PC0**	**PC1**	**PC2**	**PC3**	**PC4**	**PC5**	**PC6**
00000b (Initial value)	Hi-Z						
00001b	—	—	—	—	—	MTIOC1B	MTIOC1A
00011b	—	—	—	—	—	MTIOC1B#	MTIOC1A#
01001b	—	ADSM1	ADSM0	—	ADST2	—	—
01010b	RXD8 SMISO8 SSCL8	TXD8 SMOSI8 SSDA8	SCK8	RXD1 SMISO1 SSCL1	TXD1 SMOSI1 SSDA1	—	—
01011b	—	—	—	—	—	TXD11 SMOSI11 SSDA11	RXD11 SMISO11 SSCL11
10100b	—	GTADSM1	GTADSM0	—	—	—	—
11110b	COMP3	—	—	—	—	—	—

—: Do not specify this value.

19.2.15 PDn Pin Function Control Register (PDnPFS) (n = 0 to 7)

Address(es): PD0PFS 0008 C1A8h, PD1PFS 0008 C1A9h, PD2PFS 0008 C1AAh, PD3PFS 0008 C1ABh, PD4PFS 0008 C1ACh, PD5PFS 0008 C1ADh, PD6PFS 0008 C1AEh, PD7PFS 0008 C1AFh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	ISEL	—	PSEL[4:0]				
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	PSEL[4:0]	Pin Function Select	These bits select the peripheral function. For individual pin functions, see Table 19.19.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	ISEL	Interrupt Input Function Select	0: Not used as IRQn input pin 1: Used as IRQn input pin PD4:IRQ2 (144-/100-pin) PD5:IRQ3 (144-/100-pin) PD6:IRQ5 (144-/100-pin)	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Table 19.19 Register Settings for Input/Output Pin Function in 144-/100-pin

	Pin							
PSEL[4:0] Settings	**PD0**	**PD1**	**PD2**	**PD3**	**PD4**	**PD5**	**PD6**	**PD7**
00000b (Initial value)	Hi-Z							
00001b	—	—	—	—	—	—	MTIOC9C	MTIOC9A
00011b	—	—	—	—	—	—	MTIOC9C#	MTIOC9A#
00101b	TMO6	TMO2	TMCI1	TMO0	TMCI0	TMRI0	TMO1	TMRI1
00110b	—	—	TMO4	—	TMCI6	TMRI6	—	TMRI5
01001b	—	—	—	—	—	—	ADST0	—
01010b	—	—	SCK5	TXD1 SMOSI1 SSDA1	SCK1	RXD1 SMISO1 SSCL1	CTS1# RTS1# SS1#	TXD5 SMOSI5 SSDA5
01011b	—	—	—	TXD11 SMOSI11 SSDA11	SCK11	RXD11 SMISO11 SSCL11	CTS11# RTS11# SS11#	—
01101b	RSPCKA	MISOA	MOSIA	—	—	—	SSLA0	SSLA1
10100b	GTIOC1A	GTIOC0B	GTIOC0A	—	—	—	GTIOC3B	GTIOC3A
10101b	—	—	—	GTECLKC	GTECLKB	GTECLKA	—	—
10110b	GTIOC1A#	GTIOC0B#	GTIOC0A#	—	—	—	GTIOC3B#	GTIOC3A#

—: Do not specify this value.

19.2.16 PEn Pin Function Control Register (PEnPFS) (n = 0 to 6)

Address(es): PE0PFS 0008 C1B0h, PE1PFS 0008 C1B1h, PE2PFS 0008 C1B2h, PE3PFS 0008 C1B3h, PE4PFS 0008 C1B4h, PE5PFS 0008 C1B5h, PE6PFS 0008 C1B6h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	ISEL	—	PSEL[4:0]				
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	PSEL[4:0]	Pin Function Select	These bits select the peripheral function. For individual pin functions, see Table 19.20 and Table 19.21.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	ISEL	Interrupt Input Function Select	0: Not used as IRQn input pin 1: Used as IRQn input pin PE3: IRQ2 (144-/100-pin) PE4: IRQ1 (144-/100-pin) PE5: IRQ0 (144-/100-pin) PE6: IRQ3(144-pin)	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Table 19.20 Register Settings for Input/Output Pin Function in 144-pin

	Pin					
PSEL[4:0] Settings	**PE0**	**PE1**	**PE2**	**PE3**	**PE4**	**PE6**
00000b (Initial value)	Hi-Z					
00001b	MTIOC9B	MTIOC9D	—	—	—	—
00010b	—	—	—	MTCLKD	MTCLKC	—
00011b	MTIOC9B#	MTIOC9D#	—	—	—	—
00100b	—	—	—	MTCLKD#	MTCLKC#	—
00101b	TMCI1	TMO5	—	—	—	—
00110b	TMCI5	—	—	—	—	—
00111b	—	—	POE10#	POE11#	POE10#	POE10#
01010b	RXD5 SMISO5 SSCL5	CTS5# RTS5# SS5#	—	—	—	—
01101b	SSLA2	SSLA3	—	—	—	—

—: Do not specify this value.
Note: The priority is given to NMI pin interrupt operation when the NMIER.NMIEN = 1

Table 19.21 Register Settings for Input/Output Pin Function in 100-pin

	Pin				
PSEL[4:0] Settings	**PE0**	**PE1**	**PE2**	**PE3**	**PE4**
00000b (Initial value)	Hi-Z				
00001b	MTIOC9B	MTIOC9D	—	—	—
00010b	—	—	—	MTCLKD	MTCLKC
00011b	MTIOC9B#	MTIOC9D#	—	—	—
00100b	—	—	—	MTCLKD#	MTCLKC#
00101b	TMCI1	TMO5	—	—	—
00110b	TMCI5	—	—	—	—
00111b	—	—	POE10#	POE11#	POE10#
01010b	RXD5 SMISO5 SSCL5	CTS5# RTS5# SS5#	—	—	—
01101b	SSLA2	SSLA3	—	—	—

—: Do not specify this value.
Note: The priority is given to NMI pin interrupt operation when the NMIER.NMIEN = 1

19.2.17 PFn Pin Function Control Register (PFnPFS) (n = 0 to 3)

Address(es): PF0PFS 0008 C1B8h, PF1PFS 0008 C1B9h, PF2PFS 0008 C1BAh, PF3PFS 0008 C1BBh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	PSEL[4:0]				
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	PSEL[4:0]	Pin Function Select	These bits select the peripheral function. For individual pin functions, see Table 19.22.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Table 19.22 Register Settings for Input/Output Pin Function in 144-pin

	Pin			
PSEL[4:0] Settings	**PF0**	**PF1**	**PF2**	**PF3**
00000b (Initial value)	Hi-Z			
00101b	TMO1	TMO5	TMO3	TMO7
01011b	TXD11 SMOSI11 SSDA11	RXD11 SMISO11 SSCL11	SCK11	CTS11# RTS11# SS11#
10000b	—	—	CTXD0	CRXD0
11110b	COMP3	COMP2	COMP1	COMP0

—: Do not specify this value.

19.2.18 PGn Pin Function Control Register (PGnPFS) (n = 0 to 2)

Address(es): PG0PFS 0008 C1C0h, PG1PFS 0008 C1C1h, PG2PFS 0008 C1C2h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	PSEL[4:0]				
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	PSEL[4:0]	Pin Function Select	These bits select the peripheral function. For individual pin functions, see Table 19.23.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Table 19.23 Register Settings for Input/Output Pin Function in 144-pin

	Pin		
PSEL[4:0] Settings	**PG0**	**PG1**	**PG2**
00000b (Initial value)	Hi-Z		
01010b	RXD9 SMISO9 SSCL9	TXD9 SMOSI9 SSDA9	SCK9
10100b	—	—	GTETRG
11110b	COMP2	COMP1	COMP0

—: Do not specify this value.

19.3 Usage Notes

19.3.1 Procedure for Specifying Input/Output Pin Function

Use the following procedure to specify the input/output pin functions.

(1) Clear the port mode register (PMR) to 0 to select the general I/O port function.
(2) Specify the assignments of input/output signals for peripheral functions to the desired pins.
(3) Enable writing to the Pmn pin function control register (PmnPFS) through the write-protect register (PWPR) setting. (m = 0 to 9, A to G; n = 0 to 7)
(4) Specify the input/output function for the pin through the PSEL[4:0] bit settings in the PmnPFS register.
(5) Clear the PFSWE bit in the PWPR register to 0 to disable writing to the PmnPFS register.
(6) Set the PMR to 1 as necessary to switch to the selected input/output function for the pin.

19.3.2 Notes on MPC Register Setting

(1) Settings of the Pmn pin function control register (PmnPFS) should be made only while the PMR register for the target pin is cleared to 0. If a Pmn pin function control register is set while the PMR register of corresponding pin is 1, unexpected edges may be input through the input pin or unexpected pulses are output through the output pin.
(2) Only the allowed values (functions) should be specified in the Pmn pin function control registers. If a value that is not allowed for the register is specified, correct operation is not guaranteed.
(3) Do not assign a single function to multiple pins through the MPC settings.
(4) Analog input functions for the A/D converter are multiplexed with input pins of ports 2, 4, 5 and 6. If a pin is to be used as an analog input, avoid loss of resolution by setting the given bits of the port mode register (PMR) and of the port direction register (PDR) to 0, i.e. configuring the pin as a general-purpose input, and setting the PmnPFS.ASEL bit to 1.
(5) Points to note regarding the port mode register (PMR), port direction register (PDR), and Pmn pin function control register (PmnPFS) settings for pins that have multiplexed pin functions are listed in Table 19.24.
The pin state is readable when the PmnPFS.ASEL bit is 0.
If the value of the PmnPFS.PSEL[4:0] bits is to be changed, do so while the PMR.Bj bit is 0.
(6) P23 and P24 also function as analog output pins for the D/A converter. When using these ports as analog output pins, set them as general inputs by setting the corresponding bits in the port mode register (PMR) and port direction register (PDR) to 0, and set the PmnPFS.ASEL bit to 1 and the PSEL[4:0] bits to 00000b, to avoid degradation of accuracy.

Table 19.24 Register Settings

Item	PMR.Bn	PDR.Bn	PmnPFS			Point to Note
			ASEL	ISEL	PSEL[4:0]	
After a reset	0	0	0	0	00000b	Pins function as general input port pins after release from the reset state.
General input ports	0	0	0	0/1	x	Set the ISEL bit to 1 if these are multiplexed with interrupt inputs.
General output ports	0	1	0	0	x	
Peripheral functions	1	x	0	0/1	Peripheral functions (see Table 19.2 to Table 19.23)	Set the ISEL bit to 1 if these are multiplexed with interrupt inputs.
Interrupt inputs	0	0	0	1	x	
NMI	x	x	x	x	x	Register settings are not required.
Analog inputs and outputs	0*2	0	1	x*1	x/00000b*3	Set these as general input port pins so that the output buffers are turned off.

x: Setting not required.
0/1: Setting the PmnPFS.ISEL bit to 0 makes the pin incapable of functioning as an IRQ pin.
Setting the PmnPFS.ISEL bit to 1 makes the pin capable of functioning as an IRQ pin (if the IRQ is selected from the multiplexed functions).
Note: - The pin state is readable when the PmnPFS.ASEL bit is 0.
- If the value of the PmnPFS.PSEL[4:0] bits is to be changed, do so while the PMR.Bn bit is 0.
- If an RIIC function is assigned to a port pin, clear the PCR.Bn (to 0); pulling up is automatically turned off for outputs from peripheral modules other than the RIIC.
Note 1. The pin does not function as the IRQn input pin even if the PmnPFS.ISEL bit is set to 1.
Note 2. Setting PORT4 to PORT6 are not required.
Note 3. When P23 and P24 are used as analog output of the D/A converter, set the PmnPFS.PSEL[4:0] bits to 00000b.

19.3.3 Note on Using Analog Functions

When an analog function is in use, configure the pin as a general-purpose input by setting the given bits of the port mode register (PMR) and of the port direction register (PDR) to 0, and then set the ASEL bit in the Pmn pin function control register (PmnPFS) to 1.

19.3.4 Note on PB1/PB2 Pin Input Level

PB1/PB2 input level is specified to TTL when SCL/SDA is selected in the PB1PFS.PSEL bit or PB2PFS.PSEL bit and SMBus is selected in the ICMR3.SMBS bit in RIIC. At this time, input levels of the PB1/PB2 port read also become TTL.

19.3.5 Notes when Switching to the General Input and Output Ports when a Source is Generated

When a POE source signal is generated, the pins specified in the PMMCRn register (n = 0 to 3) of the POE module switch to general I/O port pins. The settings of the port direction register (PDR) for the control pins and the port output data register (PODR) determine the states of the pins after switching. The value of the port mode register (PMR) is retained.

19.3.6 Notes on Inversion of the Input and Output Pins of the MTU and GPT

The PmnPFS.PSEL[4:0] bits for the corresponding pins can select inversion of the signals on the input and output pins of the MTU and GPT listed in Table 19.25. If this is selected, acquired input signals are inverted and output signals are inverted before output. Switch between the non-inverted and inverted input and output states while the PMR register setting for the corresponding pins is 0.

Table 19.25 I/O Pins of MTU and GPT (1/2)

Module/Function	Channel	Non-Inverted I/O Pin	Inverted I/O Pin
Multi-function timer unit 3	MTU0	MTIOC0A	MTIOC0A#
		MTIOC0B	MTIOC0B#
		MTIOC0C	MTIOC0C#
		MTIOC0D	MTIOC0D#
	MTU1	MTIOC1A	MTIOC1A#
		MTIOC1B	MTIOC1B#
	MTU2	MTIOC2A	MTIOC2A#
		MTIOC2B	MTIOC2B#
	MTU3	MTIOC3A	MTIOC3A#
		MTIOC3B	MTIOC3B#
		MTIOC3C	MTIOC3C#
		MTIOC3D	MTIOC3D#
	MTU4	MTIOC4A	MTIOC4A#
		MTIOC4B	MTIOC4B#
		MTIOC4C	MTIOC4C#
		MTIOC4D	MTIOC4D#
	MTU5	MTIC5U	MTIC5U#
		MTIC5V	MTIC5V#
		MTIC5W	MTIC5W#
	MTU6	MTIOC6A	MTIOC6A#
		MTIOC6B	MTIOC6B#
		MTIOC6C	MTIOC6C#
		MTIOC6D	MTIOC6D#
	MTU7	MTIOC7A	MTIOC7A#
		MTIOC7B	MTIOC7B#
		MTIOC7C	MTIOC7C#
		MTIOC7D	MTIOC7D#
	MTU9	MTIOC9A	MTIOC9A#
		MTIOC9B	MTIOC9B#
		MTIOC9C	MTIOC9C#
		MTIOC9D	MTIOC9D#
	MTU	MTCLKA	MTCLKA#
		MTCLKB	MTCLKB#
		MTCLKC	MTCLKC#
		MTCLKD	MTCLKD#

Table 19.25 I/O Pins of MTU and GPT (2/2)

Module/Function	Channel	Non-Inverted I/O Pin	Inverted I/O Pin
General PWM timer	GPT0	GTIOC0A	GTIOC0A#
		GTIOC0B	GTIOC0B#
	GPT1	GTIOC1A	GTIOC1A#
		GTIOC1B	GTIOC1B#
	GPT2	GTIOC2A	GTIOC2A#
		GTIOC2B	GTIOC2B#
	GPT3	GTIOC3A	GTIOC3A#
		GTIOC3B	GTIOC3B#

20. Multi-Function Timer Pulse Unit 3 (MTU3d)

20.1 Overview

This MCU has an on-chip multi-function timer pulse unit 3 (MTU3d), consisting of nine 16-bit timer channels. Table 20.1 shows the specifications of the MTU and Table 20.2 lists the functions of the MTU. Figure 20.1 and Figure 20.2 show block diagrams of the MTU.

Table 20.1 MTU Specifications

Item	Description
Pulse input/output	28 lines max.
Pulse input	3 lines
Count clock	11 clocks for each channel (14 clocks for MTU0 and MTU9, 12 clocks for MTU2, 10 clocks for MTU5, and four clocks for MTU1 & MTU2 (LWA = 1))
Operating frequency	Up to 80 MHz
Available operations	[MTU0 to MTU4, MTU6, MTU7, MTU9] • Waveform output on compare match • Input capture function (noise filter setting available) • Counter-clearing operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing on compare match or input capture • Simultaneous input and output to registers in synchronization with counter operations • Up to 14-phase PWM output in combination with synchronous operation
	[MTU0, MTU3, MTU4, MTU6, MTU7, MTU9] • Buffer operation specifiable
	[MTU1, MTU2] • Phase counting mode can be specified independently • 32-bit phase counting mode can be specified for interlocked operation of MTU1 and MTU2 (when TMDR3.LWA = 1) • Cascade connection operation available
	[MTU3, MTU4, MTU6, MTU7] • Through interlocked operation of MTU3/4 and MTU6/7, the positive and negative signals in six phases (12 phases in total) can be output in complementary PWM and reset PWM operation. • In complementary PWM mode, transfer of values from buffer registers to temporary registers on peaks and troughs of the timer-counter values or writing to the buffer registers (MTU4.TGRD and MTU7.TGRD) • Double-buffering selectable in complementary PWM mode
	[MTU3, MTU4] • Through interlocking with MTU0, a mode for driving AC synchronous motors (brushless DC motors) by using complementary PWM output and reset PWM output is settable and allows the selection of two types of waveform output (chopping or level)
	[MTU5] • Capable of operation as a dead-time compensation counter
	[MTU6, MTU7] • Through interlocking with MTU9, a mode for driving AC synchronous motors (brushless DC motors) by using complementary PWM output and reset PWM output is settable and allows the selection of two types of waveform output (chopping or level)
Interrupt skipping function	• In complementary PWM mode, interrupts on crests and troughs of counter values and triggers to start conversion by the A/D converter can be skipped
Interrupt sources	45 sources
Buffer operation	Automatic transfer of register data (transfer from the buffer register to the timer register)
Trigger generation	A/D converter start triggers can be generated
	A/D converter start request delaying function enables A/D converter to be started with any desired timing and to be synchronized with PWM output
Low power consumption function	Module stop mode can be set

Table 20.2 MTU Functions (1/2)

Item	MTU0	MTU1	MTU2	MTU1 & MTU2 (LWA = 1)	MTU3	MTU4	MTU5	MTU6	MTU7	MTU9
Count clock	PCLKA/1 PCLKA/2 PCLKA/4 PCLKA/8 PCLKA/16 PCLKA/32 PCLKA/64 PCLKA/256 PCLKA/1024 MTCLKA MTCLKB MTCLKC MTCLKD MTIOC1A	PCLKA/1 PCLKA/2 PCLKA/4 PCLKA/8 PCLKA/16 PCLKA/32 PCLKA/64 PCLKA/256 PCLKA/1024 MTCLKA MTCLKB	PCLKA/1 PCLKA/2 PCLKA/4 PCLKA/8 PCLKA/16 PCLKA/32 PCLKA/64 PCLKA/256 PCLKA/1024 MTCLKA MTCLKB MTCLKC	MTCLKA MTCLKB MTCLKC MTCLKD	PCLKA/1 PCLKA/2 PCLKA/4 PCLKA/8 PCLKA/16 PCLKA/32 PCLKA/64 PCLKA/256 PCLKA/1024 MTCLKA MTCLKB	PCLKA/1 PCLKA/2 PCLKA/4 PCLKA/8 PCLKA/16 PCLKA/32 PCLKA/64 PCLKA/256 PCLKA/1024 MTCLKA MTCLKB	PCLKA/1 PCLKA/2 PCLKA/4 PCLKA/8 PCLKA/16 PCLKA/32 PCLKA/64 PCLKA/256 PCLKA/1024 MTIOC1A	PCLKA/1 PCLKA/2 PCLKA/4 PCLKA/8 PCLKA/16 PCLKA/32 PCLKA/64 PCLKA/256 PCLKA/1024 MTCLKA MTCLKB	PCLKA/1 PCLKA/2 PCLKA/4 PCLKA/8 PCLKA/16 PCLKA/32 PCLKA/64 PCLKA/256 PCLKA/1024 MTCLKA MTCLKB	PCLKA/1 PCLKA/2 PCLKA/4 PCLKA/8 PCLKA/16 PCLKA/32 PCLKA/64 PCLKA/256 PCLKA/1024 MTCLKA MTCLKB MTCLKC MTCLKD MTIOC1A
External clock for phase counting mode	—	MTCLKA MTCLKB	MTCLKA MTCLKB MTCLKC MTCLKD	MTCLKA MTCLKB MTCLKC MTCLKD	—	—	—	—	—	—
General registers (TGR)	TGRA TGRB TGRE	TGRA TGRB	TGRA TGRB	TRGALW TRGBLW	TGRA TGRB	TGRA TGRB	TGRU TGRV TGRW	TGRA TGRB	TGRA TGRB	TGRA TGRB TGRE
General registers/ buffer registers	TGRC TGRD TGRF	—	—	—	TGRC TGRD TGRE	TGRC TGRD TGRE TGRF	—	TGRC TGRD TGRE	TGRC TGRD TGRE TGRF	TGRC TGRD TGRF
I/O pins	MTIOC0A MTIOC0B MTIOC0C MTIOC0D	MTIOC1A MTIOC1B	MTIOC2A MTIOC2B	MTIOC1A MTIOC1B	MTIOC3A MTIOC3B MTIOC3C MTIOC3D	MTIOC4A MTIOC4B MTIOC4C MTIOC4D	MTIC5U MTIC5V MTIC5W	MTIOC6A MTIOC6B MTIOC6C MTIOC6D	MTIOC7A MTIOC7B MTIOC7C MTIOC7D	MTIOC9A MTIOC9B MTIOC9C MTIOC9D
Counter clear function	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	TGRALW/ TGRBLW compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture
Compare match output: 0 output	✓	✓	✓	✓	✓	✓	—	✓	✓	✓
Compare match output: 1 output	✓	✓	✓	✓	✓	✓	—	✓	✓	✓
Compare match output: Toggle output	✓	✓	✓	✓	✓	✓	—	✓	✓	✓
Input capture function	✓	✓	✓	✓*1	✓	✓	✓	✓	✓	✓
Synchronous operation	✓	✓	✓	—	✓	✓	—	✓	✓	✓
PWM mode 1	✓	✓	✓	—	✓	✓	—	✓	✓	✓
PWM mode 2	✓	✓	✓	—	—	—	—	—	—	✓
Complementary PWM mode	—	—	—	—	✓	✓	—	✓	✓	—
Reset-synchronized PWM mode	—	—	—	—	✓	✓	—	✓	✓	—
AC synchronous motor drive mode	✓	—	—	—	✓	✓	—	✓	✓	✓
Phase counting mode	—	✓	✓	✓	—	—	—	—	—	—
Buffer operation	✓	—	—	—	✓	✓	—	✓	✓	✓
Dead time compensation counter function	—	—	—	—	—	—	✓	—	—	—
DTC activation	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	TGRALW/ TGRBLW compare match or input capture	TGR compare match or input capture	TGR compare match or input capture and TCNT overflow/ underflow (only in complement ary PWM mode)	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture and TCNT overflow/ underflow (only in complement ary PWM mode)	TGR compare match or input capture
A/D converter start trigger	TGRA compare match or input capture TGRE compare match	TGRA compare match or input capture	TGRA compare match or input capture	TGRALW compare match or input capture	TGRA compare match or input capture	TGRA compare match or input capture, or TCNT underflow (trough) in complement ary PWM mode	—	TGRA compare match or input capture	TGRA compare match or input capture, or TCNT underflow (trough) in complement ary PWM mode	TGRA compare match or input capture TGRE compare match

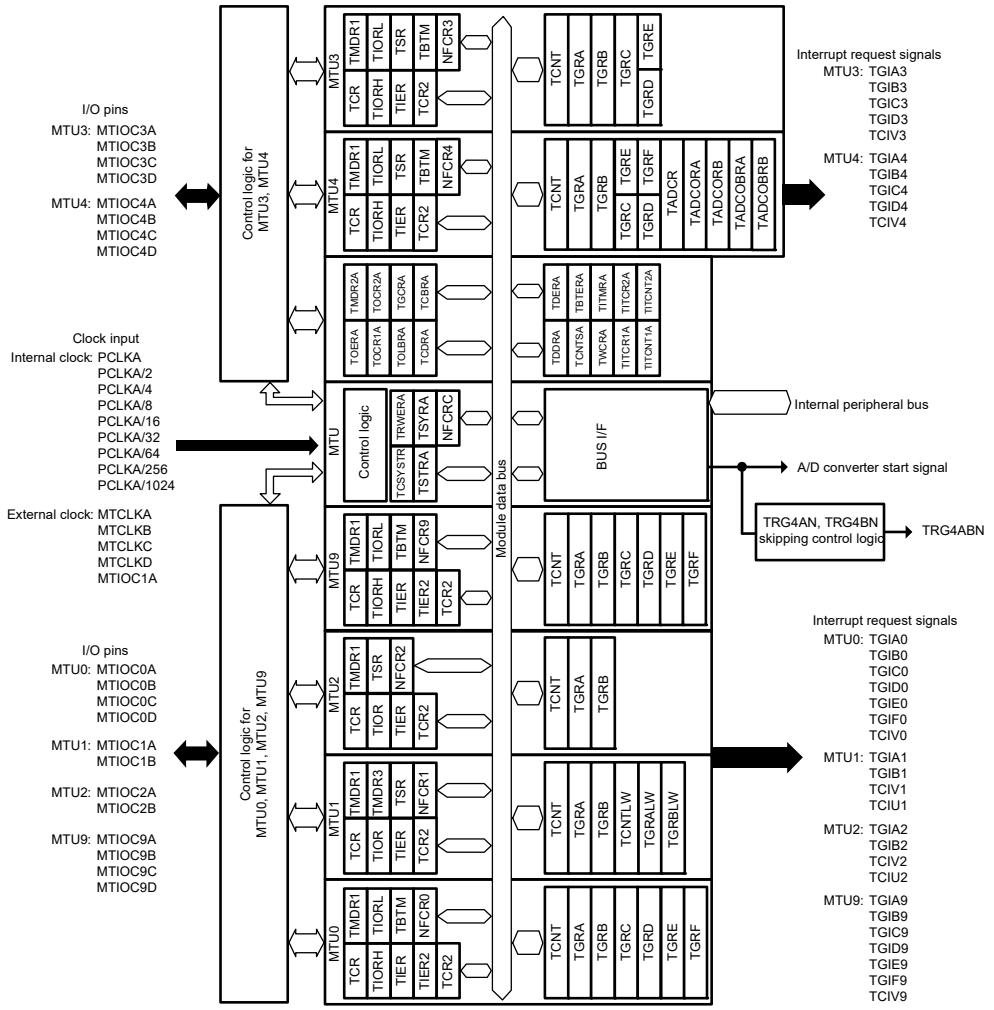
Table 20.2 MTU Functions (2/2)

Item	MTU0	MTU1	MTU2	MTU1 & MTU2 (LWA = 1)	MTU3	MTU4	MTU5	MTU6	MTU7	MTU9
Interrupt sources	Seven sources •Compare match or input capture 0A •Compare match or input capture 0B •Compare match or input capture 0C •Compare match or input capture 0D •Compare match0E •Compare match0F •Overflow	Four sources •Compare match or input capture 1A •Compare match or input capture 1B •Overflow •Underflow	Four sources •Compare match or input capture 2A •Compare match or input capture 2B •Overflow •Underflow	Four sources •Compare match or input capture 1A •Compare match or input capture 1B •Overflow •Underflow	Five sources •Compare match or input capture 3A •Compare match or input capture 3B •Compare match or input capture 3C •Compare match or input capture 3D •Overflow	Five sources •Compare match or input capture 4A •Compare match or input capture 4B •Compare match or input capture 4C •Compare match or input capture 4D •Overflow or underflow (only in complementary PWM mode)	Three sources •Compare match or input capture 5U •Compare match or input capture 5V •Compare match or input capture 5W	Five sources •Compare match or input capture 6A •Compare match or input capture 6B •Compare match or input capture 6C •Compare match or input capture 6D •Overflow	Five sources •Compare match or input capture 7A •Compare match or input capture 7B •Compare match or input capture 7C •Compare match or input capture 7D •Overflow or underflow (only in complementary PWM mode)	Seven sources •Compare match or input capture 9A •Compare match or input capture 9B •Compare match or input capture 9C •Compare match or input capture 9D •Compare match 9E •Compare match 9F •Overflow
A/D converter start request delaying function	—	—	—	—	—	•A/D converter start request at a match between TADCORA and TCNT or A/D converter start request at a match between TADCORB and TCNT	—	—	•A/D converter start request at a match between TADCORA and TCNT or A/D converter start request at a match between TADCORB and TCNT	—
Interrupt skipping 1	—	—	—	—	•Skips TGRA compare match interrupts	•Skips TCIV interrupts	—	•Skips TGRA compare match interrupts	•Skips TCIV interrupts	—
Interrupt skipping 2	—	—	—	—	—	•Skipping in compare count between TADCORA and TCNT, and TADCORB and TCNT	—	—	•Skipping in compare count between TADCORA and TCNT, and TADCORB and TCNT	—
Module stop function	MSTPCRA.MSTPA9*2									

✓: Possible —: Not possible

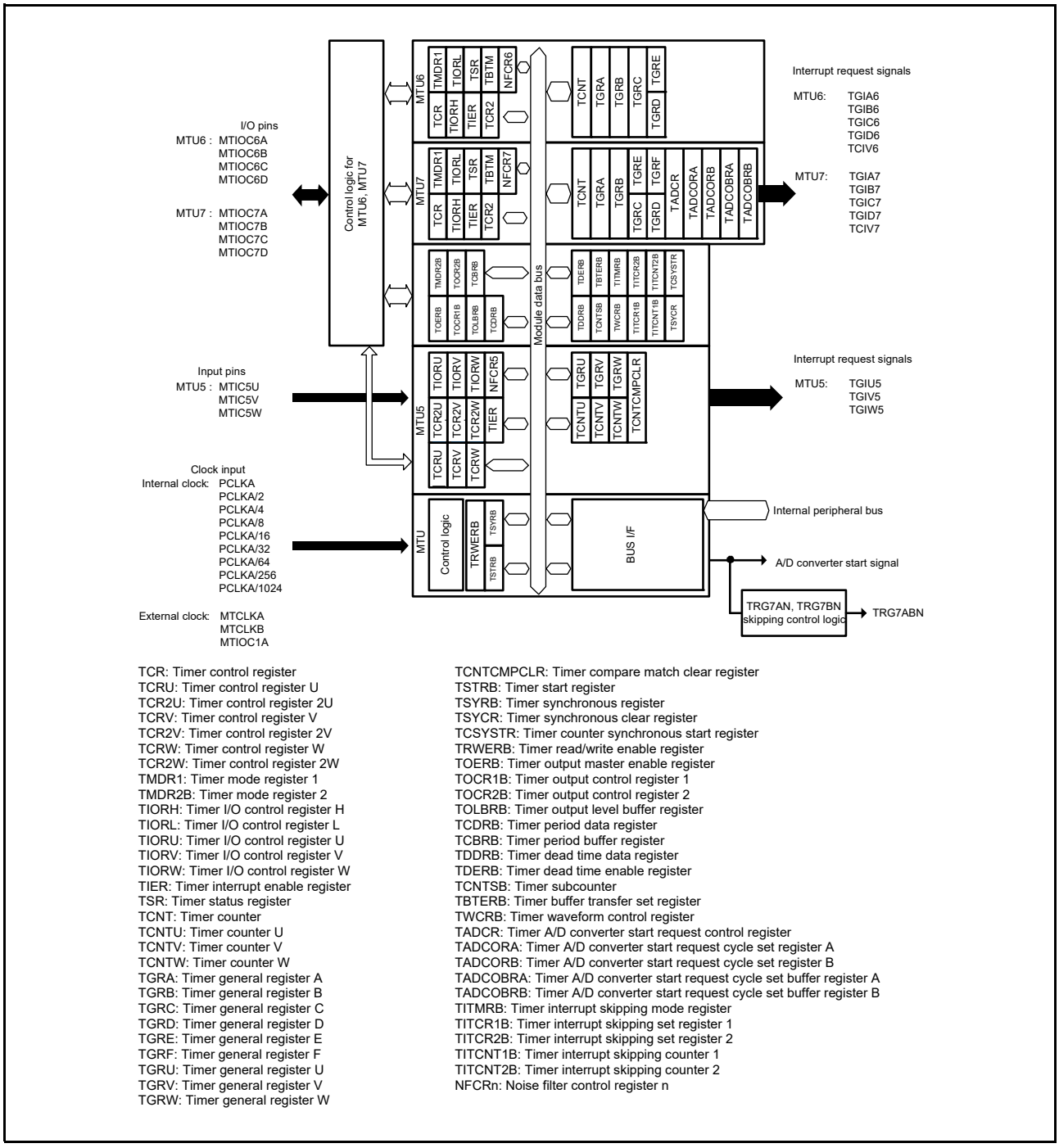
Note 1. When LWA is 1, the TGRALW capture source can be selected from either of the following: an input from MTIOC1A or MTU0.TGRA compare match/input capture event.
The TGRBLW capture source can be selected from any of the following: an input from MTIOC1B, MTU0.TGRC compare match/input capture event.

Note 2. For details on the module stop function, refer to section 11, Low Power Consumption.



TCR: Timer control register
TCR2: Timer control register 2
TMDR1: Timer mode register 1
TMDR2A: Timer mode register 2
TMDR3: Timer mode register 3
TIOR: Timer I/O control register
TIORH: Timer I/O control register H
TIORL: Timer I/O control register L
TIER: Timer interrupt enable register
TIER2: Timer interrupt enable register 2
TSR: Timer status register
TBTM: Timer buffer operation transfer mode register
TCNT: Timer counter
TCNTLW: Timer longword counter
TGRA: Timer general register A
TGRALW: Timer longword general register A
TGRB: Timer general register B
TGRBLW: Timer longword general register B
TGRC: Timer general register C
TGRD: Timer general register D
TGRE: Timer general register E
TGRF: Timer general register F
TSTRA: Timer start register
TSYRA: Timer synchronous register
TCSYSTR: Timer counter synchronous start register
TRWERA: Timer read/write enable register
TOERA: Timer output master enable register
TOCR1A: Timer output control register 1
TOCR2A: Timer output control register 2
TOLBRA: Timer output level buffer register
TGCRA: Timer gate control register A
TCNTSA: Timer subcounter
TCDRA: Timer period data register
TCBRA: Timer period buffer register
TDDRA: Timer dead time data register
TDERA: Timer dead time enable register
TBTERA: Timer buffer transfer set register
TWCRA: Timer waveform control register
TICCR: Timer input capture control register
TADCR: Timer A/D converter start request control register
TADCORA: Timer A/D converter start request cycle set register A
TADCORB: Timer A/D converter start request cycle set register B
TADCOBRA: Timer A/D converter start request cycle set buffer register A
TADCOBRB: Timer A/D converter start request cycle set buffer register B
TITMRA: Timer interrupt skipping mode register
TITCR1A: Timer interrupt skipping set register 1
TITCR2A: Timer interrupt skipping set register 2
TITCNT1A: Timer interrupt skipping counter 1
TITCNT2A: Timer interrupt skipping counter 2
NFCRn: Noise filter control register n

Figure 20.1 Block Diagram of MTU (MTU0 to MTU4, MTU9)



TCR: Timer control register
TCRU: Timer control register U
TCR2U: Timer control register 2U
TCRV: Timer control register V
TCR2V: Timer control register 2V
TCRW: Timer control register W
TCR2W: Timer control register 2W
TMDR1: Timer mode register 1
TMDR2B: Timer mode register 2
TIORH: Timer I/O control register H
TIORL: Timer I/O control register L
TIORU: Timer I/O control register U
TIORV: Timer I/O control register V
TIORW: Timer I/O control register W
TIER: Timer interrupt enable register
TSR: Timer status register
TCNT: Timer counter
TCNTU: Timer counter U
TCNTV: Timer counter V
TCNTW: Timer counter W
TGRA: Timer general register A
TGRB: Timer general register B
TGRC: Timer general register C
TGRD: Timer general register D
TGRE: Timer general register E
TGRF: Timer general register F
TGRU: Timer general register U
TGRV: Timer general register V
TGRW: Timer general register W

TCNTCMPCLR: Timer compare match clear register
TSTRB: Timer start register
TSYRB: Timer synchronous register
TSYCR: Timer synchronous clear register
TCSYSTR: Timer counter synchronous start register
TRWERB: Timer read/write enable register
TOERB: Timer output master enable register
TOCR1B: Timer output control register 1
TOCR2B: Timer output control register 2
TOLBRB: Timer output level buffer register
TCDRB: Timer period data register
TCBRB: Timer period buffer register
TDDRB: Timer dead time data register
TDERB: Timer dead time enable register
TCNTSB: Timer subcounter
TBTERB: Timer buffer transfer set register
TWCRB: Timer waveform control register
TADCR: Timer A/D converter start request control register
TADCORA: Timer A/D converter start request cycle set register A
TADCORB: Timer A/D converter start request cycle set register B
TADCOBRA: Timer A/D converter start request cycle set buffer register A
TADCOBRB: Timer A/D converter start request cycle set buffer register B
TITMRB: Timer interrupt skipping mode register
TITCR1B: Timer interrupt skipping set register 1
TITCR2B: Timer interrupt skipping set register 2
TITCNT1B: Timer interrupt skipping counter 1
TITCNT2B: Timer interrupt skipping counter 2
NFCRn: Noise filter control register n

Figure 20.2 Block Diagram of MTU (MTU5 to MTU7)

Table 20.3 shows the configuration of pins for the MTU.

Table 20.3 Pin Configuration of the MTU

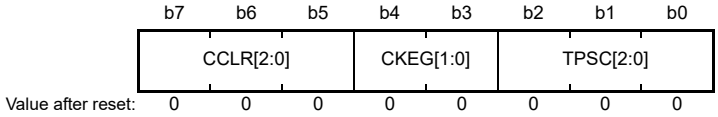
Channel	Pin Name	I/O	Function
MTU	MTCLKA	Input	External clock A input pin (MTU1 phase counting mode A phase input)
	MTCLKB	Input	External clock B input pin (MTU1 phase counting mode B phase input)
	MTCLKC	Input	External clock C input pin (MTU2 phase counting mode A phase input)
	MTCLKD	Input	External clock D input pin (MTU2 phase counting mode B phase input)
	ADSM0	Output	A/D conversion start request frame synchronization signal 0 output pin
	ADSM1	Output	A/D conversion start request frame synchronization signal 1 output pin
MTU0	MTIOC0A	I/O	MTU0 TGRA input capture input/output compare output/PWM output pin
	MTIOC0B	I/O	MTU0 TGRB input capture input/output compare output/PWM output pin
	MTIOC0C	I/O	MTU0 TGRC input capture input/output compare output/PWM output pin
	MTIOC0D	I/O	MTU0 TGRD input capture input/output compare output/PWM output pin
MTU1	MTIOC1A	I/O	MTU1 TGRA input capture input/output compare output/PWM output pin
	MTIOC1B	I/O	MTU1 TGRB input capture input/output compare output/PWM output pin
MTU2	MTIOC2A	I/O	MTU2 TGRA input capture input/output compare output/PWM output pin
	MTIOC2B	I/O	MTU2 TGRB input capture input/output compare output/PWM output pin
MTU3	MTIOC3A	I/O	MTU3 TGRA input capture input/output compare output/PWM output pin
	MTIOC3B	I/O	MTU3 TGRB input capture input/output compare output/PWM output pin
	MTIOC3C	I/O	MTU3 TGRC input capture input/output compare output/PWM output pin
	MTIOC3D	I/O	MTU3 TGRD input capture input/output compare output/PWM output pin
MTU4	MTIOC4A	I/O	MTU4 TGRA input capture input/output compare output/PWM output pin
	MTIOC4B	I/O	MTU4 TGRB input capture input/output compare output/PWM output pin
	MTIOC4C	I/O	MTU4 TGRC input capture input/output compare output/PWM output pin
	MTIOC4D	I/O	MTU4 TGRD input capture input/output compare output/PWM output pin
MTU5	MTIC5U	Input	MTU5 TGRU input capture input/external pulse input pin
	MTIC5V	Input	MTU5 TGRV input capture input/external pulse input pin
	MTIC5W	Input	MTU5 TGRW input capture input/external pulse input pin
MTU6	MTIOC6A	I/O	MTU6 TGRA input capture input/output compare output/PWM output pin
	MTIOC6B	I/O	MTU6 TGRB input capture input/output compare output/PWM output pin
	MTIOC6C	I/O	MTU6 TGRC input capture input/output compare output/PWM output pin
	MTIOC6D	I/O	MTU6 TGRD input capture input/output compare output/PWM output pin
MTU7	MTIOC7A	I/O	MTU7 TGRA input capture input/output compare output/PWM output pin
	MTIOC7B	I/O	MTU7 TGRB input capture input/output compare output/PWM output pin
	MTIOC7C	I/O	MTU7 TGRC input capture input/output compare output/PWM output pin
	MTIOC7D	I/O	MTU7 TGRD input capture input/output compare output/PWM output pin
MTU9	MTIOC9A	I/O	MTU9 TGRA input capture input/output compare output/PWM output pin
	MTIOC9B	I/O	MTU9 TGRB input capture input/output compare output/PWM output pin
	MTIOC9C	I/O	MTU9 TGRC input capture input/output compare output/PWM output pin
	MTIOC9D	I/O	MTU9 TGRD input capture input/output compare output/PWM output pin

20.2 Register Descriptions

20.2.1 Timer Control Register (TCR)

- MTU0.TCR, MTU1.TCR, MTU2.TCR, MTU3.TCR, MTU4.TCR, MTU6.TCR, MTU7.TCR, MTU9.TCR

Address(es): MTU0.TCR 000C 1300h, MTU1.TCR 000C 1380h, MTU2.TCR 000C 1400h, MTU3.TCR 000C 1200h, MTU4.TCR 000C 1201h, MTU6.TCR 000C 1A00h, MTU7.TCR 000C 1A01h, MTU9.TCR 000C 1580h



Bit	Symbol	Bit Name	Description	R/W
b2 to b0	TPSC[2:0]	Time Prescaler Select	Refer to Table 20.6 to Table 20.9.	R/W
b4, b3	CKEG[1:0]	Clock Edge Select	b4 b3 0 0: Count at rising edge 0 1: Count at falling edge 1 x: Count at both edges	R/W
b7 to b5	CCLR[2:0]	Counter Clear Source Select	Refer to Table 20.4 and Table 20.5.	R/W

x: Don’t care

The TCR register controls the TCNT operation for each channel in combination with the TCR2 register. The MTU has a total of 11 TCR registers, one each for MTU0 to MTU4, MTU6, MTU7, and MTU9 and three (TCRU, TCRV, and TCRW) for MTU5. TCR values should be specified only while TCNT operation is stopped.

TPSC[2:0] Bits (Time Prescaler Select)

These bits select the TCNT count clock source. The count clock source can be selected independently for each channel. Refer to Table 20.6 to Table 20.9 for details.

CKEG[1:0] Bits (Clock Edge Select)

These bits select the clock edge, including the MTIOC1A pin. When the internal clock is counted at both edges, the count clock period is halved (e.g. PCLKA/4 at both edges = PCLKA/2 at rising edge). If phase counting mode is used on MTU1 and MTU2, the setting of these bits is ignored and the phase counting mode setting has priority. Internal clock edge selection is valid when the count clock source is PCLKA/2 or slower. When PCLKA/1 or the overflow/underflow in another channel is selected for the count clock source, a value can be written to these bits but counter operation compiles with the initial value.

CCLR[2:0] Bits (Counter Clear Source Select)

These bits select the TCNT counter clearing source. Refer to Table 20.4 and Table 20.5 for details.

Table 20.4 CCLR[2:0] (MTU0, MTU3, MTU4, MTU6, MTU7, MTU9)

Channel	Bit 7 CCLR[2]	Bit 6 CCLR[1]	Bit 5 CCLR[0]	Description
MTU0 MTU3 MTU4 MTU6 MTU7 MTU9	0	0	0	TCNT clearing disabled
	0	0	1	TCNT cleared by TGRA compare match/input capture
	0	1	0	TCNT cleared by TGRB compare match/input capture
	0	1	1	TCNT cleared by counter clearing in another channel performing synchronous clearing/ synchronous operation*1
	1	0	0	TCNT clearing disabled
	1	0	1	TCNT cleared by TGRC compare match/input capture*2
	1	1	0	TCNT cleared by TGRD compare match/input capture*2
	1	1	1	TCNT cleared by counter clearing in another channel performing synchronous clearing/ synchronous operation*1

Note 1. Synchronous operation is selected by setting the TSYRA.SYNC or TSYRB.SYNC bit to 1
Note 2. When TGRC or TGRD is used as a buffer register, TCNT is not cleared because the buffer register setting has priority and compare match/input capture does not occur.

Table 20.5 CCLR[2:0] (MTU1 and MTU2)

Channel	Bit 7 Reserved*2	Bit 6 CCLR[1]	Bit 5 CCLR[0]	Description
MTU1 MTU2	0	0	0	TCNT clearing disabled
	0	0	1	TCNT cleared by TGRA compare match/input capture
	0	1	0	TCNT cleared by TGRB compare match/input capture
	0	1	1	TCNT cleared by counter clearing in another channel performing synchronous clearing/synchronous operation*1

Note 1. Synchronous operation is selected by setting the TSYRA.SYNC and TSYRB.SYNC bits to 1.
Note 2. Bit 7 is reserved in MTU1 and MTU2. It is read as 0. The write value is ignored.

- MTU5.TCRU, MTU5.TCRV, MTU5.TCRW

Address(es): MTU5.TCRU 000C 1C84h, MTU5.TCRV 000C 1C94h, MTU5.TCRW 000C 1CA4h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	TPSC[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	TPSC[1:0]	Time Prescaler Select	Refer to Table 20.10.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TPSC[1:0] Bits (Time Prescaler Select)

These bits select the TCNT count clock source. Refer to Table 20.10 for details.

20.2.2 Timer Control Register 2 (TCR2)

- MTU0.TCR2, MTU3.TCR2, MTU4.TCR2, MTU6.TCR2, MTU7.TCR2, MTU9.TCR2

Address(es): MTU0.TCR2 000C 1328h, MTU3.TCR2 000C 124Ch, MTU4.TCR2 000C 124Dh, MTU6.TCR2 000C 1A4Ch, MTU7.TCR2 000C 1A4Dh, MTU9.TCR2 000C 15A8h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	TPSC2[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

- MTU1.TCR2, MTU2.TCR2

Address(es): MTU1.TCR2 000C 1394h, MTU2.TCR2 000C 140Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	PCB[1:0]		TPSC2[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	TPSC2[2:0]	Time Prescaler Select	Refer to Table 20.6 to Table 20.9.	R/W
b4, b3	PCB[1:0]	Phase Counting Mode Function Expansion Control	Functional Expansion Control for Phase Counting Modes 2, 3, and 5	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The TCR2 register controls the TCNT operation for each channel in combination with the TCR register. The MTU has a total of 11 TCR2 registers, one each for MTU0 to MTU4, MTU6, MTU7, and MTU9 and three (TCRU, TCRV, and TCRW) for MTU5. TCR2 values should be specified only while TCNT operation is stopped.

TPSC2[2:0] Bits (Time Prescaler Select)

These bits select the TCNT count clock source. The count clock source can be selected independently for each channel. Refer to Table 20.6 to Table 20.9 for details.

PCB[1:0] Bits (Phase Counting Mode Function Expansion Control)

These bits control extended functions for phase counting mode 2, 3, and 5 in MTU1 and MTU2. Refer to section 20.3.6, Phase Counting Mode.

- MTU5.TCR2U, MTU5.TCR2V, MTU5.TCR2W

Address(es): MTU5.TCR2U 000C 1C85h, MTU5.TCR2V 000C 1C95h, MTU5.TCR2W 000C 1CA5h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	CKEG[1:0]		TPSC2[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	TPSC2[2:0]	Time Prescaler Select	Refer to Table 20.10.	R/W
b4, b3	CKEG[1:0]	Clock Edge Select	b4 b3 0 0: Counts at the rising edge. 0 1: Counts at the falling edge. 1 x: Counts at both edges.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

x: Don't care

TPSC2[2:0] Bits (Time Prescaler Select)

These bits select the TCNT count clock source. Refer to Table 20.10 for details.

CKEG[1:0] Bits (Clock Edge Select)

These bits select the edge of the count clock signal input from the MTIOC1A pin.

Table 20.6 TPSC[2:0], TPSC2[2:0] (MTU0 and MTU9)

	TCR2 register			TCR register			
	Bit 2	Bit 1	Bit 0	Bit 2	Bit 1	Bit 0	
Channel	TPSC2[2]	TPSC2[1]	TPSC2[0]	TPSC[2]	TPSC[1]	TPSC[0]	Description
MTU0 MTU9	0	0	0	0	0	0	Internal clock: counts on PCLKA/1
	0	0	0	0	0	1	Internal clock: counts on PCLKA/4
	0	0	0	0	1	0	Internal clock: counts on PCLKA/16
	0	0	0	0	1	1	Internal clock: counts on PCLKA/64
	0	0	0	1	0	0	External clock: counts on MTCLKA pin input
	0	0	0	1	0	1	External clock: counts on MTCLKB pin input
	0	0	0	1	1	0	External clock: counts on MTCLKC pin input
	0	0	0	1	1	1	External clock: counts on MTCLKD pin input
	0	0	1	x	x	x	Internal clock: counts on PCLKA/2
	0	1	0	x	x	x	Internal clock: counts on PCLKA/8
	0	1	1	x	x	x	Internal clock: counts on PCLKA/32
	1	0	0	x	x	x	Internal clock: counts on PCLKA/256
	1	0	1	x	x	x	Internal clock: counts on PCLKA/1024
	1	1	0	x	x	x	Setting prohibited
	1	1	1	x	x	x	External clock: counts on MTIOC1A pin input

x: Don't care

Table 20.7 TPSC[2:0], TPSC2[2:0] (MTU1)

	TCR2 register			TCR register			
	Bit 2	Bit 1	Bit 0	Bit 2	Bit 1	Bit 0	
Channel	TPSC2[2]	TPSC2[1]	TPSC2[0]	TPSC[2]	TPSC[1]	TPSC[0]	Description
MTU1	0	0	0	0	0	0	Internal clock: counts on PCLKA/1
	0	0	0	0	0	1	Internal clock: counts on PCLKA/4
	0	0	0	0	1	0	Internal clock: counts on PCLKA/16
	0	0	0	0	1	1	Internal clock: counts on PCLKA/64
	0	0	0	1	0	0	External clock: counts on MTCLKA pin input
	0	0	0	1	0	1	External clock: counts on MTCLKB pin input
	0	0	0	1	1	0	Internal clock: counts on PCLKA/256
	0	0	0	1	1	1	Overflow/underflow of MTU2.TCNT
	0	0	1	x	x	x	Internal clock: counts on PCLKA/2
	0	1	0	x	x	x	Internal clock: counts on PCLKA/8
	0	1	1	x	x	x	Internal clock: counts on PCLKA/32
	1	0	0	x	x	x	Internal clock: counts on PCLKA/1024
	1	0	1	x	x	x	Setting prohibited
	1	1	0	x	x	x	Setting prohibited
	1	1	1	x	x	x	Setting prohibited

x: Don't care

Note: This setting has no effect when MTU1 is in phase counting mode.

Table 20.8 TPSC[2:0], TPSC2[2:0] (MTU2)

	TCR2 register			TCR register			
	Bit 2	Bit 1	Bit 0	Bit 2	Bit 1	Bit 0	
Channel	TPSC2[2]	TPSC2[1]	TPSC2[0]	TPSC[2]	TPSC[1]	TPSC[0]	Description
MTU2	0	0	0	0	0	0	Internal clock: counts on PCLKA/1
	0	0	0	0	0	1	Internal clock: counts on PCLKA/4
	0	0	0	0	1	0	Internal clock: counts on PCLKA/16
	0	0	0	0	1	1	Internal clock: counts on PCLKA/64
	0	0	0	1	0	0	External clock: counts on MTCLKA pin input
	0	0	0	1	0	1	External clock: counts on MTCLKB pin input
	0	0	0	1	1	0	External clock: counts on MTCLKC pin input
	0	0	0	1	1	1	Internal clock: counts on PCLKA/1024
	0	0	1	x	x	x	Internal clock: counts on PCLKA/2
	0	1	0	x	x	x	Internal clock: counts on PCLKA/8
	0	1	1	x	x	x	Internal clock: counts on PCLKA/32
	1	0	0	x	x	x	Internal clock: counts on PCLKA/256
	1	0	1	x	x	x	Setting prohibited
	1	1	0	x	x	x	Setting prohibited
	1	1	1	x	x	x	Setting prohibited

x: Don't care

Note: This setting has no effect when the MTU2 is in phase counting mode.

Table 20.9 TPSC[2:0], TPSC2[2:0] (MTU3, MTU4, MTU6, MTU7)

	TCR2 register			TCR register			
	Bit 2	Bit 1	Bit 0	Bit 2	Bit 1	Bit 0	
Channel	TPSC2[2]	TPSC2[1]	TPSC2[0]	TPSC[2]	TPSC[1]	TPSC[0]	Description
MTU3 MTU4 MTU6 MTU7	0	0	0	0	0	0	Internal clock: counts on PCLKA/1
	0	0	0	0	0	1	Internal clock: counts on PCLKA/4
	0	0	0	0	1	0	Internal clock: counts on PCLKA/16
	0	0	0	0	1	1	Internal clock: counts on PCLKA/64
	0	0	0	1	0	0	Internal clock: counts on PCLKA/256
	0	0	0	1	0	1	Internal clock: counts on PCLKA/1024
	0	0	0	1	1	0	External clock: counts on MTCLKA pin input
	0	0	0	1	1	1	External clock: counts on MTCLKB pin input
	0	0	1	x	x	x	Internal clock: counts on PCLKA/2
	0	1	0	x	x	x	Internal clock: counts on PCLKA/8
	0	1	1	x	x	x	Internal clock: counts on PCLKA/32
	1	0	0	x	x	x	Setting prohibited
	1	0	1	x	x	x	Setting prohibited
	1	1	0	x	x	x	Setting prohibited
	1	1	1	x	x	x	Setting prohibited

x: Don't care

Table 20.10 TPSC[1:0], TPSC2[2:0] (MTU5)

	TCR2 register			TCR register		
	Bit 2	Bit 1	Bit 0	Bit 1	Bit 0	
Channel	TPSC2[2]	TPSC2[1]	TPSC2[0]	TPSC[1]	TPSC[0]	Description
MTU5	0	0	0	0	0	Internal clock: counts on PCLKA/1
	0	0	0	0	1	Internal clock: counts on PCLKA/4
	0	0	0	1	0	Internal clock: counts on PCLKA/16
	0	0	0	1	1	Internal clock: counts on PCLKA/64
	0	0	1	x	x	Internal clock: counts on PCLKA/2
	0	1	0	x	x	Internal clock: counts on PCLKA/8
	0	1	1	x	x	Internal clock: counts on PCLKA/32
	1	0	0	x	x	Internal clock: counts on PCLKA/256
	1	0	1	x	x	Internal clock: counts on PCLKA/1024
	1	1	0	x	x	Setting prohibited
	1	1	1	x	x	Internal clock: counts on MTIOC1A pin input

x: Don't care

20.2.3 Timer Mode Register 1 (TMDR1)

- MTU0.TMDR1, MTU9.TMDR1

Address(es): MTU0.TMDR1 000C 1301h, MTU9.TMDR1 000C 1581h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	BFE	BFB	BFA	MD[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

- MTU1.TMDR1, MTU2.TMDR1

Address(es): MTU1.TMDR1 000C 1381h, MTU2.TMDR1 000C 1401h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	MD[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

- MTU3.TMDR1, MTU4.TMDR1, MTU6.TMDR1, MTU7.TMDR1

Address(es): MTU3.TMDR1 000C 1202h, MTU4.TMDR1 000C 1203h, MTU6.TMDR1 000C 1A02h, MTU7.TMDR1 000C 1A03h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	BFB	BFA	MD[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	MD[3:0]	Mode Select	These bits specify the timer operating mode. Refer to Table 20.11 for details.	R/W
b4	BFA	Buffer Operation A	0: TGRA and TGRC operate normally 1: TGRA and TGRC used together for buffer operation	R/W
b5	BFB	Buffer Operation B	0: TGRB and TGRD operate normally 1: TGRB and TGRD used together for buffer operation	R/W
b6	BFE	Buffer Operation E	0: MTU0.TGRE and MTU0.TGRF, and MTU9.TGRE and MTU9.TGRF operate normally 1: MTU0.TGRE and MTU0.TGRF, and MTU9.TGRE and MTU9.TGRF used together for buffer operation	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

The TMDR1 register specifies the operating mode of each channel. The MTU has a total of eight TMDR1 registers, one each for MTU0 to MTU4, MTU6, MTU7, and MTU9. TMDR1 register values should be specified only while TCNT operation is stopped.

Table 20.11 Operating Mode Setting by MD[3:0] Bits (MTU0 to MTU4, MTU6, MTU7, and MTU9)

Bit 3	Bit 2	Bit 1	Bit 0									
MD[3]	MD[2]	MD[1]	MD[0]	Description	MTU0	MTU1	MTU2	MTU1 & MTU2 (LWA = 1)	MTU3	MTU4	MTU6	MTU7	MTU9
0	0	0	0	Normal mode	✓	✓	✓		✓	✓	✓	✓	✓
0	0	0	1	Setting prohibited									
0	0	1	0	PWM mode 1	✓	✓	✓		✓	✓	✓	✓	✓
0	0	1	1	PWM mode 2	✓	✓	✓						✓
0	1	0	0	Phase counting mode 1		✓	✓	✓					
0	1	0	1	Phase counting mode 2		✓	✓	✓					
0	1	1	0	Phase counting mode 3		✓	✓	✓					
0	1	1	1	Phase counting mode 4		✓	✓	✓					
1	0	0	0	Reset-synchronized PWM mode*1					✓		✓		
1	0	0	1	Phase counting mode 5		✓	✓	✓					
1	0	1	x	Setting prohibited									
1	1	0	0	Setting prohibited									
1	1	0	1	Complementary PWM mode 1 (transfer at crest)*1					✓		✓		
1	1	1	0	Complementary PWM mode 2 (transfer at trough)*1					✓		✓		
1	1	1	1	Complementary PWM mode 3 (transfer at crest and trough)*1					✓		✓		

x: Don't care

Note: Only set the corresponding operating mode listed above for each channel.

Note 1. Reset-synchronized PWM mode and complementary PWM mode can only be set for MTU3 and MTU6. When MTU3 or MTU6 is set to reset-synchronized PWM mode or complementary PWM mode, the MTU4 or MTU7 settings become ineffective and automatically conform to the MTU3 or MTU6 setting, respectively. MTU4 and MTU7 should be set to the initial values (normal mode).

BFA Bit (Buffer Operation A)

This bit specifies whether to operate TGRA in the normal way or to use TGRA and TGRC together for buffer operation. When TGRC is used as a buffer register, TGRC input capture/output compare does not take place in modes other than complementary PWM mode, but compare match with TGRC occurs in complementary PWM mode.

If a compare match occurs on MTU4 in the Tb interval in complementary PWM mode, the TGIEC bit in timer interrupt enable register (MTU4.TIER) should be set to 0.

In reset-synchronized PWM mode or complementary PWM mode, buffer operation in MTU3 and MTU4 (or MTU6 and MTU7) depends on the settings in the BFA bit of MTU3.TMDR1 (MTU6.TMDR1). The BFA bit of MTU4.TMDR1 (MTU7.TMDR1) should be set to 0.

In MTU1 and MTU2, which have no TGRC, this bit is reserved. It is read as 0. The write value should be 0.

Refer to Figure 20.49 for an illustration of the Tb interval in complementary PWM mode.

BFB Bit (Buffer Operation B)

This bit specifies whether to operate TGRB in the normal way or to use TGRB and TGRD together for buffer operation. When TGRD is used as a buffer register, TGRD input capture/output compare does not take place in modes other than complementary PWM mode, but compare match with TGRD occurs in complementary PWM mode.

If a compare match occurs on MTU4 in the Tb interval in complementary PWM mode, the TGIED bit in timer interrupt enable register (MTU4.TIER) should be set to 0.

In reset-synchronized PWM mode or complementary PWM mode, buffer operation in MTU3 and MTU4 (or MTU6 and MTU7) depends on the settings in the BFB bit of MTU3.TMDR1 (MTU6.TMDR1). The BFB bit of MTU4.TMDR1

(MTU7.TMDR1) should be set to 0.
In MTU1 and MTU2, which have no TGRD, this bit is reserved. It is read as 0. The write value should be 0.
Refer to Figure 20.49 for an illustration of the Tb interval in complementary PWM mode.

BFE Bit (Buffer Operation E)

This bit specifies whether to operate MTU0.TGRE and MTU0.TGRF, and MTU9.TGRE and MTU9.TGRF in the normal way or to use them together for buffer operation. Compare match with TGRF occurs even when TGRF is used as a buffer register.
In MTU0 to MTU4, MTU6, MTU7, this bit is reserved. It is read as 0. The write value should be 0.

20.2.4 Timer Mode Registers 2 (TMDR2A, TMDR2B)

Address(es): MTU.TMDR2A 000C 1270h, MTU.TMDR2B 000C 1A70h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DRS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DRS	Double Buffer Select	0: Double buffer function is disabled 1: Double buffer function is enabled	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TMDR2A and TMDR2B specify the double buffer function in complementary PWM mode 3 (transfer at the crest and trough of the counter value). The MTU has two TMDR2 registers, and one each for MTU3 (TMDR2A) and MTU6 (TMDR2B). TMDR2A and TMDR2B values should be specified only while TCNT operation is stopped.

DRS Bit (Double Buffer Select)

This bit enables or disables the double buffer function in complementary PWM mode.

20.2.5 Timer Mode Register 3 (TMDR3)

Address(es): MTU1.TMDR3 000C 1391h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PHCKSEL	LWA
Value after reset:	0	0	0	0	0	0	1	0

Bit	Symbol	Bit Name	Description	R/W
b0	LWA	MTU1/MTU2 Combination Longword Access Control	0: 16-bit access is enabled. 1: 32-bit access is enabled.	R/W
b1	PHCKSEL	External Input Phase Clock Select	0: MTCLKA and MTCLKB are selected for the external phase clock. 1: MTCLKC and MTCLKD are selected for the external phase clock.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The TMDR3 register controls longword access to a 32-bit register or counter in a combination of MTU1 and MTU2. There is only one TMDR3 register in MTU1. The counter (TCNTLW), general register A (TGRALW), and general register B (TGRBLW) of MTU1 and MTU2 are accessed in the combinations listed in Table 20.12.

LWA Bit (MTU1/MTU2 Combination Longword Access Control)

This bit selects a 32-bit access in a combination of MTU1 and MTU2.

When LWA is set to 0, the MTU1 and MTU2 independently operate as a 16-bit timer. therefore registers TCNTLW, TGRALW, and TGRBLW cannot be accessed.

When LWA is set to 1, MTU1 and MTU2 operate as a 32-bit cascaded timer and the timer is controlled by registers MTU1.TCR, MTU1.TCR2, MTU1.TIOR, and MTU1.TMDR1. The settings of registers MTU2.TCR, MTU2.TCR2, MTU2.TIOR, and MTU2.TMDR1 are disabled and the 16-bit registers (TCNT, TGRA, and TGRB) in MTU1 and MTU2 cannot be accessed. Furthermore, MTU2 input capture and compare match are also disabled.

The cascaded connection of MTU1 and MTU2 with the LWA bit set to 1 can only be used in phase counting mode, but not in normal mode, PWM1 mode, or PWM2 mode. Select phase counting mode when setting the LWA bit to 1.

Initialize the registers TCNT, TGRA, and TGRB in MTU1 and MTU2 in advance before setting the LWA bit to 1.

PHCKSEL Bit (External Input Phase Clock Select)

When the MTU1 and MTU2 registers are combined for 32-bit phase counting mode or MTU2 phase counting mode, this bit selects either the A- or B-phase signal from the external clock. Refer to Table 20.67, Clock Input Pins in Phase Counting Mode for details.

Table 20.12 Setting and Combination of the TMDR3 Register

	TMDR3.LWA = 0		TMDR3.LWA = 1	
Register	**Symbol**	**Access mode**	**Symbol**	**Access mode**
Counter in MTU1*1	MTU1.TCNT	Word	MTU1.TCNTLW	Longword
Counter in MTU2	MTU2.TCNT	Word		
General register A in MTU1	MTU1.TGRA	Word	MTU1.TGRALW	Longword
General register A in MTU2	MTU2.TGRA	Word		
General register B in MTU1	MTU1.TGRB	Word	MTU1.TGRBLW	Longword
General register B in MTU2	MTU2.TGRB	Word		

Note 1. When the LWA bit is set to 1, setting the count clock for MTU1 as MTU2.TCNT overflow/underflow is not required.

20.2.6 Timer I/O Control Register (TIOR)

- MTU0.TIORH, MTU1.TIOR, MTU2.TIOR, MTU3.TIORH, MTU4.TIORH, MTU6.TIORH, MTU7.TIORH, MTU9.TIORH

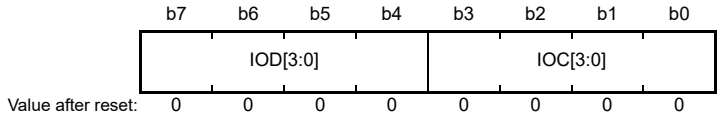
Address(es): MTU0.TIORH 000C 1302h, MTU1.TIOR 000C 1382h, MTU2.TIOR 000C 1402h, MTU3.TIORH 000C 1204h, MTU4.TIORH 000C 1206h, MTU6.TIORH 000C 1A04h, MTU7.TIORH 000C 1A06h, MTU9.TIORH 000C 1582h

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	IOA[3:0]	I/O Control A*1	Refer to the following tables. MTU0.TIORH: Table 20.27 MTU1.TIOR: Table 20.29 MTU2.TIOR: Table 20.30 MTU3.TIORH: Table 20.31 MTU4.TIORH: Table 20.33 MTU6.TIORH: Table 20.35 MTU7.TIORH: Table 20.37 MTU9.TIORH: Table 20.39	R/W
b7 to b4	IOB[3:0]	I/O Control B*1	Refer to the following tables. MTU0.TIORH: Table 20.13 MTU1.TIOR: Table 20.15 MTU2.TIOR: Table 20.16 MTU3.TIORH: Table 20.17 MTU4.TIORH: Table 20.19 MTU6.TIORH: Table 20.21 MTU7.TIORH: Table 20.23 MTU9.TIORH: Table 20.25	R/W

Note 1. When the value of IOn[3:0] (n = A, B) is changed to the output-prohibited state (0000b or 0100b) during low, high, or toggle output at compare match, this register is in Hi-Z.

- MTU0.TIORL, MTU3.TIORL, MTU4.TIORL, MTU6.TIORL, MTU7.TIORL, MTU9.TIORL

Address(es): MTU0.TIORL 000C 1303h, MTU3.TIORL 000C 1205h, MTU4.TIORL 000C 1207h, MTU6.TIORL 000C 1A05h, MTU7.TIORL 000C 1A07h, MTU9.TIORL 000C 1583h

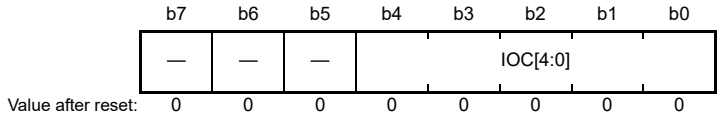


Bit	Symbol	Bit Name	Description	R/W
b3 to b0	IOC[3:0]	I/O Control C*1	Refer to the following tables. MTU0.TIORL: Table 20.28 MTU3.TIORL: Table 20.32 MTU4.TIORL: Table 20.34 MTU6.TIORL: Table 20.36 MTU7.TIORL: Table 20.38 MTU9.TIORL: Table 20.40	R/W
b7 to b4	IOD[3:0]	I/O Control D*1	Refer to the following tables. MTU0.TIORL: Table 20.14 MTU3.TIORL: Table 20.18 MTU4.TIORL: Table 20.20 MTU6.TIORL: Table 20.22 MTU7.TIORL: Table 20.24 MTU9.TIORL: Table 20.26	R/W

Note 1. When the value of IOn[3:0] (n = C, D) is changed to the output-prohibited state (0000b or 0100b) during low, high, or toggle output at compare match, this register is in Hi-Z.

- MTU5.TIORU, MTU5.TIORV, MTU5.TIORW

Address(es): MTU5.TIORU 000C 1C86h, MTU5.TIORV 000C 1C96h, MTU5.TIORW 000C 1CA6h



Bit	Symbol	Bit Name	Description	R/W
b4 to b0	IOC[4:0]	I/O Control C	Refer to the following table. MTU5.TIORU, MTU5.TIORV, MTU5.TIORW: Table 20.41	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The TIOR register controls the TGR register. The MTU has a total of 17 TIOR registers, two each for MTU0, MTU3, MTU4, MTU6, MTU7, and MTU9, one each for MTU1 and MTU2, and three (MTU5.TIORU/TIORV/TIORW) for MTU5. The TIOR register should be set when the TMDR register setting is normal mode, PWM mode, or phase counting mode.

Note that TIOR is affected by the TMDR1 setting.

The initial output specified by TIOR is valid when the counter is stopped (the CST bit in TSTRA and the CST bit in TSTRB are cleared to 0). Note also that, in PWM mode 2, the output at the point at which the counter is cleared to 0 is specified.

When TGRC or TGRD is designated for buffer operation, this setting is invalid and the register operates as a buffer register.

Table 20.13 TIORH (MTU0)

Bit 7	Bit 6	Bit 5	Bit 4	Description	
IOB[3]	IOB[2]	IOB[1]	IOB[0]	TGRB Register Function	MTIOC0B Pin Function
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	0	0	0	Input capture register	Input capture at rising edge.
1	0	0	1		Input capture at falling edge.
1	0	1	x		Input capture at both edges.
1	1	x	x		Capture input source is the clock source for counting in MTU1. Input capture on counting up or down by MTU1.TCNT (LWA = 0) or MTU1.TCNTLW (LWA = 1).*1

x: Don't care

Note 1. When PCLKA/1 is selected as the count clock for MTU1, MTU0 input capture is not generated. Do not select PCLKA/1 as the count clock for MTU1.

Table 20.14 TIORL (MTU0)

Bit 7	Bit 6	Bit 5	Bit 4	Description	
IOD[3]	IOD[2]	IOD[1]	IOD[0]	TGRD Register Function	MTIOC0D Pin Function
0	0	0	0	Output compare register*1	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	0	0	0	Input capture register*1	Input capture at rising edge.
1	0	0	1		Input capture at falling edge.
1	0	1	x		Input capture at both edges.
1	1	x	x		Capture input source is the clock source for counting in MTU1. Input capture on counting up or down by MTU1.TCNT (LWA = 0) or MTU1.TCNTLW (LWA = 1).*2

x: Don't care

Note 1. When the MTU0.TMDR1.BFB bit is set to 1 and MTU0.TGRD register is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Note 2. When PCLKA/1 is selected as the count clock for MTU1, MTU0 input capture is not generated. Do not select PCLKA/1 as the count clock for MTU1.

Table 20.15 TIOR (MTU1)

Bit 7	Bit 6	Bit 5	Bit 4	Description	
IOB[3]	IOB[2]	IOB[1]	IOB[0]	TGRB/TGRBLW Register Function	MTIOC1B Pin Function
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	0	0	0	Input capture register	Input capture at rising edge.
1	0	0	1		Input capture at falling edge.
1	0	1	x		Input capture at both edges.
1	1	0	x		Input capture at occurrence of compare match or input capture in the MTU0.TGRC register

x: Don't care

Table 20.16 TIOR (MTU2)

Bit 7	Bit 6	Bit 5	Bit 4	Description	
IOB[3]	IOB[2]	IOB[1]	IOB[0]	TGRB Register Function	MTIOC2B Pin Function
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Table 20.17 TIORH (MTU3)

Bit 7	Bit 6	Bit 5	Bit 4	Description	
IOB[3]	IOB[2]	IOB[1]	IOB[0]	TGRB Register Function	MTIOC3B Pin Function
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Table 20.18 TIORL (MTU3)

Bit 7	Bit 6	Bit 5	Bit 4	Description	
IOD[3]	IOD[2]	IOD[1]	IOD[0]	TGRD Register Function	MTIOC3D Pin Function
0	0	0	0	Output compare register*1	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register*1	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Note 1. When the MTU3.TMDR1.BFB bit is set to 1 and MTU3.TGRD register is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Table 20.19 TIORH (MTU4)

Bit 7	Bit 6	Bit 5	Bit 4	Description	
IOB[3]	IOB[2]	IOB[1]	IOB[0]	TGRB Register Function	MTIOC4B Pin Function
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Table 20.20 TIORL (MTU4)

Bit 7	Bit 6	Bit 5	Bit 4	Description	
IOD[3]	IOD[2]	IOD[1]	IOD[0]	TGRD Register Function	MTIOC4D Pin Function
0	0	0	0	Output compare register*1	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register*1	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Note 1. When the MTU4.TMDR1.BFB bit is set to 1 and MTU4.TGRD register is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Table 20.21 TIORH (MTU6)

Bit 7	Bit 6	Bit 5	Bit 4	Description	
IOB[3]	IOB[2]	IOB[1]	IOB[0]	TGRB Register Function	MTIOC6B Pin Function
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Table 20.22 TIORL (MTU6)

Bit 7	Bit 6	Bit 5	Bit 4	Description	
IOD[3]	IOD[2]	IOD[1]	IOD[0]	TGRD Register Function	MTIOC6D Pin Function
0	0	0	0	Output compare register*1	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register*1	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Note 1. When the MTU6.TMDR1.BFB bit is set to 1 and MTU6.TGRD register is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Table 20.23 TIORH (MTU7)

Bit 7	Bit 6	Bit 5	Bit 4	Description	
IOB[3]	IOB[2]	IOB[1]	IOB[0]	TGRB Register Function	MTIOC7B Pin Function
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Table 20.24 TIORL (MTU7)

Bit 7	Bit 6	Bit 5	Bit 4	Description	
IOD[3]	IOD[2]	IOD[1]	IOD[0]	TGRD Register Function	MTIOC7D Pin Function
0	0	0	0	Output compare register*1	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register*1	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Note 1. When the MTU7.TMDR1.BFB bit is set to 1 and MTU7.TGRD register is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Table 20.25 TIORH (MTU9)

Bit 7	Bit 6	Bit 5	Bit 4	Description	
IOB[3]	IOB[2]	IOB[1]	IOB[0]	TGRB Register Function	MTIOC9B Pin Function
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	0	0	0	Input capture register	Input capture at rising edge.
1	0	0	1		Input capture at falling edge.
1	0	1	x		Input capture at both edges.
1	1	x	x		Capture input source is the clock source for counting in MTU2. Input capture on counting up or down by MTU2.TCNT.*1

x: Don't care

Note 1. When PCLKA/1 is selected as the count clock for MTU2, MTU9 input capture is not generated. Do not select PCLKA/1 as the count clock for MTU2.

Table 20.26 TIORL (MTU9)

Bit 7	Bit 6	Bit 5	Bit 4	Description	
IOD[3]	IOD[2]	IOD[1]	IOD[0]	TGRD Register Function	MTIOC9D Pin Function
0	0	0	0	Output compare register*1	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	0	0	0	Input capture register*1	Input capture at rising edge.
1	0	0	1		Input capture at falling edge.
1	0	1	x		Input capture at both edges.
1	1	x	x		Capture input source is the clock source for counting in MTU2. Input capture on counting up or down by MTU2.TCNT.*2

x: Don't care

Note 1. When the MTU9.TMDR1.BFB bit is set to 1 and the MTU9.TGRD register is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Note 2. When PCLKA/1 is selected as the count clock for MTU2, MTU9 input capture is not generated. Do not select PCLKA/1 as the count clock for MTU2.

Table 20.27 TIORH (MTU0)

Bit 3	Bit 2	Bit 1	Bit 0	Description	
IOA[3]	IOA[2]	IOA[1]	IOA[0]	TGRA Register Function	MTIOC0A Pin Function
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	0	0	0	Input capture register	Input capture at rising edge.
1	0	0	1		Input capture at falling edge.
1	0	1	x		Input capture at both edges.
1	1	0	x		Capture input source is the clock source for counting in MTU1. Input capture on counting up or down by MTU1.TCNT (LWA = 0) or MTU1.TCNTLW (LWA = 1).*1

x: Don't care

Note 1. When PCLKA/1 is selected as the count clock for MTU1, MTU0 input capture is not generated. Do not select PCLKA/1 as the count clock for MTU1.

Table 20.28 TIORL (MTU0)

Bit 3	Bit 2	Bit 1	Bit 0	Description	
IOC[3]	IOC[2]	IOC[1]	IOC[0]	TGRC Register Function	MTIOC0C Pin Function
0	0	0	0	Output compare register*1	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	0	0	0	Input capture register*1	Input capture at rising edge.
1	0	0	1		Input capture at falling edge.
1	0	1	x		Input capture at both edges.
1	1	x	x		Capture input source is the clock source for counting in MTU1. Input capture on counting up or down by MTU1.TCNT (LWA = 0) or MTU1.TCNTLW (LWA = 1).*2

x: Don't care

Note 1. When the MTU0.TMDR1.BFB bit is set to 1 and MTU0.TGRC register is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Note 2. When PCLKA/1 is selected as the count clock for MTU1, MTU0 input capture is not generated. Do not select PCLKA/1 as the count clock for MTU1.

Table 20.29 TIOR (MTU1)

Bit 3	Bit 2	Bit 1	Bit 0	Description	
IOA[3]	IOA[2]	IOA[1]	IOA[0]	TGRA/TGRALW Register Function	MTIOC1A Pin Function
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	0	0	0	Input capture register	Input capture at rising edge.
1	0	0	1		Input capture at falling edge.
1	0	1	x		Input capture at both edges.
1	1	x	x		Input capture at generation of MTU0.TGRA compare match/input capture.

x: Don't care

Table 20.30 TIOR (MTU2)

Bit 3	Bit 2	Bit 1	Bit 0	Description	
IOA[3]	IOA[2]	IOA[1]	IOA[0]	TGRA Register Function	MTIOC2A Pin Function
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Table 20.31 TIORH (MTU3)

Bit 3	Bit 2	Bit 1	Bit 0	Description	
IOA[3]	IOA[2]	IOA[1]	IOA[0]	TGRA Register Function	MTIOC3A Pin Function
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Table 20.32 TIORL (MTU3)

Bit 3	Bit 2	Bit 1	Bit 0	Description	
IOC[3]	IOC[2]	IOC[1]	IOC[0]	TGRC Register Function	MTIOC3C Pin Function
0	0	0	0	Output compare register*1	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register*1	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Note 1. When the MTU3.TMDR1.BFB bit is set to 1 and MTU3.TGRC register is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Table 20.33 TIORH (MTU4)

Bit 3	Bit 2	Bit 1	Bit 0	Description	
IOA[3]	IOA[2]	IOA[1]	IOA[0]	TGRA Register Function	MTIOC4A Pin Function
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Table 20.34 TIORL (MTU4)

Bit 3	Bit 2	Bit 1	Bit 0	Description	
IOC[3]	IOC[2]	IOC[1]	IOC[0]	TGRC Register Function	MTIOC4C Pin Function
0	0	0	0	Output compare register*1	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register*1	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Note 1. When the MTU4.TMDR1.BFB bit is set to 1 and MTU4.TGRC register is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Table 20.35 TIORH (MTU6)

Bit 3	Bit 2	Bit 1	Bit 0	Description	
IOA[3]	IOA[2]	IOA[1]	IOA[0]	TGRA Register Function	MTIOC6A Pin Function
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Table 20.36 TIORL (MTU6)

Bit 3	Bit 2	Bit 1	Bit 0	Description	
IOC[3]	IOC[2]	IOC[1]	IOC[0]	TGRC Register Function	MTIOC6C Pin Function
0	0	0	0	Output compare register*1	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register*1	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Note 1. When the MTU6.TMDR1.BFB bit is set to 1 and MTU6.TGRC register is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Table 20.37 TIORH (MTU7)

Bit 3	Bit 2	Bit 1	Bit 0	Description	
IOA[3]	IOA[2]	IOA[1]	IOA[0]	TGRA Register Function	MTIOC7A Pin Function
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Table 20.38 TIORL (MTU7)

Bit 3	Bit 2	Bit 1	Bit 0	Description	
IOC[3]	IOC[2]	IOC[1]	IOC[0]	TGRC Register Function	MTIOC7C Pin Function
0	0	0	0	Output compare register*1	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register*1	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Note 1. When the MTU7.TMDR1.BFB bit is set to 1 and MTU7.TGRC register is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Table 20.39 TIORH (MTU9)

Bit 3	Bit 2	Bit 1	Bit 0	Description	
IOA[3]	IOA[2]	IOA[1]	IOA[0]	TGRA Register Function	MTIOC9A Pin Function
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	0	0	0	Input capture register	Input capture at rising edge.
1	0	0	1		Input capture at falling edge.
1	0	1	x		Input capture at both edges.
1	1	0	x		Capture input source is the clock source for counting in MTU2. Input capture on counting up or down by MTU2.TCNT.*1

x: Don't care

Note 1. When PCLKA/1 is selected as the count clock for MTU2, MTU9 input capture is not generated. Do not select PCLKA/1 as the count clock for MTU2.

Table 20.40 TIORL (MTU9)

Bit 3	Bit 2	Bit 1	Bit 0	Description	
IOC[3]	IOC[2]	IOC[1]	IOC[0]	TGRC Register Function	MTIOC9C Pin Function
0	0	0	0	Output compare register*1	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	0	0	0	Input capture register*1	Input capture at rising edge.
1	0	0	1		Input capture at falling edge.
1	0	1	x		Input capture at both edges.
1	1	x	x		Capture input source is the clock source for counting in MTU2. Input capture on counting up or down by MTU2.TCNT.*2

x: Don't care

Note 1. When the MTU9.TMDR1.BFA bit is set to 1 and the MTU9.TGRC register is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Note 2. When PCLKA/1 is selected as the count clock for MTU2, MTU9 input capture is not generated. Do not select PCLKA/1 as the count clock for MTU2.

Table 20.41 TIORU, TIORV, and TIORW (MTU5)

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Description	
IOC[4]	IOC[3]	IOC[2]	IOC[1]	IOC[0]	TGRU, TGRV, TGRW Registers Function	MTIC5U, MTIC5V, MTIC5W Pin Function
0	0	0	0	0	Output compare register	No function
0	0	0	0	1		Setting prohibited
0	0	0	1	x		Setting prohibited
0	0	1	x	x		Setting prohibited
0	1	x	x	x		Setting prohibited
1	0	0	0	0	Input capture register*1	Setting prohibited
1	0	0	0	1		Input capture at rising edge.
1	0	0	1	0		Input capture at falling edge.
1	0	0	1	1		Input capture at both edges.
1	0	1	x	x		Setting prohibited
1	1	0	0	0		Setting prohibited
1	1	0	0	1		Measurement of low pulse width of external input signal. Capture at trough in complementary PWM mode.
1	1	0	1	0		Measurement of low pulse width of external input signal. Capture at crest of complementary PWM mode.
1	1	0	1	1		Measurement of low pulse width of external input signal. Capture at crest and trough of complementary PWM mode.
1	1	1	0	0		Setting prohibited
1	1	1	0	1		Measurement of high pulse width of external input signal. Capture at trough in complementary PWM mode.
1	1	1	1	0		Measurement of high pulse width of external input signal. Capture at crest of complementary PWM mode.
1	1	1	1	1		Measurement of high pulse width of external input signal. Capture at crest and trough of complementary PWM mode.

x: Don't care

Note 1. Set the IOC[4:0] bits to 19h, 1Ah, 1Bh, 1Dh, 1Eh, or 1Fh only when using external pulse width measurement or only when using dead time compensation linked with MTU6 and MTU7. For details, refer to section 20.3.11, External Pulse Width Measurement and section 20.3.12, Dead Time Compensation.

20.2.7 Timer Compare Match Clear Register (TCNTCMPCLR)

Address(es): MTU5.TCNTCMPCLR 000C 1CB6h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	CMPCLR5U	CMPCLR5V	CMPCLR5W
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CMPCLR5W	TCNT Compare Clear 5W	0: Disables MTU5.TCNTW to be cleared to 0000h at MTU5.TCNTW and MTU5.TGRW compare match or input capture 1: Enables MTU5.TCNTW to be cleared to 0000h at MTU5.TCNTW and MTU5.TGRW compare match or input capture	R/W
b1	CMPCLR5V	TCNT Compare Clear 5V	0: Disables MTU5.TCNTV to be cleared to 0000h at MTU5.TCNTV and MTU5.TGRV compare match or input capture 1: Enables MTU5.TCNTV to be cleared to 0000h at MTU5.TCNTV and MTU5.TGRV compare match or input capture	R/W
b2	CMPCLR5U	TCNT Compare Clear 5U	0: Disables MTU5.TCNTU to be cleared to 0000h at MTU5.TCNTU and MTU5.TGRU compare match or input capture 1: Enables MTU5.TCNTU to be cleared to 0000h at MTU5.TCNTU and MTU5.TGRU compare match or input capture	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TCNTCMPCLR specifies requests to clear MTU5.TCNTU, MTU5.TCNTV, and MTU5.TCNTW. The MTU has one TCNTCMPCLR (on MTU5).

20.2.8 Timer Interrupt Enable Register (TIER)

- MTU1.TIER, MTU2.TIER

Address(es): MTU1.TIER 000C 1384h, MTU2.TIER 000C 1404h

	b7	b6	b5	b4	b3	b2	b1	b0
	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA
Value after reset:	0	0	0	0	0	0	0	0

- MTU0.TIER, MTU3.TIER, MTU6.TIER, MTU9.TIER

Address(es): MTU0.TIER 000C 1304h, MTU3.TIER 000C 1208h, MTU6.TIER 000C 1A08h, MTU9.TIER 000C 1584h

	b7	b6	b5	b4	b3	b2	b1	b0
	TTGE	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA
Value after reset:	0	0	0	0	0	0	0	0

- MTU4.TIER, MTU7.TIER

Address(es): MTU4.TIER 000C 1209h, MTU7.TIER 000C 1A09h

	b7	b6	b5	b4	b3	b2	b1	b0
	TTGE	TTGE2	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TGIEA	TGR Interrupt Enable A	0: Interrupt requests (TGIA) disabled 1: Interrupt requests (TGIA) enabled	R/W
b1	TGIEB	TGR Interrupt Enable B	0: Interrupt requests (TGIB) disabled 1: Interrupt requests (TGIB) enabled	R/W
b2	TGIEC	TGR Interrupt Enable C	0: Interrupt requests (TGIC) disabled 1: Interrupt requests (TGIC) enabled	R/W
b3	TGIED	TGR Interrupt Enable D	0: Interrupt requests (TGID) disabled 1: Interrupt requests (TGID) enabled	R/W
b4	TCIEV	Overflow Interrupt Enable	0: Interrupt requests (TCIV) disabled 1: Interrupt requests (TCIV) enabled	R/W
b5	TCIEU	Underflow Interrupt Enable	0: Interrupt requests (TCIU) disabled 1: Interrupt requests (TCIU) enabled	R/W
b6	TTGE2	A/D Converter Start Request Enable 2	0: A/D converter start request generation by MTUn.TCNT underflow (trough) disabled 1: A/D converter start request generation by MTUn.TCNT underflow (trough) enabled	R/W
b7	TTGE	A/D Converter Start Request Enable	0: A/D converter start request generation disabled 1: A/D converter start request generation enabled	R/W

n = 4, 7

The TIER register enables or disables interrupt requests from each channel. The MTU has a total of eleven TIER registers, two for MTU0 and MTU9 and one each for MTU1 to MTU7.

TGIEA and TGIEB Bits (TGR Interrupt Enable A and B)

Each bit enables or disables interrupt requests (TGIn) (n = A, B).

TGIEC and TGIED Bits (TGR Interrupt Enable C and D)

Each bit enables or disables an interrupt request (TGIn) (n = C, D).
In MTU1 and MTU2, these bits are reserved. They are read as 0. The write value should be 0.

TCIEV Bit (Overflow Interrupt Enable)

This bit enables or disables interrupt requests (TCIV).

TCIEU Bit (Underflow Interrupt Enable)

This bit enables or disables interrupt requests (TCIU).
In MTU0, MTU3, MTU4, MTU6, MTU7, and MTU9, this bit is reserved. It is read as 0. The write value should be 0.

TTGE2 Bit (A/D Converter Start Request Enable 2)

This bit enables or disables generation of A/D converter start requests by MTUn.TCNT underflow (trough) in complementary PWM mode (n = 4, 7).
In MTU0 to MTU3, MTU6, and MTU9, this bit is reserved. It is read as 0. The write value should be 0.

TTGE Bit (A/D Converter Start Request Enable)

This bit enables or disables generation of A/D converter start requests by TGRA input capture/compare match.

- MTU0.TIER2, MTU9.TIER2

Address(es): MTU0.TIER2 000C 1324h, MTU0.TIER2 000C 15A4h

	b7	b6	b5	b4	b3	b2	b1	b0
	TTGE2	—	—	—	—	—	TGIEF	TGIEE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TGIEE	TGR Interrupt Enable E	0: Interrupt requests (TGIE) disabled 1: Interrupt requests (TGIE) enabled	R/W
b1	TGIEF	TGR Interrupt Enable F	0: Interrupt requests (TGIF) disabled 1: Interrupt requests (TGIF) enabled	R/W
b6 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	TTGE2	A/D Converter Start Request Enable 2	0: A/D converter start request generation by compare match between MTU0.TCNT and MTU0.TGRE, and MTU9.TCNT and MTU9.TGRE disabled 1: A/D converter start request generation by compare match between MTU0.TCNT and MTU0.TGRE, and MTU9.TCNT and MTU9.TGRE enabled	R/W

TGIEE and TGIEF Bits (TGR Interrupt Enable E and F)

Each bit enables or disables interrupt requests by compare match between MTU0.TCNT and MTU0.TGRn, and MTU9.TCNT and MTU9.TGRn (n = E, F).

TTGE2 Bit (A/D Converter Start Request Enable 2)

Each bit enables or disables A/D converter start requests by compare match between MTU0.TCNT and MTU0.TGRE, and MTU9.TCNT and MTU9.TGRE.

- MTU5.TIER

Address(es): MTU5.TIER 000C 1CB2h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	TGIE5U	TGIE5V	TGIE5W
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	TGIE5W	TGR Interrupt Enable 5W	0: Interrupt requests TGIW5 disabled 1: Interrupt requests TGIW5 enabled	R/W
b1	TGIE5V	TGR Interrupt Enable 5V	0: Interrupt requests TGIV5 disabled 1: Interrupt requests TGIV5 enabled	R/W
b2	TGIE5U	TGR Interrupt Enable 5U	0: Interrupt requests TGIU5 disabled 1: Interrupt requests TGIU5 enabled	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TGIE5n Bits (TGR Interrupt Enable 5n)

Each bit enables or disables interrupt requests (TGIn5) (n = U, V, W).

20.2.9 Timer Status Register (TSR)

- MTU1.TSR, MTU2.TSR

Address(es): MTU1.TSR 000C 1385h, MTU2.TSR 000C 1405h

	b7	b6	b5	b4	b3	b2	b1	b0
	TCFD	—	—	—	—	—	—	—
Value after reset:	1	1	0	0	0	0	0	0

- MTU3.TSR, MTU4.TSR, MTU6.TSR, MTU7.TSR

Address(es): MTU3.TSR 000C 122Ch, MTU4.TSR 000C 122Dh, MTU6.TSR 000C 1A2Ch, MTU7.TSR 000C 1A2Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	TCFD	—	—	—	—	—	—	—
Value after reset:	1	1	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	—	Reserved	The read value is undefined.The write value should be 1.	R/W
b6	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b7	TCFD	Count Direction Flag	0: TCNT counts down 1: TCNT counts up	R

TSR indicates the states of each of the channels. The MTU has a total of six TSR registers, one each for MTU1 to MTU4, MTU6, and MTU7.

TCFD Flag (Count Direction Flag)

Status flag that indicates the direction in which TCNT is counting in MTU1 to MTU4, MTU6, and MTU7.

20.2.10 Timer Buffer Operation Transfer Mode Register (TBTM)

- MTU0.TBTM, MTU9.TBTM

Address(es): MTU0.TBTM 000C 1326h, MTU9.TBTM 000C 15A6h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	TTSE	TTSB	TTSA
Value after reset:	0	0	0	0	0	0	0	0

- MTU3.TBTM, MTU4.TBTM, MTU6.TBTM, MTU7.TBTM

Address(es): MTU3.TBTM 000C 1238h, MTU4.TBTM 000C 1239h, MTU6.TBTM 000C 1A38h, MTU7.TBTM 000C 1A39h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	TTSB	TTSA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TTSA	Timing Select A	0: When compare match A occurs in each channel, data is transferred from TGRC to TGRA 1: When TCNT is cleared in each channel, data is transferred from TGRC to TGRA	R/W
b1	TTSB	Timing Select B	0: When compare match B occurs in each channel, data is transferred from TGRD to TGRB 1: When TCNT is cleared in each channel, data is transferred from TGRD to TGRB	R/W
b2	TTSE	Timing Select E	0: When compare match E occurs in MTU0 or MTU9, data is transferred from MTU0.TGRF to MTU0.TGRE or MTU9.TGRF to MTU9.TGRE 1: When MTU0.TCNT or MTU9.TCNT is cleared, data is transferred from MTU0.TGRF to MTU0.TGRE or MTU9.TGRF to MTU9.TGRE	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TBTM specifies the timing for transferring data from the buffer register to the timer general register in PWM mode. The MTU has a total of six TBTM registers, one each for MTU0, MTU3, MTU4, MTU6, MTU7, and MTU9.

TTSA Bit (Timing Select A)

This bit specifies the timing for transferring data from TGRC to TGRA in each channel when they are used together for buffer operation. When a channel is not set to PWM mode, do not set the TTSA bit in the channel to 1.

TTSB Bit (Timing Select B)

This bit specifies the timing for transferring data from TGRD to TGRB in each channel when they are used together for buffer operation. When a channel is not set to PWM mode, do not set the TTSB bit in the channel to 1.

TTSE Bit (Timing Select E)

This bit specifies the timing for transferring data from MTU0.TGRF to MTU0.TGRE or MTU9.TGRF to MTU9.TGRE when they are used together for buffer operation.
In MTU3, MTU4, MTU6, and MTU7, this bit is reserved. It is read as 0 and the write value should be 0. When a channel is not set to PWM mode, do not set the TTSE bit in the channel to 1.

20.2.11 Timer Input Capture Control Register (TICCR)

Address(es): MTU1.TICCR 000C 1390h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	I2BE	I2AE	I1BE	I1AE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	I1AE	Input Capture Enable	0: Does not include the MTIOC1A pin in the MTU2.TGRA input capture conditions 1: Includes the MTIOC1A pin in the MTU2.TGRA input capture conditions	R/W
b1	I1BE	Input Capture Enable	0: Does not include the MTIOC1B pin in the MTU2.TGRB input capture conditions 1: Includes the MTIOC1B pin in the MTU2.TGRB input capture conditions	R/W
b2	I2AE	Input Capture Enable	0: Does not include the MTIOC2A pin in the MTU1.TGRA input capture conditions 1: Includes the MTIOC2A pin in the MTU1.TGRA input capture conditions	R/W
b3	I2BE	Input Capture Enable	0: Does not include the MTIOC2B pin in the MTU1.TGRB input capture conditions 1: Includes the MTIOC2B pin in the MTU1.TGRB input capture conditions	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TICCR specifies input capture conditions when MTU1.TCNT and MTU2.TCNT are cascaded. The MTU has one TICCR for MTU1.

20.2.12 Timer Synchronous Clear Register (TSYCR)

Address(es): MTU6.TSYCR 000C 1A50h

	b7	b6	b5	b4	b3	b2	b1	b0
	CE0A	CE0B	CE0C	CE0D	CE1A	CE1B	CE2A	CE2B
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CE2B	Clear Enable 2B	0: Disables counter clearing by the MTU2.TGIB2 interrupt generation timing. 1: Enables counter clearing by the MTU2.TGIB2 interrupt generation timing.	R/W
b1	CE2A	Clear Enable 2A	0: Disables counter clearing by the MTU2.TGIA2 interrupt generation timing*1. 1: Enables counter clearing by the MTU2.TGIA2 interrupt generation timing*1.	R/W
b2	CE1B	Clear Enable 1B	0: Disables counter clearing by the MTU1.TGIB1 interrupt generation timing*1. 1: Enables counter clearing by the MTU1.TGIB1 interrupt generation timing*1.	R/W
b3	CE1A	Clear Enable 1A	0: Disables counter clearing by the MTU1.TGIA1 interrupt generation timing*1. 1: Enables counter clearing by the MTU1.TGIA1 interrupt generation timing*1.	R/W
b4	CE0D	Clear Enable 0D	0: Disables counter clearing by the MTU0.TGID0 interrupt generation timing*1. 1: Enables counter clearing by the MTU0.TGID0 interrupt generation timing*1.	R/W
b5	CE0C	Clear Enable 0C	0: Disables counter clearing by the MTU0.TGIC0 interrupt generation timing*1. 1: Enables counter clearing by the MTU0.TGIC0 interrupt generation timing*1.	R/W
b6	CE0B	Clear Enable 0B	0: Disables counter clearing by the MTU0.TGIB0 interrupt generation timing*1. 1: Enables counter clearing by the MTU0.TGIB0 interrupt generation timing*1.	R/W
b7	CE0A	Clear Enable 0A	0: Disables counter clearing by the MTU0.TGIA0 interrupt generation timing*1. 1: Enables counter clearing by the MTU0.TGIA0 interrupt generation timing*1.	R/W

Note 1. This does not depend on the TIERn.TGIEm bit setting. (n = 0, 1, 2; m = A, B, C, D)

TSYCR specifies synchronous clear conditions for MTU6.TCNT and MTU7.TCNT. The MTU has one TSYCR for MTU1.

CEnm Bits (Clear Enable nm; n = 0, 1, 2; m = A, B, C, D)

These bits enable or disable counter clearing by the MTUn.TGImn interrupt generation timing.

20.2.13 Timer Counter (TCNT)

Address(es): MTU0.TCNT 000C 1306h, MTU1.TCNT 000C 1386h, MTU2.TCNT 000C 1406h, MTU3.TCNT 000C 1210h, MTU4.TCNT 000C 1212h, MTU5.TCNTU 000C 1C80h, MTU5.TCNTV 000C 1C90h, MTU5.TCNTW 000C 1CA0h, MTU6.TCNT 000C 1A10h, MTU7.TCNT 000C 1A12h, MTU9.TCNT 000C 1586h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note: TCNT must not be accessed in 8 bits; it should be accessed in 16 bits.

TCNT is a 16-bit readable/writable counter. The MTU has a total of 11 TCNT counters, one each for MTU0 to MTU4, MTU6, MTU7, and MTU9 and three (MTU5.TCNTU, TCNTV, and TCNTW) for MTU5. The TCNT counters in MTU0 to MTU4, MTU6, MTU7, and MTU9 are initialized to 0000h by a reset. MTU5.TCNTU, MTU5.TCNTV, and MTU5.TCNTW are initialized to 0000h by a reset.
In MTU0 to MTU4, MTU6, MTU7, and MTU9, the TCNT counters must not be accessed in 8-bit units; they should be accessed in 16- bit units.
The MTU1.TCNT and MTU2.TCNT counters are read as 0000h when TMDR3.LWA is 1. Refer to section 20.2.5, Timer Mode Register 3 (TMDR3) for details.

20.2.14 Timer Longword Counter (TCNTLW)

Address(es): MTU1.TCNTLW 000C 13A0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note: TCNTLW must not be accessed in 8 or 16 bits; it should be accessed in 32 bits.

The TCNTLW counter is a 32-bit readable/writable counter. Only one counter of this type is provided, and is formed by combining MTU1.TCNT and MTU2.TCNT. Such operation is only effective when TMDR3.LWA is 1. The TCNTLW counter is initialized to 0000 0000h by a reset. This counter is read as 0000 0000h when TMDR3.LWA is 0. Refer to section 20.2.5, Timer Mode Register 3 (TMDR3) for details. This register can only be used in 32-bit phase counting mode.

20.2.15 Timer General Register (TGR)

Address(es): MTU0.TGRA 000C 1308h, MTU0.TGRB 000C 130Ah, MTU0.TGRC 000C 130Ch, MTU0.TGRD 000C 130Eh, MTU0.TGRE 000C 1320h, MTU0.TGRF 000C 1322h,
MTU1.TGRA 000C 1388h, MTU1.TGRB 000C 138Ah,
MTU2.TGRA 000C 1408h, MTU2.TGRB 000C 140Ah,
MTU3.TGRA 000C 1218h, MTU3.TGRB 000C 121Ah, MTU3.TGRC 000C 1224h, MTU3.TGRD 000C 1226h, MTU3.TGRE 000C 1272h
MTU4.TGRA 000C 121Ch, MTU4.TGRB 000C 121Eh, MTU4.TGRC 000C 1228h, MTU4.TGRD 000C 122Ah, MTU4.TGRE 000C 1274h, MTU4.TGRF 000C 1276h,
MTU5.TGRU 000C 1C82h, MTU5.TGRV 000C 1C92h, MTU5.TGRW 000C 1CA2h,
MTU6.TGRA 000C 1A18h, MTU6.TGRB 000C 1A1Ah, MTU6.TGRC 000C 1A24h, MTU6.TGRD 000C 1A26h, MTU6.TGRE 000C 1A72h,
MTU7.TGRA 000C 1A1Ch, MTU7.TGRB 000C 1A1Eh, MTU7.TGRC 000C 1A28h, MTU7.TGRD 000C 1A2Ah, MTU7.TGRE 000C 1A74h, MTU7.TGRF 000C 1A76h,
MTU9.TGRA 000C 1588h, MTU9.TGRB 000C 158Ah, MTU9.TGRC 000C 158Ch, MTU9.TGRD 000C 158Eh, MTU9.TGRE 000C 15A0h, MTU9.TGRF 000C 15A2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: TGR must not be accessed in 8 bits; it should be accessed in 16 bits. The initial value of TGR is FFFFh.

The TGR register is 16-bit readable/writable register. The MTU has a total of 41 TGR registers, six for MTU0 and MTU9, two each for MTU1 and MTU2, five each for MTU3 and MTU6, six each for MTU4 and MTU7, and three for MTU5.

The TGRA, TGRB, TGRC, and TGRD registers function as either output compare or input capture registers. The TGRC and TGRD registers for MTU0, MTU3, MTU4, MTU6, MTU7, and MTU9 can also be designated for operation as buffer registers. TGR buffer register combinations are TGRA and TGRC, and TGRB and TGRD.

MTU0.TGRE and MTU0.TGRF, and MTU9.TGRE and MTU9.TGRF function as compare registers. When the MTU0.TCNT count matches the MTU0.TGRE value or the MTU9.TCNT count matches the MTU9.TGRE value, an A/D converter start request can be issued. The TGRF register can also be designated for operation as a buffer register. TGR buffer register combination is TGRE and TGRF. MTU5.TGRU, MTU5.TGRV, and MTU5.TGRW function as compare match, input capture, or external pulse width measurement registers.

The MTU1.TGRA, MTU2.TGRA, MTU1.TGRB, and MTU2.TGRB registers are read as 0000h when TMDR3.LWA is 1. Refer to section 20.2.5, Timer Mode Register 3 (TMDR3) for details.

20.2.16 Timer Longword General Registers (TGRALW, TGRBLW)

Address(es): MTU1.TGRALW 000C 13A4h, MTU1.TGRBLW 000C 13A8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: TGRALW and TGRBLW must not be accessed in 8 or 16 bits; it should be accessed in 32 bits.

The TGRnLW register (n = A, B) is a 32-bit readable/writable register. Two general registers of this type are provided, and are formed by combining MTU1.TGRn and MTU2.TGRn. Such operation is only effective when TMDR3.LWA is 1. The TGRnLW register is initialized to FFFF FFFFh by a reset, but it is read as 0000 0000h when TMDR3.LWA is 0. Refer to section 20.2.5, Timer Mode Register 3 (TMDR3) for details.

The TGRnLW register functions as an output compare or input capture register when TMDR3.LWA is 1.

This register can only be used in 32-bit phase counting mode.

20.2.17 Timer Start Registers (TSTRA, TSTRB, TSTR)

- MTU.TSTRA (for MTU0, MTU1, MTU2, MTU3, MTU4, and MTU9

Address(es): MTU.TSTRA 000C 1280h

	b7	b6	b5	b4	b3	b2	b1	b0
	CST4	CST3	—	CST9	—	CST2	CST1	CST0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CST0	Counter Start 0	0: MTU0.TCNT counting is stopped 1: MTU0.TCNT performs count operation	R/W
b1	CST1	Counter Start 1	0: MTU1.TCNT counting is stopped 1: MTU1.TCNT performs count operation	R/W
b2	CST2	Counter Start 2	0: MTU2.TCNT counting is stopped 1: MTU2.TCNT performs count operation	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	CST9	Counter start 9	0: MTU9.TCNT counting is stopped 1: MTU9.TCNT performs count operation	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	CST3	Counter Start 3	0: MTU3.TCNT counting is stopped 1: MTU3.TCNT performs count operation	R/W
b7	CST4	Counter Start 4	0: MTU4.TCNT counting is stopped 1: MTU4.TCNT performs count operation	R/W

Note: When 1 is written to a bit in TCSYSTR, the corresponding bit in TSTRA is also set to 1 automatically.

The TSTRA register starts or stops TCNT operation in MTU0 to MTU4 and MTU9.
TSTRB starts or stops TCNT operation in MTU6 and MTU7.
TSTR starts or stops TCNT operation in MTU5.
Before setting the operating mode in TMDR1 or setting the TCNT count clock in TCR, be sure to stop the TCNT counter.

CSTn Bits (Counter Start n) (n = 0, 1, 2, 3, 4, 9)

Each bit starts or stops TCNT in the corresponding channel.
If 0 is written to the CSTn bit during operation with the MTIOC pin designated for output, the counter stops. At this time, initial output level specified in the TOCR1A or TOCR2A register is output from the MTIOC pin in complementary PWM mode or reset-synchronized PWM mode. In any mode other than complementary PWM mode and reset synchronous PWM mode, the output compare signal level from the MTIOC pin is retained. If TIOR is written to while the CSTn bit is 0, the pin output level will be changed to the specified initial output value.

- MTU.TSTRB (for MTU6 and MTU7)

Address(es): MTU.TSTRB 000C 1A80h

	b7	b6	b5	b4	b3	b2	b1	b0
	CST7	CST6	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	CST6	Counter Start 6	0: MTU6.TCNT counting is stopped 1: MTU6.TCNT performs count operation	R/W
b7	CST7	Counter Start 7	0: MTU7.TCNT counting is stopped 1: MTU7.TCNT performs count operation	R/W

Note: When 1 is written to a bit in TCSYSTR, the corresponding bit in TSTRB is also set to 1 automatically.

CSTn Bits (Counter Start n) (n = 6, 7)

Each bit starts or stops TCNT in the corresponding channel.
If 0 is written to the CSTn bit during operation with the MTIOC pin designated for output, the counter stops. At this time the MTIOC pin output the initial output level set in the TOCR1B or TOCR2B register in complementary PWM mode or reset-synchronized PWM mode, but the output compare signal level from the MTIOC pin is retained in the other modes.
If TIOR is written to while the CSTn bit is 0, the pin output level will be changed to the specified initial output value.

- MTU5.TSTR

Address(es): MTU5.TSTR 000C 1CB4h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	CSTU5	CSTV5	CSTW5
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CSTW5	Counter Start W5	0: MTU5.TCNTW counting is stopped 1: MTU5.TCNTW performs count operation	R/W
b1	CSTV5	Counter Start V5	0: MTU5.TCNTV counting is stopped 1: MTU5.TCNTV performs count operation	R/W
b2	CSTU5	Counter Start U5	0: MTU5.TCNTU counting is stopped 1: MTU5.TCNTU performs count operation	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

20.2.18 Timer Synchronous Registers (TSYRA, TSYRB)

- MTU.TSYRA (for MTU0 to MTU4 and MTU9)

Address(es): MTU.TSYRA 000C 1281h

	b7	b6	b5	b4	b3	b2	b1	b0
	SYNC4	SYNC3	—	—	SYNC9	SYNC2	SYNC1	SYNC0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SYNC0	Timer Synchronous Operation 0	0: MTU0.TCNT operates independently (TCNT setting/clearing is not related to other channels). 1: MTU0.TCNT performs synchronous operation. (TCNT synchronous setting/synchronous clearing is enabled.)	R/W
b1	SYNC1	Timer Synchronous Operation 1	0: MTU1.TCNT operates independently (TCNT setting/clearing is not related to other channels). 1: MTU1.TCNT performs synchronous operation. (TCNT synchronous setting/synchronous clearing is enabled.)	R/W
b2	SYNC2	Timer Synchronous Operation 2	0: MTU2.TCNT operates independently (TCNT setting/clearing is not related to other channels). 1: MTU2.TCNT performs synchronous operation. (TCNT synchronous setting/synchronous clearing is enabled.)	R/W
b3	SYNC9	Timer Synchronous Operation 9	0: MTU9.TCNT operates independently (TCNT setting/clearing is not related to other channels). 1: MTU9.TCNT performs synchronous operation. (TCNT synchronous setting/synchronous clearing is enabled.)	R/W
b5, b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	SYNC3	Timer Synchronous Operation 3	0: MTU3.TCNT operates independently (TCNT setting/clearing is not related to other channels). 1: MTU3.TCNT performs synchronous operation. (TCNT synchronous setting/synchronous clearing is enabled.)	R/W
b7	SYNC4	Timer Synchronous Operation 4	0: MTU4.TCNT operates independently (TCNT setting/clearing is not related to other channels). 1: MTU4.TCNT performs synchronous operation. (TCNT synchronous setting/synchronous clearing is enabled.)	R/W

TSYRA selects independent operation or synchronous operation of TCNT in MTU0 to MTU4 and MTU9.
TSYRB selects independent operation or synchronous operation of TCNT in MTU6 and MTU7.
A channel performs synchronous operation when the corresponding bit in TSYR is set to 1.

SYNCn Bits (Timer Synchronous Operation n) (n = 0, 1, 2, 3, 4, 9)

Each bit selects whether operation is independent of or synchronized with other channels.
When synchronous operation is selected, the TCNT synchronous setting of multiple channels and synchronous clearing by counter clearing on another channel are possible.
To set synchronous operation, the SYNC bits for at least two channels must be set to 1. To set synchronous clearing, in addition to the SYNC bit, the TCNT clearing source must also be set by means of the TCR.CCLR[2:0] bits.

- MTU.TSYRB (for MTU6 and MTU7)

Address(es): MTU.TSYRB 000C 1A81h

	b7	b6	b5	b4	b3	b2	b1	b0
	SYNC7	SYNC6	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	SYNC6	Timer Synchronous Operation 6	0: MTU6.TCNT operates independently (TCNT setting/clearing is not related to other channels). 1: MTU6.TCNT performs synchronous operation. (TCNT synchronous setting/synchronous clearing is enabled.)	R/W
b7	SYNC7	Timer Synchronous Operation 7	0: MTU7.TCNT operates independently (TCNT setting/clearing is not related to other channels). 1: MTU7.TCNT performs synchronous operation. (TCNT synchronous setting/synchronous clearing is enabled.)	R/W

SYNCn Bits (Timer Synchronous Operation n) (n = 6, 7)

Each bit selects whether operation is independent of or synchronized with other channels.

When synchronous operation is selected, the TCNT synchronous setting of multiple channels and synchronous clearing by counter clearing on another channel are possible.

To set synchronous operation, the SYNC bits for at least two channels must be set to 1. To set synchronous clearing, in addition to the SYNC bit, the TCNT clearing source must also be set by means of bits TCR.CCLR[2:0].

20.2.19 Timer Counter Synchronous Start Register (TCSYSTR)

Address(es): MTU.TCSYSTR 000C 1282h

	b7	b6	b5	b4	b3	b2	b1	b0
	SCH0	SCH1	SCH2	SCH3	SCH4	SCH9	SCH6	SCH7
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SCH7	Synchronous Start 7	0: Does not specify synchronous start for MTU7.TCNT 1: Specifies synchronous start for MTU7.TCNT	R/(W)*1
b1	SCH6	Synchronous Start 6	0: Does not specify synchronous start for MTU6.TCNT 1: Specifies synchronous start for MTU6.TCNT	R/(W)*1
b2	SCH9	Synchronous Start 9	0: Does not specify synchronous start for MTU9.TCNT 1: Specifies synchronous start for MTU9.TCNT	R/(W)*1
b3	SCH4	Synchronous Start 4	0: Does not specify synchronous start for MTU4.TCNT 1: Specifies synchronous start for MTU4.TCNT	R/(W)*1
b4	SCH3	Synchronous Start 3	0: Does not specify synchronous start for MTU3.TCNT 1: Specifies synchronous start for MTU3.TCNT	R/(W)*1
b5	SCH2	Synchronous Start 2	0: Does not specify synchronous start for MTU2.TCNT 1: Specifies synchronous start for MTU2.TCNT	R/(W)*1
b6	SCH1	Synchronous Start 1	0: Does not specify synchronous start for MTU1.TCNT 1: Specifies synchronous start for MTU1.TCNT	R/(W)*1
b7	SCH0	Synchronous Start 0	0: Does not specify synchronous start for MTU0.TCNT 1: Specifies synchronous start for MTU0.TCNT	R/(W)*1

Note 1. Only 1 can be written to this bit, and doing so sets the flag.
TCSYSTR is automatically cleared after 1 is written to.

TCSYSTR specifies synchronous start of the counters.

SCH7 Bit (Synchronous Start 7)

This bit controls synchronous start of MTU7.TCNT.
[Clearing condition]

- When 1 is set to the TSTRA.CST7 bit while SCH7 = 1

SCH6 Bit (Synchronous Start 6)

This bit controls synchronous start of MTU6.TCNT.
[Clearing condition]

- When 1 is set to the TSTRA.CST6 bit while SCH6 = 1

SCH9 Bit (Synchronous Start 9)

This bit controls synchronous start of MTU9.TCNT.
[Clearing condition]

- When 1 is set to the TSTRA.CST9 bit while SCH9 = 1

SCH4 Bit (Synchronous Start 4)

This bit controls synchronous start of MTU4.TCNT.
[Clearing condition]

- When 1 is set to the TSTRA.CST4 bit while SCH4 = 1

SCH3 Bit (Synchronous Start 3)

This bit controls synchronous start of MTU3.TCNT.
[Clearing condition]

- When 1 is set to the TSTRA.CST3 bit while SCH3 = 1

SCH2 Bit (Synchronous Start 2)

This bit controls synchronous start of MTU2.TCNT.
[Clearing condition]

- When 1 is set to the TSTRA.CST2 bit while SCH2 = 1

SCH1 Bit (Synchronous Start 1)

This bit controls synchronous start of MTU1.TCNT.
[Clearing condition]

- When 1 is set to the TSTRA.CST1 bit while SCH1 = 1

SCH0 Bit (Synchronous Start 0)

This bit controls synchronous start of MTU0.TCNT.
[Clearing condition]

- When 1 is set to the TSTRA.CST0 bit while SCH0 = 1

20.2.20 Timer Read/Write Enable Registers (TRWERA, TRWERB)

Address(es): MTU.TRWERA 000C 1284h, MTU.TRWERB 000C 1A84h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	RWE
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	RWE	Read/Write Enable	0: Read/write access to the registers is disabled 1: Read/write access to the registers is enabled	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TRWERA enables or disables access to the registers and counters that have write-protection capability against accidental modification in MTU3 and MTU4.
TRWERB enables or disables access to the registers and counters that have write-protection capability against accidental modification in MTU6 and MTU7.

RWE Bit (Read/Write Enable)

This bit enables or disables access to the registers that have write-protection capability against accidental modification.
[Clearing condition]

- When 0 is written to the RWE bit after reading RWE = 1

- Registers and Counters having Write-Protection Capability against Accidental Modification (TRWERA)

24 registers: MTUn.TCR, MTUn.TCR2, MTUn.TMDR1, MTUn.TIORH, MTUn.TIORL, MTUn.TIER, MTUn.TGRA, MTUn.TGRB, MTU.TOERA, MTU.TOCR1A, MTU.TOCR2A, MTU.TGCRA, MTU.TCDRA, MTU.TDDRA, and MTUn.TCNT (n = 3, 4)

- Registers and Counters having Write-Protection Capability against Accidental Modification (TRWERB)

24 registers: MTUn.TCR, MTUn.TCR2, MTUn.TMDR1, MTUn.TIORH, MTUn.TIORL, MTUn.TIER, MTUn.TGRA, MTUn.TGRB, MTU.TOERB, MTU.TOCR1B, MTU.TOCR2B, MTU.TGCRB, MTU.TCDRB, MTU.TDDRB, and MTUn.TCNT (n = 6, 7)

20.2.21 Timer Output Master Enable Registers (TOERA, TOERB)

- MTU.TOERA

Address(es): MTU.TOERA 000C 120Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	OE4D	OE4C	OE3D	OE4B	OE4A	OE3B
Value after reset:	1	1	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	OE3B	Master Enable MTIOC3B	0: MTU output is disabled*1 1: MTU output is enabled	R/W
b1	OE4A	Master Enable MTIOC4A	0: MTU output is disabled*1 1: MTU output is enabled	R/W
b2	OE4B	Master Enable MTIOC4B	0: MTU output is disabled*1 1: MTU output is enabled	R/W
b3	OE3D	Master Enable MTIOC3D	0: MTU output is disabled*1 1: MTU output is enabled	R/W
b4	OE4C	Master Enable MTIOC4C	0: MTU output is disabled*1 1: MTU output is enabled	R/W
b5	OE4D	Master Enable MTIOC4D	0: MTU output is disabled*1 1: MTU output is enabled	R/W
b7, b6	—	Reserved	These bits are read as 1. The write value should be 1.	R/W

Note 1. To output the inactive level from each pin when the MTU output is set to disabled, first set the data direction register (PDR) and port output data register (PODR) of I/O ports to output the inactive level from general I/O ports, and then set the port mode register (PMR) to use general I/O ports. For details, refer to section 18, I/O Ports.

TOERA enables or disables output settings for output pins MTIOC4D, MTIOC4C, MTIOC3D, MTIOC4B, MTIOC4A, and MTIOC3B.

These pins do not output correctly if the bits in the TOERA register have not been set. In MTU3 and MTU4, set TOERA prior to setting TIOR.

Set MTU.TOERA after clearing the CST3 and CST4 bits in MTU.TSTRA to 0 (refer to Figure 20.43 and Figure 20.47).

- MTU.TOERB

Address(es): MTU.TOERB 000C 1A0Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	OE7D	OE7C	OE6D	OE7B	OE7A	OE6B
Value after reset:	1	1	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	OE6B	Master Enable MTIOC6B	0: MTU output is disabled*1 1: MTU output is enabled	R/W
b1	OE7A	Master Enable MTIOC7A	0: MTU output is disabled*1 1: MTU output is enabled	R/W
b2	OE7B	Master Enable MTIOC7B	0: MTU output is disabled*1 1: MTU output is enabled	R/W
b3	OE6D	Master Enable MTIOC6D	0: MTU output is disabled*1 1: MTU output is enabled	R/W
b4	OE7C	Master Enable MTIOC7C	0: MTU output is disabled*1 1: MTU output is enabled	R/W
b5	OE7D	Master Enable MTIOC7D	0: MTU output is disabled*1 1: MTU output is enabled	R/W
b7, b6	—	Reserved	These bits are read as 1. The write value should be 1.	R/W

Note 1. To output the inactive level from each pin when the MTU output is set to disabled, first set the data direction register (PDR) and port output data register (PODR) of I/O ports to output the inactive level from general I/O ports, and then set the port mode register (PMR) to use general I/O ports. For details, refer to section 18, I/O Ports.

TOERB enables or disables output settings for output pins MTIOC7D, MTIOC7C, MTIOC6D, MTIOC7B, MTIOC7A, and MTIOC6B.

These pins do not output correctly if the bits in the TOERB register have not been set. In MTU6, and MTU7, set TOERB prior to setting TIOR.

Set MTU.TOERB after clearing the CST6 and CST7 bits in MTU.TSTRB to 0 (refer to Figure 20.43 and Figure 20.47).

20.2.22 Timer Output Control Registers 1 (TOCR1A, TOCR1B)

Address(es): MTU.TOCR1A 000C 120Eh, MTU.TOCR1B 000C 1A0Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	PSYE	—	—	TOCL	TOCS	OLSN	OLSP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	OLSP	Output Level Select P*1, *3	Refer to Table 20.42.	R/W
b1	OLSN	Output Level Select N*1, *3	Refer to Table 20.43.	R/W
b2	TOCS	TOC Select	0: TOCR1j setting is selected (j = A, B) 1: TOCR2j setting is selected	R/W
b3	TOCL	TOC Register Write Protection *2, *4	0: Write access to the TOCS, OLSN, and OLSP bits is enabled 1: Write access to the TOCS, OLSN, and OLSP bits is disabled	R/W
b5, b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	PSYE	PWM Synchronous Output Enable	0: Toggle output is disabled 1: Toggle output is enabled	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note 1. Clearing the TOCR1j.TOCS bit to 0 makes this bit setting valid.
Note 2. Setting the TOCR1j.TOCL bit to 1 prevents accidental modification when the CPU goes out of control.
Note 3. If dead-time is not generated, the negative-phase output is the exact inverse of the positive-phase output. In this case, only the OLSP bit is valid.
Note 4. This bit can be set to 1 only once after a reset. After 1 is written, 0 cannot be written to the bit.

TOCR1A and TOCR1B enable or disable PWM-synchronized toggle output in complementary PWM mode and reset-synchronized PWM mode, and control inversion of PWM output level.

OLSP Bit (Output Level Select P)

This bit selects the positive-phase output level in reset-synchronized PWM mode and complementary PWM mode. The initial output is selected while the counter is stopped.

OLSN Bit (Output Level Select N)

This bit selects the negative-phase output level in reset-synchronized PWM mode and complementary PWM mode. The initial output is selected while the counter is stopped.

TOCS Bit (TOC Select)

This bit selects either the TOCR1j or TOCR2j (j = A, B) setting to be used for the output level in complementary PWM mode and reset-synchronized PWM mode.

TOCL Bit (TOC Register Write Protection)

This bit enables or disables write access to the TOCS, OLSN, and OLSP bits in TOCR1j (j = A, B).

PSYE Bit (PWM Synchronous Output Enable)

This bit enables or disables toggle output synchronized with the PWM period.

Table 20.42 Output Level Select Function

Bit 0			Function	
			Compare Match Output	
OLSP	Initial Output	Active Level	Up-Counting	Down-Counting
0	High level	Low level	Low level	High level
1	Low level	High level	High level	Low level

Table 20.43 Output Level Select Function

Bit 1			Function	
			Compare Match Output	
OLSN	Initial Output	Active Level	Up-Counting	Down-Counting
0	High level	Low level	High level	Low level
1	Low level	High level	Low level	High level

Note: The initial output value of negative-phase waveform changes to an active level after the dead time has passed since counting starts.

Figure 20.3 shows an example of output in complementary PWM mode (one phase) when OLSN = 1 and OLSP = 1.

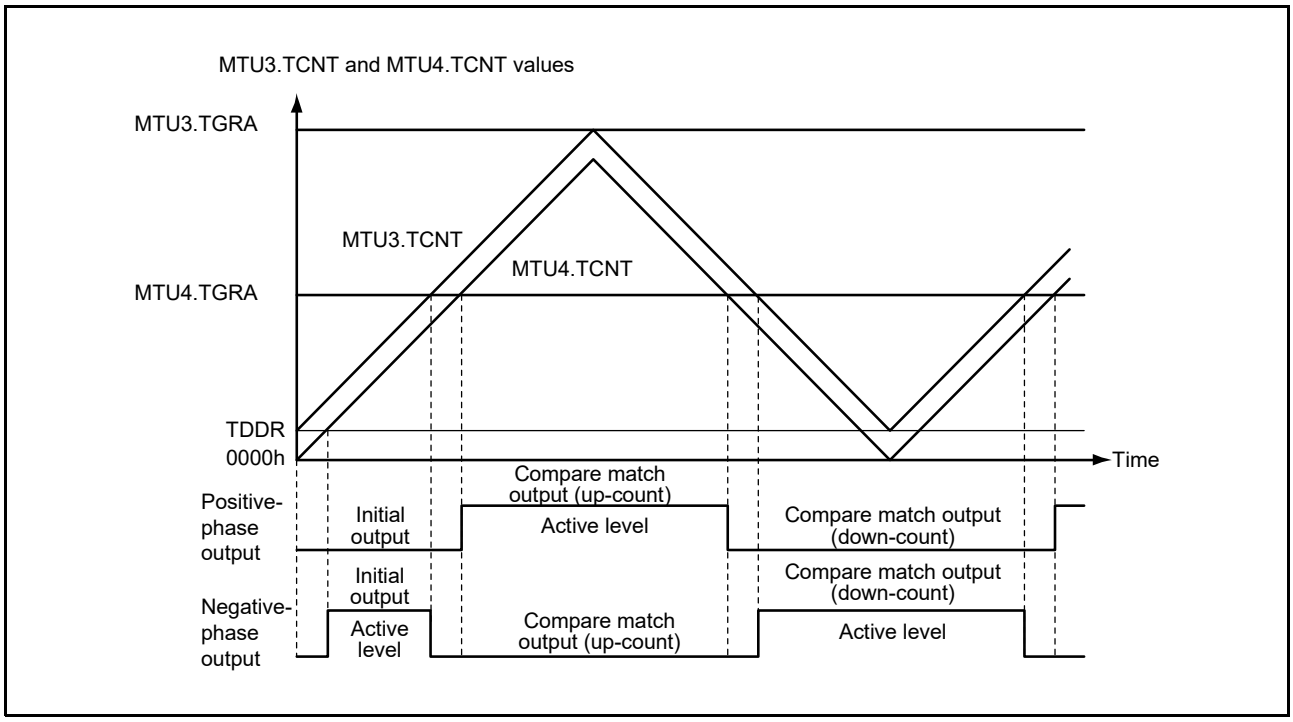


Figure 20.3 Example of Output in Complementary PWM Mode

20.2.23 Timer Output Control Registers 2 (TOCR2A, TOCR2B)

Address(es): MTU.TOCR2A 000C 120Fh, MTU.TOCR2B 000C 1A0Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	BF[1:0]		OLS3N	OLS3P	OLS2N	OLS2P	OLS1N	OLS1P
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	OLS1P	Output Level Select 1P*1, *2	This bit selects the output level on MTIOC3B or MTIOC6B in reset-synchronized PWM mode and complementary PWM mode. Refer to Table 20.44.	R/W
b1	OLS1N	Output Level Select 1N*1, *2	This bit selects the output level on MTIOC3D or MTIOC6D in reset-synchronized PWM mode and complementary PWM mode. Refer to Table 20.45.	R/W
b2	OLS2P	Output Level Select 2P*1, *2	This bit selects the output level on MTIOC4A or MTIOC7A in reset-synchronized PWM mode and complementary PWM mode. Refer to Table 20.46.	R/W
b3	OLS2N	Output Level Select 2N*1, *2	This bit selects the output level on MTIOC4C or MTIOC7C in reset-synchronized PWM mode and complementary PWM mode. Refer to Table 20.47.	R/W
b4	OLS3P	Output Level Select 3P*1, *2	This bit selects the output level on MTIOC4B or MTIOC7B in reset-synchronized PWM mode and complementary PWM mode. Refer to Table 20.48.	R/W
b5	OLS3N	Output Level Select 3N*1, *2	This bit selects the output level on MTIOC4D or MTIOC7D in reset-synchronized PWM mode and complementary PWM mode. Refer to Table 20.49.	R/W
b7, b6	BF[1:0]	TOLBR Buffer Transfer Timing Select	These bits select the timing for transferring data from TOLBRj to TOCR2j. Refer to Table 20.50 for details.	R/W

j = A, B

Note 1. Setting the TOCR1j.TOCS bit to 1 makes this bit setting valid.

Note 2. If dead-time is not generated, the negative-phase output is the exact inverse of the positive-phase output. In this case, only the OLSiP bits are valid (i = 1 to 3).

TOCR2A and TOCR2B control inversion of PWM output level in complementary PWM mode and reset-synchronized PWM mode.

The initial output is selected while the counter is stopped.

Table 20.44 MTIOCmB Output Level Select Function

Bit 0	Function			
			Compare Match Output	
OLS1P	Initial Output	Active Level	Up-Counting	Down-Counting
0	High level	Low level	Low level	High level
1	Low level	High level	High level	Low level

m = 3, 6

Table 20.45 MTIOCmD Output Level Select Function

Bit 1	Function			
			Compare Match Output	
OLS1N	Initial Output	Active Level	Up-Counting	Down-Counting
0	High level	Low level	High level	Low level
1	Low level	High level	Low level	High level

m = 3, 6

Note: The initial output value of negative-phase waveform changes to an active level after the dead time has passed since counting starts.

Table 20.46 MTIOCmA Output Level Select Function

Bit 2	Function			
			Compare Match Output	
OLS2P	Initial Output	Active Level	Up-Counting	Down-Counting
0	High level	Low level	Low level	High level
1	Low level	High level	High level	Low level

m = 4, 7

Table 20.47 MTIOCmC Output Level Select Function

Bit 3	Function			
			Compare Match Output	
OLS2N	Initial Output	Active Level	Up-Counting	Down-Counting
0	High level	Low level	High level	Low level
1	Low level	High level	Low level	High level

m = 4, 7

Note: The initial output value of negative-phase waveform changes to an active level after the dead time has passed since counting starts.

Table 20.48 MTIOCmB Output Level Select Function

Bit 4	Function			
			Compare Match Output	
OLS3P	Initial Output	Active Level	Up-Counting	Down-Counting
0	High level	Low level	Low level	High level
1	Low level	High level	High level	Low level

m = 4, 7

Table 20.49 MTIOCmD Output Level Select Function

Bit 5	Function			
			Compare Match Output	
OLS3N	Initial Output	Active Level	Up-Counting	Down-Counting
0	High level	Low level	High level	Low level
1	Low level	High level	Low level	High level

m = 4, 7

Note: The initial output value of negative-phase waveform changes to an active level after the dead time has passed since counting starts.

Table 20.50 Setting of TOCR2j.BF[1:0] Bits

Bit 7	Bit 6	Description	
BF[1]	**BF[0]**	**Complementary PWM Mode**	**Reset-Synchronized PWM Mode**
0	0	Does not transfer data from the buffer register (TOLBRj) to TOCR2j.	Does not transfer data from the buffer register (TOLBRj) to TOCR2j.
0	1	Transfers data from the buffer register (TOLBRj) to TOCR2j at the crest of the MTUn.TCNT count.	Transfers data from the buffer register (TOLBRj) to TOCR2j when MTUm.TCNT or MTUn.TCNT is cleared.
1	0	Transfers data from the buffer register (TOLBRj) to TOCR2j at the trough of the MTUn.TCNT count.	Setting prohibited
1	1	Transfers data from the buffer register (TOLBRj) to TOCR2j at the crest and trough of the MTUn.TCNT count.	Setting prohibited

n = 4, 7; m = 3, 6; j = A, B

20.2.24 Timer Output Level Buffer Registers (TOLBRA, TOLBRB)

Address(es): MTU.TOLBRA 000C 1236h, MTU.TOLBRB 000C 1A36h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	OLS3N	OLS3P	OLS2N	OLS2P	OLS1N	OLS1P
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	OLS1P	Output Level Select 1P	Specify the buffer value to be transferred to the OLS1P bit in TOCR2j.	R/W
b1	OLS1N	Output Level Select 1N	Specify the buffer value to be transferred to the OLS1N bit in TOCR2j.	R/W
b2	OLS2P	Output Level Select 2P	Specify the buffer value to be transferred to the OLS2P bit in TOCR2j.	R/W
b3	OLS2N	Output Level Select 2N	Specify the buffer value to be transferred to the OLS2N bit in TOCR2j.	R/W
b4	OLS3P	Output Level Select 3P	Specify the buffer value to be transferred to the OLS3P bit in TOCR2j.	R/W
b5	OLS3N	Output Level Select 3N	Specify the buffer value to be transferred to the OLS3N bit in TOCR2j.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

j = A, B

TOLBRA and TOLBRB are buffer registers for TOCR2A and TOCR2B and specify the PWM output level in complementary PWM mode and reset-synchronized PWM mode.

Figure 20.4 shows an example of the PWM output level setting procedure in buffer operation.

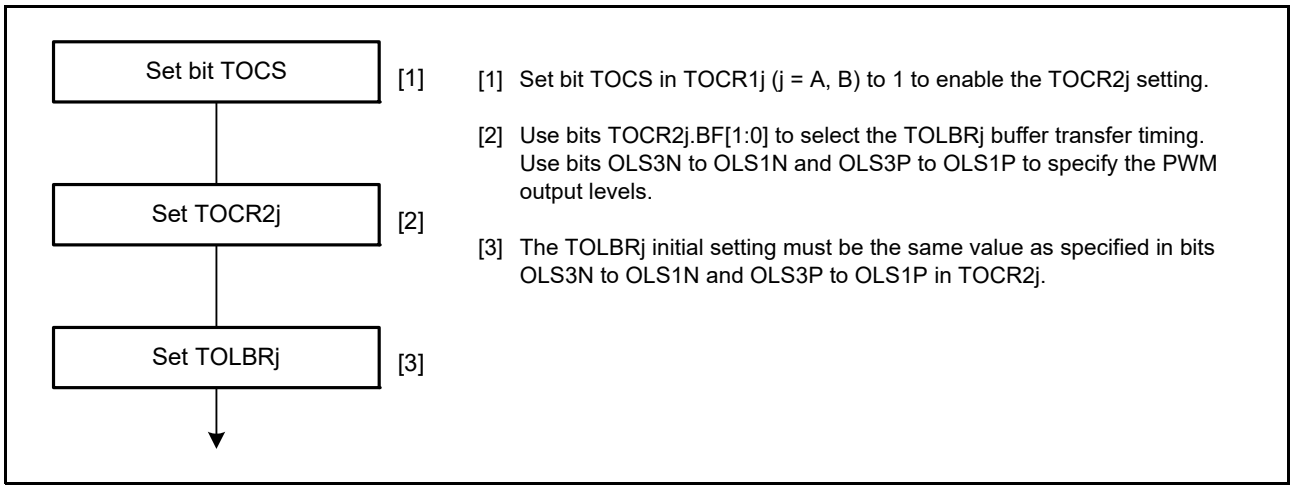


Figure 20.4 Example of PWM Output Level Setting Procedure in Buffer Operation

20.2.25 Timer Gate Control Registers (TGCRA, TGCRB)

Address(es): MTU.TGCRA 000C 120Dh, MTU.TGCRB 000C 1A0Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	BDC	N	P	FB	WF	VF	UF
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	UF	Output Phase Switch	These bits turn on or off the positive-phase/negative-phase output. The setting of these bits is valid only when the FB bit is set to 1. In this case, the setting of b0 to b2 is used instead of the external input. Refer to Table 20.51.	R/W
b1	VF			R/W
b2	WF			R/W
b3	FB	External Feedback Signal Enable	0: Output is switched by external input (input sources are TGRA, TGRB, and TGRC input capture signals in MTU0 and MTU9) 1: Output is switched by software (TGCRA and TGCRB's UF, VF, and WF settings)	R/W
b4	P	Positive-Phase Output (P) Control	0: Level output 1: Reset-synchronized PWM or complementary PWM output	R/W
b5	N	Negative-Phase Output (N) Control	0: Level output 1: Reset-synchronized PWM or complementary PWM output	R/W
b6	BDC	Brushless DC Motor	0: Ordinary output 1: Functions of this register are made effective	R/W
b7	—	Reserved	This bit is read as 1. The write value should be 1.	R/W

TGCRA and TGCRB control the output waveform necessary for brushless DC motor control in reset-synchronized PWM mode and complementary PWM mode. TGCRA and TGCRB register settings are ineffective for anything other than complementary PWM mode and reset-synchronized PWM mode.

UF, VF, and WF Bits (Output Phase Switch)

The setting of these bits is valid only when the FB bit is set to 1. In this case, the setting of b0 to b2 is used instead of the external input. Refer to Table 20.51 for details.

FB Bit (External Feedback Signal Enable)

This bit selects whether the positive-/negative-phase output is switched automatically with the TGRA, TGRB, and TGRC input capture signals in MTU0 and MTU9 or by writing 0 or 1 to bits 2 to 0 in TGCRA and TGCRB.
When the TGCRA.FB bit is 0, output of MTU3 and MTU4 can be switched with the TGRA, TGRB, and TGRC input capture signals in MTU0.
When the TGCRB.FB bit is 0, output of MTU6 and MTU7 can be switched with the TGRA, TGRB, and TGRC input capture signals in MTU9.

P Bit (Positive-Phase Output (P) Control)

This bit selects the level output or the reset-synchronized PWM/complementary PWM output for the positive-phase output pins (MTIOC3B, MTIOC4A, MTIOC4B, MTIOC6B, MTIOC7A, and MTIOC7B pins).

N Bit (Negative-Phase Output (N) Control)

This bit selects the level output or the reset-synchronized PWM/complementary PWM output for the negative-phase output pins (MTIOC3D, MTIOC4C, MTIOC4D, MTIOC6D, MTIOC7C, and MTIOC7D pins).

BDC Bit (Brushless DC Motor)

This bit selects whether to make the functions of TGCRA and TGCRB effective or ineffective.

Table 20.51 Output Level Select Function

Bit 2	Bit 1	Bit 0	Function					
			MTIOC3B, MTIOC6B	MTIOC4A, MTIOC7A	MTIOC4B, MTIOC7B	MTIOC3D, MTIOC6D	MTIOC4C, MTIOC7C	MTIOC4D, MTIOC7D
WF	VF	UF	U Phase	V Phase	W Phase	U Phase	V Phase	W Phase
0	0	0	OFF	OFF	OFF	OFF	OFF	OFF
0	0	1	ON	OFF	OFF	OFF	OFF	ON
0	1	0	OFF	ON	OFF	ON	OFF	OFF
0	1	1	OFF	ON	OFF	OFF	OFF	ON
1	0	0	OFF	OFF	ON	OFF	ON	OFF
1	0	1	ON	OFF	OFF	OFF	ON	OFF
1	1	0	OFF	OFF	ON	ON	OFF	OFF
1	1	1	OFF	OFF	OFF	OFF	OFF	OFF

20.2.26 Timer Subcounters (TCNTSA, TCNTSB)

Address(es): MTU.TCNTSA 000C 1220h, MTU.TCNTSB 000C 1A20h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note: TCNTSA and TCNTSB must not be accessed in 8 bits; it should be accessed in 16 bits.

TCNTSA and TCNTSB are 16-bit read-only counters used only in complementary PWM mode.
The initial value of TCNTSA and TCNTSB after a reset is 0000h.

20.2.27 Timer Period Data Registers (TCDRA, TCDRB)

Address(es): MTU.TCDRA 000C 1214h, MTU.TCDRB 000C 1A14h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: TCDRA and TCDRB must not be accessed in 8 bits; it should be accessed in 16 bits.

TCDRA and TCDRB are 16-bit readable/writable registers used only in complementary PWM mode. Set half the PWM carrier period as the TCDRA and TCDRB values. The TCDRA and TCDRB registers are constantly compared with the TCNTSA and TCNTSB counters in complementary PWM mode, respectively. When a match occurs, the TCNTSA and TCNTSB counters switch the count direction (down-count to up-count). The initial value of TCDRA and TCDRB after a reset is FFFFh.

20.2.28 Timer Period Buffer Registers (TCBRA, TCBRB)

Address(es): MTU.TCBRA 000C 1222h, MTU.TCBRB 000C 1A22h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: TCBRA and TCBRB must not be accessed in 8 bits; it should be accessed in 16 bits.

TCBRA and TCBRB are 16-bit readable/writable registers, used only in complementary PWM mode, that function as buffer registers for TCDRA and TCDRB. The TCBRA and TCBRB values are transferred to TCDRA and TCDRB with the transfer timing set in TMDR1. The initial value of TCBRA and TCBRB after a reset is FFFFh.

20.2.29 Timer Dead Time Data Registers (TDDRA, TDDRB)

Address(es): MTU.TDDRA 000C 1216h, MTU.TDDRB 000C 1A16h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: TDDRA and TDDRB must not be accessed in 8 bits; it should be accessed in 16 bits.

TDDRA and TDDRB are 16-bit readable/writable registers, used only in complementary PWM mode, that specify the MTU3.TCNT (MTU6.TCNT) and MTU4.TCNT (MTU7.TCNT) counter offset value. In complementary PWM mode, when the MTU3.TCNT (MTU6.TCNT) and MTU4.TCNT (MTU7.TCNT) counters are cleared and then restarted, the TDDRA (TDDRB) value is loaded into the MTU3.TCNT (MTU6.TCNT) counter and the count operation starts. The initial value of TDDRA and TDDRB after a reset is FFFFh.

20.2.30 Timer Dead Time Enable Registers (TDERA, TDERB)

Address(es): MTU.TDERA 000C 1234h, MTU.TDERB 000C 1A34h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	TDER
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	TDER	Dead Time Enable	0: No dead time is generated 1: Dead time is generated*1	R/(W)
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. TDDRA and TDDRB must be set to 1 or a larger value.

TDERA and TDERB control dead time generation in complementary PWM mode. The MTU has one TDER each for MTU3 and MTU6. TDERA and TDERB should be modified only while TCNT stops.

TDER Bit (Dead Time Enable)

This bit specifies whether to generate dead time.

[Clearing condition]

- When 0 is written to TDER after reading TDER = 1

20.2.31 Timer Buffer Transfer Set Registers (TBTERA, TBTERB)

Address(es): MTU.TBTERA 000C 1232h, MTU.TBTERB 000C 1A32h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	BTE[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	BTE[1:0]	Buffer Transfer Disable and Interrupt Skipping Link Setting	These bits enable or disable transfer from the buffer registers*1 used in complementary PWM mode to the temporary registers, and specify whether to link the transfer with interrupt skipping function 1. For details, refer to Table 20.52.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Applicable buffer registers (TBTERA):
MTU3.TGRC, MTU3.TGRD, MTU4.TGRC, MTU4.TGRD, and TCBRA
Applicable buffer registers (TBTERB):
MTU6.TGRC, MTU6.TGRD, MTU7.TGRC, MTU7.TGRD, and TCBRB

TBTERA and TBTERB enable or disable transfer from the buffer registers used in complementary PWM mode to the temporary registers, and specify whether to link the transfer with interrupt skipping 1 operation.

Table 20.52 Setting of TBTERA.BTE[1:0] Bits and TBTERB.BTE[1:0] Bits

Bit 1	Bit 0	
BTE[1]	BTE[0]	Description
0	0	Enables transfer from the buffer registers to the temporary registers*1 and does not link the transfer with interrupt skipping function 1.
0	1	Disables transfer from the buffer registers to the temporary registers.
1	0	Links transfer from the buffer registers to the temporary registers with interrupt skipping function 1.*2
1	1	Setting prohibited

Note 1. Data is transferred according to the MD3 to MD0 bit setting in TMDR1. For details, refer to section 20.3.8, Complementary PWM Mode.

Note 2. When interrupt skipping is disabled the T3AEN and T4VEN (T6AEN and T7VEN) bits are cleared to 0 in the timer interrupt skipping set register (TITCR1A (TITCR1B)) or the skipping count set bits (T3ACOR and T4VCOR (T6ACOR and T7VCOR)) in TITCR1A (TITCR1B) are cleared to 0), be sure to disable link of buffer transfer with interrupt skipping (clear the BTE1 bit in the timer buffer transfer set register (TBTERA (TBTERB)) to 0). If link with interrupt skipping is enabled while interrupt skipping is disabled, buffer transfer will not be performed.

20.2.32 Timer Waveform Control Registers (TWCRA, TWCRB)

Address(es): MTU.TWCRA 000C 1260h, MTU.TWCRB 000C 1A60h

	b7	b6	b5	b4	b3	b2	b1	b0
	CCE	—	—	—	—	—	SCC	WRE
Value after reset:	0*2	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	WRE	Waveform Retain Enable	0: Initial values specified in TOCR1A and TOCR2A (TOCR1B and TOCR2B) are output 1: Initial output is inhibited	R/(W)*3
b1	SCC *1, *3	Synchronous Clearing Control	(Only valid in TWCRB) 0: Clearing of MTU6.TCNT and MTU7.TCNT in response to synchronous clearing for MTU0, MTU1, MTU2–MTU6, MTU7 is enabled. 1: Clearing of MTU6.TCNT and MTU7.TCNT in response to synchronous clearing for MTU0, MTU1, MTU2–MTU6, MTU7 is disabled.	R/(W)
b6 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	CCE*2	Compare Match Clear Enable	0: Counters are not cleared at MTU3.TGRA (MTU6.TGRA) compare match 1: Counters are cleared at MTU3.TGRA (MTU6.TGRA) compare match	R/(W)

Note 1. This bit is only valid in register TWCRB and is a reserved bit in register TWCRA.
Note 2. Do not set to 1 when complementary PWM mode 1 is not selected.
Note 3. Do not set to 1 when complementary PWM mode is not selected.

TWCRA and TWCRB control the output waveform when synchronous counter clearing occurs in MTU3.TCNT and MTU4.TCNT (MTU6.TCNT and MTU7.TCNT) in complementary PWM mode and specifies whether to clear the counters at MTU3.TGRA (MTU6.TGRA) compare match.
The CCE bit and WRE bit in TWCRA and TWCRB should be modified only while TCNT stops.

WRE Bit (Waveform Retain Enable)

This bit selects the waveform output when synchronous counter clearing occurs in complementary PWM mode.
The initial output is inhibited with this function only when synchronous clearing occurs within the Tb interval at the trough in complementary PWM mode. When synchronous clearing occurs outside this interval, the initial values specified in TOCR1A and TOCR2A (TOCR1B and TOCR2B) are output regardless of the WRE bit setting. The initial values specified in TOCR1A and TOCR2A (TOCR1B and TOCR2B) are also output when synchronous clearing occurs in the Tb interval at the trough immediately after MTU3.TCNT and MTU4.TCNT (MTU6.TCNT and MTU7.TCNT) start operation.
For the Tb interval at the trough in complementary PWM mode, refer to Figure 20.49.
[Setting condition]

- When 1 is written to the WRE bit after reading WRE = 0

SCC Bit (Synchronous Clearing Control)

The setting of this bit selects whether MTU6.TCNT and MTU7.TCNT are or are not cleared when counter-synchronous clearing is generated for MTU0, MTU1, MTU2–MTU6, MTU7 in complementary PWM mode.
Make the complementary PWM mode settings for MTU6 and MTU7 when this function is in use. When writing a new value to the SCC bit while the counter is operating, do so in such a way that the values of the CCE and WRE bits are not changed.
Synchronous clearing from the MTU module only becomes disabled due to the setting of the SCC bit when synchronous clearing is generated outside the Tb interval in the trough. If synchronous clearing is generated within the Tb interval in the trough including immediately after the value at which MTU6.TCNT and MTU7.TCNT start, MTU6.TCNT and MTU7.TCNT are cleared.
Regarding the Tb interval in the trough in complementary PWM mode, refer to Figure 20.49.
[Setting condition]

- Writing of 1 to the SCC bit after reading it as 0

The corresponding bit in register TWCRA is reserved and is read as 0. When writing to TWCRA, write 0 to this bit.

CCE Bit (Compare Match Clear Enable)

This bit specifies whether to clear counters at MTU3.TGRA (MTU6.TGRA) compare match in complementary PWM mode.
[Setting condition]

- When 1 is written to CCE after reading CCE = 0

20.2.33 Noise Filter Control Register n (NFCRn) (n = 0 to 4, 6, 7, 9, C)

- MTU0.NFCR0, MTU1.NFCR1, MTU2.NFCR2, MTU3.NFCR3, MTU4.NFCR4, MTU6.NFCR6, MTU7.NFCR7, MTU9.NFCR9

Address(es): MTU0.NFCR0 000C 1290h, MTU1.NFCR1 000C 1291h, MTU2.NFCR2 000C 1292h, MTU3.NFCR3 000C 1293h, MTU4.NFCR4 000C 1294h, MTU6.NFCR6 000C 1A93h, MTU7.NFCR7 000C 1A94h, MTU9.NFCR9 000C 1296h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	NFCS[1:0]		NFDEN	NFCEN	NFBEN	NFAEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	NFAEN	Noise Filter A Enable	0: The noise filter for the MTIOCnA pin is disabled. 1: The noise filter for the MTIOCnA pin is enabled.	R/W
b1	NFBEN	Noise Filter B Enable	0: The noise filter for the MTIOCnB pin is disabled. 1: The noise filter for the MTIOCnB pin is enabled.	R/W
b2	NFCEN	Noise Filter C Enable	0: The noise filter for the MTIOCnC pin is disabled. 1: The noise filter for the MTIOCnC pin is enabled.	R/W*1
b3	NFDEN	Noise Filter D Enable	0: The noise filter for the MTIOCnD pin is disabled. 1: The noise filter for the MTIOCnD pin is enabled.	R/W*1
b5, b4	NFCS[1:0]	Noise Filter Clock Select	b5 b4 0 0: PCLKA/1 0 1: PCLKA/8 1 0: PCLKA/32 1 1: Clock source for counting	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. These bits are reserved in the NFCR1 and NFCR2 registers. These bits are read as 0 and writing to them has no effect.

The NFCRn register sets the noise filter function of external clock pins common to each channel.

NFAEN Bit (Noise Filter A Enable)

This bit disables or enables the noise filter for input from the MTIOCnA pin. Since changing the value of the bit may lead to the internal generation of an unexpected edge, select the output compare function for the relevant pin in the timer I/O control register or set the TMDR.MD[3:0] bits to a value other than that for normal mode (0000b) before doing so.

NFBEN Bit (Noise Filter B Enable)

This bit disables or enables the noise filter for input from the MTIOCnB pin. Since changing the value of the bit may lead to the internal generation of an unexpected edge, select the output compare function for the relevant pin in the timer I/O control register or set the TMDR.MD[3:0] bits to a value other than that for normal mode (0000b) before doing so.

NFCEN Bit (Noise Filter C Enable)

This bit disables or enables the noise filter for input from the MTIOCnC pin. Since changing the value of the bit may lead to the internal generation of an unexpected edge, select the output compare function for the relevant pin in the timer I/O control register or set the TMDR.MD[3:0] bits to a value other than that for normal mode (0000b) before doing so.

NFDEN Bit (Noise Filter D Enable)

This bit disables or enables the noise filter for input from the MTIOCnD pin. Since changing the value of the bit may lead to the internal generation of an unexpected edge, select the output compare function for the relevant pin in the timer I/O control register or set the TMDR.MD[3:0] bits to a value other than that for normal mode (0000b) before doing so.

NFCS[1:0] Bits (Noise Filter Clock Select)

These bits set the sampling interval for the noise filters. When setting the NFCS[1:0] bits, wait for two cycles of the selected sampling interval before setting the input-capture function. When the NFCS[1:0] bits are set to 11b, i.e. selecting the external clock as the source to drive counting, wait for two cycles of the external clock before setting the input capture function.

- MTU0.NFCRC

Address(es): MTU0.NFCRC 000C 1299h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	NFCS[1:0]		NFDEN	NFCEN	NFBEN	NFAEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	NFAEN	Noise Filter A Enable	0: The noise filter for the MTCLKA pin is disabled. 1: The noise filter for the MTCLKA pin is enabled.	R/W
b1	NFBEN	Noise Filter B Enable	0: The noise filter for the MTCLKB pin is disabled. 1: The noise filter for the MTCLKB pin is enabled.	R/W
b2	NFCEN	Noise Filter C Enable	0: The noise filter for the MTCLKC pin is disabled. 1: The noise filter for the MTCLKC pin is enabled.	R/W
b3	NFDEN	Noise Filter D Enable	0: The noise filter for the MTCLKD pin is disabled. 1: The noise filter for the MTCLKD pin is enabled.	R/W
b5, b4	NFCS[1:0]	Noise Filter Clock Select	b5 b4 0 0: PCLKA/1 0 1: PCLKA/2 1 0: PCLKA/8 1 1: PCLKA/32	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

NFAEN Bit (Noise Filter A Enable)

This bit disables or enables the noise filter for input from the MTCLKA pin. Since changing the value of the bit may lead to the internal generation of an unexpected edge, do so after stopping the internal counter.

NFBEN Bit (Noise Filter B Enable)

This bit disables or enables the noise filter for input from the MTCLKB pin. Since changing the value of the bit may lead to the internal generation of an unexpected edge, do so after stopping the internal counter.

NFCEN Bit (Noise Filter C Enable)

This bit disables or enables the noise filter for input from the MTCLKC pin. Since changing the value of the bit may lead to the internal generation of an unexpected edge, do so after stopping the internal counter.

NFDEN Bit (Noise Filter D Enable)

This bit disables or enables the noise filter for input from the MTCLKD pin. Since changing the value of the bit may lead to the internal generation of an unexpected edge, do so after stopping the internal counter.

NFCS[1:0] Bits (Noise Filter Clock Select)

These bits set the sampling interval for the noise filters. After setting the NFCS[1:0] bits, wait for two cycles of the selected sampling interval to set the input capture function.

20.2.34 Noise Filter Control Register 5 (NFCR5)

Address(es): MTU5.NFCR5 000C 1A95h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	NFCS[1:0]		—	NFWEN	NFVEN	NFUEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	NFUEN	Noise Filter U Enable	0: The noise filter for the MTIC5U pin is disabled. 1: The noise filter for the MTIC5U pin is enabled.	R/W
b1	NFVEN	Noise Filter V Enable	0: The noise filter for the MTIC5V pin is disabled. 1: The noise filter for the MTIC5V pin is enabled.	R/W
b2	NFWEN	Noise Filter W Enable	0: The noise filter for the MTIC5W pin is disabled. 1: The noise filter for the MTIC5W pin is enabled.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b5, b4	NFCS[1:0]	Noise Filter Clock Select	b5 b4 0 0: PCLKA/1 0 1: PCLKA/8 1 0: PCLKA/32 1 1: Clock source for counting	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

NFUEN Bit (Noise Filter U Enable)

This bit disables or enables the noise filter for input from the MTIC5U pin. Since unexpected edges may be internally generated when the value of this bit is changed, select the output compare function for the relevant pin in the timer I/O control register.

NFVEN Bit (Noise Filter V Enable)

This bit disables or enables the noise filter for input from the MTIC5V pin. Since unexpected edges may be internally generated when the value of this bit is changed, select the output compare function for the relevant pin in the timer I/O control register.

NFWEN Bit (Noise Filter W Enable)

This bit disables or enables the noise filter for input from the MTIC5W pin. Since unexpected edges may be internally generated when the value of this bit is changed, select the output compare function for the relevant pin in the timer I/O control register.

NFCS[1:0] Bits (Noise Filter Clock Select)

These bits set the sampling interval for the noise filters. When setting the NFCS[1:0] bits, wait for two cycles of the selected sampling interval before setting the input-capture function.

20.2.35 Timer A/D Converter Start Request Control Register (TADCR)

- MTU4.TADCR

Address(es): MTU4.TADCR 000C 1240h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BF[1:0]		—	—	—	—	—	—	UT4AE	DT4AE	UT4BE	DT4BE	ITA3AE	ITA4VE	ITB3AE	ITB4VE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ITB4VE	TCIV4 Interrupt Skipping Link Enable*1, *2, *3	0: A/D converter start request signal TRG4BN and TCI4V interrupt skipping 1 are not linked 1: A/D converter start request signal TRG4BN and TCI4V interrupt skipping 1 are linked	R/W
b1	ITB3AE	TGIA3 Interrupt Skipping Link Enable*1, *2, *3	0: A/D converter start request signal TRG4BN and TGI3A interrupt skipping 1 are not linked 1: A/D converter start request signal TRG4BN and TGI3A interrupt skipping 1 are linked	R/W
b2	ITA4VE	TCIV4 Interrupt Skipping Link Enable*1, *2, *3	0: A/D converter start request signal TRG4AN and TCI4V interrupt skipping 1 are not linked 1: A/D converter start request signal TRG4AN and TCI4V interrupt skipping 1 are linked	R/W
b3	ITA3AE	TGIA3 Interrupt Skipping Link Enable*1, *2, *3	0: A/D converter start request signal TRG4AN and TGI3A interrupt skipping 1 are not linked 1: A/D converter start request signal TRG4AN and TGI3A interrupt skipping 1 are linked	R/W
b4	DT4BE	Down-Count TRG4BN Enable*3	0: A/D converter start requests (TRG4BN) disabled during MTU4.TCNT down-count operation 1: A/D converter start requests (TRG4BN) enabled during MTU4.TCNT down-count operation	R/W
b5	UT4BE	Up-Count TRG4BN Enable	0: A/D converter start requests (TRG4BN) disabled during MTU4.TCNT up-count operation 1: A/D converter start requests (TRG4BN) enabled during MTU4.TCNT up-count operation	R/W
b6	DT4AE	Down-Count TRG4AN Enable*3	0: A/D converter start requests (TRG4AN) disabled during MTU4.TCNT down-count operation 1: A/D converter start requests (TRG4AN) enabled during MTU4.TCNT down-count operation	R/W
b7	UT4AE	Up-Count TRG4AN Enable	0: A/D converter start requests (TRG4AN) disabled during MTU4.TCNT up-count operation 1: A/D converter up requests (TRG4AN) enabled during MTU4.TCNT down-count operation	R/W
b13 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15, b14	BF[1:0]	MTU4.TADCOBRA/TADCOBRB Transfer Timing Select	Refer to Table 20.53 for details. These bits specify the transfer timing from MTU4.TADCOBRA and MTU4.TADCOBRB to MTU4.TADCORA and MTU4.TADCORB.	R/W

Note: MTU4.TADCR must not be accessed in 8 bits; it should be accessed in 16 bits.
Note 1. Set to 0 when interrupt skipping is disabled (the T3AEN and T4VEN bits in TITCR1A are cleared to 0 or the T3ACOR and T4VCOR bits in TITCR1A are cleared to 0).
Note 2. If link with interrupt skipping is enabled while interrupt skipping is disabled, A/D converter start requests will not be issued.
Note 3. Set to 0 when complementary PWM mode is not selected.

TADCR enables or disables A/D converter start requests and specifies whether to link A/D converter start requests with interrupt skipping function. The MTU has one TADCR each for MTU4 and MTU7.

Table 20.53 Setting of Transfer Timing by TADCR.BF[1:0] Bits (MTU4)

Bit 15	Bit 14	Description			
BF[1]	**BF[0]**	**In Complementary PWM Mode**	**In Reset-Synchronized PWM Mode**	**In PWM Mode 1**	**In Normal Mode**
0	0	Data is not transferred from the cycle set buffer register (MTU4.TADCOBRA, MTU4.TADCOBRB) to the cycle set register (MTU4.TADCORA, MTU4.TADCORB).	Data is not transferred from the cycle set buffer register (MTU4.TADCOBRA, MTU4.TADCOBRB) to the cycle set register (MTU4.TADCORA, MTU4.TADCORB).	Data is not transferred from the cycle set buffer register (MTU4.TADCOBRA, MTU4.TADCOBRB) to the cycle set register (MTU4.TADCORA, MTU4.TADCORB).	Data is not transferred from the cycle set buffer register (MTU4.TADCOBRA, MTU4.TADCOBRB) to the cycle set register (MTU4.TADCORA, MTU4.TADCORB).
0	1	Data is transferred from the cycle set buffer register (MTU4.TADCOBRA, MTU4.TADCOBRB) to the cycle set register (MTU4.TADCORA, MTU4.TADCORB) at the crest of the MTU4.TCNT.	Data is transferred from the cycle set buffer register (MTU4.TADCOBRA, MTU4.TADCOBRB) to the cycle set register (MTU4.TADCORA, MTU4.TADCORB) when a compare match occurs between MTU3.TCNT and MTU3.TGRA.	Data is transferred from the cycle set buffer register (MTU4.TADCOBRA, MTU4.TADCOBRB) to the cycle set register (MTU4.TADCORA, MTU4.TADCORB) when a compare match occurs between MTU4.TCNT and MTU4.TGRA.	Data is transferred from the cycle set buffer register (MTU4.TADCOBRA, MTU4.TADCOBRB) to the cycle set register (MTU4.TADCORA, MTU4.TADCORB) when a compare match occurs between MTU4.TCNT and MTU4.TGRA.
1	0	Data is transferred from the cycle set buffer register (MTU4.TADCOBRA, MTU4.TADCOBRB) to the cycle set register (MTU4.TADCORA, MTU4.TADCORB) at the trough of the MTU4.TCNT.	Setting prohibited	Setting prohibited	Setting prohibited
1	1	Data is transferred from the cycle set buffer register (MTU4.TADCOBRA, MTU4.TADCOBRB) to the cycle set register (MTU4.TADCORA, MTU4.TADCORB) at the crest and trough of the MTU4.TCNT.	Setting prohibited	Setting prohibited	Setting prohibited

- MTU7.TADCR

Address(es): MTU7.TADCR 000C 1A40h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BF[1:0]		—	—	—	—	—	—	UT7AE	DT7AE	UT7BE	DT7BE	ITA6AE	ITA7VE	ITB6AE	ITB7VE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ITB7VE	TCIV7 Interrupt Skipping Link Enable*1, *2, *3	0: A/D converter start request signal TRG7BN and TCI7V interrupt skipping 1 are not linked 1: A/D converter start request signal TRG7BN and TCI7V interrupt skipping 1 are linked	R/W
b1	ITB6AE	TGIA6 Interrupt Skipping Link Enable*1, *2, *3	0: A/D converter start request signal TRG7BN and TGI6A interrupt skipping 1 are not linked 1: A/D converter start request signal TRG7BN and TGI6A interrupt skipping 1 are linked	R/W
b2	ITA7VE	TCIV7 Interrupt Skipping Link Enable*1, *2, *3	0: A/D converter start request signal TRG7AN and TCI7V interrupt skipping 1 are not linked 1: A/D converter start request signal TRG7AN and TCI7V interrupt skipping 1 are linked	R/W
b3	ITA6AE	TGIA6 Interrupt Skipping Link Enable*1, *2, *3	0: A/D converter start request signal TRG7AN and TGI6A interrupt skipping 1 are not linked 1: A/D converter start request signal TRG7AN and TGI6A interrupt skipping 1 are linked	R/W
b4	DT7BE	Down-Count TRG7BN Enable*3	0: A/D converter start requests (TRG7BN) disabled during MTU7.TCNT down-count operation 1: A/D converter start requests (TRG7BN) enabled during MTU7.TCNT down-count operation	R/W
b5	UT7BE	Up-Count TRG7BN Enable	0: A/D converter start requests (TRG7BN) disabled during MTU7.TCNT up-count operation 1: A/D converter start requests (TRG7BN) enabled during MTU7.TCNT up-count operation	R/W
b6	DT7AE	Down-Count TRG7AN Enable*3	0: A/D converter start requests (TRG7AN) disabled during MTU7.TCNT down-count operation 1: A/D converter start requests (TRG7AN) enabled during MTU7.TCNT down-count operation	R/W
b7	UT7AE	Up-Count TRG7AN Enable	0: A/D converter start requests (TRG7AN) disabled during MTU7.TCNT up-count operation 1: A/D converter up requests (TRG7AN) enabled during MTU7.TCNT down-count operation	R/W
b13 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15, b14	BF[1:0]	MTU7.TADCOBRA/TADCOBRB Transfer Timing Select	Refer to Table 20.54 for details. These bits specify the transfer timing from MTU7.TADCOBRA and MTU7.TADCOBRB to MTU7.TADCORA and MTU7.TADCORB.	R/W

Note: MTU7.TADCR must not be accessed in 8 bits; it should be accessed in 16 bits.
Note 1. Set to 0 when interrupt skipping is disabled (the T6AEN and T7VEN bits in TITCR1B are cleared to 0 or the T6ACOR and T7VCOR bits in TITCR1B are cleared to 0).
Note 2. If link with interrupt skipping is enabled while interrupt skipping is disabled, A/D converter start requests will not be issued.
Note 3. Set to 0 when complementary PWM mode is not selected.

Table 20.54 Setting of Transfer Timing by TADCR.BF[1:0] Bits (MTU7)

Bit 15	Bit 14	Description			
BF[1]	**BF[0]**	**In Complementary PWM Mode**	**In Reset-Synchronized PWM Mode**	**In PWM Mode 1**	**In Normal Mode**
0	0	Data is not transferred from the cycle set buffer register (MTU7.TADCOBRA, MTU7.TADCOBRB) to the cycle set register (MTU7.TADCORA, MTU7.TADCORB).	Data is not transferred from the cycle set buffer register (MTU7.TADCOBRA, MTU7.TADCOBRB) to the cycle set register (MTU7.TADCORA, MTU7.TADCORB).	Data is not transferred from the cycle set buffer register (MTU7.TADCOBRA, MTU7.TADCOBRB) to the cycle set register (MTU7.TADCORA, MTU7.TADCORB).	Data is not transferred from the cycle set buffer register (MTU7.TADCOBRA, MTU7.TADCOBRB) to the cycle set register (MTU7.TADCORA, MTU7.TADCORB).
0	1	Data is transferred from the cycle set buffer register (MTU7.TADCOBRA, MTU7.TADCOBRB) to the cycle set register (MTU7.TADCORA, MTU7.TADCORB) at the crest of the MTU7.TCNT.	Data is transferred from the cycle set buffer register (MTU7.TADCOBRA, MTU7.TADCOBRB) to the cycle set register (MTU7.TADCORA, MTU7.TADCORB) when a compare match occurs between MTU6.TCNT and MTU6.TGRA.	Data is transferred from the cycle set buffer register (MTU7.TADCOBRA, MTU7.TADCOBRB) to the cycle set register (MTU7.TADCORA, MTU7.TADCORB) when a compare match occurs between MTU7.TCNT and MTU7.TGRA.	Data is transferred from the cycle set buffer register (MTU7.TADCOBRA, MTU7.TADCOBRB) to the cycle set register (MTU7.TADCORA, MTU7.TADCORB) when a compare match occurs between MTU7.TCNT and MTU7.TGRA.
1	0	Data is transferred from the cycle set buffer register (MTU7.TADCOBRA, MTU7.TADCOBRB) to the cycle set register (MTU7.TADCORA, MTU7.TADCORB) at the trough of the MTU7.TCNT.	Setting prohibited	Setting prohibited	Setting prohibited
1	1	Data is transferred from the cycle set buffer register (MTU7.TADCOBRA, MTU7.TADCOBRB) to the cycle set register (MTU7.TADCORA, MTU7.TADCORB) at the crest and trough of the MTU7.TCNT.	Setting prohibited	Setting prohibited	Setting prohibited

20.2.36 Timer A/D Converter Start Request Cycle Set Registers (TADCORA, TADCORB)

Address(es): MTU4.TADCORA 000C 1244h, MTU4.TADCORB 000C 1246h, MTU7.TADCORA 000C 1A44h, MTU7.TADCORB 000C 1A46h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: TADCORA and TADCORB must not be accessed in 8 bits; it should be accessed in 16 bits.

Note 1. When the A/D converter start request delaying function linked with skipping function 1 (for details, refer to section 20.3.9 (5), A/D Converter Start Request Delaying Function Linked with Interrupt Skipping Function 1) is used, the value of this register should be 0002h to TCDRA setting – 2 in MTU4 and 0002h to TCDRB setting – 2 in MTU7.

Note 2. When interrupt skipping function 2 is used and the difference between the TADCORA value and the TADCORB value is small, the skipping count may not be counted correctly and the A/D converter start request may not be generated with the expected timing in some cases. The TADCORA and TADCORB values should satisfy the following conditions.

(1) When skipping function 2 is specified with the skipping count set to 0
- The difference between the TADCORA and TADCORB values should be equal to or greater than 4.
- The TADCORA compare interval should be equal to or greater than 4 PCLKA cycles (the TADCORA update value should be the previous value + 4 or greater, or previous value – 4 or smaller).
- The TADCORB compare interval should be equal to or greater than 4 PCLKA cycles (the TADCORB update value should be the previous value + 4 or greater, or previous value – 4 or smaller).

(2) When skipping function 2 is specified with the skipping count set to 1 or greater
- The difference between the TADCORA and TADCORB values should be equal to or greater than 2.
- The TADCORB compare interval should be equal to or greater than 2 PCLKA cycles (the TADCORB update value should be the previous value + 2 or greater, or previous value – 2 or smaller)

TADCORA and TADCORB are 16-bit readable/writable registers that issue a corresponding A/D converter start request when the MTUn.TCNT (n = 4, 7) count reaches the value in TADCORA or TADCORB.
MTUn.TADCORA and TADCORB are initialized to FFFFh by a reset.

20.2.37 Timer A/D Converter Start Request Cycle Set Buffer Registers (TADCOBRA, TADCOBRB)

Address(es): MTU4.TADCOBRA 000C 1248h, MTU4.TADCOBRB 000C 124Ah, MTU7.TADCOBRA 000C 1A48h, MTU7.TADCOBRB 000C 1A4Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: TADCOBRA and TADCOBRB must not be accessed in 8 bits; it should be accessed in 16 bits.

TADCOBRA and TADCOBRB are 16-bit readable/writable registers whose values are transferred to TADCORA and TADCORB, respectively, when the crest or trough of the MTUn.TCNT count is reached.
TADCOBRA and TADCOBRB are initialized to FFFFh by a reset.

20.2.38 Timer Interrupt Skipping Mode Registers (TITMRA, TITMRB)

Address(es): MTU.TITMRA 000C 123Ah, MTU.TITMRB 000C 1A3Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	TITM
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TITM	Interrupt Skipping Function Select	Selects one of the two types of interrupt skipping functions shown in Table 20.55.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TITMRA and TITMRB are used to select either of two skipping functions for the TITMRA and TITMRB registers.

Table 20.55 Interrupt Skipping Function Selected through TITM Bit

Bit 0	
TITM	**Description**
0	Selects interrupt skipping function 1*1
1	Selects interrupt skipping function 2*2

Note 1. TITCR1A or TITCR1B enables interrupt skipping function 1.
Note 2. TITCR2A or TITCR2B enables interrupt skipping function 2.

20.2.39 Timer Interrupt Skipping Set Registers 1 (TITCR1A, TITCR1B)

- MTU.TITCR1A

Address(es): MTU.TITCR1A 000C 1230h

	b7	b6	b5	b4	b3	b2	b1	b0
	T3AEN	T3ACOR[2:0]			T4VEN	T4VCOR[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	T4VCOR[2:0]	TCIV4 Interrupt Skipping Count Setting	These bits specify the TCIV4 interrupt skipping count within the range from 0 to 7.*1 For details, refer to Table 20.56.	R/W
b3	T4VEN	T4VEN	0: TCIV4 interrupt skipping disabled 1: TCIV4 interrupt skipping enabled	R/W
b6 to b4	T3ACOR[2:0]	TGIA3 Interrupt Skipping Count Setting	These bits specify the TGIA3 interrupt skipping count within the range from 0 to 7.*1 For details, refer to Table 20.57.	R/W
b7	T3AEN	T3AEN	0: TGIA3 interrupt skipping disabled 1: TGIA3 interrupt skipping enabled	R/W

Note 1. When 0 is specified for the interrupt skipping count, no interrupt skipping will be performed.
Before changing the interrupt skipping count, be sure to clear the TITCR1A.T3AEN and TITCR1A.T4VEN bits to 0 to clear the skipping counter (TITCNT1A).

- MTU.TITCR1B

Address(es): MTU.TITCR1B 000C 1A30h

	b7	b6	b5	b4	b3	b2	b1	b0
	T6AEN	T6ACOR[2:0]			T7VEN	T7VCOR[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	T7VCOR[2:0]	TCIV7 Interrupt Skipping Count Setting	These bits specify the TCIV7 interrupt skipping count within the range from 0 to 7.*1 For details, refer to Table 20.58.	R/W
b3	T7VEN	T7VEN	0: TCIV7 interrupt skipping disabled 1: TCIV7 interrupt skipping enabled	R/W
b6 to b4	T6ACOR[2:0]	TGIA6 Interrupt Skipping Count Setting	These bits specify the TGIA6 interrupt skipping count within the range from 0 to 7.*1 For details, refer to Table 20.59.	R/W
b7	T6AEN	T6AEN	0: TGIA6 interrupt skipping disabled 1: TGIA6 interrupt skipping enabled	R/W

Note 1. When 0 is specified for the interrupt skipping count, no interrupt skipping will be performed.
Before changing the interrupt skipping count, be sure to clear the TITCR1B.T6AEN and TITCR1B.T7VEN bits to 0 to clear the skipping counter (TITCNT1B).

Registers TITCR1A and TITCR1B enable or disable interrupt skipping and specify the interrupt skipping count. This setting is valid only while the TITMRA.TITM or TITMRB.TITM bit is set to 0; when the TITMRA.TITM (TITMRB.TITM) bit is set to 1, the setting in the TITCR1A (TITCR1B) register is cleared.

Table 20.56 Setting of Interrupt Skipping Count by T4VCOR[2:0] Bits

Bit 2	Bit 1	Bit 0	
T4VCOR[2]	T4VCOR[1]	T4VCOR[0]	Description
0	0	0	Does not skip TCIV4 interrupts.
0	0	1	Sets the TCIV4 interrupt skipping count to 1.
0	1	0	Sets the TCIV4 interrupt skipping count to 2.
0	1	1	Sets the TCIV4 interrupt skipping count to 3.
1	0	0	Sets the TCIV4 interrupt skipping count to 4.
1	0	1	Sets the TCIV4 interrupt skipping count to 5.
1	1	0	Sets the TCIV4 interrupt skipping count to 6.
1	1	1	Sets the TCIV4 interrupt skipping count to 7.

Table 20.57 Setting of Interrupt Skipping Count by T3ACOR[2:0] Bits

Bit 6	Bit 5	Bit 4	
T3ACOR[2]	T3ACOR[1]	T3ACOR[0]	Description
0	0	0	Does not skip TGIA3 interrupts.
0	0	1	Sets the TGIA3 interrupt skipping count to 1.
0	1	0	Sets the TGIA3 interrupt skipping count to 2.
0	1	1	Sets the TGIA3 interrupt skipping count to 3.
1	0	0	Sets the TGIA3 interrupt skipping count to 4.
1	0	1	Sets the TGIA3 interrupt skipping count to 5.
1	1	0	Sets the TGIA3 interrupt skipping count to 6.
1	1	1	Sets the TGIA3 interrupt skipping count to 7.

Table 20.58 Setting of Interrupt Skipping Count by T7VCOR[2:0] Bits

Bit 2	Bit 1	Bit 0	
T7VCOR[2]	T7VCOR[1]	T7VCOR[0]	Description
0	0	0	Does not skip TCIV7 interrupts.
0	0	1	Sets the TCIV7 interrupt skipping count to 1.
0	1	0	Sets the TCIV7 interrupt skipping count to 2.
0	1	1	Sets the TCIV7 interrupt skipping count to 3.
1	0	0	Sets the TCIV7 interrupt skipping count to 4.
1	0	1	Sets the TCIV7 interrupt skipping count to 5.
1	1	0	Sets the TCIV7 interrupt skipping count to 6.
1	1	1	Sets the TCIV7 interrupt skipping count to 7.

Table 20.59 Setting of Interrupt Skipping Count by T6ACOR[2:0] Bits

Bit 6	Bit 5	Bit 4	
T6ACOR[2]	T6ACOR[1]	T6ACOR[0]	Description
0	0	0	Does not skip TGIA6 interrupts.
0	0	1	Sets the TGIA6 interrupt skipping count to 1.
0	1	0	Sets the TGIA6 interrupt skipping count to 2.
0	1	1	Sets the TGIA6 interrupt skipping count to 3.
1	0	0	Sets the TGIA6 interrupt skipping count to 4.
1	0	1	Sets the TGIA6 interrupt skipping count to 5.
1	1	0	Sets the TGIA6 interrupt skipping count to 6.
1	1	1	Sets the TGIA6 interrupt skipping count to 7.

20.2.40 Timer Interrupt Skipping Counters 1 (TITCNT1A, TITCNT1B)

- MTU.TITCNT1A

Address(es): MTU.TITCNT1A 000C 1231h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	T3ACNT[2:0]			—	T4VCNT[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	T4VCNT[2:0]	TCIV4 Interrupt Counter	While the T4VEN bit in TITCR1A is set to 1, the count in these bits is incremented every time a TCIV4 interrupt occurs.	R
b3	—	Reserved	This bit is read as 0. Writing to this bit has no effect.	R
b6 to b4	T3ACNT[2:0]	TGIA3 Interrupt Counter	While the T3AEN bit in TITCR1A is set to 1, the count in these bits is incremented every time a TGIA3 interrupt occurs.	R
b7	—	Reserved	This bit is read as 0. Writing to this bit has no effect.	R

Note 1. To clear the TITCNT1A, clear the TITCR1A.T3AEN and TITCR1A.T4VEN bits to 0.

TITCNT1A and TITCNT1B are 8-bit readable/writable counters. TITCNT1A and TITCNT1B retain their values even after stopping the count operation of MTU3.TCNT and MTU4.TCNT (MTU6.TCNT and MTU7.TCNT).

T4VCNT[2:0] Bits (TCIV4 Interrupt Counter)

[Clearing conditions]

- When the TITM bit in TITMRA is 1
- When the T4VEN bit in TITCR1A is cleared to 0
- When the T4VCOR[2:0] bits in TITCR1A are cleared to 000b
- When the T4VCNT[2:0] bits in TITCNT1A match the T4VCOR[2:0] bits in TITCR1A

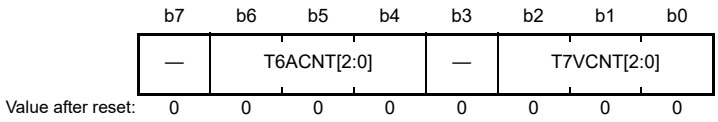
T3ACNT[2:0] Bits (TGIA3 Interrupt Counter)

[Clearing conditions]

- When the TITM bit in TITMRA is 1
- When the T3AEN bit in TITCR1A is cleared to 0
- When the T3ACOR[2:0] bits in TITCR1A are cleared to 000b
- When the T3ACNT[2:0] bits in TITCNT1A match the T3ACOR[2:0] bits in TITCR1A

- MTU.TITCNT1B

Address(es): MTU.TITCNT1B 000C 1A31h



Bit	Symbol	Bit Name	Description	R/W
b2 to b0	T7VCNT[2:0]	TCIV7 Interrupt Counter	While the T7VEN bit in TITCR1B is set to 1, the count in these bits is incremented every time a TCIV7 interrupt occurs.	R
b3	—	Reserved	This bit is read as 0. Writing to this bit has no effect.	R
b6 to b4	T6ACNT[2:0]	TGIA6 Interrupt Counter	While the T6AEN bit in TITCR1B is set to 1, the count in these bits is incremented every time a TGIA6 interrupt occurs.	R
b7	—	Reserved	This bit is read as 0. Writing to this bit has no effect.	R

Note 1. To clear the TITCNT1B, clear the TITCR1B.T6AEN and TITCR1B.T7VEN bits to 0.

T7VCNT[2:0] Bits (TCIV7 Interrupt Counter)

[Clearing conditions]

- When the TITM bit in TITMRB is 1
- When the T7VEN bit in TITCR1B is cleared to 0
- When the T7VCOR[2:0] bits in TITCR1B are cleared to 000b
- When the T7VCNT[2:0] bits in TITCNT1B match the T7VCOR[2:0] bits in TITCR1B

T6ACNT[2:0] Bits (TGIA6 Interrupt Counter)

[Clearing conditions]

- When the TITM bit in TITMRB is 1
- When the T6AEN bit in TITCR1B is cleared to 0
- When the T6ACOR[2:0] bits in TITCR1B are cleared to 000b
- When the T6ACNT[2:0] bits in TITCNT1B match the T6ACOR[2:0] bits in TITCR1B

20.2.41 Timer Interrupt Skipping Set Registers 2 (TITCR2A, TITCR2B)

- MTU.TITCR2A

Address(es): MTU.TITCR2A 000C 123Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	TRG4COR[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	TRG4COR[2:0]	TRG4AN/TRG4BN Interrupt Skipping Count Setting	These bits specify the TRG4AN/TRG4BN interrupt skipping count within the range from 0 to 7. For details, refer to Table 20.60.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TITCR2A and TITCR2B specify the interrupt skipping count for TRG4AN and TRG4BN (TRG7AN and TRG7BN). This setting is valid only while TITMRA or TITMRB is set to 1.

Table 20.60 Setting of Interrupt Skipping Count by TRG4COR[2:0] Bits

Bit 2	Bit 1	Bit 0	
TRG4COR[2]	TRG4COR[1]	TRG4COR[0]	Description
0	0	0	Does not skip TRG4AN and TRG4BN interrupts.
0	0	1	Sets the TRG4AN and TRG4BN interrupt skipping count to 1.
0	1	0	Sets the TRG4AN and TRG4BN interrupt skipping count to 2.
0	1	1	Sets the TRG4AN and TRG4BN interrupt skipping count to 3.
1	0	0	Sets the TRG4AN and TRG4BN interrupt skipping count to 4.
1	0	1	Sets the TRG4AN and TRG4BN interrupt skipping count to 5.
1	1	0	Sets the TRG4AN and TRG4BN interrupt skipping count to 6.
1	1	1	Sets the TRG4AN and TRG4BN interrupt skipping count to 7.

- MTU.TITCR2B

Address(es): MTU.TITCR2B 000C 1A3Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	TRG7COR[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	TRG7COR[2:0]	TRG7AN/TRG7BN Interrupt Skipping Count Setting	These bits specify the TRG7AN/TRG7BN interrupt skipping count within the range from 0 to 7. For details, refer to Table 20.61.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Table 20.61 Setting of Interrupt Skipping Count by TRG7COR[2:0] Bits

Bit 2	Bit 1	Bit 0	
TRG7COR[2]	TRG7COR[1]	TRG7COR[0]	Description
0	0	0	Does not skip TRG7AN and TRG7BN interrupts.
0	0	1	Sets the TRG7AN and TRG7BN interrupt skipping count to 1.
0	1	0	Sets the TRG7AN and TRG7BN interrupt skipping count to 2.
0	1	1	Sets the TRG7AN and TRG7BN interrupt skipping count to 3.
1	0	0	Sets the TRG7AN and TRG7BN interrupt skipping count to 4.
1	0	1	Sets the TRG7AN and TRG7BN interrupt skipping count to 5.
1	1	0	Sets the TRG7AN and TRG7BN interrupt skipping count to 6.
1	1	1	Sets the TRG7AN and TRG7BN interrupt skipping count to 7.

20.2.42 Timer Interrupt Skipping Counters 2 (TITCNT2A, TITCNT2B)

- MTU.TITCNT2A

Address(es): MTU.TITCNT2A 000C 123Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	TRG4CNT[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	TRG4CNT[2:0]	TRG4AN/TRG4BN Interrupt Counter	These bits start counting from the value set in TRG4COR[2:0] and the count decrements every time TRG4AN or TRG4BN is generated. When the count reaches 0 and is reloaded, the TRG4AN and TRG4BN interrupts become valid.	R
b7 to b3	—	Reserved	These bits are read as 0. Writing to these bit has no effect.	R

TITCNT2A and TITCNT2B start counting from the values set in the TRG4COR[2:0] and TRG7COR[2:0] bits and the count decrements every time TRG4AN or TRG4BN (TITCNT2A) is generated or TRG7AN or TRG7BN (TITCNT2B) is generated. When the count reaches 0 and is reloaded, the TRG4AN and TRG4BN interrupts or the TRG7AN and TRG7BN interrupts become valid.

TRG4CNT[2:0] Bits (TRG4AN/TRG4BN Interrupt Counter)

These bits start counting from the value set in the TRG4COR[2:0] bits and the count decrements every time a TRG4AN or TRG4BN interrupt is generated. When the count reaches 0 and is reloaded, the TRG4AN and TRG4BN interrupts become valid.

[Clearing conditions]

- When the TITM bit in TITMRA is 0
- When the TRG4COR[2:0] bits in TITCR2A are cleared to 000b
- When the count of TRG4AN and TRG4BN occurrence matches the TRG4COR[2:0] value in TITCR2A

- MTU.TITCNT2B

Address(es): MTU.TITCNT2B 000C 1A3Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	TRG7CNT[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	TRG7CNT[2:0]	TRG7AN/TRG7BN Interrupt Counter	These bits start counting from the value set in TRG7COR[2:0] and the count decrements every time TRG7AN or TRG7BN is generated. When the count reaches 0 and is reloaded, the TRG7AN and TRG7BN interrupts become valid.	R
b7 to b3	—	Reserved	These bits are read as 0. Writing to these bit has no effect.	R

TRG7CNT[2:0] Bits (TRG7AN/TRG7BN Interrupt Counter)

These bits start counting from the value set in the TRG7COR[2:0] bits and the count decrements every time a TRG7AN or TRG7BN interrupt is generated. When the count reaches 0 and is reloaded, the TRG7AN and TRG7BN interrupts become valid.

[Clearing conditions]

- When the TITM bit in TITMRB is 0
- When the TRG7COR[2:0] bits in TITCR2B are cleared to 000b
- When the count of TRG7AN and TRG7BN occurrence matches the TRG7COR[2:0] value in TITCR2B

20.2.43 A/D Conversion Start Request Select Register 0 (TADSTRGR0)

Address(es): MTU.TADSTRGR0 000C 1D30h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	TADSTRS0[4:0]				
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	TADSTRS0[4:0]	A/D Conversion Start Request Select for ADSM0 Pin Output Frame Synchronization Signal Generation	These bits select the A/D conversion start request for generating the frame synchronization signal to be output from the ADSM0 pin. Refer to Table 20.62 for the relationship between the A/D conversion start request and settings. Settings other than those listed in Table 20.62 are prohibited.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The TADSTRGR0 register selects the A/D conversion start request for generating the A/D conversion start request frame synchronization signal to be output from the ADSM0 pin.

20.2.44 A/D Conversion Start Request Select Register 1 (TADSTRGR1)

Address(es): MTU.TADSTRGR1 000C 1D32h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	TADSTRS1[4:0]				
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	TADSTRS1[4:0]	A/D Conversion Start Request Select for ADSM1 Pin Output Frame Synchronization Signal Generation	These bits select the A/D conversion start request for generating the frame synchronization signal to be output from the ADSM1 pin. Refer to Table 20.62 for the relationship between the A/D conversion start request and settings. Settings other than those listed in Table 20.62 are prohibited.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The TADSTRGR1 register selects the A/D conversion start request for generating the A/D conversion start request frame synchronization signal to be output from the ADSM1 pin.

Table 20.62 Settings of A/D Conversion Start Request for Generating Frame Synchronization Signal (n = 0, 1)

TADSTRSn[4:0]						
[4]	[3]	[2]	[1]	[0]	Source	Descriptions
0	0	0	0	0	—	Source not selected
0	0	0	0	1	TRGA0N	Compare match/input capture in MTU0.TGRA
0	0	0	1	0	TRGA1N	Compare match/input capture in MTU1.TGRA
0	0	0	1	1	TRGA2N	Compare match/input capture in MTU2.TGRA
0	0	1	0	0	TRGA3N	Compare match/input capture in MTU3.TGRA
0	0	1	0	1	TRGA4N	Compare match/input capture in MTU4.TGRA or MTU4.TCNT underflow (trough) in complementary PWM mode
0	0	1	1	0	TRGA6N	Compare match/input capture in MTU6.TGRA
0	0	1	1	1	TRGA7N	Compare match/input capture in MTU7.TGRA or MTU7.TCNT underflow (trough) in complementary PWM mode
0	1	0	0	0	TRG0N	Compare match in MTU0.TGRE
0	1	0	0	1	TRG4AN	Compare match between MTU4.TADCORA and MTU4.TCNT
0	1	0	1	0	TRG4BN	Compare match between MTU4.TADCORB and MTU4.TCNT
0	1	1	0	0	TRG4ABN	Compare match between MTU4.TADCORA and MTU4.TCNT or compare match between MTU4.TADCORB and MTU4.TCNT (Interrupt skipping function 2 used)
0	1	1	0	1	TRG7AN	Compare match between MTU7.TADCORA and MTU7.TCNT
0	1	1	1	0	TRG7BN	Compare match between MTU7.TADCORB and MTU7.TCNT
1	0	0	0	0	TRG7ABN	Compare match between MTU7.TADCORA and MTU7.TCNT or compare match between MTU7.TADCORB and MTU7.TCNT (Interrupt skipping function 2 used)
1	0	0	0	1	TRGA9N	Compare match/input capture in MTU9.TGRA
1	0	0	1	0	TRG9N	Compare match in MTU9.TGRE
1	0	0	1	1	TRG9AEN	Compare match/input capture in MTU9.TGRA or compare match in MTU9.TGRE
1	0	1	0	0	TRG0AEN	Compare match/input capture in MTU0.TGRA or compare match in MTU0.TGRE
1	0	1	0	1	TRGA09N	Compare match/input capture in MTU0.TGRA or compare match/input capture in MTU9.TGRA
1	0	1	1	0	TRG09N	Compare match in MTU0.TGRE or compare match in MTU9.TGRE

20.3 Operation

20.3.1 Basic Functions

Each channel has TCNT and TGR register. TCNT performs up-counting, and is also capable of free-running operation, periodic counting, and external event counting.
Each TGR register can be used as an input capture register or an output compare register.

(1) Counter Operation

When one of bits CST0 to CST4 and CST9 in the TSTRA register, bits CST6 and CST7 in the TSTRB register, and bits CSTU5, CSTV5, and CSTW5 in the MTU5.TSTR register is set to 1, TCNT for the corresponding channel begins counting. TCNT can operate as a free-running counter, periodic counter, for example.

(a) Example of Count Operation Setting Procedure

Figure 20.5 shows an example of the count operation setting procedure.

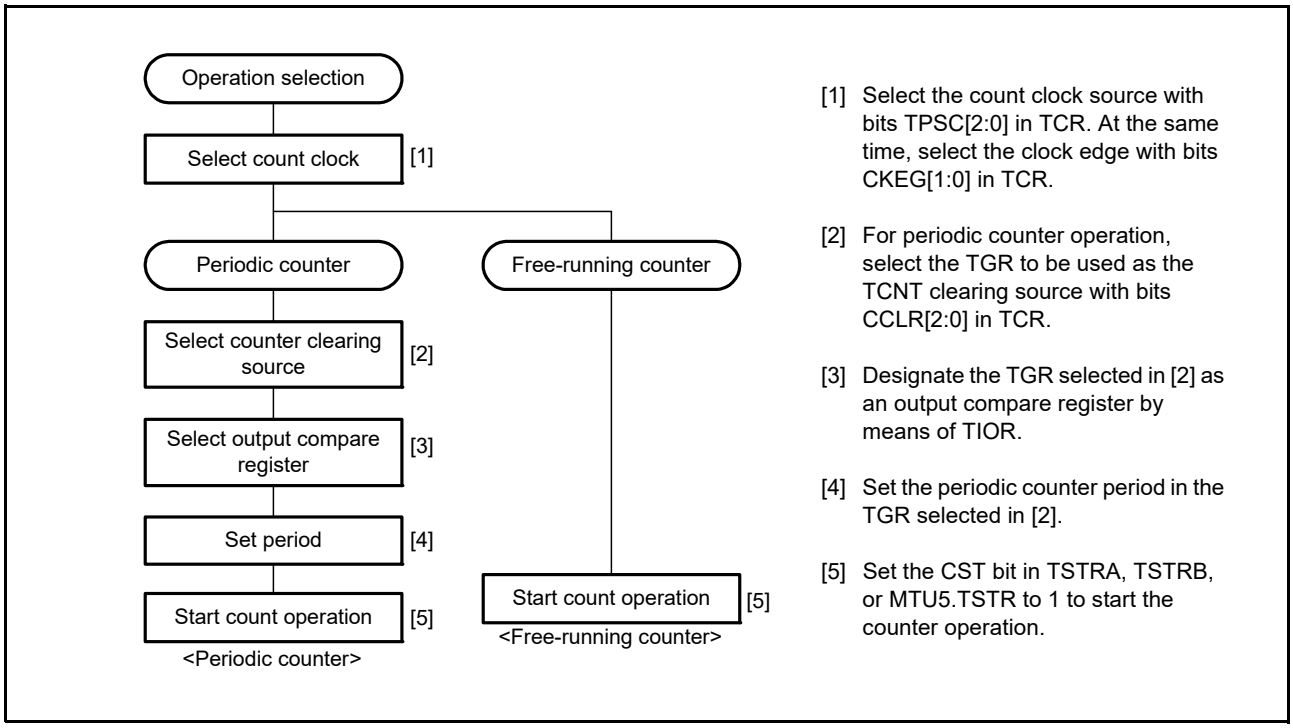


Figure 20.5 Example of Counter Operation Setting Procedure

(b) Free-Running Count Operation and Periodic Count Operation

Immediately after a reset, the TCNT counters are all designated as free-running counters. When the relevant bit in TSTRA, TSTRB, or MTU5.TSTR is set to 1, the corresponding TCNT counter starts up-count operation as a free-running counter. When TCNT overflows (from FFFFh to 0000h), an interrupt request is issued to the CPU if the corresponding TIER.TCIEV bit is 1. After an overflow, TCNT starts counting up again from 0000h.
Figure 20.6 illustrates free-running counter operation.

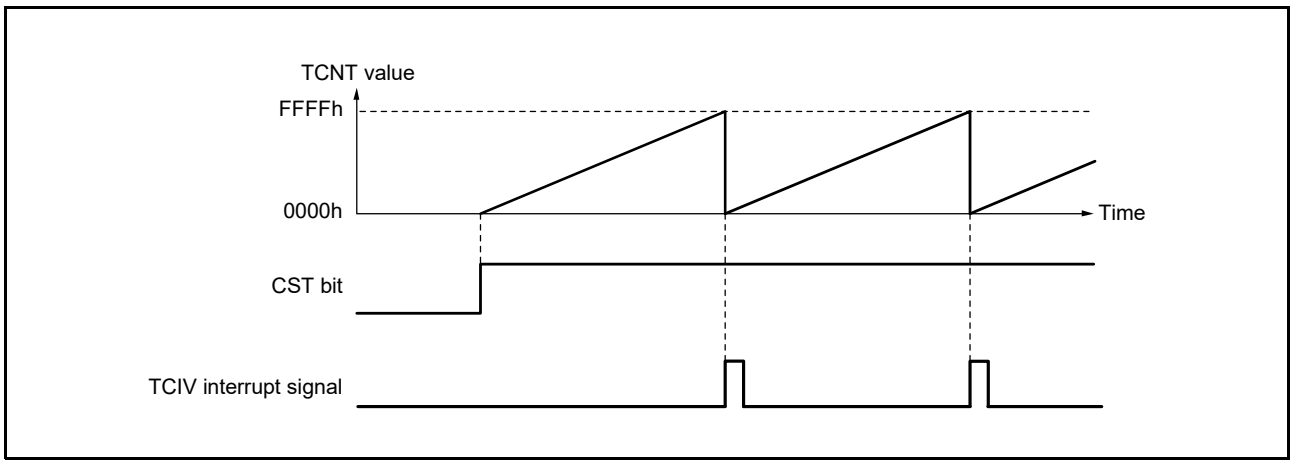


Figure 20.6 Free-Running Counter Operation

When compare match is selected as the TCNT clearing source, TCNT for the relevant channel performs periodic count operation. TGR for setting the period is designated as an output compare register, and counter clearing by compare match is selected by means of bits CCLR[2:0] in TCR. After the settings have been made, TCNT starts up-count operation as a periodic counter when the corresponding bit in TSTRA, TSTRB or MTU5.TSTR is set to 1. When the count matches the value in TGR, TCNT is cleared to 0000h.
If the value of the corresponding TIER.TGIE bit is 1 at this point, an interrupt request is issued to the CPU. After a compare match, TCNT starts counting up again from 0000h.
Figure 20.7 illustrates periodic counter operation.

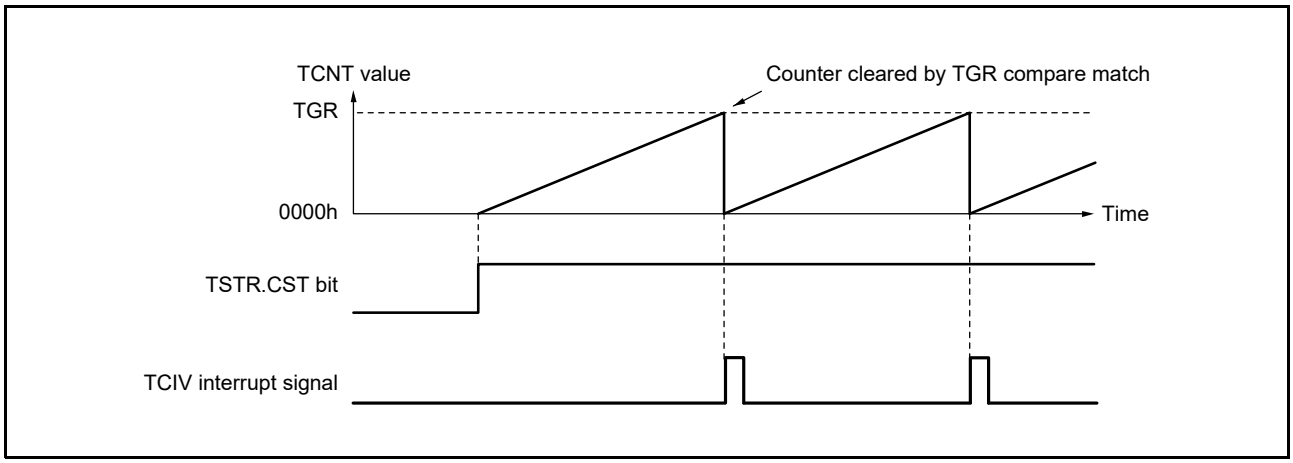


Figure 20.7 Periodic Counter Operation

(2) Waveform Output by Compare Match

Upon compare match, low, high, or toggle output from the corresponding pin can be performed.

(a) Example of Procedure for Setting Waveform Output by Compare Match

Figure 20.8 shows an example of the procedure for setting waveform output by compare match

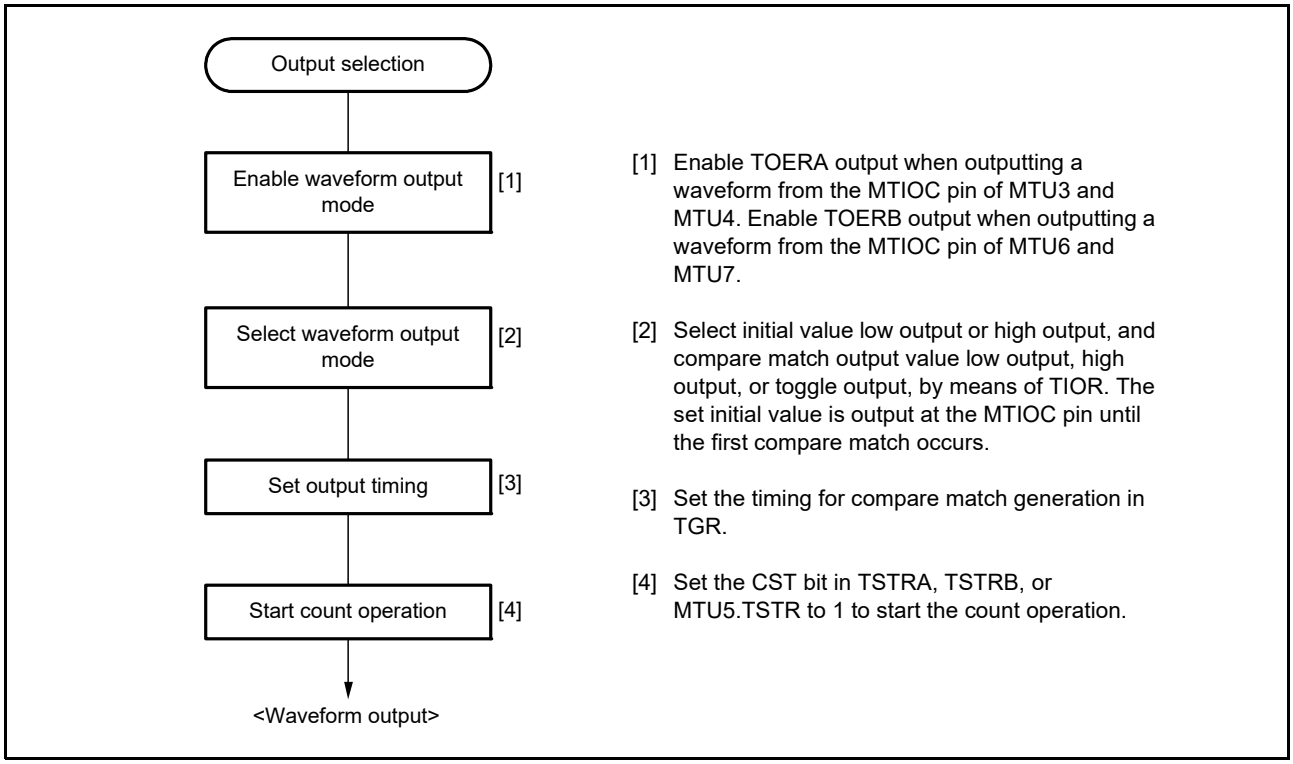


Figure 20.8 Example of Procedure for Setting Waveform Output by Compare Match

(b) Examples of Waveform Output Operation

Figure 20.9 shows an example of low output and high output.
In this example, TCNT has been designated as a free-running counter, and settings have been made so that high is output by compare match A and low is output by compare match B. When the pin level is the same as the specified level, the pin level does not change.

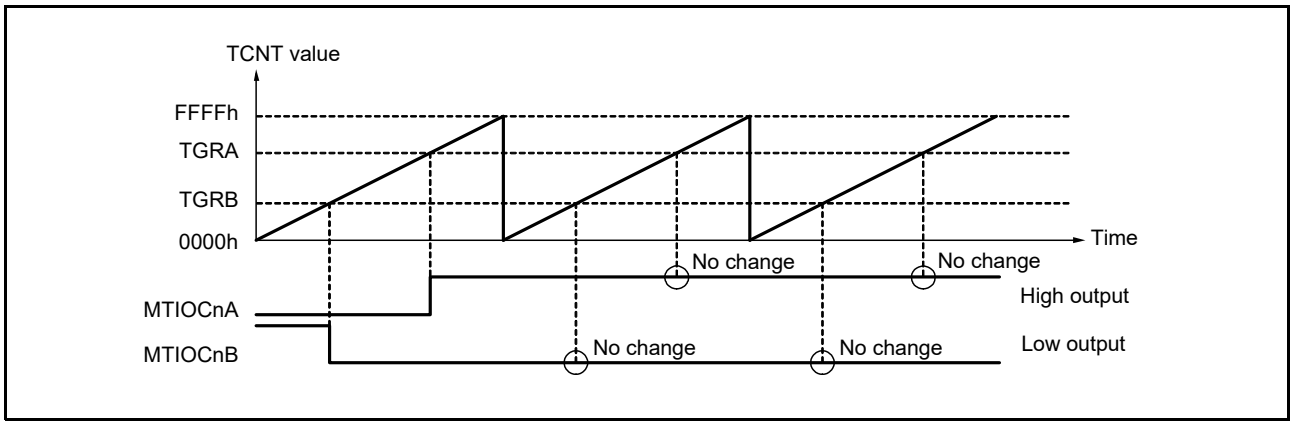


Figure 20.9 Example of low output and high output Operation (n = 0 to 4, 6, 7, 9)

Figure 20.10 shows an example of toggle output.
In this example, TCNT has been designated as a periodic counter (with counter clearing on compare match B), and settings have been made so that the output is toggled by both compare match A and compare match B.

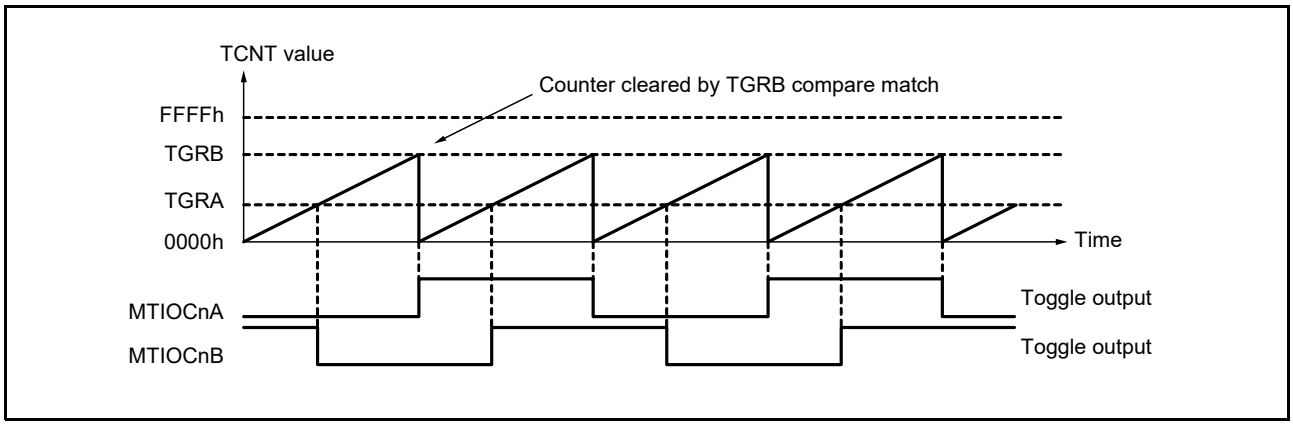


Figure 20.10 Example of Toggle Output Operation (n = 0 to 4, 6, 7, 9)

(3) Input Capture Function

The TCNT value can be transferred to TGR on detection of the MTIOCnm pin (n = 0 to 4, 6, 7, 9; m = A to D) input edge.
The rising edge, falling edge, or both edges can be selected as the detection edge. For MTU0, MTU1, and MTU9, another channel's count clock or compare match signal can also be specified as the input capture source.

Note: When another channel's count clock is used as the input capture input for MTU0, MTU1, and MTU9, PCLKA/1 should not be selected as the count clock used for input capture input. Input capture will not be generated if PCLKA/1 is selected.

(a) Example of Input Capture Operation Setting Procedure

Figure 20.11 shows an example of the input capture operation setting procedure.

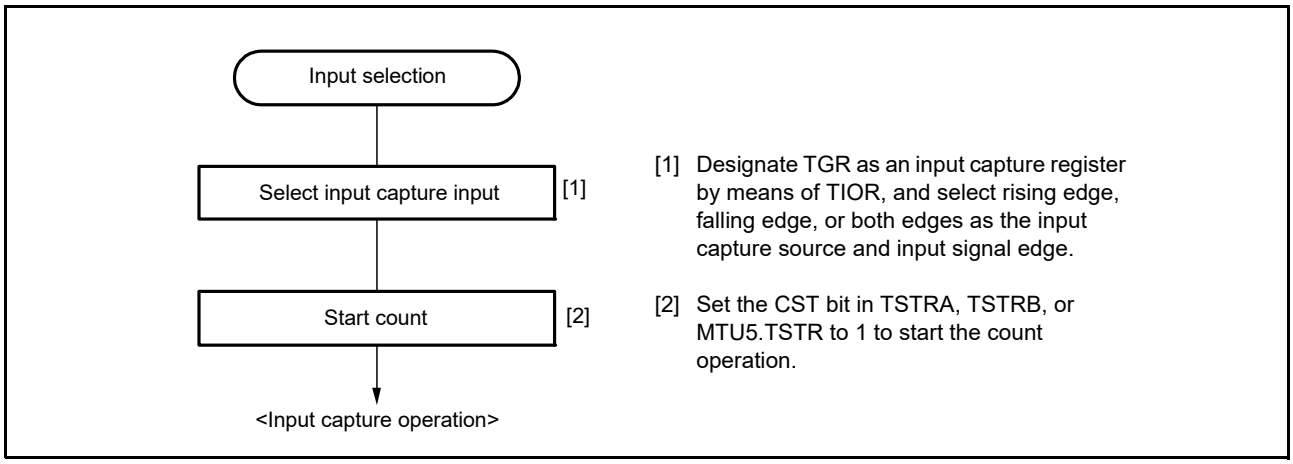


Figure 20.11 Example of Input Capture Operation Setting Procedure

(b) Example of Input Capture Operation

Figure 20.12 shows an example of input capture operation.
In this example, both rising and falling edges have been selected as the MTIOCnA pin input capture input edge, the falling edge has been selected as the MTIOCnB pin input capture input edge, and counter clearing by TGRB input capture has been designated for TCNT. (n = 0 to 4, 6, 7, 9)

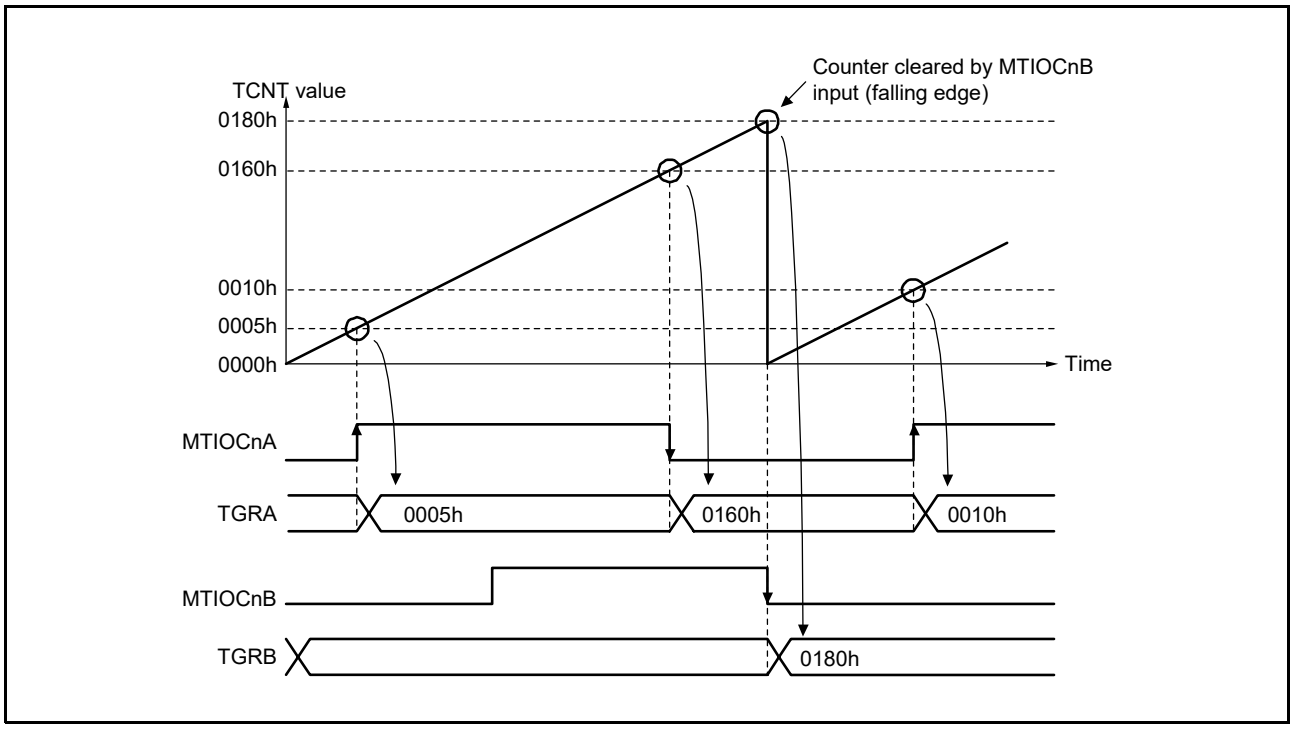


Figure 20.12 Example of Input Capture Operation (n = 0 to 4, 6, 7, 9)

20.3.2 Synchronous Operation

In synchronous operation, the values in multiple TCNT counters can be modified simultaneously (synchronous setting). In addition, multiple TCNT counters can be cleared simultaneously (synchronous clearing) by making the appropriate setting in TCR.
Synchronous operation can increase the number of TGR registers assigned to the same time base.
MTU0 to MTU4, MTU6, MTU7, and MTU9 can all be designated for synchronous operation. MTU5 cannot be used for synchronous operation.

(1) Example of Synchronous Operation Setting Procedure

Figure 20.13 shows an example of the synchronous operation setting procedure.

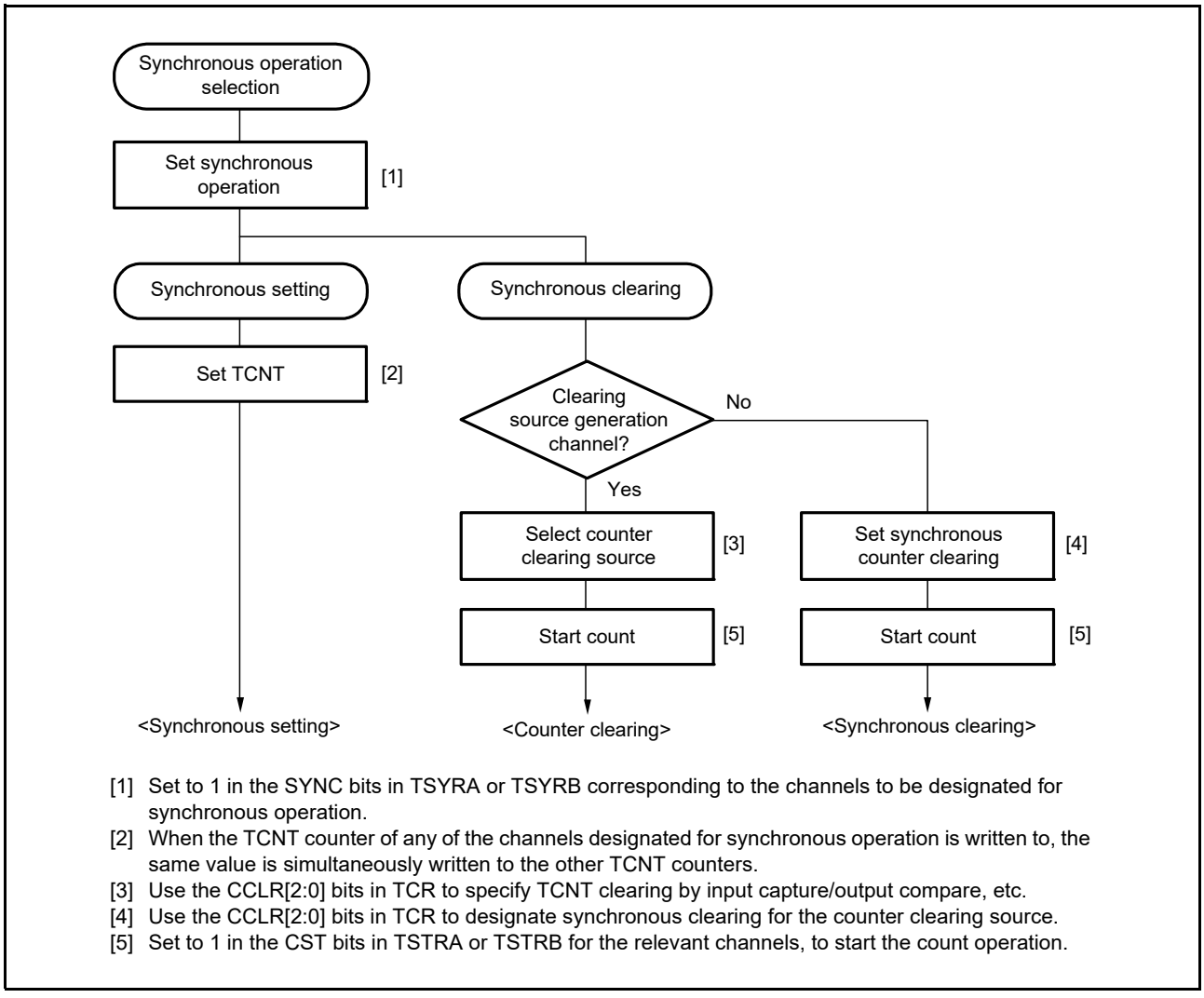


Figure 20.13 Example of Synchronous Operation Setting Procedure

(2) Example of Synchronous Operation

Figure 20.14 shows an example of synchronous operation.
In this example, synchronous operation and PWM mode 1 have been designated for MTU0 to MTU 2, MTU0.TGRB compare match has been set as the counter clearing source in MTU0, and synchronous clearing has been set for the counter clearing source in MTU1 and MTU2.
Three-phase PWM waveforms are output from pins MTIOC0A, MTIOC1A, and MTIOC2A. At this time, synchronous setting and synchronous clearing by MTU0.TGRB compare match are performed for the TCNT counters in MTU0 to MTU2, and the data set in MTU0.TGRB is used as the PWM period.
For details of PWM modes, refer to section 20.3.5, PWM Modes.

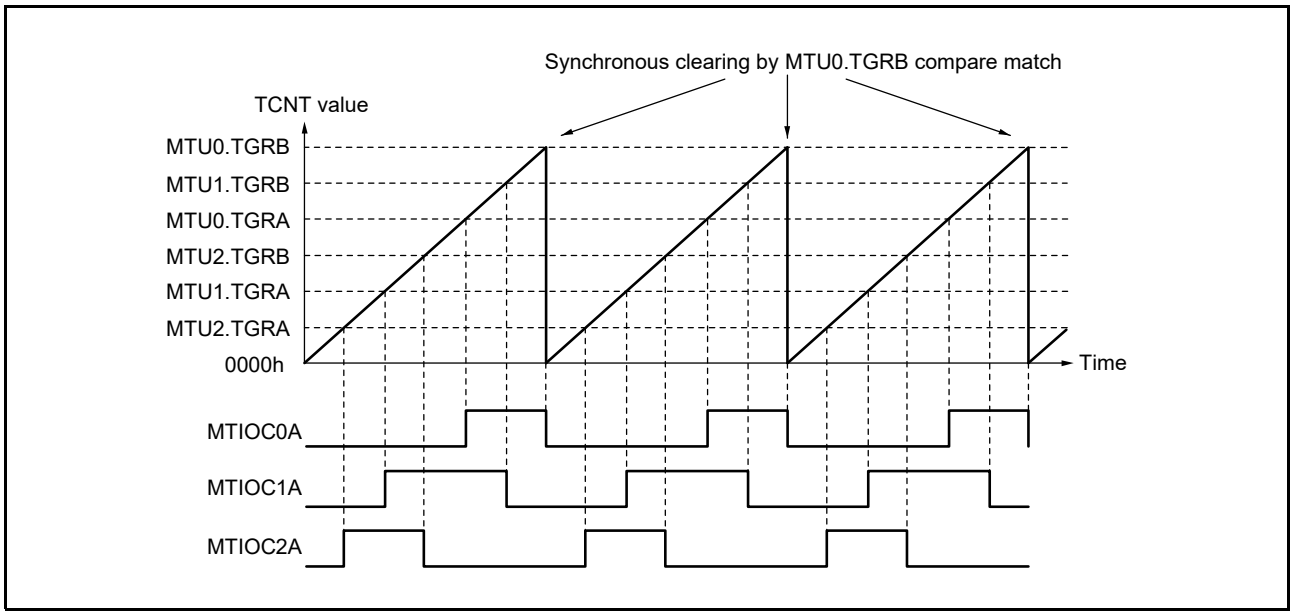


Figure 20.14 Example of Synchronous Operation

20.3.3 Buffer Operation

Buffer operation, provided for MTU0, MTU3, MTU4, MTU6, MTU7, and MTU9, enables TGRC and TGRD to be used as buffer registers. In MTU0 and MTU9, TGRF can also be used as a buffer register.
Buffer operation differs depending on whether TGR has been designated as an input capture register or as a compare match register.

Note: MTU0.TGRE and MTU9.TGRE cannot be designated as an input capture register and can only operate as a compare match register.

Table 20.63 shows the register combinations used in buffer operation.

Table 20.63 Register Combinations in Buffer Operation

Channel	Timer General Register	Buffer Register
MTU0	TGRA	TGRC
	TGRB	TGRD
	TGRE	TGRF
MTU3	TGRA	TGRC
	TGRB	TGRD
MTU4	TGRA	TGRC
	TGRB	TGRD
MTU6	TGRA	TGRC
	TGRB	TGRD
MTU7	TGRA	TGRC
	TGRB	TGRD
MTU9	TGRA	TGRC
	TGRB	TGRD
	TGRE	TGRF

- When TGR is an output compare register

When a compare match occurs, the value in the buffer register for the corresponding channel is transferred to the timer general register.
This operation is illustrated in Figure 20.15.

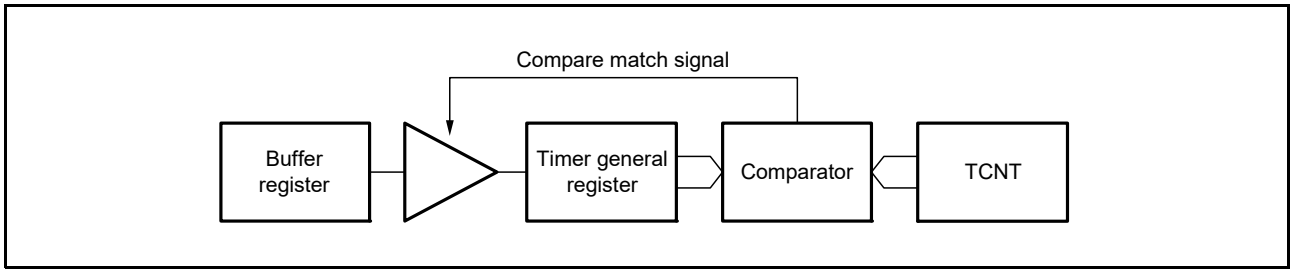


Figure 20.15 Compare Match Buffer Operation

- When TGR is an input capture register

When an input capture occurs, the value in TCNT is transferred to TGR and the value previously held in TGR is transferred to the buffer register.
This operation is illustrated in Figure 20.16.

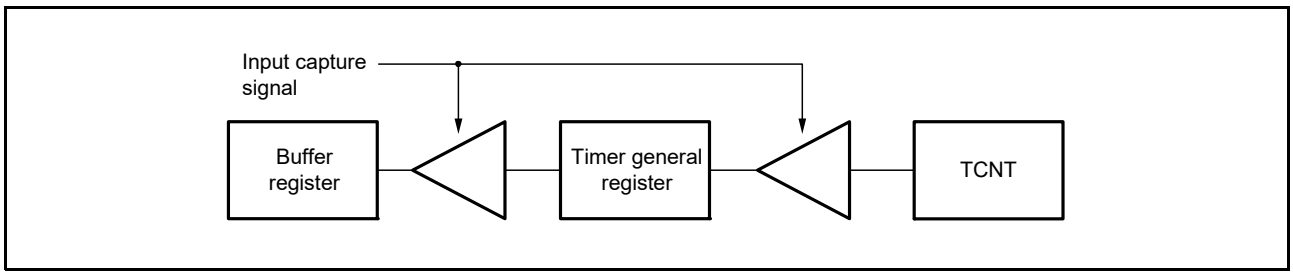


Figure 20.16 Input Capture Buffer Operation

(1) Example of Buffer Operation Setting Procedure

Figure 20.17 shows an example of the buffer operation setting procedure.

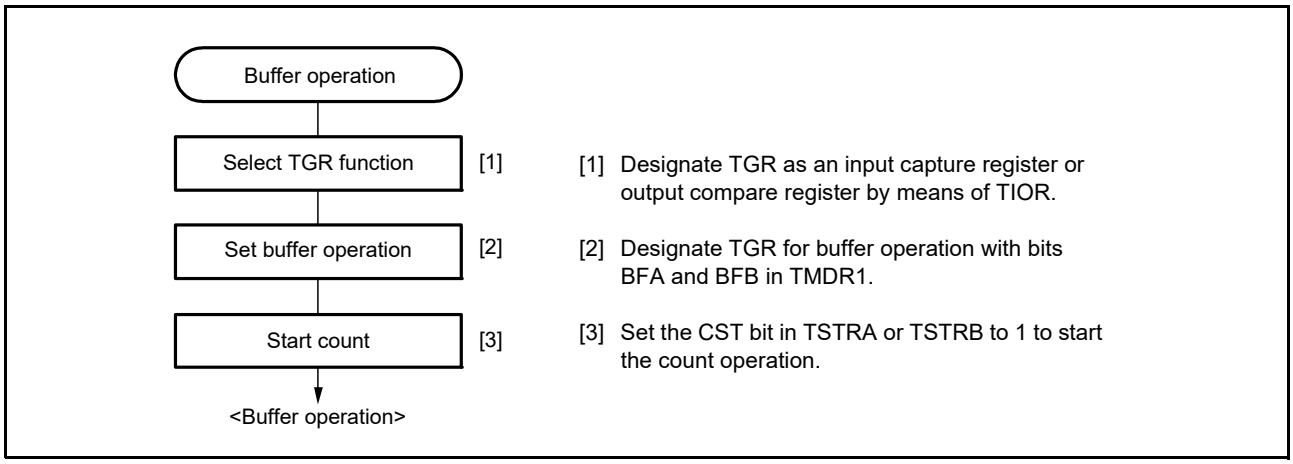


Figure 20.17 Example of Buffer Operation Setting Procedure

(2) Examples of Buffer Operation

(a) When TGR is an Output Compare Register

Figure 20.18 shows an operation example in which PWM mode 1 has been designated for MTU0, and buffer operation has been designated for TGRA and TGRC. The settings used in this example are TCNT clearing by compare match B, high output at compare match A, and low output at compare match B. In this example, the TTSA bit in TBTM is cleared to 0.
As buffer operation has been set, when compare match A occurs, the output changes and the value in buffer register TGRC is simultaneously transferred to timer general register TGRA. This operation is repeated each time compare match A occurs.
For details of PWM modes, refer to section 20.3.5, PWM Modes.

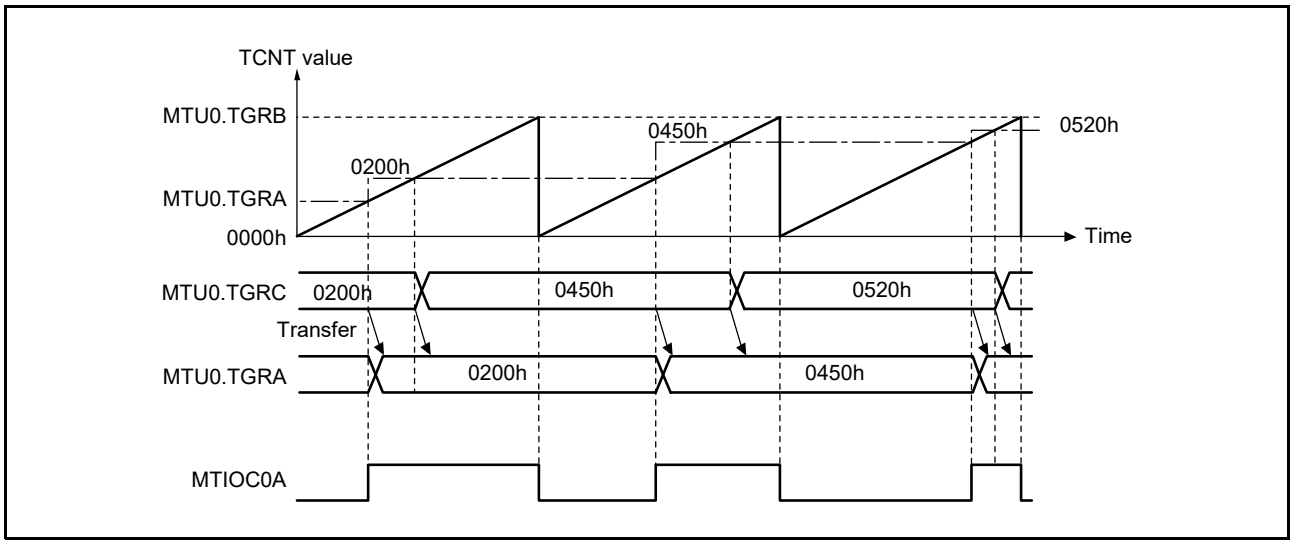


Figure 20.18 Example of Buffer Operation (1)

(b) When TGR is an Input Capture Register

Figure 20.19 shows an operation example in which TGRA has been designated as an input capture register, and buffer operation has been designated for TGRA and TGRC.

Counter clearing by TGRA input capture has been set for TCNT, and both rising and falling edges have been selected as the MTIOCnA pin input capture input edge. (n = 0 to 4, 6, 7, 9)

As buffer operation has been set, when the TCNT value is transferred to TGRA upon occurrence of input capture A, the value previously stored in TGRA is simultaneously transferred to TGRC.

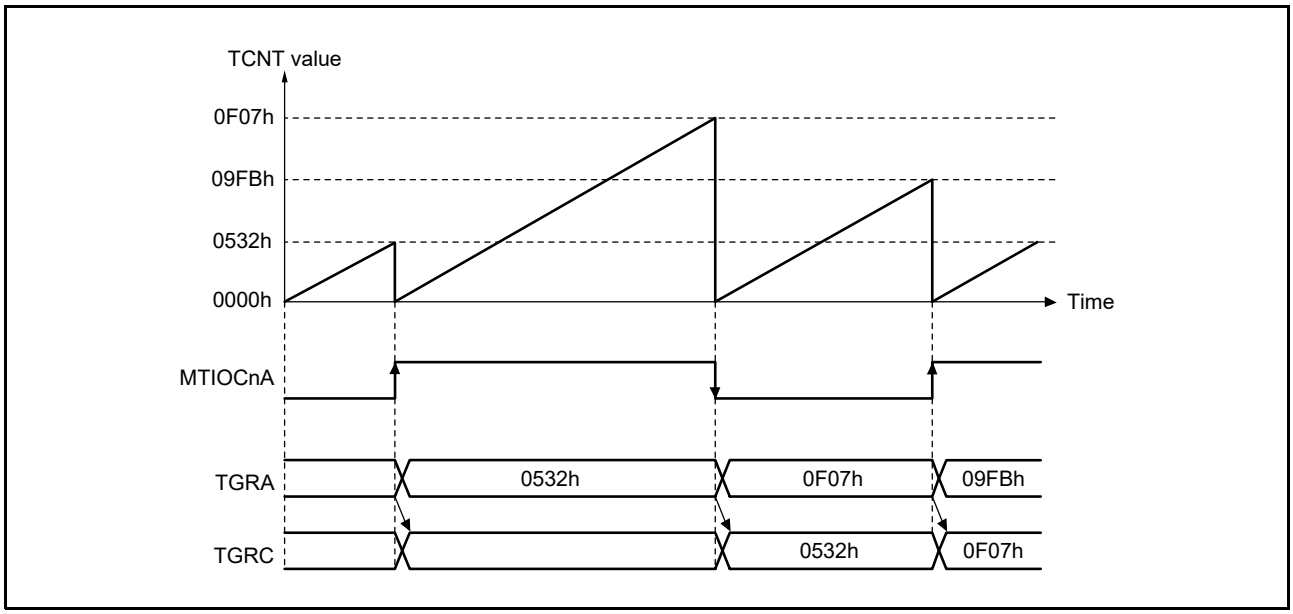


Figure 20.19 Example of Buffer Operation (2) (n = 0 to 4, 6, 7, 9)

(3) Selecting Timing for Transfer from Buffer Registers to Timer General Registers in Buffer Operation

The timing for transfer from buffer registers to timer general registers can be selected in PWM mode 1 or 2 for MTU0 and MTU9 or in PWM mode 1 for MTU3, MTU4, MTU6, and MTU7 by setting the buffer operation transfer mode registers (MTUn.TBTM (n = 0, 3, 4, 6, 7, 9)). Either compare match (value after reset) or TCNT clearing can be selected for the transfer timing. TCNT clearing as transfer timing is one of the following cases.

- When TCNT overflows (FFFFh to 0000h)
- When 0000h is written to TCNT during counting
- When TCNT is cleared to 0000h under the condition specified in the CCLR[2:0] bits in TCR

Note: TBTM must be modified only while TCNT stops.

Figure 20.20 shows an operation example in which PWM mode 1 is designated for MTU0 and buffer operation is designated for MTU0.TGRA and MTU0.TGRC. The settings used in this example are MTU0.TCNT clearing by compare match B, high output at compare match A, and low output at compare match B. The TTSA bit in MTU0.TBTM is set to 1.

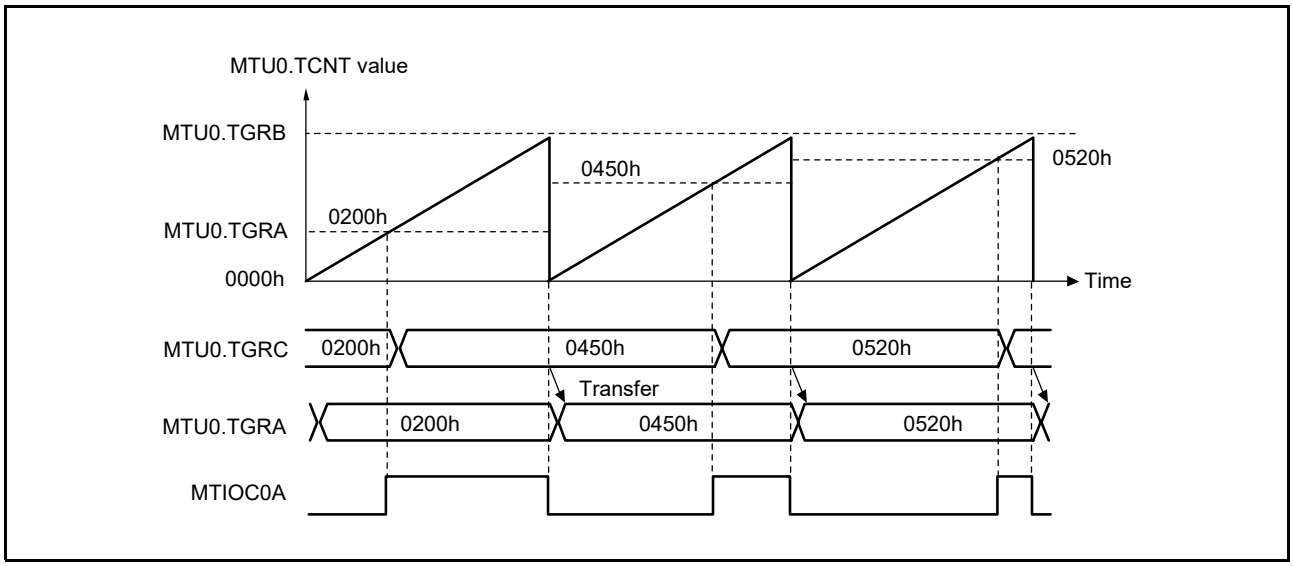


Figure 20.20 Example of Buffer Operation When MTU0.TCNT Clearing is Selected for MTU0.TGRC to MTU0.TGRA Transfer Timing

20.3.4 Cascaded Operation

In cascaded operation, two 16-bit counters in different channels are used together as a 32-bit counter.
There are two functions for connecting MTU1 and MTU2 to use as a 32-bit counter: cascade connection to be set when the MTU1.TMDR3.LWA bit is 0, and cascade connection 32-bit phase counting mode to be set when the MTU1.TMDR3.LWA bit is 1. For details on cascade connection 32-bit phase counting mode, refer to section 20.3.6.2, Cascade Connection 32-Bit Phase Counting Mode. This section describes the cascade connection function to be set when the MTU1.TMDR3.LWA bit is 0.
This function operates when the MTU1.TMDR3.LWA bit is set to 0 and the MTU1.TCR.TPSC[2:0] bits are set so that MTU1.TCNT counts at an overflow/underflow of MTU2.TCNT. Underflow occurs only when the MTU2 to which the lower 16 bits allocated is in phase counting mode.
Table 20.64 shows the register combinations used in cascaded operation.

Note: When phase counting mode is set for MTU1, the count clock setting is invalid and the counters operate independently in phase counting mode.

Table 20.64 Cascaded Combinations

Combination	Upper 16 Bits	Lower 16 Bits
MTU1 and MTU2	MTU1.TCNT	MTU2.TCNT

For simultaneous input capture of MTU1.TCNT and MTU2.TCNT during cascaded operation, additional input capture input pins can be specified by the input capture control register (TICCR). The input-capture condition is of edges in the signal produced by taking the logical OR of the input level on the main input pin and the input level on the added input pin. Accordingly, if either is at the high level, a change in the level of the other will not produce an edge for detection. For details, refer to (4), Cascaded Operation Example (c). For input capture in cascade connection, refer to section 20.6.21, Simultaneous Input Capture in MTU1.TCNT and MTU2.TCNT in Cascade Connection.
Table 20.65 shows the TICCR setting and input capture input pins.

Table 20.65 TICCR Setting and Input Capture Input Pins

Target Input Capture	TICCR Setting	Input Capture Input Pin
Input capture from MTU1.TCNT to MTU1.TGRA	I2AE bit = 0 (Initial value)	MTIOC1A
	I2AE bit = 1	MTIOC1A, MTIOC2A
Input capture from MTU1.TCNT to MTU1.TGRB	I2BE bit = 0 (Initial value)	MTIOC1B
	I2BE bit = 1	MTIOC1B, MTIOC2B
Input capture from MTU2.TCNT to MTU2.TGRA	I1AE bit = 0 (Initial value)	MTIOC2A
	I1AE bit = 1	MTIOC2A, MTIOC1A
Input capture from MTU2.TCNT to MTU2.TGRB	I1BE bit = 0 (Initial value)	MTIOC2B
	I1BE bit = 1	MTIOC2B, MTIOC1B

(1) Example of Cascaded Operation Setting Procedure

Figure 20.21 shows an example of the cascaded operation setting procedure.

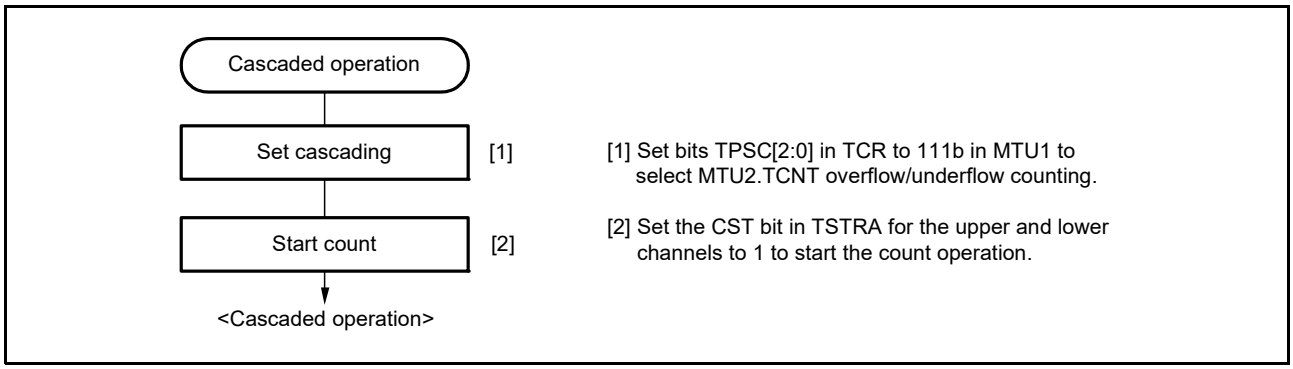


Figure 20.21 Cascaded Operation Setting Procedure

(2) Cascaded Operation Example (a)

Figure 20.22 shows the operation when MTU1.TCNT is set for counting at MTU2.TCNT overflow/underflow and MTU2 is set for phase counting mode 1 while MTU1.TCNT and MTU2.TCNT are cascaded.
MTU1.TCNT is incremented by MTU2.TCNT overflow and decremented by MTU2.TCNT underflow.

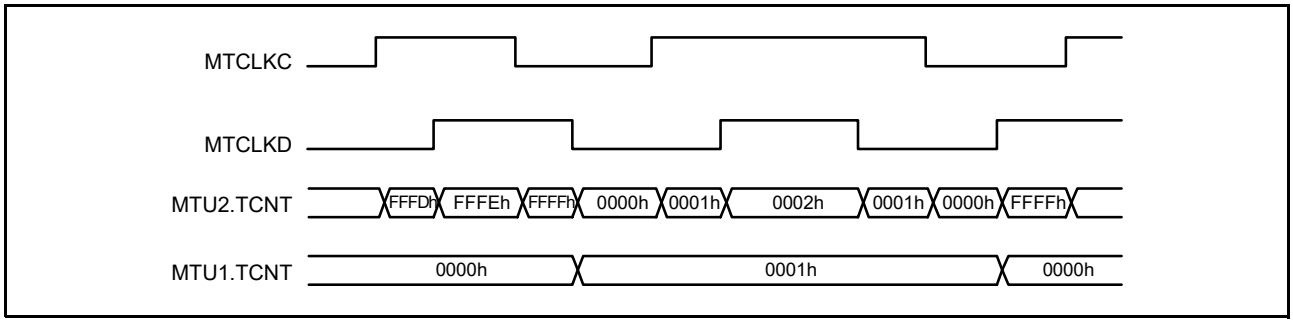


Figure 20.22 Cascaded Operation Example (a)

(3) Cascaded Operation Example (b)

Figure 20.23 illustrates the operation when MTU1.TCNT and MTU2.TCNT have been cascaded and the I2AE bit in TICCR has been set to 1 to include the MTIOC2A pin in the MTU1.TGRA input capture conditions. In this example, the MTU1.TIOR.IOA[3:0] bits have selected the MTIOC1A rising edge for the input capture timing while the MTU2.TIOR.IOA[3:0] bits have selected the MTIOC2A rising edge for the input capture timing.
Under these conditions, the rising edge of both MTIOC1A and MTIOC2A is used for the MTU1.TGRA input capture condition. For the MTU2.TGRA input capture condition, the MTIOC2A rising edge is used.

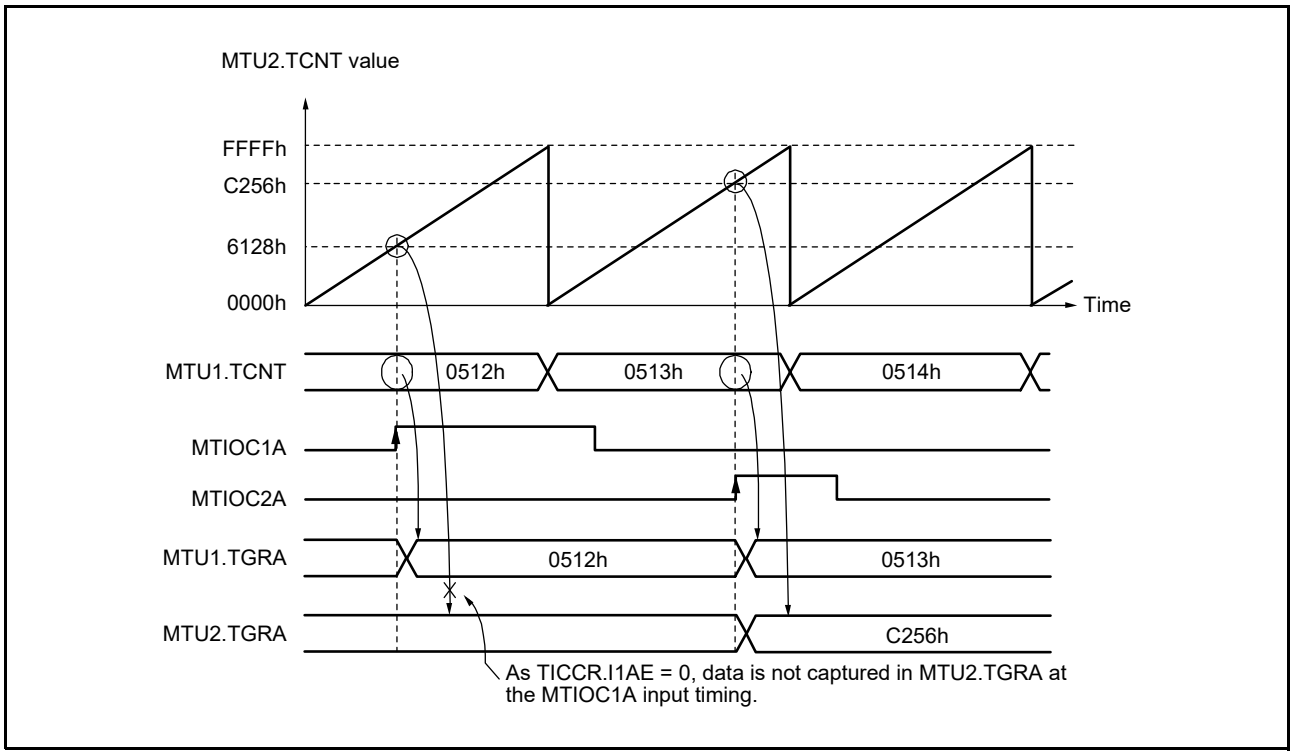
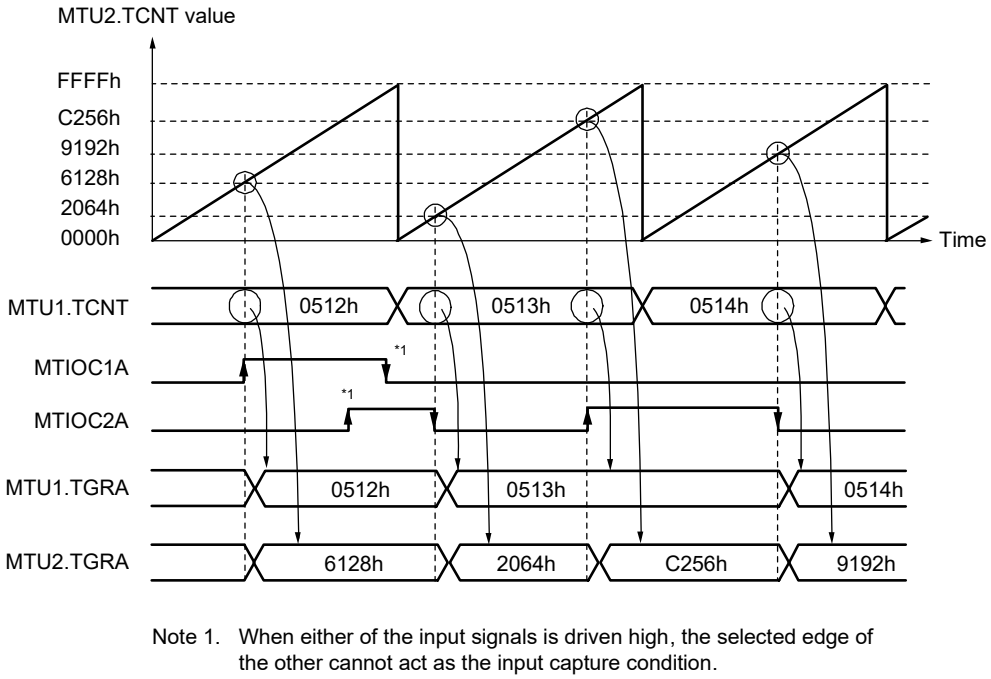


Figure 20.23 Cascaded Operation Example (b)

(4) Cascaded Operation Example (c)

Figure 20.24 illustrates the operation when MTU1.TCNT and MTU2.TCNT have been cascaded and the TICCR.I2AE and I1AE bits have been set to 1 to include the MTIOC2A and MTIOC1A pins in the MTU1.TGRA and MTU2.TGRA input capture conditions, respectively. In this example, the IOA[3:0] bits in both MTU1.TIOR and MTU2.TIOR have selected both the rising and falling edges for the input capture timing. Under these conditions, the ORed result of MTIOC1A and MTIOC2A input is used for the MTU1.TGRA and MTU2.TGRA input capture conditions.



Note 1. When either of the input signals is driven high, the selected edge of the other cannot act as the input capture condition.

Figure 20.24 Cascaded Operation Example (c)

(5) Cascaded Operation Example (d)

Figure 20.25 illustrates the operation when MTU1.TCNT and MTU2.TCNT have been cascaded and the TICCR.I2AE bit has been set to 1 to include the MTIOC2A pin in the MTU1.TGRA input capture conditions. In this example, the IOA[3:0] bits in MTU1.TIOR have selected occurrence of MTU0.TGRA compare match or input capture for the input capture timing while the IOA[3:0] bits in MTU2.TIOR have selected the MTIOC2A rising edge for the input capture timing.

Under these conditions, as MTU1.TIOR has selected occurrence of MTU0.TGRA compare match or input capture for the input capture timing, the MTIOC2A edge is not used for MTU1.TGRA input capture condition although the I2AE bit in TICCR has been set to 1.

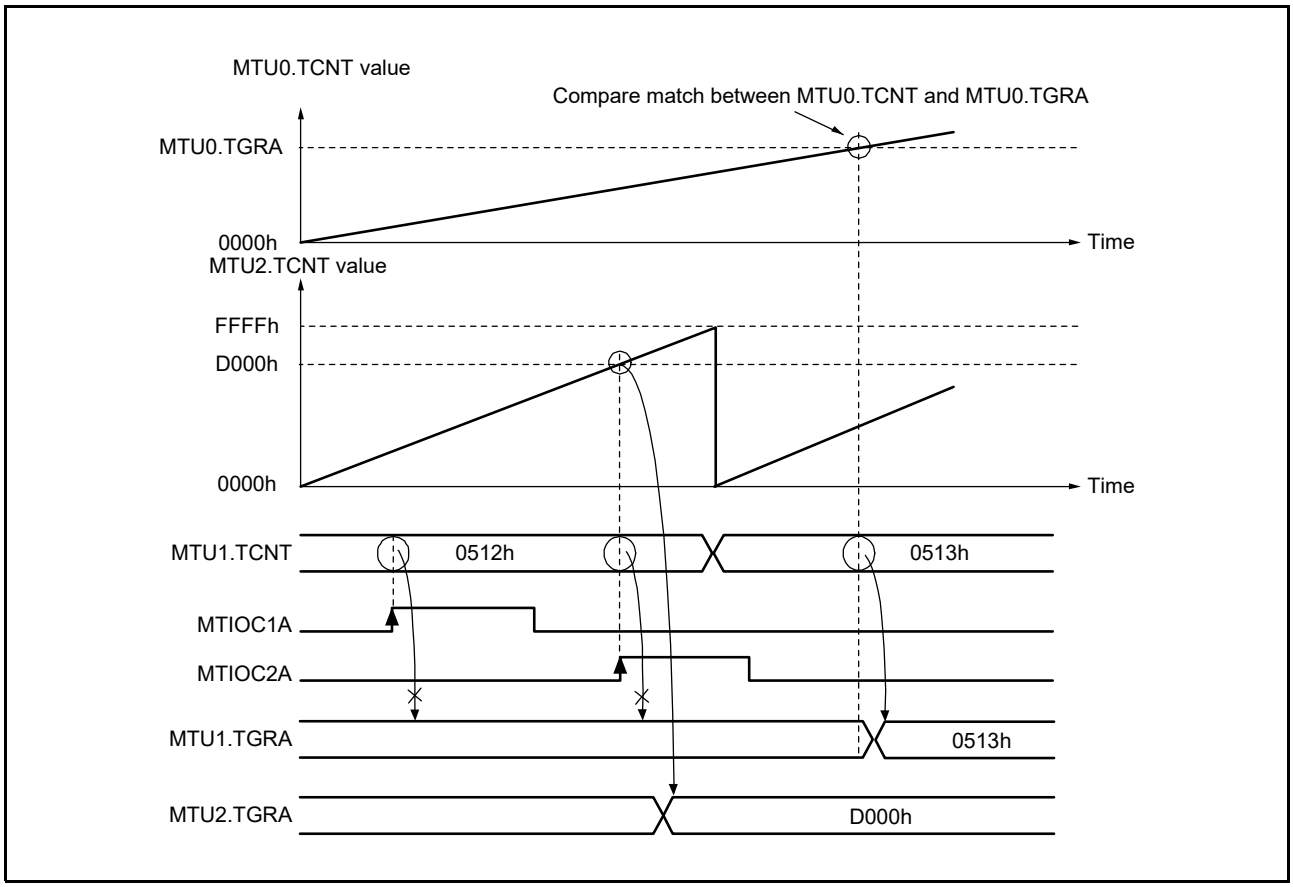


Figure 20.25 Cascaded Operation Example (d)

20.3.5 PWM Modes

PWM modes are provided to output PWM waveforms from the external pins. The output level can be selected as low, high, or toggle output in response to a compare match of each TGR.
PWM waveforms in the range of 0% to 100% duty cycle can be output according to the TGR settings.
By designating TGR compare match as the counter clearing source, the PWM period can be specified in that register.
Every channel except MTU5 can be set to PWM mode independently. Channels set to PWM mode can perform synchronous operation with each other or other channels set to any other mode.
There are two PWM modes as described below.

(a) PWM Mode 1

PWM waveforms are output from the MTIOCnA and MTIOCnC pins by pairing TGRA with TGRB and TGRC with TGRD. The levels specified by the TIOR.IOA[3:0] and IOC[3:0] bits are output from the MTIOCnA and MTIOCnC pins at compare matches A and C, and the level specified by the TIOR.IOB[3:0] and IOD[3:0] bits are output at compare matches B and D (n = 0 to 4, 6, 7, 9). The initial output value is set in TGRA or TGRC. If the values set in paired TGRs are identical, the output value does not change even when a compare match occurs.
In PWM mode 1, PWM waveforms in up to 14 phases can be output.

(b) PWM Mode 2

PWM waveform output is generated using one TGR as the period register and the others as duty registers. The level specified in TIOR is output at compare matches. Upon counter clearing by a period register compare match, the initial value set in TIOR is output from each pin. If the values set in the period and duty registers are identical, the output value does not change even when a compare match occurs.

Up to 12 phases of PWM waveforms can be output by combining synchronous clearing of channels that cannot be set to PWM mode 2 as synchronous operation.

The correspondence between PWM output pins and registers is shown in Table 20.66.

Table 20.66 PWM Output Registers and Output Pins

		Output Pins	
Channel	**Register**	**PWM Mode 1**	**PWM Mode 2**
MTU0	TGRA	MTIOC0A	MTIOC0A
	TGRB		MTIOC0B
	TGRC	MTIOC0C	MTIOC0C
	TGRD		MTIOC0D
MTU1	TGRA	MTIOC1A	MTIOC1A
	TGRB		MTIOC1B
MTU2	TGRA	MTIOC2A	MTIOC2A
	TGRB		MTIOC2B
MTU3	TGRA	MTIOC3A	Setting prohibited
	TGRB		
	TGRC	MTIOC3C	
	TGRD		
MTU4	TGRA	MTIOC4A	
	TGRB		
	TGRC	MTIOC4C	
	TGRD		
MTU6	TGRA	MTIOC6A	
	TGRB		
	TGRC	MTIOC6C	
	TGRD		
MTU7	TGRA	MTIOC7A	
	TGRB		
	TGRC	MTIOC7C	
	TGRD		
MTU9	TGRA	MTIOC9A	MTIOC9A
	TGRB		MTIOC9B
	TGRC	MTIOC9C	MTIOC9C
	TGRD		MTIOC9D

Note: In PWM mode 2, PWM waveform output is not possible for the TGR register in which the PWM period is set.

(1) Example of PWM Mode Setting Procedure

Figure 20.26 shows an example of the PWM mode setting procedure.

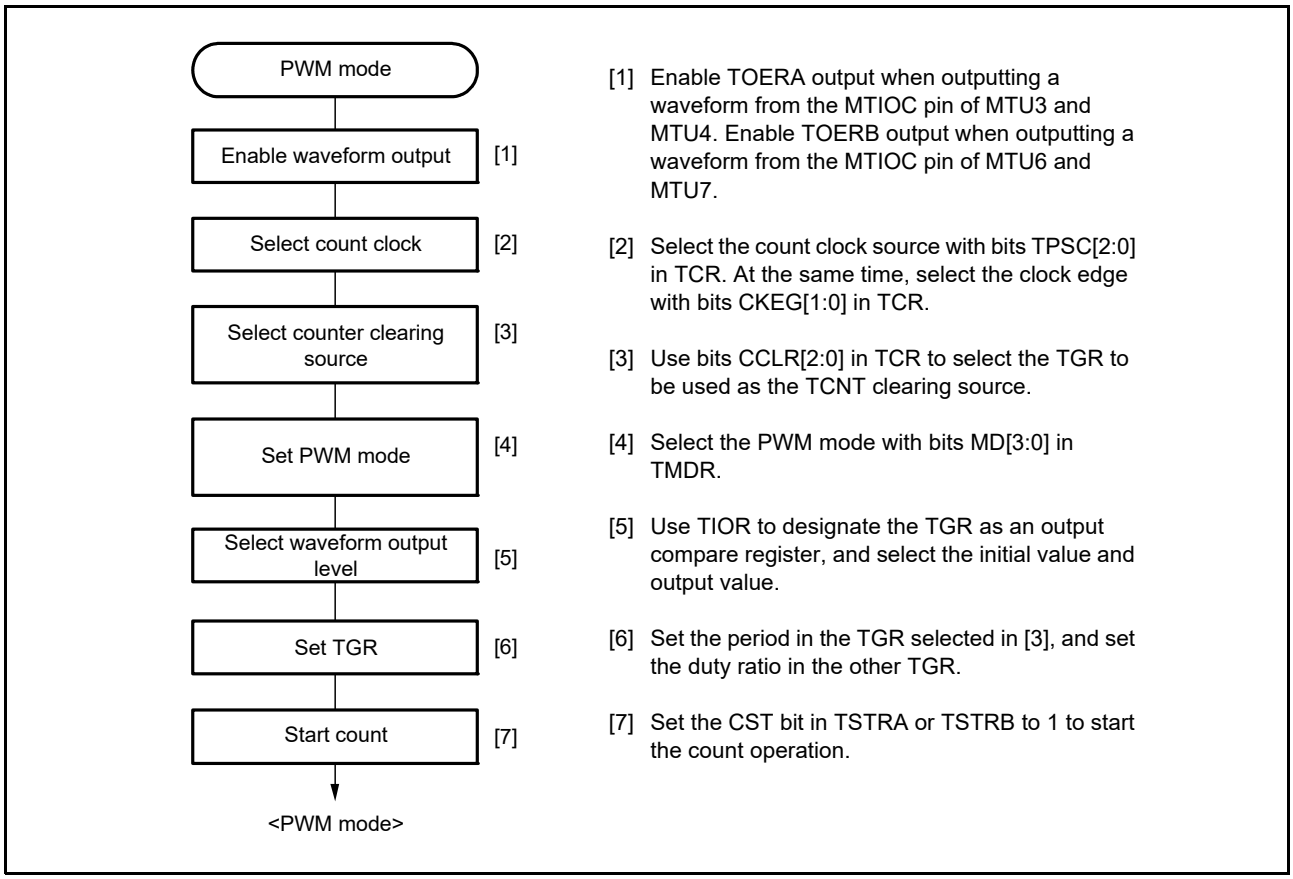


Figure 20.26 Example of PWM Mode Setting Procedure

(2) Examples of PWM Mode Operation

Figure 20.27 shows an example of operation in PWM mode 1.

In this example, TGRA compare match is set as the TCNT clearing source, 0 is set as the initial output value and output value for TGRA, and 1 is set as the output value for TGRB.

In this case, the value set in TGRA is used as the period, and the value set in TGRB is used as the duty ratio.

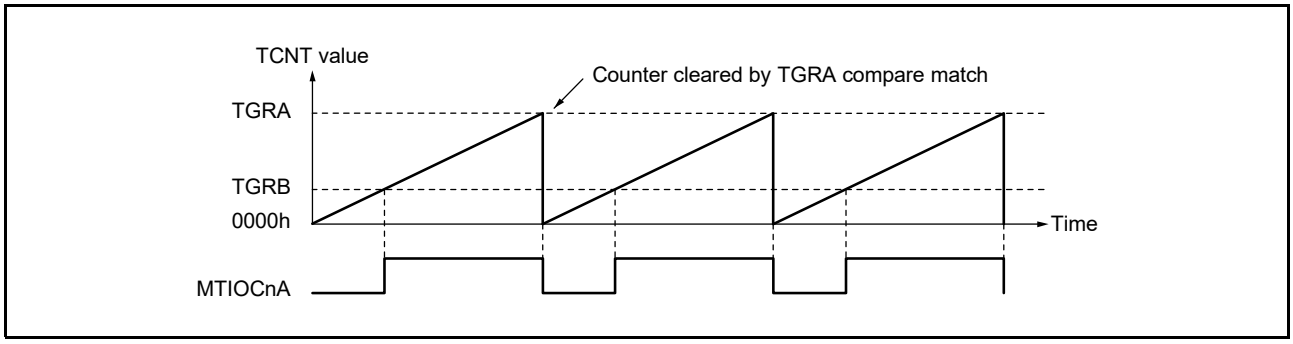


Figure 20.27 Example of PWM Mode 1 Operation (n = 0 to 4, 6, 7, 9)

Figure 20.28 shows an example of operation in PWM mode 2.
In this example, synchronous operation is designated for MTU0 and MTU1, MTU1.TGRB compare match is set as the TCNT clearing source, and low is set as the initial output value and high as the output value for the other TGR registers (MTU0.TGRA to MTU0.TGRD and MTU1.TGRA), outputting 5-phase PWM waveforms.
In this case, the value set in MTU1.TGRB is used as the period, and the values set in the other TGRs are used as the duty ratio.

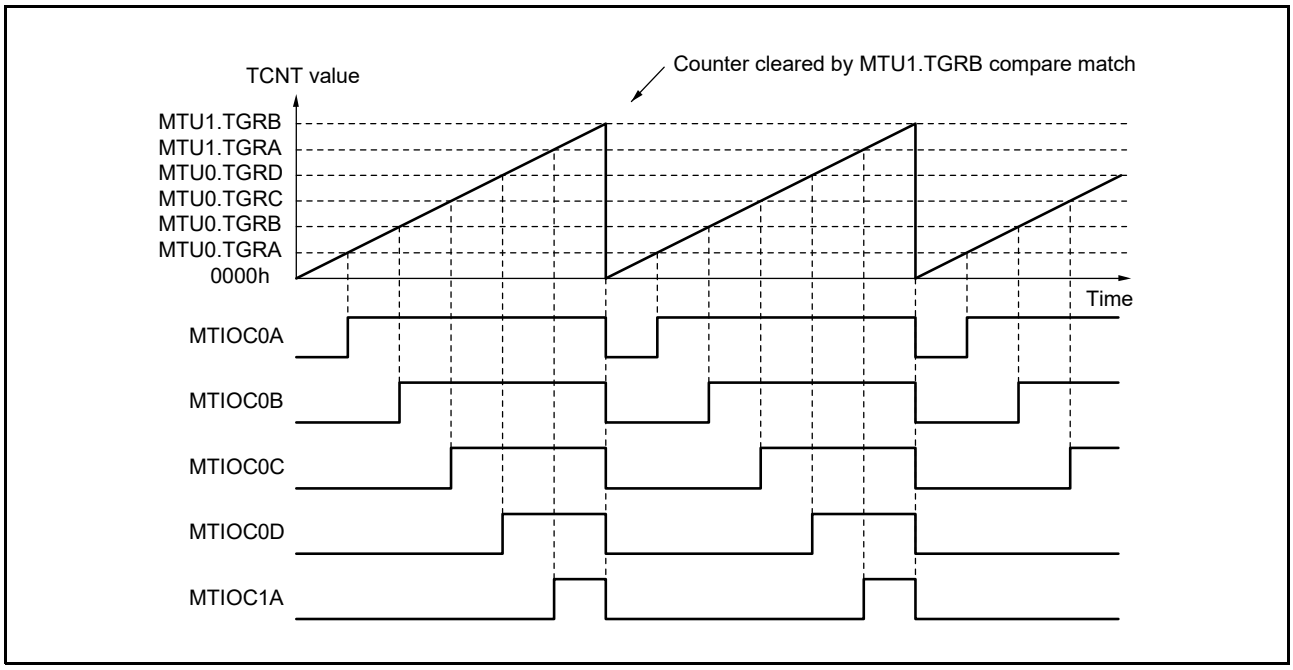


Figure 20.28 Example of PWM Mode 2 Operation

Figure 20.29 shows examples of PWM waveform output with 0% duty and 100% duty in PWM mode 1.
In this example, TGRA compare match is set as the TCNT clearing source, a low level is set as the initial output value and output value for TGRA, and a high level is set as the output value for TGRB.

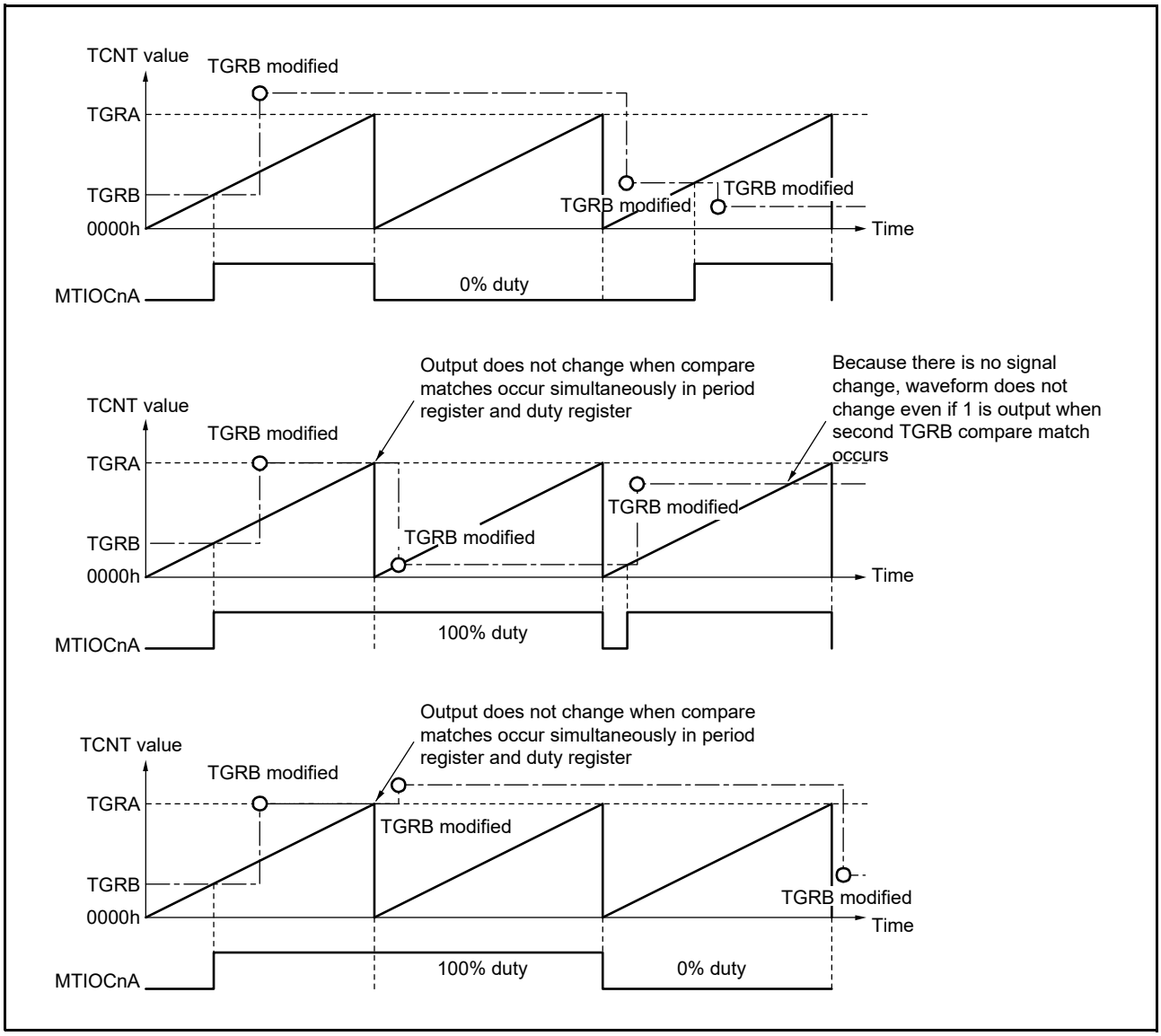


Figure 20.29 Examples of PWM Mode Operation (PWM Waveform Output with 0% Duty and 100% Duty) (n = 0 to 4, 6, 7, 9)

20.3.6 Phase Counting Mode

There are two phase counting modes: 16-bit phase counting mode in which MTU1 and MTU2 operate independently, and cascade connection 32-bit phase counting mode in which MTU1 and MTU2 are cascaded.
In phase counting mode, the phase difference between two external input clocks is detected and the corresponding TCNT is incremented or decremented.
Two external clock input pins for each phase counting mode are not affected by the settings of TCR.TPSC[2:0], TCR2.TPSC2[2:0], and CKEG[1:0]. The two external clock input pins used in 16-bit phase counting mode and cascade connection 32-bit phase counting mode of MTU2 can be selected by MTU1.TMDR3.PHCKSEL. In a phase counting mode other than 16-bit phase counting mode and cascade connection 32-bit phase counting mode of MTU2, MTCLKA and MTCLKB are selected for A-phase and B-phase, respectively. In phase counting mode, the external clock pins MTCLKA, MTCLKB, MTCLKC, and MTCLKD are used for two-phase encoder pulse input.
Table 20.67 lists the external clock input pins to be connected in each phase counting mode.

Table 20.67 Clock Input Pins in Phase Counting Mode

		External Clock Input Pins	
Phase Counting Mode	**TMDR3.PHCKSEL bit**	**A-Phase**	**B-Phase**
MTU1 16-bit phase counting mode	x (Don't care)	MTCLKA	MTCLKB
MTU2 16-bit phase counting mode	0	MTCLKA	MTCLKB
	1 (initial value)	MTCLKC	MTCLKD
Cascade connection 32-bit phase counting mode	0	MTCLKA	MTCLKB
	1 (initial value)	MTCLKC	MTCLKD

20.3.6.1 16-Bit Phase Counting Mode

When the MTU1.TMDR3.LWA is 0, 16-bit phase counting mode can be set individually for MTU1 and MTU2.
In 16-bit phase counting mode, the phase difference between two external input clocks is detected and the 16-bit counter TCNT of the corresponding channel is incremented or decremented.
When 16-bit phase counting mode is specified, an external clock is selected as the count clock and TCNT operates as an up-counter/down-counter regardless of the setting of TCR.TPSC[2:0], TCR2.TPSC2[2:0], and CKEG[1:0]. However, the functions of TCR.CCLR[1:0],TIOR, TIER, and TGR are enabled, and input capture/compare match and interrupt functions can be used.
These external input pins can be used for two-phase encoder pulse input.
When an overflow occurs while TCNT is counting up and the corresponding TIER.TCIEV bit is 1, a TCIV interrupt is generated. When an underflow occurs while TCNT is counting down and the corresponding TIER.TCIEU bit is 1, a TCIU interrupt is generated.
The TSR.TCFD flag is the count direction flag. Read the TCFD flag to check whether TCNT is counting up and down.

(1) Example of 16-Bit Phase Counting Mode Setting Procedure

Figure 20.30 shows an example of the phase counting mode setting procedure.

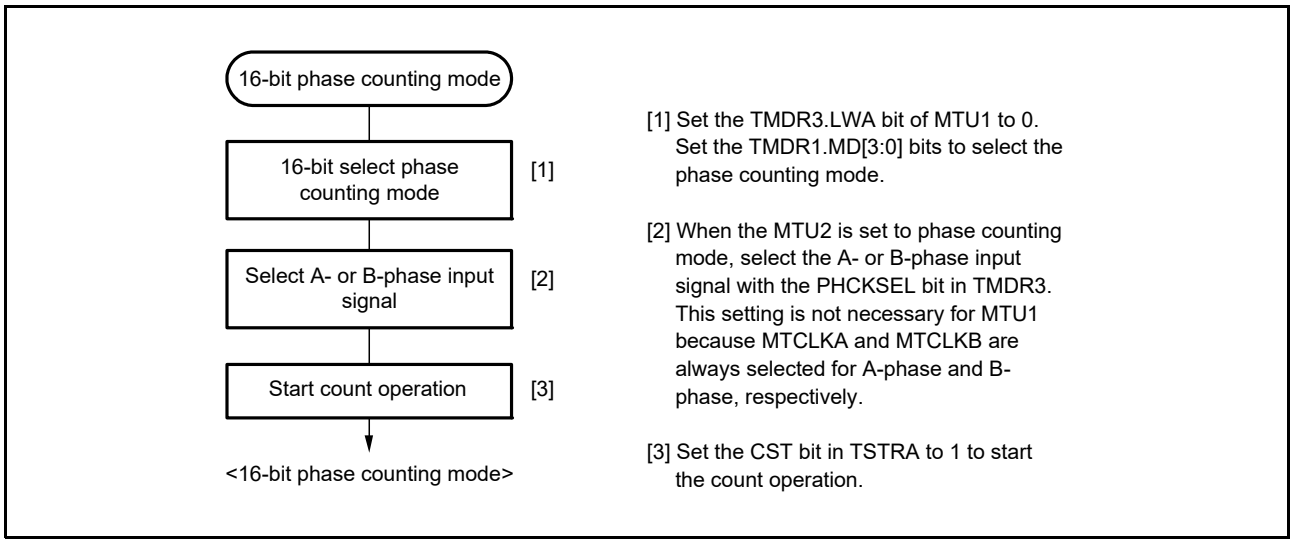


Figure 20.30 Example of 16-Bit Phase Counting Mode Setting Procedure

(2) Examples of 16-Bit Phase Counting Mode Operation

In phase counting mode, TCNT is incremented or decremented according to the phase difference between two external clocks. There are five modes according to the count conditions. Each mode operates under the condition PHCKSEL = 1, which means the phase clock for MTU1 is input from MTCLKA or MTCLKB and that for MTU2 is input from MTCLKC or MTCLKD.

(a) Phase Counting Mode 1

Figure 20.31 shows an example of operation in phase counting mode 1, and Table 20.68 summarizes the TCNT up-counting and down-counting conditions.

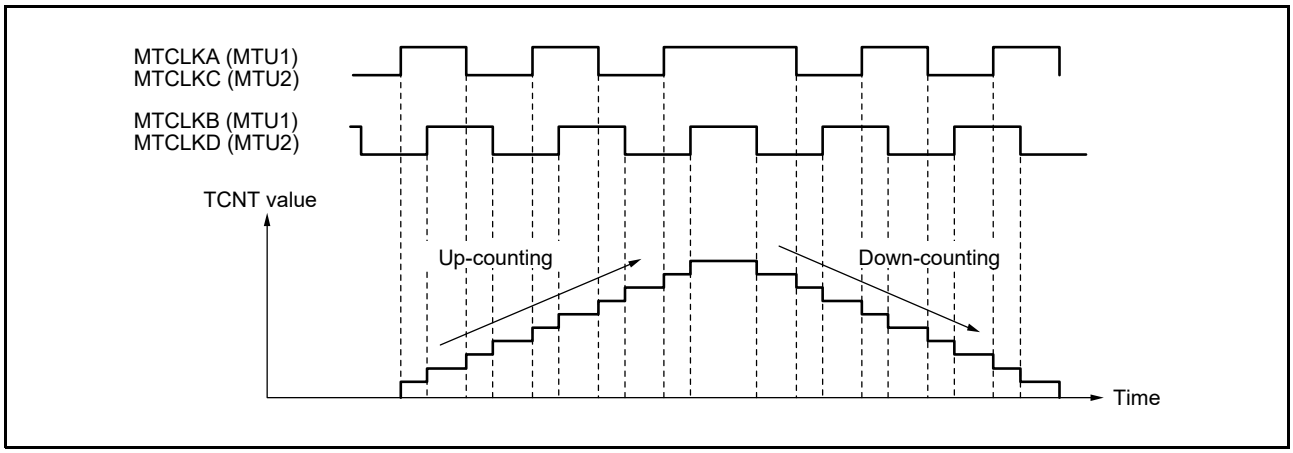


Figure 20.31 Example of Operation in Phase Counting Mode 1

Table 20.68 Up-Counting and Down-Counting Conditions in Phase Counting Mode 1

MTCLKA (MTU1) MTCLKC (MTU2)	MTCLKB (MTU1) MTCLKD (MTU2)	Operation
High	↑	Up-counting
Low	↓	
↑	Low	
↓	High	
High	↓	Down-counting
Low	↑	
↑	High	
↓	Low	

↑ : Rising edge

↓ : Falling edge

(b) Phase Counting Mode 2

Figure 20.32 to Figure 20.34 show the examples of operation in phase counting mode 2 and Table 20.69 summarizes the TCNT up-counting and down-counting conditions.

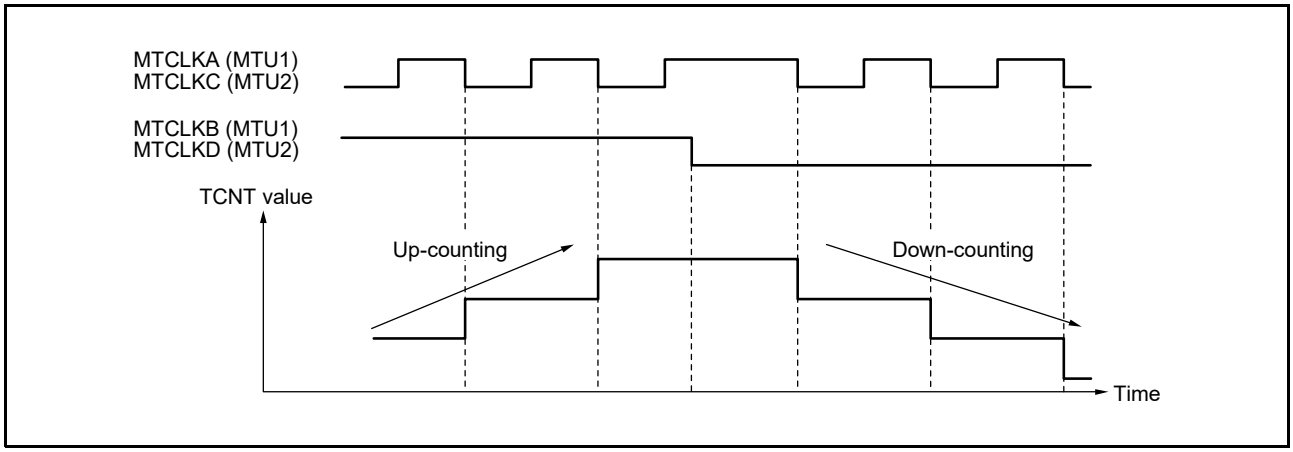


Figure 20.32 Example of Operation in Phase Counting Mode 2 (When MTUn.TCR2.PCB[1:0] = 00b (n = 1, 2))

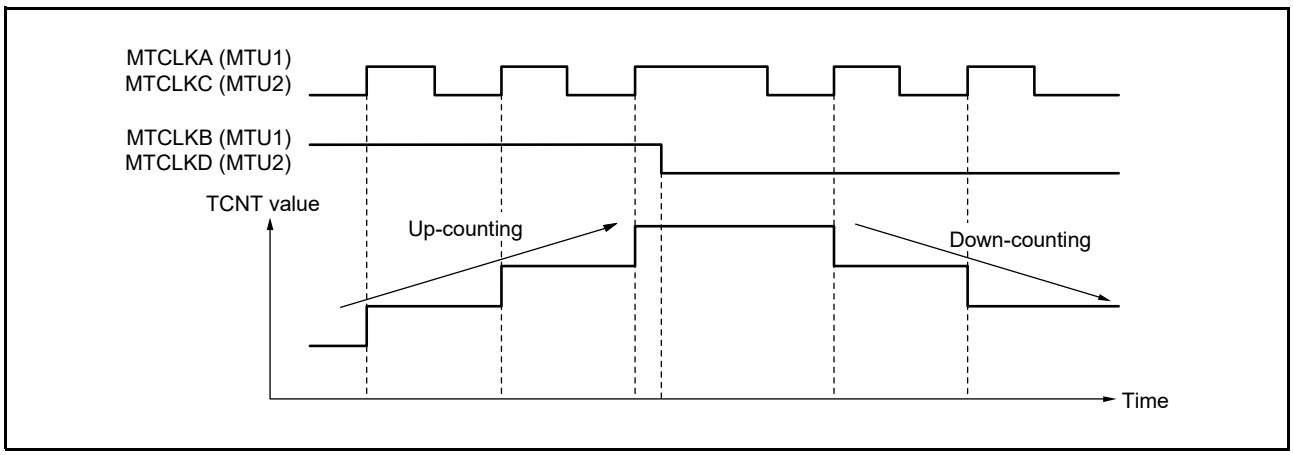


Figure 20.33 Example of Operation in Phase Counting Mode 2 (When MTUn.TCR2.PCB[1:0] = 01b (n = 1, 2))

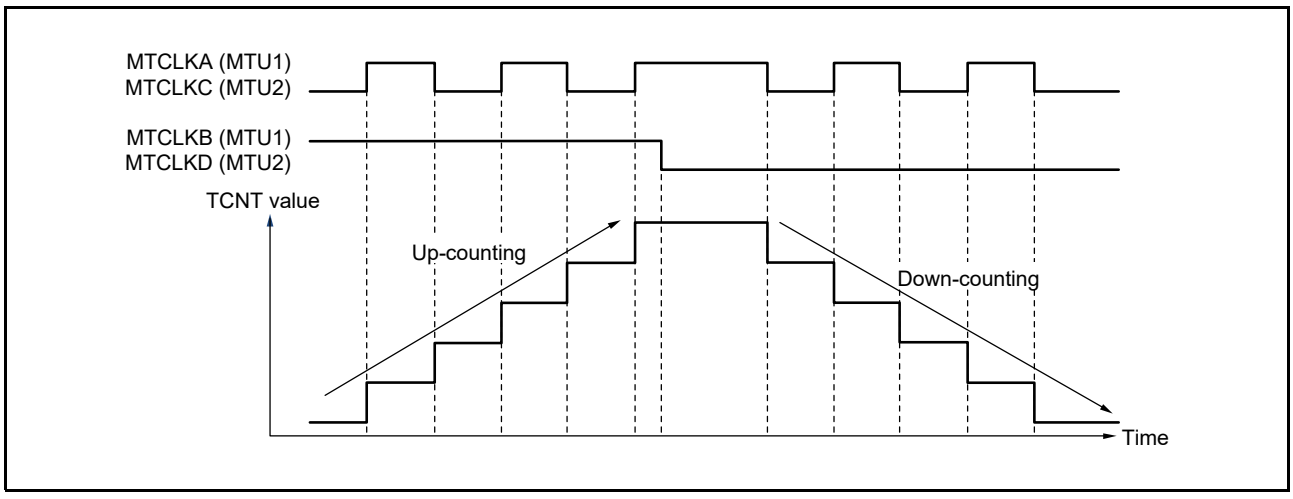


Figure 20.34 Example of Operation in Phase Counting Mode 2 (When MTUn.TCR2.PCB[1:0] = 1xb (n = 1, 2))

Table 20.69 Up-Counting and Down-Counting Conditions in Phase Counting Mode 2

PCB[1:0]	MTCLKA (MTU1) MTCLKC (MTU2)	MTCLKB (MTU1) MTCLKD (MTU2)	Operation
00b	High	↑	Not counted (Don't care)
	Low	↓	
	↑	Low	
	↓	High	Up-counting
	High	↓	Not counted (Don't care)
	Low	↑	
	↑	High	
	↓	Low	Down-counting
01b	High	↑	Not counted (Don't care)
	Low	↓	
	↑	Low	Down-counting
	↓	High	Not counted (Don't care)
	High	↓	
	Low	↑	
	↑	High	Up-counting
	↓	Low	Not counted (Don't care)
1xb	High	↑	Not counted (Don't care)
	Low	↓	
	↑	Low	Down-counting
	↓	High	Up-counting
	High	↓	Not counted (Don't care)
	Low	↑	
	↑	High	Up-counting
	↓	Low	Down-counting

↑ : Rising edge

↓ : Falling edge

(c) Phase Counting Mode 3

Figure 20.35 to Figure 20.37 show the examples of operation in phase counting mode 3 and Table 20.70 summarizes the TCNT up-counting and down-counting conditions.

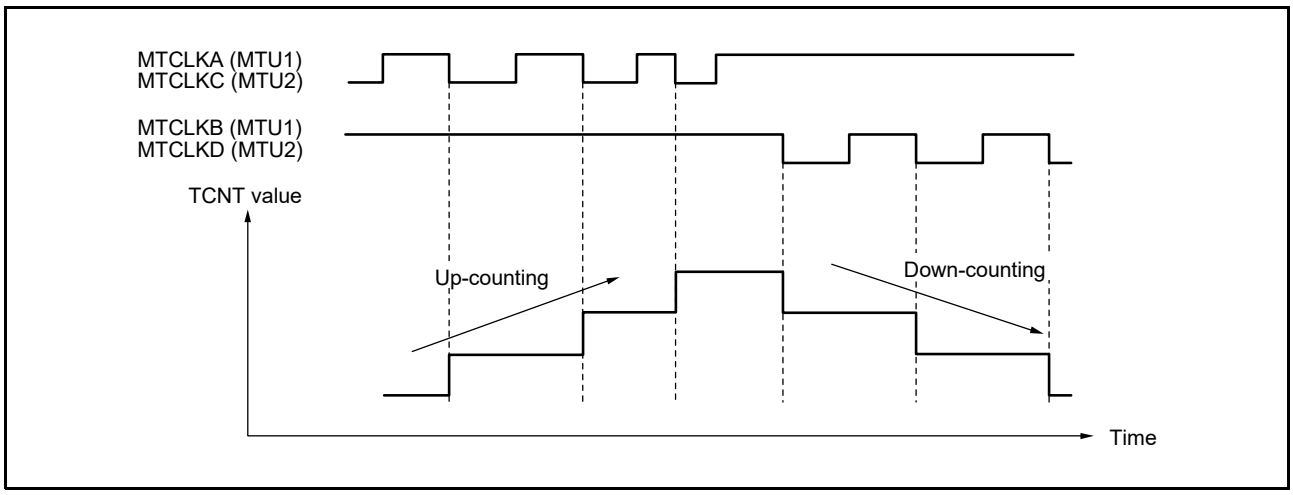


Figure 20.35 Example of Operation in Phase Counting Mode 3 (When MTUn.TCR2.PCB[1:0] = 00b (n = 1, 2))

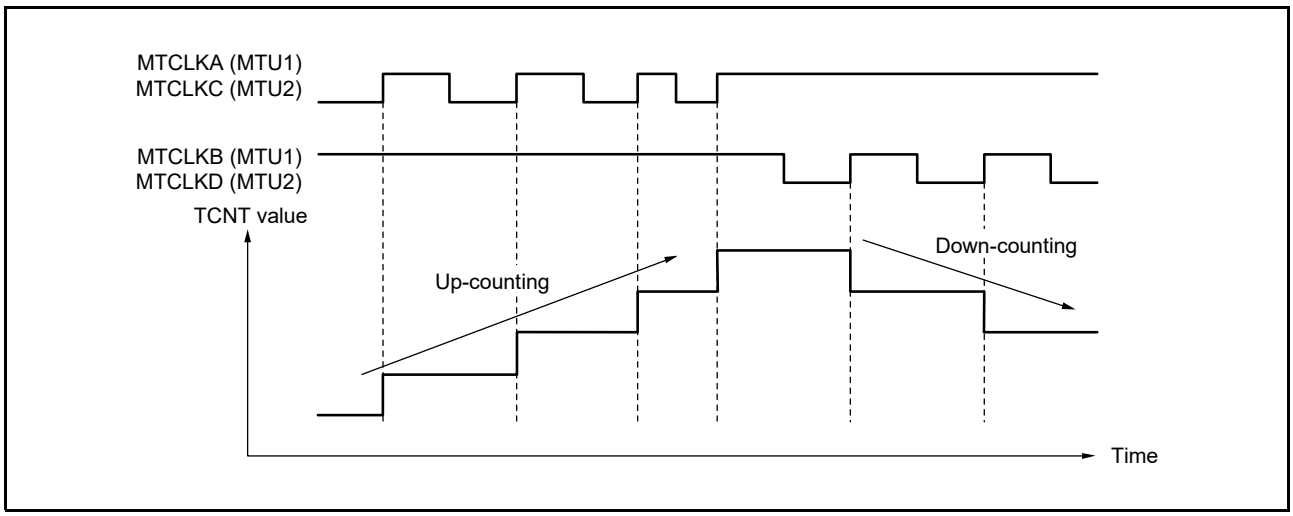


Figure 20.36 Example of Operation in Phase Counting Mode 3 (When MTUn.TCR2.PCB[1:0] = 01b (n = 1, 2))

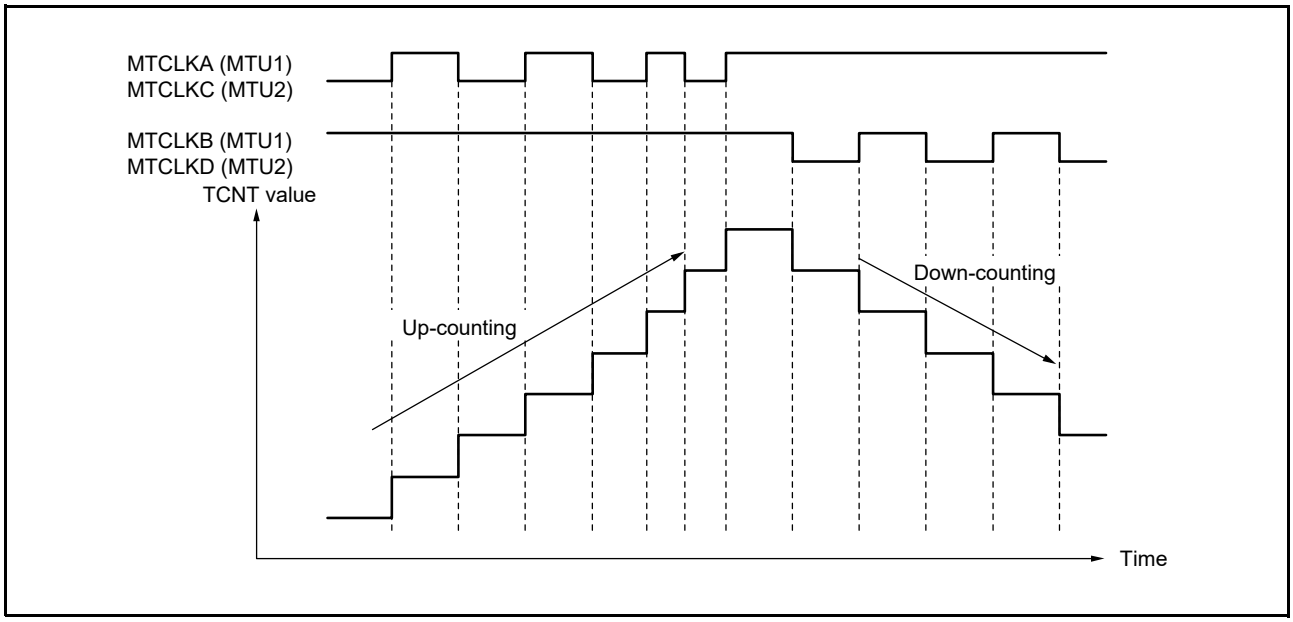


Figure 20.37 Example of Operation in Phase Counting Mode 3 (When MTUn.TCR2.PCB[1:0] = 1xb (n = 1, 2))

Table 20.70 Up-Counting and Down-Counting Conditions in Phase Counting Mode 3

PCB[1:0]	MTCLKA (MTU1) MTCLKC (MTU2)	MTCLKB (MTU1) MTCLKD (MTU2)	Operation
00b	High	↑	Not counted (Don't care)
	Low	↓	
	↑	Low	
	↓	High	Up-counting
	High	↓	Down-counting
	Low	↑	Not counted (Don't care)
	↑	High	
	↓	Low	
01b	High	↑	Down-counting
	Low	↓	Not counted (Don't care)
	↑	Low	
	↓	High	
	High	↓	
	Low	↑	
	↑	High	Up-counting
	↓	Low	Not counted (Don't care)
1xb	High	↑	Down-counting
	Low	↓	Not counted (Don't care)
	↑	Low	
	↓	High	Up-counting
	High	↓	Down-counting
	Low	↑	Not counted (Don't care)
	↑	High	Up-counting
	↓	Low	Not counted (Don't care)

↑ : Rising edge

↓ : Falling edge

(d) Phase Counting Mode 4

Figure 20.38 shows an example of operation in phase counting mode 4, and Table 20.71 summarizes the TCNT up-counting and down-counting conditions.

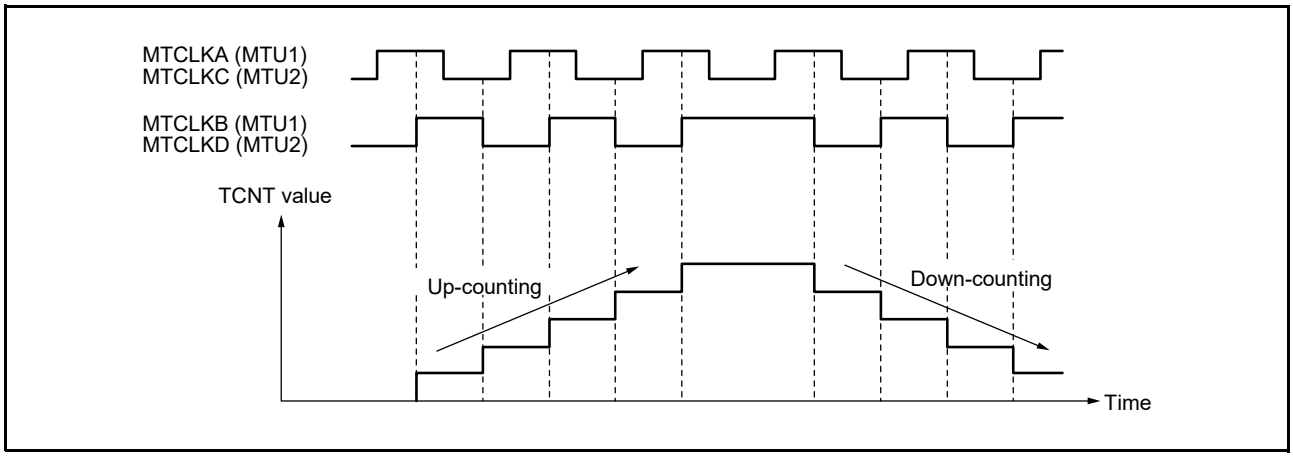


Figure 20.38 Example of Operation in Phase Counting Mode 4

Table 20.71 Up-Counting and Down-Counting Conditions in Phase Counting Mode 4

MTCLKA (MTU1) MTCLKC (MTU2)	MTCLKB (MTU1) MTCLKD (MTU2)	Operation
High	↑	Up-counting
Low	↓	
↑	Low	Not counted (Don't care)
↓	High	
High	↓	Down-counting
Low	↑	
↑	High	Not counted (Don't care)
↓	Low	

↑ : Rising edge

↓ : Falling edge

(e) Phase Counting Mode 5

Figure 20.39 and Figure 20.40 show the examples of operation in phase counting mode 5 and Table 20.72 summarizes the TCNT up-counting and down-counting conditions.

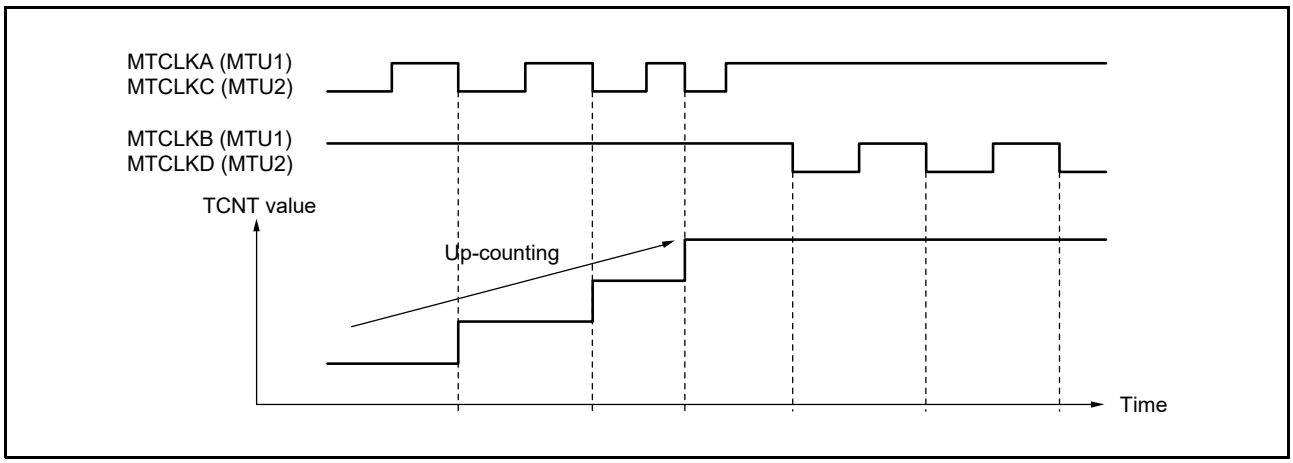


Figure 20.39 Example of Operation in Phase Counting Mode 5 (When MTUn.TCR2.PCB[1:0] = 0xb (n = 1, 2))

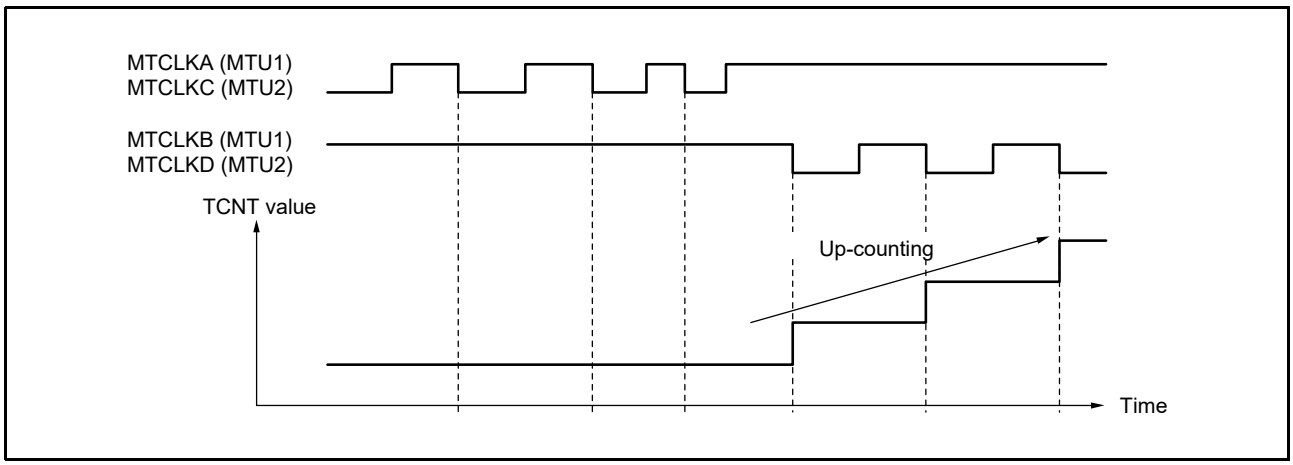


Figure 20.40 Example of Operation in Phase Counting Mode 5 (When MTUn.TCR2.PCB[1:0] = 1xb (n = 1, 2))

Table 20.72 Up-Counting and Down-Counting Conditions in Phase Counting Mode 5

PCB[1:0]	MTCLKA (MTU1) MTCLKC (MTU2)	MTCLKB (MTU1) MTCLKD (MTU2)	Operation
0xb	High	↑	Not counted (Don't care)
	Low	↓	
	↑	Low	
	↓	High	Up-counting
	High	↓	Not counted (Don't care)
	Low	↑	
	↑	High	
	↓	Low	Up-counting
1xb	High	↑	Not counted (Don't care)
	Low	↓	Up-counting
	↑	Low	Not counted (Don't care)
	↓	High	
	High	↓	Up-counting
	Low	↑	Not counted (Don't care)
	↑	High	
	↓	Low	

↑ : Rising edge

↓ : Falling edge

(3) 16-Bit Phase Counting Mode Application Example

Figure 20.41 shows an example in which MTU1 is in phase counting mode, and MTU1 is coupled with MTU0 to input 2-phase encoder pulses of a servo motor in order to detect position or speed.
MTU1 is set to phase counting mode 1, and the encoder pulse A-phase and B-phase are input to MTCLKA and MTCLKB.
In MTU0, MTU0.TGRC compare match is specified as the TCNT clearing source and MTU0.TGRA and MTU0.TGRC are used for the compare match function and are set with the speed control period and position control period.
MTU0.TGRB is used for input capture, with MTU0.TGRB and MTU0.TGRD operating in buffer mode. The MTU1 count clock is designated as the MTU0.TGRB input capture source, and the widths of 2-phase encoder 4-multiplication pulses are detected.
MTU1.TGRA and MTU1.TGRB for MTU1 are designated for the input capture function and MTU0.TGRA and MTU0.TGRC compare matches in MTU0 are selected as the input capture sources to store the up/down-counter values for the control periods.
This procedure enables the accurate detection of position and speed.

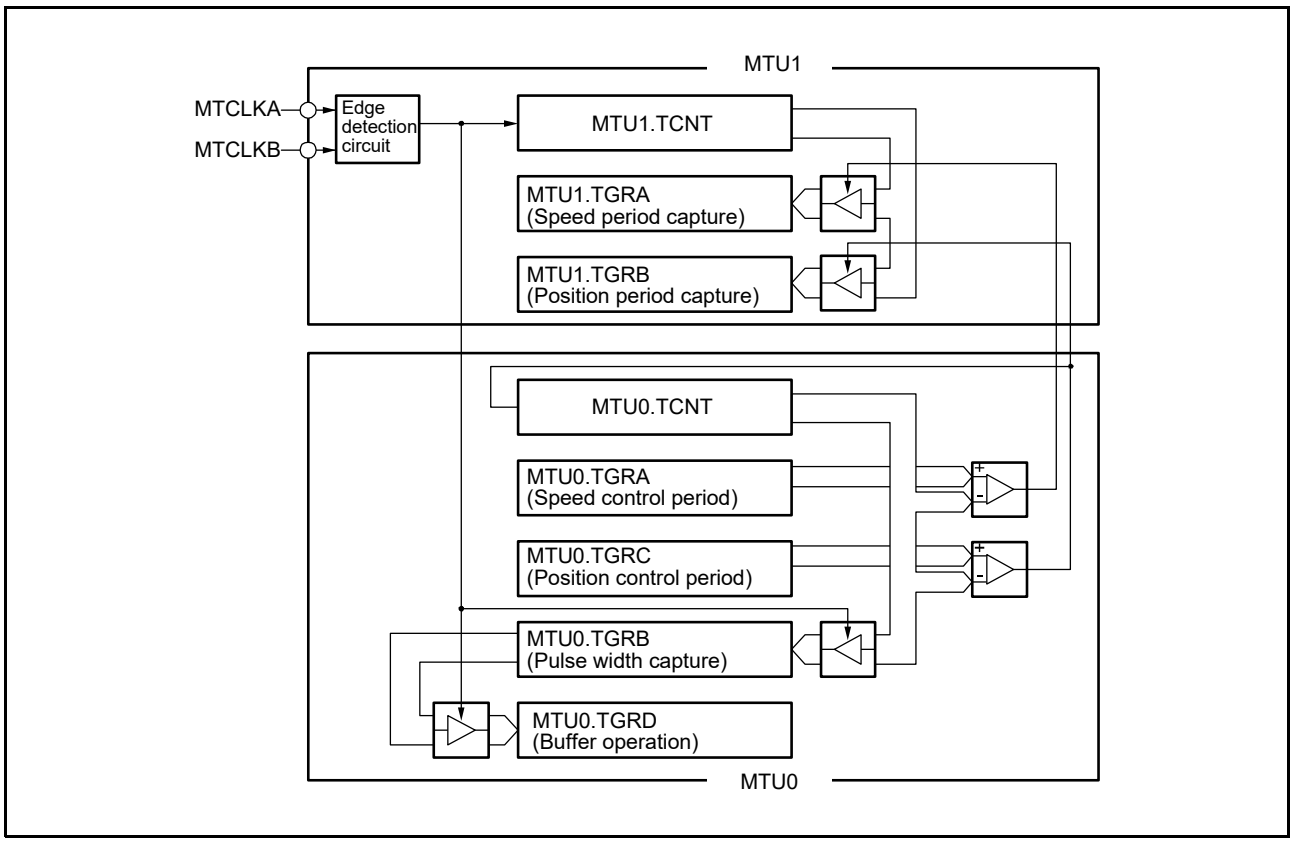


Figure 20.41 16-Bit Phase Counting Mode Application Example

20.3.6.2 Cascade Connection 32-Bit Phase Counting Mode

When MTU1 is set to phase counting mode by setting MTU1.TMDR3.LWA = 1, MTU1 and MTU2 are connected to operate in cascade connection 32-bit phase counting mode. When this mode is used, the TCR, TCR2, TIOR, TIER, TGR, and TSR registers are controlled by MTU1 and the settings of MTU2 are disabled. Refer to Figure 20.42 for the procedure for setting cascade connection 32-bit phase counting mode.
Refer to section 20.3.4, Cascaded Operation, for details on the cascade connection function for connecting MTU1 and MTU2 in a mode other than cascade connection 32-bit phase counting mode.

(1) Example of Setting Cascade Connection 32-Bit Phase Counting Mode

Figure 20.42 shows an example of the procedure for setting cascade connection 32-bit phase counting mode.

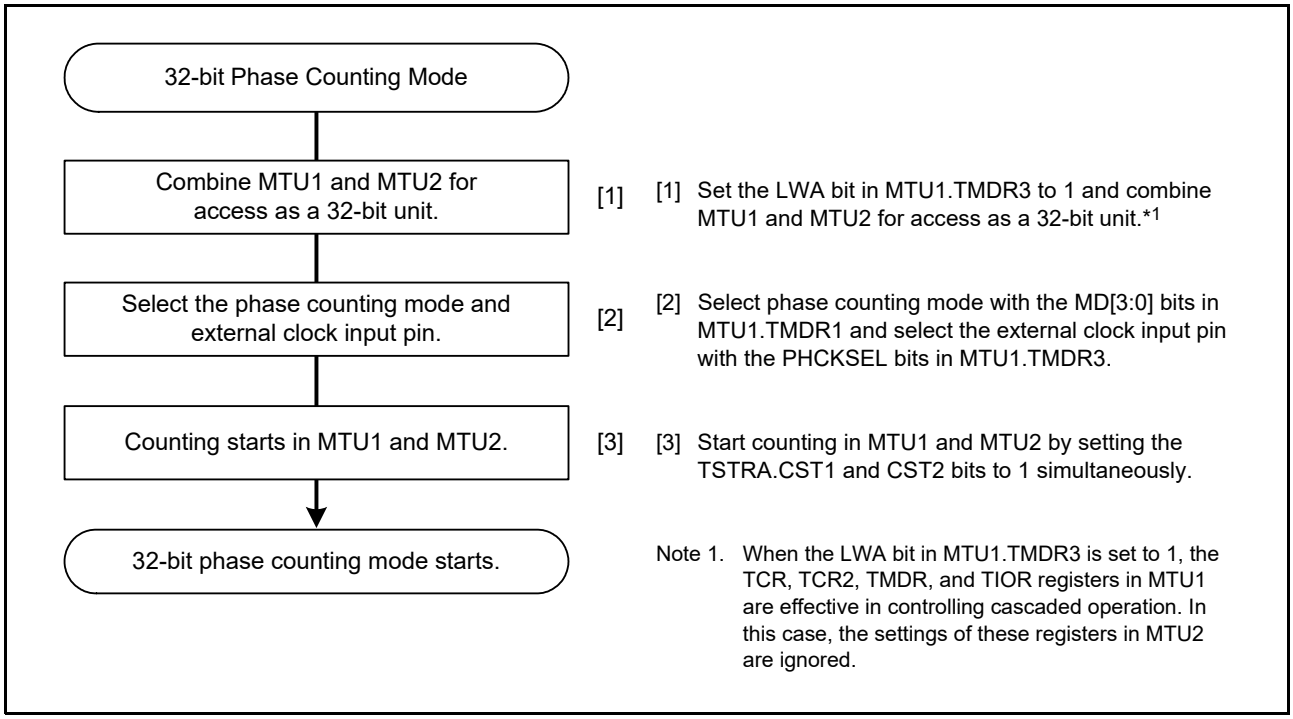


Figure 20.42 Procedure for Setting Cascade Connection 32-Bit Phase Counting Mode

20.3.7 Reset-Synchronized PWM Mode

In the reset-synchronized PWM mode, six phases of positive and negative PWM waveforms (12 phases in total) that share a common wave transition point can be output by combining MTU3 and MTU4 and MTU6 and MTU7.
When set for reset-synchronized PWM mode, the MTIOC3B, MTIOC3D, MTIOC4A, MTIOC4C, MTIOC4B, MTIOC4D, MTIOC6B, MTIOC6D, MTIOC7A, MTIOC7C, MTIOC7B, and MTIOC7D pins function as PWM output pins and timer counters 3 and 6 (MTU3.TCNT and MTU6.TCNT) functions as an up-counter.
Table 20.73 shows the PWM output pins used. Table 20.74 shows the settings of the registers.

Table 20.73 Output Pins for Reset-Synchronized PWM Mode

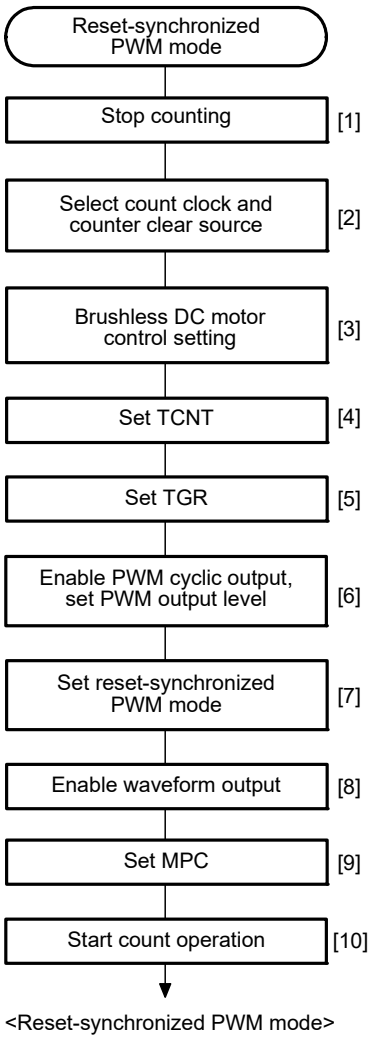
Channel	Output Pin	Description
MTU3	MTIOC3B	PWM output pin 1
	MTIOC3D	PWM output pin 1' (negative-phase waveform of PWM output 1)
MTU4	MTIOC4A	PWM output pin 2
	MTIOC4C	PWM output pin 2' (negative-phase waveform of PWM output 2)
	MTIOC4B	PWM output pin 3
	MTIOC4D	PWM output pin 3' (negative-phase waveform of PWM output 3)
MTU6	MTIOC6B	PWM output pin 4
	MTIOC6D	PWM output pin 4' (negative-phase waveform of PWM output 4)
MTU7	MTIOC7A	PWM output pin 5
	MTIOC7C	PWM output pin 5' (negative-phase waveform of PWM output 5)
	MTIOC7B	PWM output pin 6
	MTIOC7D	PWM output pin 6' (negative-phase waveform of PWM output 6)

Table 20.74 Register Settings for Reset-Synchronized PWM Mode

Register	Setting
MTU3.TCNT	Initial setting (0000h)
MTU4.TCNT	Initial setting (0000h)
MTU3.TGRA	Set the count period for MTU3.TCNT
MTU3.TGRB	Set the transition point of the PWM waveform to be output from the MTIOC3B and MTIOC3D pins
MTU4.TGRA	Set the transition point of the PWM waveform to be output from the MTIOC4A and MTIOC4C pins
MTU4.TGRB	Set the transition point of the PWM waveform to be output from the MTIOC4B and MTIOC4D pins
MTU6.TCNT	Initial setting (0000h)
MTU7.TCNT	Initial setting (0000h)
MTU6.TGRA	Set the count period for MTU6.TCNT
MTU6.TGRB	Set the transition point of the PWM waveform to be output from the MTIOC6B and MTIOC6D pins
MTU7.TGRA	Set the transition point of the PWM waveform to be output from the MTIOC7A and MTIOC7C pins
MTU7.TGRB	Set the transition point of the PWM waveform to be output from the MTIOC7B and MTIOC7D pins

(1) Example of Procedure for Setting Reset-Synchronized PWM Mode

Figure 20.43 shows an example of procedure for setting the reset-synchronized PWM mode.



[1] Clear the TSTRA.CST3 (TSTRB.CST6) and TSTRA.CST4 (TSTRB.CST7) bits to 0 to stop the TCNT count operation. Specify the reset-synchronized PWM mode while MTU3.TCNT (MTU6.TCNT) and MTU4.TCNT (MTU7.TCNT) are stopped.

[2] Set the TCR.TPSC[2:0] and TCR.CKEG[1:0] bits of MTU3 (MTU6) to select the count clock source and clock edge for MTU3 (MTU6). Set the TCR.CCLR[2:0] bits to select TGRA compare match as the counter clear source.

[3] To control a brushless DC motor, set the TGCRA.BDC (TGCRB.BDC) bit and set the feedback signal input source and output chopping or gate signal direct output.

[4] Set MTU3.TCNT (MTU6.TCNT) and MTU4.TCNT (MTU7.TCNT) to 0000h.

[5] MTU3.TGRA (MTU6.TGRA) is the period register. Set the PWM period in MTU3.TGRA (MTU6.TGRA).
Set the PWM output transition timing in MTU3.TGRB (MTU6.TGRB), MTU4.TGRA (MTU7.TGRA), and MTU4.TGRB (MTU7.TGRB).
Note that the setting values should be within the range of compare match with MTU3.TCNT (MTU6.TCNT).

$X \leq$ MTU3.TGRA (X: Set value)

[6] Set the PSYE bit in the TOCR1A (TOCR1B) register to enable or disable toggle output synchronized with the PWM period, and set the OLSP and OLSN bits to select the PWM output level.
When specifying the PWM output level using the TOCR2A (TOCR2B) and TOLBRA (TOLBRB) in buffer operation, refer to Timer Output Level Buffer Registers (TOLBRA and TOLBRB).

[7] Set the MD[3:0] bits in MTU3.TMDR1 (MTU6.TMDR1) register to 1000b to select the reset-synchronized PWM mode. Specify the buffer operation (BFA = 1) of the MTU3.TGRA (MTU6.TGRA) register and the buffer operation (BFB = 1) of the MTU3.TGRB (MTU6.TGRB) register when necessary. Set the MTU4.TMDR1 (MTU7.TMDR1) register to the initial value (normal operation; BFA = 0 and BFB = 0).

[8] Set the TOERA (TOERB) register to enable or disable output from the PWM output pin. Then, set the MTU3.TIORH (MTU6.TIORH), MTU3.TIORL (MTU6.TIORL), MTU4.TIORH (MTU7.TIORH), and MTU4.TIORL (MTU7.TIORL) registers to 00h.

[9] Set the MPU and the port mode register (PMR) of the I/O ports.

[10] Set the TSTRA.CST3 (TSTRB.CST6) bit to 1 to start count operation.

Note: The output waveform starts to toggle at the point of MTU3.TCNT (MTU6.TCNT) = MTU3.TGRA (MTU6.TGRA) = X by setting X = MTU3.TGRA (MTU6.TGRA), i.e., period = duty ratio.

Figure 20.43 Procedure for Selecting Reset-Synchronized PWM Mode

(2) Example of Reset-Synchronized PWM Mode Operation

Figure 20.44 shows an example of operation in the reset-synchronized PWM mode.
MTU3.TCNT and MTU4.TCNT (MTU6.TCNT and MTU7.TCNT) operate as up-counters. The counters are cleared when a compare match occurs between MTU3.TCNT (MTU6.TCNT) and MTU3.TGRA (MTU6.TGRA), and then begin incrementing from 0000h. The output from the PWM pins toggles every time a compare match occurs in MTU3.TGRB (MTU6.TGRB), MTU4.TGRA (MTU7.TGRA), and MTU4.TGRB (MTU7.TGRB) and the counters are cleared.

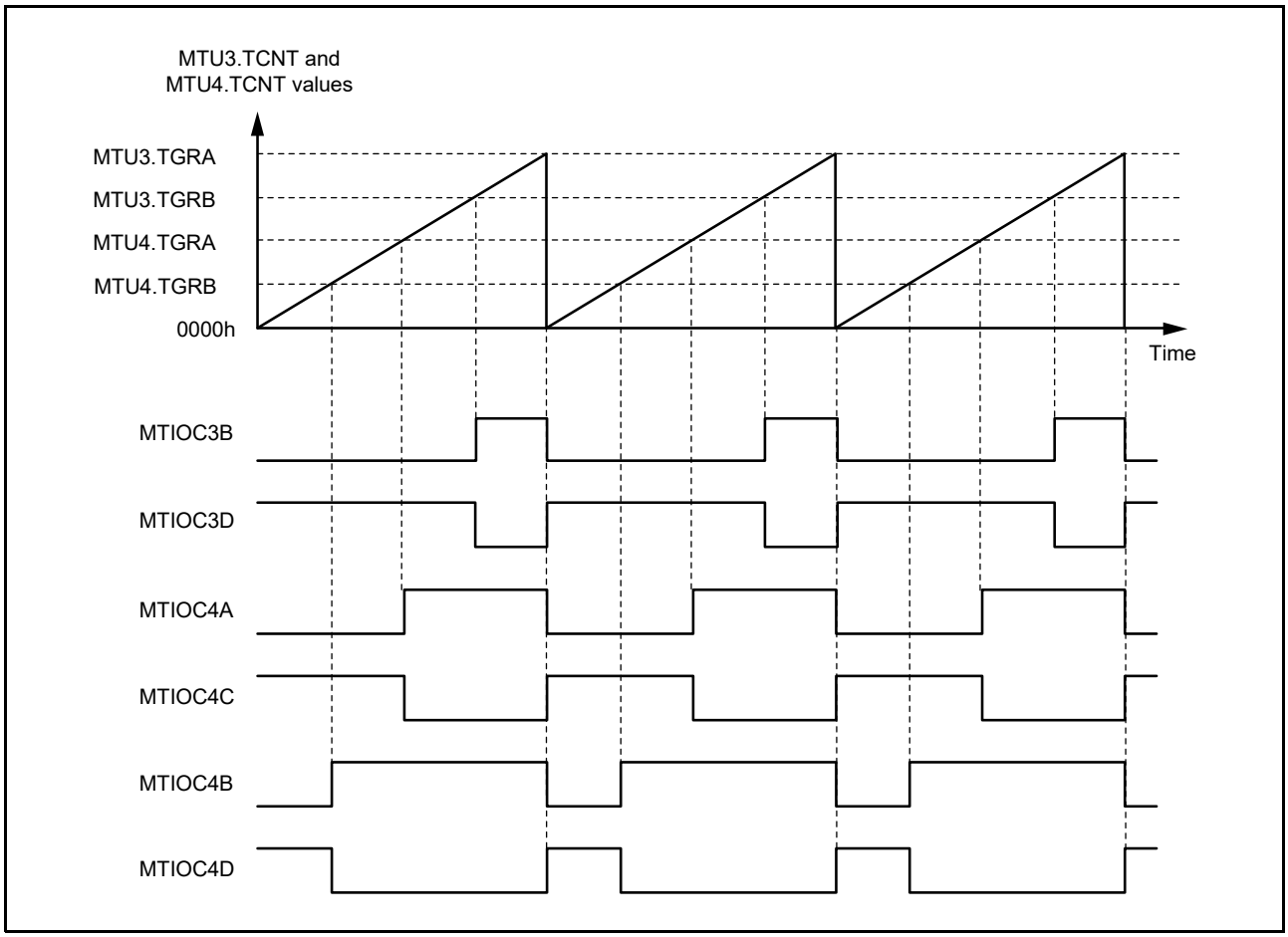


Figure 20.44 Example of Reset-Synchronized PWM Mode Operation (When OLSN = 1 and OLSP = 1 in MTU3.TOCR1 and MTU4.TOCR1)

20.3.8 Complementary PWM Mode

In complementary PWM mode, dead time can be set for PWM waveforms to be output. The dead time is the period during which the upper and lower arm transistors are set to the inactive level in order to prevent short-circuiting of the arms.
Six positive-phase and six negative-phase PWM waveforms (12 phases in total) with dead time can be output by combining MTU3/ MTU4 and MTU6/MTU7. PWM waveforms without dead time can also be output.
In complementary PWM mode, MTIOC3B, MTIOC3D, MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D, MTIOC6B, MTIOC6D, MTIOC7A, MTIOC7B, MTIOC7C, and MTIOC7D pins function as PWM output pins, and the MTIOC3A and MTIOC6A pins can be set for toggle output synchronized with the PWM period.
MTU3.TCNT, MTU4.TCNT, MTU6.TCNT, and MTU7.TCNT function as up/down-counters.
Table 20.75 shows the PWM output pins used. Table 20.76 shows the settings of the registers used.
A function to directly cut off the PWM output by using an external signal is supported as a port function.

Table 20.75 Output Pins for Complementary PWM Mode

Channel	Output Pin	Description
MTU3	MTIOC3A	Toggle output synchronized with PWM period (or I/O port)
	MTIOC3B	PWM output pin 1
	MTIOC3C	I/O port*1
	MTIOC3D	PWM output pin 1' (negative-phase waveform output of PWM output 1)
MTU4	MTIOC4A	PWM output pin 2
	MTIOC4C	PWM output pin 2' (negative-phase waveform output of PWM output 1)
	MTIOC4B	PWM output pin 3
	MTIOC4D	PWM output pin 3' (negative-phase waveform output of PWM output 1)
MTU6	MTIOC6A	Toggle output synchronized with PWM period (or I/O port)
	MTIOC6B	PWM output pin 4
	MTIOC6C	I/O port*1
	MTIOC6D	PWM output pin 4' (negative-phase waveform output of PWM output 4)
MTU7	MTIOC7A	PWM output pin 5
	MTIOC7C	PWM output pin 5' (negative-phase waveform output of PWM output 5)
	MTIOC7B	PWM output pin 6
	MTIOC7D	PWM output pin 6' (negative-phase waveform output of PWM output 6)

Note 1. Avoid setting the MTIOC3C and MTIOC6C pins as timer I/O pins in complementary PWM mode.

Table 20.76 Register Settings for Complementary PWM Mode (1/2)

Channel	Counter/ Register	Description	Read/Write from CPU
MTU3	TCNT	Starts up-counting from the value set in the dead time register	Maskable by TRWERA setting*1
	TGRA	Set MTU3.TCNT upper limit value (1/2 carrier period + dead time)	Maskable by TRWERA setting*1
	TGRB	PWM output 1 compare register	Maskable by TRWERA setting*1
	TGRC	MTU3.TGRA buffer register	Readable/writable
	TGRD	PWM output 1/MTU3.TGRB buffer register	Readable/writable
	TGRE	MTU3.TGRB buffer register B (when double buffer function is used)	Readable/writable
MTU4	TCNT	Starts up-counting after being initialized to 0000h	Maskable by TRWERA setting*1
	TGRA	PWM output 2 compare register	Maskable by TRWERA setting*1
	TGRB	PWM output 3 compare register	Maskable by TRWERA setting*1
	TGRC	PWM output 2/MTU4.TGRA buffer register	Readable/writable
	TGRD	PWM output 3/MTU4.TGRB buffer register	Readable/writable
	TGRE	MTU4.TGRA buffer register B (when double buffer function is used)	Readable/writable
	TGRF	MTU4.TGRB buffer register B (when double buffer function is used)	Readable/writable
MTU6	TCNT	Starts up-counting from the value set in the dead time register	Maskable by TRWERB setting*2
	TGRA	Set MTU6.TCNT upper limit value (1/2 carrier period + dead time)	Maskable by TRWERB setting*2
	TGRB	PWM output 4 compare register	Maskable by TRWERB setting*2
	TGRC	MTU6.TGRA buffer register	Readable/writable
	TGRD	PWM output 4/MTU6.TGRB buffer register	Readable/writable
	TGRE	MTU6.TGRB buffer register B (when double buffer function is used)	Readable/writable
MTU7	TCNT	Starts up-counting after being initialized to 0000h	Maskable by TRWERB setting*2
	TGRA	PWM output 5 compare register	Maskable by TRWERB setting*2
	TGRB	PWM output 6 compare register	Maskable by TRWERB setting*2
	TGRC	PWM output 5/MTU7.TGRA buffer register	Readable/writable
	TGRD	PWM output 6/MTU7.TGRB buffer register	Readable/writable
	TGRE	MTU7.TGRA buffer register B (when double buffer function is used)	Readable/writable
	TGRF	MTU7.TGRB buffer register B (when double buffer function is used)	Readable/writable

Note 1. Access can be enabled or disabled according to the setting in TRWERA (timer read/write enable register A).
Note 2. Access can be enabled or disabled according to the setting in TRWERB (timer read/write enable register B).

Table 20.77 Register Settings for Complementary PWM Mode (2/2)

Channel	Counter/ Register	Description	Read/Write from CPU
Timer dead time data register A (TDDRA)		Set MTU4.TCNT and MTU3.TCNT offset value (dead time value)	Maskable by TRWERA setting*1
Timer dead time data register B (TDDRB)		Set MTU7.TCNT and MTU6.TCNT offset value (dead time value)	Maskable by TRWERB setting *2
Timer period data register A (TCDRA)		Set MTU4.TCNT upper limit value (1/2 carrier period)	Maskable by TRWERA setting*1
Timer period data register B (TCDRB)		Set MTU7.TCNT upper limit value (1/2 carrier period)	Maskable by TRWERB setting*2
Timer period buffer register A (TCBRA)		TCDRA buffer register	Readable/writable
Timer period buffer register B (TCBRB)		TCDRB buffer register	Readable/writable
Subcounter A (TCNTSA)		Subcounter A for dead time generation	Read-only
Subcounter B (TCNTSB)		Subcounter B for dead time generation	Read-only
Temporary register 1A (TEMP1A)		PWM output 1/MTU3.TGRB temporary register A	Not readable/writable
Temporary register 1B (TEMP1B)		PWM output 1/MTU3.TGRB temporary register B (when double buffer function is used)	Not readable/writable
Temporary register 2A (TEMP2A)		PWM output 2/MTU4.TGRA temporary register A	Not readable/writable
Temporary register 2B (TEMP2B)		PWM output 2/MTU4.TGRA temporary register B (when double buffer function is used)	Not readable/writable
Temporary register 3A (TEMP3A)		PWM output 3/MTU4.TGRB temporary register A	Not readable/writable
Temporary register 3B (TEMP3B)		PWM output 3/MTU4.TGRB temporary register B (when double buffer function is used)	Not readable/writable
Temporary register 4A (TEMP4A)		PWM output 4/MTU6.TGRB temporary register A	Not readable/writable
Temporary register 4B (TEMP4B)		PWM output 4/MTU6.TGRB temporary register B (when double buffer function is used)	Not readable/writable
Temporary register 5A (TEMP5A)		PWM output 5/MTU7.TGRA temporary register A	Not readable/writable
Temporary register 5B (TEMP5B)		PWM output 5/MTU7.TGRA temporary register B (when double buffer function is used)	Not readable/writable
Temporary register 6A (TEMP6A)		PWM output 6/MTU7.TGRB temporary register A	Not readable/writable
Temporary register 6B (TEMP6B)		PWM output 6/MTU7.TGRB temporary register B (when double buffer function is used)	Not readable/writable

Note 1. Access can be enabled or disabled according to the setting in TRWERA (timer read/write enable register A).
Note 2. Access can be enabled or disabled according to the setting in TRWERB (timer read/write enable register B).

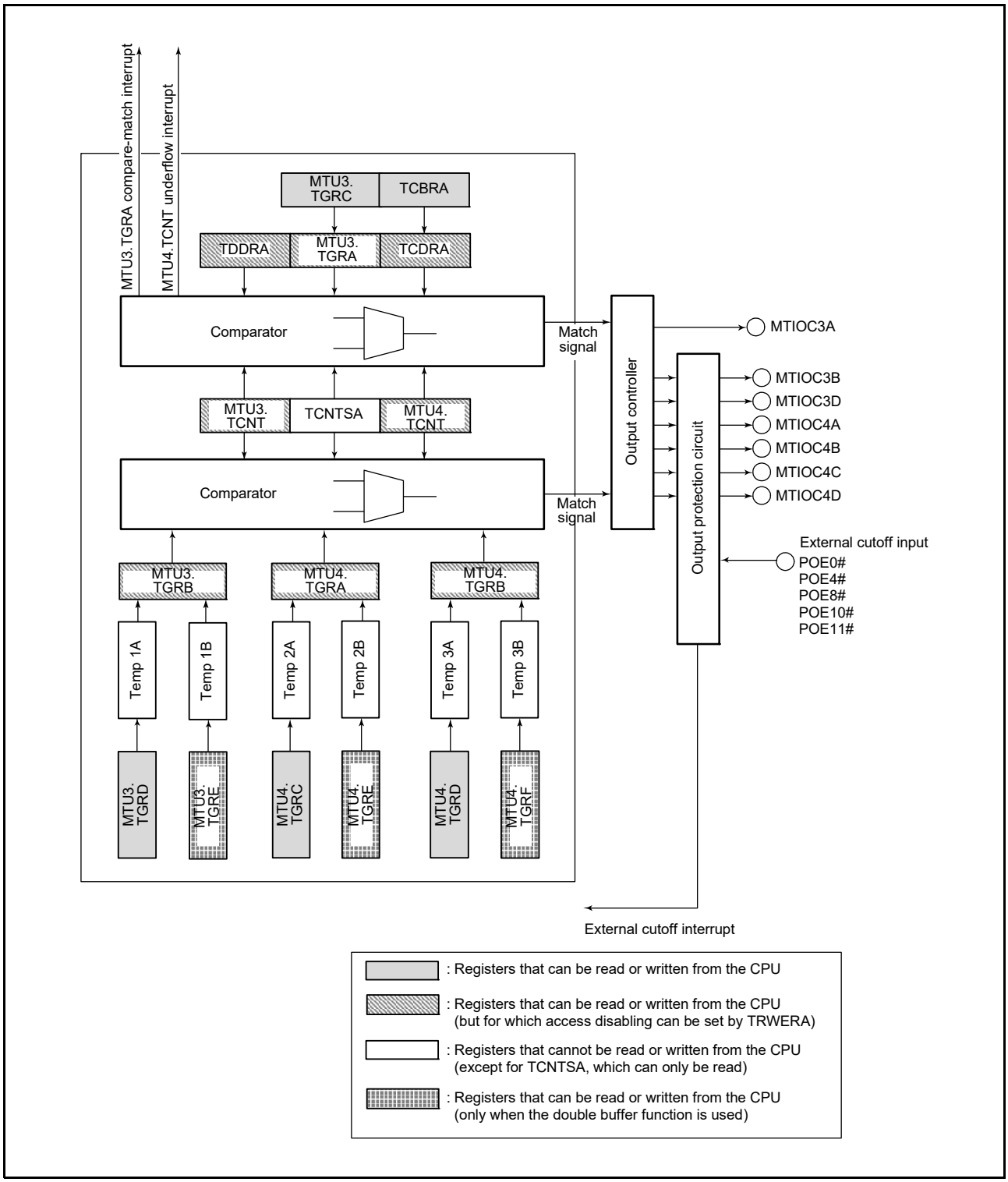


Figure 20.45 Block Diagram of MTU3 and MTU4 in Complementary PWM Mode

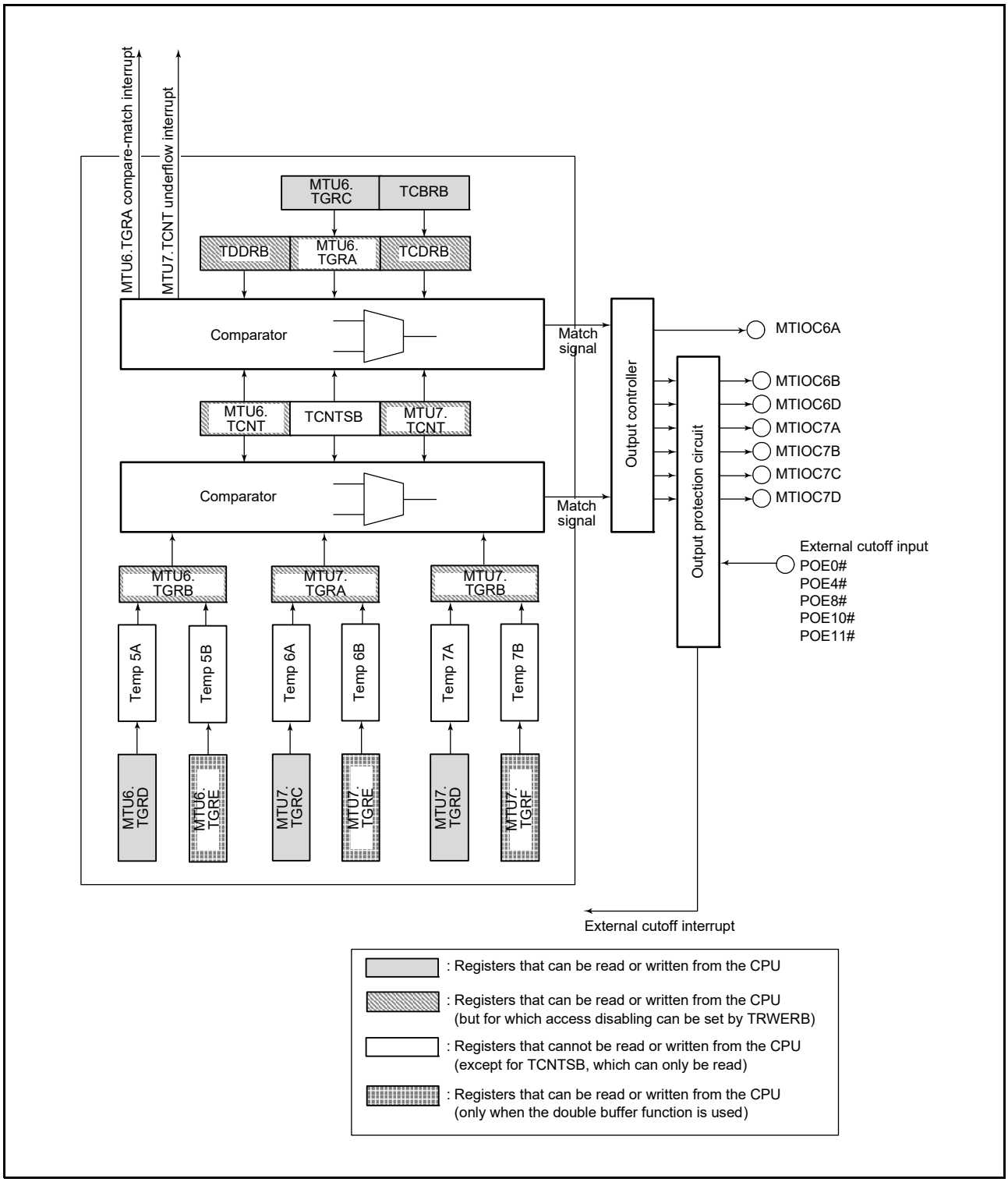
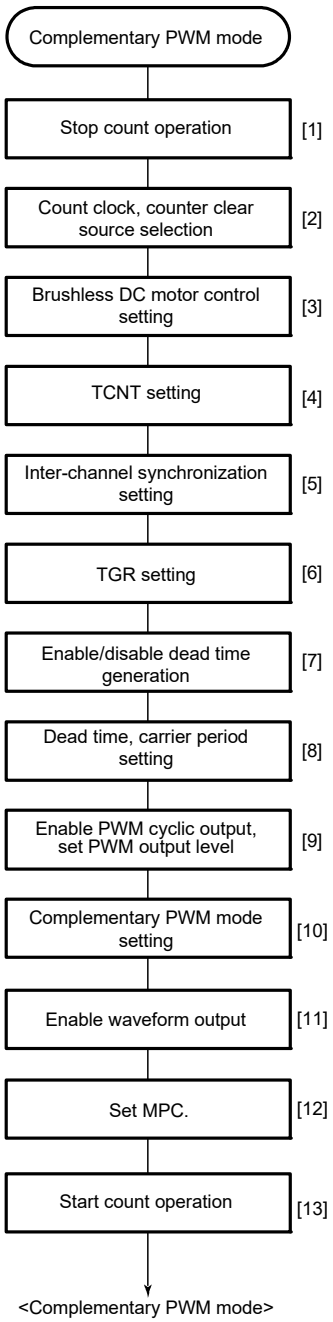


Figure 20.46 Block Diagram of MTU6 and MTU7 in Complementary PWM Mode

(1) Example of Complementary PWM Mode Setting Procedure

Figure 20.47 shows an example of the complementary PWM mode setting procedure.



[1] Clear the TSTRA.CST3 (TSTRB.CST6) and TSTRA.CST4 (TSTRB.CST7) bits to 0 to stop the TCNT count operation.
Specify complementary PWM mode while MTU3.TCNT (MTU6.TCNT) and MTU4.TCNT (MTU7.TCNT) are stopped.

[2] Set the TCR.TPSC[2:0] and TCR.CKEG[1:0] bits of MTU3 and MTU4 (MTU6 and MTU7) to select the same count clock source and clock edge for MTU3 and MTU4 (MTU6 and MTU7).
Set the TCR.CCLR[2:0] bits only when restarting by synchronous clearing with another channel during complementary PWM operation.

[3] To control a brushless DC motor, set the TGCRA.BDC (TGCRB.BDC) bit and set the feedback signal input source and output chopping or gate signal direct output.

[4] Set the dead time in MTU3.TCNT (MTU6.TCNT). Set MTU4.TCNT (MTU7.TCNT) to 0000h.

[5] Make this setting only when restarting by synchronous clearing with another channel during complementary PWM mode operation. In this case, set the TSYRA register (TSYRB) to synchronize the channel generating the synchronous clear with MTU3 and MTU4 (MTU6 and MTU7).

[6] When MTU3 and MTU6 are used, set the PWM output duty ratio in the duty registers (MTU3.TGRB, MTU4.TGRA, and MTU4.TGRB) and buffer registers (MTU3.TGRD, MTU4.TGRC, and MTU4.TGRD).
Be sure to set the same value in each pair of the duty registers (MTU3.TGRD, MTU4.TGRC, and MTU4.TGRD) and buffer registers (MTU3.TGRB, MTU4.TGRA, and MTU4.TGRB).
Only when the double buffer function is used, set the buffer registers (MTU3.TGRE, MTU4.TGRE, and MTU4.TGRF).
When MTU6 and MTU7 are used, set the value to the following registers:
Duty registers (MTU6.TGRB, MTU7.TGRA, and MTU7.TGRB)
Buffer registers (MTU6.TGRD, MTU7.TGRC, and MTU7.TGRD)
Buffer registers when the double buffer function is used (MTU6.TGRE, MTU7.TGRE, and MTU7.TGRF)

[7] This setting is necessary only when no dead time should be generated. Make appropriate settings in the TDERA (TDERB) register so that no dead time generated.

[8] Set the dead time in the TDDRA (TDDRB) register, 1/2 the PWM period in the TCDRA (TCDRB) register and TCBRA (TCBRB) register, and 1/2 the PWM period plus the dead time in MTU3.TGRA (MTU6.TGRA) and MTU3.TGRC (MTU6.TGRC).
When no dead time generation is selected, set 1 in the TDDRA (TDDRB) register and 1/2 the PWM period + 1 in MTU3.TGRA (MTU6.TGRA) and MTU3.TGRC (MTU6.TGRC).

[9] Set the PSYE bit in the TOCR1A (TOCR1B) register to enable or disable toggle output synchronized with the PWM period, and set the OLSP and OLSN bits to select the PWM output level.
When specifying the PWM output level using the TOCR2A (TOCR2B) and TOLBRA (TOLBRA) in buffer operation, refer to Timer Output Level Buffer Registers (TOLBRA and TOLBRB).

[10] Select complementary PWM mode in MTU3.TMDR1 (MTU6.TMDR1). Specify the buffer operation (BFA = 1) of MTU3.TGRA (MTU6.TGRA) and the buffer operation (BFB = 1) of MTU3.TGRB (MTU6.TGRB).
Only when the double buffer function is used, set the TMDR2A (TMDR2B) register to enable the double buffer function.

[11] Set the TOERA (TOERB) register to enable or disable output from the PWM output pin. Then, set the MTU3.TIORH (MTU6.TIORH), MTU3.TIORL (MTU6.TIORL), MTU4.TIORH (MTU7.TIORH), and MTU4.TIORL (MTU7.TIORL) to 00h.

[12] Set the MPU and the port mode register (PMR) of the I/O ports.

[13] Set the TSTRA.CST3 (TSTRB.CST6) and TSTRA.CST4 (TSTRB.CST7) bits to 1 simultaneously to start count operation.

Figure 20.47 Example of Complementary PWM Mode Setting Procedure

(2) Outline of Complementary PWM Mode Operation

In complementary PWM mode, six phases (three positive and three negative) PWM waveforms can be output. Figure 20.48 illustrates counter operation in complementary PWM mode (MTU3 and MTU4), and Figure 20.49 shows an example of operation in complementary PWM mode.

(a) Counter Operation

In complementary PWM mode, three counters—MTU3.TCNT, MTU4.TCNT, and TCNTSA (MTU6.TCNT, MTU7.TCNT, and TCNTSB) —in each unit perform up-/down-count operations.
MTU3.TCNT (MTU6.TCNT) is automatically initialized to the value set in TDDRA (TDDRB) when complementary PWM mode is selected and the CST bit in TSTRA (TSTRB) is 0. When the CST bit is set to 1, MTU3.TCNT (MTU6.TCNT) counts up to the value set in MTU3.TGRA (MTU6.TGRA), then switches to down-counting when it matches MTU3.TGRA (MTU6.TGRA). When the MTU4.TCNT (MTU7.TCNT) value matches 0000h, MTU3.TCNT (MTU6.TCNT) switches to up-counting, and the operation is repeated in this way.
MTU4.TCNT (MTU7.TCNT) should be initialized to 0000h after a reset. When the CST bit is set to 1, MTU4.TCNT (MTU7.TCNT) counts up in synchronization with MTU3.TCNT (MTU6.TCNT), and switches to down-counting when MTU3.TCNT (MTU6.TCNT) matches MTU3.TGRA (MTU6.TGRA). On reaching 0000h, MTU4.TCNT (MTU7.TCNT) switches to up-counting, and the operation is repeated in this way. TCNTSA (TCNTSB) is a read-only counter. It does not need to be initialized after a reset.
In counting up by MTU3.TCNT and MTU4.TCNT (or MTU6.TCNT and MTU7.TCNT), MTU3.TCNT (or MTU6.TCNT) starts counting up when it matches TCDRA (or TCDRB) and switches to counting down when it matches MTU3.TGRA (or MTU6.TGRA). Furthermore, when MTU4.TCNT (or MTU7.TCNT) matches TDDRA (or TDDRB), TCNTSA (or TCNTSB) is set to the value in MTU3.TGRA (or MTU6.TGRA) and counting is stopped.
When MTU4.TCNT (MTU7.TCNT) matches TDDRA (TDDRB) during down-counting of MTU3.TCNT and MTU4.TCNT (MTU6.TCNT and MTU7.TCNT), TCNTSA (TCNTSB) starts up-counting, and when MTU4.TCNT (MTU7.TCNT) matches 0000h, the operation switches to down-counting. When MTU3.TCNT (MTU6.TCNT) matches TCDRA (TCDRB), TCNTSA (TCNTSB) is cleared to 0000h and stops counting.
TCNTSA (TCNTSB) is compared with the compare register and temporary register, in which the PWM duty is specified, only during the count operation.

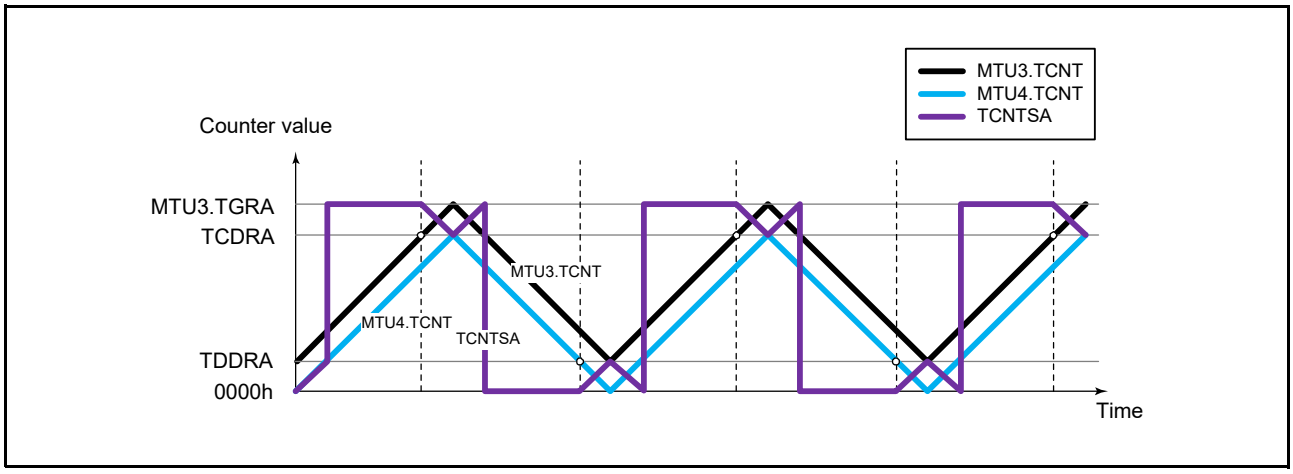


Figure 20.48 Counter Operation in Complementary PWM Mode

(b) Register Operation

In complementary PWM mode, nine registers (compare registers, buffer registers, and temporary registers) are used to control the duty ratio for the PWM output. Figure 20.49 shows an example of operation in complementary PWM mode (MTU3 and MTU4).

MTU3.TGRB, MTU4.TGRA, and MTU4.TGRB (MTU6.TGRB, MTU7.TGRA, and MTU7.TGRB) are constantly compared with the counters to generate PWM waveforms. When these registers match the counter, the value set in the OLSN and OLSP bits in the timer output control registers (TOCR1A and TOCR1B) is output from the PWM output pin.

MTU3.TGRD, MTU4.TGRC, and MTU4.TGRD (MTU6.TGRD, MTU7.TGRC, and MTU7.TGRD) are buffer registers for these compare registers.

When the double buffer function is used, MTU3.TGRE, MTU4.TGRE, and MTU4.TGRF (MTU6.TGRE, MTU7.TGRE, and MTU7.TGRF) are also used as buffer registers B. For details of double buffer operation, refer to section 20.3.8 (2) (s), Double Buffer Function in Complementary PWM Mode.

Data in a compare register can be changed by writing new data to the corresponding buffer register. The buffer registers can be read or written at any time.

When modifying data in a buffer register, write to MTU4.TGRD (MTU7.TGRD) last and enable data transfer from the buffer register to a temporary register. At this time, transfer from the TCBRA (TCBRB) register and MTU3.TGRC (MTU6.TGRC) register, which operate as buffer registers for the timer period registers, to temporary registers is also enabled. Data is transferred to all five temporary registers at the same time.

When transfer is enabled in the Ta interval, data written to a buffer register is transferred to the temporary register. The data is not transferred to the temporary register in the Tb1 and Tb2 intervals. Data enabled for transfer in this interval is transferred to the temporary register at the end of this interval.

The value transferred to a temporary register is transferred to the compare register at the end of the Tb1 interval (when matches MTU3.TGRA (MTU6.TGRA) while TCNTSA (TCNTSB) is counting up), or at the end of the Tb2 interval (when matches 0000h while TCNTSA (TCNTSB) is counting down). The timing for transfer from the temporary register to the compare register can be selected with bits MD[3:0] in the timer mode register 1 (TMDR1). Figure 20.49 shows an example in which the trough is selected for the transfer timing.

In the Tb interval in which data is not transferred to the temporary register (Tb1 in Figure 20.49), the temporary register has the same function as the compare register and is compared with the counter. In this interval, therefore, there are two compare match registers for one output phase; the compare register contains the pre-change data and the temporary register contains new data. In this interval, three counters MTU3.TCNT, MTU4.TCNT, and TCNTSA (MTU6.TCNT, MTU7.TCNT, and TCNTSB) and two registers (compare register and temporary register) are compared, and PWM output is controlled accordingly.

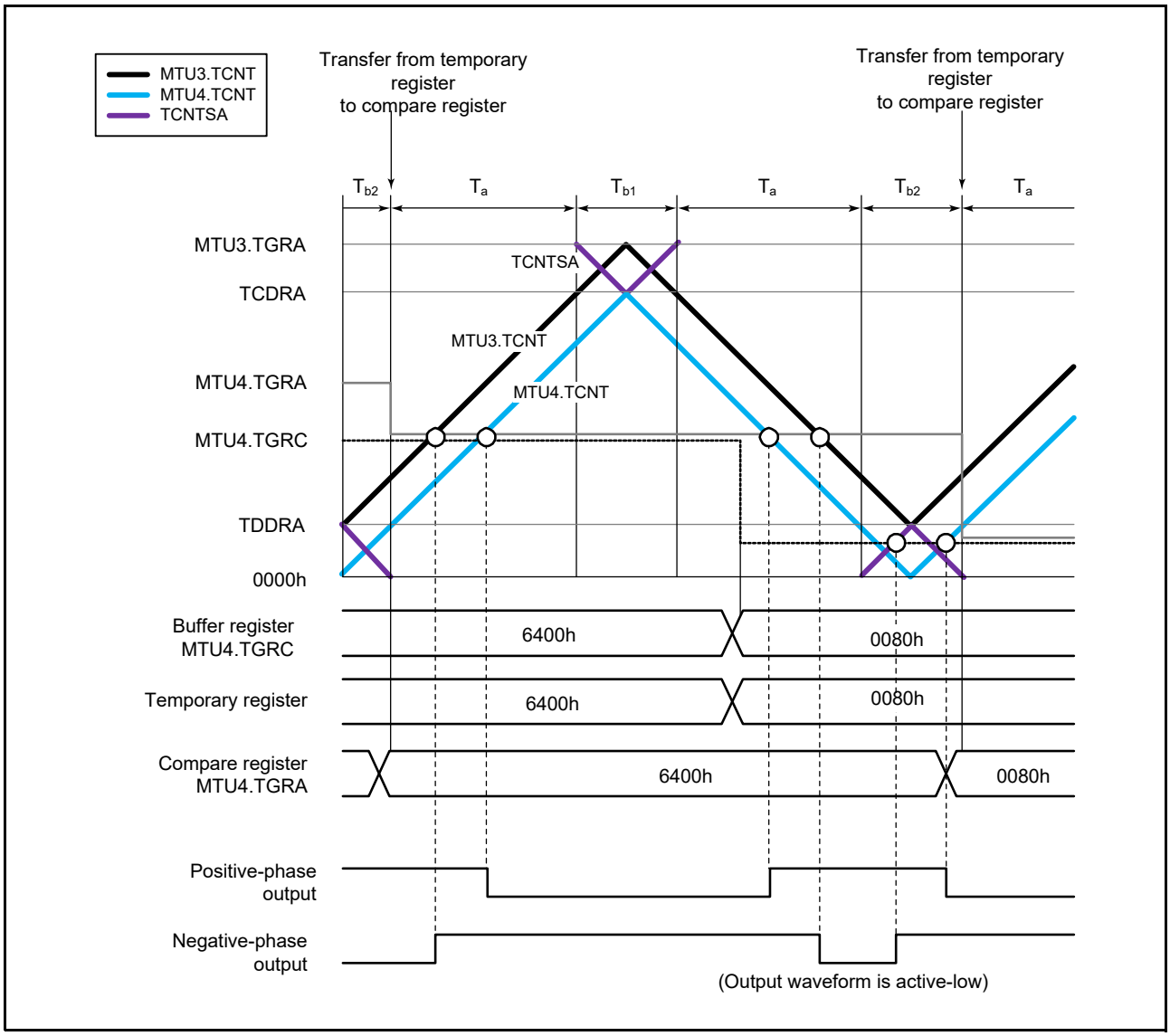


Figure 20.49 Example of Operation in Complementary PWM Mode (MTU3 and MTU4)

(c) Initial Setting

In complementary PWM mode, there are nine registers that require initial setting. In addition, there is a register that specifies whether to generate dead time (it should be used only when dead time generation should be disabled).
Before setting complementary PWM mode with MTU3.TMDR1.MD[3:0] (MTU6.TMDR1.MD[3:0]) bits, initial values should be set in the following registers.
The TOCR1A, TOCR2A, TOCR1B, and TOCR2B registers are used to set the PWM output level. MTU3.TGRC (MTU6.TGRC) operates as the buffer register for MTU3.TGRA (MTU6.TGRA), and should be set with 1/2 the PWM period + dead time Td. The timer period buffer register (TCBRA or TCBRB) operates as the buffer register for the timer period data register (TCDRA or TCDRB), and should be set with 1/2 the PWM period. Set dead time Td in the timer dead time data register (TDDRA or TDDRB).
When dead time is not needed, the TDER bit in the timer dead time enable register (TDERA or TDERB) should be cleared to 0, MTU3.TGRC and MTU3.TGRA (MTU6.TGRC and MTU6.TGRA) should be set to 1/2 the PWM carrier period + 1, and TDDRA (TDDRB) should be set to 1.
Set the respective initial PWM duty values in three buffer registers A (MTU3.TGRD, MTU4.TGRC, and MTU4.TGRD (MTU6.TGRD, MTU7.TGRC, and MTU7.TGRD)).
Set three buffer registers B (MTU3.TGRE, MTU4.TGRE, and MTU4.TGRF (MTU6.TGRE, MTU7.TGRE, and MTU7.TGRF)) only when the double buffer function is used.
The values set in the five buffer registers excluding TDDRA (TDDRB) are transferred to the corresponding compare registers as soon as complementary PWM mode is set.
Set MTU4.TCNT (MTU7.TCNT) to 0000h before setting complementary PWM mode.

Table 20.78 Registers and Counters Requiring Initial Setting

Register and Counter	Setting
TOCR1A, TOCR2A, TOCR1B, TOCR2B	PWM output level
MTU3.TGRC MTU6.TGRC	1/2 PWM period + dead time Td (1/2 PWM period + 1 when dead time generation is disabled by TDERA or TDERB)
TDDRA, TDDRB	Dead time Td (1 when dead time generation is disabled by TDERA or TDERB)
TCBRA, TCBRB	1/2 PWM period
MTU3.TGRD, MTU4.TGRC, MTU4.TGRD MTU6.TGRD, MTU7.TGRC, MTU7.TGRD	Initial PWM duty ratio value for each phase
MTU3.TGRE, MTU4.TGRE, MTU4.TGRF MTU6.TGRE, MTU7.TGRE, MTU7.TGRF	Initial PWM duty ratio value for each phase (only when double buffer function is used)
MTU4.TCNT MTU7.TCNT	0000h

Note: The value set in MTU3.TGRC (MTU6.TGRC) should be the sum of 1/2 the PWM period set in TCBRA (TCBRB) and dead time Td set in TDDRA (TDDRB). When dead time generation is disabled by TDERA (TDERB), TGRC should be set to 1/2 the PWM period + 1.

(d) PWM Output Level Setting

In complementary PWM mode, the PWM output level is set with bits OLSN and OLSP in timer output control register 1 (TOCR1A or TOCR1B) or bits OLS1P to OLS3P and OLS1N to OLS3N in timer output control register 2 (TOCR2A or TOCR2B).
The output level can be set for each of the three positive phases and three negative phases of 6-phase output.
Complementary PWM mode should be cleared before setting or changing output levels.

(e) Dead Time Setting

In complementary PWM mode, dead time can be set for PWM output.
The dead time is set in the timer dead time data register (TDDRA or TDDRB). The value set in TDDRA (TDDRB) is used as the MTU3.TCNT (MTU6.TCNT) counter start value and creates a non-overlapping interval between MTU3.TCNT (MTU6.TCNT) and MTU4.TCNT (MTU7.TCNT). Complementary PWM mode should be cleared before changing the contents of TDDRA (TDDRB).

(f) Dead Time Suppressing

Dead time generation is suppressed by clearing the TDER bit in the timer dead time enable register (TDERA or TDERB) to 0. TDERA (TDERB) can be cleared to 0 only when 0 is written to it after reading TDER = 1.
MTU3.TGRA and MTU3.TGRC (MTU6.TGRA and MTU6.TGRC) should be set to 1/2 PWM period + 1 and the timer dead time data register (TDDRA or TDDRB) should be set to 1.
By the above settings, PWM waveforms without dead time can be obtained. Figure 20.50 shows an example of operation without dead time (MTU3 and MTU4).

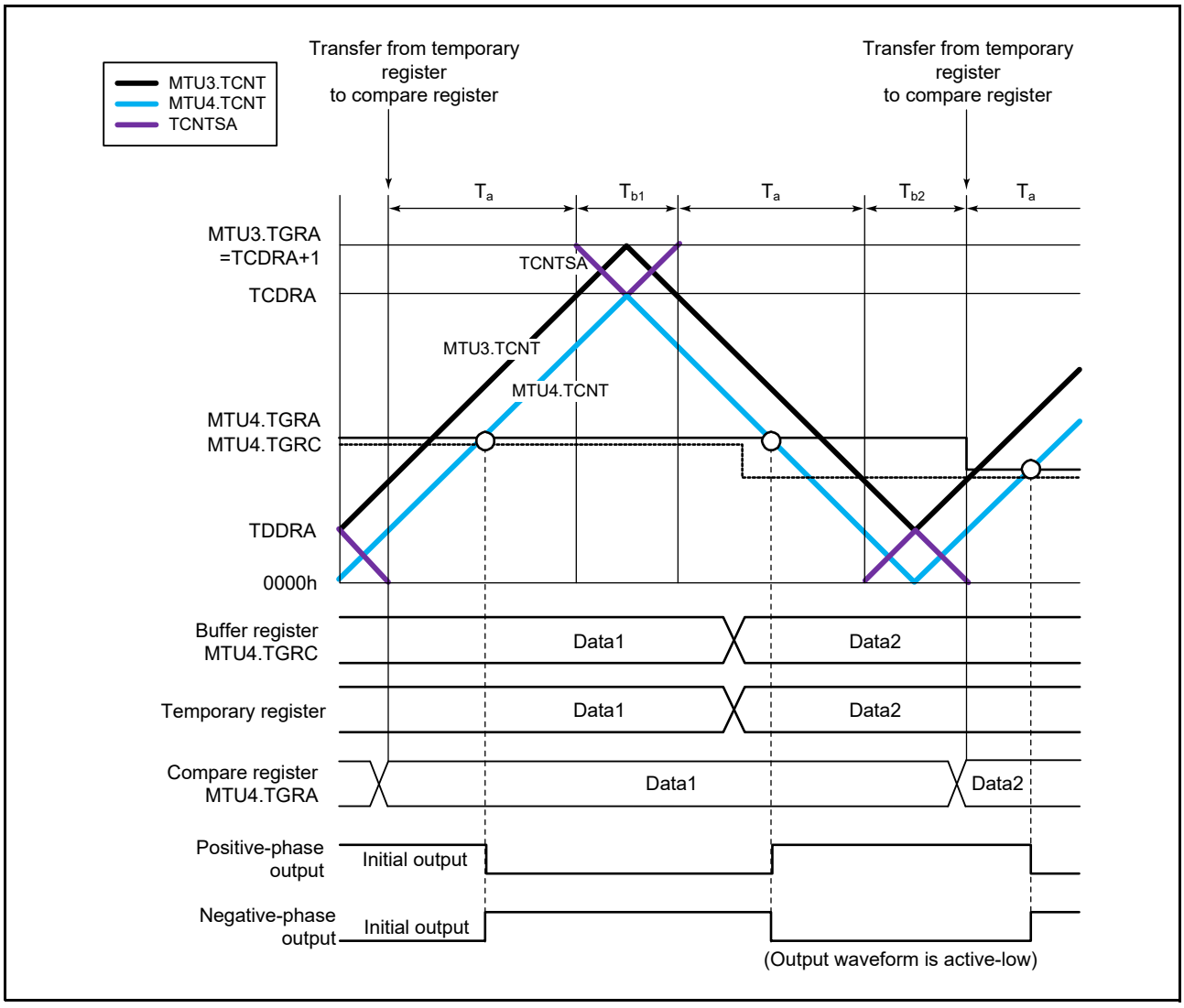


Figure 20.50 Example of Operation without Dead Time (MTU3 and MTU4)

(g) PWM Period Setting

In complementary PWM mode, the PWM period is set in two registers—MTU3.TGRA (MTU6.TGRA), in which the MTU3.TCNT (MTU6.TCNT) upper limit value is set, and TCDRA (TCDRB), in which the MTU4.TCNT (MTU7.TCNT) upper limit value is set. The settings should be made so as to achieve the following relationship between these two registers:

With dead time: MTU3.TGRA (MTU6.TGRA) setting = TCDRA (TCDRB) setting + TDDRA (TDDRB) setting
Without dead time: MTU3.TGRA (MTU6.TGRA) setting = TCDRA (TCDRB) setting + 1

In addition, the settings should be made so as to achieve the following relationship between the TCDRA (TCDRB) register and the TDDRA (TDDRB) register:

TCDRA (TCDRB) setting > TDDRA (TDDRB) setting × 2 + 2

The MTU3.TGRA and TCDRA (MTU6.TGRA and TCDRB) settings are made by setting values in buffer registers MTU3.TGRC and TCBRA (MTU6.TGRC and TCBRB). When data is written to MTU4.TGRD (MTU7.TGRD) to enable transfers, the values set in MTU3.TGRC and TCBRA (MTU6.TGRC and TCBRB) are transferred simultaneously to the MTU3.TGRA and TCDRA (MTU6.TGRA and TCDRB) with the transfer timing selected with the MTU3.TMDR1.MD[3:0] (MTU6.TMDR1.MD[3:0]) bits.
The new PWM period is reflected from the next cycle when data is updated at the crest, or from the current cycle when updated in the trough. Figure 20.51 illustrates the operation when the PWM period is updated at the crest.
Refer to the following section, (h), Register Data Updating, for the method of updating the data in each buffer register.

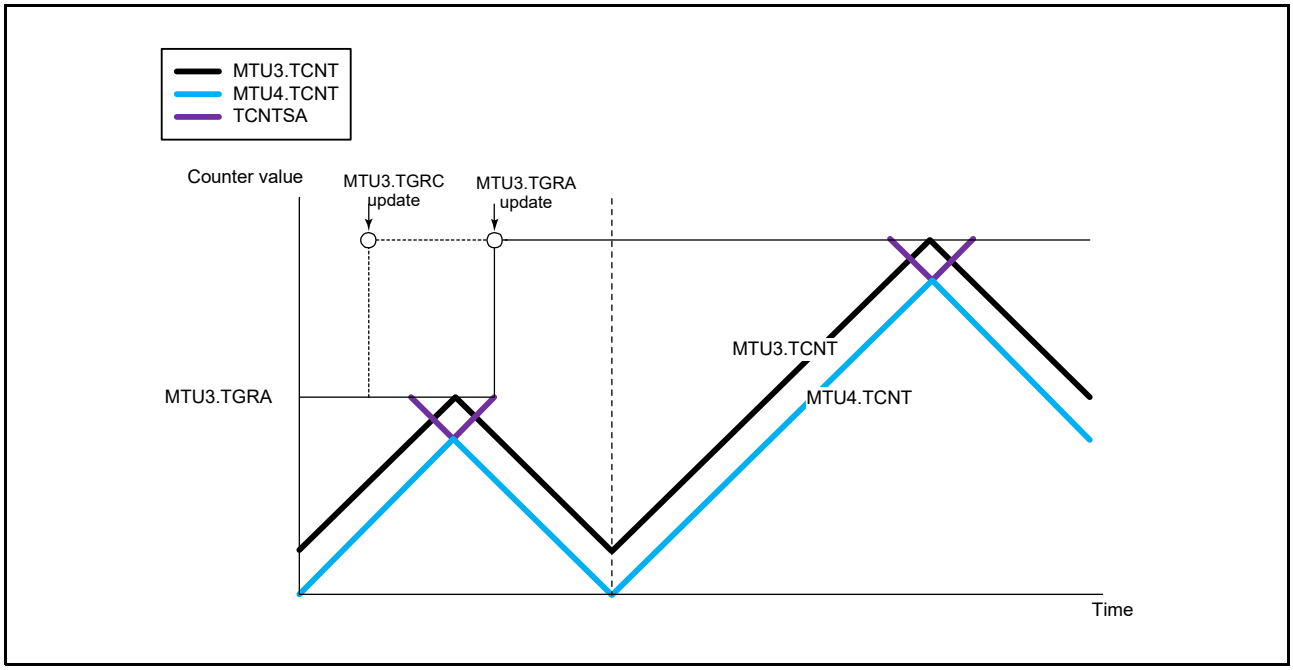


Figure 20.51 Example of PWM Period Updating (MTU3 and MTU4)

(h) Register Data Updating

The buffer registers are used to update the data in five compare registers for the PWM duty and PWM period in complementary PWM mode. The update data can be written to the buffer register at any time.

There is a temporary register between each of these registers and its buffer register. While subcounter TCNTSA (TCNTSB) is not counting, if buffer register data is updated, the temporary register value also changes. Data is not transferred from buffer registers to temporary registers while TCNTSA (TCNTSB) is counting; in this case, the value written to a buffer register is transferred after TCNTSA (TCNTSB) halts.

The temporary register value is transferred to the compare register at the data update timing set with MTU3.TMDR1.MD[3:0] (MTU6.TMDR1.MD[3:0]) bits. Figure 20.52 shows an example of data updating in complementary PWM mode (MTU3 and MTU4). This example shows the mode in which data is updated at both the counter crest and trough.

When updating buffer register data, be sure to write to MTU4.TGRD (MTU7.TGRD) at the end of the update. Data is transferred from buffer registers to the temporary registers simultaneously for all five registers after the write to MTU4.TGRD (MTU7.TGRD).

Even when not updating all five registers or when not updating the MTU4.TGRD (MTU7.TGRD) data, be sure to write to MTU4.TGRD (MTU7.TGRD) after writing data to the registers to be updated. In this case, the data written to MTU4.TGRD (MTU7.TGRD) should be the same as the data prior to the write operation.

Refer to section 20.3.8 (2) (s), Double Buffer Function in Complementary PWM Mode, for data updating when the double buffer function is used.

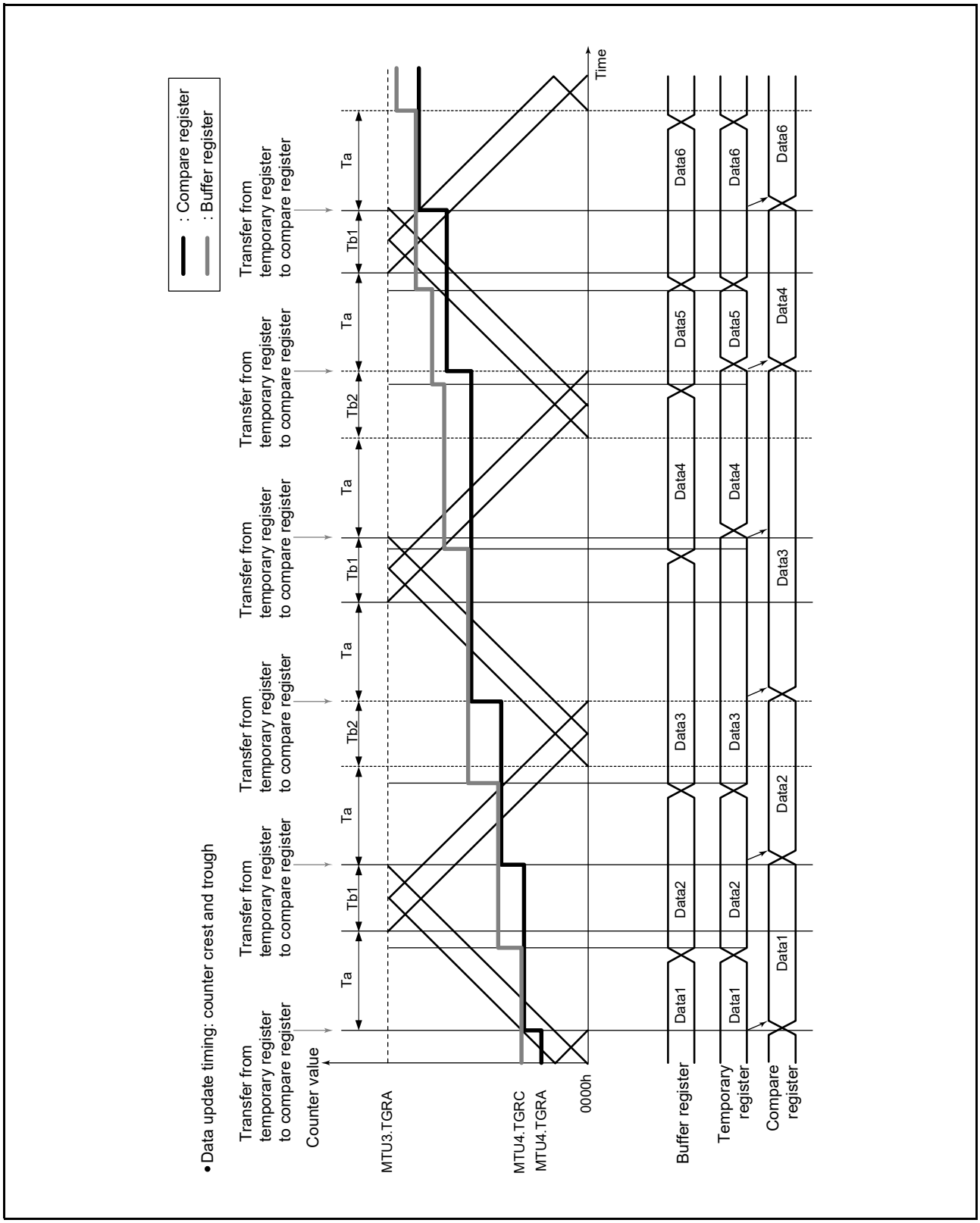


Figure 20.52 Example of Data Updating in Complementary PWM Mode (MTU3 and MTU4)

(i) Initial Output in Complementary PWM Mode

In complementary PWM mode, the initial output is determined by the setting of the OLSN and OLSP bits in the TOCR1A (TOCR1B) register or the OLS1N to OLS3N and OLS1P to OLS3P bits in the TOCR2A register (TOCR2B). This initial output is the non-active level of the PWM output and continues from when complementary PWM mode is set with the MTU3.TMDR1 (MTU6.TMDR1) until MTU4.TCNT (MTU7.TCNT) exceeds the value set in the TDDRA (TDDRB) register. Figure 20.53 shows an example of the initial output in complementary PWM mode.
An example of the waveform when the initial PWM duty ratio value is smaller than the TDDRA (TDDRB) value is shown in Figure 20.54.

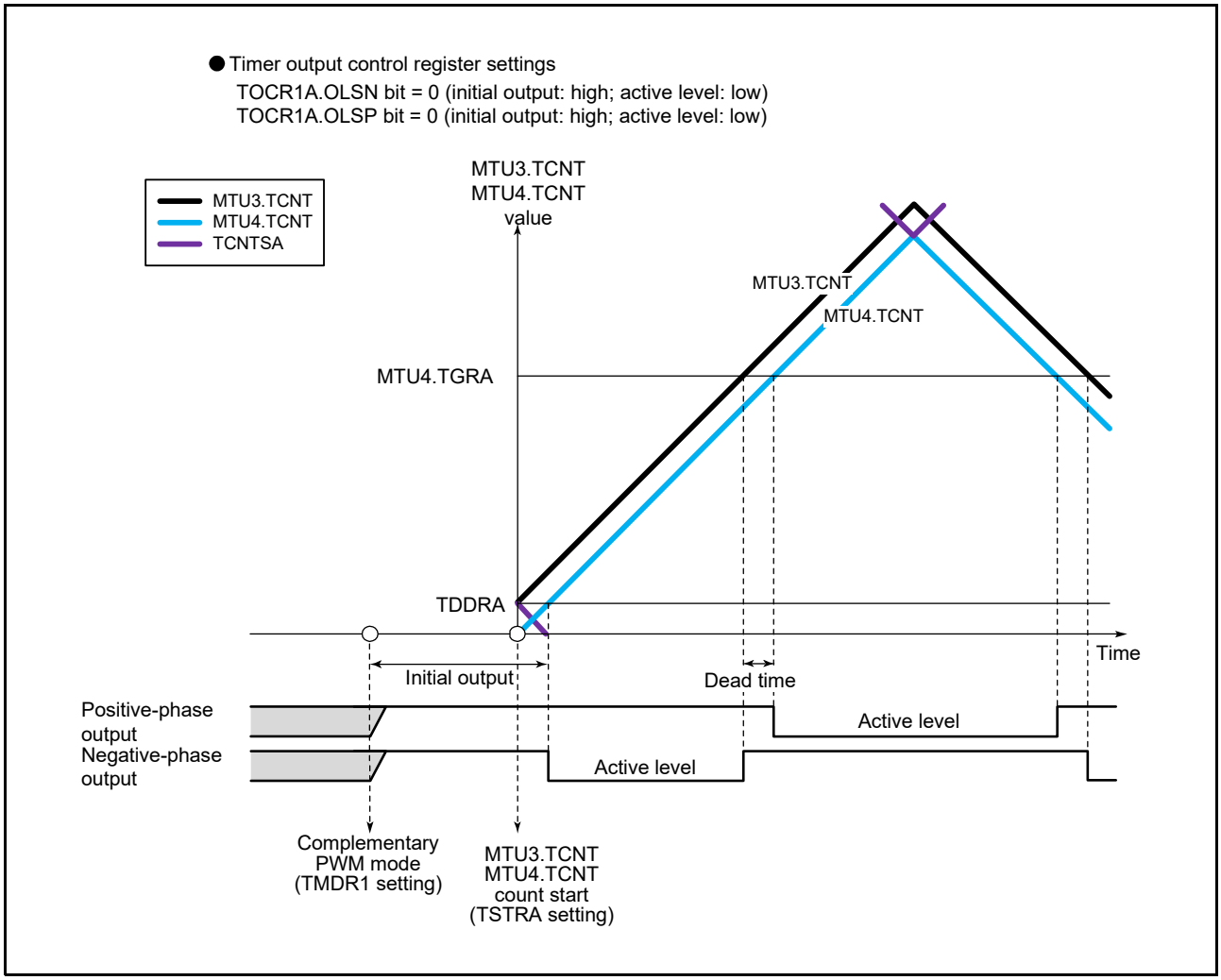


Figure 20.53 Example of Initial Output in Complementary PWM Mode (MTU3 and MTU4) (1))

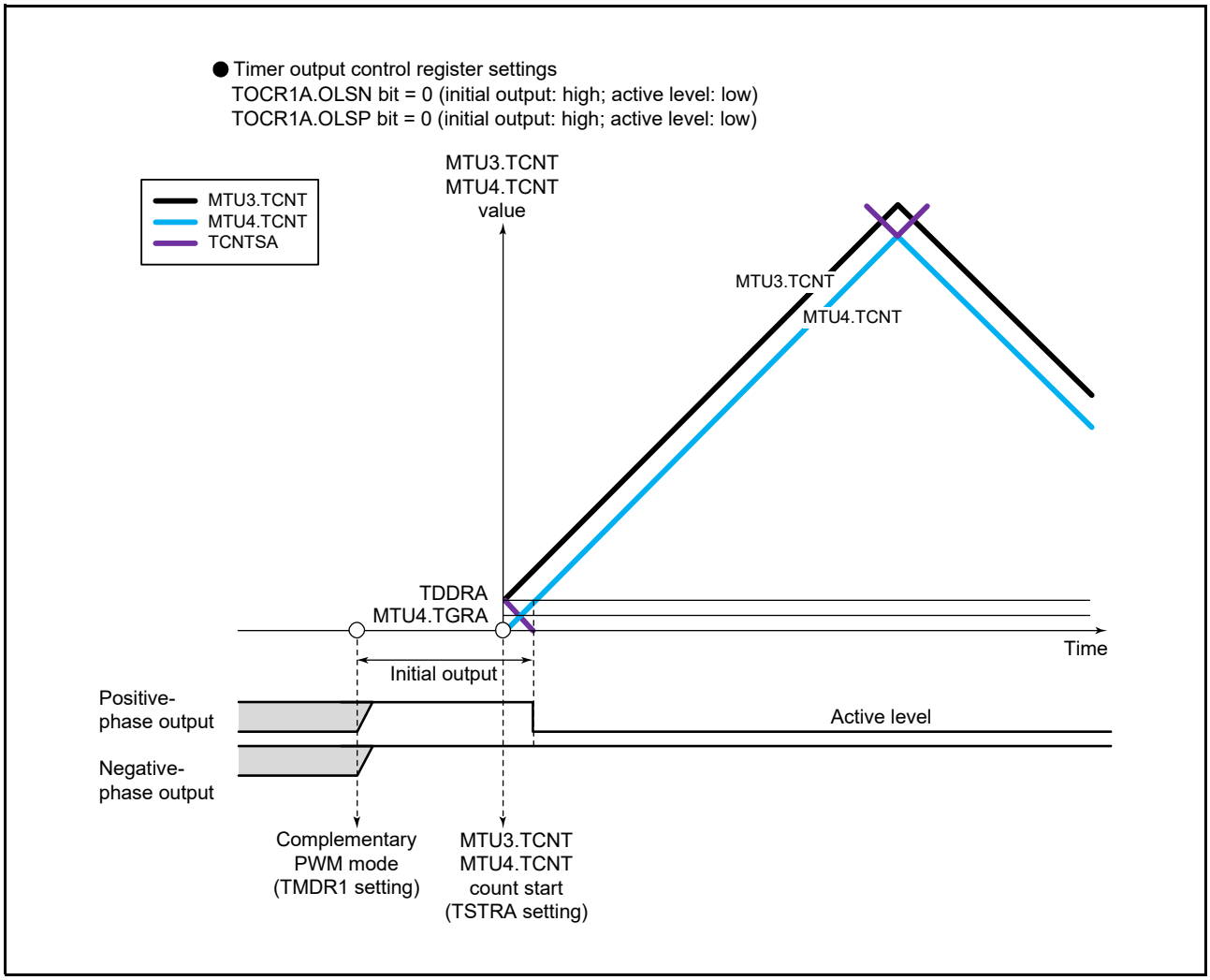


Figure 20.54 Example of Initial Output in Complementary PWM Mode (MTU3 and MTU4) (2)

(j) Method for Generating PWM Output in Complementary PWM Mode

In complementary PWM mode, six phases (three positive and three negative) PWM waveforms can be output. Dead time can be set for PWM waveforms to be output.

A PWM waveform is generated by output of the level selected in the timer output control register in the event of a compare match between a counter and a compare register. While TCNTSA (TCNTSB) is counting, the compare register and temporary register values are simultaneously compared to create consecutive PWM output from 0 to 100% duty ratio. The relative timing of turn-on and turn-off compare match occurrence may vary, but the compare match that turns off each phase takes precedence to secure the dead time and ensure that the positive-phase and negative-phase turn-on times do not overlap. Figure 20.55 to Figure 20.57 show examples of waveform generation in complementary PWM mode.

The positive-phase and negative-phase turn-off timing is generated by a compare match with the counter indicated by a solid line, and the turn-on timing is generated by a compare match with the counter indicated by a dotted line, which operates with a delay equal to the dead time behind the counter indicated by a solid line. In the T1 period, compare match a that turns off the negative phase has the highest priority, and compare matches before a are ignored. In the T2 period, compare match c that turns off the positive phase has the highest priority, and compare matches before c are ignored.

In most cases, compare matches occur in the order a → b → c → d (or c → d → a' → b') as shown in Figure 20.55.

If compare matches deviate from the a → b → c → d order, since the time for which the negative phase is off is shorter than twice the dead time, the positive phase is not turned on. If compare matches deviate from the c → d → a' → b' order, since the time for which the positive phase is off is shorter than twice the dead time, the negative phase is not turned on.

As shown in Figure 20.56, if compare match c follows compare match a before compare match b, compare match b is ignored and the negative phase is turned on by compare match d. This is because turning off the positive phase has priority due to the occurrence of compare match c (positive-phase off timing) before compare match b (positive-phase on timing) (consequently, the waveform does not change because the positive phase goes from off to off).

Similarly, in the example in Figure 20.57, turning off the negative phase has priority due to the occurrence of compare match a' (negative-phase off timing) before compare match d (negative-phase on timing). As a result, the negative phase is not turned on.

Thus, in complementary PWM mode, compare matches at turn-off timings take precedence, and turn-on timing compare matches that occur before a turn-off timing compare match are ignored.

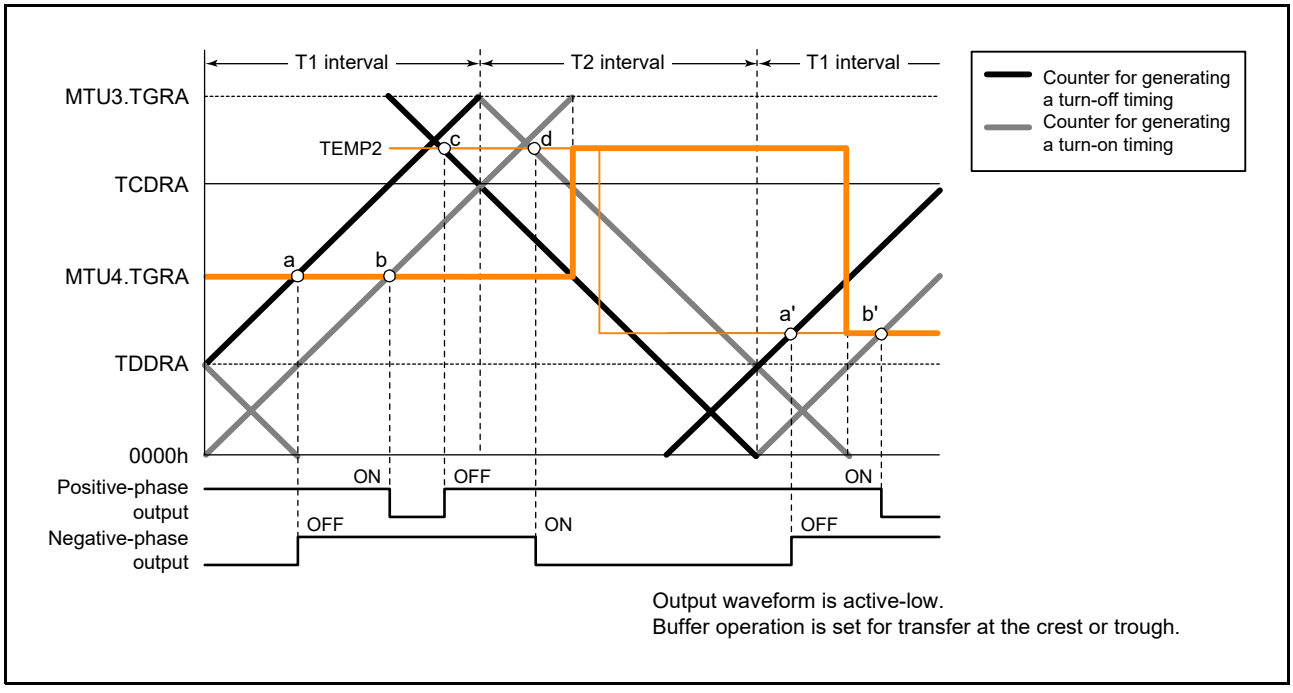


Figure 20.55 Example of Waveform Output in Complementary PWM Mode (MTU3 and MTU4) (1)

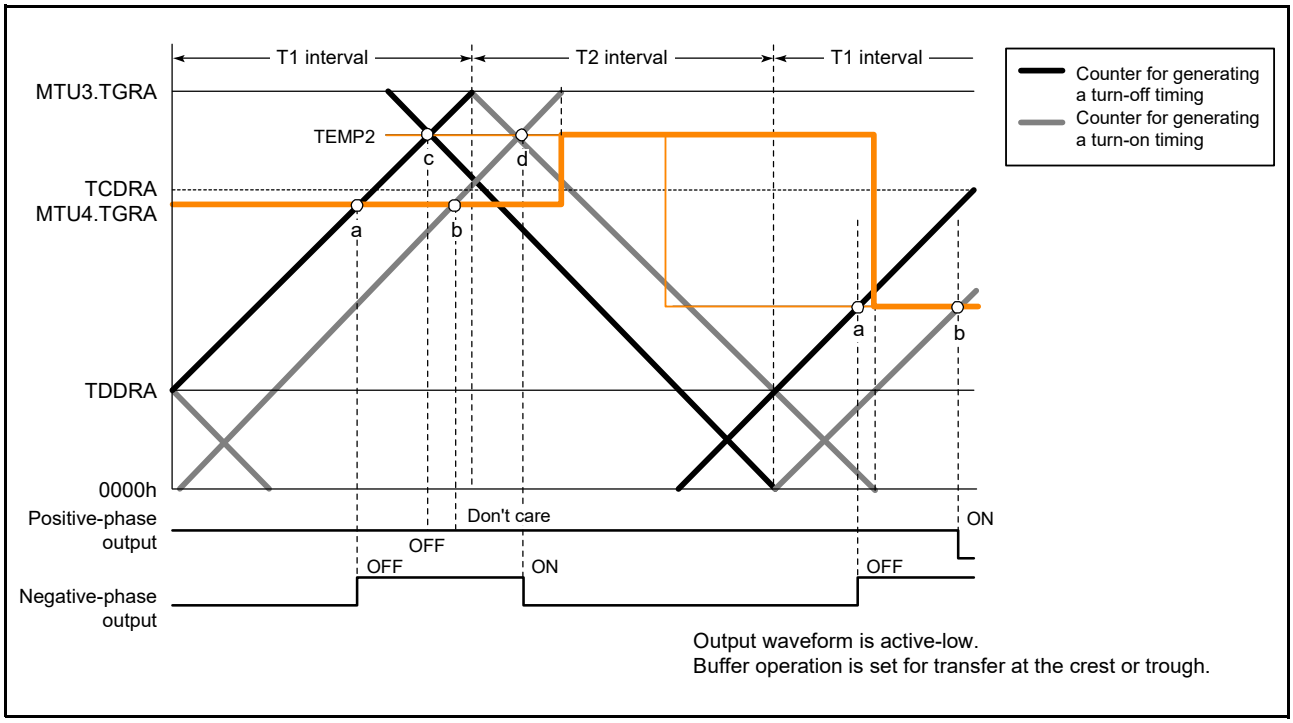


Figure 20.56 Example of Waveform Output in Complementary PWM Mode (MTU3 and MTU4) (2)

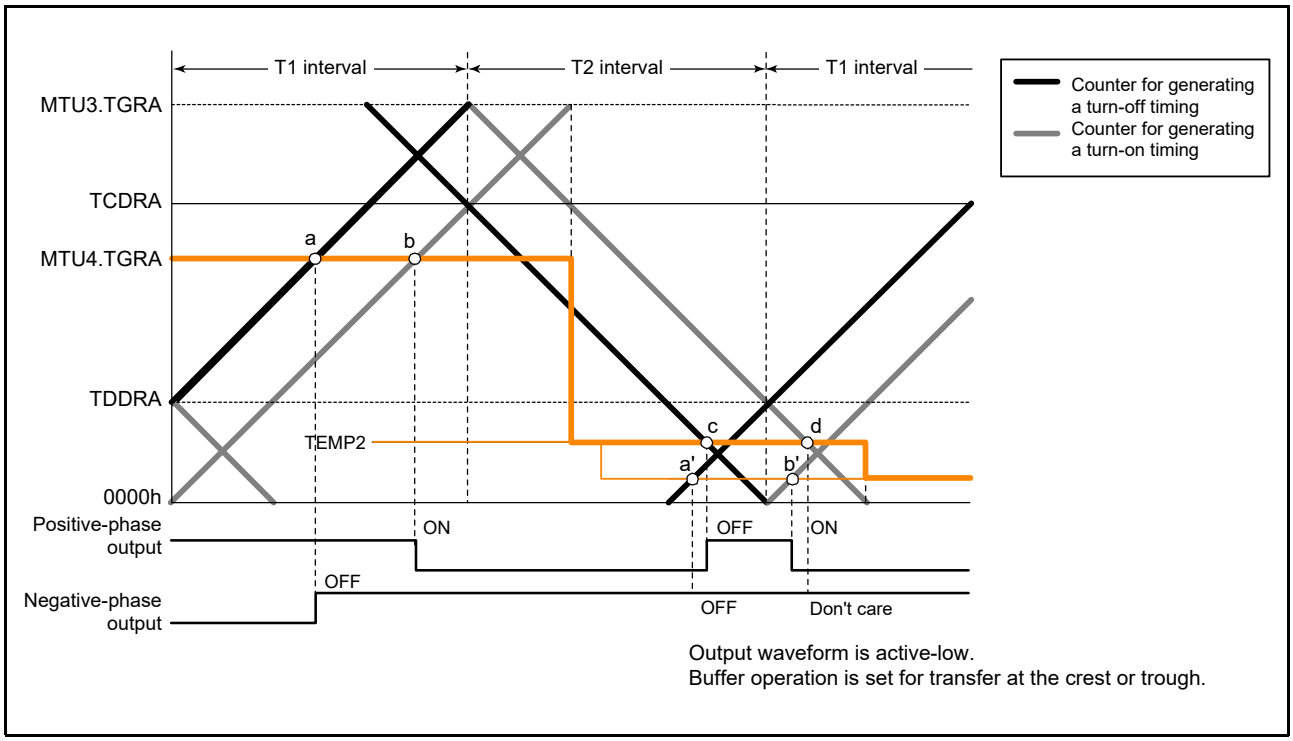


Figure 20.57 Example of Waveform Output in Complementary PWM Mode (MTU3 and MTU4) (3)

(k) 0% and 100% Duty Ratio Output in Complementary PWM Mode

In complementary PWM mode, 0% and 100% duty PWM output can be output as required. Figure 20.58 to Figure 20.62 show output examples.

A 100% duty waveform is output when the compare register value is set to 0000h. The waveform in this case has a positive phase with a 100% on-state. A 0% duty waveform is output when the compare register value is set to the same value as MTU3.TGRA (MTU6.TGRA). The waveform in this case has a positive phase with a 100% off-state.

Turn-on and turn-off compare matches occur simultaneously, but if a turn-on compare match and turn-off compare match for the same phase occur simultaneously, both compare matches are ignored and the waveform does not change.

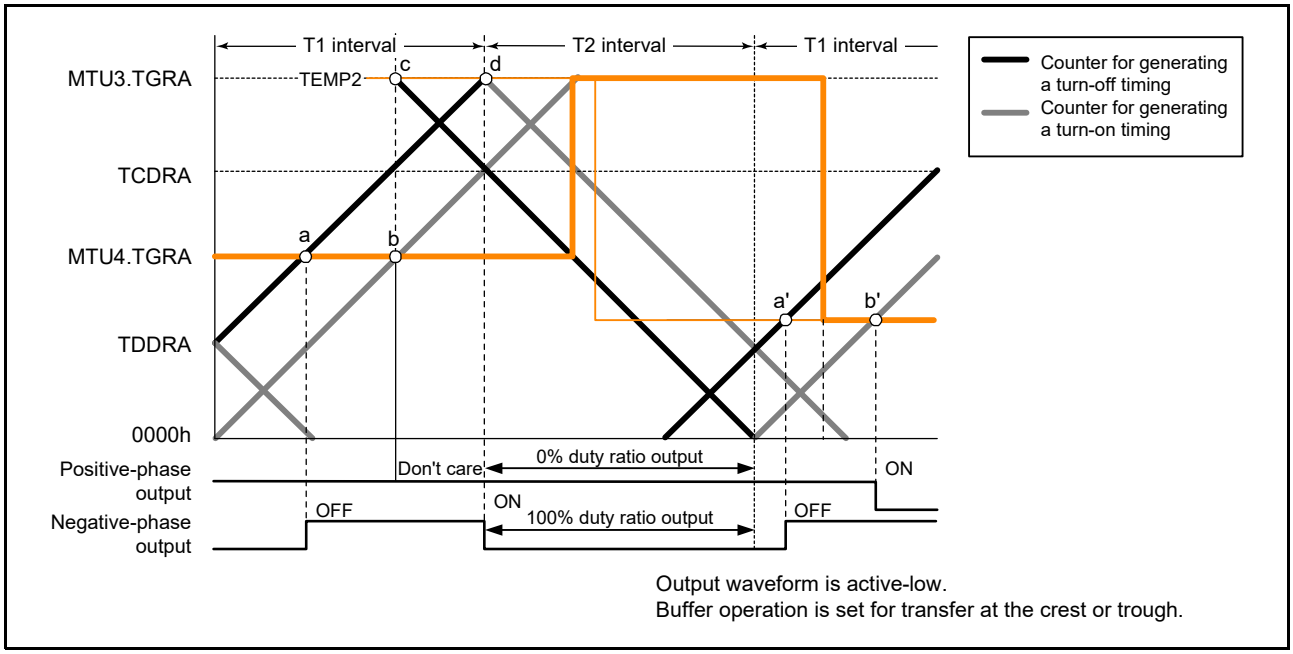


Figure 20.58 Example of 0% and 100% Waveform Output in Complementary PWM Mode (MTU3 and MTU4) (1)

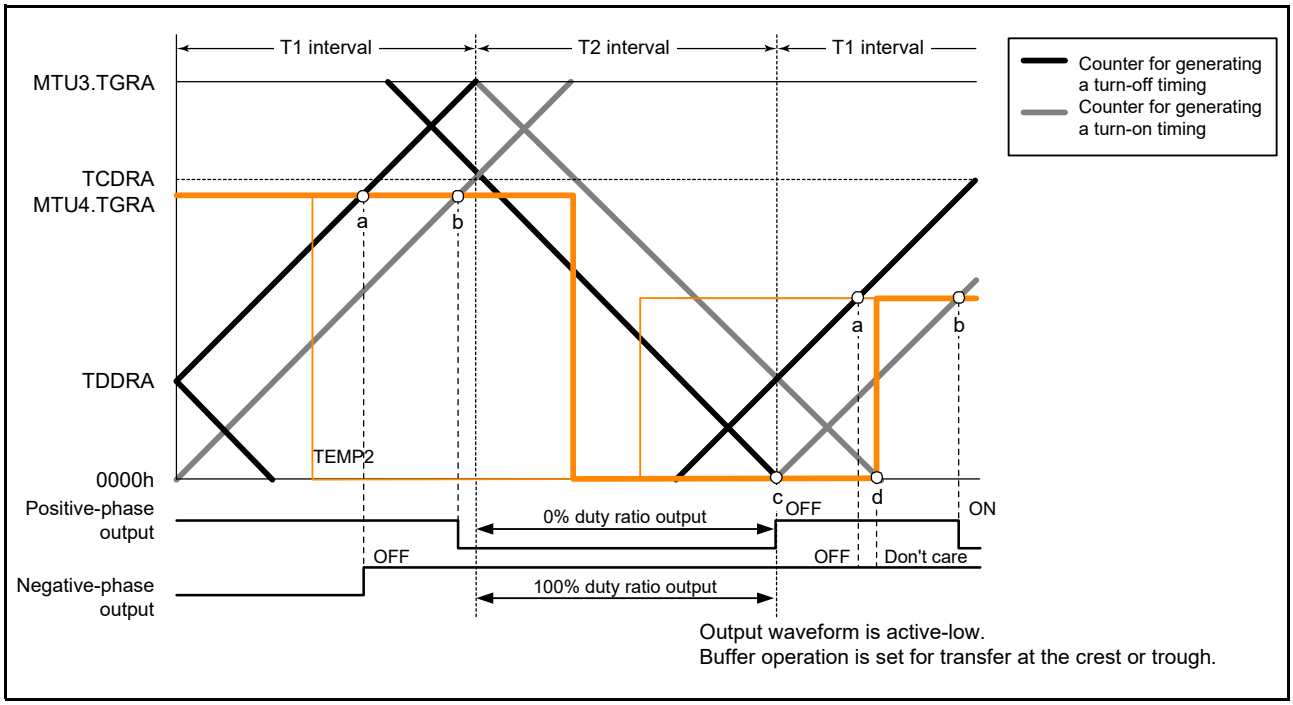


Figure 20.59 Example of 0% and 100% Waveform Output in Complementary PWM Mode (MTU3 and MTU4) (2)

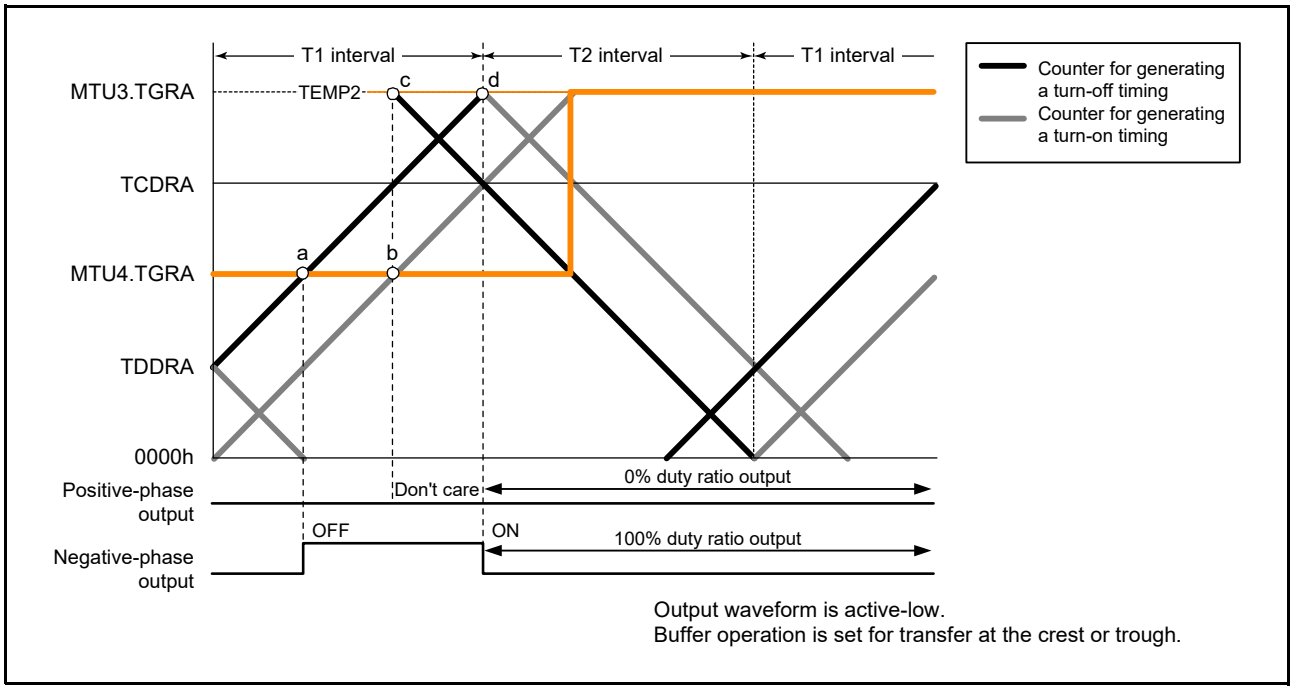


Figure 20.60 Example of 0% and 100% Waveform Output in Complementary PWM Mode (MTU3 and MTU4) (3)

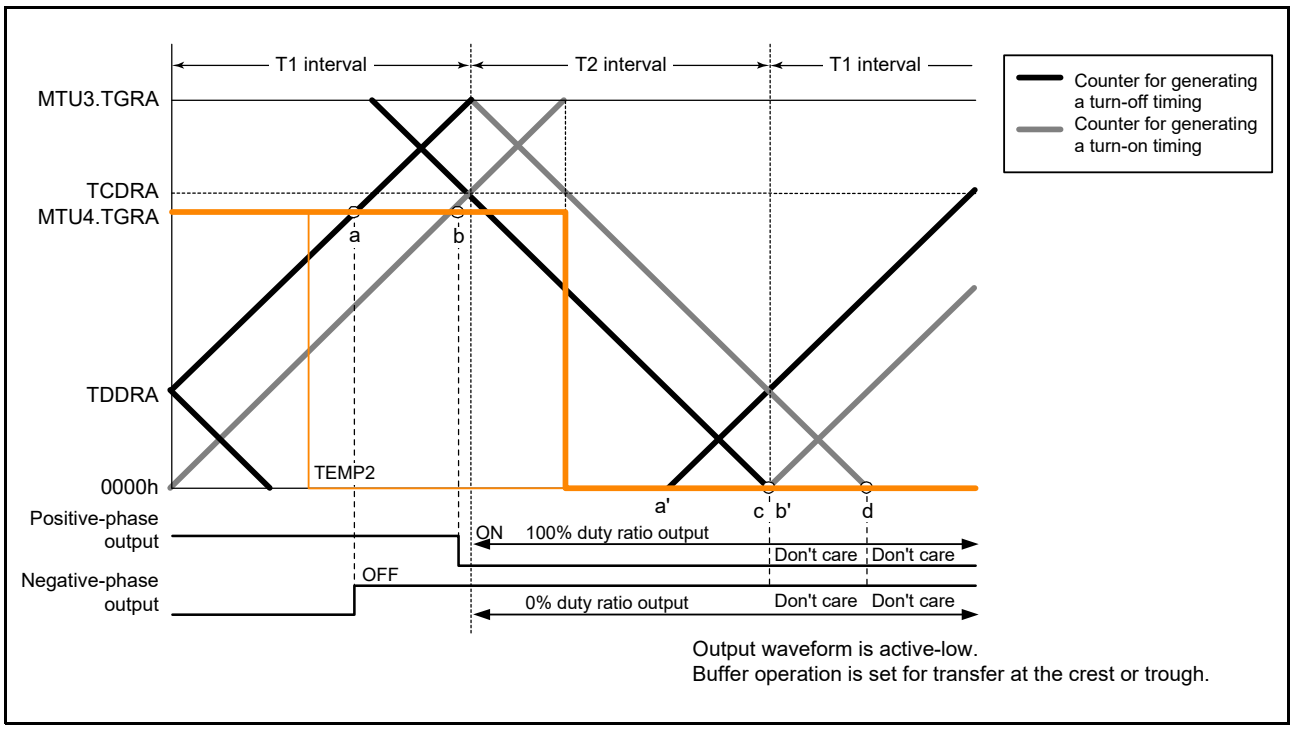


Figure 20.61 Example of 0% and 100% Waveform Output in Complementary PWM Mode (MTU3 and MTU4) (4)

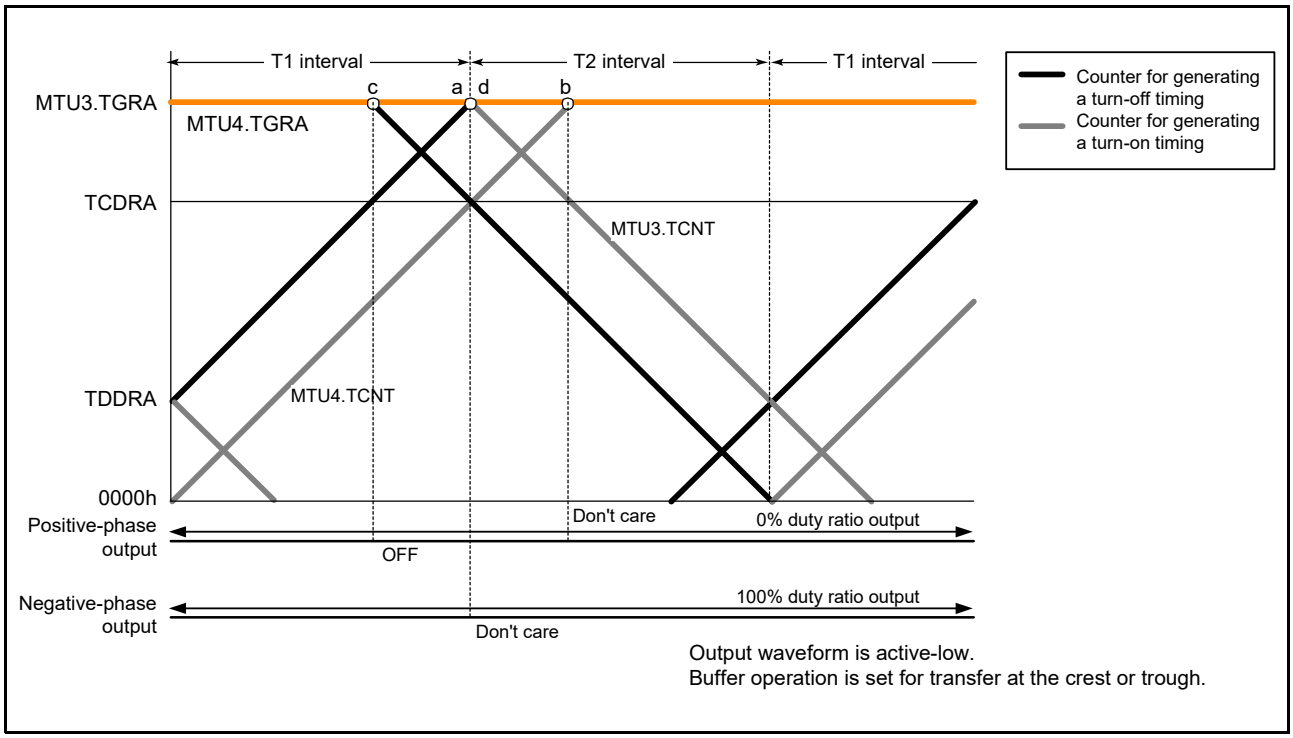


Figure 20.62 Example of 0% and 100% Waveform Output in Complementary PWM Mode (MTU3 and MTU4) (5)

(l) Toggle Output Synchronized with PWM Period

In complementary PWM mode, toggle output from the PWM output pin in synchronization with the PWM period can be enabled by setting the PSYE bit in the TOCR1A (TOCR1B) register to 1. An example of a toggle output waveform is shown in Figure 20.63.

This output is toggled by a compare match between MTU3.TCNT and MTU3.TGRA (MTU6.TCNT and MTU6.TGRA) and a compare match between MTU4.TCNT (MTU7.TCNT) and 0000h.

The MTIOC3A (MTIOC6A) pin is assigned for this toggle output. The initial output is high-level output.

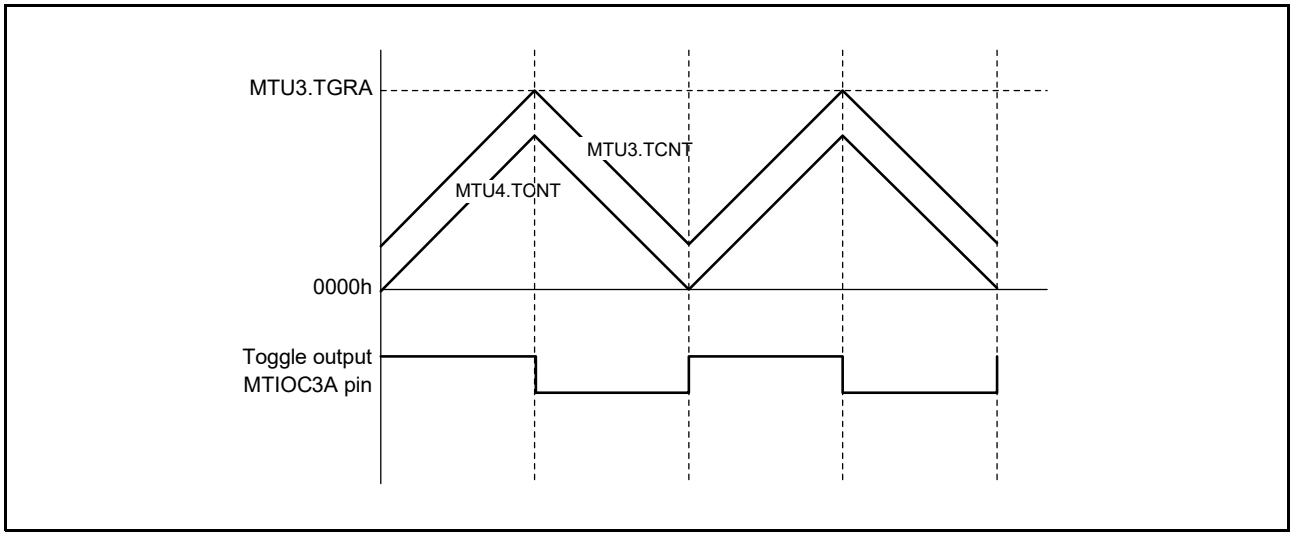


Figure 20.63 Example of Toggle Output Waveform Synchronized with PWM Output (MTU3 and MTU4)

(m) Counter Clearing by Another Channel

In complementary PWM mode, MTU3.TCNT, MTU4.TCNT, and TCNTSA (MTU6.TCNT, MTU7.TCNT, and TCNTSB) can be cleared by another channel source when a mode for synchronization with another channel is specified through the TSYRA (TSYRB) register and synchronous clearing is selected with MTU3.TCR.CCLR[2:0] (MTU6.TCR.CCLR[2:0]) bits.

Figure 20.64 illustrates an example of this operation.

Use of this function enables a counter to be cleared and restarted through an external signal.

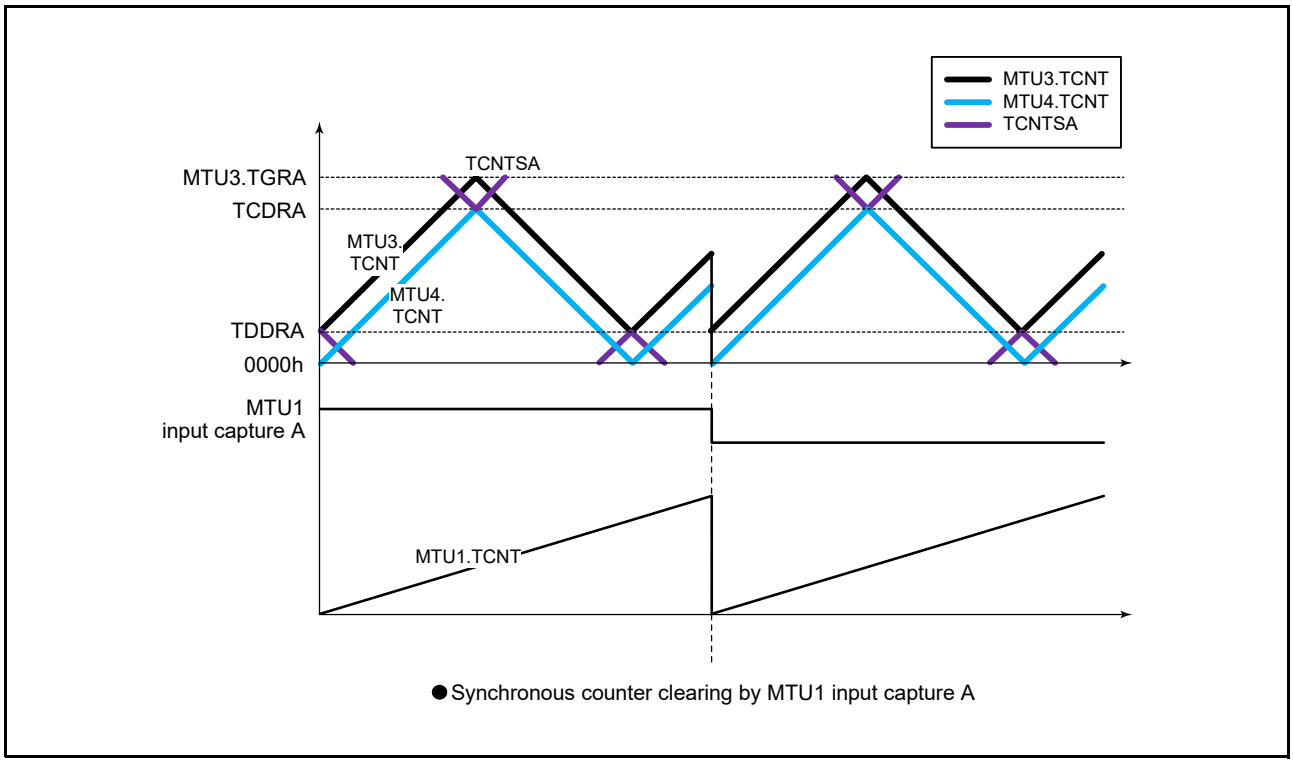


Figure 20.64 Counter Clearing Synchronized with Another Channel (MTU3 and MTU4)

(n) Output Waveform Control at Synchronous Counter Clearing in Complementary PWM Mode

Setting the WRE bit in TWCRA (TWCRB) to 1 suppresses initial output when synchronous counter clearing occurs in the Tb interval (Tb2 interval) at the trough in complementary PWM mode and controls abrupt change in duty cycle at synchronous counter clearing.

Initial output suppression through the WRE bit = 1 is applicable only when synchronous clearing occurs in the Tb2 interval as indicated by (10) or (11) in Figure 20.65. When synchronous clearing occurs outside that interval, the initial value specified by the OLSN and OLSP bits in TOCR1A (TOCR1B) is output. Even in the Tb2 interval, if synchronous clearing occurs in the initial value output period (indicated by (1) in Figure 20.65) immediately after the counters start operation, initial value output is not suppressed.

This function can be used in both channel combinations of MTU3 and MTU4, and MTU6 and MTU7. In MTU3 and MTU4, synchronous clearing in any of MTU0 to MTU2 can cause counter clearing; in MTU6 and MTU7,compare match or input capture in any of MTU0 to MTU2 can cause counter clearing.

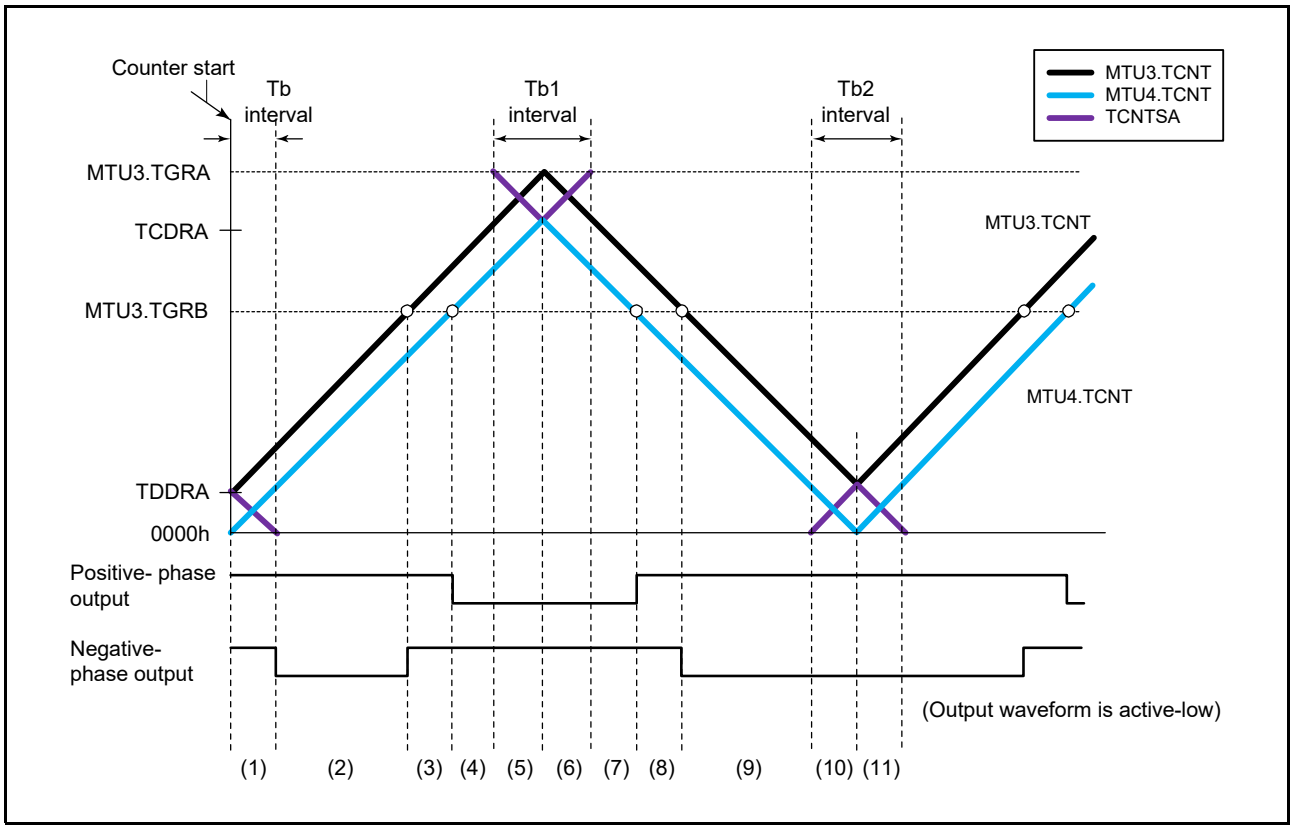


Figure 20.65 Timing for Synchronous Counter Clearing (MTU3 and MTU4)

- Example of Procedure for Setting Output Waveform Control at Synchronous Counter Clearing in Complementary PWM Mode.

An example of the procedure for setting output waveform control at synchronous counter clearing in complementary PWM mode is shown in Figure 20.66.

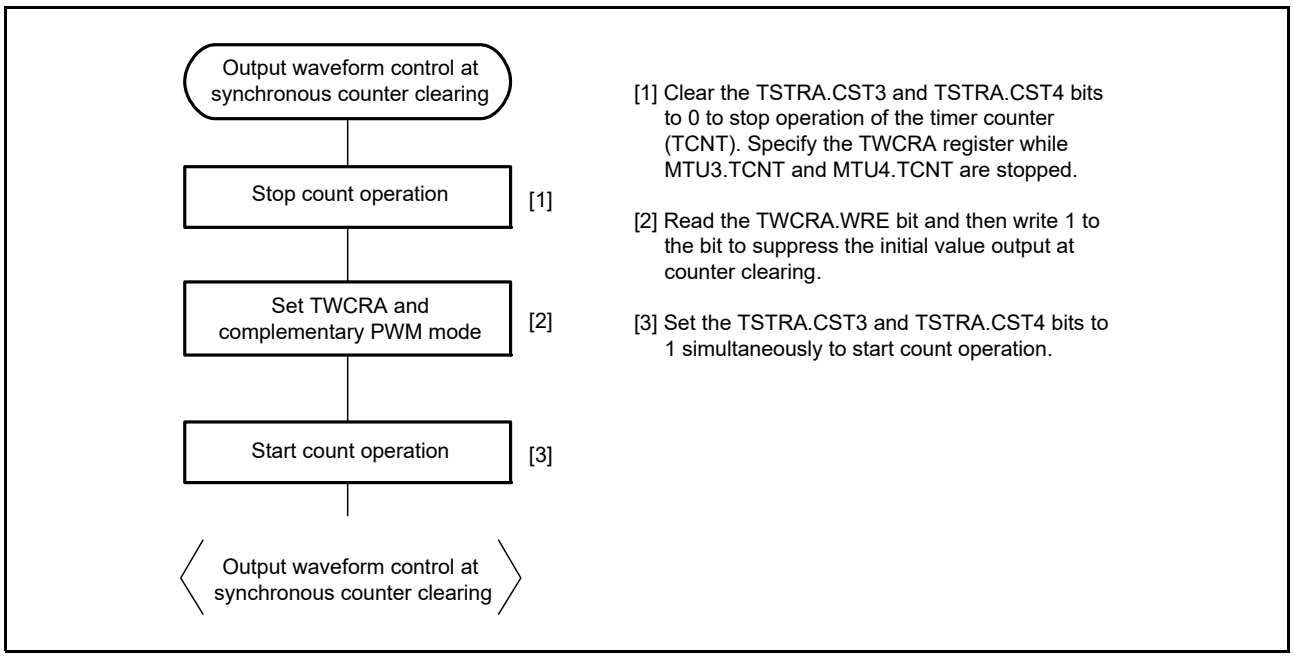


Figure 20.66 Example of Procedure for Setting Output Waveform Control at Synchronous Counter Clearing in Complementary PWM Mode (MTU3 and MTU4)

- Examples of Output Waveform Control at Synchronous Counter Clearing in Complementary PWM Mode

Figure 20.67 to Figure 20.70 show examples of output waveform control in which MTU3 and MTU4 operate in complementary PWM mode and synchronous counter clearing is generated while the WRE bit in TWCRA is set to 1. In the examples shown in Figure 20.67 to Figure 20.70, synchronous counter clearing occurs at timing (3), (6), (8), and (11) shown in Figure 20.65, respectively.

In MTU6 and MTU7, these examples are equivalent to the cases when MTU6 and MTU7 operate in complementary PWM mode and synchronous counter clearing is generated while the SCC bit is cleared to 0 and the WRE bit is set to 1 in TWCRB.

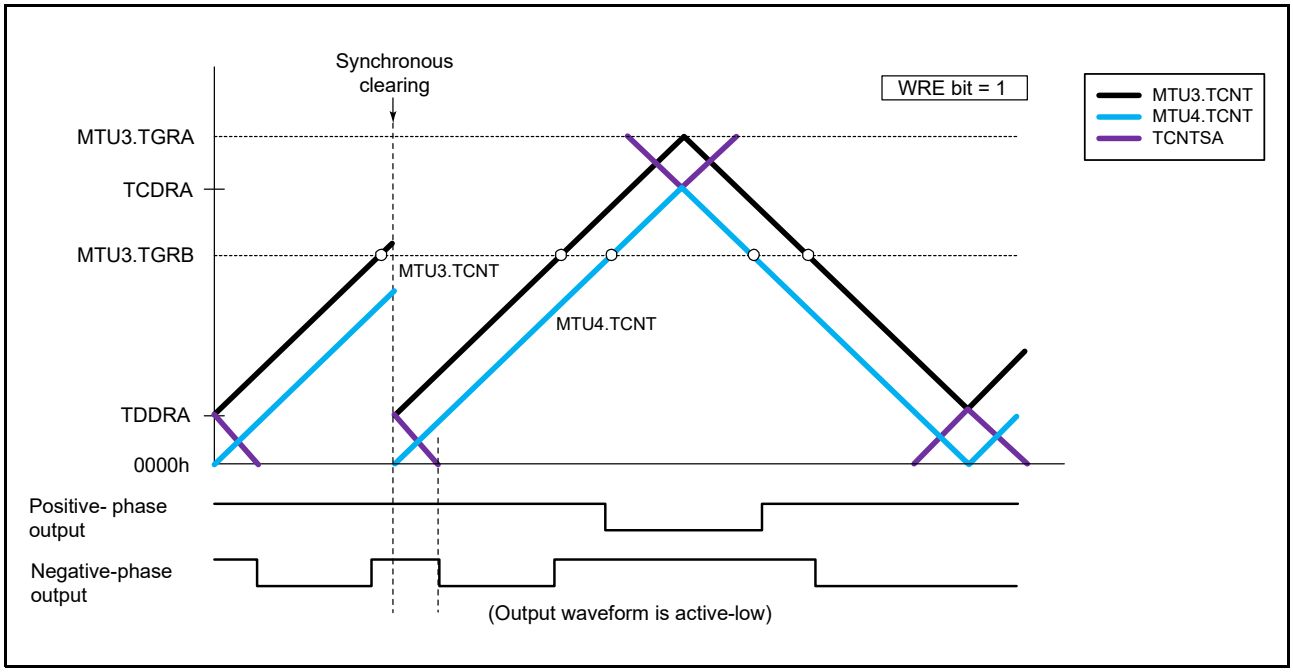


Figure 20.67 Example of Synchronous Clearing in Dead Time during Up-Counting (Timing (3) in Figure 20.65; TWCRA.WRE Bit is 1)

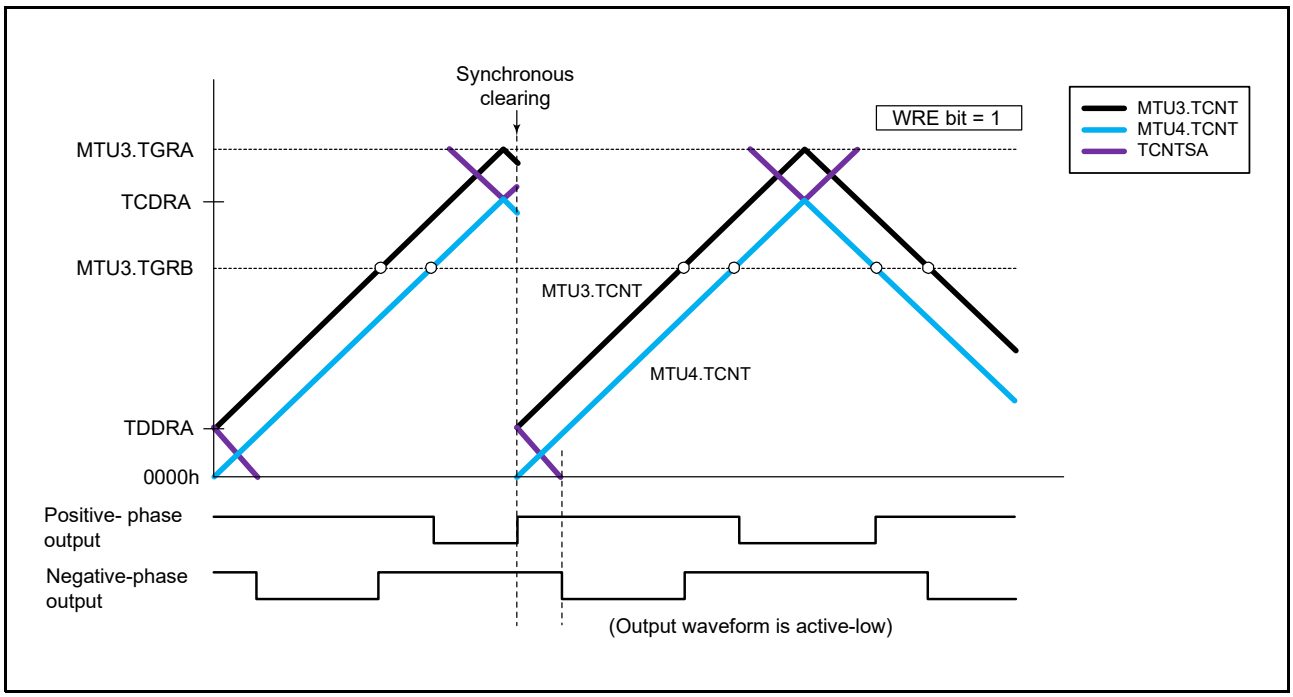


Figure 20.68 Example of Synchronous Clearing in Tb1 interval (Timing (6) in Figure 20.65; TWCRA.WRE Bit is 1)

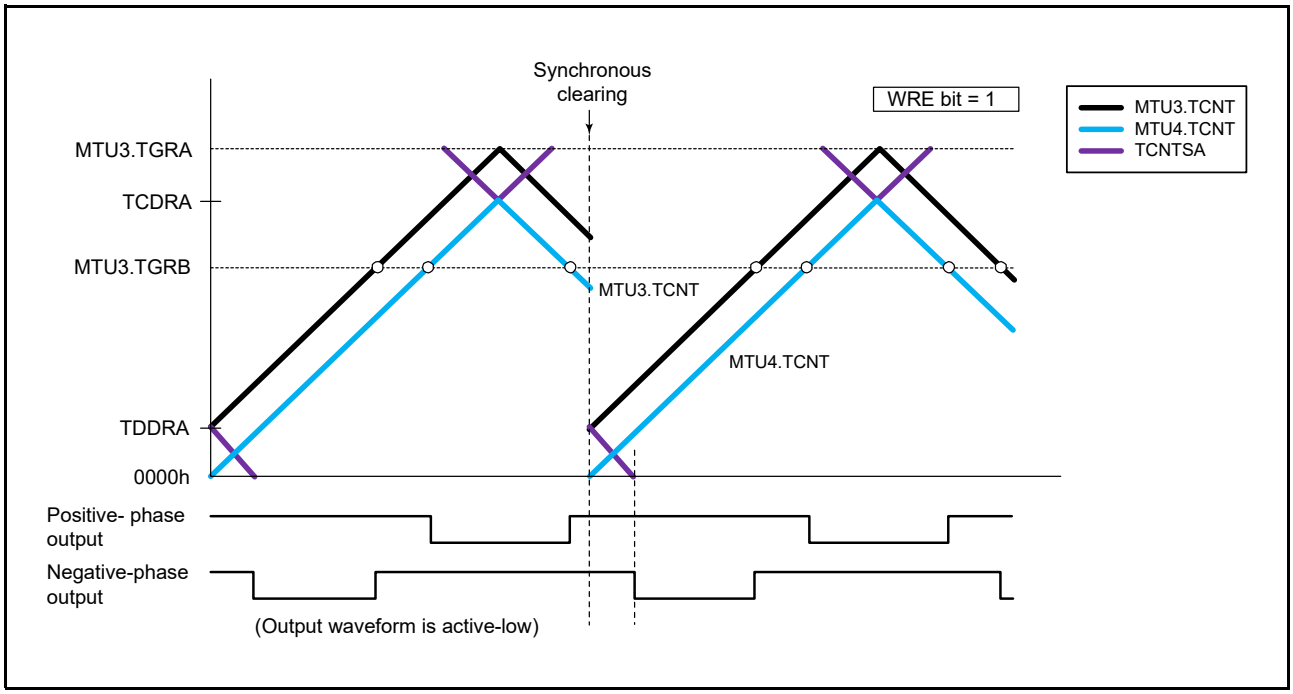


Figure 20.69 Example of Synchronous Clearing in Dead Time during Down-Counting (Timing (8) in Figure 20.65; TWCRA.WRE Bit is 1)

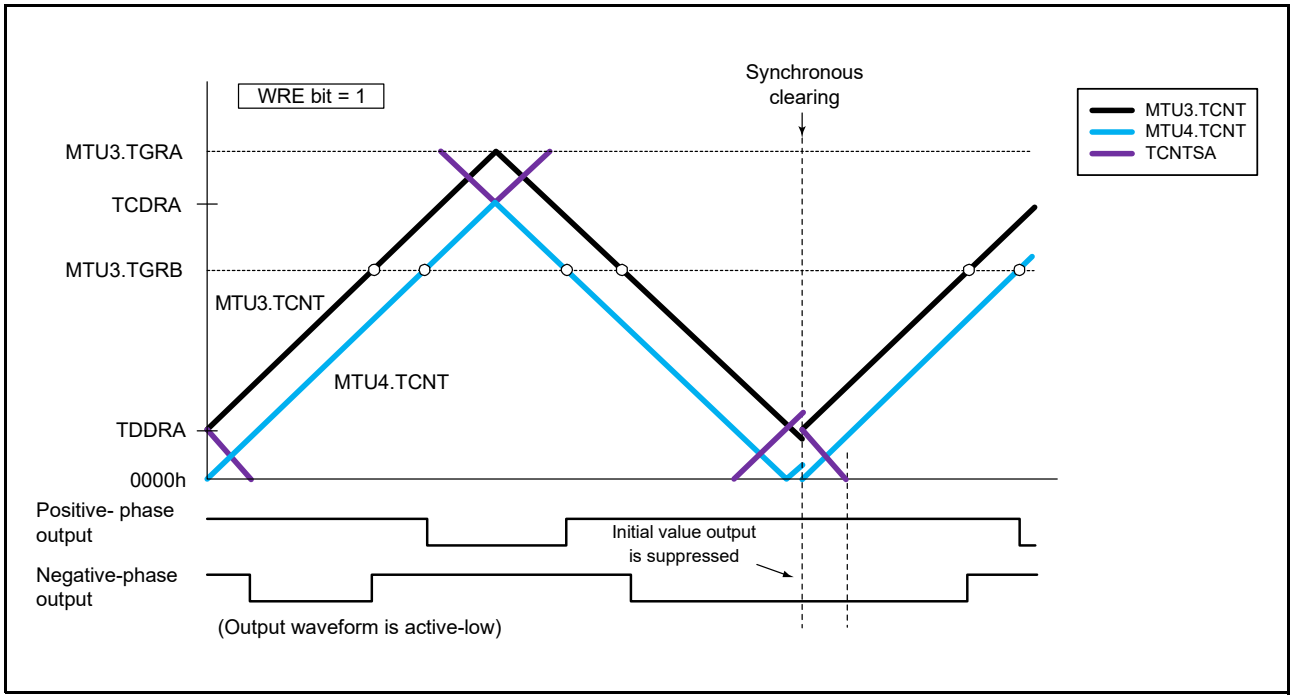


Figure 20.70 Example of Synchronous Clearing in Tb2 interval (Timing (11) in Figure 20.65; TWCRA.WRE Bit is 1)

(o) Suppressing Synchronous Counter Clearing for MTU0 to MTU2, and MTU6 and MTU7

In MTU6 and MTU7, setting the SCC bit in TWCRB to 1 suppresses synchronous counter clearing caused by MTU0 to MTU2.

Synchronous counter clearing is suppressed only within the interval shown in Figure 20.71. When using this function, MTU6 and MTU7 should be set to complementary PWM mode.

For details of synchronous clearing caused by MTU0 to MTU2, refer to section 20.3.10 (2), Synchronous Counter Clearing for MTU6 and MTU7.

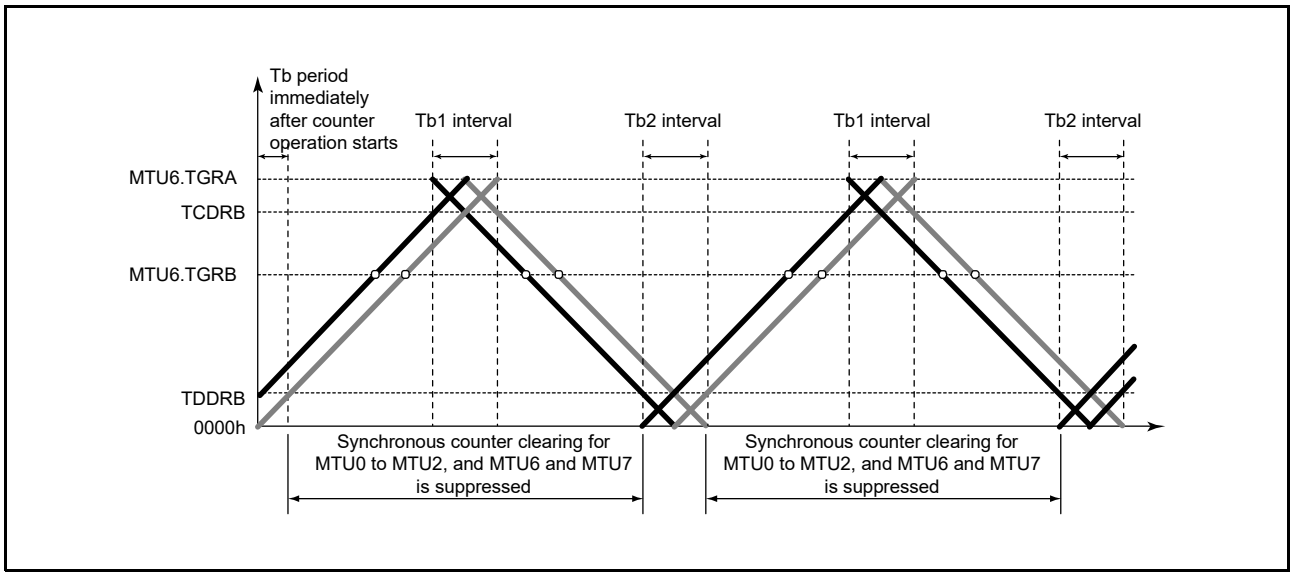


Figure 20.71 Synchronous Clearing-Suppressed Interval Specified by TWCRB.SCC Bit for MTU0 to MTU2, and MTU6 and MTU7

- Example of Procedure for Suppressing Synchronous Counter Clearing for MTU0 to MTU2, and MTU6 and MTU7

An example of the procedure for suppressing synchronous counter clearing for MTU0 to MTU2, and MTU6 and MTU7 is shown in Figure 20.72.

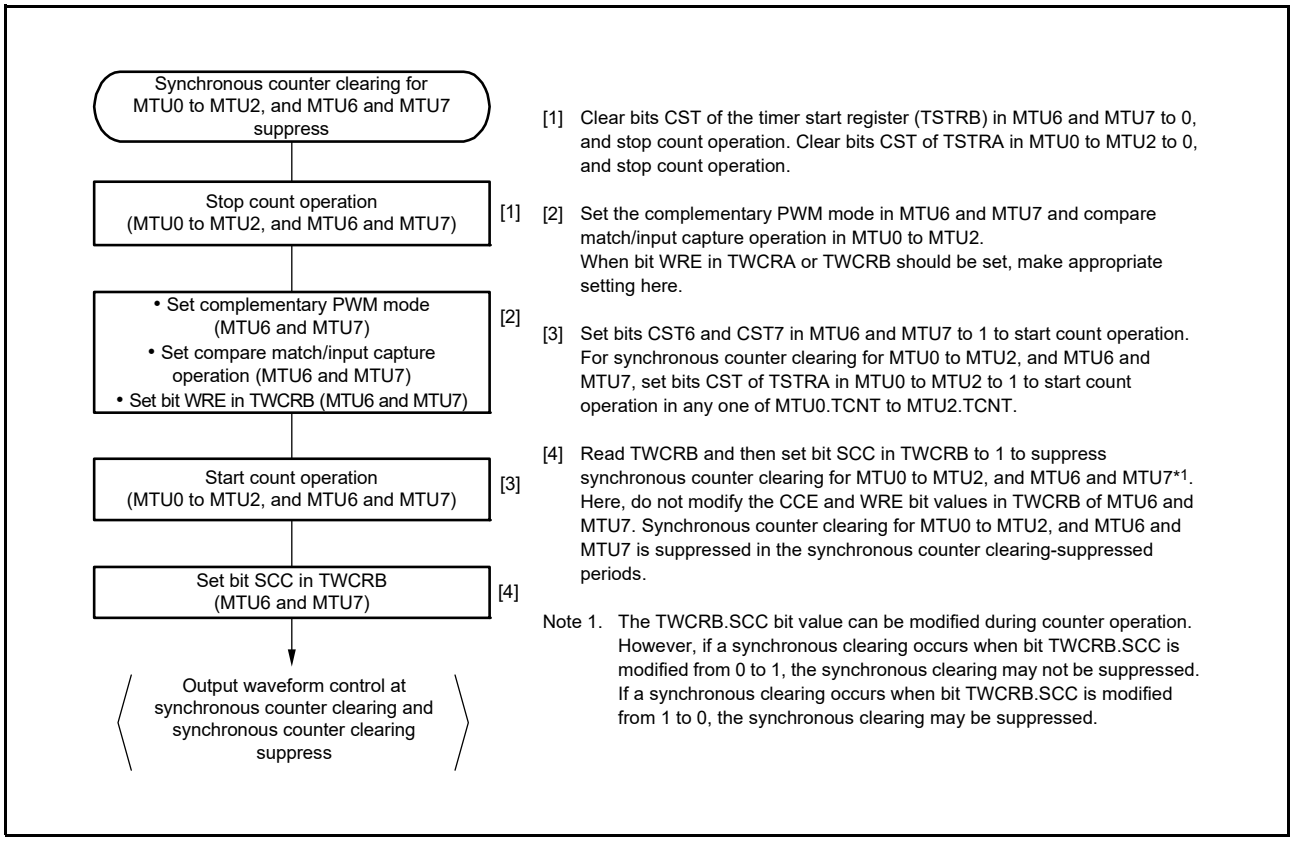


Figure 20.72 Example of Procedure for Suppressing Synchronous Counter Clearing for MTU0 to MTU2, and MTU6 and MTU7

- Examples of Suppression of Synchronous Counter Clearing for MTU 0 to MTU2, and MTU6 and MTU7

Figure 20.73 to Figure 20.76 show examples of operation in which MTU6 and MTU7 operate in complementary PWM mode and synchronous counter clearing for MTU 0 to MTU2, and MTU6 and MTU7 is suppressed by setting the SCC bit in TWCRB in MTU6 and MTU7 to 1. In the examples shown in Figure 20.73 to Figure 20.76, synchronous counter clearing occurs at timing (3), (6), (8), and (11) shown in Figure 20.65, respectively. In these examples, the WRE bit in TWCRB in MTU6 and MTU7 is set to 1.

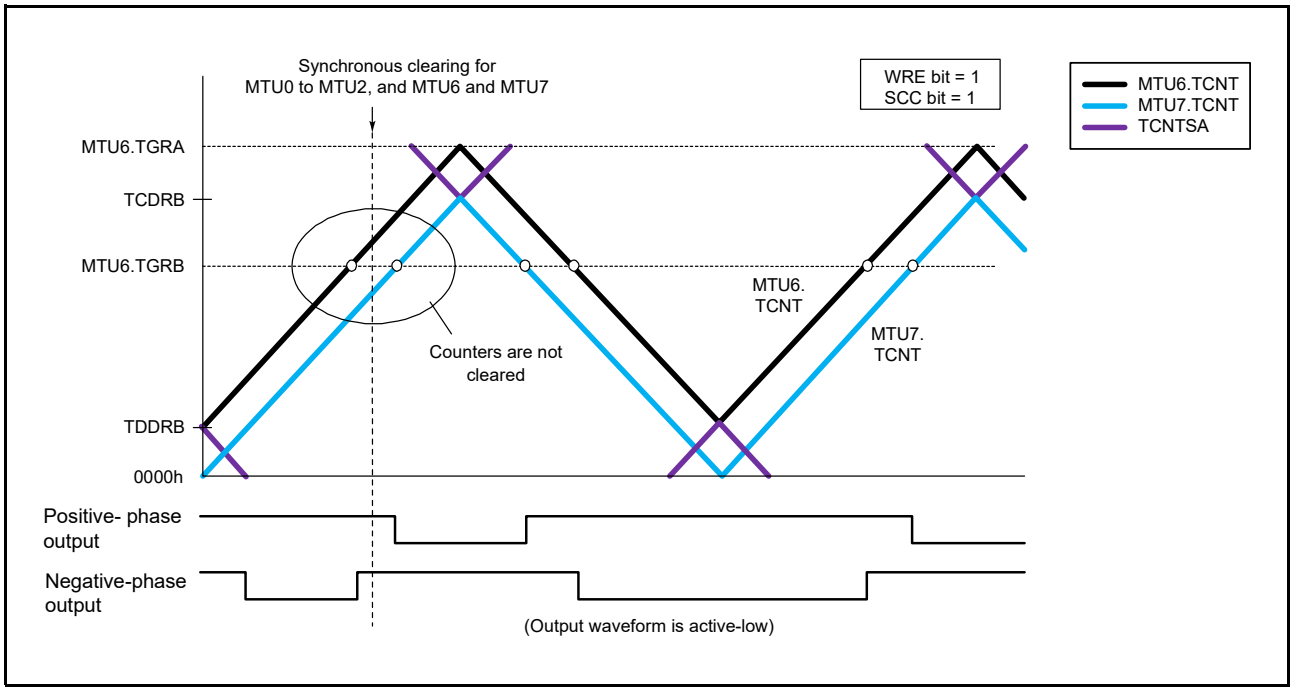


Figure 20.73 Example of Synchronous Clearing in Dead Time during Up-Counting (Timing (3) in Figure 20.65; TWCRB.WRE Bit is 1 and SCC Bit is 1 in MTU6 and MTU7)

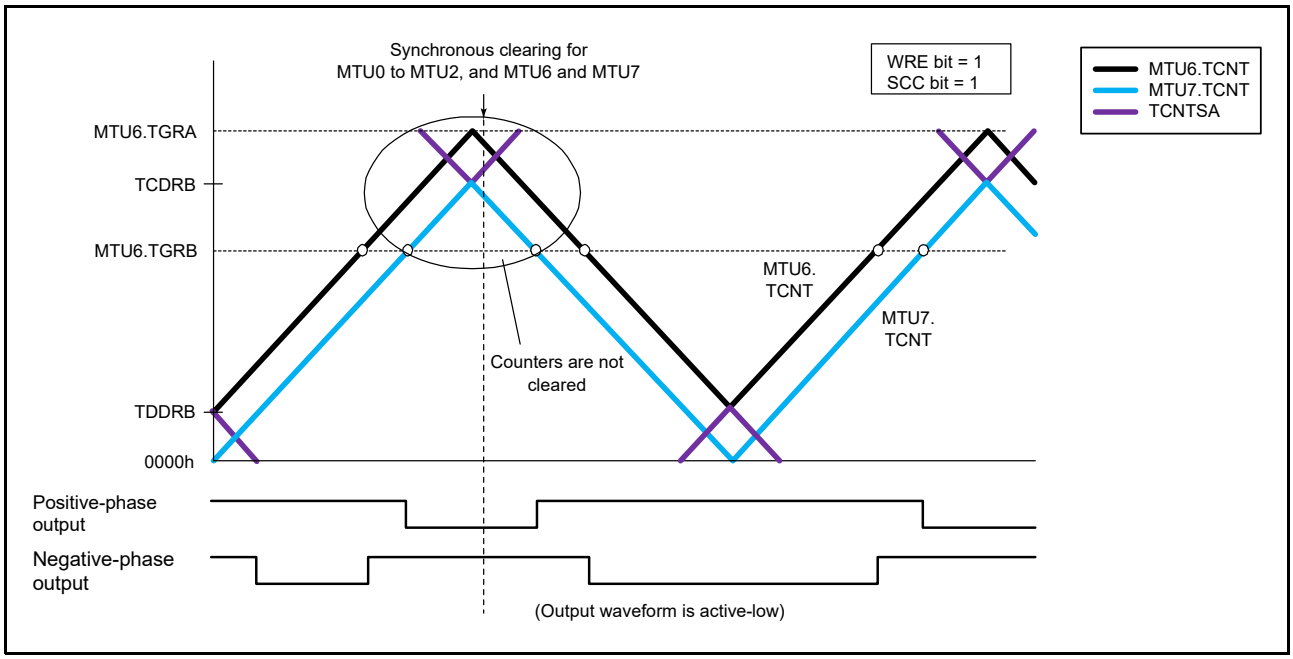


Figure 20.74 Example of Synchronous Clearing in Tb1 interval (Timing (6) in Figure 20.65; TWCRB.WRE Bit is 1 and SCC Bit is 1 in MTU6 and MTU7)

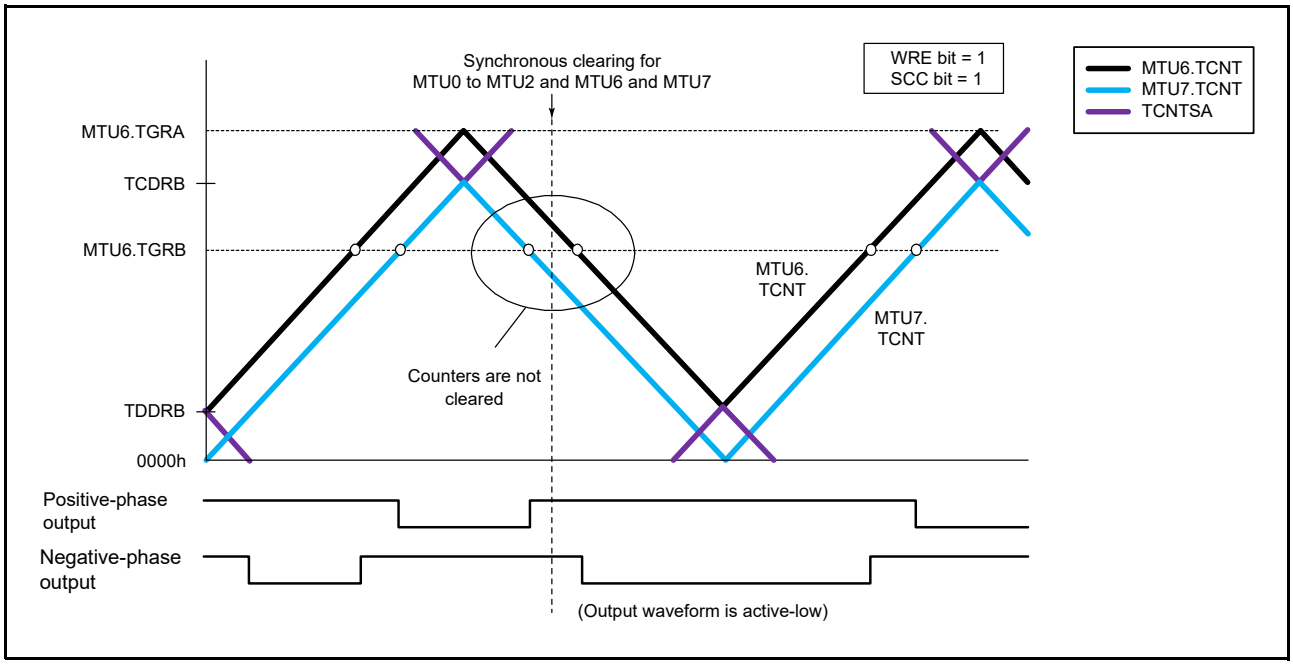


Figure 20.75 Example of Synchronous Clearing in Dead Time during Down-Counting (Timing (8) in Figure 20.65; TWCRB.WRE Bit is 1 and SCC Bit is 1 in MTU6 and MTU7)

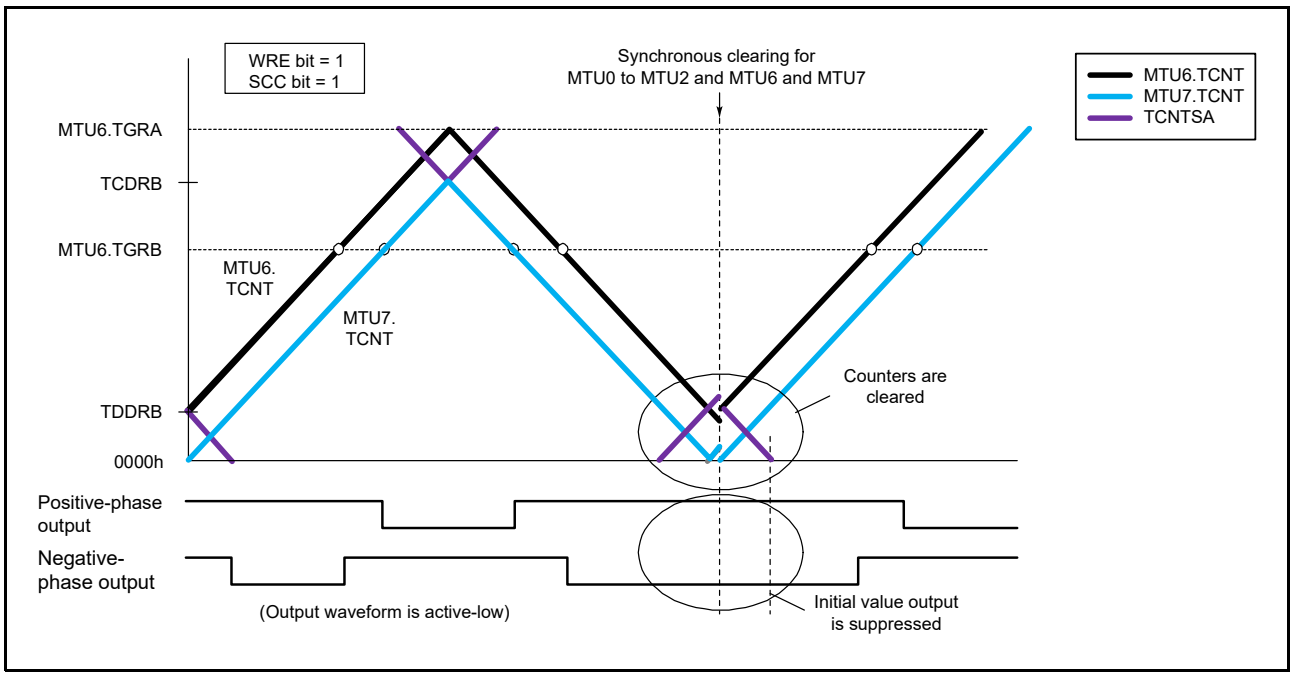


Figure 20.76 Example of Synchronous Clearing in Tb2 interval (Timing (11) in Figure 20.65; TWCRB.WRE Bit is 1 and SCC Bit is 1 in MTU6 and MTU7)

(p) Counter Clearing by MTU3.TGRA (MTU6.TGRA) Compare Match

In complementary PWM mode, MTU3.TCNT, MTU4.TCNT, and TCNTSA (MTU6.TCNT, MTU7.TCNT, and TCNTSB) can be cleared by MTU3.TGRA (MTU6.TGRA) compare match when the TWCRA.CCE (TWCRB.CCE) bit. Figure 20.77 illustrates an operation example.

Note 1. Use this function only in complementary PWM mode 1 (transfer at crest).
Note 2. Do not specify synchronous clearing by another channel (do not set 1 in the SYNC0 to SYNC4, SYNC9, or SYNC6 and SYNC7 bits in the timer synchronous register (TSYRA or TSYRB) and the CE0A to CE0D, CE1A, CE1B, CE2A, or CE2B bits in TSYCR).
Note 3. Do not set the PWM duty value to 0000h.
Note 4. Do not set the PSYE bit in timer output control register 1 (TOCR1A or TOCR1B) to 1.

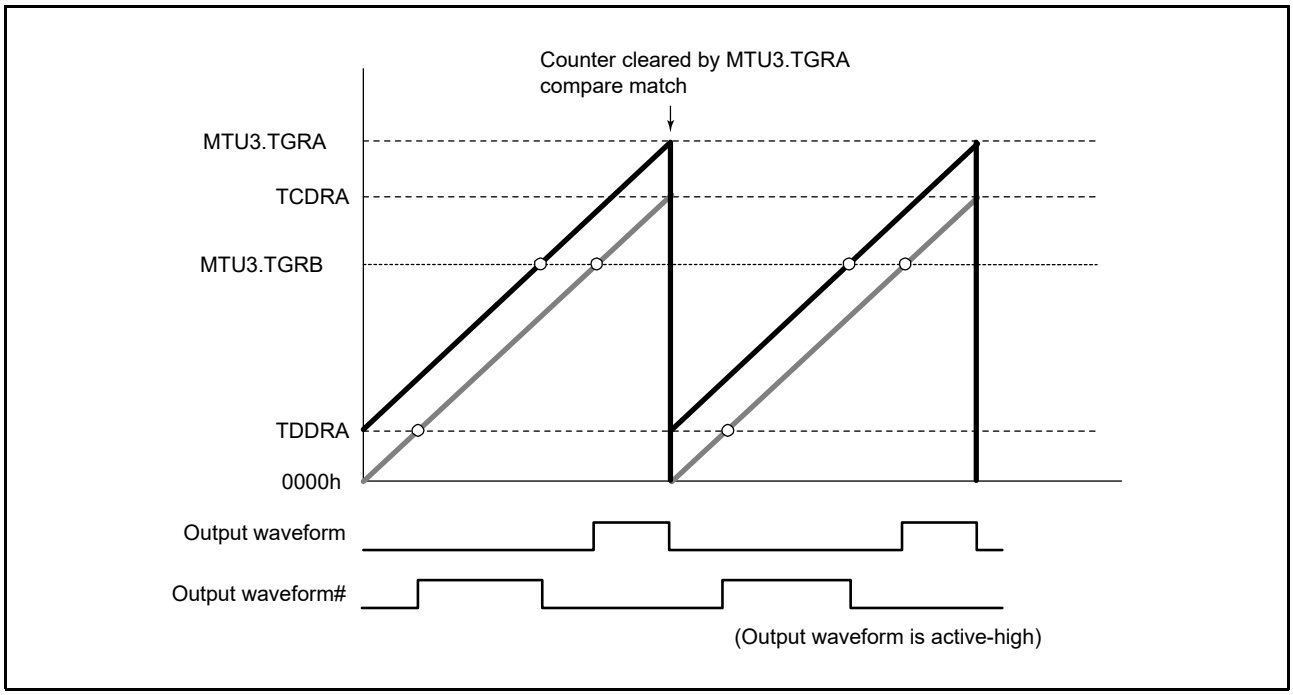


Figure 20.77 Example of Counter Clearing Operation by MTU3.TGRA Compare Match

(q) Example of Waveform Output for Driving AC Synchronous Motor (Brushless DC Motor)

In complementary PWM mode, a brushless DC motor can easily be controlled using the TGCRA (TGCRB) register. Figure 20.78 to Figure 20.81 show examples of brushless DC motor driving waveforms when MTU3 and MTU4 are used.

The TGCRB register enables driving waveform output from MTU6 and MTU7. The MTIOC9A, MTIOC9B, and MTIOC9C pins are used for external signals.

To switch the output phases for a 3-phase brushless DC motor by means of external signals detected with a Hall element, etc., clear the TGCRA.FB (TGCRB.FB) bit to 0. In this case, the external signals indicating the magnetic pole position should be input to timer input pins MTIOC0A, MTIOC0B, and MTIOC0C (MTIOC9A, MTIOC9B, and MTIOC9C) in MTU0 (MTU9) (make appropriate settings with the MPC and port mode registers (PMR) of the I/O ports). When an edge is detected at pin MTIOC0A, MTIOC0B, or MTIOC0C (MTIOC9A, MTIOC9B, and MTIOC9C), the output on/off state is switched automatically.

When the TGCRA.FB (TGCRB.FB) bit is 1, the output on/off state is switched when the UF, VF, or WF bit in TGCRA (TGCRB) is cleared to 0 or set to 1.

The driving waveforms are output from the 6-phase PWM output pins for complementary PWM mode.

With this 6-phase output, while the output is turned on, chopping output is available through complementary PWM mode output function by setting the N bit or P bit in TGCRA (TGCRB) to 1. When the N bit or P bit is 0, the level output is selected.

The active level of the 6-phase output (on output level) can be set with the TOCR1A.OLSN (TOCR1B.OLSN) and TOCR1A.OLSP (TOCR1B.OLSP) bits regardless of the setting of the N and P bits.

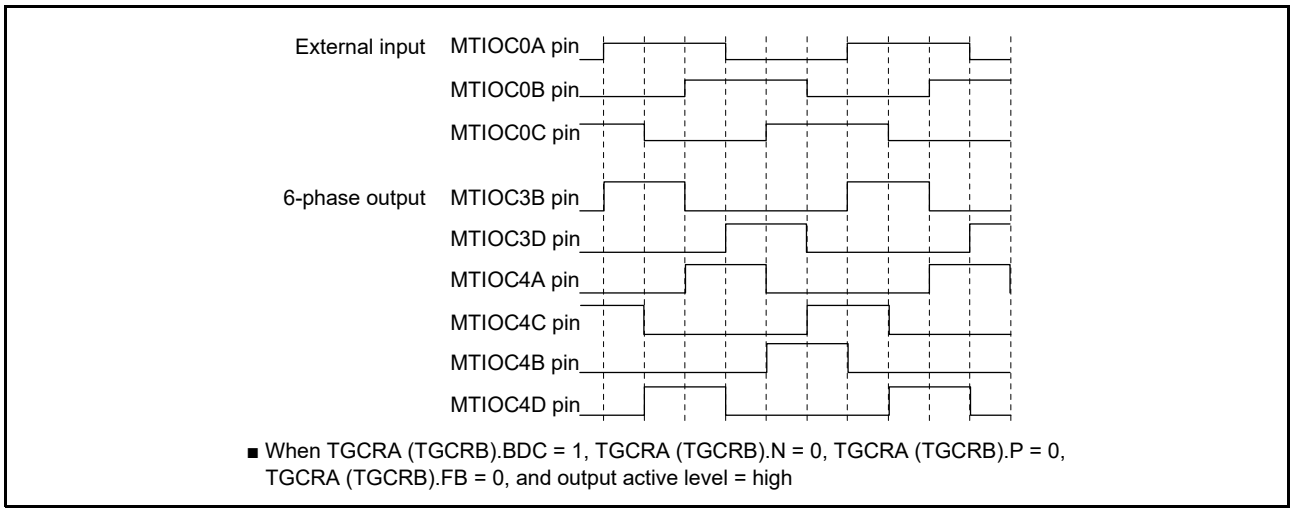
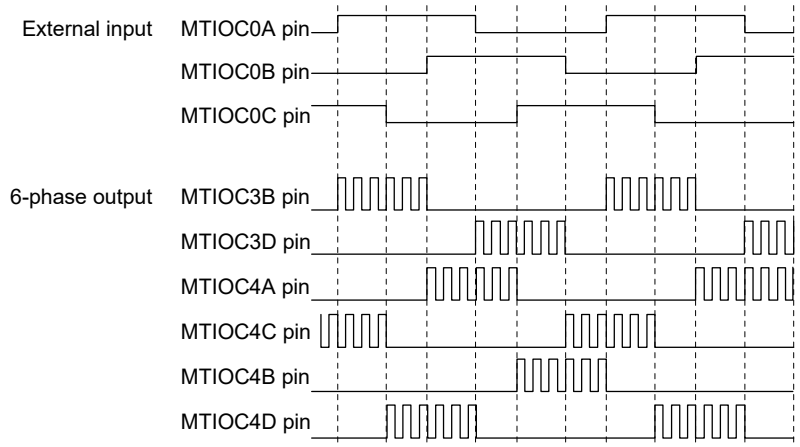
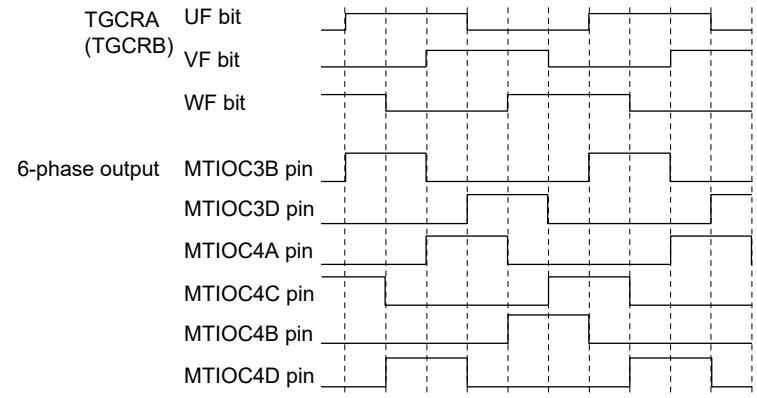


Figure 20.78 Example of Output Phase Switching by External Input (1)



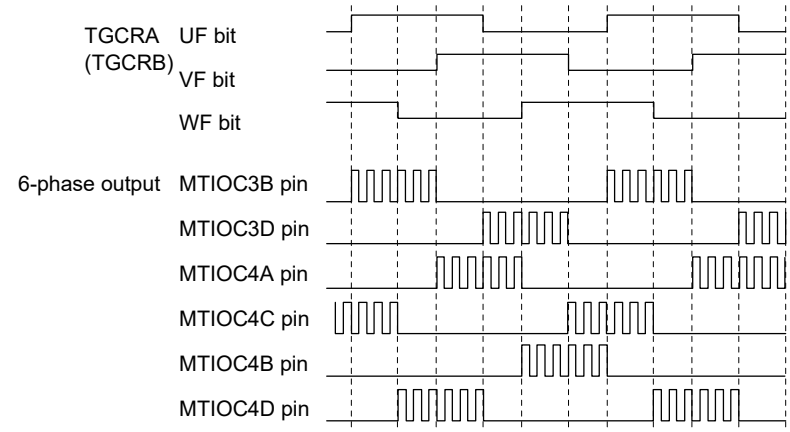
■ When TGCRA (TGCRB).BDC = 1, TGCRA (TGCRB).N = 1, TGCRA (TGCRB).P = 1, TGCRA (TGCRB).FB = 0, and output active level = high

Figure 20.79 Example of Output Phase Switching by External Input (2)



■ When TGCRA (TGCRB).BDC = 1, TGCRA (TGCRB).N = 0, TGCRA (TGCRB).P = 0, TGCRA (TGCRB).FB = 1, and output active level = high

Figure 20.80 Example of Output Phase Switching through UF, VF, and WF Bit Settings (1)



■ When TGCRA (TGCRB).BDC = 1, TGCRA (TGCRB).N = 1, TGCRA (TGCRB).P = 1, TGCRA (TGCRB).FB = 1, and output active level = high

Figure 20.81 Example of Output Phase Switching through UF, VF, and WF Bit Settings (2)

(r) A/D Converter Start Request Setting

In complementary PWM mode, an A/D converter start request can be issued using MTU3.TGRA (MTU6.TGRA) compare match, MTU4.TCNT (MTU7.TCNT) underflow (trough), or compare match on a channel other than MTU3 and MTU4 (MTU6 and MTU7).
When start requests using MTU3.TGRA (MTU6.TGRA) compare match are specified, A/D conversion can be started at the crest of the MTU3.TCNT (MTU6.TCNT) count.
A/D converter start requests can be specified by setting the TIER.TTGE bit. To issue an A/D converter start request at an MTU4.TCNT (MTU7.TCNT) underflow (trough), set the MTU4.TIER.TTGE2 (MTU7.TIER.TTGE2) bit to 1.

(s) Double Buffer Function in Complementary PWM Mode

In complementary PWM mode 3 (transfer at the crest and trough), the PWM output setting resolution can be improved from ±2 to ±1 by setting the TMDR2A.DRS (TMDR2B.DRS) bit to 1.
When setting buffer registers A (MTU3.TGRD, MTU4.TGRC, MTU4.TGRD, MTU6.TGRD, MTU7.TGRC, and MTU7.TGRD), set also buffer registers B (MTU3.TGRE, MTU4.TGRE, MTU4.TGRF, MTU6.TGRE, MTU7.TGRE, and MTU7.TGRF) at the same time. For details of the setting procedure, refer to section 20.3.8 (1), Example of Complementary PWM Mode Setting Procedure

Note: When a buffer register B is set to the buffer register A value, symmetric PWM waveforms are output. When a buffer register B is not set to the buffer register A value, asymmetric PWM waveforms are output.

Figure 20.82 shows an example of double buffer operation.
Each register data is transferred as follows.

- After MTU4.TGRD or MTU7.TGRD (buffer A) is written to, data is transferred from MTU4.TGRD or MTU7.TGRD (buffer A) to Temp3A or Temp6A (temporary A) and from MTU4.TGRF or MTU7.TGRF (buffer B) to Temp3B or Temp6B (temporary B).
- With timing (1) in the figure, data is transferred from Temp3A or Temp6A (temporary A) to MTU4.TGRB or MTU7.TGRB (compare).
- With timing (2) in the figure, data is transferred from Temp3B or Temp6B (temporary B) to MTU4.TGRB or MTU7.TGRB (compare).

In the crest interval (Tb1 interval), the compare register and temporary register A are valid; in the trough interval (Tb2 interval), the compare register and temporary register B are valid.

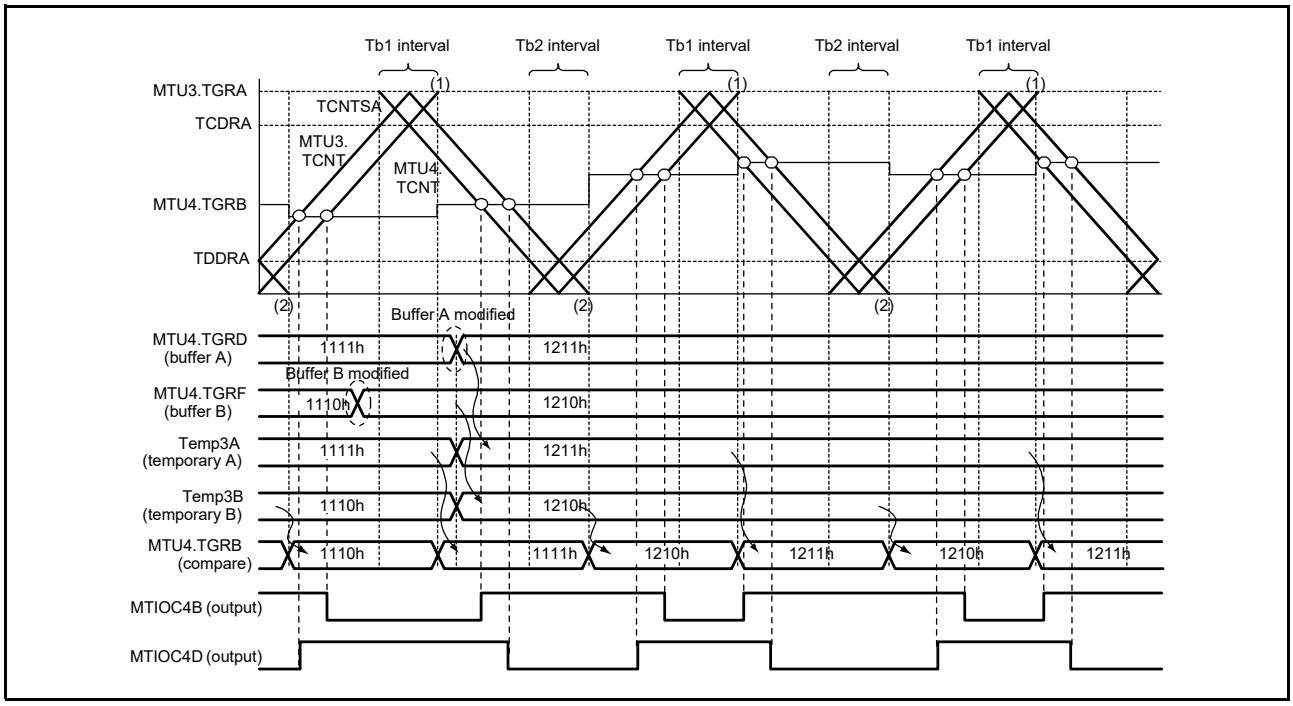


Figure 20.82 Example of Double Buffer Operation

Figure 20.83 shows an example when the buffer write value is smaller than the TDDRA (TDDRB) value, and Figure 20.84 shows an example when the write value is greater than TCDRA (TCDRB).
In the crest interval, the output is controlled according to the compare match with the compare register or temporary register A; in the trough interval, the output is controlled according to the compare match with the compare register or temporary register B.

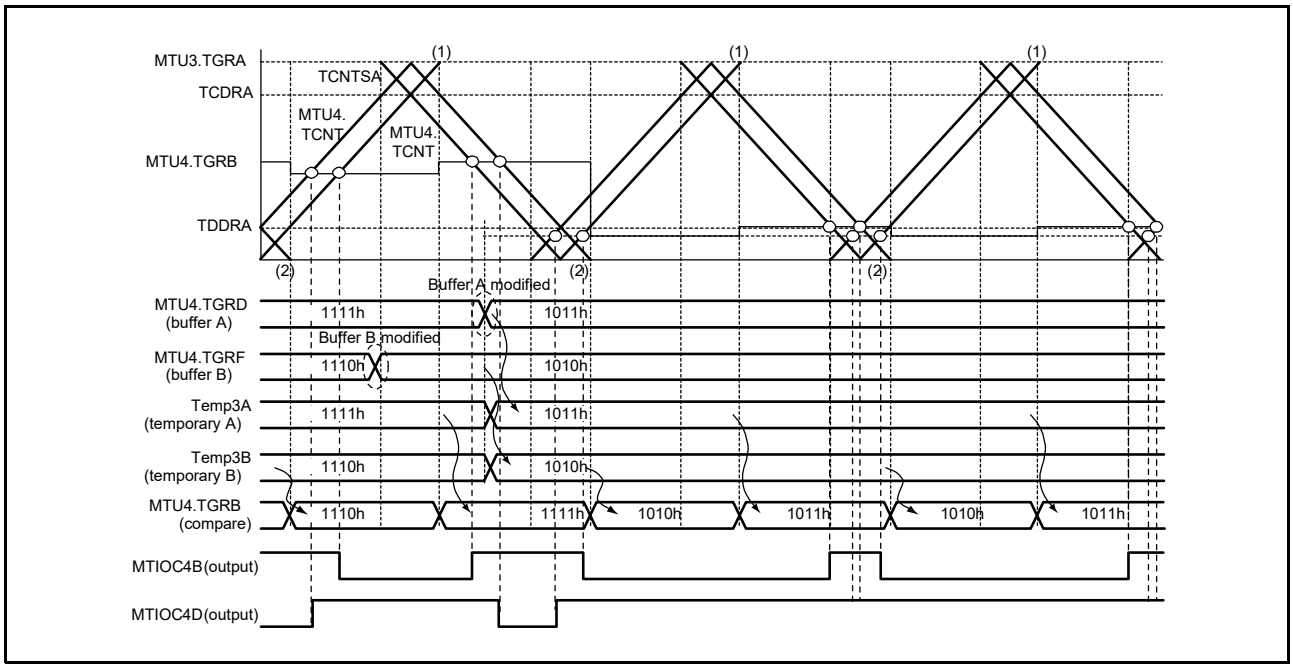


Figure 20.83 Example of Double Buffer Operation (Buffer Write Value is Smaller than TDDRA)

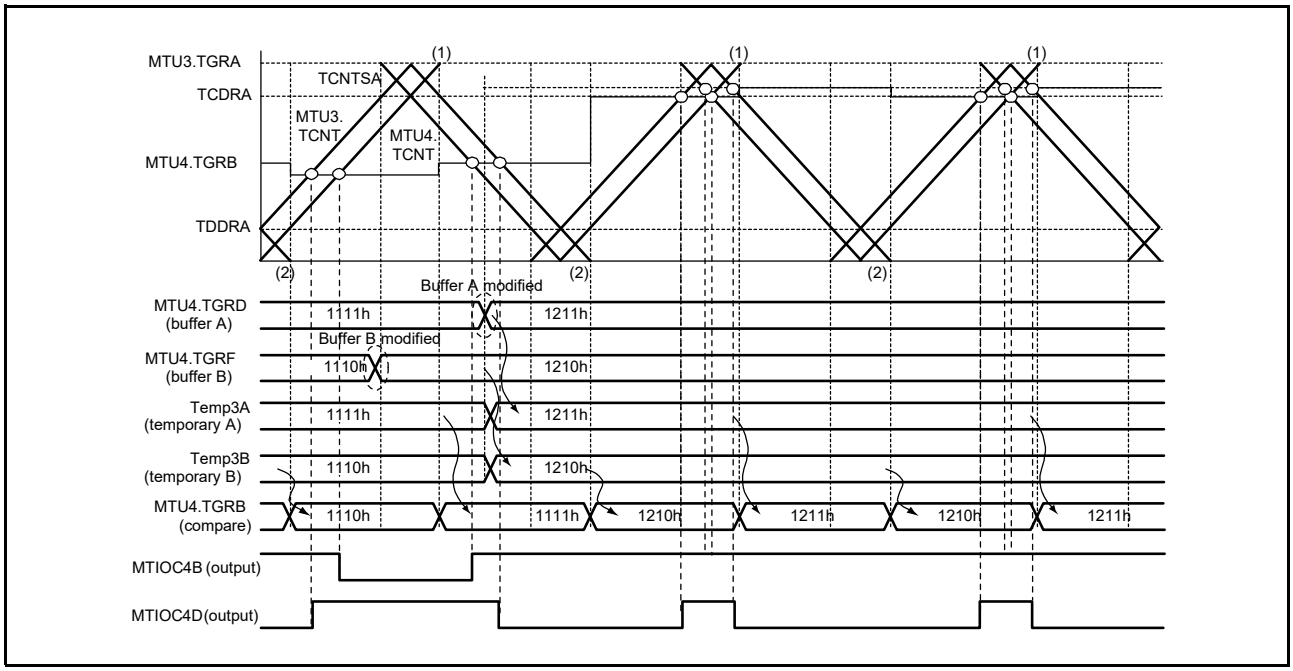


Figure 20.84 Example of Double Buffer Operation (Buffer Write Value is Greater than TCDRA)

(3) Interrupt Skipping Function 1 in Complementary PWM Mode

Interrupts TGIA3 (TGIA6) (at the crest) and TCIV4 (TCIV7) (at the trough) in MTU3 and MTU4 (MTU6 and MTU7) can be skipped up to seven times by making settings in the TITCR1A (TITCR1B) register.
Transfers from a buffer register to a temporary register or a compare register can be skipped in coordination with interrupt skipping by making settings in the TBTERA (TBTERB) register. For the linkage with buffer registers, refer to description (c), Buffer Transfer Control Linked with Interrupt Skipping, below.
A/D converter start requests generated by the A/D converter start request delaying function can also be skipped in coordination with interrupt skipping by making settings in the MTU4.TADCR (MTU7.TADCR) register. For the linkage with the A/D converter start request delaying function, refer to section 20.3.9, A/D Converter Start Request Delaying Function.
The TITCR1A (TITCR1B) register should be set while interrupt skipping function 1 is selected by setting the TITM bit in the timer interrupt skipping mode register (TITMRA or TITMRB) to 0, TGIA3 (TGIA6) interrupt requests are disabled by setting the MTU3.TIER (MTU6.TIER) register, TCIV4 (TCIV7) interrupt requests are disabled by setting the MTU4.TIER (MTU7.TIER) register, and a compare match is not generated. Before changing the skipping count, be sure to clear the T3AEN (T6AEN) and T4VEN (T7VEN) bits to 0 to clear the skipping counter.

(a) Example of Interrupt Skipping Function 1 Setting Procedure

Figure 20.85 shows an example of the interrupt skipping function 1 setting procedure. Figure 20.86 shows the periods during which interrupt skipping count can be changed.

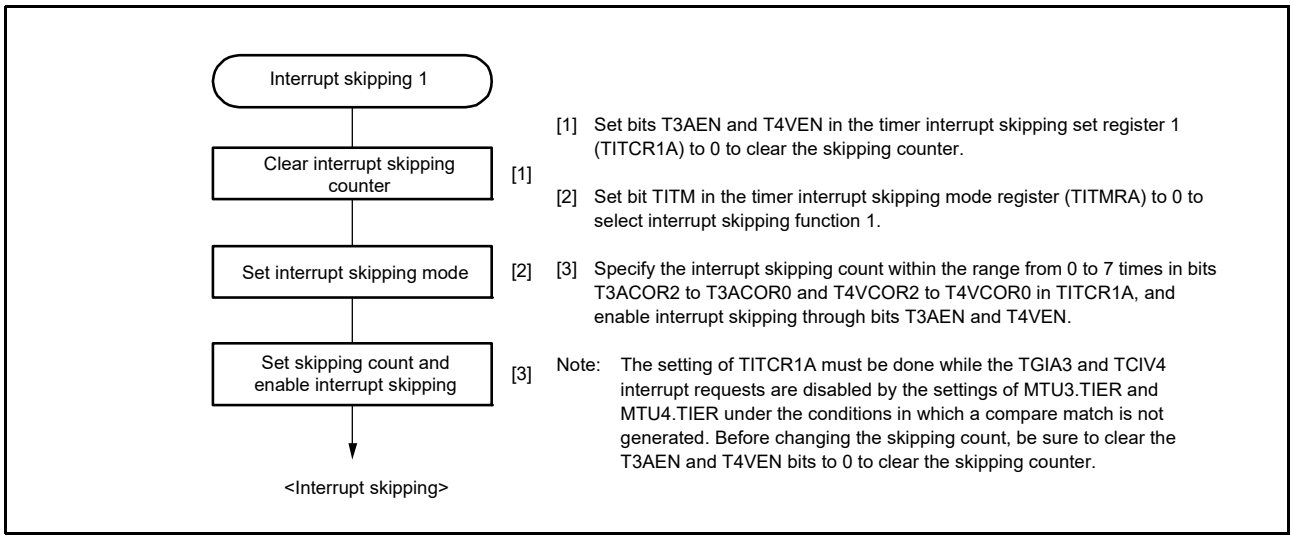


Figure 20.85 Example of Interrupt Skipping Function 1 Setting Procedure

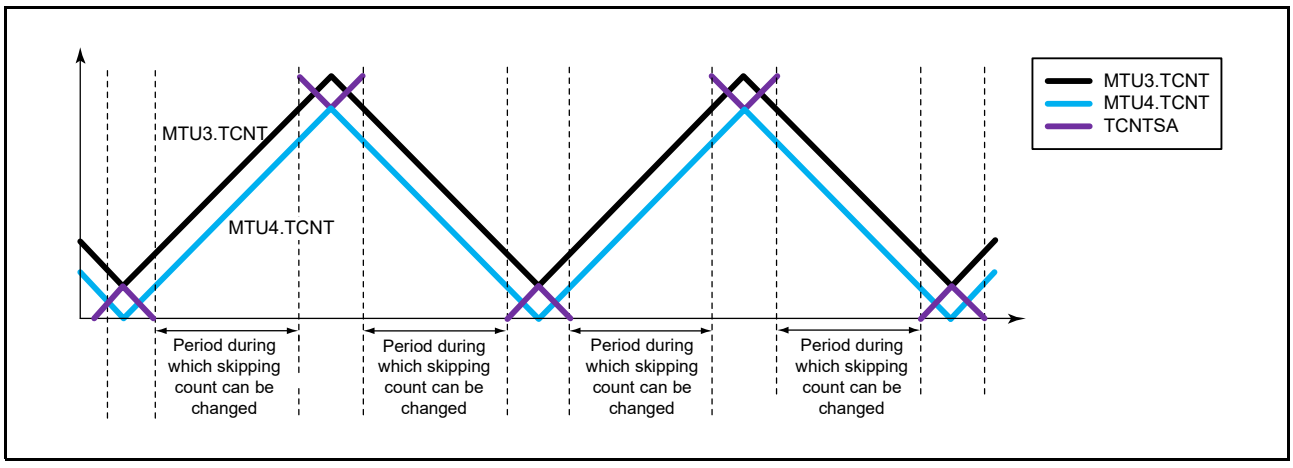


Figure 20.86 Periods during which Interrupt Skipping Count can be Changed

(b) Example of Interrupt Skipping Function 1

Figure 20.87 shows an example of TGIA3 (TGIA6) interrupt skipping in which the interrupt skipping count is set to three by the T3ACOR (T6ACOR) bits and the T3AEN (T6AEN) bit is set to 1 in the TITCR1A (TITCR1B) register.

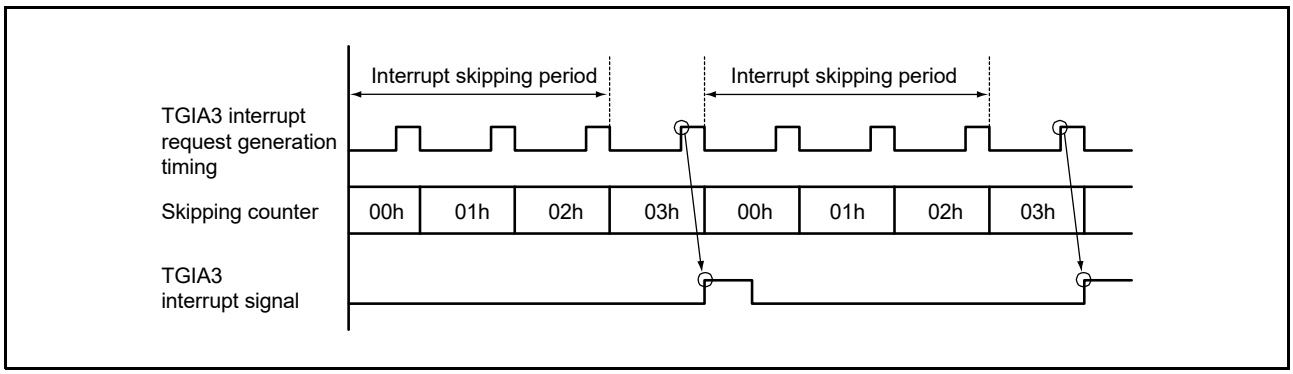
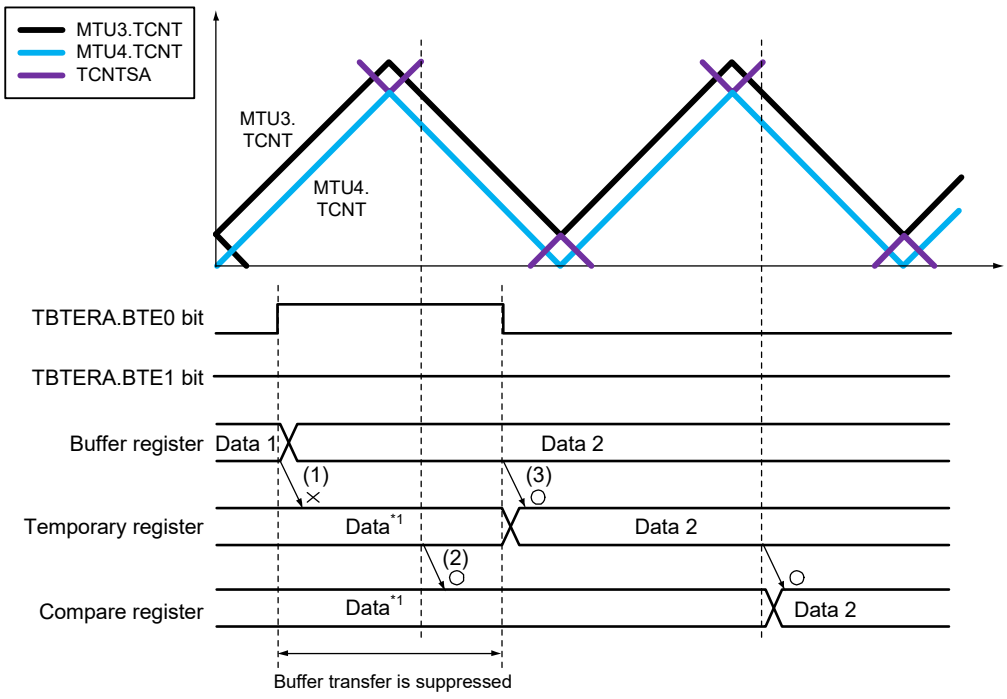


Figure 20.87 Example of Interrupt Skipping Function 1

(c) Buffer Transfer Control Linked with Interrupt Skipping

In complementary PWM mode, whether to transfer data from a buffer register to a temporary register and whether to link the transfer with interrupt skipping can be specified with the BTE[1:0] bits in the TBTERA (TBTERB) register.
Figure 20.88 shows an example of operation when buffer transfer is disabled (BTE[1:0] = 01b). While this setting is valid, data is not transferred from the buffer register to the temporary register.
Figure 20.89 shows an example of operation when buffer transfer is linked with interrupt skipping (BTE[1:0] = 10b). While this setting is valid, data is not transferred from the buffer register outside the buffer transfer-enabled period. Note that the buffer transfer-enabled period differs depending on whether only the T3AEN (T6AEN) bit in the TITCR1A (TITCR1B) register is set to 1, only the T4VEN (T7VEN) bit in the TITCR1A (TITCR1B) register is set to 1, or both the T3AEN and T4VEN (T6AEN and T7VEN) bits are set to 1. Figure 20.90 shows the relationship between the T3AEN (T6AEN) and T4VEN (T7VEN) bit settings in TITCR1A (TITCR1B) and buffer transfer-enabled period.

Note: This function must be used in combination with interrupt skipping function 1.
When interrupt skipping is disabled (the T3AEN and T4VEN (T6AEN and T7VEN) bits in the timer interrupt skipping set register 1 (TITCR1A or TITCR1B) are cleared to 0 or the skipping count set bits (T3ACOR and T4VCOR (T6ACOR and T7VCOR)) in TITCR1A (TITCR1B) are cleared to 0), make sure that buffer transfer is not linked with interrupt skipping (clear the BTE1 bit in TBTERA or TBTERB to 0).
If buffer transfer is linked with interrupt skipping while interrupt skipping is disabled, buffer transfer is never performed.



(1) No data is transferred from the buffer register to the temporary register in the buffer transfer-disabled period (bits BTE[1:0] in TBTERA are set to 01b).
(2) Data is transferred from the temporary register to the compare register even in the buffer transfer-disabled period.
(3) After buffer transfer is enabled, data is transferred from the buffer register to the temporary register.

Note 1. When buffer transfer at the crest is selected.

Figure 20.88 Example of Operation When Buffer Transfer is Disabled (BTE[1:0] = 01b)

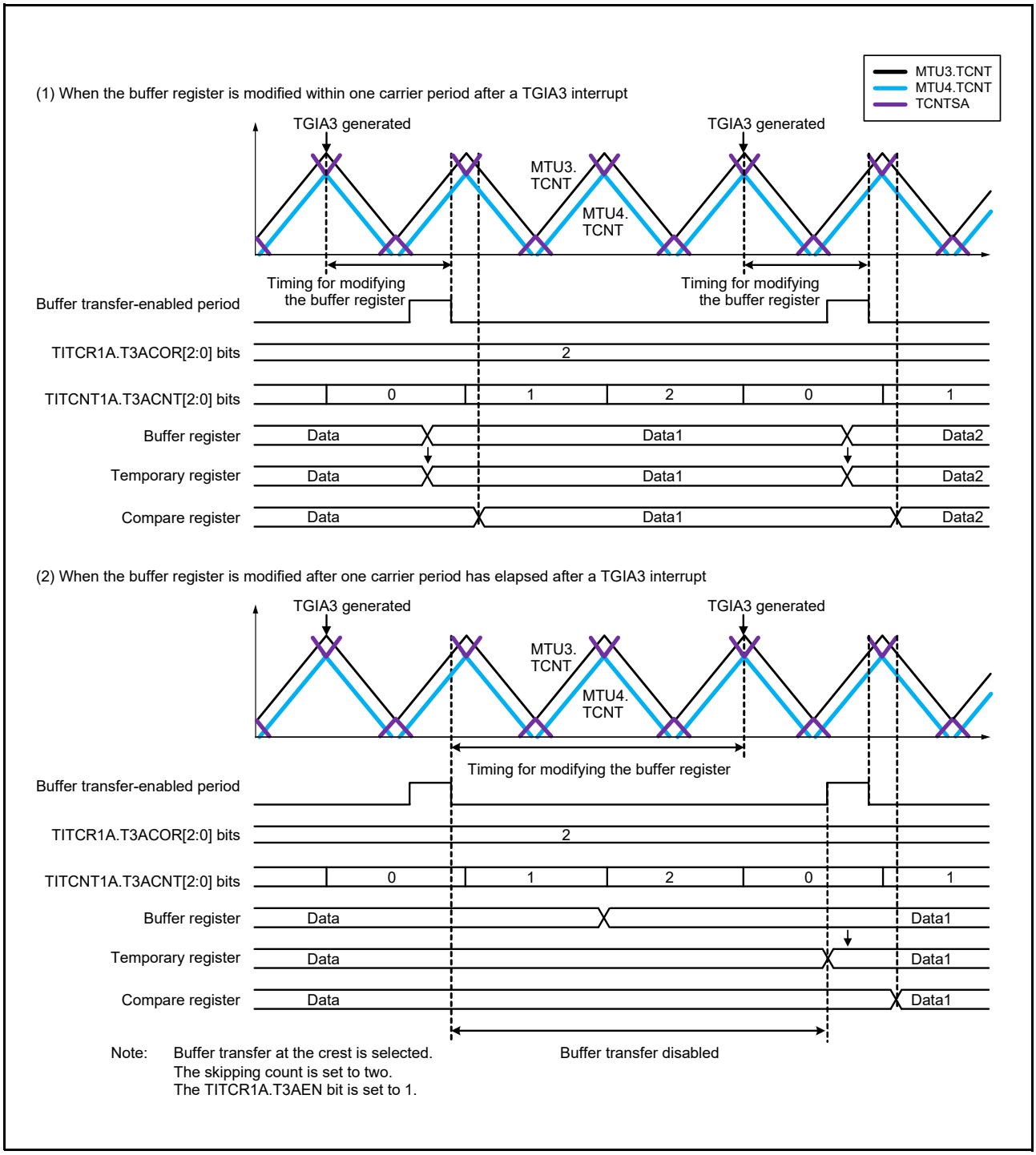


Figure 20.89 Example of Operation When Buffer Transfer is Linked with Interrupt Skipping (BTE[1:0] = 10b)

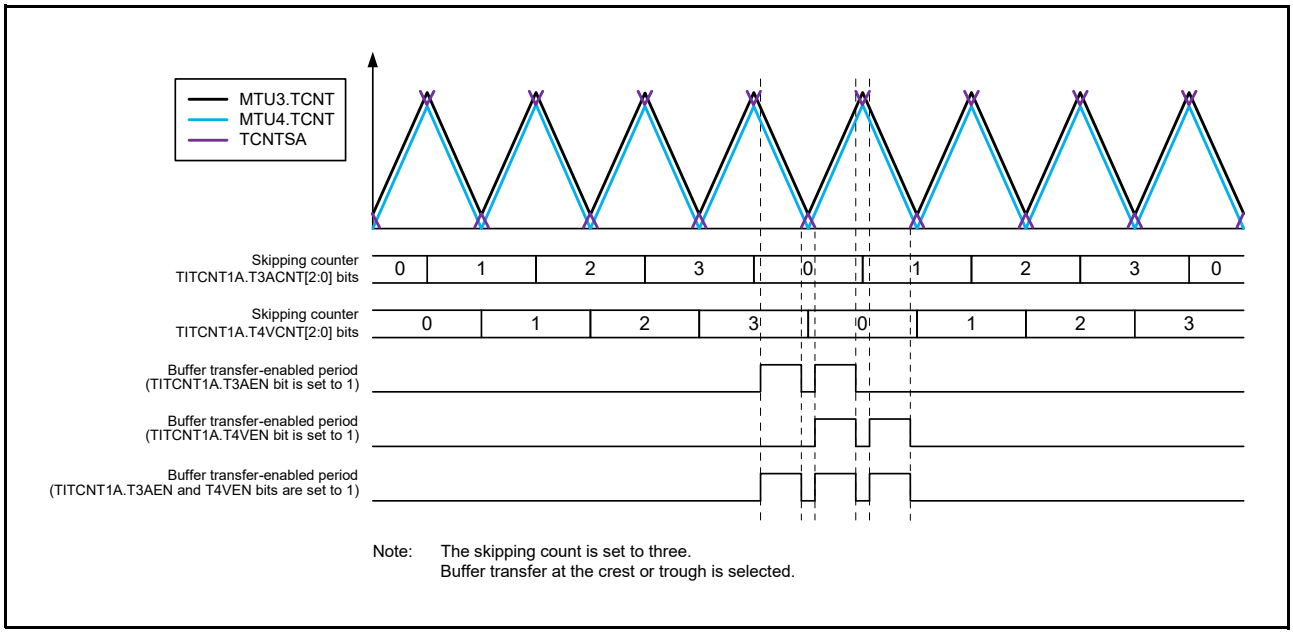


Figure 20.90 Relationship between Bits T3AEN and T4VEN in TITCR1A and Buffer Transfer-Enabled Period

(4) Complementary PWM Mode Output Protection Functions

The following output protection functions are provided for complementary PWM mode.

(a) Register and Counter Miswrite Prevention Function

Access from the CPU to the mode registers, control registers, compare registers, and counters can be enabled or disabled by setting the RWE bit in the TRWERA (TRWERB) register. The applicable registers are some of the registers in MTU3, MTU4, MTU6, and MTU7 shown below:
48 registers in total
MTU3.TCR, MTU4.TCR, MTU3.TCR2, MTU4.TCR2, MTU3.TMDR1, MTU4.TMDR1, MTU3.TIORH, MTU4.TIORH, MTU3.TIORL, MTU4.TIORL, MTU3.TIER, MTU4.TIER, MTU3.TCNT, MTU4.TCNT, MTU3.TGRA, MTU4.TGRA, MTU3.TGRB, MTU4.TGRB, MTU.TOERA, MTU.TOCR1A, MTU.TOCR2A, MTU.TGCRA, MTU.TCDRA, MTU.TDDRA,
MTU6.TCR, MTU7.TCR, MTU6.TCR2, MTU7.TCR2, MTU6.TMDR1, MTU7.TMDR1, MTU6.TIORH, MTU7.TIORH, MTU6.TIORL, MTU7.TIORL, MTU6.TIER, MTU7.TIER, MTU6.TCNT, MTU7.TCNT, MTU6.TGRA, MTU7.TGRA, MTU6.TGRB, MTU7.TGRB, MTU.TOERB, MTU.TOCR1B, MTU.TOCR2B, MTU.TGCRB, MTU.TCDRB, and MTU.TDDRB
This function can disable CPU access to the mode registers, control registers, and counters to prevent miswriting due to CPU runaway. In the access-disabled state, the applicable registers are read as undefined and writing to these registers is ignored.

(b) Halting of PWM Output by External Signal

The PWM output pins of MTU0, MTU3, MTU4, MTU6, MTU7, and MTU9 can be set to the high-impedance state automatically.
Refer to section 21, Port Output Enable 3 (POE3A), for details.

20.3.9 A/D Converter Start Request Delaying Function

A/D converter start requests can be issued in MTU4 or MTU7 by making settings in the timer A/D converter start request control register (MTU4.TADCR or MTU7.TADCR), timer A/D converter start request cycle set registers (MTU4.TADCORA and MTU4.TADCORB, or MTU7.TADCORA and MTU7.TADCORB), and timer A/D converter start request cycle set buffer registers (MTU4.TADCOBRA and MTU4.TADCOBRB, or MTU7.TADCOBRA and MTU7.TADCOBRB).
The A/D converter start request delaying function compares MTU4.TCNT with MTU4.TADCORA or MTU4.TADCORB (MTU7.TCNT with MTU7.TADCORA or MTU7.TADCORB), and when their values match, the function issues a respective A/D converter start request (TRG4AN or TRG4BN (TRG7AN or TRG7BN)).
A/D converter start requests (TRG4AN and TRG4BN (TRG7AN and TRG7BN)) can be skipped in coordination with interrupt skipping by making settings in the ITA3AE, ITA4VE, ITB3AE, and ITB4VE bits in MTU4.TADCR (the ITA6AE, ITA7VE, ITB6AE, and ITB7VE bits in MTU7.TADCR).

(1) Example of Procedure for Specifying A/D Converter Start Request Delaying Function

Figure 20.91 shows an example of procedure for specifying the A/D converter start request delaying function.

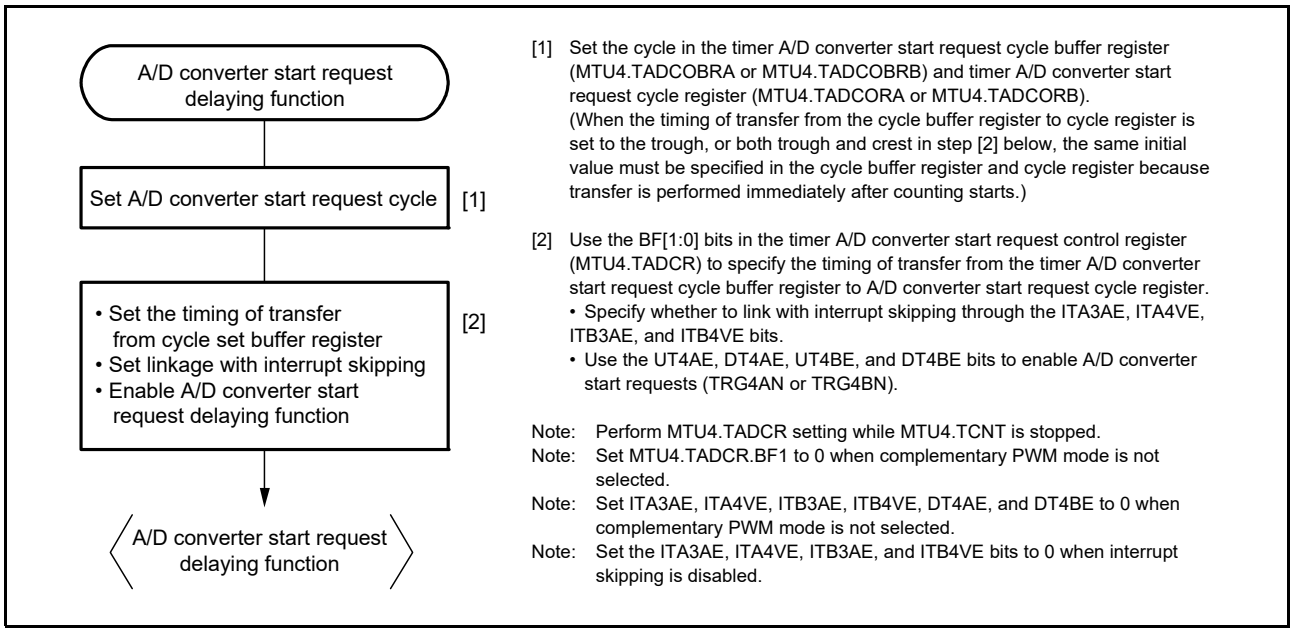
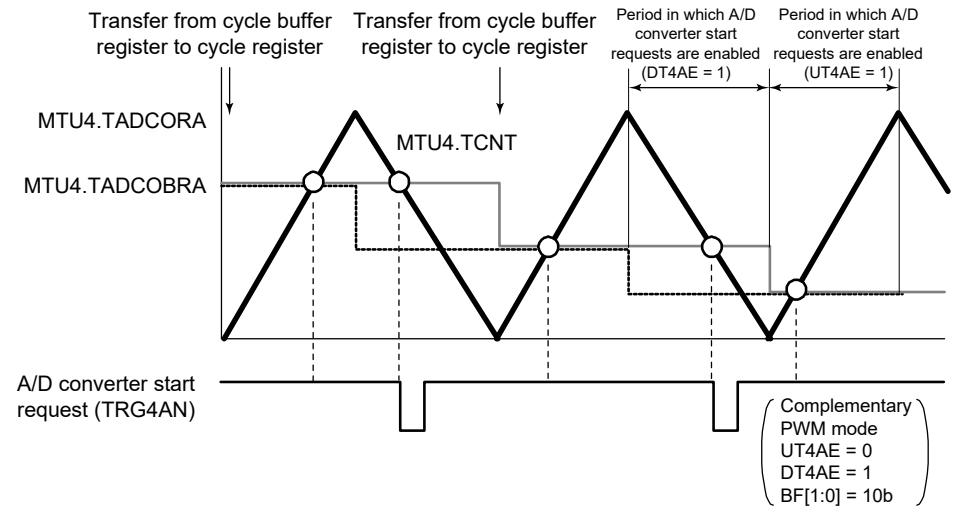


Figure 20.91 Example of Procedure for Specifying A/D Converter Start Request Delaying Function (MTU3 and MTU4)

(2) Basic Example of A/D Converter Start Request Delaying Function Operation

Figure 20.92 shows a basic example of A/D converter start request signal (TRG4AN (TRG7AN)) operation when the trough of MTU4.TCNT (MTU7.TCNT) is specified for the buffer transfer timing and an A/D converter start request signal is output during MTU4.TCNT (MTU7.TCNT) down-counting.



Period in which A/D converter start requests are enabled (UT4AE = 1): 0 ≤ MTU4.TCNT ≤ TCDR - 1
Period in which A/D converter start requests are enabled (DT4AE = 1): TCDR ≥ MTU4.TCNT ≥ 1

UT4AE, DT4AE, BF[1:0]: Bits in TADCR

Figure 20.92 Basic Example of A/D Converter Start Request Signal (TRG4AN) Operation

(3) Period in Which A/D Converter Start Requests are Enabled

When the MTU4.TCNT (MTU7.TCNT) counter and the MTU4.TADCORA or MTU4.TADCORB (MTU7.TADCORA or MTU7.TADCORB) register matches within the period enabled by the UT4AE and UT4BE (UT7AE and UT7BE) bits, the corresponding A/D converter start request (TRG4AN or TRG4BN) is issued.

When the UT4AE and UT4BE (UT7AE and UT7BE) bits in the MTU4.TADCR (MTU7.TADCR) register are set to 1 in complementary PWM mode, A/D converter start requests are enabled during the MTU4.TCNT (MTU7.TCNT) up-counting (0 ≤ MTU4.TCNT (MTU7.TCNT) ≤ TCDR – 1). When the DT4AE and DT4BE (DT7AE and DT7BE) bits in the MTU4.TADCR (MTU7.TADCR) register are set to 1, A/D converter start requests are enabled during MTU4.TCNT (MTU7.TCNT) down-counting (TCDR ≥ MTU4.TCNT (MTU7.TCNT) ≥ 1). Refer to Figure 20.92.

(4) Buffer Transfer

The data in the timer A/D converter start request cycle set registers (MTU4.TADCORA and MTU4.TADCORB, or MTU7.TADCORA and MTU7.TADCORB) is updated by writing data to the timer A/D converter start request cycle set buffer registers (MTU4.TADCOBRA and MTU4.TADCOBRB, or MTU7.TADCOBRA and MTU7.TADCOBRB). Data is transferred from the buffer registers to the respective cycle set registers at the timing selected with the BF[1:0] bits in the MTU4.TADCR (MTU7.TADCR) register.

In complementary PWM mode, data is also transferred from the timer A/D converter start request cycle set buffer registers to the timer A/D converter start request cycle set registers when MTU4.TGRD (MTU7.TGRD) register is updated.

There are notes on the timing for transferring data when using buffer transfer in complementary PWM mode.

For details, section 20.6.27, Usage Notes on A/D Converter Delaying Function in Complementary PWM Mode.

In modes other than complementary PWM mode, set the BF1 bit in the MTU4.TADCR (MTU7.TADCR) register to 0.

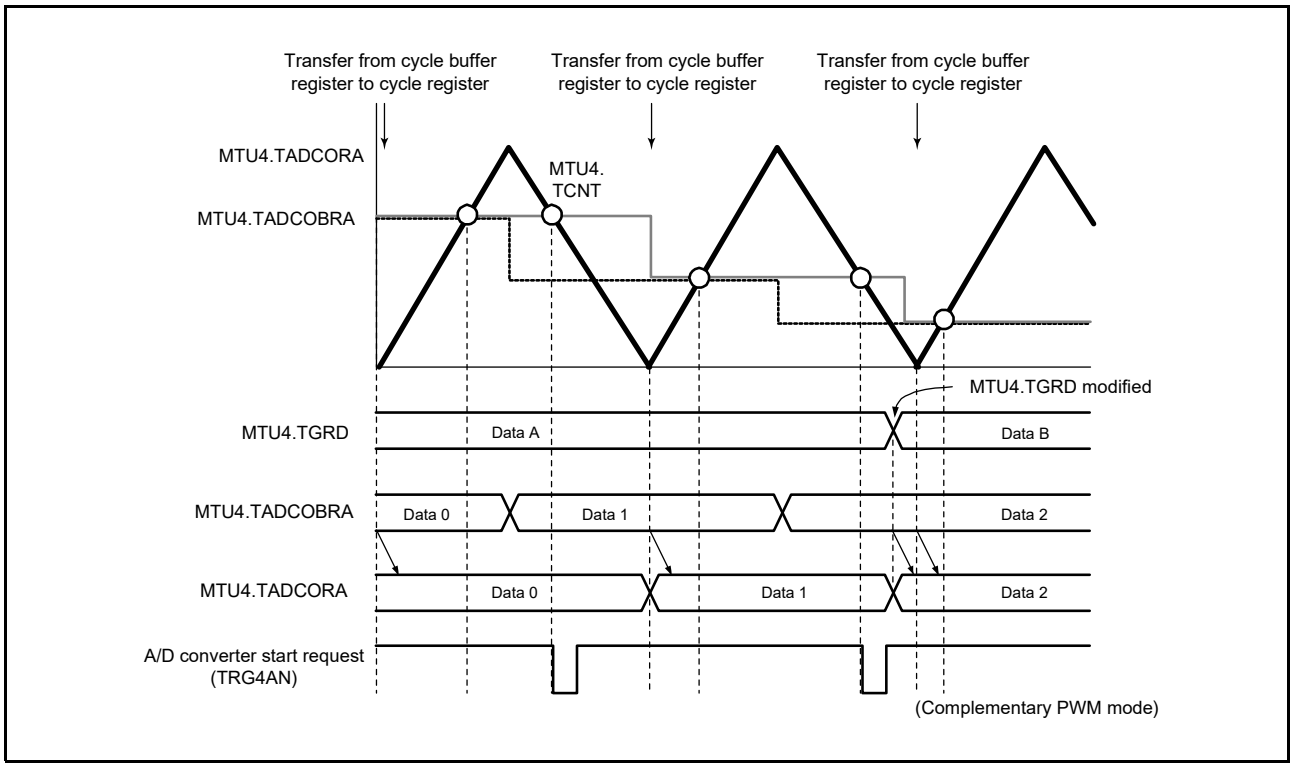


Figure 20.93 Example of A/D Converter Start Request Signal (TRG4AN) and Buffer Transfer Operation

(5) A/D Converter Start Request Delaying Function Linked with Interrupt Skipping Function 1

In complementary PWM mode, A/D converter start requests (TRG4AN and TRG4BN (TRG7AN and TRG7BN)) can be issued in coordination with interrupt skipping 1 by making settings in the ITA3AE, ITA4VE, ITB3AE, and ITB4VE (ITA6AE, ITA7VE, ITB6AE, and ITB7VE) bits in the MTU4.TADCR (MTU7.TADCR) register.

Figure 20.94 shows an example of A/D converter start request signal (TRG4AN (TRG7AN)) operation when TRG4AN (TRG7AN) output is enabled during MTU4.TCNT (MTU7.TCNT) up-counting and down-counting and A/D converter start requests are linked with interrupt skipping 1.

Figure 20.95 shows another example of A/D converter start request signal (TRG4AN (TRG7AN)) operation when TRG4AN (TRG7AN) output is enabled during MTU4.TCNT (MTU7.TCNT) up-counting and A/D converter start requests are linked with interrupt skipping 1.

In modes other than complementary PWM mode, do not use the A/D converter start request delaying function linked with the interrupt skipping function 1.

Set the ITA3AE, ITA4VE, ITB3AE, and ITB4VE (ITA6AE, ITA7VE, ITB6AE, and ITB7VE) bits in the MTU4.TADCR (MTU7.TADCR) register to 0.

Note: This function should be used in combination with interrupt skipping 1.
When interrupt skipping is disabled (the T3AEN and T4VEN (T6AEN and T7VEN) bits in the timer interrupt skipping set register (TITCR1A (TITCR1B)) are cleared to 0 or the skipping count set bits (T3ACOR and T4VCOR (T6ACOR and T7VCOR)) in TITCR1A (TITCR1B) are cleared to 0), make sure that A/D converter start requests are not linked with interrupt skipping 1 (clear the ITA3AE, ITA4VE, ITB3AE, and ITB4VE (ITA6AE, ITA7VE, ITB6AE, and ITB7VE) bits in the timer A/D converter start request control register (MTU4.TADCR (MTU7.TADCR)) to 0).
When this function is used, MTU4.TADCORA and MTU4.TADCORB (MTU7.TADCORA and MTU7.TADCORB) should be set with the value ranging 0002h to the value set in TCDRA minus 2 (value set in TCDRB minus 2).

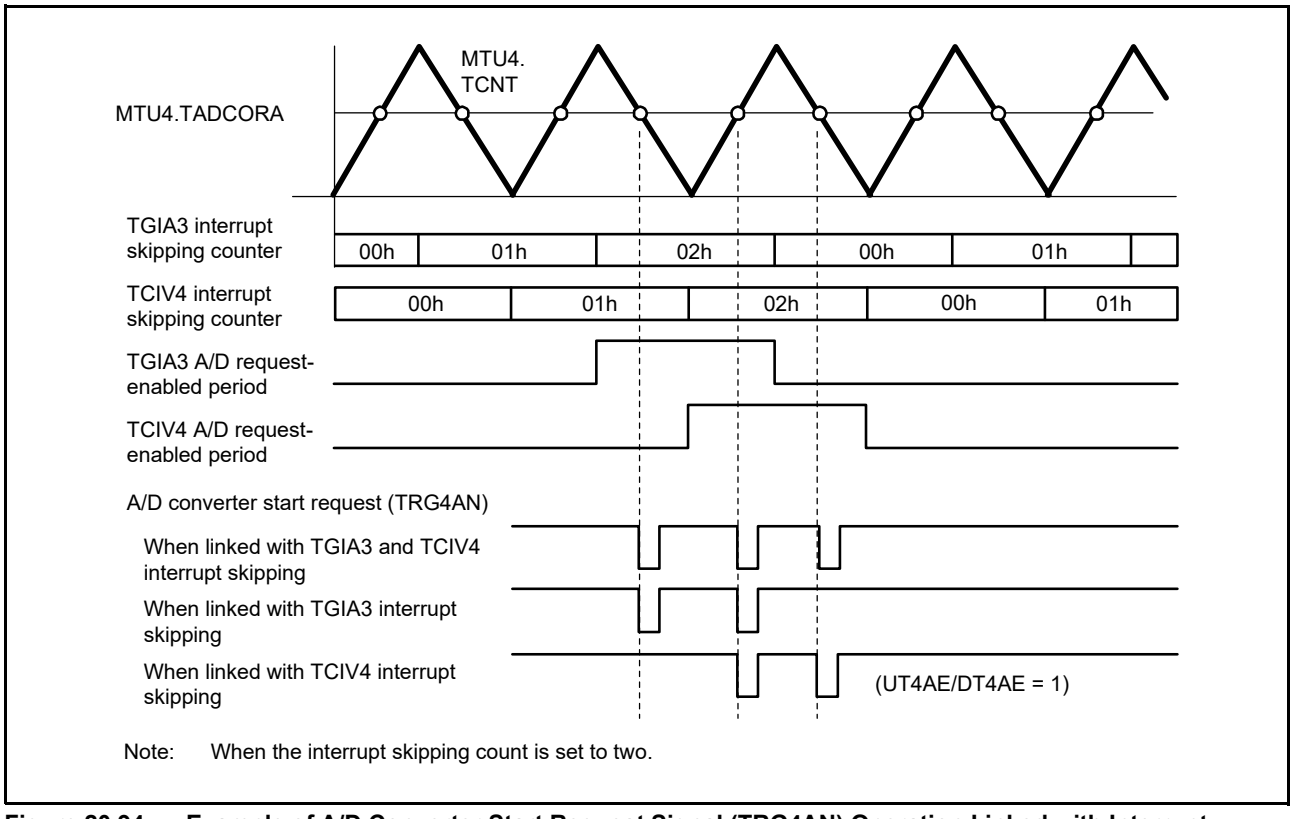


Figure 20.94 Example of A/D Converter Start Request Signal (TRG4AN) Operation Linked with Interrupt Skipping Function 1 (UT4AE and DT4AE = 1)

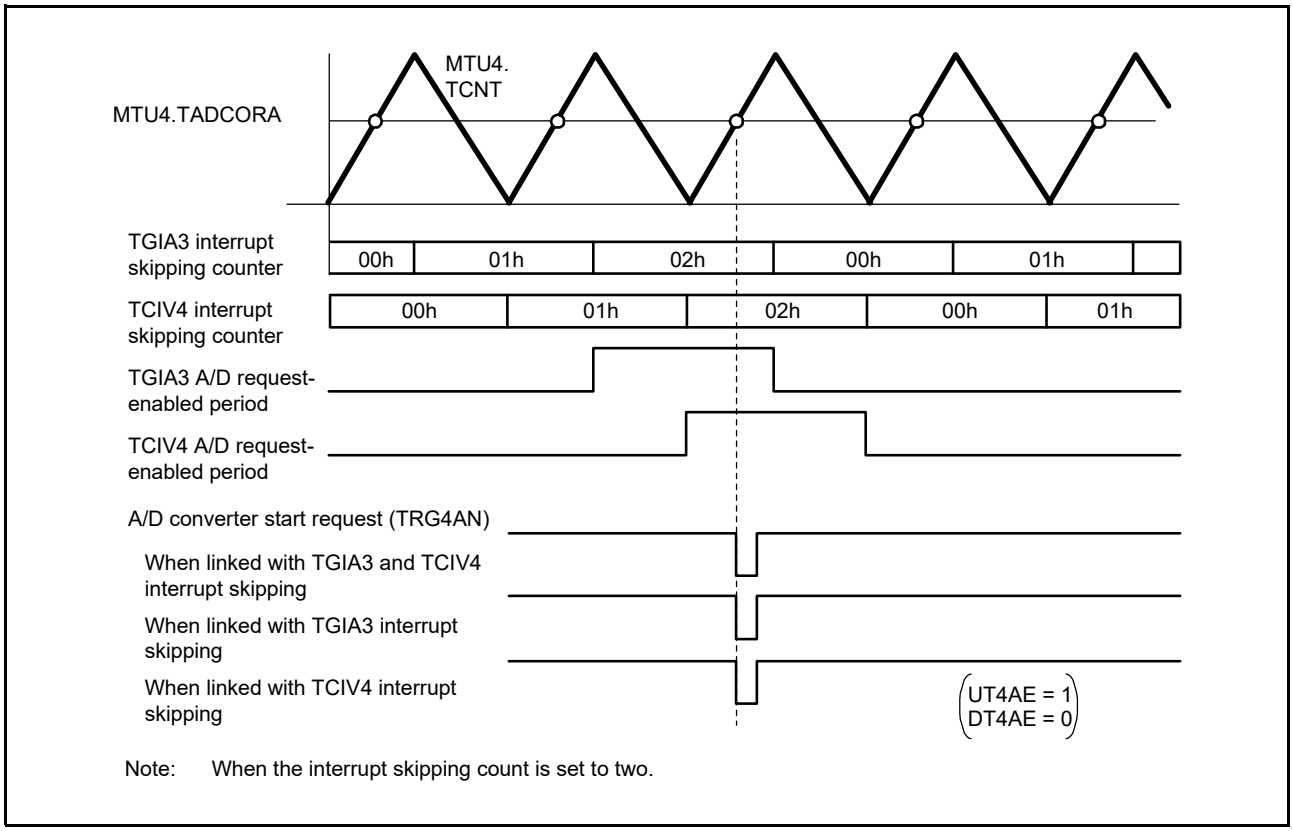


Figure 20.95 Example of A/D Converter Start Request Signal (TRG4AN) Operation Linked with Interrupt Skipping Function 1 (UT4AE = 1, DT4AE = 0)

(6) A/D Converter Start Request Delaying Function Linked with Interrupt Skipping Function 2

By setting the TITM bit to 1 in the TITMRA (TITMRB) register, the counter starts down-counting from the value (0 to 7) set in the TRG4COR[2:0] (TRG7COR[2:0]) bits in TITCR2A (TITCR2B) register every time an A/D converter start trigger (TRG4AN or TRG4BN (TRG7AN or TRG7BN)) is generated. When the counter value reaches 0 and is reloaded, the TRG4AN and TRG4BN (TRG7AN and TRG7BN) interrupts become valid and an A/D converter start request signal (TRG4ABN (TRG7ABN)) is output.
This function is valid only when the A/D converter request delaying function is enabled.

(a) Example of Procedure for Setting Interrupt Skipping Function 2

Figure 20.96 shows an example of procedure for setting interrupt skipping function 2.

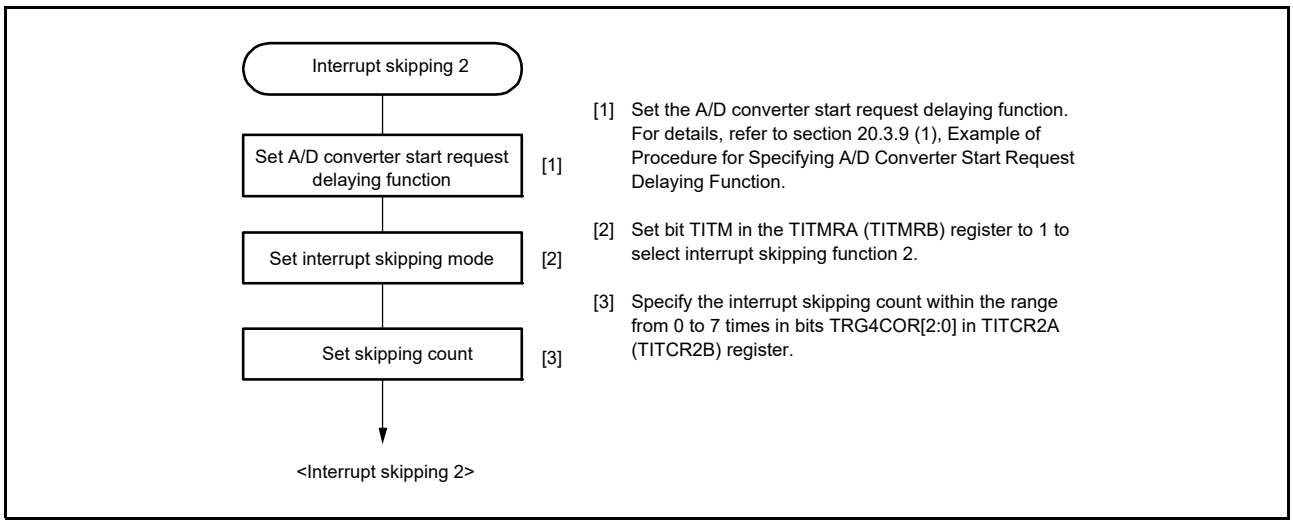


Figure 20.96 Example of Procedure for Setting Interrupt Skipping Function 2

(b) Example of Interrupt Skipping Function 2 Operation

Figure 20.97 shows an example of interrupt skipping function 2 operation.

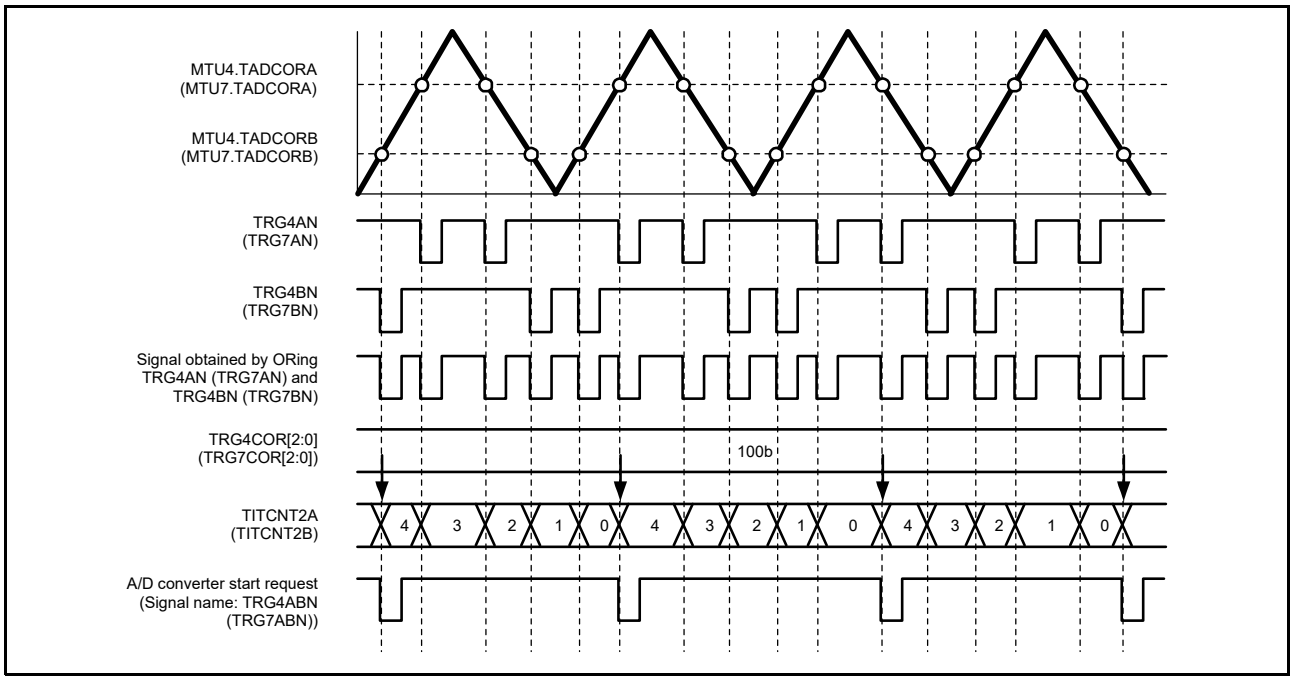


Figure 20.97 Example of Interrupt Skipping Function 2 Operation (Skipping Count is Set to Four)

20.3.10 Synchronous Operation of MTU0 to MTU4, MTU6, MTU7, and MTU9

(1) Synchronous Counter Start for MTU0 to MTU4, MTU6, MTU7, and MTU9

The counters in MTU0 to MTU4, MTU6, MTU7, and MTU9 can be started synchronously by making the TCSYSTR settings.

(a) Example of Procedure for Setting Synchronous Counter Start for MTU0 to MTU4, MTU6, MTU7, and MTU9

Figure 20.98 shows an example of procedure for setting synchronous counter start for MTU0 to MTU4, MTU6, MTU7, and MTU9.

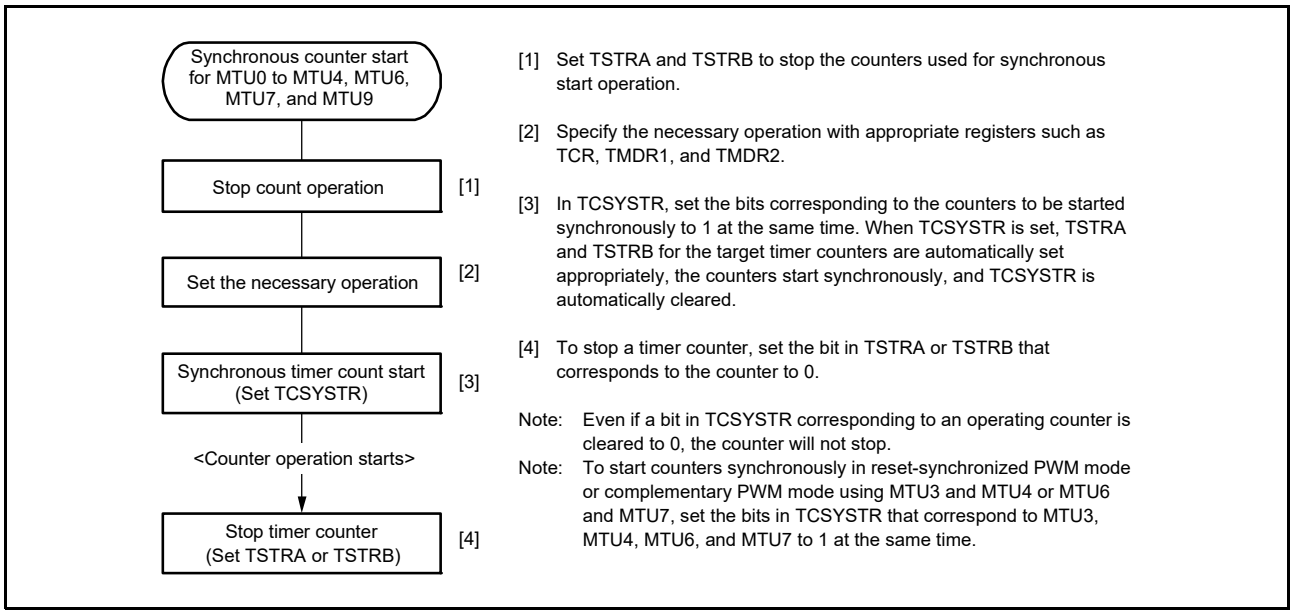


Figure 20.98 Example of Procedure for Setting Synchronous Counter Start for MTU0 to MTU4, MTU6, MTU7, and MTU9

(b) Examples of Synchronous Counter Start Operation

Figure 20.99 shows an examples of synchronous counter start operation for MTU0 to MTU4, MTU6, MTU7, and MTU9.

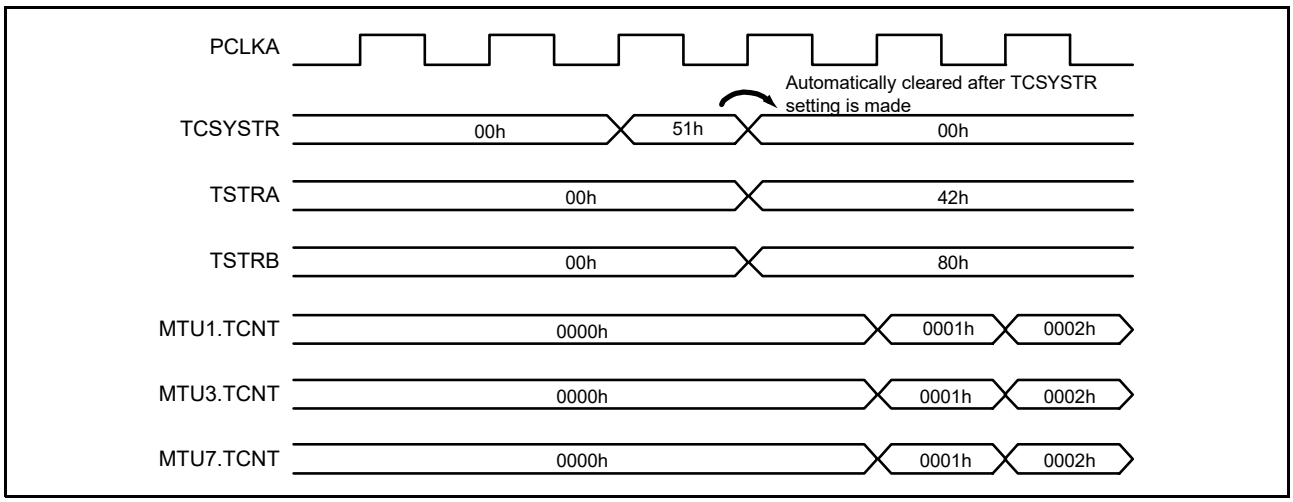


Figure 20.99 Examples of Synchronous Counter Start Operation for MTU0 to MTU4, MTU6, MTU7, and MTU9

(2) Synchronous Counter Clearing for MTU6 and MTU7

The counters in MTU6 and MTU7 can be cleared by the TGImn interrupt generation timing (m = A to D; n = 0 to 2) through the TSYCR setting.

(a) Example of Procedure for Specifying Synchronous Counter Clearing for MTU6 and MTU7

Figure 20.100 shows an example of procedure for specifying synchronous counter clearing for MTU6 and MTU7 by interrupt generation timing.

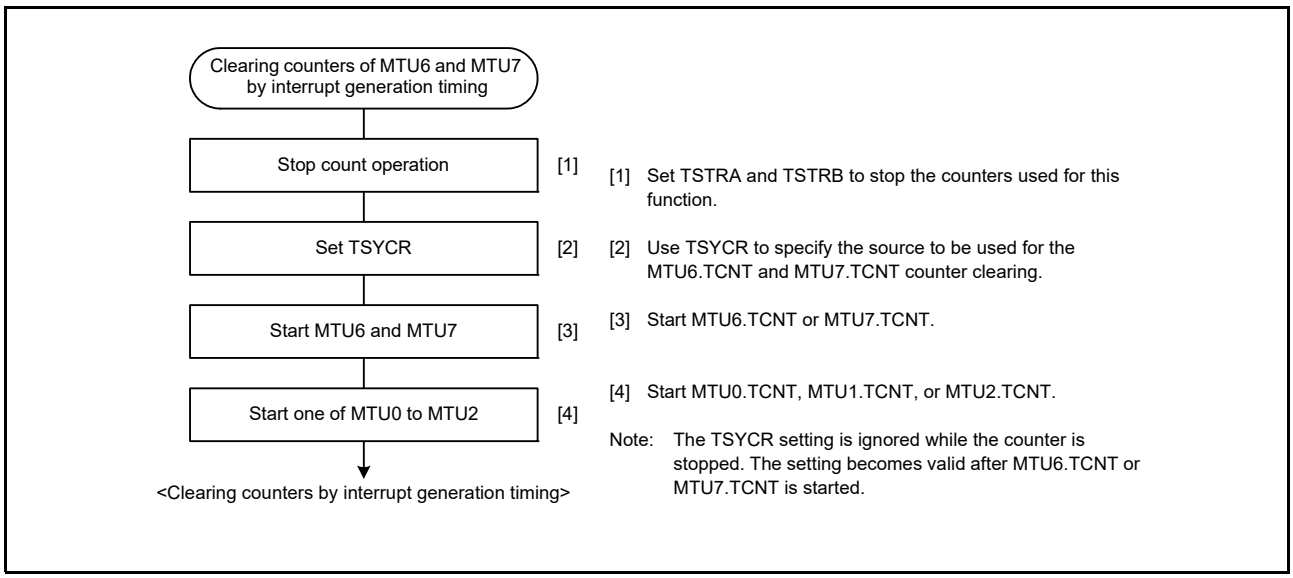


Figure 20.100 Example of Procedure for Specifying Synchronous Counter Clearing for MTU6 and MTU7

(b) Examples of Synchronous Counter Clearing for MTU6 and MTU7

Figure 20.101 and Figure 20.102 show examples of synchronous counter clearing for MTU6 and MTU7 by interrupt generation timing.

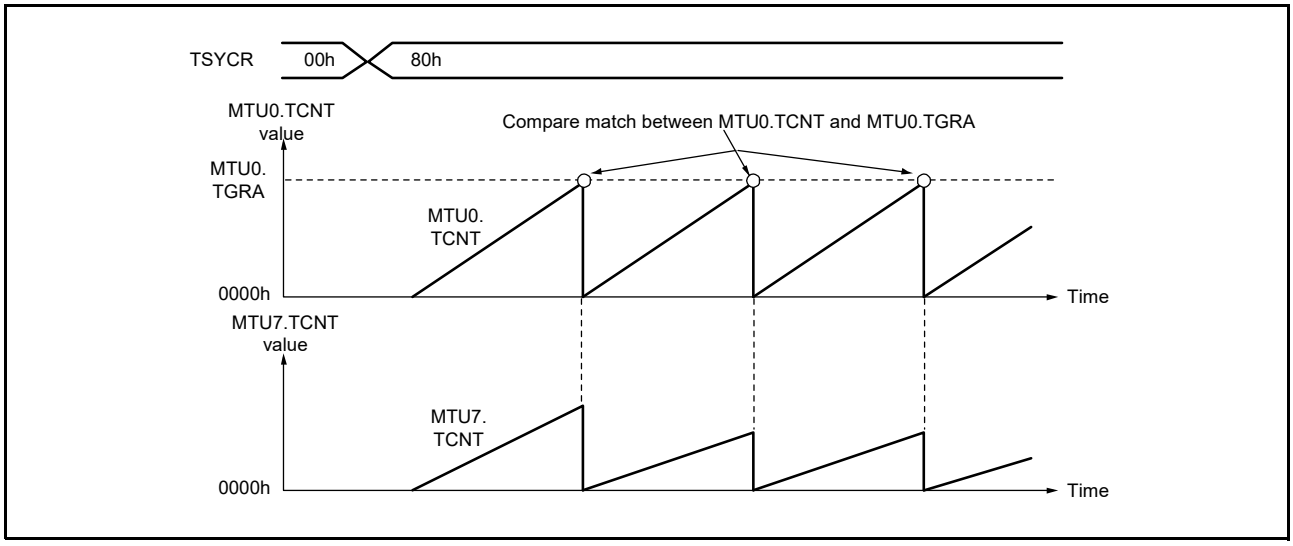


Figure 20.101 Example of Synchronous Counter Clearing for MTU6 and MTU7 (1)

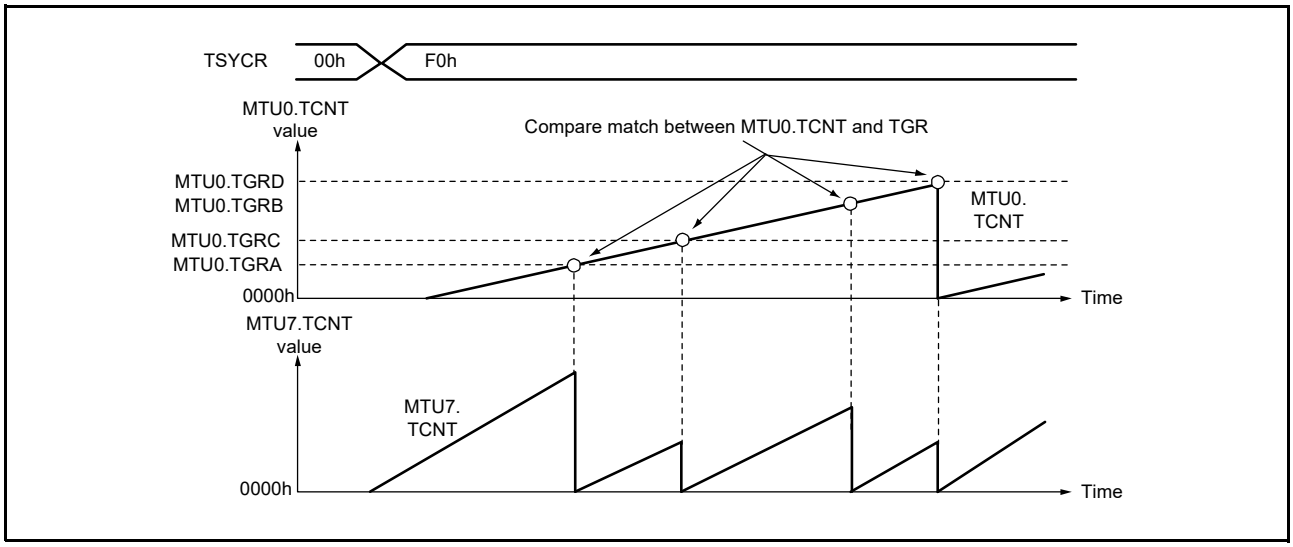


Figure 20.102 Example of Synchronous Counter Clearing for MTU6 and MTU7 (2)

20.3.11 External Pulse Width Measurement

The pulse widths of up to three external input lines can be measured in MTU5.
When the IOC[4:0] bits in MTU5.TIORU, MTU5.TIORV, MTU5.TIORW are set for pulse width measurement, the pulse width of the signal input to the MTIC5U, MTIC5V, and MTIC5W pins are measured. TCNTU, TCNTV, and TCNTW count up while the level specified by the IOC[4:0] bits is input.
Figure 20.103 shows an example of setting external pulse width measurement, and Figure 20.104 an example of external pulse width measurement.

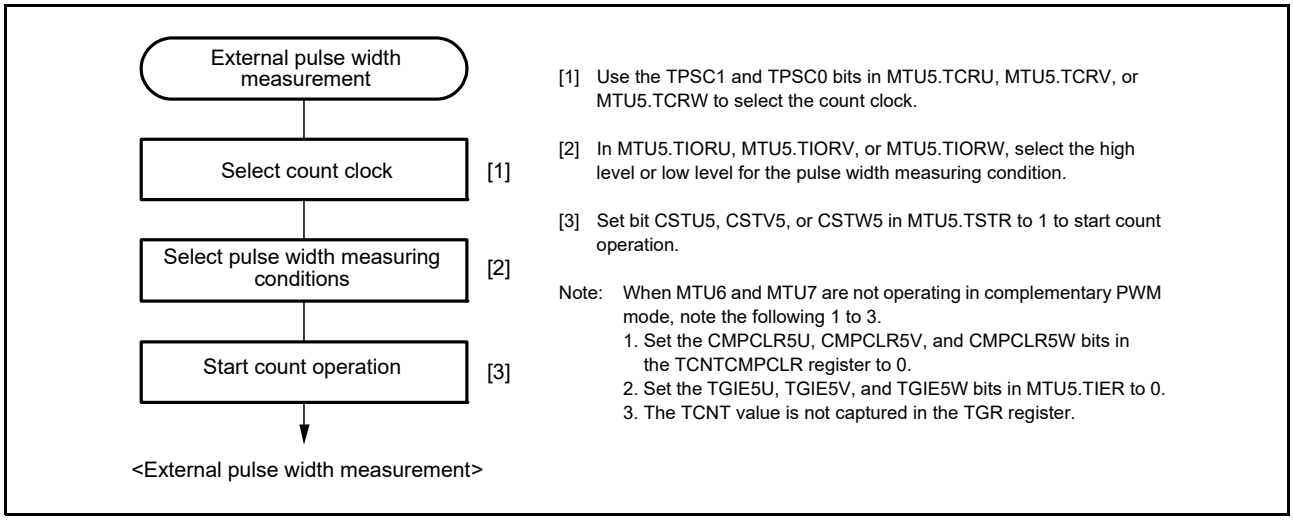


Figure 20.103 Example of External Pulse Width Measurement Setting Procedure

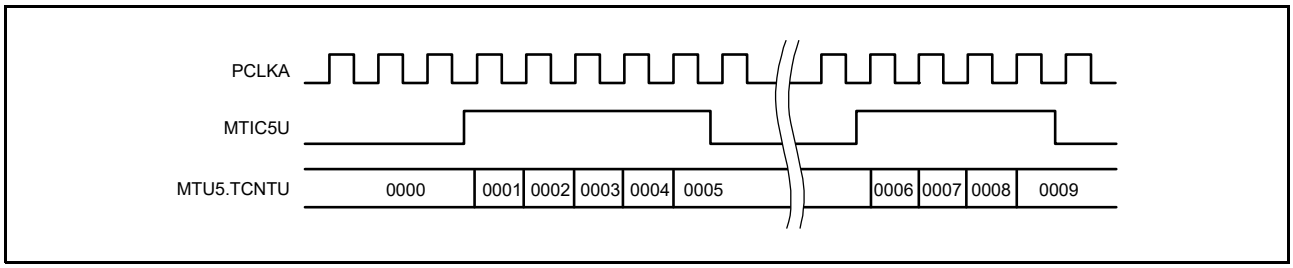


Figure 20.104 Example of External Pulse Width Measurement (Measuring High Pulse Width)

20.3.12 Dead Time Compensation

Figure 20.105 shows an example of the motor control circuit used to feed back a delay in the dead time (delay between complementary PWM output and inverter output) to MTU5. The MTU5 external pulse measurement function allows the delay between the complementary PWM output and inverter output to be measured and reflected in the duty ratio, which can be used as dead time compensation for the PWM output waveform in complementary PWM operation when MTU6 and MTU7 are used (Figure 20.106). Figure 20.107 shows the procedure for setting dead time compensation using MTU5. For details on MTU5 operation at this time, refer to section 20.3.13, TCNTU, TCNTV, and TCNTW Capture at Crest and/or Trough in Complementary PWM Mode.

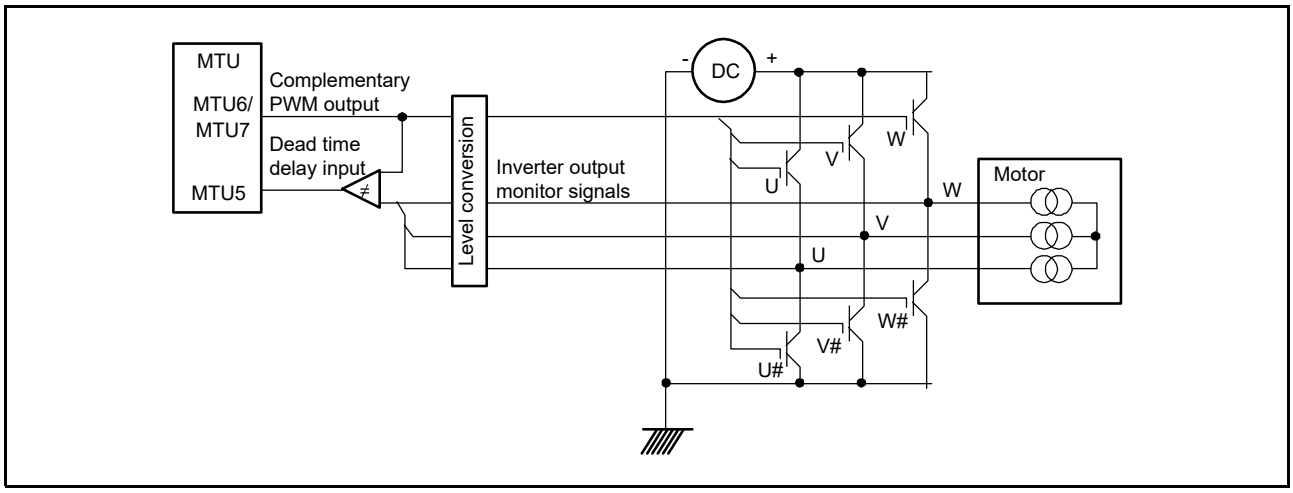


Figure 20.105 Motor Control Circuit Example

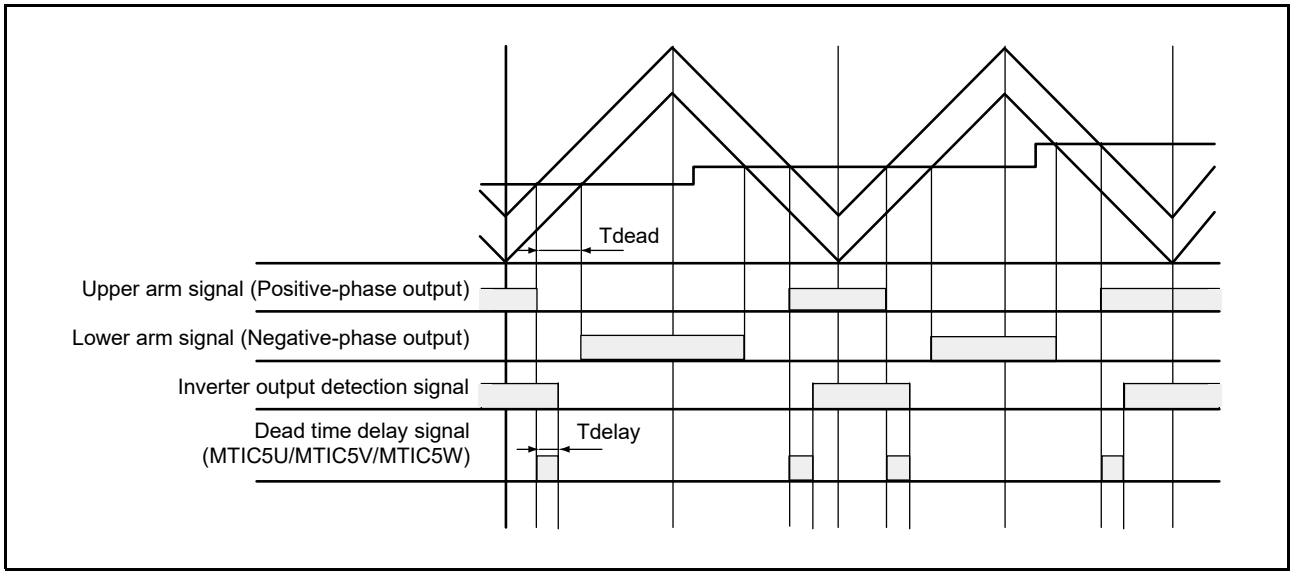
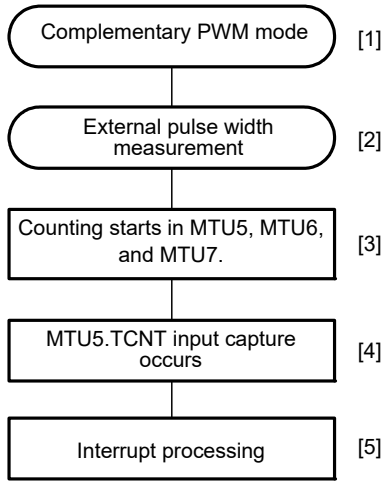


Figure 20.106 Delay in Dead Time in Complementary PWM Operation

(1) Example of Dead Time Compensation Setting Procedure

Figure 20.107 shows an example of dead time compensation setting procedure by using three counters in MTU5.



[1] Set MTU6 and MTU7 to complementary PWM mode. For details, refer to section 20.3.8, Complementary PWM Mode.

[2] Specify the external pulse width measurement function for the target TIOR in MTU5. For details, refer to section 20.3.11, External Pulse Width Measurement.

[3] Set bits CST6 and CST7 in TSTRB and bits CSTU5, CSTV5, and CSTW5 in MTU5.TSTR to 1 to start count operation.

[4] When the capture condition specified in TIOR is satisfied, the MTU5.TCNT value is captured in MTU5.TGR.
To prevent the generation of the MTU5.TGIm5 interrupt (m = U, V, W) request under the capture condition specified in TIOR, do not enable interrupt requests in MTU5.TIER.

[5] For U-phase dead time compensation, when an interrupt is generated at the crest (TGIA6) or trough (TCIV7) in complementary PWM mode, read the MTU5.TGRU value, calculate the difference in time between MTU6.TGRB and MTU5.TGRU, and write the corrected value to MTU6.TGRD in the interrupt processing.
For the V phase and W phase, read the MTU5.TGRV and MTU5.TGRW values and write the corrected values to MTU7.TGRC and TGRD, respectively, in the same way as for U-phase compensation.
The MTU5.TCNT value should be cleared through the TCNTCMPCLR setting or by software.

Note: The MPC and port mode registers (PMR) of the I/O ports should be set up in advance.
As the interrupt flag is set under the capture condition specified in TIOR, do not enable interrupt requests in MTU5.TIER.

Figure 20.107 Example of Dead Time Compensation Setting Procedure

20.3.13 TCNTU, TCNTV, and TCNTW Capture at Crest and/or Trough in Complementary PWM Mode

The MTU5 external pulse width measurement function can be used to transfer the value in TCNTU, TCNTV, and TCNTW to TGRU, TGRV, and TGRW at the crest, or trough, or crest and trough. The transfer timing is set in TIORU, TIORV, and TIORW. When the CMPCLR5U, CMPCLR5V, and CMPCLR5W bits in the TCNTCMPCLR register are set to 1, TCNTU, TCNTV, and TCNTW are cleared to 0 at the transfer timing for TGRU, TGRV, and TGRW.
Figure 20.108 shows an operation example in which TCNTU is used as a free-running counter without being cleared, and the value is captured in TGRU at the crest or trough in complementary PWM mode.

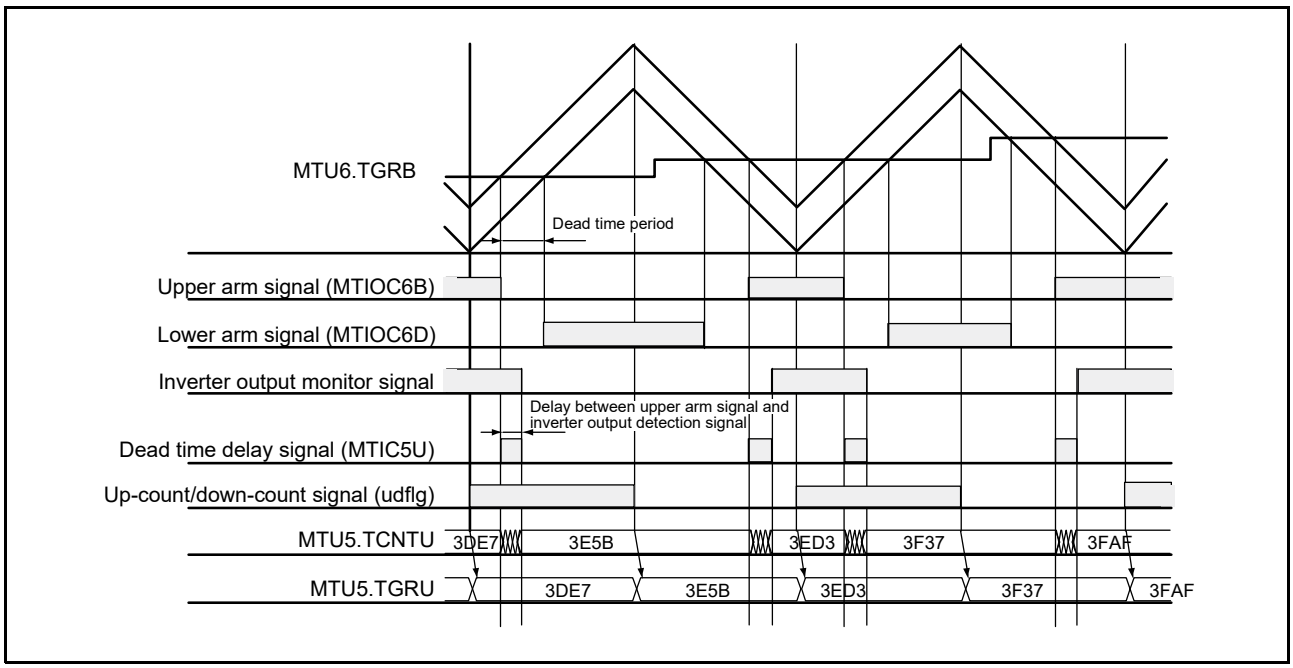


Figure 20.108 TCNTU Capture at Crest and/or Trough in Complementary PWM Operation

20.3.14 Noise Filter Function

The input capture input pins and external pulse input pins have a noise filter function.
Set the NFCRn register (n = 0 to 7, 9, C) to enable or disable the noise filter function and set the sampling clock. The noise filter for each pin can be enabled or disabled individually, and the sampling clock can be set for each channel.
Figure 20.109 shows the timing of noise filtering.

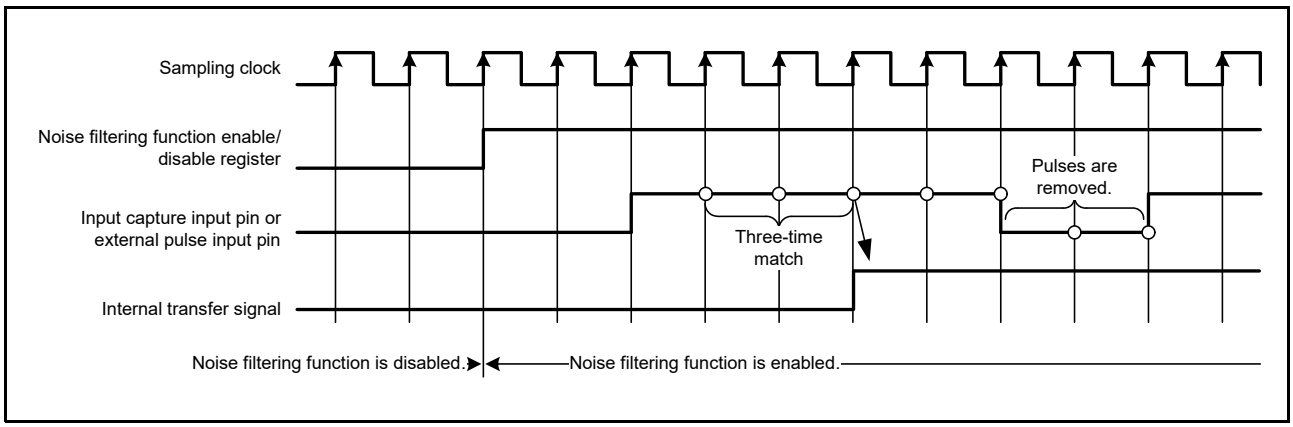


Figure 20.109 Timing of Noise Filtering

20.3.15 A/D Conversion Start Request Frame Synchronization Signal

This function can be used to monitor the generation timing of the A/D conversion start request signal using an external pin.

When the A/D conversion request signal to be monitored is selected by the TADSTRGRn register (n = 0, 1), a pulse signal is output from the ADSMn pin that is at the high level when the A/D conversion start request signal is generated, and at the low level in the timer cycle used to generate the A/D conversion start request signal.

Figure 20.110 shows an example of outputting the A/D conversion start request frame synchronization signal.

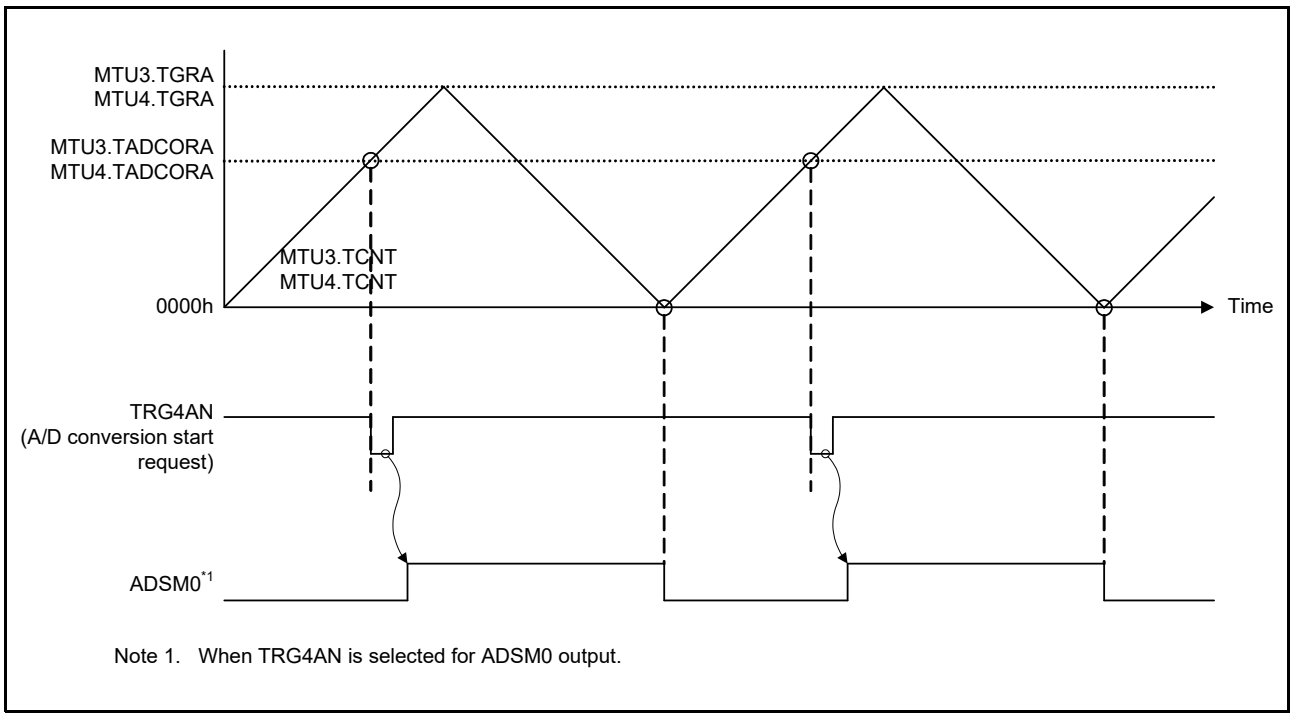


Figure 20.110 Example of Outputting A/D Conversion Start Request Frame Synchronization Signal

20.4 Interrupt Sources

20.4.1 Interrupt Sources and Priorities

There are three kinds of interrupt source; TGR input capture/compare match, TCNT overflow, and TCNT underflow. Each interrupt source has its own enable/disable bit, allowing the generation of interrupt request signals to be enabled or disabled individually.

When an interrupt source is generated, if the corresponding enable/disable bit in TIER is set to 1, an interrupt is requested.

Relative channel priorities can be changed by the interrupt controller; however the priority within a channel is fixed. For details, refer to section 14, Interrupt Controller (ICUb). Table 20.79 lists the MTU interrupt sources.

Table 20.79 MTU Interrupt Sources

Channel	Name	Interrupt Source	DTC Activation	Priority
MTU0	TGIA0	MTU0.TGRA input capture/compare match	Possible	High
	TGIB0	MTU0.TGRB input capture/compare match	Possible	
	TGIC0	MTU0.TGRC input capture/compare match	Possible	
	TGID0	MTU0.TGRD input capture/compare match	Possible	
	TCIV0	MTU0.TCNT overflow	Not possible	
	TGIE0	MTU0.TGRE compare match	Not possible	
	TGIF0	MTU0.TGRF compare match	Not possible	
MTU1	TGIA1	MTU1.TGRA input capture/compare match	Possible	
	TGIB1	MTU1.TGRB input capture/compare match	Possible	
	TCIV1	MTU1.TCNT overflow	Not possible	
	TCIU1	MTU1.TCNT underflow	Not possible	
MTU2	TGIA2	MTU2.TGRA input capture/compare match	Possible	
	TGIB2	MTU2.TGRB input capture/compare match	Possible	
	TCIV2	MTU2.TCNT overflow	Not possible	
	TCIU2	MTU2.TCNT underflow	Not possible	
MTU3	TGIA3	MTU3.TGRA input capture/compare match	Possible	
	TGIB3	MTU3.TGRB input capture/compare match	Possible	
	TGIC3	MTU3.TGRC input capture/compare match	Possible	
	TGID3	MTU3.TGRD input capture/compare match	Possible	
	TCIV3	MTU3.TCNT overflow	Not possible	
MTU4	TGIA4	MTU4.TGRA input capture/compare match	Possible	
	TGIB4	MTU4.TGRB input capture/compare match	Possible	
	TGIC4	MTU4.TGRC input capture/compare match	Possible	
	TGID4	MTU4.TGRD input capture/compare match	Possible	
	TCIV4	MTU4.TCNT overflow/underflow*1	Possible	
MTU5	TGIU5	MTU5.TGRU input capture/compare match	Possible	
	TGIV5	MTU5.TGRV input capture/compare match	Possible	
	TGIW5	MTU5.TGRW input capture/compare match	Possible	
MTU6	TGIA6	MTU6.TGRA input capture/compare match	Possible	
	TGIB6	MTU6.TGRB input capture/compare match	Possible	
	TGIC6	MTU6.TGRC input capture/compare match	Possible	
	TGID6	MTU6.TGRD input capture/compare match	Possible	
	TCIV6	MTU6.TCNT overflow	Not possible	
MTU7	TGIA7	MTU7.TGRA input capture/compare match	Possible	
	TGIB7	MTU7.TGRB input capture/compare match	Possible	
	TGIC7	MTU7.TGRC input capture/compare match	Possible	
	TGID7	MTU7.TGRD input capture/compare match	Possible	
	TCIV7	MTU7.TCNT overflow/underflow*1	Possible	
MTU9	TGIA9	MTU9.TGRA input capture/compare match	Possible	
	TGIB9	MTU9.TGRB input capture/compare match	Possible	
	TGIC9	MTU9.TGRC input capture/compare match	Possible	
	TGID9	MTU9.TGRD input capture/compare match	Possible	
	TCIV9	MTU9.TCNT overflow	Not possible	
	TGIE9	MTU9.TGRE compare match	Not possible	
	TGIF9	MTU9.TGRF compare match	Not possible	Low

Note: This table shows the initial state immediately after a reset. The relative channel priorities can be changed by the interrupt controller.

Note 1. Only in complementary PWM mode

(1) Input Capture/Compare Match Interrupt

If the TIER.TGIE bit is set to 1 when a TGR input capture/compare match occurs on a channel, an interrupt is requested. The MTU has 35 input capture/compare match interrupts (six for MTU0 and MTU9, four each for MTU3, MTU4, MTU6, and MTU7, two each for MTU1 and MTU2, and three for MTU5).

(2) Overflow Interrupt

If the TIER.TCIEV bit is set to 1 when a TCNT overflow occurs on a channel, clearing an interrupt is requested. The MTU has eight overflow interrupts (one for each channel except MTU5).

(3) Underflow Interrupt

If the TIER.TCIEU bit is set to 1 when a TCNT underflow occurs on a channel, an interrupt is requested. The MTU has two underflow interrupts (one each for MTU1, and MTU2).

20.4.2 DTC Activation

(1) DTC Activation

The DTC can be activated by the TGR input capture/compare match interrupt in each channel or the overflow interrupt in MTU4 and MTU7. For details, refer to section 17, Data Transfer Controller (DTCa).
The MTU provides a total of 33 input capture/compare match interrupts and overflow interrupts that can be used as DTC activation sources: four each for MTU0, MTU3, MTU6, and MTU9, two each for MTU1 and MTU2, five each for MTU4 and MTU7, and three for MTU5.

20.4.3 A/D Converter Activation

The A/D converter can be activated by one of the following three methods in the MTU. Table 20.80 shows the relationship between interrupt sources and A/D converter start request signals.

(1) A/D Converter Activation by TGRA Input Capture/Compare Match or at MTU4.TCNT (MTU7.TCNT) Trough in Complementary PWM Mode

The A/D converter can be activated by the occurrence of a TGRA input capture/compare match in each channel. In addition, if complementary PWM operation is performed while the TTGE2 bit in MTU4.TIER (MTU7.TIER) is set to 1, the A/D converter can be activated at the trough of MTU4.TCNT (MTU7.TCNT) count (MTU4.TCNT (MTU7.TCNT) = 0000h).
A/D converter start request signal TRGAnN is issued to the A/D converter under either of the following conditions (n = 0 to 4, 6, 7, 9).

- When a TGRA input capture/compare match occurs on a channel while the TIER.TTGE bit is set to 1
- When the MTU4.TCNT (MTU7.TCNT) count reaches the trough (MTU4.TCNT (MTU7.TCNT) = 0000h) during complementary PWM operation while the TTGE2 bit in MTU4.TIER (MTU7.TIER) is set to 1

When either condition is satisfied, if A/D converter start signal TRGAnN from the MTU is selected as the trigger in the A/D converter, A/D conversion will start.

(2) A/D Converter Activation by Compare Match between MTU0.TCNT and MTU0.TGRE, or MTU9.TCNT and MTU9.TGRE

A/D converter start request signal TRG0N and TRG9N is issued to the A/D converter when a compare match occurs between MTU0.TCNT and MTU0.TGRE, MTU9.TCNT and MTU9.TGRE.
When a compare match occurs between MTU0.TCNT and MTU0.TGRE, MTU9.TCNT and MTU9.TGRE while the TTGE2 bit in MTU0.TIER2, MTU9.TIER2 are set to 1, A/D converter start request TRG0N, TRG0AEN, TRG9N, TRG9AEN, or TRG09N is issued to the A/D converter. If A/D converter start signal TRG0N, TRG0AEN, TRG9N, TRG9AEN, or TRG09N from the MTU is selected as the trigger in the A/D converter, A/D conversion will start.

(3) A/D Converter Activation by A/D Converter Start Request Delaying Function

The A/D converter can be activated by generating A/D converter start request signal TRG4AN or TRG4BN (TRG7AN or TRG7BN) when the MTU4.TCNT (MTU7.TCNT) count matches the MTU4.TADCORA or MTU4.TADCORB (MTU7.TADCORA or MTU7.TADCORB) value if the UT4AE, DT4AE, UT4BE, or DT4BE (UT7AE, DT7AE, UT7BE, or DT7BE) bit in the A/D converter start request control register (MTU4.TADCR (MTU7.TADCR)) is set to 1. For details, refer to section 20.3.9, A/D Converter Start Request Delaying Function.
A/D conversion will start when TRG4AN (TRG7AN) is generated if A/D converter start signal TRG4AN (TRG7AN) from the MTU is selected as the trigger in the A/D converter, when TRG4BN (TRG7BN) is generated if TRG4BN (TRG7BN) from the MTU is selected as the trigger in the A/D converter, or when TRG4ABN (TRG7ABN) is generated if TRG4ABN (TRG7ABN) from the MTU is selected as the trigger in the A/D converter.

Table 20.80 Interrupt Sources and A/D Converter Start Request Signals

Target Registers	Interrupt Source	A/D Converter Start Request Signal
MTU0.TGRA and MTU0.TCNT	Input capture/compare match	TRGA0N
MTU9.TGRA and MTU9.TCNT		TRGA9N
MTU9.TGRA and MTU9.TCNT, MTU9.TGRE and MTU9.TCNT*1		TRG9AEN
MTU0.TGRA and MTU0.TCNT, MTU0.TGRE and MTU0.TCNT*1		TRG0AEN
MTU0.TGRA and MTU0.TCNT, MTU9.TGRA and MTU9.TCNT		TRGA09N
MTU1.TGRA and MTU1.TCNT		TRGA1N
MTU2.TGRA and MTU2.TCNT		TRGA2N
MTU3.TGRA and MTU3.TCNT		TRGA3N
MTU4.TGRA and MTU4.TCNT*2		TRGA4N
MTU4.TCNT	MTU4.TCNT trough in complementary PWM mode	
MTU6.TGRA and MTU6.TCNT	Input capture/compare match	TRGA6N
MTU7.TGRA and MTU7.TCNT*2		TRGA7N
MTU7.TCNT	MTU7.TCNT trough in complementary PWM mode	
MTU0.TGRE and MTU0.TCNT	Compare match	TRG0N
MTU9.TGRE and MTU9.TCNT		TRG9N
MTU0.TGRE and MTU0.TCNT*1, MTU9.TGRE and MTU9.TCNT*1		TRG09N
MTU4.TADCORA and MTU4.TCNT		TRG4AN
MTU4.TADCORB and MTU4.TCNT		TRG4BN
MTU7.TADCORA and MTU7.TCNT		TRG7AN
MTU7.TADCORB and MTU7.TCNT		TRG7BN
MTU4.TADCORA and MTU4.TCNT, MTU4.TADCORB and MTU4.TCNT	Compare match (interrupt skipping function 2)	TRG4ABN
MTU7.TADCORA and MTU7.TCNT, MTU7.TADCORB and MTU7.TCNT		TRG7ABN

Note 1. Since the compare match source of TGRE is used as the A/D trigger start source, set the MTU0.TIER2.TTGE2 and MTU9.TIER2.TTGE2 to 1.

Note 2. Since PWM waveforms are generated in complementary PWM mode, MTU4.TGRA (MTU7.TGRA) compare match not only with MTU4.TCNT (MTU7.TCNT) but also with MTU3.TCNT (MTU6.TCNT) and TCNTSA (TCNTSB) is detected. Accordingly, when compare match with MTU3.TCNT (MTU6.TCNT) and TCNTSA (TCNTSB) occurs, TRGA4N (TRGA7N) is also generated. When MTU3 and MTU 4 (MTU 6 and MTU7) are made to operate in complementary PWM mode for generating an A/D converter start request, use the A/D converter start request by compare match between MTU4.TCNT (MTU7.TCNT) and MTU4.TADCORA/TADCORB (MTU7.TADCORA/TADCORB).

20.5 Operation Timing

20.5.1 Input/Output Timing

(1) TCNT Count Timing

Figure 20.111 and Figure 20.112 show the TCNT count timing in internal clock operation, Figure 20.113 shows the TCNT count timing in external clock operation (normal mode), and Figure 20.114 shows the TCNT count timing in external clock operation (phase counting mode).

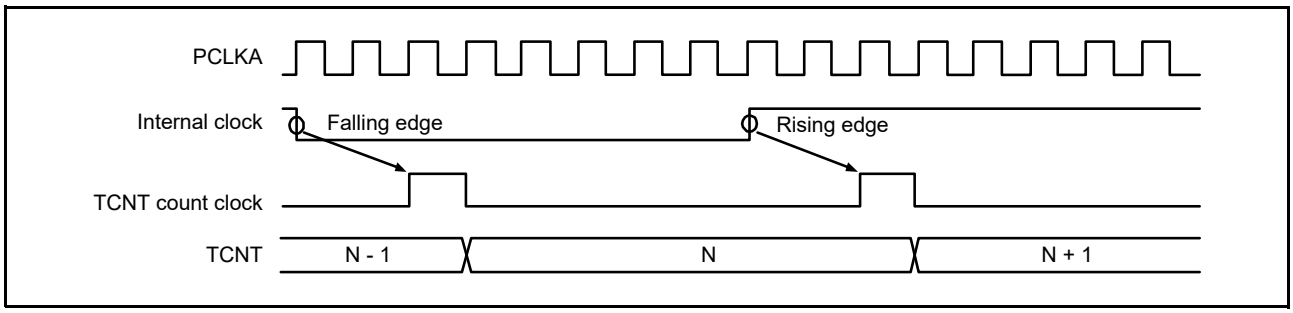


Figure 20.111 Count Timing in Internal Clock Operation (MTU0 to MTU4, MTU6, MTU7, and MTU9)

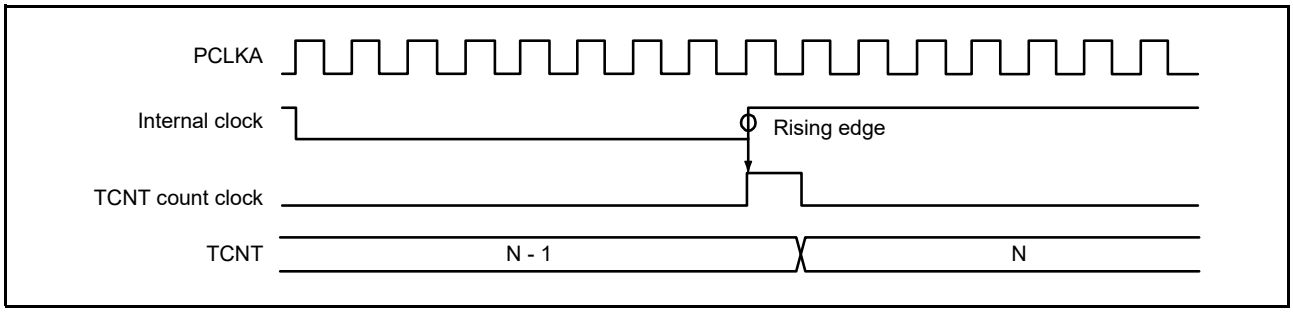


Figure 20.112 Count Timing in Internal Clock Operation (MTU5)

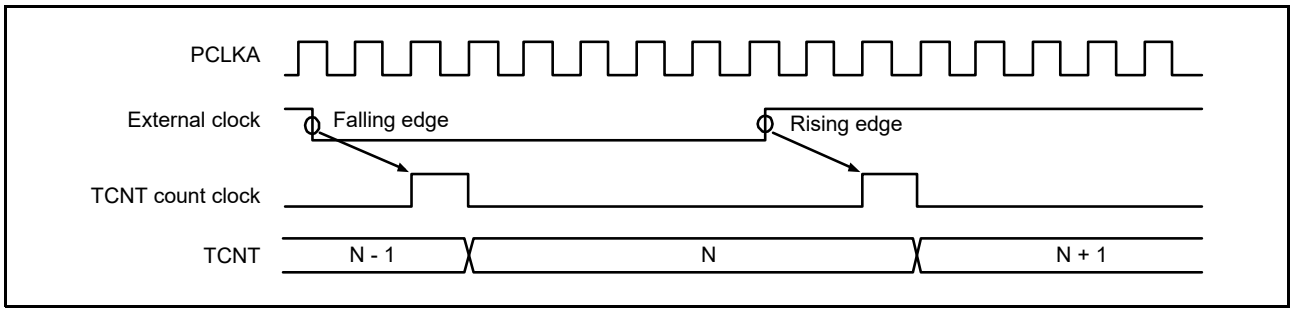


Figure 20.113 Count Timing in External Clock Operation (MTU0 to MTU4, MTU6, MTU7, and MTU9)

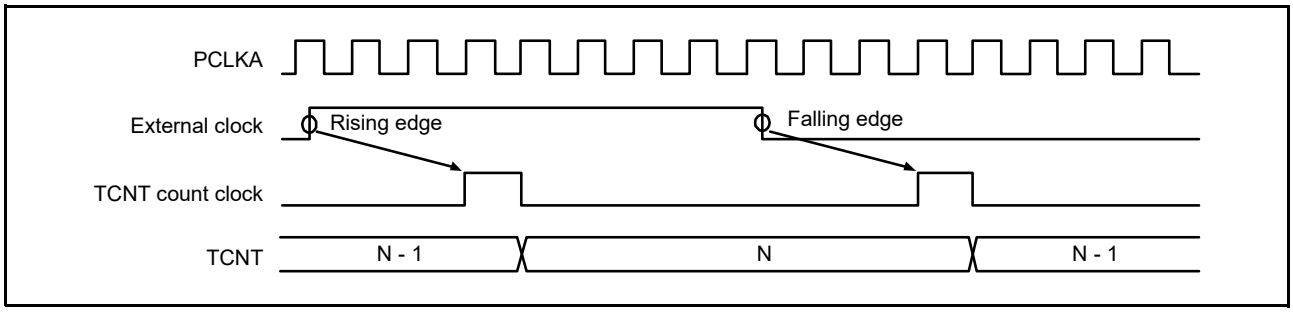


Figure 20.114 Count Timing in External Clock Operation (Phase Counting Mode)

(2) Output Compare Output Timing

A compare match signal is generated in the final state in which TCNT and TGR match (the point at which the count value matched by TCNT is updated). When a compare match signal is generated, the value set in TIOR is output from MTIOCnm pin (n = 0 to 4, 6, 7, 9; m = A to D). After a match between TCNT and TGR, the compare match signal is not generated until the TCNT count clock is generated.

Figure 20.115 shows the output compare output timing (normal mode or PWM mode) and Figure 20.116 shows the output compare output timing (complementary PWM mode or reset-synchronized PWM mode).

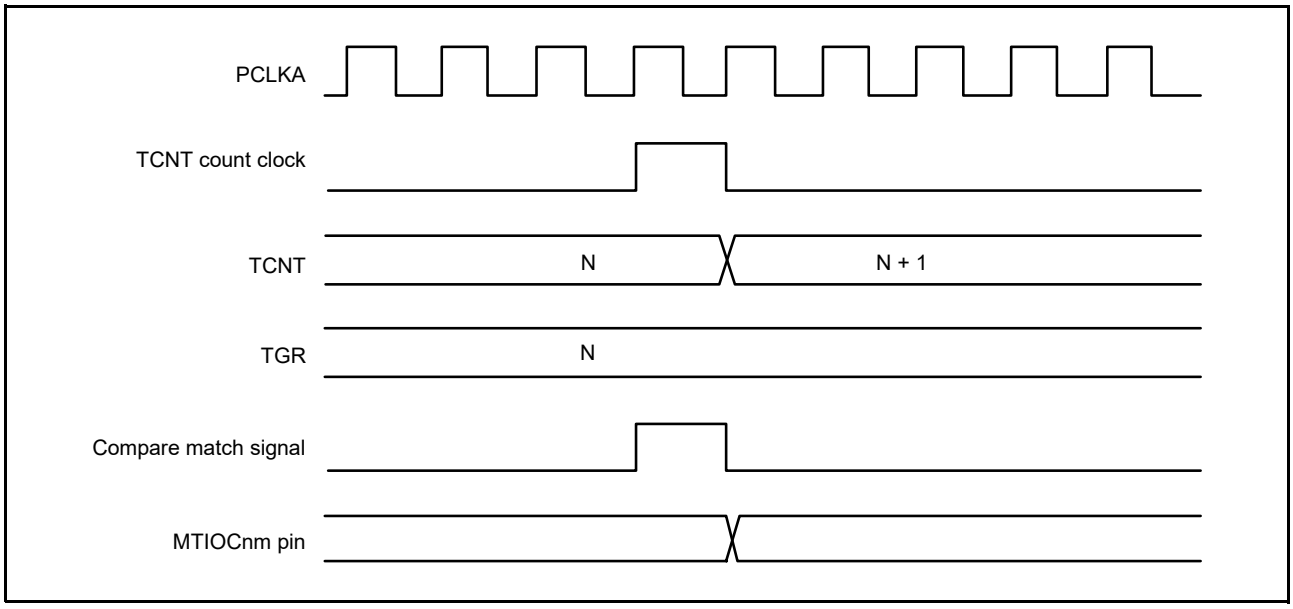


Figure 20.115 Output Compare Output Timing (Normal Mode or PWM Mode) (n = 0 to 4, 6, 7, 9; m = A to D)

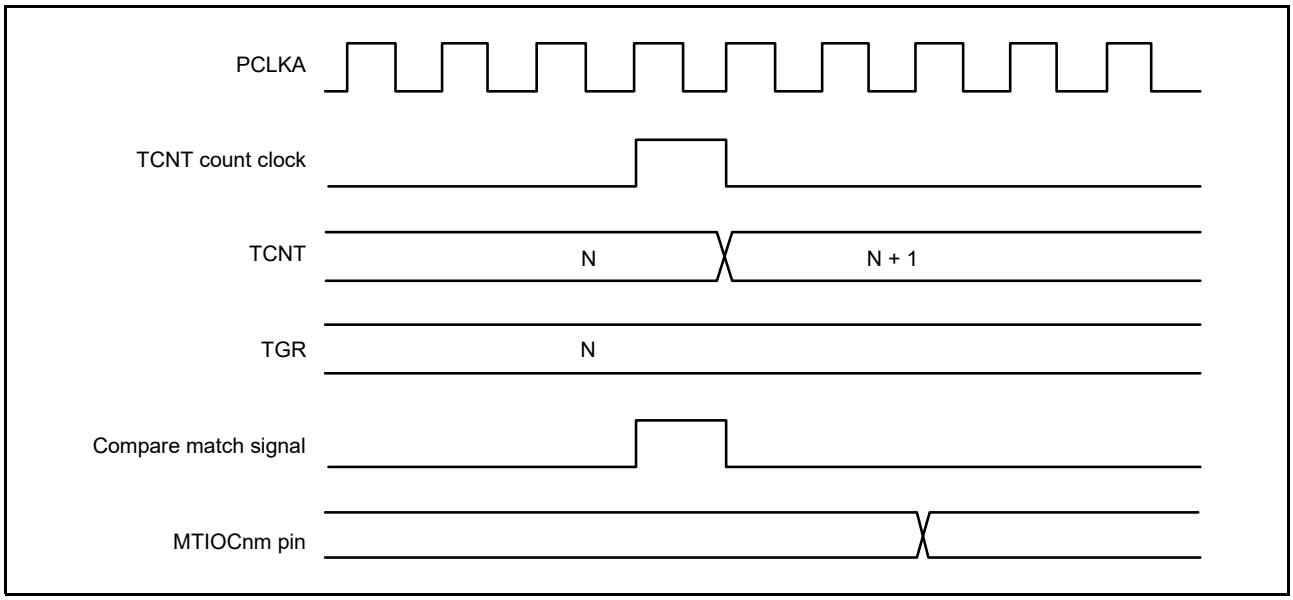


Figure 20.116 Output Compare Output Timing (Complementary PWM Mode or Reset-Synchronized PWM Mode) (n = 0 to 4, 6, 7, 9; m = A to D)

(3) Input Capture Signal Timing

Figure 20.117 shows the input capture signal timing.

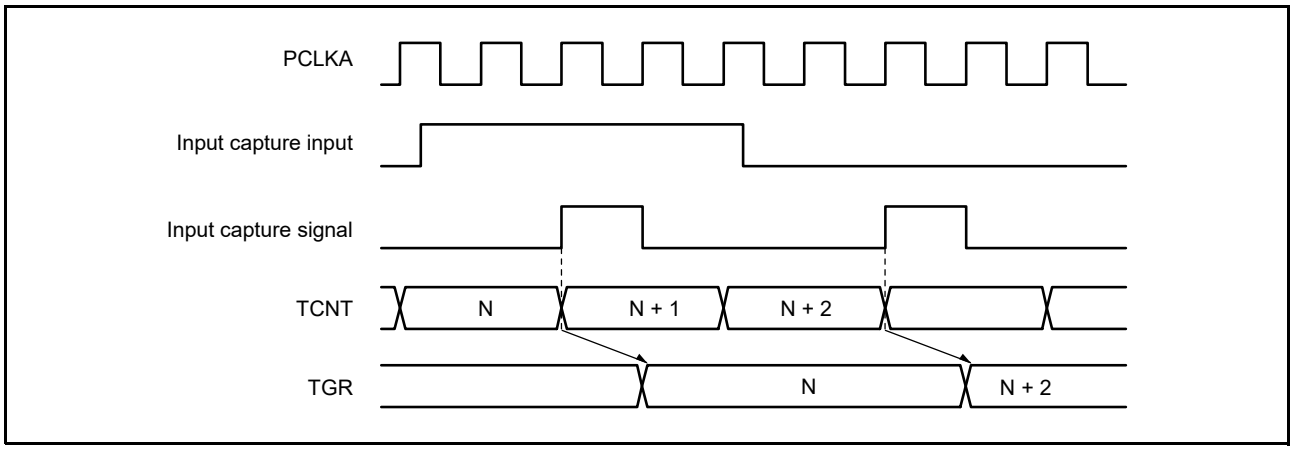


Figure 20.117 Input Capture Input Signal Timing

(4) Timing for Counter Clearing by Compare Match/Input Capture

FFigure 20.118 and Figure 20.119 show the timing when counter clearing on compare match is specified, and Figure 20.120 shows the timing when counter clearing on input capture is specified.

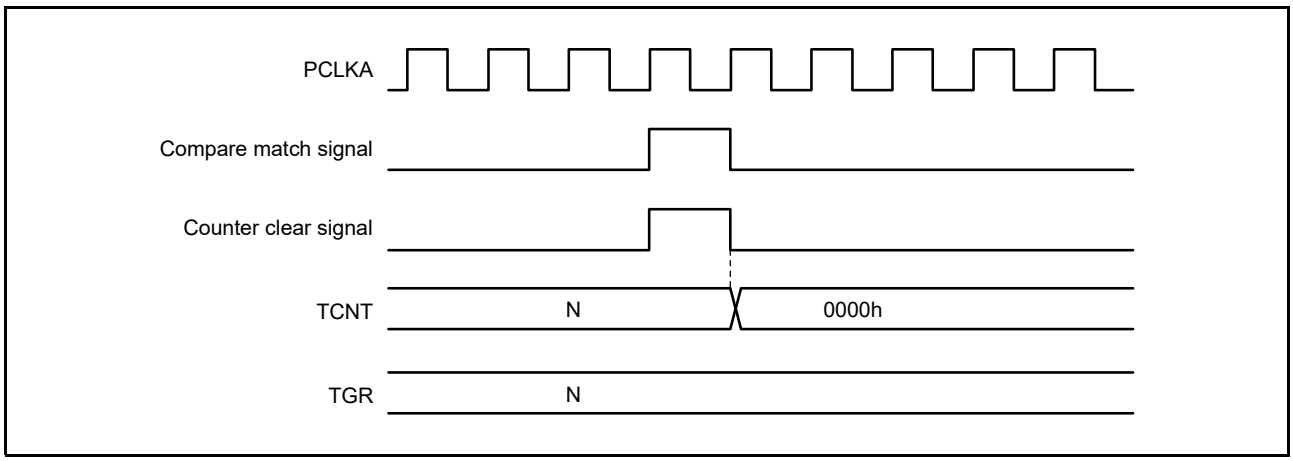


Figure 20.118 Counter Clear Timing (Compare Match) (MTU0 to MTU4, MTU6, MTU7, and MTU9)

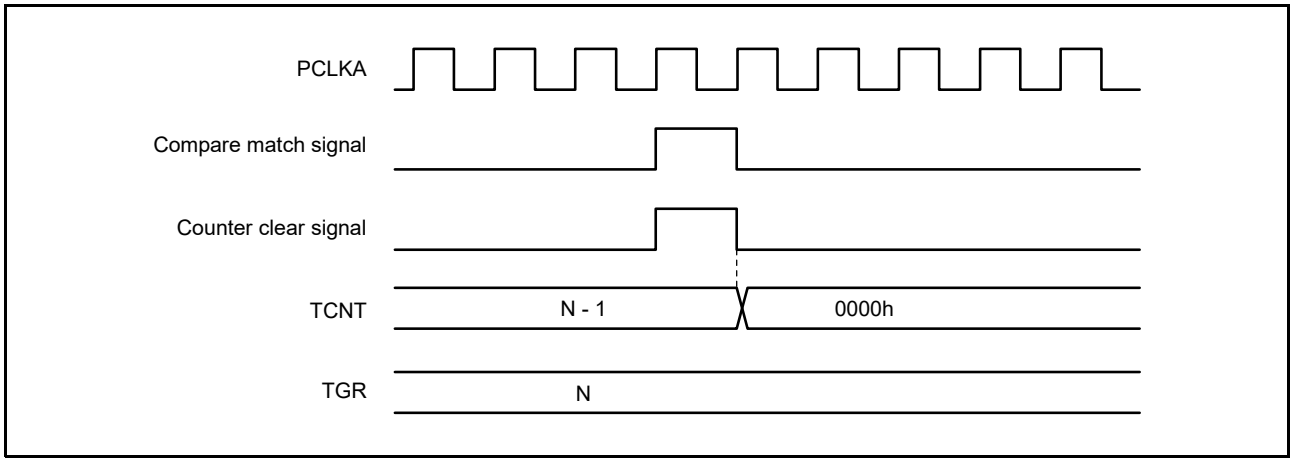


Figure 20.119 Counter Clear Timing (Compare Match) (MTU5)

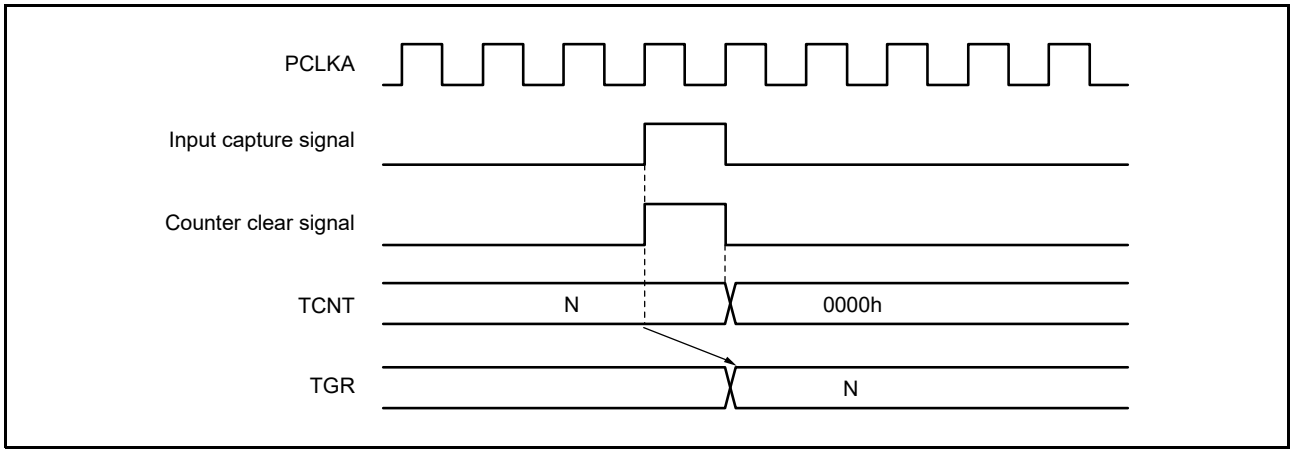


Figure 20.120 Counter Clear Timing (Input Capture) (MTU0 to MTU7, and MTU9)

(5) Buffer Operation Timing

Figure 20.121 to Figure 20.123 show the timing in buffer operation.

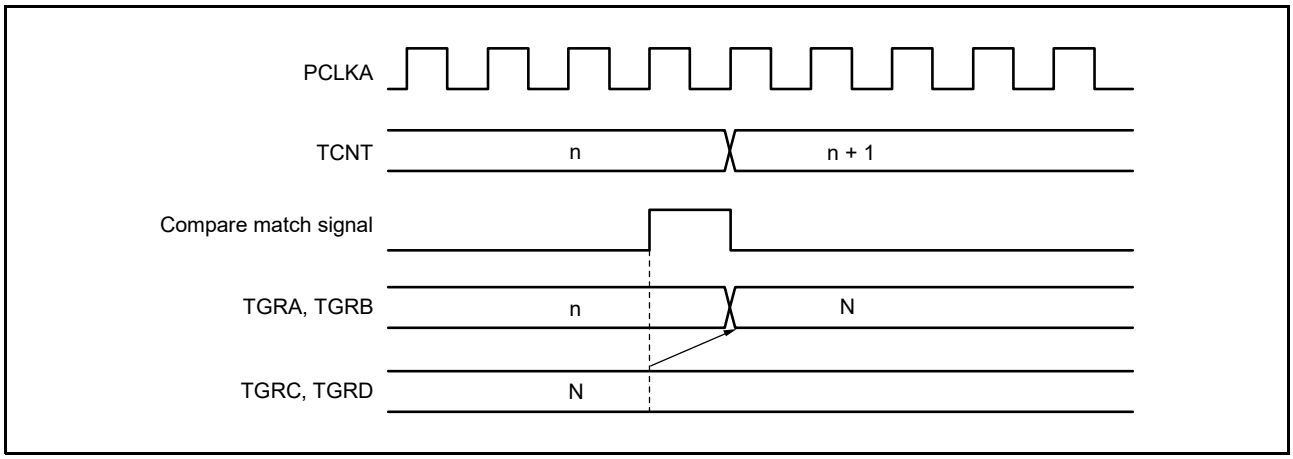


Figure 20.121 Buffer Operation Timing (Compare Match)

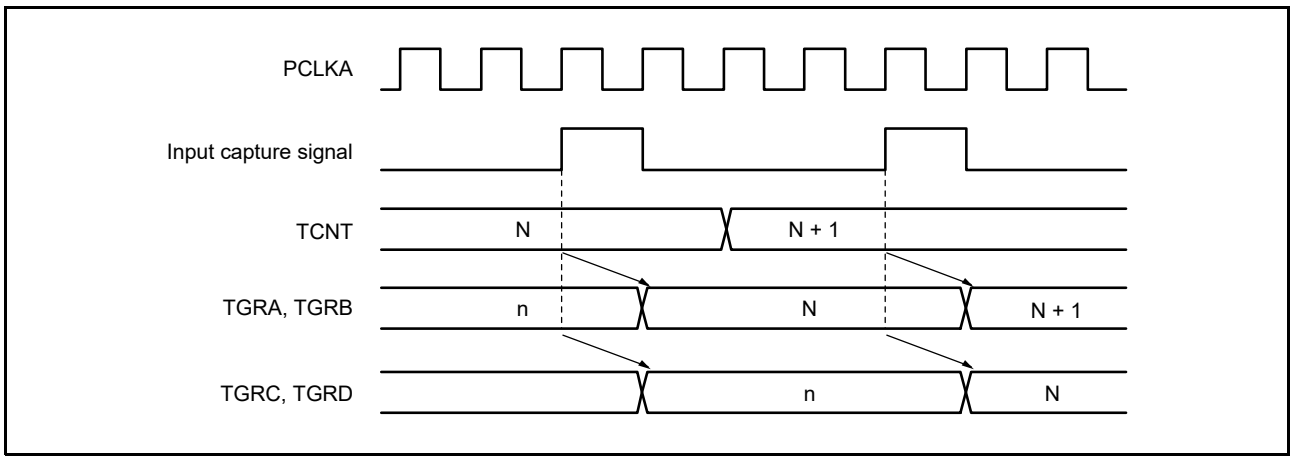


Figure 20.122 Buffer Operation Timing (Input Capture)

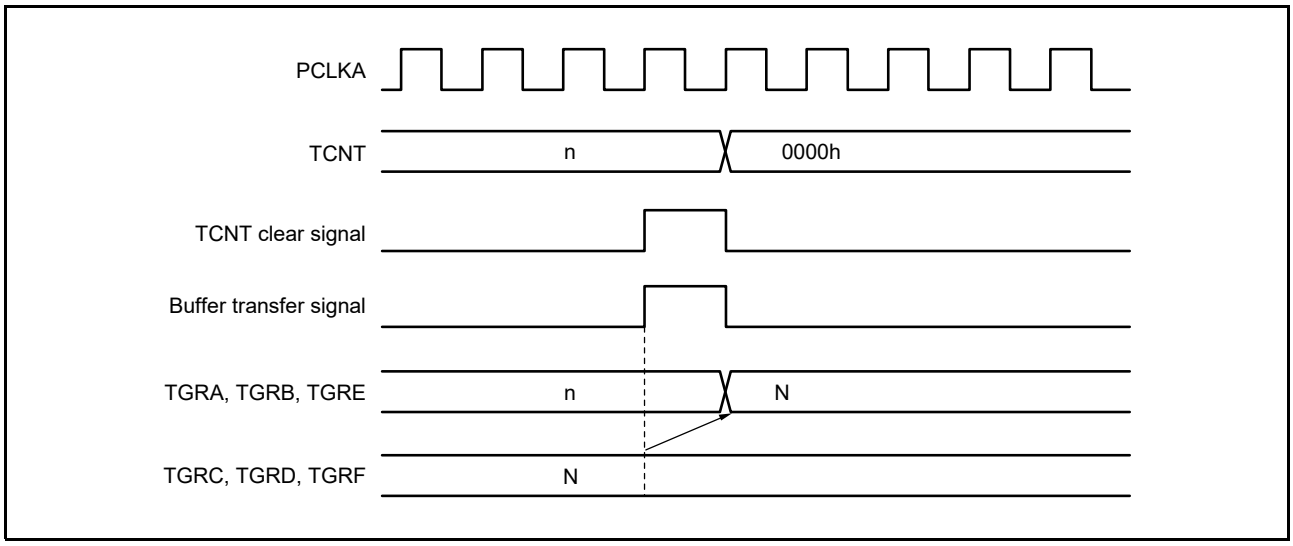


Figure 20.123 Buffer Operation Timing (When TCNT Cleared)

(6) Buffer Transfer Timing (Complementary PWM Mode)

Figure 20.124 to Figure 20.126 show the buffer transfer timing in complementary PWM mode.

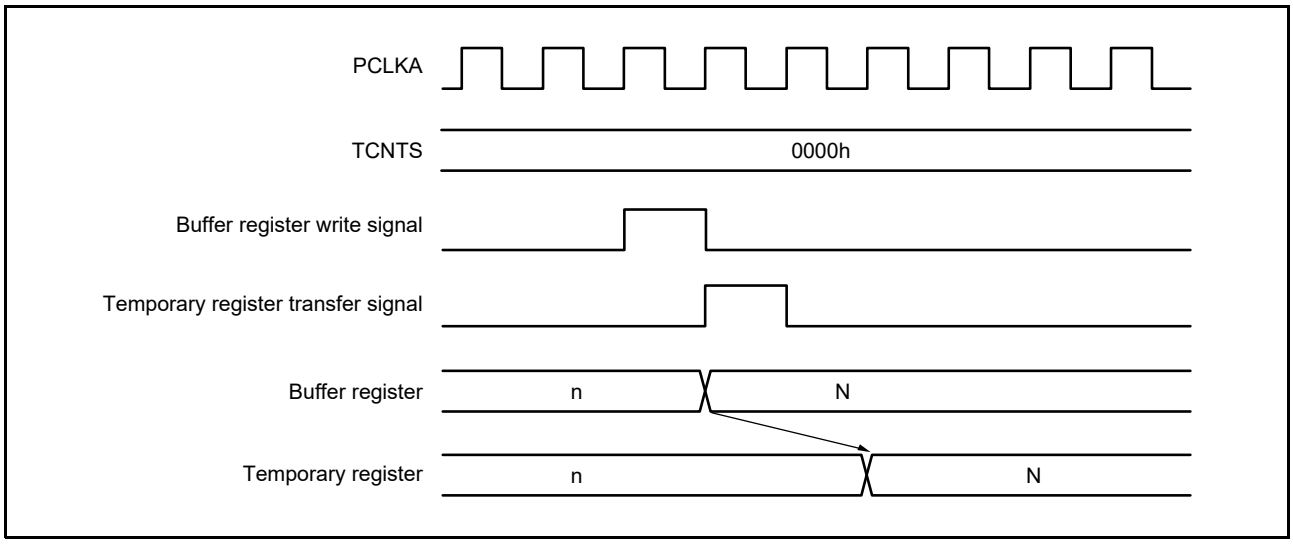


Figure 20.124 Transfer Timing from Buffer Register to Temporary Register (TCNTSA Stopped)

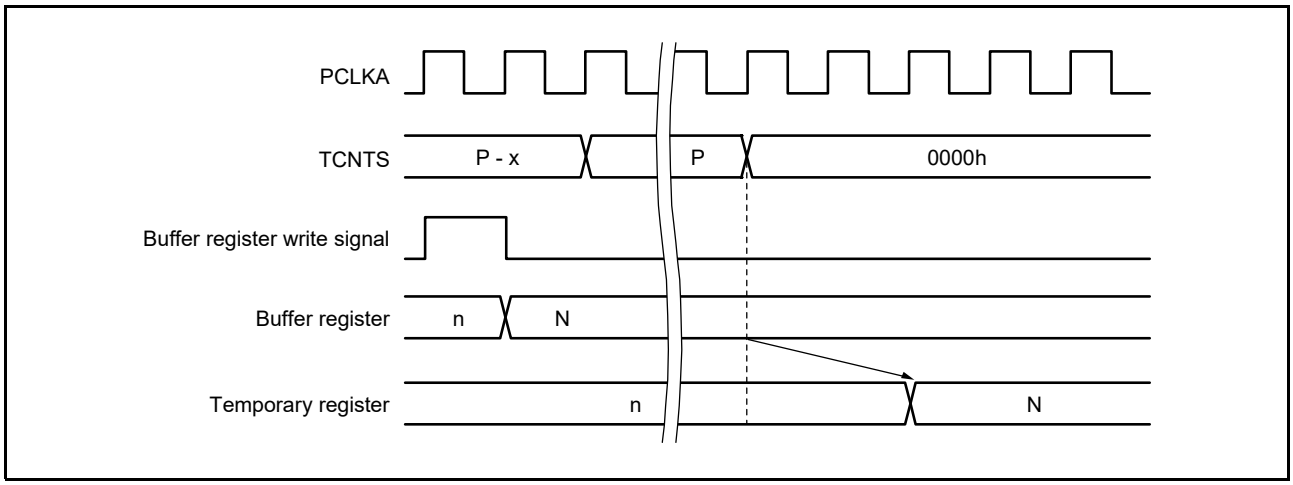


Figure 20.125 Transfer Timing from Buffer Register to Temporary Register (TCNTSA Operating)

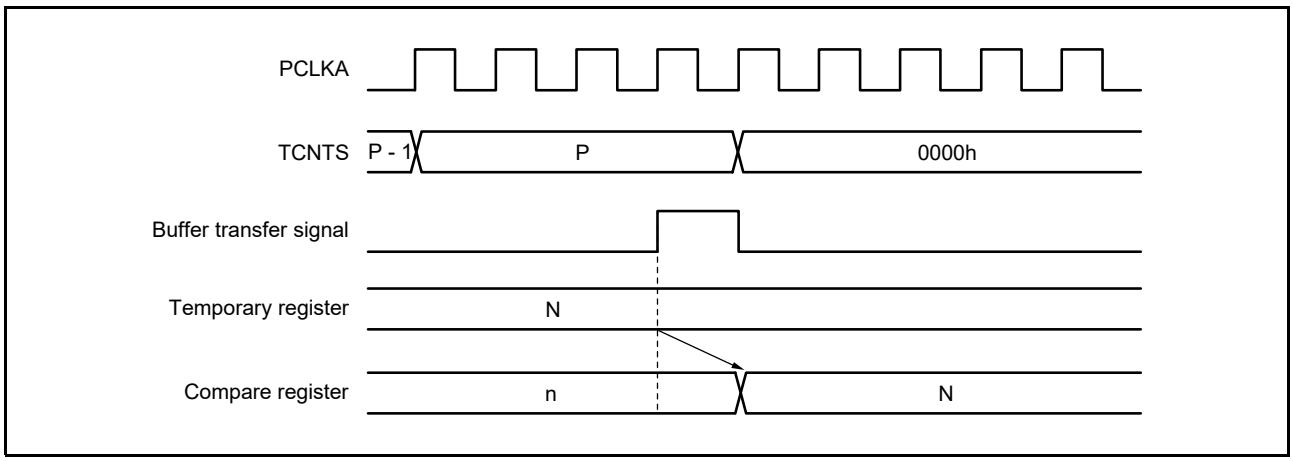


Figure 20.126 Transfer Timing from Temporary Register to Compare Register

20.5.2 Interrupt Signal Timing

(1) TGI Interrupt Timing by Compare Match

Figure 20.127 and Figure 20.128 show the TGI interrupt request signal timing when a compare match occurs.

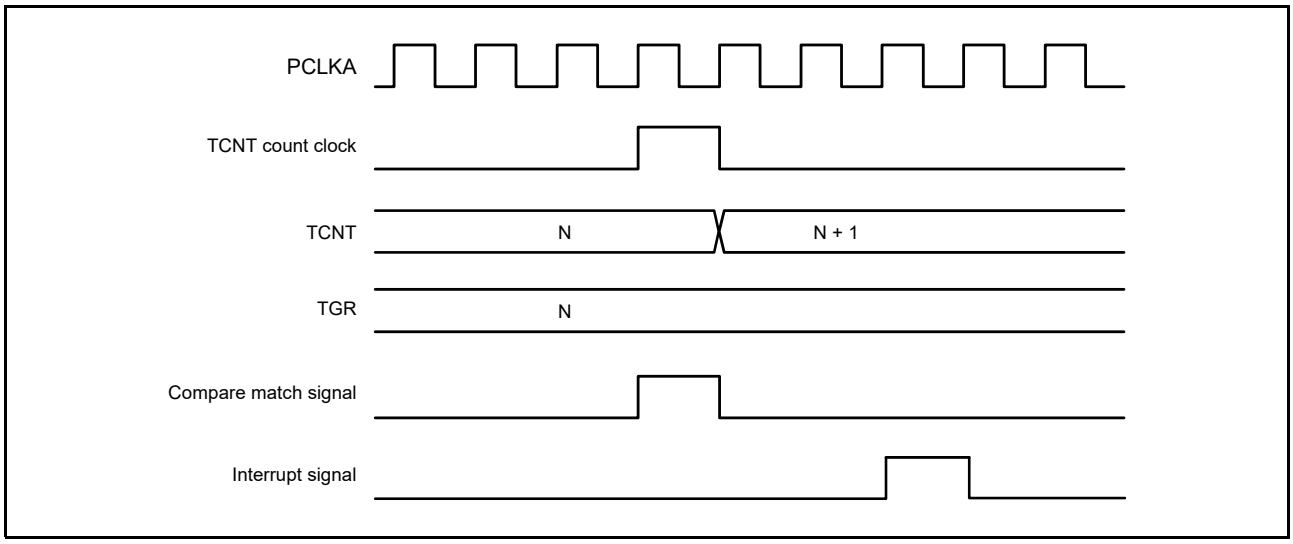


Figure 20.127 TGI Interrupt Timing (Compare Match) (MTU0 to MTU4, MTU6, MTU7, and MTU9)

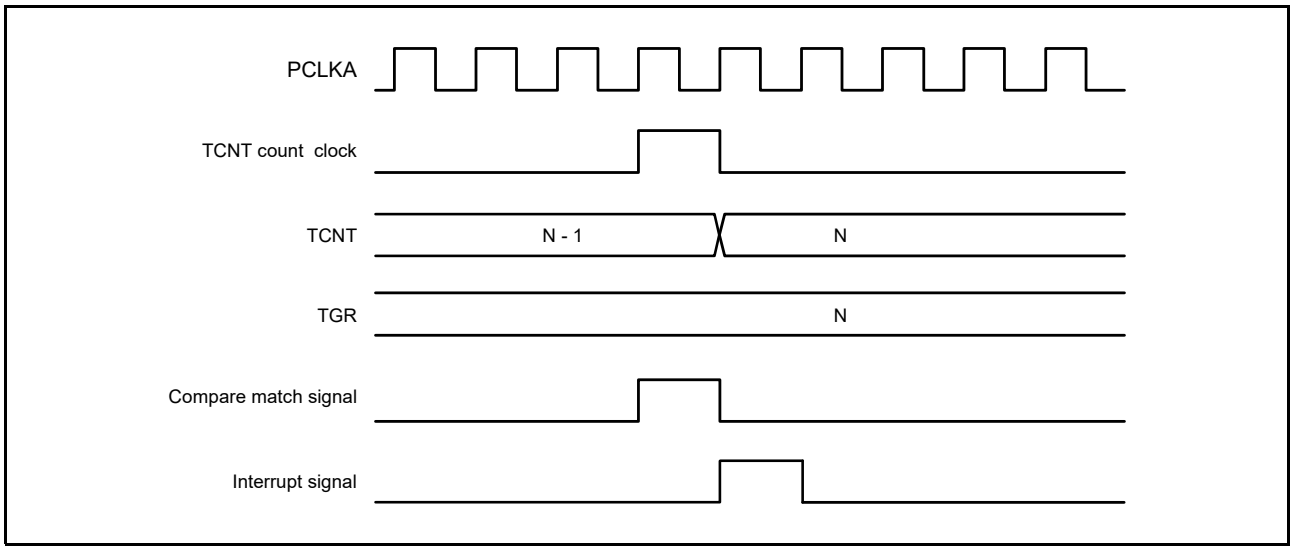


Figure 20.128 TGI Interrupt Timing (Compare Match) (MTU5)

(2) TGI Interrupt Timing by Input Capture

Figure 20.129 and Figure 20.130 show the TGI interrupt request signal timing when an input capture occurs.

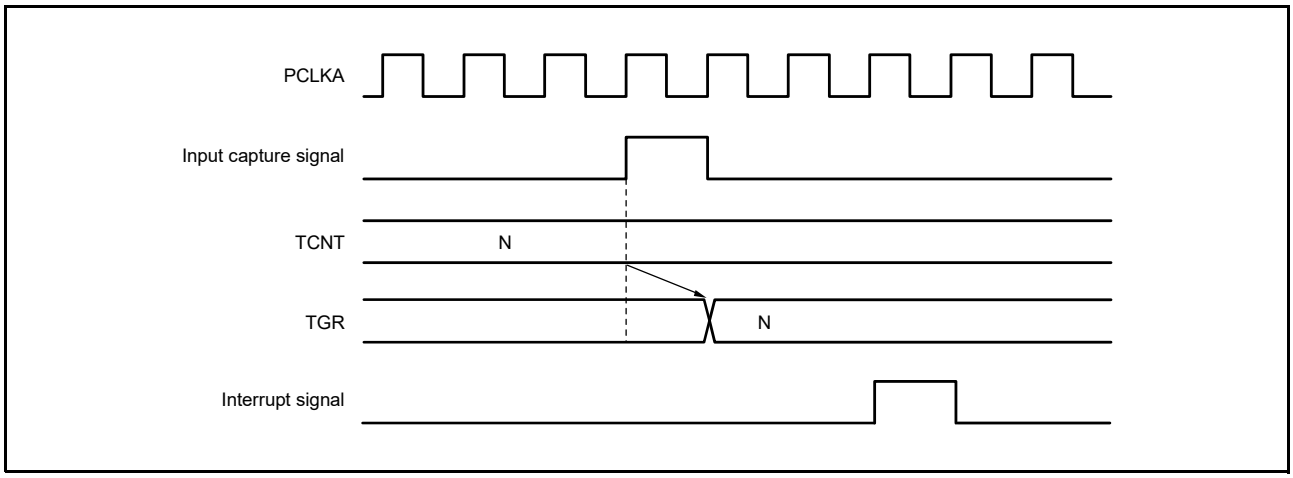


Figure 20.129 TGI Interrupt Timing (Input Capture) (MTU0 to MTU4, MTU6, MTU7, and MTU9)

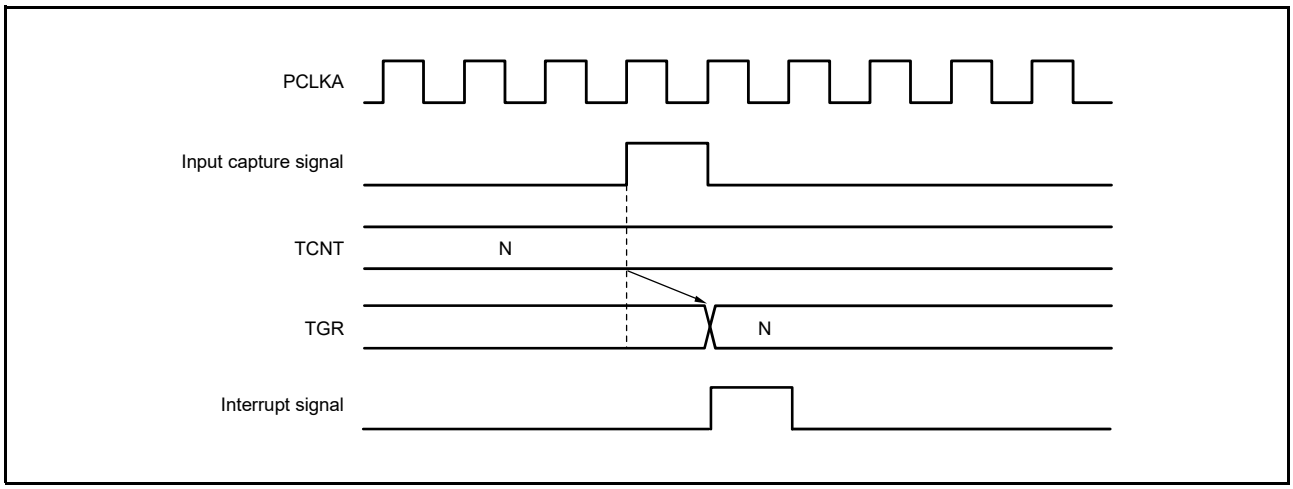


Figure 20.130 TGI Interrupt Timing (Input Capture) (MTU5)

(3) TCIV and TCIU Interrupt Timing

Figure 20.131 shows the TCIV interrupt request signal timing when an overflow is generated.
Figure 20.132 shows the TCIU interrupt request signal timing when an underflow is generated.

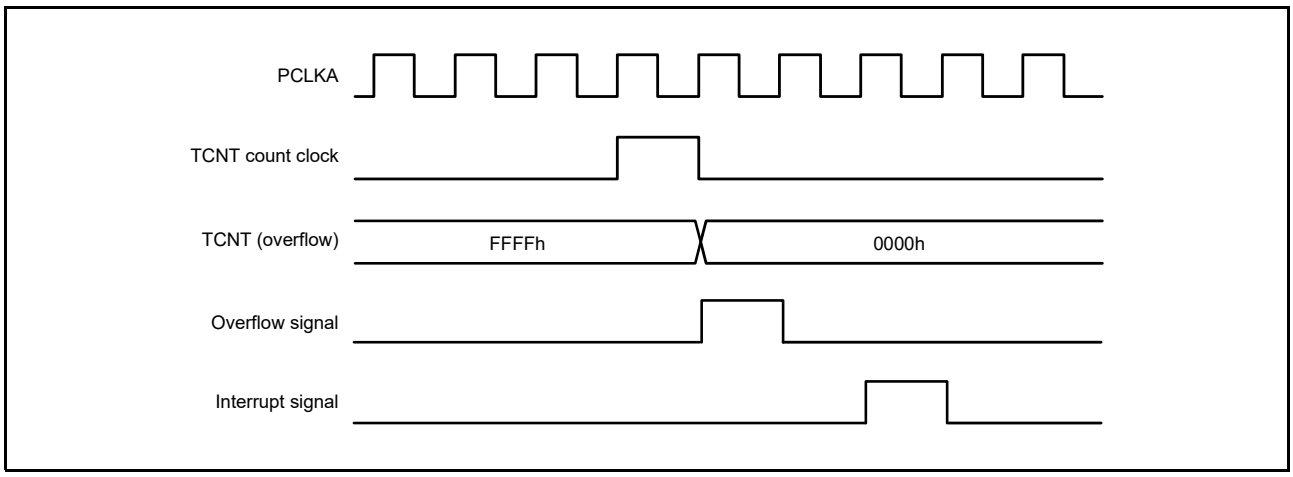


Figure 20.131 TCIV Interrupt Timing

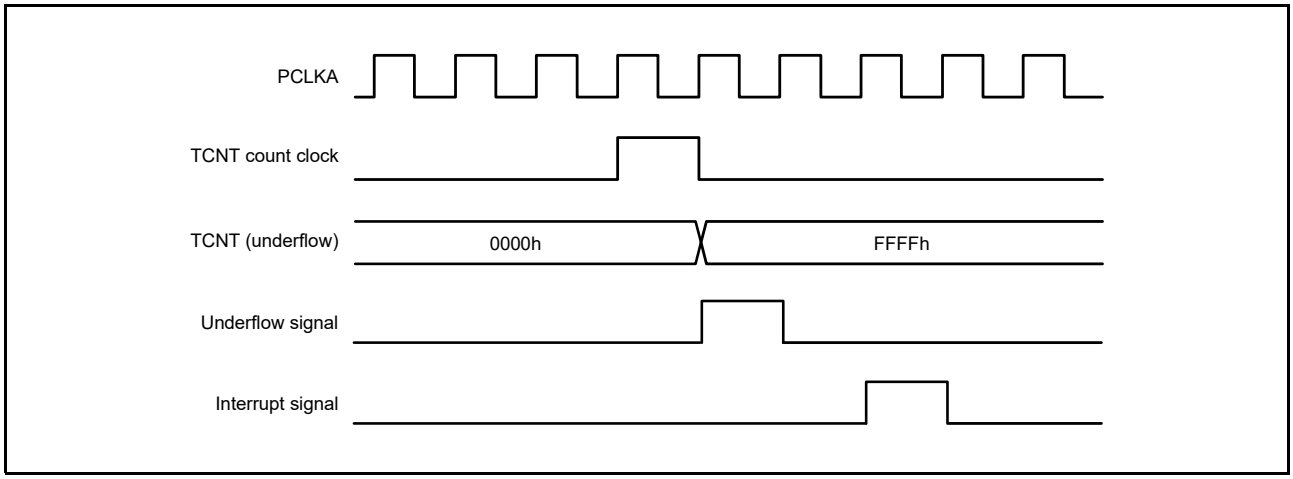


Figure 20.132 TCIU Interrupt Timing

20.6 Usage Notes

20.6.1 Module Stop Function Setting

MTU operation can be disabled or enabled using the module stop control register. MTU operation is stopped with the initial setting. Register access is enabled by releasing the module clock stop state. For details, refer to section 11, Low Power Consumption.

20.6.2 Count Clock Restrictions

The count clock source pulse width must be at least three PCLKA clocks for single-edge detection, and at least five PCLKA clocks for both-edge detection. The MTU will not operate properly at narrower pulse widths.
In phase counting mode, the phase difference and overlap between the two input clocks must be at least three PCLKA clocks, and the pulse width must be at least five PCLKA clocks. Figure 20.133 shows the input clock conditions in phase counting mode.

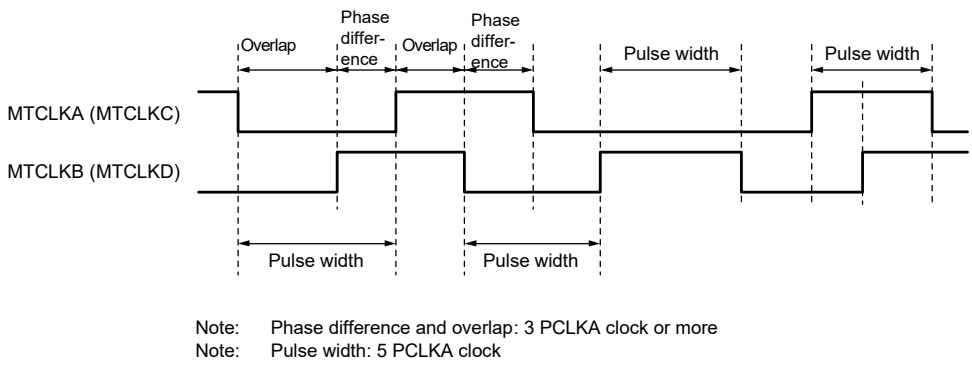


Figure 20.133 Phase Difference, Overlap, and Pulse Width in Phase Counting Mode

20.6.3 Note on Period Setting

When counter clearing on compare match is set, TCNT is cleared in the final state in which it matches the TGR value (the point at which TCNT updates the matched count value). Consequently, the actual counter frequency is given by the following formula:

- MTU0 to MTU4, MTU6, MTU7, and MTU9

$$f = \frac{CNTCLK}{N + 1}$$

- MTU5

$$f = \frac{CNTCLK}{N}$$

f: Counter frequency
CNTCLK: The count clock frequency set by TCR.TPSC[2:0] and TCR2.TPSC2[2:0]
N: TGR setting

20.6.4 Contention between TCNT Write and Clear Operations

If the counter clear signal is generated in the TCNT write cycle, TCNT clearing takes precedence and TCNT write operation is not performed.
Figure 20.134 shows the timing in this case.

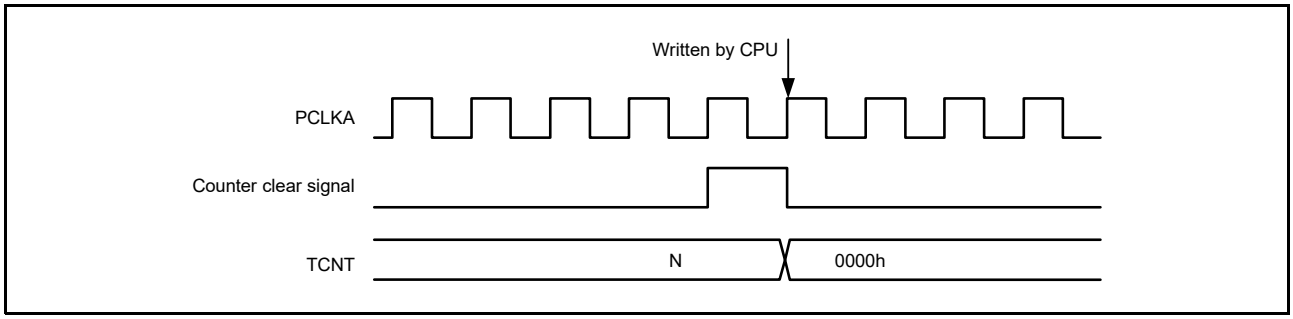


Figure 20.134 Contention between TCNT Write and Clear Operations

20.6.5 Contention between TCNT Write and Increment Operations

If incrementing occurs in a TCNT write cycle, TCNT write operation takes precedence and TCNT is not incremented.
Figure 20.135 shows the timing in this case.

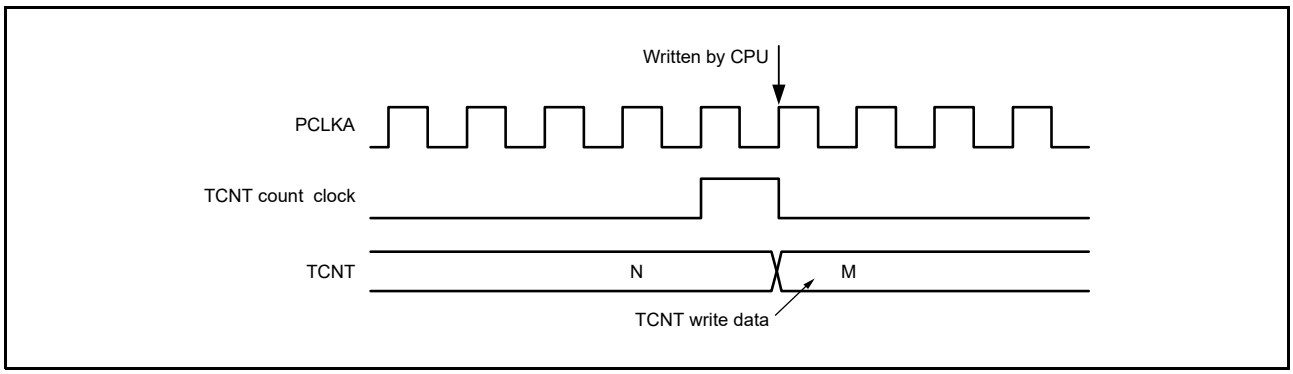


Figure 20.135 Contention between TCNT Write and Increment Operations

Input capture is performed regardless of occurrence of contention when the count clock of MTU1 or MTU2 is selected for the source of the input capture.

20.6.6 Contention between TGR Write Operation and Compare Match

If a compare match occurs in a TGR write cycle, TGR write operation is executed and the compare match signal is also generated.

Figure 20.136 shows the timing in this case.

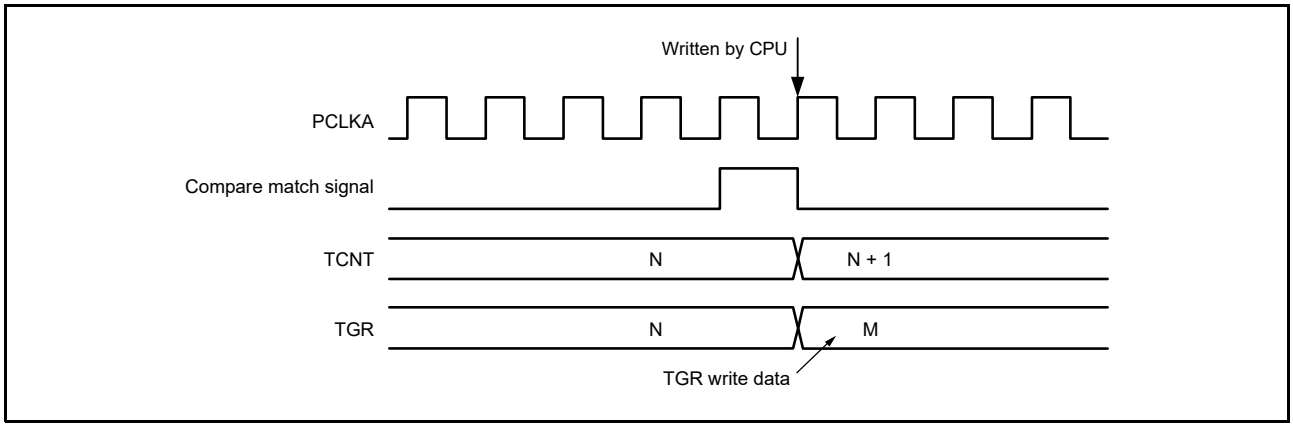


Figure 20.136 Contention between TGR Write Operation and Compare Match

20.6.7 Contention between Buffer Register Write Operation and Compare Match

If a compare match occurs in the T2 state in a TGR write cycle, the data before write operation is transferred to TGR by the buffer operation.

Figure 20.137 shows the timing in this case.

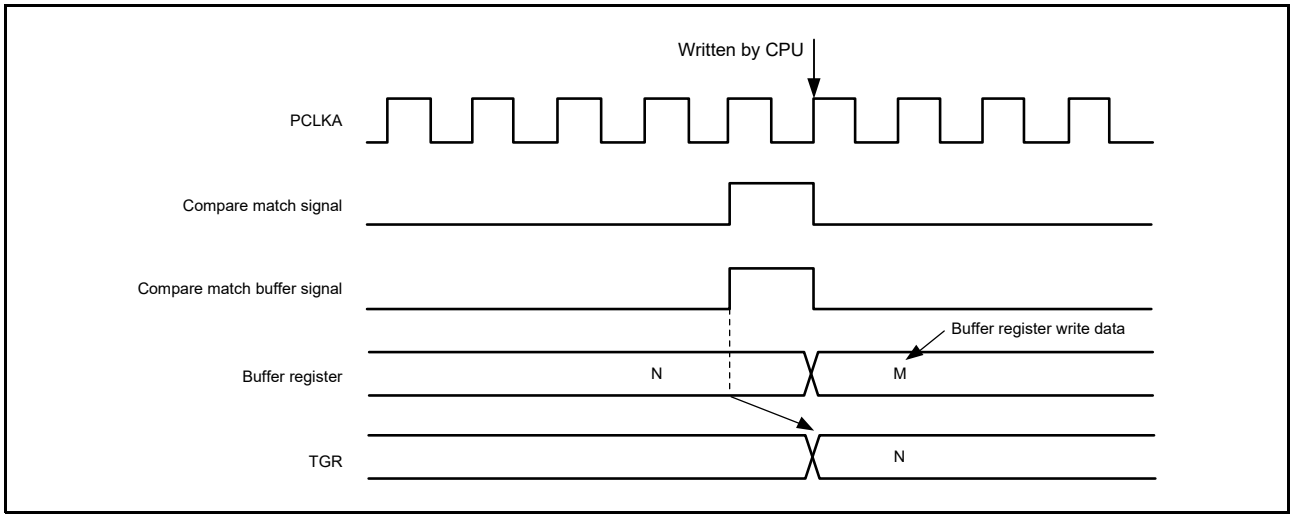


Figure 20.137 Contention between Buffer Register Write Operation and Compare Match

20.6.8 Contention between Buffer Register Write and TCNT Clear Operations

When the buffer transfer timing is set at the TCNT clear timing by the timer buffer transfer mode register (TBTM), if TCNT clearing occurs in the TGR write cycle, the data before write operation is transferred to TGR by the buffer operation.
Figure 20.138 shows the timing in this case.

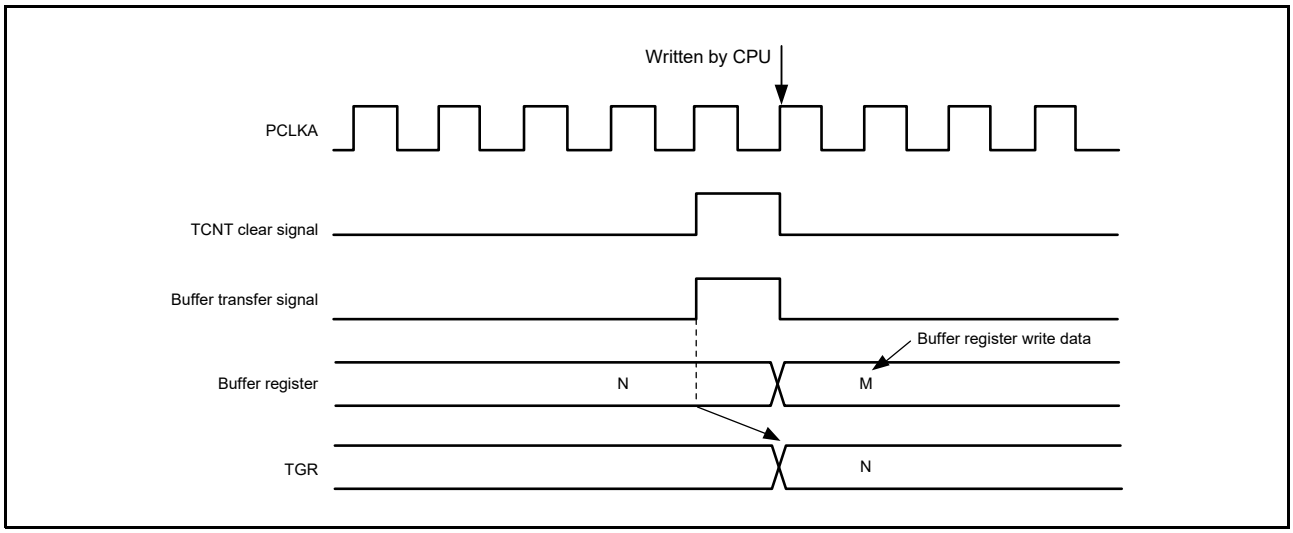


Figure 20.138 Contention between Buffer Register Write and TCNT Clear Operations

20.6.9 Contention between TGR Read Operation and Input Capture

If an input capture signal is generated in a TGR read cycle, the data before input capture transfer is read.
Figure 20.139 shows the timing in this case.

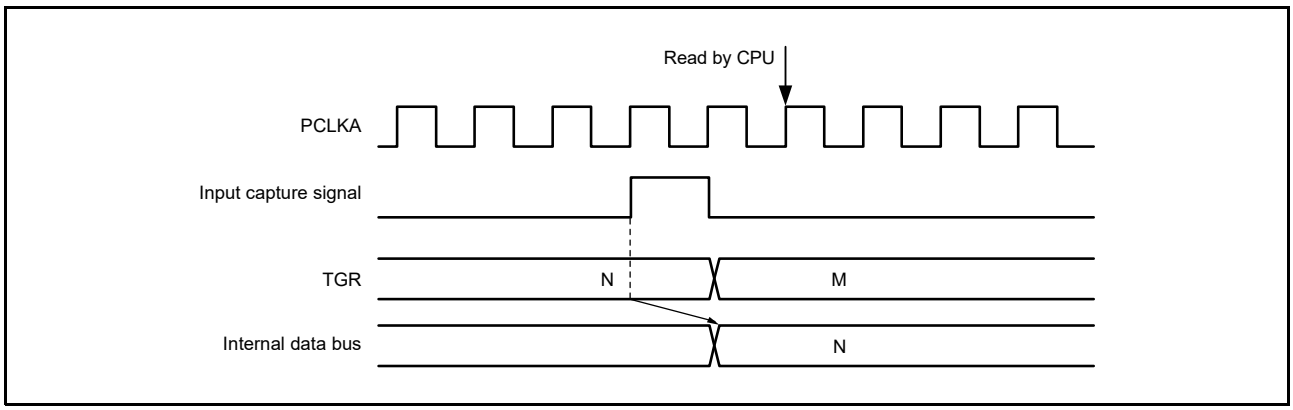


Figure 20.139 Contention between TGR Read Operation and Input Capture (MTU0 to MTU7, and MTU9)

20.6.10 Contention between TGR Write Operation and Input Capture

If an input capture signal is generated in the TGR write cycle, the input capture operation takes precedence and the TGR write operation is not performed in MTU0 to MTU4, MTU6, MTU7, and MTU9. In MTU5, the TGR write operation is performed and the input capture signal is generated.
Figure 20.140 and Figure 20.141 show the timing in this case.

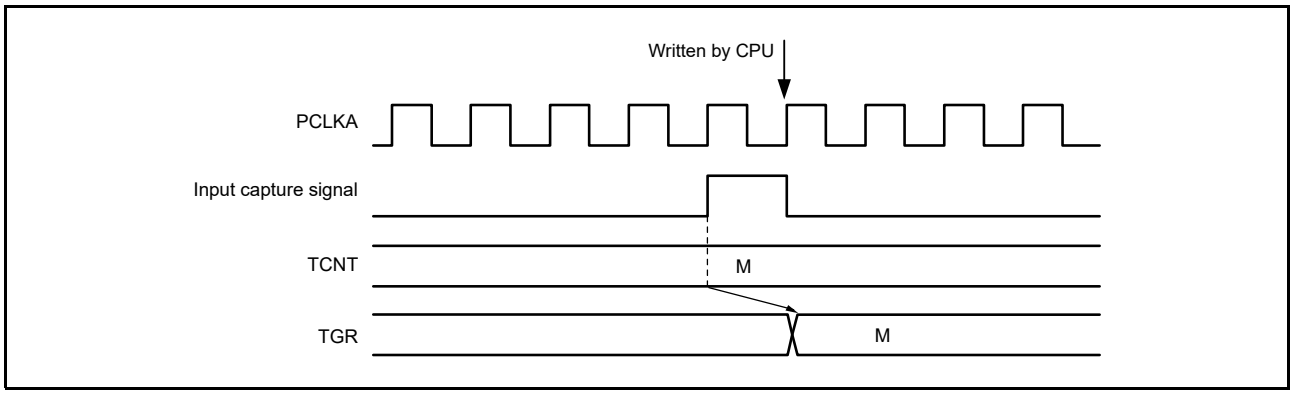


Figure 20.140 Contention between TGR Write Operation and Input Capture (MTU0 to MTU4, MTU6, MTU7, and MTU9)

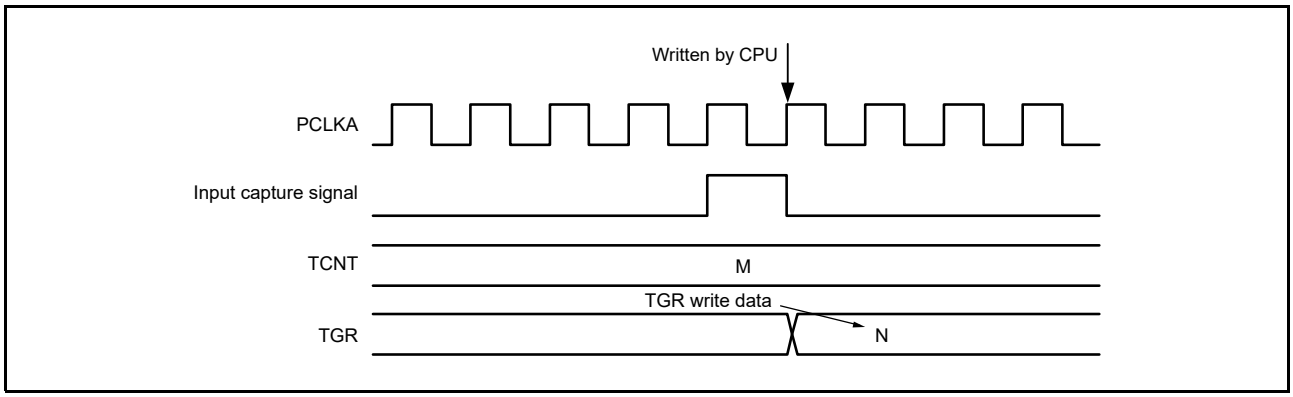


Figure 20.141 Contention between TGR Write Operation and Input Capture (MTU5)

20.6.11 Contention between Buffer Register Write Operation and Input Capture

If an input capture signal is generated in the buffer register write cycle, the buffer operation takes precedence and the buffer register write operation is not performed.
Figure 20.142 shows the timing in this case.

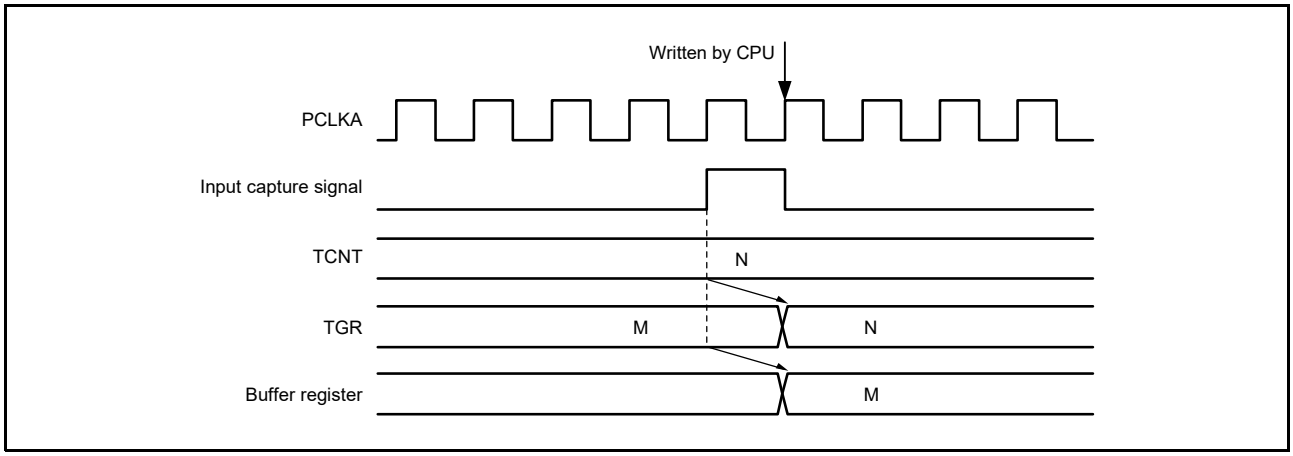


Figure 20.142 Contention between Buffer Register Write Operation and Input Capture

20.6.12 Contention between MTU2.TCNT Write Operation and Overflow/Underflow in Cascaded Operation

With timer counters MTU1.TCNT and MTU2.TCNT in a cascade, when a contention occurs between MTU1.TCNT counting (an MTU2.TCNT overflow/underflow) and the MTU2.TCNT write cycle, the MTU2.TCNT write operation is performed and the MTU1.TCNT count signal is disabled. In this case, if MTU1.TGRA works as a compare match register and there is a match between the MTU1.TGRA and MTU1.TCNT values, a compare match signal is issued. Furthermore, when the MTU1.TCNT (MTU2.TCNT) count clock is selected as the input capture source of MTU0 (MTU9), MTU0.TGRA to MTU0.TGRD (MTU9.TGRA to MTU9.TGRD) work in input capture mode. In addition, when the MTU0.TGRC compare match/input capture is selected as the input capture source of MTU1.TGRB, MTU1.TGRB works in input capture mode.

Figure 20.143 shows the timing in this case.

When setting the TCNT clearing function in cascaded operation, be sure to synchronize MTU1 and MTU2.

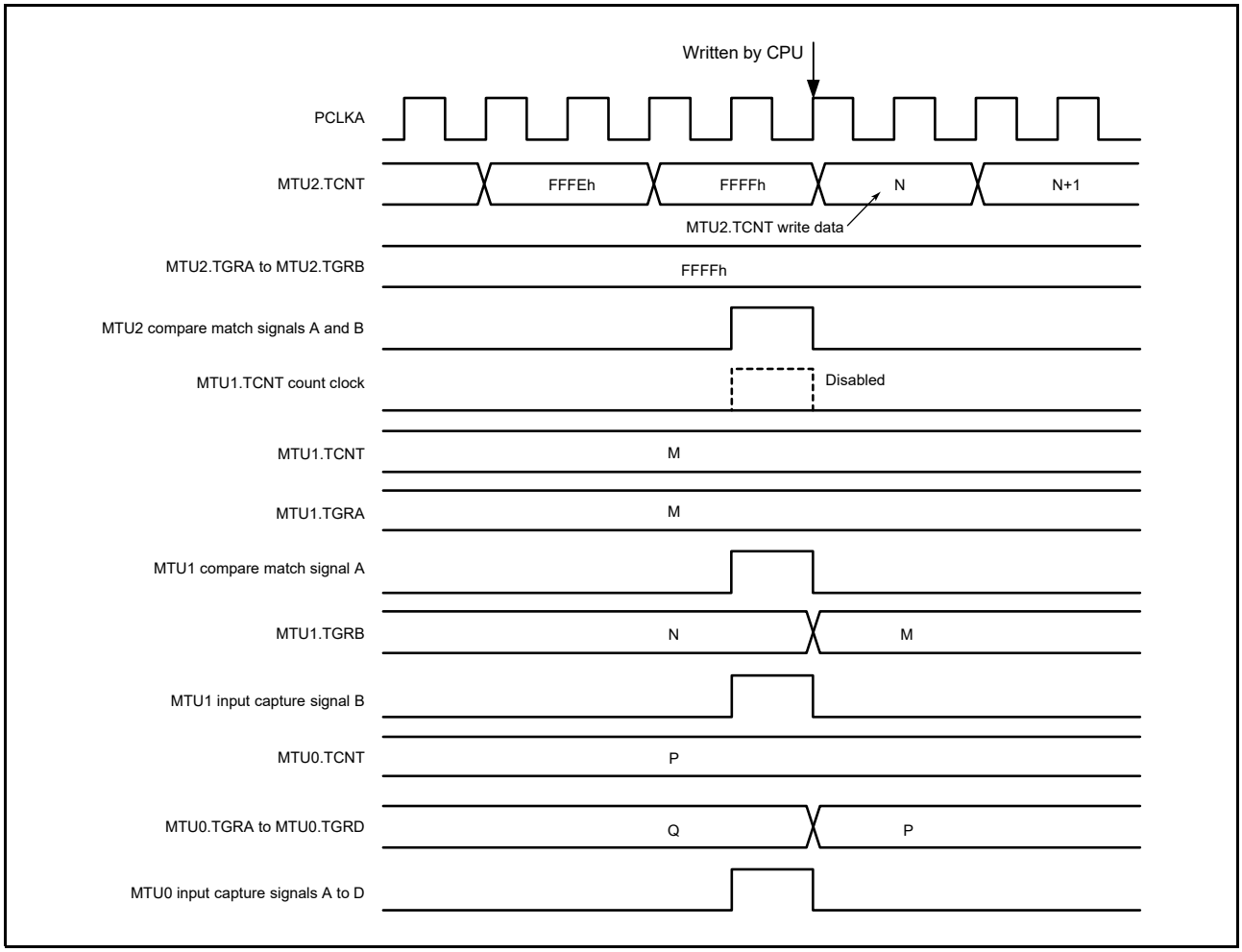


Figure 20.143 Contention between MTU2.TCNT Write Operation and Overflow/Underflow in Cascaded Operation

20.6.13 Counter Value When Count Operation is Stopped in Complementary PWM Mode

When counting operation in MTU3.TCNT and MTU4.TCNT (MTU6.TCNT and MTU7.TCNT) is stopped in complementary PWM mode, the MTU3.TCNT (MTU6.TCNT) value is set to the timer dead time register (TDDRA (TDDRB)) value and MTU4.TCNT (MTU7.TCNT) is set to 0000h.
When operation is restarted in complementary PWM mode, counting begins automatically from the initial setting state. Figure 20.144 shows this operation.
When counting begins in another operating mode, be sure to make initial settings in MTU3.TCNT and MTU4.TCNT (MTU6.TCNT and MTU7.TCNT).

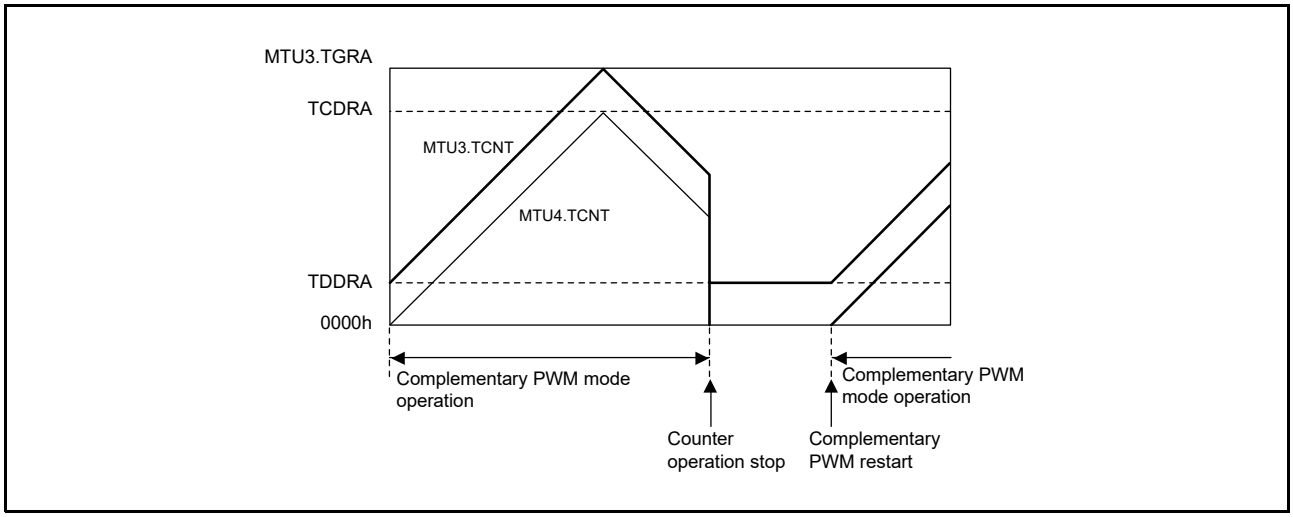


Figure 20.144 Counter Value When Stopped in Complementary PWM Mode

20.6.14 Buffer Operation Setting in Complementary PWM Mode

When modifying the PWM period set register (MTU3.TGRA or MTU6.TGRA), timer period data register (TCDRA or TCDRB), and duty set registers (MTU3.TGRB, MTU4.TGRA, and MTU4.TGRB (MTU6.TGRB, MTU7.TGRA, and MTU7.TGRB)) in complementary PWM mode, be sure to use buffer operation. In addition, set the BFA and BFB bits in MTU4.TMDR1 (MTU7.TMDR1) to 0. The MTIOC4C (MTIOC7C) pin cannot output waveforms if the BFA bit in MTU4.TMDR1 (MTU7.TMDR1) is set to 1. Likewise, the MTIOC4D (MTIOC7D) pin cannot output waveforms if the BFB bit in MTU4.TMDR1 (MTU7.TMDR1) is set to 1.
In complementary PWM mode, buffer operation in MTU3 and MTU4 (or MTU6 and MTU7) depends on the settings in bits BFA and BFB of MTU3.TMDR1 (MTU6.TMDR1). When the BFA bit in MTU3.TMDR1 (MTU6.TMDR1) is set to 1, MTU3.TGRC (MTU6.TGRC) functions as a buffer register for MTU3.TGRA (MTU6.TGRA). At the same time, MTU4.TGRC (MTU7.TGRC) functions as a buffer register for MTU4.TGRA (MTU7.TGRA), and TCBRA (TCBRB) functions as a buffer register for TCDRA (TCDRB).

20.6.15 Buffer Operation and Compare Match in Reset-Synchronized PWM Mode

When setting buffer operation in reset-synchronized PWM mode, set the BFA and BFB bits in MTU4.TMDR1 (MTU7.TMDR1) to 0. The MTIOC4C (MTIOC7C) pin cannot output waveforms if the BFA bit in MTU4.TMDR1 (MTU7.TMDR1) is set to 1. Likewise, the MTIOC4D (MTIOC7D) pin cannot output waveforms if the BFB bit in MTU4.TMDR1 (MTU7.TMDR1) is set to 1.

In reset-synchronized PWM mode, buffer operation in MTU3 and MTU4 (or MTU 6 and MTU7) depends on the settings in the BFA and BFB bits of MTU3.TMDR1 (MTU6.TMDR1). For example, if the BFA bit in MTU3.TMDR1 (MTU6.TMDR1) is set to 1, MTU3.TGRC (MTU6.TGRC) functions as a buffer register for MTU3.TGRA (MTU6.TGRA). At the same time, MTU4.TGRC (MTU7.TGRC) functions as a buffer register for MTU4.TGRA (MTU7.TGRA).

While the MTU3.TGRC (MTU6.TGRC) and MTU3.TGRD (MTU6.TGRD) are operating as buffer registers, a TGImn interrupt (m = C, D; n = 3, 4 or 6, 7) is not generated.

Figure 20.145 shows an example of MTU3.TGR (MTU6.TGR), MTU4.TGR (MTU7.TGR), MTIOC3 (MTIOC6), and MTIOC4 (MTIOC7) operation with the BFA and BFB bits in MTU3.TMDR1 (MTU6.TMDR1) set to 1 and the BFA and BFB bits in MTU4.TMDR1 (MTU7.TMDR1) set to 0.

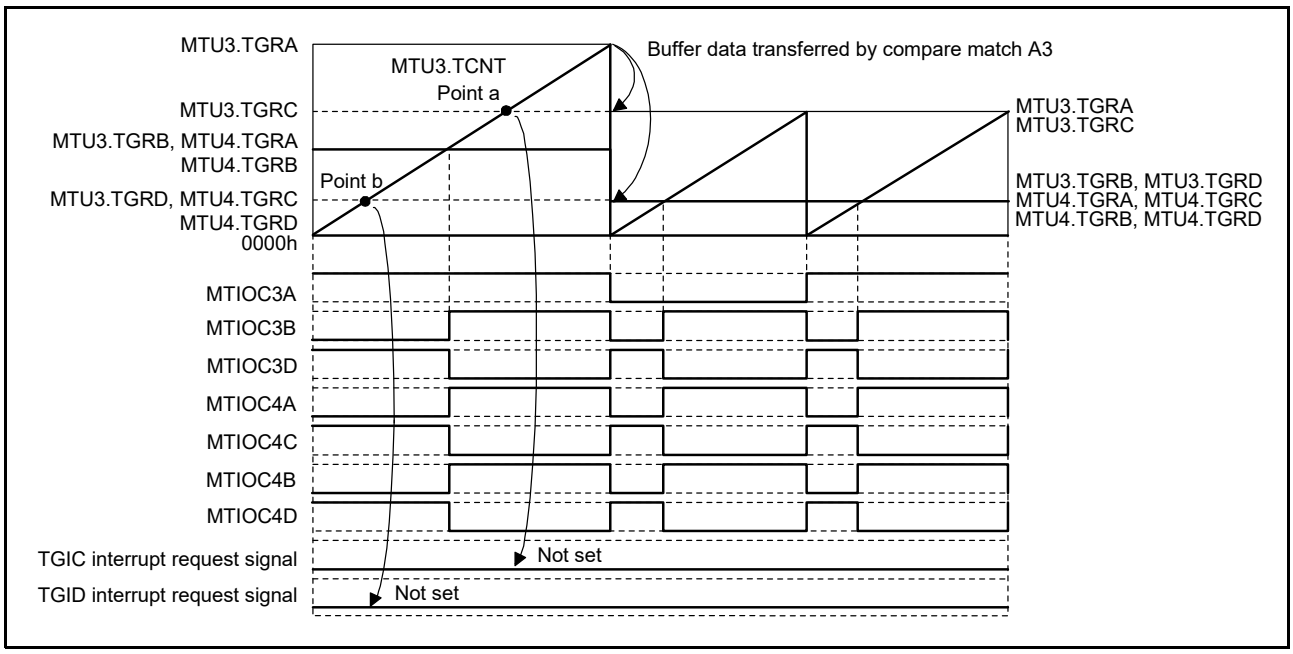


Figure 20.145 Buffer Operation and Compare Match in Reset-Synchronized PWM Mode

20.6.16 Overflow in Reset-Synchronized PWM Mode

After reset-synchronized PWM mode is selected, MTU3.TCNT and MTU4.TCNT (MTU6.TCNT and MTU7.TCNT) start counting when the CST3 (CST6) bit of TSTRA (TSTRB) is set to 1. In this state, the MTU4.TCNT (MTU7.TCNT) count clock source and count edge are determined by the MTU3.TCR (MTU6.TCR) setting.

In reset-synchronized PWM mode, with period register MTU3.TGRA (MTU6.TGRA) set to FFFFh and the MTU3.TGRA (MTU6.TGRA) compare match selected as the counter clearing source, MTU3.TCNT and MTU4.TCNT (MTU6.TCNT and MTU7.TCNT) count up to FFFFh, then a compare match occurs with MTU3.TGRA (MTU6.TGRA), and MTU3.TCNT and MTU4.TCNT (MTU6.TCNT and MTU7.TCNT) are both cleared. In this case, a TCIVn interrupt (n = 3, 4 or 6, 7) is not generated.

Figure 20.146 shows an example of operation in reset-synchronized PWM mode with period register MTU3.TGRA (MTU6.TGRA) set to FFFFh and the MTU3.TGRA (MTU6.TGRA) compare match specified for the counter clearing source.

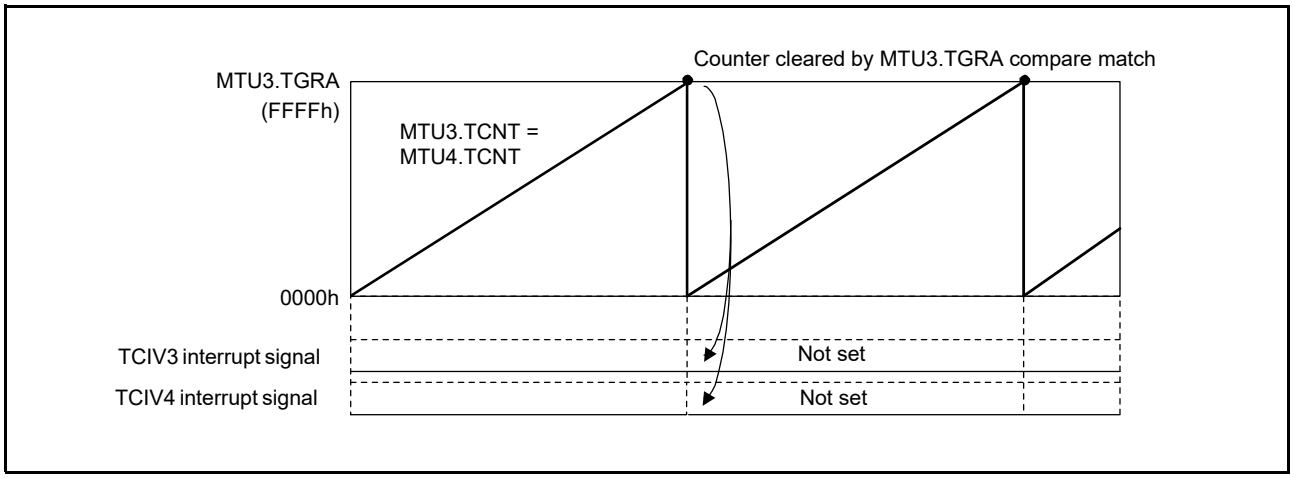


Figure 20.146 Overflow in Reset-Synchronized PWM Mode

20.6.17 Contention between Overflow/Underflow and Counter Clearing

If an overflow/underflow and counter clearing occur simultaneously, a TCIVn interrupt (n = 0 to 4, 6, 7, 9) nor a TCIUn interrupt (n = 1, 2) is not generated and TCNT clearing takes precedence.
Figure 20.147 shows the operation timing when a TGR compare match is specified as the clearing source and TGR is set to FFFFh.

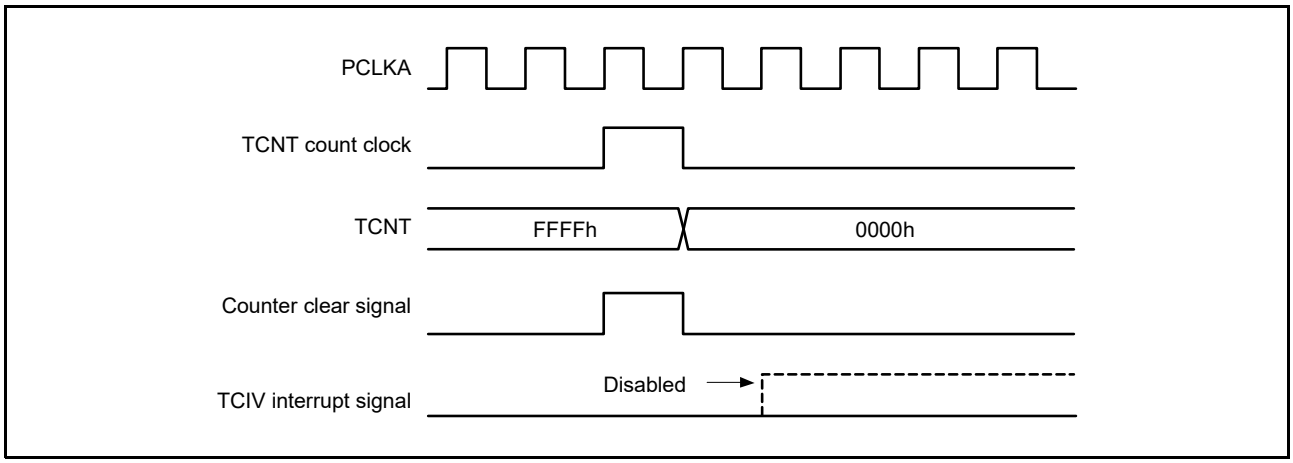


Figure 20.147 Contention between Overflow and Counter Clearing

20.6.18 Contention between TCNT Write Operation and Overflow/Underflow

If TCNT counts up or down in a TCNT write cycle and an overflow or an underflow occurs, the TCNT write operation takes precedence. A TCIVn interrupt (n = 0 to 4, 6, 7, 9) nor a TCIUn interrupt (n = 1, 2) is not generated.
Figure 20.148 shows the operation timing when there is contention between TCNT write operation and overflow.

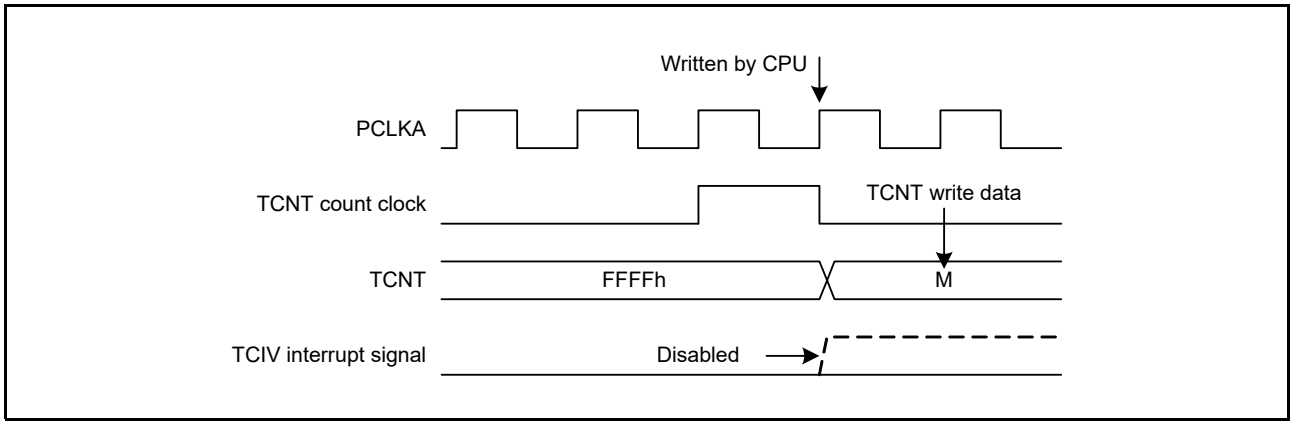


Figure 20.148 Contention between TCNT Write Operation and Overflow

20.6.19 Note on Transition from Normal Mode or PWM Mode 1 to Reset-Synchronized PWM Mode

When making a transition from normal mode or PWM mode 1 to reset-synchronized PWM mode in MTU3 and MTU4 (or MTU6 and MTU7), if the counter is stopped while the output pins (MTIOC3B, MTIOC3D, MTIOC4A, MTIOC4C, MTIOC4B, MTIOC4D, MTIOC6B, MTIOC6D, MTIOC7A, MTIOC7C, MTIOC7B, and MTIOC7D) are held at a high level and then operation is started after a transition to reset-synchronized PWM mode, the initial pin output will not be correct.

When making a transition from normal mode to reset-synchronized PWM mode, write 11h to MTU3.TIORH, MTU3.TIORL, MTU4.TIORH, and MTU4.TIORL (MTU6.TIORH, MTU6.TIORL, MTU7.TIORH, and MTU7.TIORL) to initialize the output pin state to a low level, then set the registers to the initial value (00h) before making the mode transition.

When making a transition from PWM mode 1 to reset-synchronized PWM mode, switch to normal mode, initialize the output pin state to a low level, and then set the registers to the initial value (00h) before making the transition to reset-synchronized PWM mode.

20.6.20 Output Level in Complementary PWM Mode and Reset-Synchronized PWM Mode

When MTU3 and MTU4 (or MTU6 and MTU7) are in complementary PWM mode or reset-synchronized PWM mode, the PWM waveform output level is determined by the OLSP and OLSN bits in the timer output control register (TOCR1A or TOCR1B). In complementary PWM mode or reset-synchronized PWM mode, TIOR should be set to 00h. The output level in negative phase when the TDER.TDER bit is set to 0 in complementary PWM mode (the dead time is not generated) does not depend on the setting of the TOCR1.OLSN bit. It is equivalent to the inverted level of positive phase output based on the setting of the TOCR1.OLSP bit.

20.6.21 Simultaneous Input Capture in MTU1.TCNT and MTU2.TCNT in Cascade Connection

When timer counters 1 and 2 (MTU1.TCNT and MTU2.TCNT) operate as a 32-bit counter in cascade connection, the cascaded counter value cannot be captured successfully in some cases even if input-capture input is simultaneously done to MTIOC1A and MTIOC2A or to MTIOC1B and MTIOC2B. This is because the input timing of MTIOC1A and MTIOC2A or to MTIOC1B and MTIOC2B may not be the same when external input-capture signals input into MTU1.TCNT and MTU2.TCNT are taken in synchronization with the internal clock.

For example, MTU1.TCNT (the counter for upper 16 bits) does not capture the count-up value by an overflow from MTU2.TCNT (the counter for lower 16 bits) but captures the count value before the up-counting. In this case, the values of MTU1.TCNT = FFF1h and MTU2.TCNT = 0000h should be transferred to MTU1.TGRA and MTU2.TGRA or to MTU1.TGRB and MTU2.TGRB, but the values of MTU1.TCNT = FFF0h and MTU2.TCNT = 0000h are erroneously transferred.

The MTU has a function that allows simultaneous capture of MTU1.TCNT and MTU2.TCNT with a single input capture input. This function can be used to read the 32-bit counter such that MTU1.TCNT and MTU2.TCNT are captured at the same time. For details, refer to section 20.2.11, Timer Input Capture Control Register (TICCR).

20.6.22 Interrupt Skipping Function 2

When interrupt skipping function 2 is in use and the difference between the values in MTU4.TADCORA and MTU4.TADCORB is small, correct counting of the number skipped may not be possible, in which case requests for A/D conversion will not be generated with the expected timing. The conditions listed below thus apply to these settings.
For MTU6 and MTU7, the same conditions apply to the settings of MTU7.TADCORA and MTU7.TADCORB.

(1) When the number skipped is zero for skipping function 2

- The difference between the values in MTU4.TADCORA and MTU4.TADCORB must be at least four.
- The interval of comparison for MTU4.TADCORA must be at least four cycles of PCLKA clock (the updated value of MTU4.TADCORA is set to the previous value plus or minus at least four).
- The interval of comparison for MTU4.TADCORB must be at least four cycles of PCLKA clock (the updated value of MTU4.TADCORB is set to the previous value plus or minus at least four).

(2) When the number skipped is one or more for skipping function 2

- The difference between the values in MTU4.TADCORA and MTU4.TADCORB must be at least two.
- The interval of comparison for MTU4.TADCORB must be at least two cycles of PCLKA (the updated value of MTU4.TADCORB is set to the previous value plus or minus at least two).

20.6.23 Notes When Complementary PWM Mode Output Protection Function is Not Used

The complementary PWM mode output protection function is initially enabled. For details, refer to section 21, Port Output Enable 3 (POE3A).

20.6.24 Notes Regarding Timer Counter (MTU5.TCNT) and Timer General Register (MTU5.TGR)

Do not set an MTU5.TGRj (j = U, V, W) bit to the value of the corresponding MTU5.TCNTj (j = U, V, W) plus one while counting by the MTU5.TCNTj (j = U, V, W) register is stopped. If an MTU5.TGRj (j = U, V, W) bit is set to the value of the corresponding MTU5.TCNTj (j = U, V, W) plus one while counting by the MTU5.TCNTj (j = U, V, W) is stopped, a compare-match will be generated even though counting is stopped.
In this case, if the compare match enable bit (MTU5.TIER.TGIE5j (j = U, V, W) bit is set to 1 (enabling interrupts), a compare-match interrupt will also be generated. If the value of the timer compare match clear register is 1 (enabled), the timer is automatically cleared to 0000h when the compare-match is generated, regardless of whether interrupts from the MTU5.TCNTj (j = U, V, W) are enabled or disabled.

20.6.25 Notes to Prevent Malfunctions in Synchronous Clearing for Complementary PWM Mode

If control of the output waveform is enabled (TWCRA.WRE bit = 1 or TWCRB.WRE bit = 1) at the time of synchronous counter clearing in complementary PWM mode, satisfaction of either condition 1 or 2 below has the following effects.

- Dead time on the PWM output pins is shortened (or disappears).
- The active level is output on the negative phase PWM output pins beyond the period for active-level output.

Condition 1: In portion (10) of the initial output inhibition period in Figure 20.149, synchronous clearing occurs within the dead-time period for PWM output.

Condition 2: In portions (10) and (11) of the initial output inhibition period in Figure 20.150, synchronous clearing occurs when any condition from among MTU3.TGRB (MTU6.TGRB) ≤ TDDR (TDDRB), MTU4.TGRA (MTU7.TGRA) ≤ TDDR (TDDRB), or MTU4.TGRB (MTU7.TGRB) ≤ TDDR (TDDRB) is satisfied.

The following method avoids the above phenomena.
Ensure that synchronous clearing proceeds with the value of each comparison register (MTU3.TGRB (MTU6.TGRB), MTU4.TGRA (MTU7.TGRA), and MTU4.TGRB (MTU7.TGRB) ≤ TDDR (TDDRB)) set to at least double the value of the TDDRA register (TDDRB register).

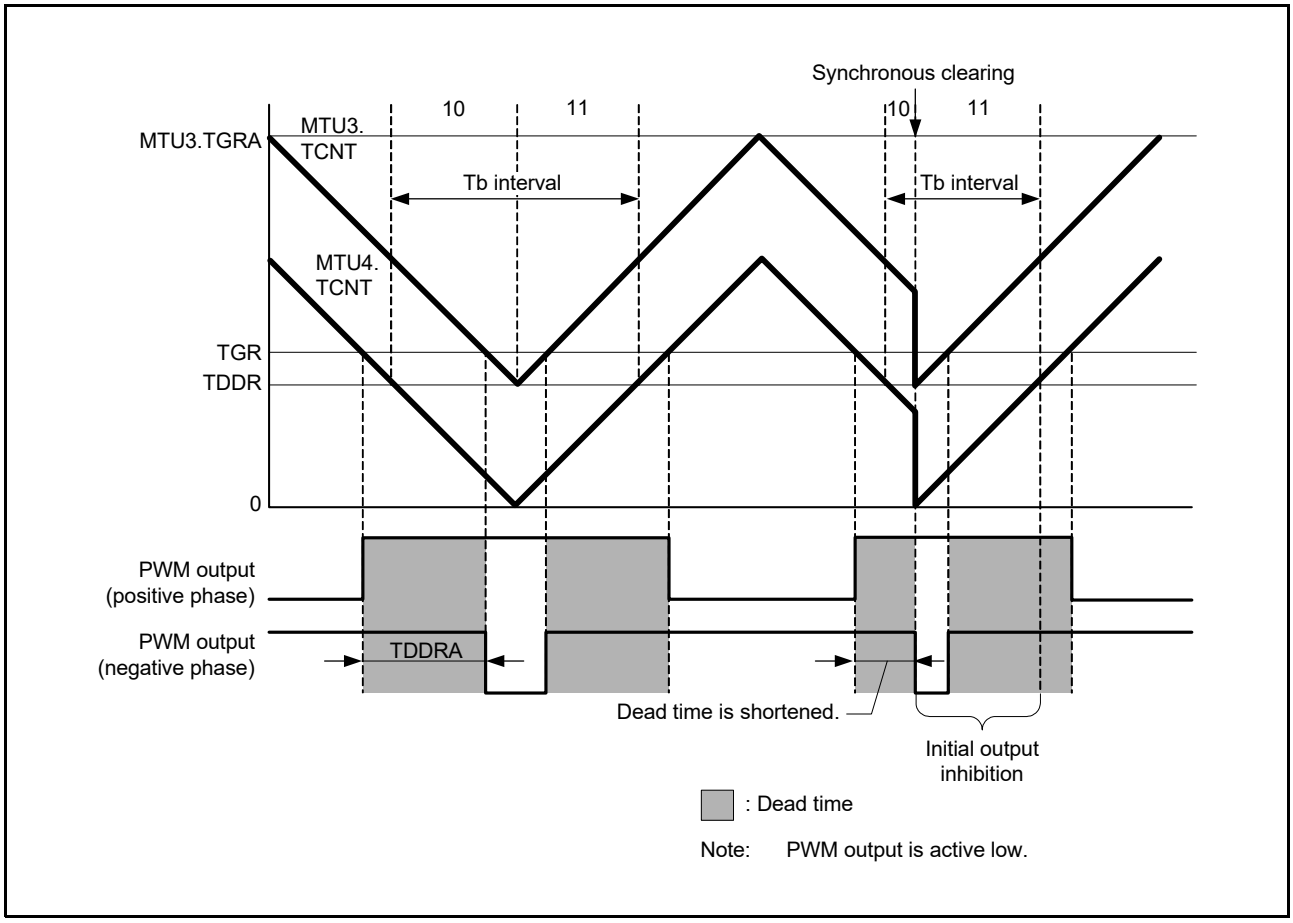


Figure 20.149 Example of Synchronous Clearing (When Condition 1 Applies)

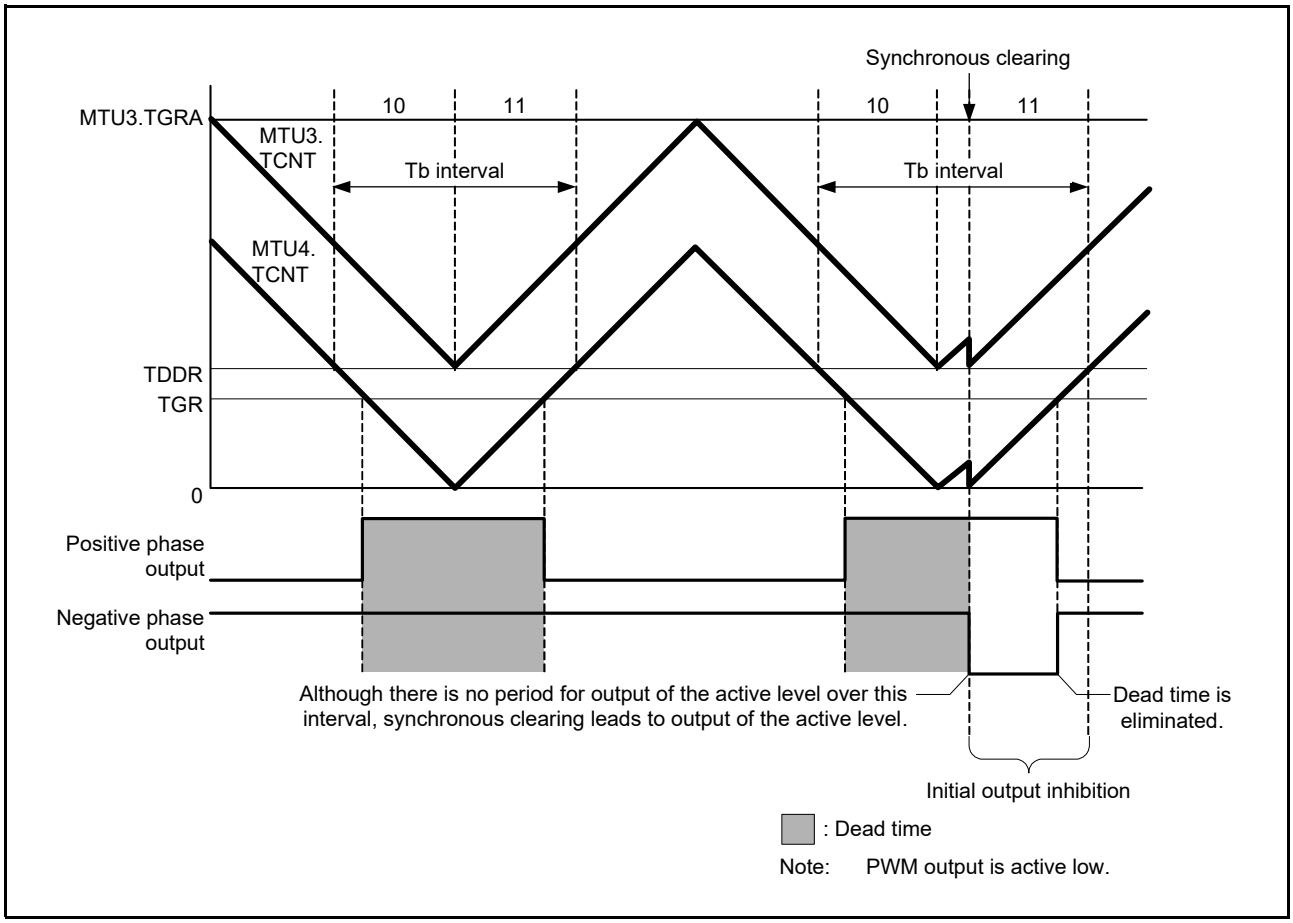


Figure 20.150 Example of Synchronous Clearing (When Condition 2 Applies)

20.6.26 Continuous Output of Interrupt Signal in Response to a Compare Match

When the TGR register is set to 0000h, the PCLKA/1 clock is set as the count clock, and compare match is set as the trigger for clearing of the count clock, the value of the TCNT counter remains 0000h, and the interrupt signal will be output continuously (i.e. its level will be flat) rather than output over a single cycle. Consequently, interrupts will not be detected in response to second and subsequent compare matches.

Figure 20.151 shows the timing for continuous output of the interrupt signal in response to a compare match.

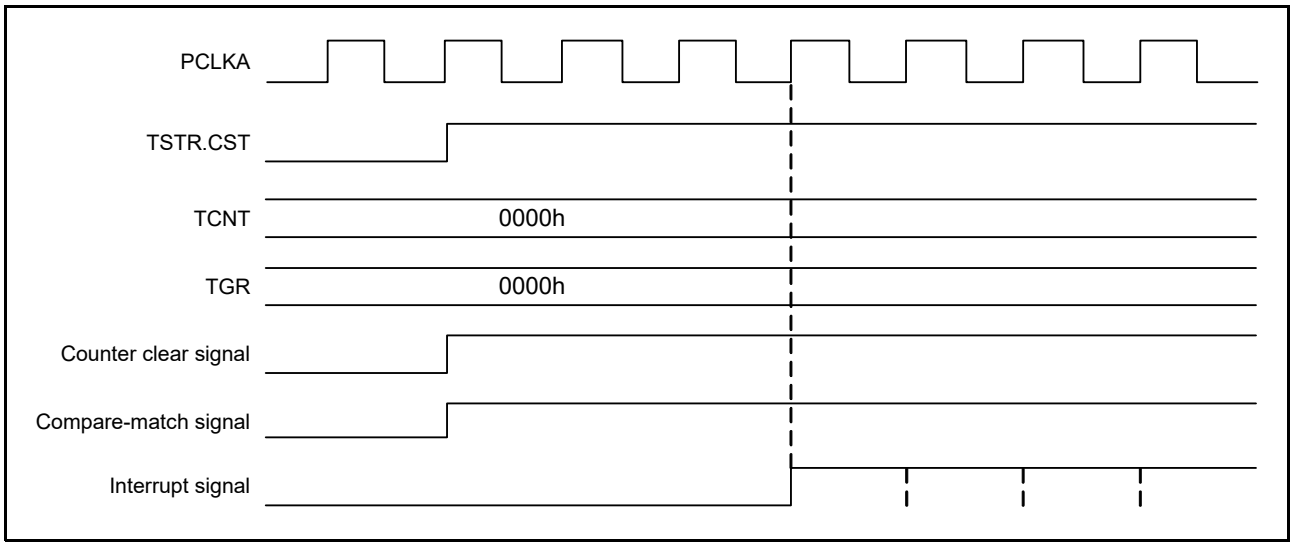


Figure 20.151 Continuous Output of Interrupt Signal in Response to a Compare Match

20.6.27 Usage Notes on A/D Converter Delaying Function in Complementary PWM Mode

- When data is transferred from a buffer register at the trough of the MTU4.TCNT (MTU7.TCNT) counter while the MTU4.TADCOBRA and MTU4.TADCOBRB (MTU7.TADCOBRA and MTU7.TADCOBRB) registers are set to 0 and the UT4AE and UT4BE (UT7AE and UT7BE) bits in the MTU4.TADCR (MTU7.TADCR) register are set to 1, no A/D converter start request is issued during up-counting immediately after transfer. Refer to Figure 20.152.
- When data is transferred from a buffer register at the crest of the MTU4.TCNT (MTU7.TCNT) counter while the MTU4.TADCOBRA and MTU4.TADCOBRB (MTU7.TADCOBRA and MTU7.TADCOBRB) registers are set to the same value as the TCDR and the UT4AE and UT4BE (UT7AE and UT7BE) bits in the MTU4.TADCR (MTU7.TADCR) register are set to 1, no A/D converter start request is issued during down-counting immediately after transfer. Refer to Figure 20.153.
- To issue an A/D converter start request linked with the interrupt skipping function, set the MTU4.TADCORA and MTU4.TADCORB (MTU7.TADCORA and MTU7.TADCORB) registers so that 2 ≤ MTUn.TADCORA/TADCORB ≤ TCDR – 2 is satisfied (n = 4, 7).

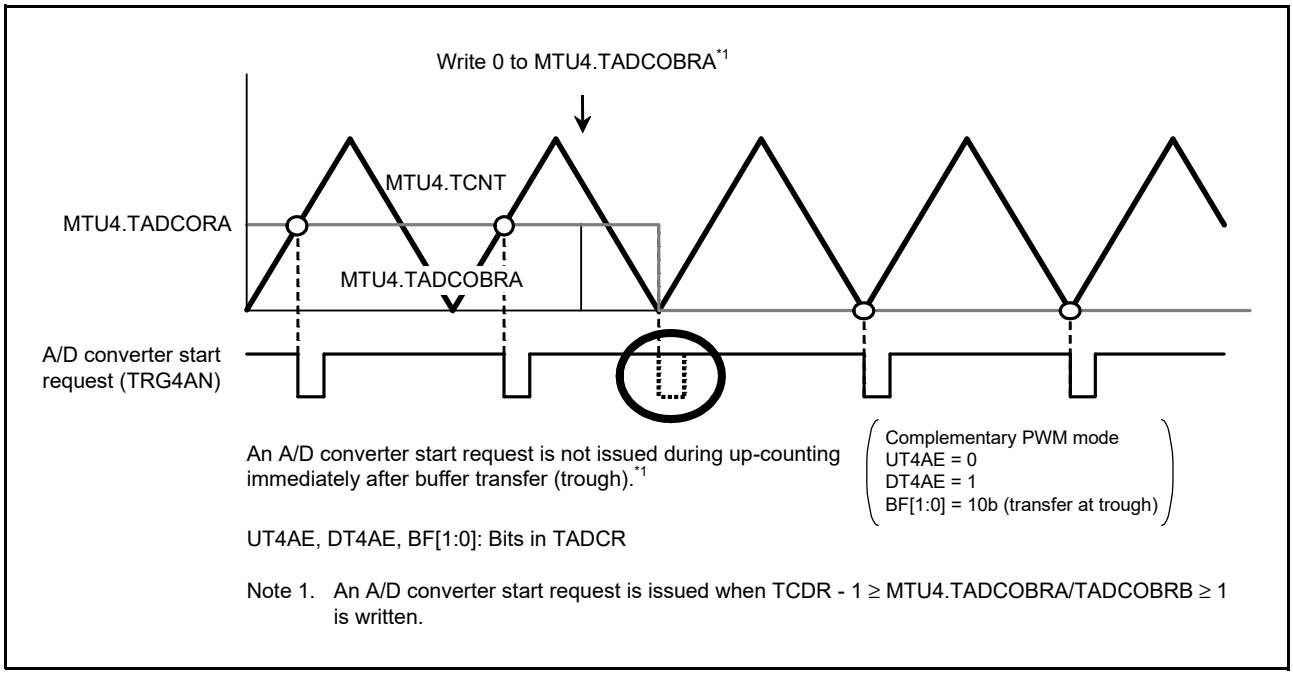


Figure 20.152 A/D Converter Start Request When 0 is Written to MTU4.TADCOBRA

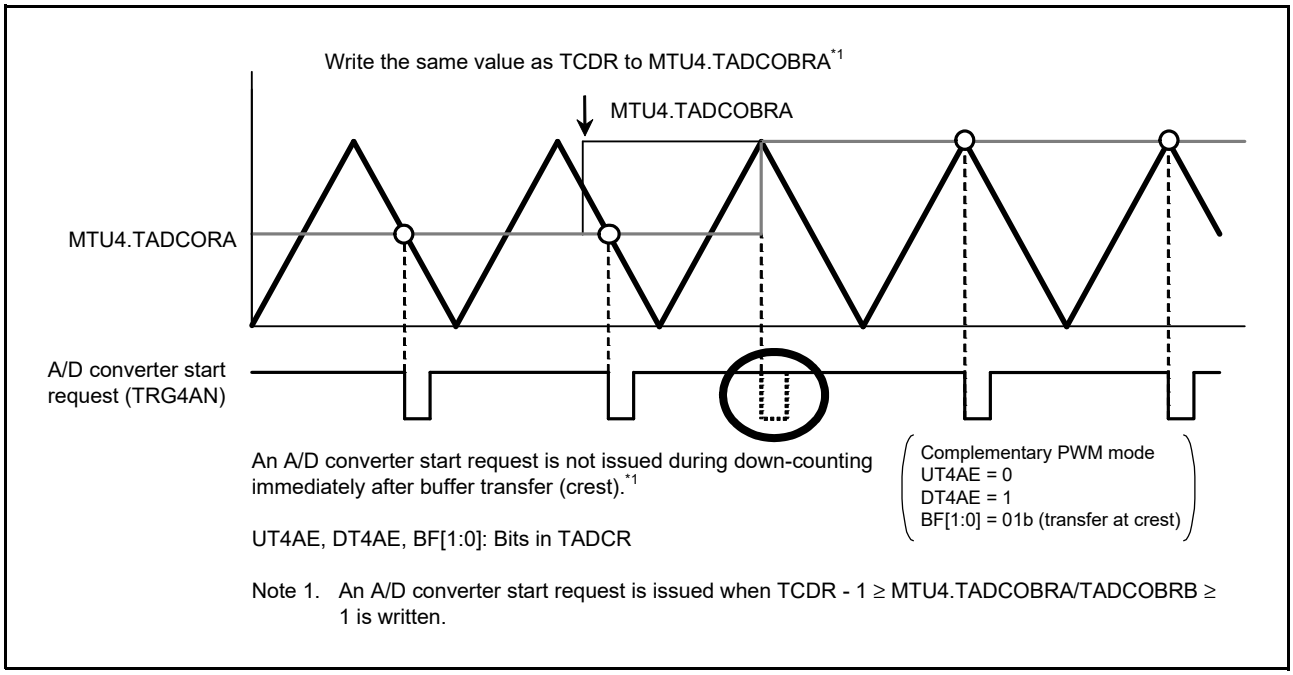


Figure 20.153 A/D Converter Start Request When the Same Value as TCDR is Written to MTU4.TADCOBRA

20.7 MTU Output Pin Initialization

20.7.1 Operating Modes

The MTU has the following six operating modes. Waveforms can be output in any of these modes.

- Normal mode (MTU0 to MTU4, MTU6, MTU7, and MTU9)
- PWM mode 1 (MTU0 to MTU4, MTU6, MTU7, and MTU9)
- PWM mode 2 (MTU0 to MTU2, and MTU9)
- Phase counting modes 1 to 5 (MTU1 and MTU2)
- Complementary PWM mode (MTU3, MTU4, MTU6, and MTU7)
- Reset-synchronized PWM mode (MTU3, MTU4, MTU6, and MTU7)

This section describes how to initialize the MTU output pins in each of these modes.

20.7.2 Operation in Case of Re-Setting Due to Error during Operation

If an error occurs during MTU operation, MTU output should be cut off by the system. The output can be cut off by allowing non-active level output from the pins by setting the pins as general output ports using the port direction registers (PDR), port output data registers (PODR), and port mode registers (PMR) of the I/O ports. MTU output can be disabled through TIOR settings. Complementary PWM output (MTIOC3B, MTIOC3D, MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D, MTIOC6B, MTIOC6D, MTIOC7A, MTIOC7B, MTIOC7C, and MTIOC7D) should be specified through TOERA and TOERB settings. For PWM output pins, output can also be cut by hardware, using port output enable 3 (POE3). The pin initialization procedures for re-setting due to an error during operation and the procedures for restarting in a different mode after re-setting are described below.

The MTU has six operating modes, as stated above. There are thus 36 mode transition combinations, but some transitions are not available with certain channel and mode combinations. Available mode transition combinations are shown in Table 20.81.

Table 20.81 Mode Transition Combinations

	Normal	PWM1	PWM2	PCM	CPWM	RPWM
Normal	(1)	(2)	(3)	(4)	(5)	(6)
PWM1	(7)	(8)	(9)	(10)	(11)	(12)
PWM2	(13)	(14)	(15)	(16)	Not available	Not available
PCM	(17)	(18)	(19)	(20)	Not available	Not available
CPWM	(21)	(22)	Not available	Not available	(23) (24)	(25)
RPWM	(26)	(27)	Not available	Not available	(28)	(29)

Normal: Normal mode
PWM1: PWM mode 1
PWM2: PWM mode 2
PCM: Phase counting modes 1 to 5
CPWM: Complementary PWM mode
RPWM: Reset-synchronized PWM mode

20.7.3 Overview of Initialization Procedures and Mode Transitions in Case of Error during Operation

- When making a transition to a mode (Normal, PWM1, PWM2, or PCM) in which the pin output level is selected by the timer I/O control register (TIOR) setting, initialize the pins by means of TIOR setting.
- In PWM mode 1, waveforms are not output to the MTIOCnB and MTIOCnD (n = 3, 4, 6, 7) pins. When a pin is configured for MTIOCnB or MTIOCnD, it enters high-impedance state. To output a specified level, set the pin to general output port.
- In PWM mode 2, a waveform is not output to the pin that corresponds to the TGR register used as a period register. When a pin is configured for MTIOCnm (n = 0 to 2, 9; m = A to D), it enters high-impedance state. To output a specified level, set the pin to general output port.
- In normal mode or PWM mode 2, if TGRC and TGRD operate as buffer registers, waveforms are not output to the corresponding pins (MTIOCnC or MTIOCnD (n = 0, 3, 4, 6, 7, 9)). When a pin is configured for MTIOCnC or MTIOCnD, it enters high-impedance state. To output a specified level, set the pin to general output port.
- In PWM mode 1, if either TGRC or TGRD operates as a buffer register, waveforms are not output to the corresponding pins (MTIOCnC or MTIOCnD (n = 0, 3, 4, 6, 7, 9)). When a pin is configured for MTIOCnC or MTIOCnD, it enters high-impedance state. To output a specified level, set the pin to general output port.
- When making a transition to a mode (CPWM or RPWM) in which the pin output level is selected by the timer output control register (TOCR1A, TOCR2A, TOCR1B, or TOCR2B) setting, temporarily disable output in MTU3 and MTU4 (or MTU6 and MTU7) with the timer output master enable register (TOERA or TOERB). At this time, when a pin is configured for MTIOCnm (n = 3, 4, 6, 7; m = A to D), it enters high-impedance state. To output a specified level, set the pin to general output port. Switch to normal mode, perform initialization with TIOR, restore TIOR to its initial value, then operate the MTU in accordance with the mode setting procedure (TOCR1A setting, TOCR2A setting, TMDR1 setting, and TOERA setting (TOCR1B setting, TOCR2B setting, TMDR1 setting, and TOERB setting)).

Note: Channel number is substituted for “n” indicated in this section.

Pin initialization procedures are described below for the numbered combinations in Table 20.81. The active level is assumed to be low.

(1) Operation When Error Occurs in Normal Mode and Operation is Restarted in Normal Mode

Figure 20.154 shows a case in which an error occurs in normal mode and operation is restarted in normal mode after re-setting.

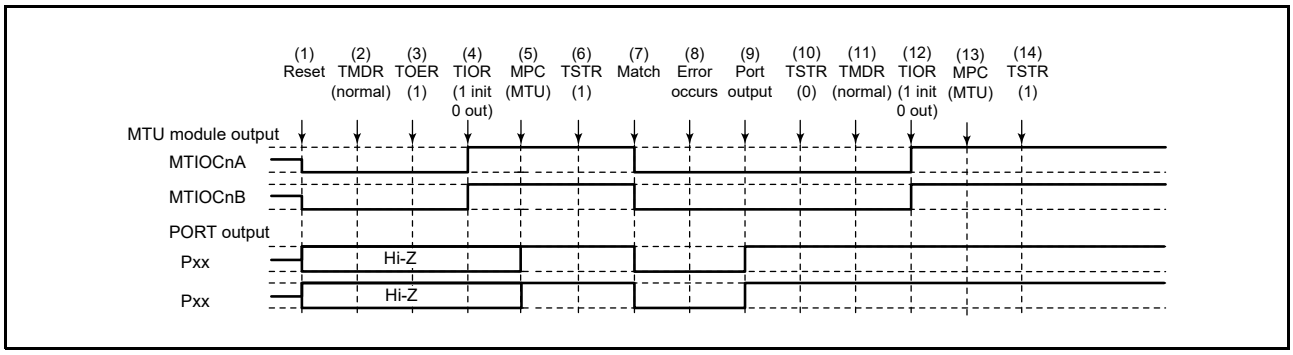


Figure 20.154 Error Occurrence in Normal Mode, Recovery in Normal Mode

(1) After a reset, the MTU output goes low and the ports enter high-impedance state.
(2) After a reset, the TMDR1 setting is for normal mode.
(3) For MTU3 and MTU4 (MTU6 and MTU7), enable output with the TOERA (TOERB) register before initializing the pins with the TIOR register.
(4) Initialize the pins with the TIOR register. (In the example, the initial output is a high level, and a low level is output on compare match occurrence.)
(5) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(6) Start count operation by setting the TSTRA (TSTRB) register.
(7) Output goes low on compare match occurrence.
(8) An error occurs.
(9) Allow non-active level output by setting the pins as general output ports using the port direction registers (PDR), port output data registers (PODR), and port mode registers (PMR) of the I/O ports.
(10) Stop count operation by setting the TSTRA (TSTRB) register.
(11) This step is not necessary when restarting in normal mode.
(12) Initialize the pins with the TIOR register.
(13) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(14) Restart operation by setting the TSTRA (TSTRB) register.

(2) Operation When Error Occurs in Normal Mode and Operation is Restarted in PWM Mode 1

Figure 20.155 shows a case in which an error occurs in normal mode and operation is restarted in PWM mode 1 after re-setting.

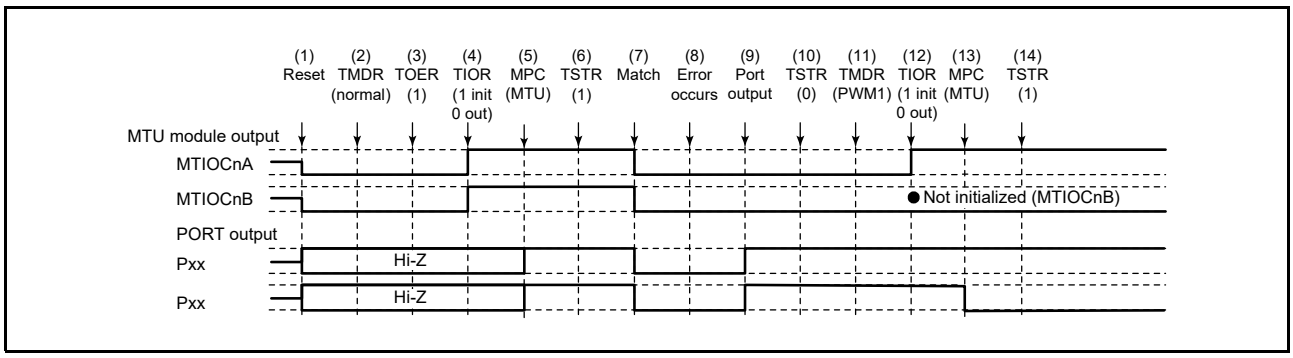


Figure 20.155 Error Occurrence in Normal Mode, Recovery in PWM Mode 1

(1) to (10) are the same as in Figure 20.154.
(11) Set PWM mode 1.
(12) Initialize the pins with the TIOR register. (In PWM mode 1, waveforms are not output to the MTIOCnB (MTIOCnD) pins. To output a specified level, make necessary settings for general output ports in the port direction registers (PDR) and port output data registers (PODR) of the I/O ports.)
(13) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(14) Restart operation by setting the TSTRA (TSTRB) register.

(3) Operation When Error Occurs in Normal Mode and Operation is Restarted in PWM mode 2

Figure 20.156 shows a case in which an error occurs in normal mode and operation is restarted in PWM mode 2 after re-setting.

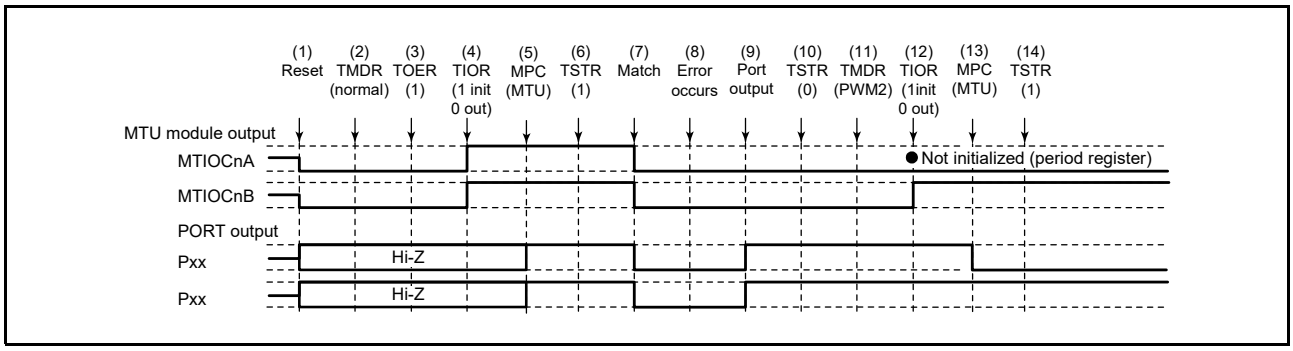


Figure 20.156 Error Occurrence in Normal Mode, Recovery in PWM Mode 2

(1) to (10) are the same as in Figure 20.154.
(11) Set PWM mode 2.
(12) Initialize the pins with the TIOR register. (In PWM mode 2, a waveform is not output to the pin that corresponds to the TGR register used as a period register. To output a specified level, make necessary settings for general output ports in the port direction registers (PDR) and port output data registers (PODR) of the I/O ports.)
(13) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(14) Restart operation by setting the TSTRA register.

Note: PWM mode 2 can only be selected for MTU0 to MTU2 and MTU9, and therefore the TOERA register setting is not necessary.

(4) Operation When Error Occurs in Normal Mode and Operation is Restarted in Phase Counting Mode

Figure 20.157 shows a case in which an error occurs in normal mode and operation is restarted in phase counting mode after re-setting.

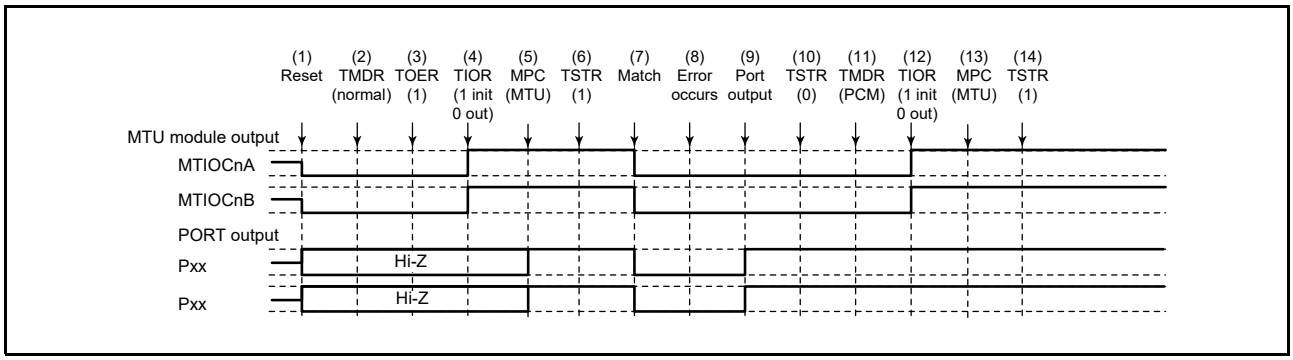


Figure 20.157 Error Occurrence in Normal Mode, Recovery in Phase Counting Mode

(1) to (10) are the same as in Figure 20.154.
(11) Set the phase counting mode.
(12) Initialize the pins with the TIOR register.
(13) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(14) Restart operation by setting the TSTRA register.

Note: The phase counting mode can only be selected for MTU1 and MTU2, and therefore the TOERA register setting is not necessary.

(5) Operation When Error Occurs in Normal Mode and Operation is Restarted in Complementary PWM Mode

Figure 20.158 shows a case in which an error occurs in normal mode and operation is restarted in complementary PWM mode after re-setting.

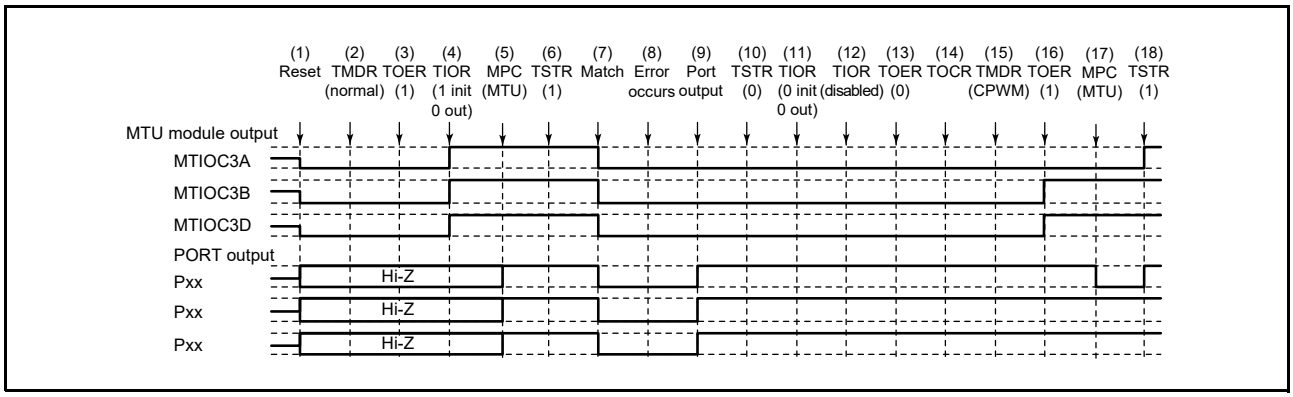


Figure 20.158 Error Occurrence in Normal Mode, Recovery in Complementary PWM Mode

(1) to (10) are the same as in Figure 20.154.
(11) Initialize the normal mode waveform generation block with the TIOR register.
(12) Disable operation of the normal mode waveform generation block with the TIOR register.
(13) Disable output in MTU3 and MTU4 (MTU6 and MTU7) with the TOERA (TOERB) register.
(14) Select the complementary PWM output level and enable or disable cyclic output with registers TOCR1A and TOCR2A (TOCR1B and TOCR2B).
(15) Set complementary PWM mode.
(16) Enable output in MTU3 and MTU4 (MTU6 and MTU7) with the TOERA (TOERB) register.
(17) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(18) Restart operation by setting the TSTRA (TSTRB) register.

(6) Operation When Error Occurs in Normal Mode and Operation is Restarted in Reset-Synchronized PWM Mode

Figure 20.159 shows a case in which an error occurs in normal mode and operation is restarted in reset-synchronized PWM mode after re-setting.

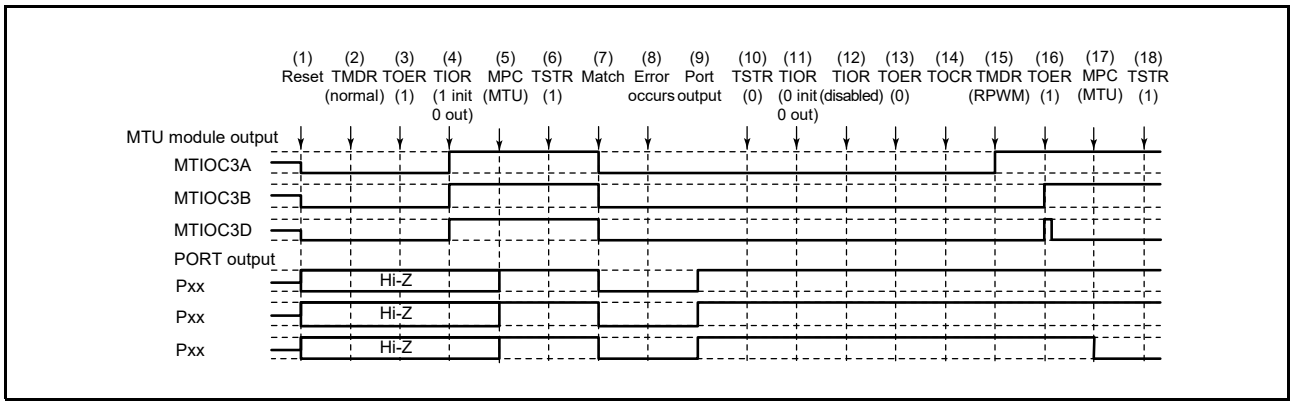


Figure 20.159 Error Occurrence in Normal Mode, Recovery in Reset-Synchronized PWM Mode

(1) to (13) are the same as in Figure 20.158.

(14) Select the reset-synchronized PWM output level and enable or disable cyclic output with registers TOCR1A and TOCR2A (TOCR1B and TOCR2B).

(15) Set reset-synchronized PWM mode.

(16) Enable output in MTU3 and MTU4 (MTU6 and MTU7) with the TOERA (TOERB) register.

(17) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.

(18) Restart operation by setting the TSTRA (TSTRB) register.

(7) Operation When Error Occurs in PWM Mode 1 and Operation is Restarted in Normal Mode

Figure 20.160 shows a case in which an error occurs in PWM mode 1 and operation is restarted in normal mode after re-setting.

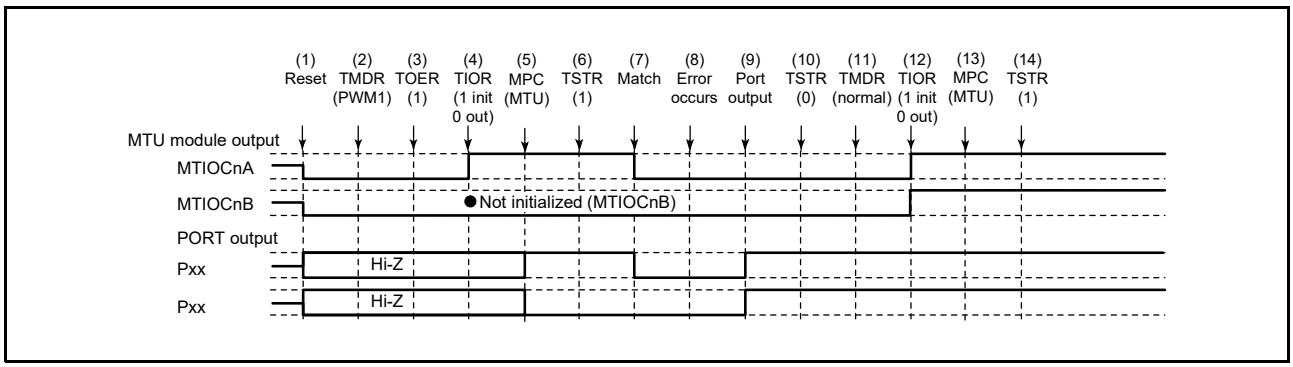


Figure 20.160 Error Occurrence in PWM Mode 1, Recovery in Normal Mode

(1) After a reset, the MTU output goes low and the ports enter high-impedance state.
(2) Set PWM mode 1.
(3) For MTU3 and MTU4 (MTU6 and MTU7), enable output with the TOERA (TOERB) register before initializing the pins with the TIOR register.
(4) Initialize the pins with the TIOR register. (In the example, the initial output is a high level, and a low level is output on compare match occurrence. In PWM mode 1, the MTIOCnB side is not initialized.)
(5) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(6) Start count operation by setting the TSTRA (TSTRB) register.
(7) Output goes low on compare match occurrence.
(8) An error occurs.
(9) Allow non-active level output by setting the pins as general output ports using the port direction registers (PDR), port output data registers (PODR), and port mode registers (PMR) of the I/O ports.
(10) Stop count operation by setting the TSTRA (TSTRB) register.
(11) Set normal mode.
(12) Initialize the pins with the TIOR register.
(13) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(14) Restart operation by setting the TSTRA (TSTRB) register.

(8) Operation When Error Occurs in PWM Mode 1 and Operation is Restarted in PWM mode 1

Figure 20.161 shows a case in which an error occurs in PWM mode 1 and operation is restarted in PWM mode 1 after re-setting.

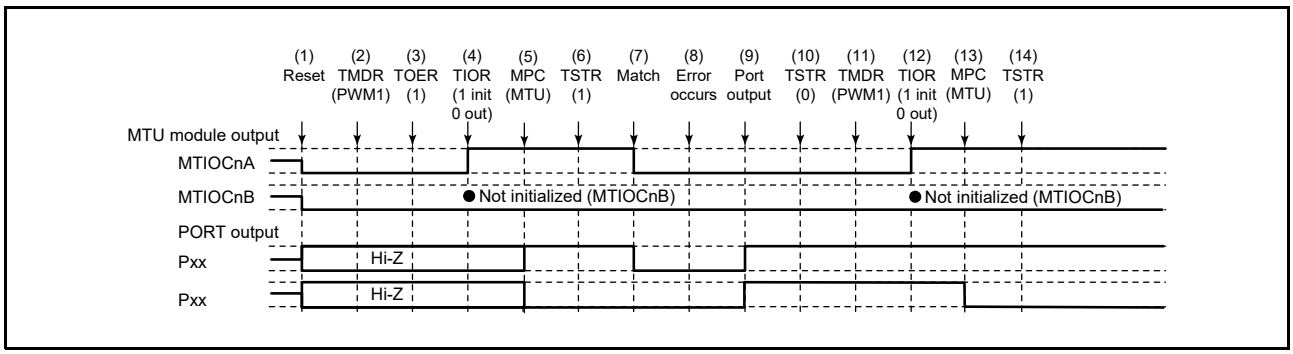


Figure 20.161 Error Occurrence in PWM Mode 1, Recovery in PWM Mode 1

(1) to (10) are the same as in Figure 20.160.
(11) This step is not necessary when restarting in PWM mode 1.
(12) Initialize the pins with the TIOR register. (In PWM mode 1, waveforms are not output to the MTIOCnB (MTIOCnD) pins. To output a specified level, make necessary settings for general output ports in the port direction registers (PDR) and port output data registers (PODR) of the I/O ports.)
(13) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(14) Restart operation by setting the TSTRA (TSTRB) register.

(9) Operation When Error Occurs in PWM Mode 1 and Operation is Restarted in PWM mode 2

Figure 20.162 shows a case in which an error occurs in PWM mode 1 and operation is restarted in PWM mode 2 after re-setting.

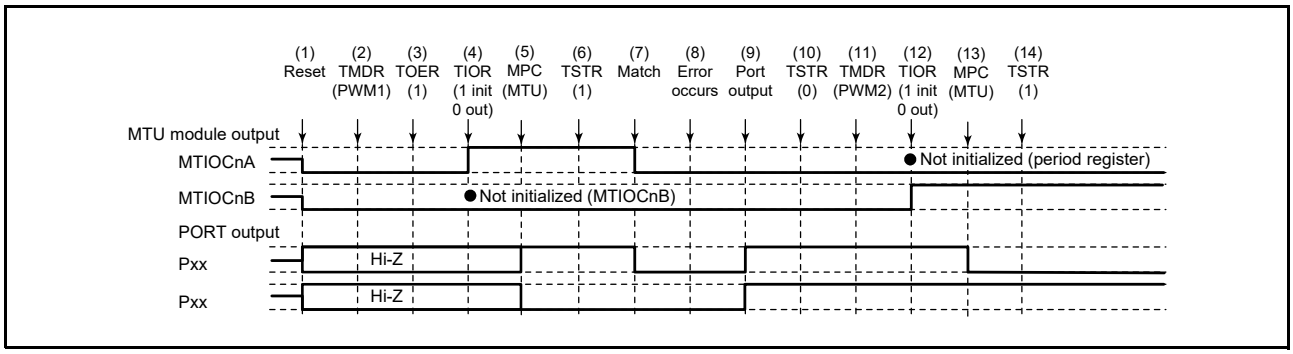


Figure 20.162 Error Occurrence in PWM Mode 1, Recovery in PWM Mode 2

(1) to (10) are the same as in Figure 20.160.
(11) Set PWM mode 2.
(12) Initialize the pins with the TIOR register. (In PWM mode 2, a waveform is not output to the pin that corresponds to the TGR register used as a period register. To output a specified level, make necessary settings for general output ports in the port direction registers (PDR) and port output data registers (PODR) of the I/O ports.)
(13) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(14) Restart operation by setting the TSTRA register.

Note: PWM mode 2 can only be selected for MTU0 to MTU2 and MTU9, and therefore the TOERA register setting is not necessary.

(10) Operation When Error Occurs in PWM Mode 1 and Operation is Restarted in Phase Counting Mode

Figure 20.163 shows a case in which an error occurs in PWM mode 1 and operation is restarted in phase counting mode after re-setting.

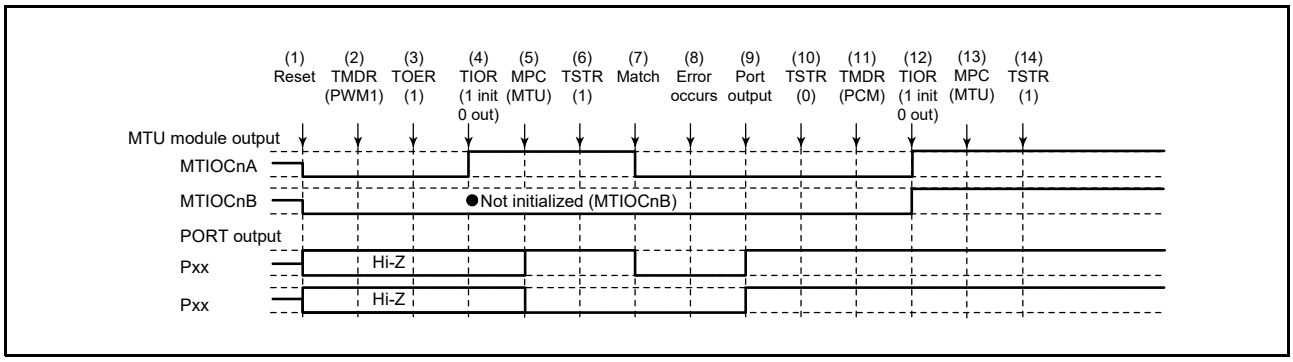


Figure 20.163 Error Occurrence in PWM Mode 1, Recovery in Phase Counting Mode

(1) to (10) are the same as in Figure 20.160.
(11) Set the phase counting mode.
(12) Initialize the pins with the TIOR register.
(13) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(14) Restart operation by setting the TSTRA register.

Note: The phase counting mode can only be selected for MTU1 and MTU2, and therefore the TOERA register setting is not necessary.

(11) Operation When Error Occurs in PWM Mode 1 and Operation is Restarted in Complementary PWM Mode

Figure 20.164 shows a case in which an error occurs in PWM mode 1 and operation is restarted in complementary PWM mode after re-setting.

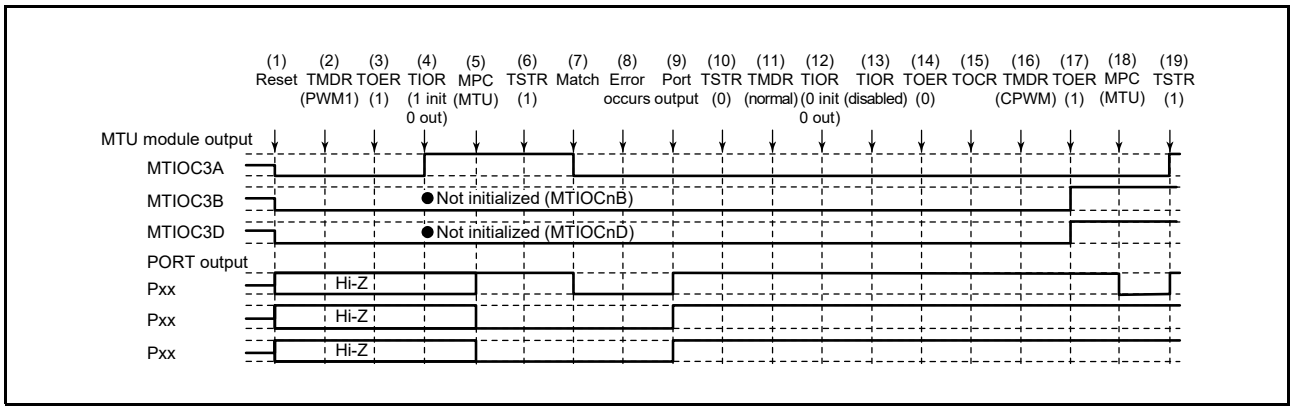


Figure 20.164 Error Occurrence in PWM Mode 1, Recovery in Complementary PWM Mode

(1) to (10) are the same as in Figure 20.160.
(11) Set normal mode to initialize the normal mode waveform generation block.
(12) Initialize the PWM mode 1 waveform generation block with the TIOR register.
(13) Disable operation of the PWM mode 1 waveform generation block with the TIOR register.
(14) Disable output in MTU3 and MTU4 (MTU6 and MTU7) with the TOERA (TOERB) register.
(15) Select the complementary PWM output level and enable or disable cyclic output with registers TOCR1A and TOCR2A (TSTRB).
(16) Set complementary PWM mode.
(17) Enable output in MTU3 and MTU4 (MTU6 and MTU7) with the TOERA (TOERB) register.
(18) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(19) Restart operation by setting the TSTRA (TSTRB) register.

(12) Operation When Error Occurs in PWM Mode 1 and Operation is Restarted in Reset-Synchronized PWM Mode

Figure 20.165 shows a case in which an error occurs in PWM mode 1 and operation is restarted in reset-synchronized PWM mode after re-setting.

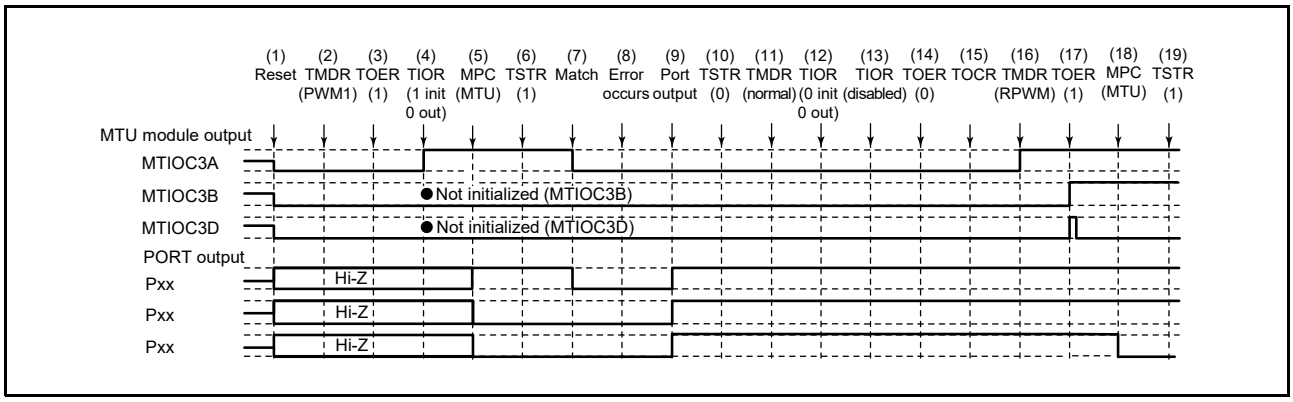


Figure 20.165 Error Occurrence in PWM Mode 1, Recovery in Reset-Synchronized PWM Mode

(1) to (14) are the same as in Figure 20.164.

(15) Select the reset-synchronized PWM output level and enable or disable cyclic output with registers TOCR1A and TOCR2A (TOCR1B and TOCR2B).

(16) Set reset-synchronized PWM mode.

(17) Enable output in MTU3 and MTU4 (MTU6 and MTU7) with the TOERA (TOERB) register.

(18) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.

(19) Restart operation by setting the TSTRA (TSTRB) register.

(13) Operation When Error Occurs in PWM Mode 2 and Operation is Restarted in Normal Mode

Figure 20.166 shows a case in which an error occurs in PWM mode 2 and operation is restarted in normal mode after re-setting.

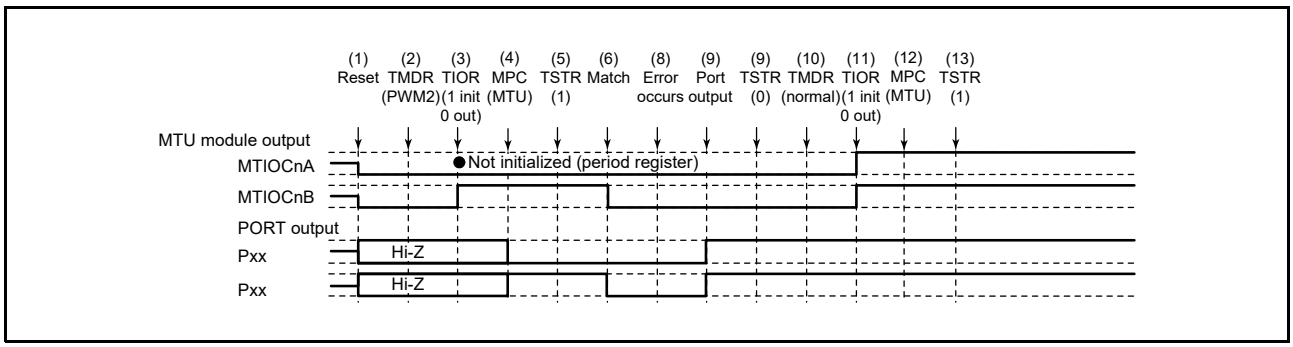


Figure 20.166 Error Occurrence in PWM Mode 2, Recovery in Normal Mode

(1) After a reset, the MTU output goes low and the ports enter high-impedance state.
(2) Set PWM mode 2.
(3) Initialize the pins with the TIOR register. (In the example, the initial output is a high level, and a low level is output on compare match occurrence. In PWM mode 2, the pin that corresponds to the TGR register used as a period register is not initialized. In the example, the the MTUn.TGRA register is used as a period register.)
(4) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(5) Start count operation by setting the TSTRA register.
(6) Output goes low on compare match occurrence.
(7) An error occurs.
(8) Allow non-active level output by setting the pins as general output ports using the port direction registers (PDR), port output data registers (PODR), and port mode registers (PMR) of the I/O ports.
(9) Stop count operation by setting the TSTRA register.
(10) Set normal mode.
(11) Initialize the pins with the TIOR register.
(12) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(13) Restart operation by setting the TSTRA register.

(14) Operation When Error Occurs in PWM Mode 2 and Operation is Restarted in PWM Mode 1

Figure 20.167 shows a case in which an error occurs in PWM mode 2 and operation is restarted in PWM mode 1 after re-setting.

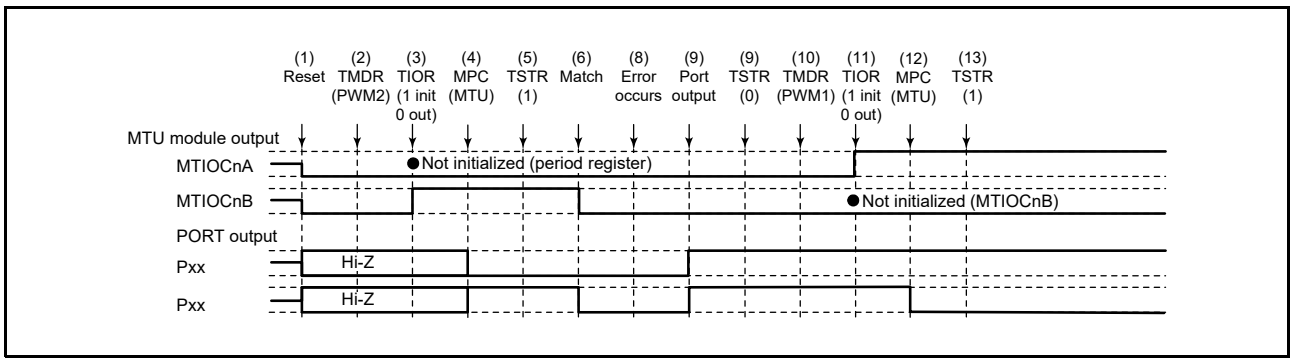


Figure 20.167 Error Occurrence in PWM Mode 2, Recovery in PWM Mode 1

(1) to (9) are the same as in Figure 20.166.
(10) Set PWM mode 1.
(11) Initialize the pins with the TIOR register. (In PWM mode 1, waveforms are not output to the MTIOCnB (MTIOCnD) pins.
To output a specified level, make necessary settings for general output ports in the port direction registers (PDR) and port output data registers (PODR) of the I/O ports.)
(12) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(13) Restart operation by setting the TSTRA register.

(15) Operation When Error Occurs in PWM Mode 2 and Operation is Restarted in PWM Mode 2

Figure 20.168 shows a case in which an error occurs in PWM mode 2 and operation is restarted in PWM mode 2 after re-setting.

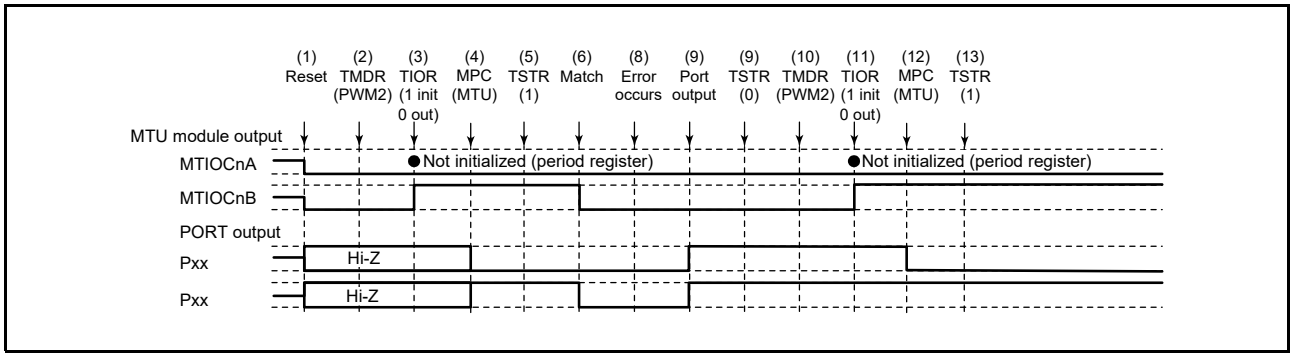


Figure 20.168 Error Occurrence in PWM Mode 2, Recovery in PWM Mode 2

(1) to (9) are the same as in Figure 20.166.
(10) This step is not necessary when restarting in PWM mode 2.
(11) Initialize the pins with the TIOR register. (In PWM mode 2, a waveform is not output to the pin that corresponds to the TGR register used as a period register. To output a specified level, make necessary settings for general output ports in the port direction registers (PDR) and port output data registers (PODR) of the I/O ports.)
(12) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(13) Restart operation by setting the TSTRA register.

(16) Operation When Error Occurs in PWM Mode 2 and Operation is Restarted in Phase Counting Mode

Figure 20.169 shows a case in which an error occurs in PWM mode 2 and operation is restarted in phase counting mode after re-setting.

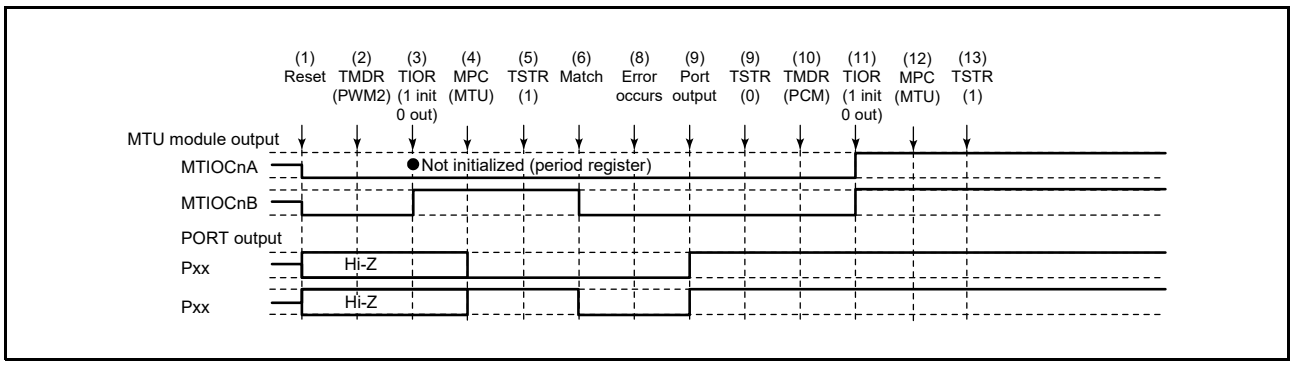


Figure 20.169 Error Occurrence in PWM Mode 2, Recovery in Phase Counting Mode

(1) to (9) are the same as in Figure 20.166.
(10) Set the phase counting mode.
(11) Initialize the pins with the TIOR register.
(12) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(13) Restart operation by setting the TSTRA register.

(17) Operation When Error Occurs in Phase Counting Mode and Operation is Restarted in Normal Mode

Figure 20.170 shows a case in which an error occurs in phase counting mode and operation is restarted in normal mode after re-setting.

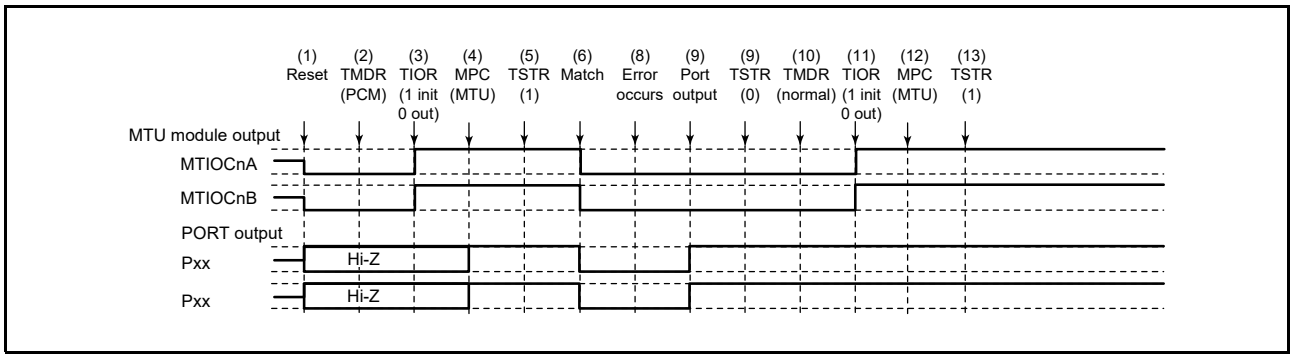


Figure 20.170 Error Occurrence in Phase Counting Mode, Recovery in Normal Mode

(1) After a reset, the MTU output goes low and the ports enter high-impedance state.
(2) Set phase counting mode.
(3) Initialize the pins with the TIOR register. (In the example, the initial output is a high level, and a low level is output on compare match occurrence.)
(4) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(5) Start count operation by setting the TSTRA register.
(6) Output goes low on compare match occurrence.
(7) An error occurs.
(8) Allow non-active level output by setting the pins as general output ports using the port direction registers (PDR), port output data registers (PODR), and port mode registers (PMR) of the I/O ports.
(9) Stop count operation by setting the TSTRA register.
(10) Set normal mode.
(11) Initialize the pins with the TIOR register.
(12) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(13) Restart operation by setting the TSTRA register.

(18) Operation When Error Occurs in Phase Counting Mode and Operation is Restarted in PWM Mode 1

Figure 20.171 shows a case in which an error occurs in phase counting mode and operation is restarted in PWM mode 1 after re-setting.

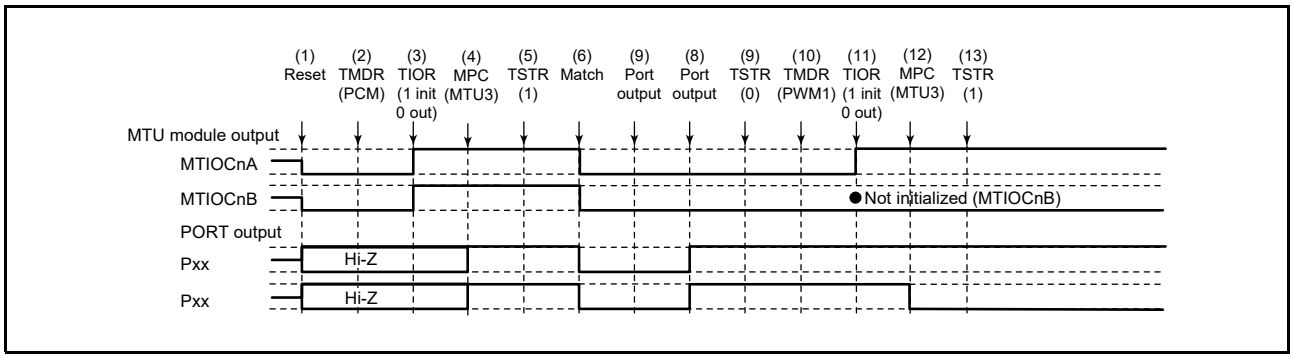


Figure 20.171 Error Occurrence in Phase Counting Mode, Recovery in PWM Mode 1

(1) to (9) are the same as in Figure 20.170.
(10) Set PWM mode 1.
(11) Initialize the pins with the TIOR register. (In PWM mode 1, waveforms are not output to the MTIOCnB (MTIOCnD) pins.
To output a specified level, make necessary settings for general output ports in the port direction registers (PDR) and port output data registers (PODR) of the I/O ports.)
(12) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(13) Restart operation by setting the TSTRA register.

(19) Operation When Error Occurs in Phase Counting Mode and Operation is Restarted in PWM Mode 2

Figure 20.172 shows a case in which an error occurs in phase counting mode and operation is restarted in PWM mode 2 after re-setting.

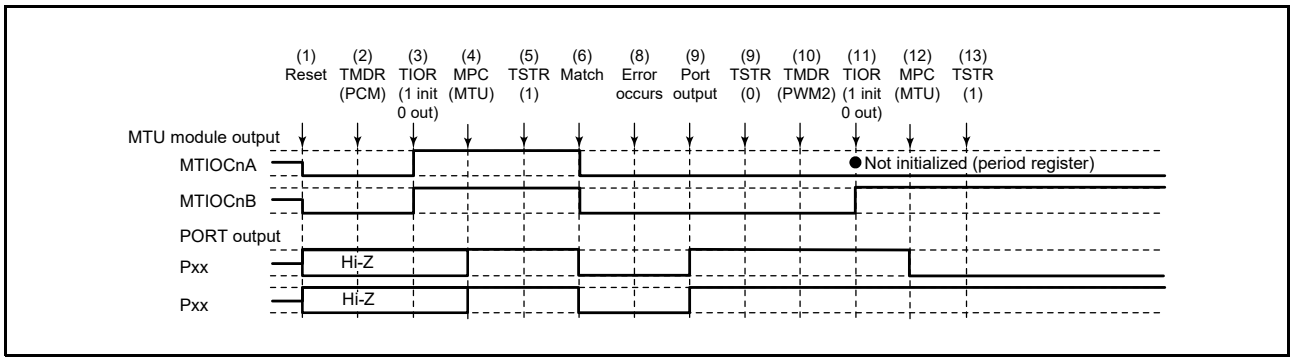


Figure 20.172 Error Occurrence in Phase Counting Mode, Recovery in PWM Mode 2

(1) to (9) are the same as in Figure 20.170.
(10) Set PWM mode 2.
(11) Initialize the pins with the TIOR register. (In PWM mode 2, a waveform is not output to the pin that corresponds to the TGR register used as a period register. To output a specified level, make necessary settings for general output ports in the port direction registers (PDR) and port output data registers (PODR) of the I/O ports.)
(12) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(13) Restart operation by setting the TSTRA register.

(20) Operation When Error Occurs in Phase Counting Mode and Operation is Restarted in Phase Counting Mode

Figure 20.173 shows a case in which an error occurs in phase counting mode and operation is restarted in phase counting mode after re-setting.

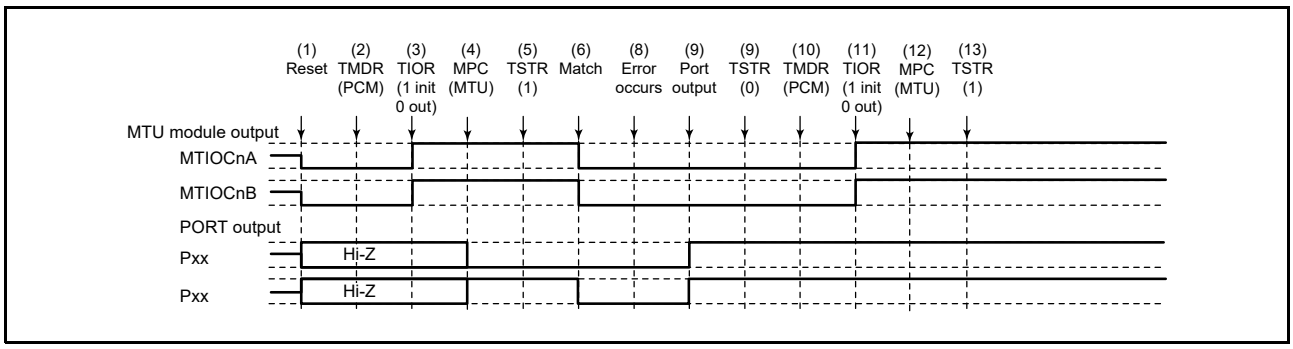


Figure 20.173 Error Occurrence in Phase Counting Mode, Recovery in Phase Counting Mode

(1) to (9) are the same as in Figure 20.170.
(10) This step is not necessary when restarting in phase counting mode.
(11) Initialize the pins with the TIOR register.
(12) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(13) Restart operation by setting the TSTRA register.

(21) Operation When Error Occurs in Complementary PWM Mode and Operation is Restarted in Normal Mode

Figure 20.174 shows a case in which an error occurs in complementary PWM mode and operation is restarted in normal mode after re-setting.

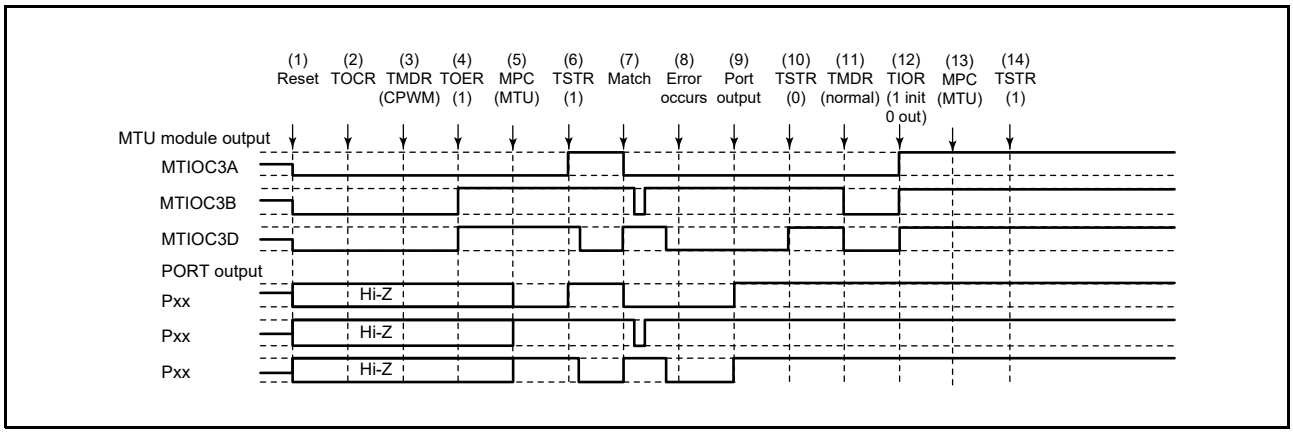


Figure 20.174 Error Occurrence in Complementary PWM Mode, Recovery in Normal Mode

(1) After a reset, the MTU3 output goes low and the ports enter high-impedance state.
(2) Select the complementary PWM output level and enable or disable cyclic output with registers TOCR1A and TOCR2A (TOCR1B and TOCR2B).
(3) Set complementary PWM mode.
(4) Enable output in MTU3 and MTU4 (MTU6 and MTU7) with the TOERA (TOERB) register.
(5) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(6) Start count operation by setting the TSTRA (TSTRB) register.
(7) The complementary PWM waveform is output on compare match occurrence.
(8) An error occurs.
(9) Allow non-active level output by setting the pins as general output ports using the port direction registers (PDR), port output data registers (PODR), and port mode registers (PMR) of the I/O ports.
(10) Stop count operation by setting the TSTRA (TSTRB) register. (MTU output becomes the initial complementary PWM output value).
(11) Set normal mode (MTU output goes low).
(12) Initialize the pins with the TIOR register.
(13) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(14) Restart operation by setting the TSTRA (TSTRB) register.

(22) Operation When Error Occurs in Complementary PWM Mode and Operation is Restarted in PWM Mode 1

Figure 20.175 shows a case in which an error occurs in complementary PWM mode and operation is restarted in PWM mode 1 after re-setting.

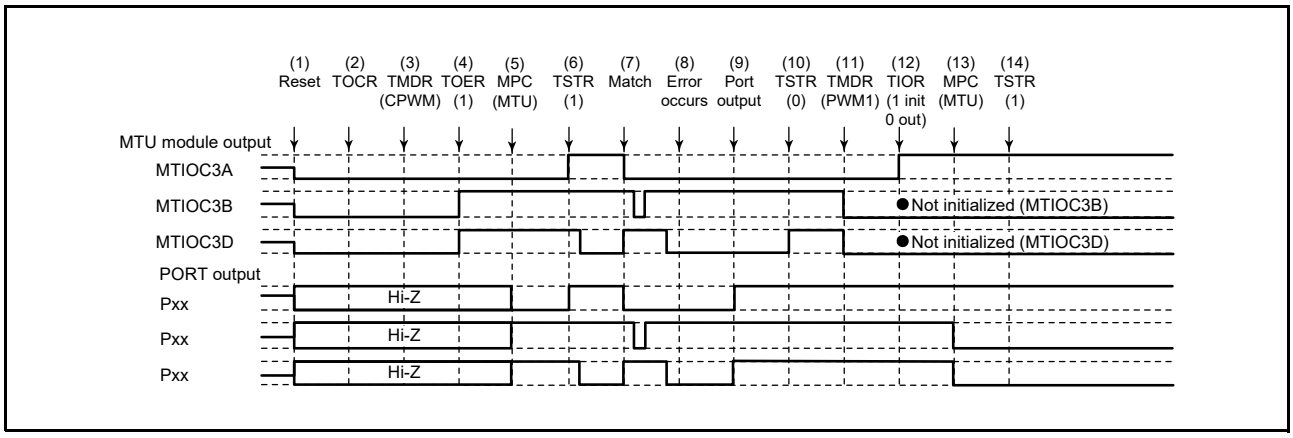


Figure 20.175 Error Occurrence in Complementary PWM Mode, Recovery in PWM Mode 1

(1) to (10) are the same as in Figure 20.174.
(11) Set PWM mode 1 (MTU output goes low).
(12) Initialize the pins with the TIOR register. (In PWM mode 1, waveforms are not output to the MTIOCnB (MTIOCnD) pins. To output a specified level, make necessary settings for general output ports in the port direction registers (PDR) and port output data registers (PODR) of the I/O ports.)
(13) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(14) Restart operation by setting the TSTRA (TSTRB) register.

(23) Operation When Error Occurs in Complementary PWM Mode and Operation is Restarted in Complementary PWM Mode

Figure 20.176 shows a case in which an error occurs in complementary PWM mode and operation is restarted in complementary PWM mode after re-setting (when operation is restarted using the period and duty settings at the time of stopping the counter).

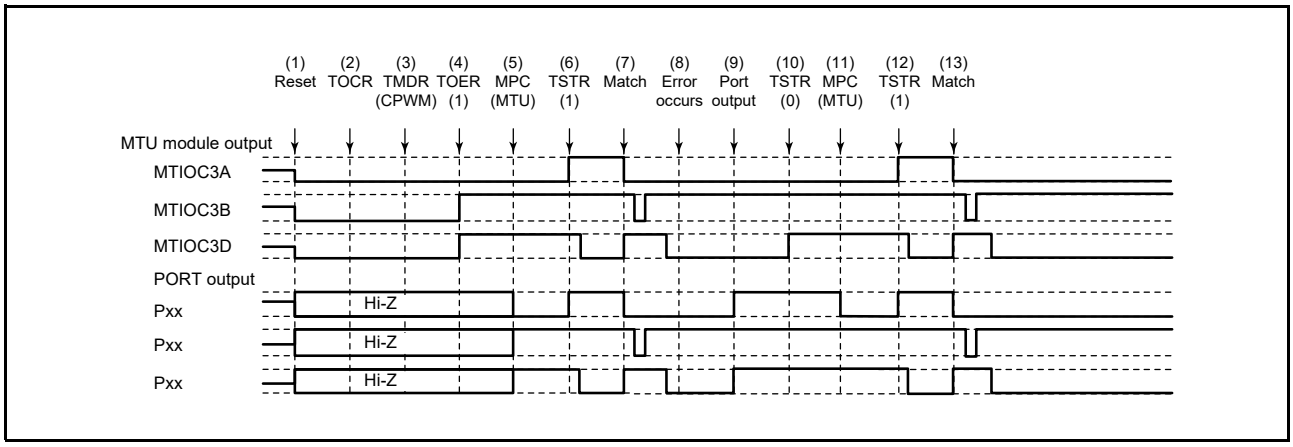


Figure 20.176 Error Occurrence in Complementary PWM Mode, Recovery in Complementary PWM Mode (1)

(1) to (10) are the same as in Figure 20.174.
(11) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(12) Restart operation by setting the TSTRA (TSTRB) register.
(13) The complementary PWM waveform is output on compare match occurrence.

(24) Operation When Error Occurs in Complementary PWM Mode and Operation is Restarted in Complementary PWM Mode with New Settings

Figure 20.177 shows a case in which an error occurs in complementary PWM mode and operation is restarted in complementary PWM mode after re-setting (operation is restarted using new period and duty ratio settings).

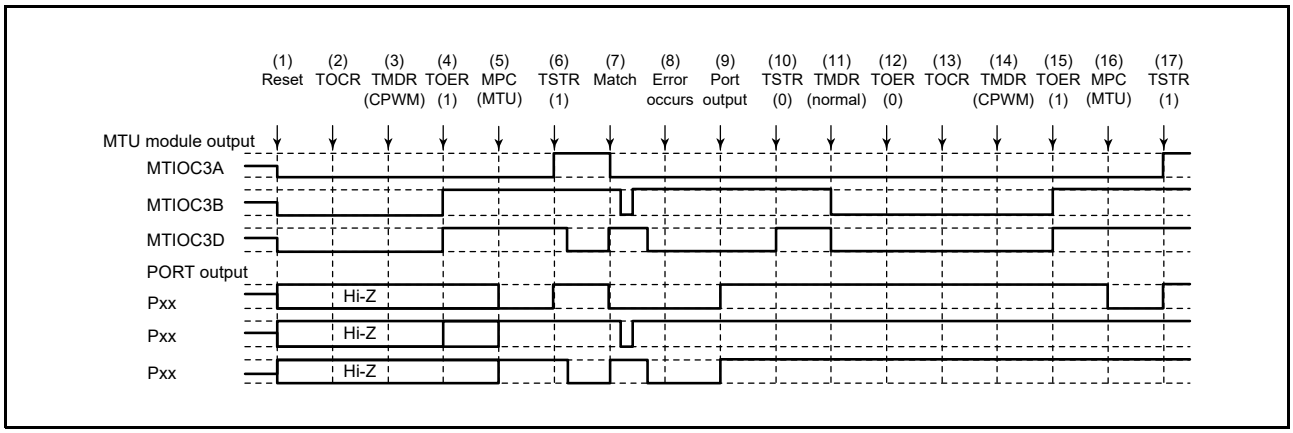


Figure 20.177 Error Occurrence in Complementary PWM Mode, Recovery in Complementary PWM Mode (2)

(1) to (10) are the same as in Figure 20.174.
(11) Set normal mode and make new settings (MTU output goes low).
(12) Disable output in MTU3 and MTU4 (MTU6 and MTU7) with the TOERA (TOERB) register.
(13) Select the complementary PWM output level and enable or disable cyclic output with registers TOCR1A and TOCR2A (TOCR1B and TOCR2B).
(14) Set complementary PWM mode.
(15) Enable output in MTU3 and MTU4 (MTU6 and MTU7) with the TOERA (TOERB) register.
(16) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(17) Restart operation by setting the TSTRA (TSTRB) register.

(25) Operation When Error Occurs in Complementary PWM Mode and Operation is Restarted in Reset-Synchronized PWM Mode

Figure 20.178 shows a case in which an error occurs in complementary PWM mode and operation is restarted in reset-synchronized PWM mode after re-setting.

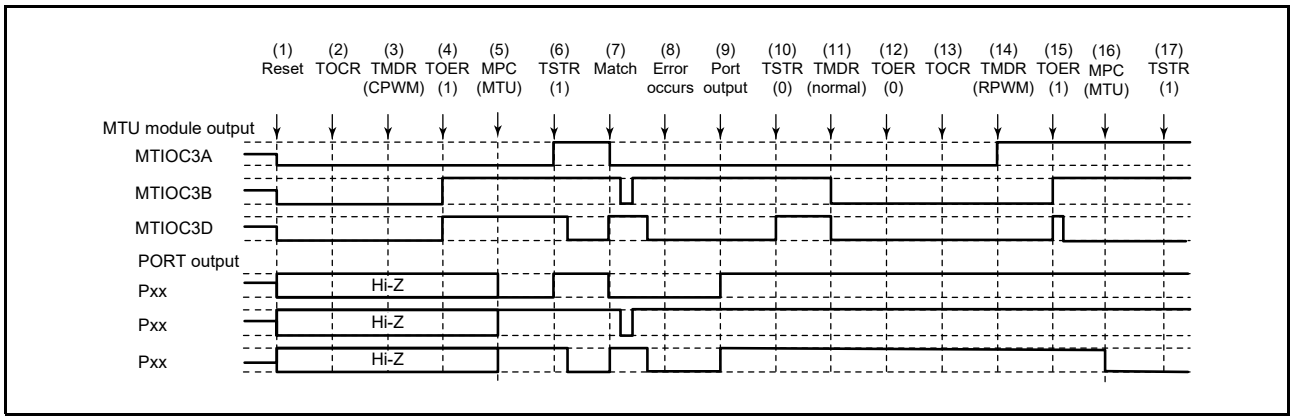


Figure 20.178 Error Occurrence in Complementary PWM Mode, Recovery in Reset-Synchronized PWM Mode

(1) to (10) are the same as in Figure 20.174.
(11) Set normal mode (MTU output goes low).
(12) Disable output in MTU3 and MTU4 (MTU6 and MTU7) with the TOERA (TOERB) register.
(13) Select the reset-synchronized PWM output level and enable or disable cyclic output with registers TOCR1A and TOCR2A (TOCR1B and TOCR2B).
(14) Set reset-synchronized PWM mode.
(15) Enable output in MTU3 and MTU4 (MTU6 and MTU7) with the TOERA (TOERB) register.
(16) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(17) Restart operation by setting the TSTRA (TSTRB) register.

(26) Operation When Error Occurs in Reset-Synchronized PWM Mode and Operation is Restarted in Normal Mode

Figure 20.179 shows a case in which an error occurs in reset-synchronized PWM mode and operation is restarted in normal mode after re-setting.

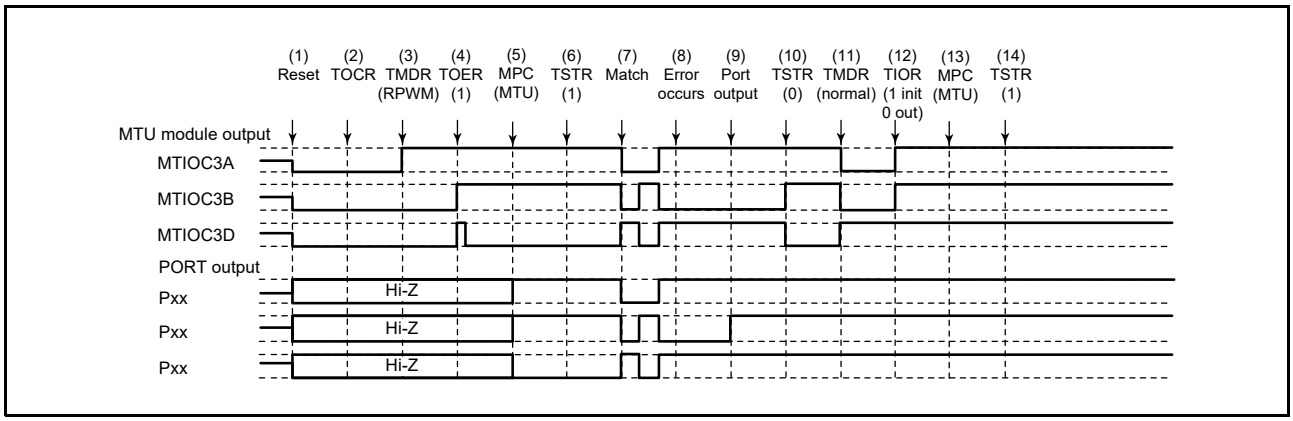


Figure 20.179 Error Occurrence in Reset-Synchronized PWM Mode, Recovery in Normal Mode

(1) After a reset, the MTU output goes low and the ports enter high-impedance state.
(2) Select the reset-synchronized PWM output level and enable or disable cyclic output with registers TOCR1A and TOCR2A (TOCR1B and TOCR2B).
(3) Set reset-synchronized PWM mode.
(4) Enable output in MTU3 and MTU4 (MTU6 and MTU7) with the TOERA (TOERB) register.
(5) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(6) Start count operation by setting the TSTRA (TSTRB) register.
(7) The reset-synchronized PWM waveform is output on compare match occurrence.
(8) An error occurs.
(9) Allow non-active level output by setting the pins as general output ports using the port direction registers (PDR), port output data registers (PODR), and port mode registers (PMR) of the I/O ports.
(10) Stop count operation by setting the TSTRA (TSTRB) register. (MTU output becomes the initial reset-synchronized PWM output value.)
(11) Set normal mode (positive-phase MTU output goes low, and negative-phase output goes high).
(12) Initialize the pins with the TIOR register.
(13) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(14) Restart operation by setting the TSTRA (TSTRB) register.

(27) Operation When Error Occurs in Reset-Synchronized PWM Mode and Operation is Restarted in PWM Mode 1

Figure 20.180 shows a case in which an error occurs in reset-synchronized PWM mode and operation is restarted in PWM mode 1 after re-setting.

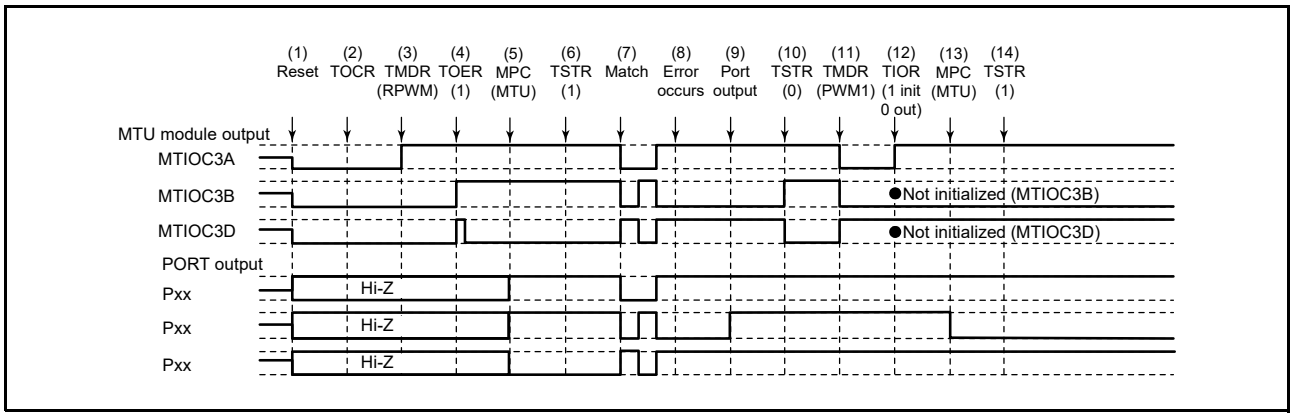


Figure 20.180 Error Occurrence in Reset-Synchronized PWM Mode, Recovery in PWM Mode 1

(1) to (10) are the same as in Figure 20.179.
(11) Set PWM mode 1 (positive-phase MTU output goes low, and negative-phase output goes high).
(12) Initialize the pins with the TIOR register. (In PWM mode 1, waveforms are not output to the MTIOCnB (MTIOCnD) pins. To output a specified level, make necessary settings for general output ports in the port direction registers (PDR) and port output data registers (PODR) of the I/O ports.)
(13) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(14) Restart operation by setting the TSTRA (TSTRB) register.

(28) Operation When Error Occurs in Reset-Synchronized PWM Mode and Operation is Restarted in Complementary PWM Mode

Figure 20.181 shows a case in which an error occurs in reset-synchronized PWM mode and operation is restarted in complementary PWM mode after re-setting.

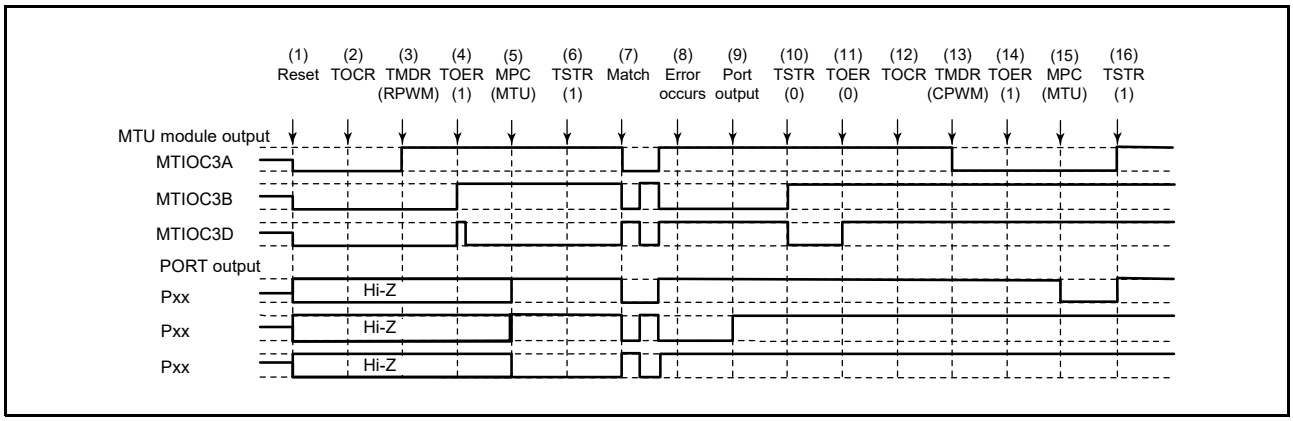


Figure 20.181 Error Occurrence in Reset-Synchronized PWM Mode, Recovery in Complementary PWM Mode

(1) to (10) are the same as in Figure 20.179.
(11) Disable output in MTU3 and MTU4 (MTU6 and MTU7) with the TOERA (TOERB) register.
(12) Select the complementary PWM output level and enable or disable cyclic output with registers TOCR1A and TOCR2A (TOCR1B and TOCR2B).
(13) Set complementary PWM mode (MTU cyclic output pin goes low).
(14) Enable output in MTU3 and MTU4 (MTU6 and MTU7) with the TOERA (TOERB) register.
(15) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(16) Restart operation by setting the TSTRA (TSTRB) register.

(29) Operation When Error Occurs in Reset-Synchronized PWM Mode and Operation is Restarted in Reset-Synchronized PWM Mode

Figure 20.182 shows a case in which an error occurs in reset-synchronized PWM mode and operation is restarted in reset-synchronized PWM mode after re-setting.

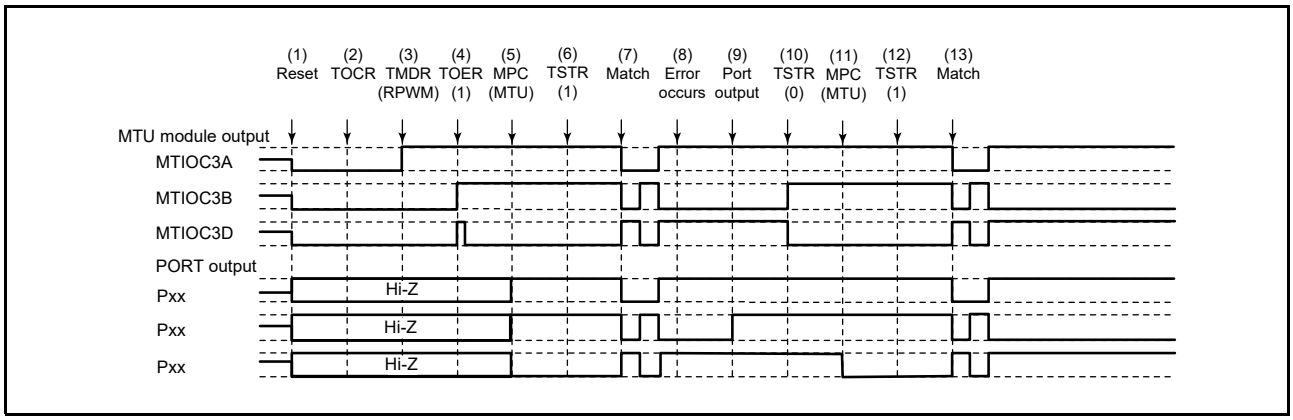


Figure 20.182 Error Occurrence in Reset-Synchronized PWM Mode, Recovery in Reset-Synchronized PWM Mode

(1) to (10) are the same as in Figure 20.179.
(11) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(12) Restart operation by setting the TSTRA (TSTRB) register.
(13) The reset-synchronized PWM waveform is output on compare match occurrence.

21. Port Output Enable 3 (POE3A)

This MCU incorporates a port output enable 3 (POE3A) which can be used to, under various conditions, disable output signals for the MTU and the GPT. The output status can be selected from high-impedance or general I/O port while the output is disabled.
In this section, “PCLK” is used to refer to PCLKB.

21.1 Overview

Table 21.1 lists the specifications of the POE, and Figure 21.1 shows a block diagram of the POE.

Table 21.1 POE Specifications

Item	Description
Pin status while output is disabled	• High-impedance • General I/O port
Target pins for disabling of signal output	• MTU output pins MTU0 pins (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) MTU3 pins (MTIOC3B, MTIOC3D) MTU4 pins (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D) MTU6 pins (MTIOC6B, MTIOC6D) MTU7 pins (MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D) MTU9 pins (MTIOC9A, MTIOC9B, MTIOC9C, MTIOC9D) • GPT output pins GPT0 pins (GTIOC0A, GTIOC0B) GPT1 pins (GTIOC1A, GTIOC1B) GPT2 pins (GTIOC2A, GTIOC2B) GPT3 pins (GTIOC3A, GTIOC3B)
Generating conditions of request to disable output	• Input signal detection: Detection of the POE0#, POE4#, POE8#, POE10#, POE11#, and POE12# signal level. • Simultaneous conduction between output pins: A match (simultaneous conduction) between the output signal levels at the active level over one or more cycles on the following combination of pins • Register setting to disable output being made • Detection that the main clock oscillator had stopped oscillating • Comparator output detection in the comparator C (CMPC)
Function	• Each of the POE0#, POE4#, POE8#, POE10#, POE11#, and POE12# input pins can be set for falling edge, PCLK/8 × 16, PCLK/16 × 16, or PCLK/128 × 16 low-level sampling. • The outputs of the target pins can be disabled by falling-edge or low-level sampling of the POE0#, POE4#, POE8#, POE10#, POE11#, or POE12# pin. • The outputs of the target pins can be disabled when oscillation stop is detected by the oscillation stop detection function of the clock generator. • The MTU complementary PWM outputs can be disabled when output levels of the MTU complementary PWM output pins are compared and simultaneous active-level output continues for one cycle or more. • The GPT outputs can be disabled when output levels of the GPT output pins (GPT0, GPT1, and GPT2) are compared and simultaneous active-level output continues for one cycle or more. • The outputs of the target pins can be disabled in response to comparator C (CMPC) output detection. • The outputs of the target pins can be disabled by modifying the settings of the POE registers. • Interrupts can be generated by input-level sampling or output-level comparison results.

	MTU Complementary PWM Output Pins
1	MTIOC3B and MTIOC3D
2	MTIOC4A and MTIOC4C
3	MTIOC4B and MTIOC4D
4	MTIOC6B and MTIOC6D
5	MTIOC7A and MTIOC7C
6	MTIOC7B and MTIOC7D

	GPT Output Pins
1	GTIOC0A and GTIOC0B
2	GTIOC1A and GTIOC1B
3	GTIOC2A and GTIOC2B

The POE has input-level detection circuits, output-level comparison circuits, and a high-impedance request/port switching request/interrupt request generating circuit as shown in Figure 21.1.

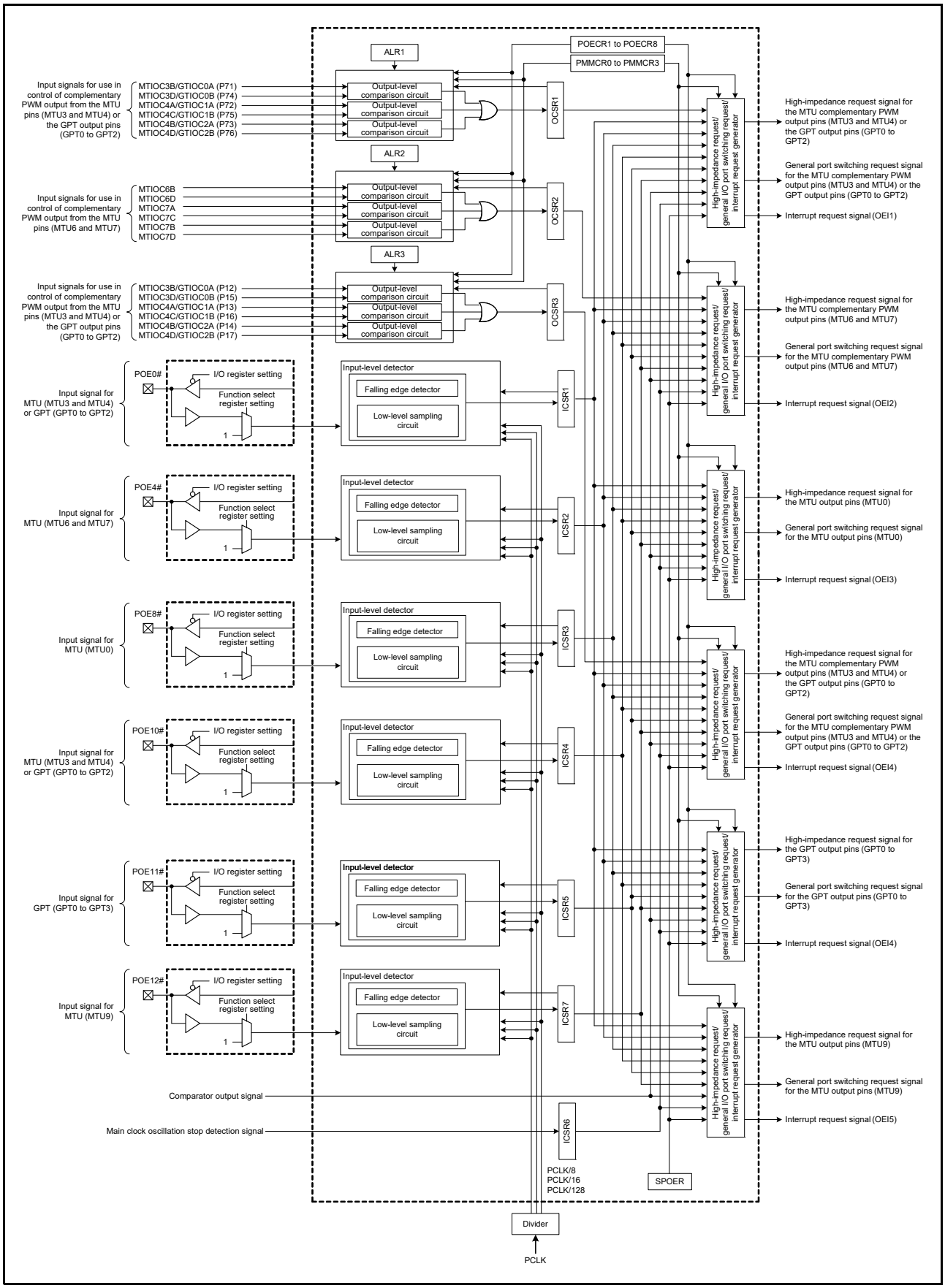


Figure 21.1 POE Block Diagram

Table 21.2 shows I/O pins to be used by the POE.

Table 21.2 POE I/O Pins

Pin Name	I/O	Description
POE0#	Input	Request signal to disable the outputs of the MTU complementary PWM output pins (MTU3, MTU4 pins) or GPT output pins of P71 to P76, and is also capable of controlling the other target pins by register settings.
POE4#	Input	Request signal to disable the output of the MTU complementary PWM output pins (MTU6, MTU7 pins), and is also capable of controlling the other target pins by register settings.
POE8#	Input	Request signal to disable the output of the MTU0 pins, and is also capable of controlling the other target pins by register settings.
POE10#	Input	Request signal to disable the output of the MTU complementary PWM output pins (MTU3, MTU4 pins) or GPT output pins of P12 to P17, and is also capable of controlling the other target pins by register settings.
POE11#	Input	Request signal to disable the output of the GPT0 to GPT3 pins of PB5 to PB7, PD0 to PD2, PD6, and PD7, and is also capable of controlling the other target pins by register settings.
POE12#	Input	Request signal to disable the output of the MTU9 pins, and is also capable of switching the other target pins by register settings.

Table 21.3 shows output-level comparisons with pin combinations.

Table 21.3 Pin Combinations

Pin Combination	I/O	Description
MTIOC3B and MTIOC3D	Output	The MTU complementary PWM output pins (MTU3 and MTU4 pins) are disabled when two pins of the set simultaneously output the active level (low level when the MTUn.TOCR1A.OLSP bit is 0 or high level when the OLSP bit is 1 while the OLSEN bit in the ALR1 or ALR3 register is 0 and the MTUn.TOCR1A.TOCS bit is 0, low level when the OLS1P, OLS1N, OLS2P, OLS2N, OLS3P, and OLS3N bits in the MTUn.TOCR2A register are 0 or high level when these bits are 1 while the OLSEN bit in the ALR1 or ALR3 register is 0 and the MTUn.TOCR1A.TOCS bit is 1, or low level when the OLSG0A, OLSG0B, OLSG1A, OLSG1B, OLSG2A, and OLSG2B bits in the ALR1 or ALR3 register are 0 and high level when these bits are 1 while the OLSEN bit in the ALR1 or ALR3 register is 1) for at least 1 cycle of the peripheral module clock (PCLK). Pin combinations for output comparison can be selected by registers of POE.
MTIOC4A and MTIOC4C	Output	
MTIOC4B and MTIOC4D	Output	
MTIOC6B and MTIOC6D	Output	The MTU complementary PWM output pins (MTU6 and MTU7 pins) are disabled when two pins of the set simultaneously output the active level (low level when the MTUn.TOCR1B.OLSP bit is 0 or high level when the OLSP bit is 1 while the ALR2.OLSEN bit is 0 and the MTUn.TOCR1B.TOCS bit is 0, low level when the OLS1P, OLS1N, OLS2P, OLS2N, OLS3P, and OLS3N bits in the MTUn.TOCR2B register are 0 or high level when these bits are 1 while the ALR2.OLSEN bit is 0 and the MTUn.TOCR1B.TOCS bit is 1, or low level when the OLSG4A, OLSG4B, OLSG5A, OLSG5B, OLSG6A, and OLSG6B bits in the ALR2 register is 0 or high level when these bits are 1 while the ALR2.OLSEN bit is 1) for at least 1 cycle of the peripheral module clock (PCLK). Pin combinations for output comparison can be selected by registers of POE.
MTIOC7A and MTIOC7C	Output	
MTIOC7B and MTIOC7D	Output	
GTIOC0A and GTIOC0B	Output	The GPT output pins (GPT0 to GPT2 pins) are disabled when two pins of the set simultaneously output the active level (low level when the OLSG0A, OLSG0B, OLSG1A, OLSG1B, OLSG2A, and OLSG2B bits in the ALR1 or ALR3 register are 0, or high level when these bits are 1) for at least 1 cycle of the peripheral module clock (PCLK). Pin combinations for output comparison can be selected by registers of POE.
GTIOC1A and GTIOC1B	Output	
GTIOC2A and GTIOC2B	Output	

21.2 Register Descriptions

The POE registers are initialized by a reset.

21.2.1 Input Level Control/Status Register 1 (ICSR1)

Address(es): 0008 C4C0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	POE0F	—	—	—	PIE1	—	—	—	—	—	—	POE0M[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	POE0M[1:0]	POE0 Mode Select	b1 b0 0 0: Accepts a request on the falling edge of POE0# pin input. 0 1: Accepts a request when POE0# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a request when POE0# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a request when POE0# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	R/W*1
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	PIE1	Port Interrupt Enable 1	0: Interrupt requests disabled 1: Interrupt requests enabled	R/W
b11 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12	POE0F	POE0 Flag	0: Indicates that an output disabling request has not been input to the POE0# pin. 1: Indicates that an output disabling request has been input to the POE0# pin.	R/(W) *2
b15 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset.
Note 2. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

The ICSR1 register selects the POE0# pin input modes, controls the enable/disable of interrupts, and indicates status.

POE0M[1:0] Bits (POE0 Mode Select)

These bits select the input mode of the POE0# pin.

PIE1 Bit (Port Interrupt Enable 1)

This bit enables or disables interrupt requests when the POE0F flag is set to 1.

POE0F Flag (POE0 Flag)

This flag indicates that an output disabling request has been input to the POE0# pin.

[Setting condition]

- When the input set by the POE0M[1:0] bits occurs at the POE0# pin

[Clearing condition]

- By writing 0 to the POE0F flag after reading POE0F = 1
  When low-level sampling is set by the POE0M[1:0] bits, the high level needs to be input to the POE0# pin to write 0 to this flag.
  For details, refer to section 21.3.8, Recover from Output Disabled State.

21.2.2 Input Level Control/Status Register 2 (ICSR2)

Address(es): 0008 C4C4h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	POE4F	—	—	—	PIE2	—	—	—	—	—	—	POE4M[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	POE4M[1:0]	POE4 Mode Select	b1 b0 0 0: Accepts a request on the falling edge of POE4# pin input. 0 1: Accepts a request when POE4# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a request when POE4# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a request when POE4# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	R/W*1
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	PIE2	Port Interrupt Enable 2	0: Interrupt requests disabled 1: Interrupt requests enabled	R/W
b11 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12	POE4F	POE4 Flag	0: Indicates that an output disabling request has not been input to the POE4# pin. 1: Indicates that an output disabling request has been input to the POE4# pin.	R/(W) *2
b15 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset.
Note 2. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

The ICSR2 register selects the POE4# pin input mode, controls the enable/disable of interrupts, and indicates status.

POE4M[1:0] Bits (POE4 Mode Select)

These bits select the input mode of the POE4# pin.

PIE2 Bit (Port Interrupt Enable 2)

This bit enables or disables interrupt requests when the POE4F flag is set to 1.

POE4F Flag (POE4 Flag)

This flag indicates that an output disabling request has been input to the POE4# pin.
[Setting condition]

- When the input set by POE4M[1:0] occurs at the POE4# pin

[Clearing condition]

- By writing 0 to POE4F after reading POE4F = 1
  When low-level sampling is set by the POE4M[1:0] bits, the high level needs to be input to the POE4# pin to write 0 to this flag.
  For details, refer to section 21.3.8, Recover from Output Disabled State.

21.2.3 Input Level Control/Status Register 3 (ICSR3)

Address(es): 0008 C4C8h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	POE8F	—	—	POE8E	PIE3	—	—	—	—	—	—	POE8M[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	POE8M[1:0]	POE8 Mode Select	b1 b0 0 0: Accepts a request on the falling edge of POE8# pin input. 0 1: Accepts a request when POE8# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a request when POE8# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a request when POE8# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	R/W*1
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	PIE3	Port Interrupt Enable 3	0: Interrupt requests disabled 1: Interrupt requests enabled	R/W
b9	POE8E	POE8 Output Disable	0: Does not disable the output by POE8# signal. 1: Disable the output by POE8# signal.	R/W*1
b11, b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12	POE8F	POE8 Flag	0: Indicates that an output disabling request has not been input to the POE8# pin. 1: Indicates that an output disabling request has been input to the POE8# pin.	R/(W)*2
b15 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset.
Note 2. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

The ICSR3 register selects the POE8# pin input mode, controls the enable/disable of interrupts, and indicates status.

POE8M[1:0] Bits (POE8 Mode Select)

These bits select the input mode of the POE8# pin.

PIE3 Bit (Port Interrupt Enable 3)

This bit enables or disables interrupt requests when the POE8F flag is set to 1.

POE8E Bit (POE8 Output Disable)

This bit specifies whether to disable the output of the corresponding pin when the POE8F flag is set to 1.

POE8F Flag (POE8 Flag)

This flag indicates that an output disabling request has been input to the POE8# pin.

[Setting condition]

- When the input set by the POE8M[1:0] bits occurs at the POE8# pin

[Clearing condition]

- By writing 0 to the POE8F flag after reading POE8F = 1
  When low-level sampling is set by the POE8M[1:0] bits, the high level needs to be input to the POE8# pin to write 0 to this flag.
  For details, refer to section 21.3.8, Recover from Output Disabled State.

21.2.4 Input Level Control/Status Register 4 (ICSR4)

Address(es): 0008 C4D6h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	POE10F	—	—	POE10E	PIE4	—	—	—	—	—	—	POE10M[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	POE10M[1:0]	POE10 Mode Select	b1 b0 0 0: Accepts a request on the falling edge of POE10# pin input. 0 1: Accepts a request when POE10# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a request when POE10# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a request when POE10# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	R/W*1
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	PIE4	Port Interrupt Enable 4	0: Interrupt requests disabled 1: Interrupt requests enabled	R/W
b9	POE10E	POE10 Output Disable	0: Does not disable the output by POE10# signal. 1: Disable the output by POE10# signal.	R/W*1
b11, b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12	POE10F	POE10 Flag	0: Indicates that an output disabling request has not been input to the POE10# pin. 1: Indicates that an output disabling request has been input to the POE10# pin.	R/(W)*2
b15 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset.
Note 2. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

The ICSR4 register selects the POE10# pin input mode, controls the enable/disable of interrupts, and indicates status.

POE10M[1:0] Bits (POE10 Mode Select)

These bits select the input mode of the POE10# pin.

PIE4 Bit (Port Interrupt Enable 4)

This bit enables or disables interrupt requests when the POE10F flag is set to 1.

POE10E Bit (POE10 Output Disable)

This bit specifies whether to disable the output of the corresponding pin when the POE10F flag is set to 1.

POE10F Flag (POE10 Flag)

This flag indicates that an output disabling request has been input to the POE10# pin.

[Setting condition]

- When the input set by the POE10M[1:0] bits occurs at the POE10# pin

[Clearing condition]

- By writing 0 to the POE10F flag after reading POE10F = 1
  When low-level sampling is set by the POE10M[1:0] bits, the high level needs to be input to the POE10# pin to write 0 to this flag.
  For details, refer to section 21.3.8, Recover from Output Disabled State.

21.2.5 Input Level Control/Status Register 5 (ICSR5)

Address(es): 0008 C4D8h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	POE11F	—	—	POE11E	PIE5	—	—	—	—	—	—	POE11M[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	
b1, b0	POE11M[1:0]	POE11 Mode Select	b1 b0 0 0: Accepts a request on the falling edge of POE11# pin input. 0 1: Accepts a request when POE11# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a request when POE11# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a request when POE11# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	R/W*1
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	PIE5	Port Interrupt Enable 5	0: Interrupt requests disabled 1: Interrupt requests enabled	R/W
b9	POE11E	POE11 Output Disable	0: Does not disable the output by POE11# signal. 1: Disable the output by POE11# signal.	R/W*1
b11, b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12	POE11F	POE11 Flag	0: Indicates that an output disabling request has not been input to the POE11# pin. 1: Indicates that an output disabling request has been input to the POE11# pin.	R/(W)*2
b15 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset.
Note 2. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

The ICSR5 register selects the POE11# pin input mode, controls the enable/disable of interrupts, and indicates status.

POE11M[1:0] Bits (POE11 Mode Select)

These bits select the input mode of the POE11# pin.

PIE5 Bit (Port Interrupt Enable 5)

This bit enables or disables interrupt requests when the POE11F flag is set to 1.

POE11E Bit (POE11 Output Disable)

This bit specifies whether to disable the output of the corresponding pin when the POE11F flag is set to 1.

POE11F Flag (POE11 Flag)

This flag indicates that an output disabling request has been input to the POE11# pin.
[Setting condition]

- When the input set by the POE11M[1:0] bits occurs at the POE11# pin

[Clearing condition]

- By writing 0 to the POE11F flag after reading POE11F = 1
  When low-level sampling is set by the POE11M[1:0] bits, the high level needs to be input to the POE11# pin to write 0 to this flag.
  For details, refer to section 21.3.8, Recover from Output Disabled State.

21.2.6 Input Level Control/Status Register 6 (ICSR6)

Address(es): 0008 C4DCh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	OSTSTF	—	—	OSTSTE	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b8 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b9	OSTSTE	Oscillation Stop Output Disable	0: Does not disable the output when the oscillation stop is detected. 1: Disable the output when the oscillation stop is detected.	R/W*1
b11, b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12	OSTSTF	Oscillation Stop Detection Flag	0: Indicates that an output disabling request by oscillation stop has not been generated. 1: Indicates that an output disabling request by oscillation stop has been generated.	R/W*2
b15 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset.
Note 2. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

The ICSR6 register controls the oscillation stop high-impedance and indicates status.

OSTSTE Bit (Oscillation Stop Output Disable)

This bit specifies whether to disable the output of the target pin when oscillation stop is detected.

OSTSTF Flag (Oscillation Stop Detection Flag)

This flag indicates that an output disabling request by the oscillation stop has been generated.
When the main clock oscillation stops, this flag is set to 1. To clear this flag, wait for at least 10 cycles of PCLK after this flag becomes 1 and write 0 to this flag while the OSTDSR.OSTDF flag is 0. Writing 0 to this flag while the OSTDSR.OSTDF flag is 1 cannot clear this flag. After clearing this flag, confirm that the flag has actually been modified to 0.
[Setting condition]

- When oscillation stop is detected

[Clearing condition]

- By writing 0 to the OSTSTF flag after reading OSTSTF = 1

21.2.7 Input Level Control/Status Register 7 (ICSR7)

Address(es): 0008 C4E0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	POE12F	—	—	POE12E	PIE7	—	—	—	—	—	—	POE12M[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	
b1, b0	POE12M[1:0]	POE12 Mode Select	b1 b0 0 0: Accepts a request on the falling edge of POE12# pin input. 0 1: Accepts a request when POE12# pin input has been sampled 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a request when POE12# pin input has been sampled 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a request when POE12# pin input has been sampled 16 times at PCLK/128 clock pulses and all are low level.	R/W*1
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	PIE7	Port Interrupt Enable 7	0: Interrupt requests disabled 1: Interrupt requests enabled	R/W
b9	POE12E	POE12 Output Disable	0: Does not disable the output by POE12# signal. 1: Disable the output by POE12# signal.	R/W*1
b11, b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12	POE12F	POE12 Flag	0: Indicates that an output disabling request has not been input to the POE12# pin. 1: Indicates that an output disabling request has been input to the POE12# pin.	R/(W)*2
b15 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset.
Note 2. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

The ICSR7 register selects the POE12# pin input mode, controls the enable/disable of interrupts, and indicates status.

POE12M[1:0] Bits (POE12 Mode Select)

These bits select the input mode of the POE12# pin.

PIE7 Bit (Port Interrupt Enable 7)

This bit enables or disables interrupt requests when the POE12F flag is set to 1.

POE12E Bit (POE12 Output Disable)

This bit specifies whether to disable the output of the corresponding pin when the POE12F flag is set to 1.

POE12F Flag (POE12 Flag)

This flag indicates that an output disabling request has been input to the POE12# pin.
[Setting condition]

- When the input set by the POE12M[1:0] bits occurs at the POE12# pin

[Clearing condition]

- By writing 0 to the POE12F flag after reading POE12F = 1
  When low-level sampling is set by the POE12M[1:0] bits, the high level needs to be input to the POE12# pin to write 0 to this flag.
  For details, refer to section 21.3.8, Recover from Output Disabled State.

21.2.8 Output Level Control/Status Register 1 (OCSR1)

Address(es): 0008 C4C2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OSF1	—	—	—	—	—	OCE1	OIE1	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	OIE1	Simultaneous Conduction Interrupt Enable 1	0: Interrupt requests disabled 1: Interrupt requests enabled	R/W
b9	OCE1	Simultaneous Conduction Output Disable 1	0: Does not disable the outputs when they simultaneously go to an active level. 1: Disable the outputs when they simultaneously go to an active level.	R/W*1
b14 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	OSF1	Simultaneous Conduction Flag 1	0: Indicates that outputs have not simultaneously become an active level. 1: Indicates that outputs have simultaneously become an active level.	R/(W) *2

Note 1. Can be modified only once after a reset.
Note 2. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

The OCSR1 register controls the enable/disable of output-level comparison and interrupts, and indicates status.

OIE1 Bit (Simultaneous Conduction Interrupt Enable 1)

This bit enables or disables interrupt requests when the OSF1 flag is set to 1.

OCE1 Bit (Simultaneous Conduction Output Disable 1)

This bit specifies whether to disable the output of the target pin when the OSF1 flag is set to 1.

OSF1 Flag (Simultaneous Conduction Flag 1)

This flag indicates that at least one of the three pairs of two-phase output pins assigned to ports P71 to P76 for MTU complementary PWM output (MTU3 and MTU4) or GPT output (GPT0 to GPT2) has simultaneously become at the active level. If the output disabling control for the corresponding pins is not enabled, this flag does not become 1.
For setting the active level, refer to section 21.2.11, Active Level Setting Register 1 (ALR1).
[Setting condition]

- When the MTIOC3B/GTIOC0A (P71) and MTIOC3D/GTIOC0B (P74) pins simultaneously go to the active level*1 while the value of the POECR2.MTU3BDZE bit, or of either or both of the PMMCR1.MTU3BME and PMMCR1.MTU3DME bits, is 1.
- When the MTIOC4A/GTIOC1A (P72) and MTIOC4C/GTIOC1B (P75) pins simultaneously go to the active level*1 while the value of the POECR2.MTU4ACZE bit, or either or both of the PMMCR1.MTU4AME and PMMCR1.MTU4CME bits, is 1.
- When the MTIOC4B/GTIOC2A (P73) and MTIOC4D/GTIOC2B (P76) pins simultaneously go to the active level*1 while the value of the POECR2.MTU4BDZE bit, or either or both of the PMMCR1.MTU4BME and PMMCR1.MTU4DME bits, is 1.

Note 1. The setting condition is judged only by the level of the pin regardless the setting of the MPC.PmnPFS register.

[Clearing condition]

- By writing 0 to the OSF1 flag after reading OSF1 = 1

To write 0 to this flag, the inactive level needs to be output from MTU complementary PWM output pins or GPT output pins. For details, refer to section 21.3.8, Recover from Output Disabled State.

21.2.9 Output Level Control/Status Register 2 (OCSR2)

Address(es): 0008 C4C6h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OSF2	—	—	—	—	—	OCE2	OIE2	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	OIE2	Simultaneous Conduction Interrupt Enable 2	0: Interrupt requests disabled 1: Interrupt requests enabled	R/W
b9	OCE2	Simultaneous Conduction Output Disable 2	0: Does not disable the outputs when they simultaneously go to an active level. 1: Disable the outputs when they simultaneously go to an active level.	R/W*1
b14 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	OSF2	Simultaneous Conduction Flag 2	0: Indicates that outputs have not simultaneously become an active level. 1: Indicates that outputs have simultaneously become an active level.	R/(W)*2

Note 1. Can be modified only once after a reset.
Note 2. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

The OCSR2 register controls the enable/disable of output-level comparison and interrupts, and indicates status.

OIE2 Bit (Simultaneous Conduction Interrupt Enable 2)

This bit enables or disables interrupt requests when the OSF2 flag is set to 1.

OCE2 Bit (Simultaneous Conduction Output Disable 2)

This bit specifies whether to disable the output of the target pin when the OSF2 flag is set to 1.

OSF2 Flag (Simultaneous Conduction Flag 2)

This flag indicates that at least one of the three pairs of two-phase output pins for MTU complementary PWM output (MTU6 and MTU7) has simultaneously become an active level. If the output disabling control for the corresponding pins is not enabled, this flag does not become 1.

For setting the active level, refer to section 21.2.12, Active Level Setting Register 2 (ALR2).

[Setting condition]

- When the MTIOC6B and MTIOC6D pins simultaneously go to the active level*1 while the value of the POECR2.MTU6BDZE bit, or either or both of the PMMCR1.MTU6BME and PMMCR1.MTU6DME bits, is 1.
- When the MTIOC7A and MTIOC7C pins simultaneously go to the active level*1 while the value of the POECR2.MTU7ACZE bit, or either or both of the PMMCR1.MTU7AME and PMMCR1.MTU7CME bits, is 1.
- When the MTIOC7B and MTIOC7D pins simultaneously go to the active level*1 while the value of the

POECR2.MTU7BDZE bit, or either or both of the PMMCR1.MTU7BME and PMMCR1.MTU7DME bits, is 1.

Note 1. The setting condition is judged only by the level of the pin regardless the setting of the MPC.PmnPFS register.

[Clearing condition]

- By writing 0 to the OSF2 flag after reading OSF2 = 1

To write 0 to this flag, the inactive level needs to be output from MTU complementary PWM output pins. For details, refer to section 21.3.8, Recover from Output Disabled State.

21.2.10 Output Level Control/Status Register 3 (OCSR3)

Address(es): 0008 C4EAh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OSF3	—	—	—	—	—	OCE3	OIE3	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	OIE3	Simultaneous Conduction Interrupt Enable 3	0: Interrupt requests disabled 1: Interrupt requests enabled	R/W
b9	OCE3	Simultaneous Conduction Output Disable 3	0: Does not disable the outputs when they simultaneously go to an active level. 1: Disable the outputs when they simultaneously go to an active level.	R/W*1
b14 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	OSF3	Simultaneous Conduction Flag 3	0: Indicates that outputs have not simultaneously become an active level. 1: Indicates that outputs have simultaneously become an active level.	R/(W)*2

Note 1. Can be modified only once after a reset.
Note 2. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

The OCSR3 register controls the enable/disable of output-level comparison and interrupts, and indicates status.

OIE3 Bit (Simultaneous Conduction Interrupt Enable 3)

This bit enables or disables interrupt requests when the OSF3 flag is set to 1.

OCE3 Bit (Simultaneous Conduction Output Disable 3)

This bit specifies whether to disable the output of the target pin when the OSF3 flag is set to 1.

OSF3 Bit (Simultaneous Conduction Flag 3)

This flag indicates that at least one of the three pairs of two-phase output pins assigned to ports P12 to P17 for GPT output (GPT0 to GPT2) or MTU complementary PWM output (MTU3 and MTU4) has simultaneously become at the active level. If the output disabling control for the corresponding pins is not enabled, this flag does not become 1.
For setting the active level, refer to section 21.2.13, Active Level Setting Register 3 (ALR3).
[Setting condition]

- When the GTIOC0A/MTIOC3B (P12) and GTIOC0B/MTIOC3D (P15) pins simultaneously go to the active level*1

while the value of either or both of the POECR3.GPT0AZE and POECR3.GPT0BZE bits, or of either or both of the PMMCR2.GPT0AME and PMMCR2.GPT0BME bits, is 1.

- When the GTIOC1A/MTIOC4A (P13) and GTIOC1B/MTIOC4C (P16) pins simultaneously go to the active level*1 while the value of either or both of the POECR3.GPT1AZE and POECR3.GPT1BZE bits, or of either or both of the PMMCR2.GPT1AME and PMMCR2.GPT1BME bits, is 1.
- When the GTIOC2A/MTIOC4B (P14) and GTIOC2B/MTIOC4D (P17) pins simultaneously go to the active level*1 while the value of either or both of the POECR3.GPT2AZE and POECR3.GPT3BZE bits, or of either or both of the PMMCR2.GPT2AME and PMMCR2.GPT2BME bits, is 1.

Note 1. The setting condition is judged only by the level of the pin regardless the setting of the MPC.PmnPFS register.

[Clearing condition]

- By writing 0 to the OSF3 flag after reading OSF3 = 1

To write 0 to this flag, the inactive level needs to be output from MTU complementary PWM output pins or GPT output pins. For details, refer to section 21.3.8, Recover from Output Disabled State.

21.2.11 Active Level Setting Register 1 (ALR1)

Address(es): 0008 C4DAh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	OLSEN	—	OLSG2B	OLSG2A	OLSG1B	OLSG1A	OLSG0B	OLSG0A
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	OLSG0A	MTIOC3B/GTIOC0A (P71) Pin Active Level Setting	0: Active low 1: Active high	R/W*1
b1	OLSG0B	MTIOC3D/GTIOC0B (P74) Pin Active Level Setting	0: Active low 1: Active high	R/W*1
b2	OLSG1A	MTIOC4A/GTIOC1A (P72) Pin Active Level Setting	0: Active low 1: Active high	R/W*1
b3	OLSG1B	MTIOC4C/GTIOC1B (P75) Pin Active Level Setting	0: Active low 1: Active high	R/W*1
b4	OLSG2A	MTIOC4B/GTIOC2A (P73) Pin Active Level Setting	0: Active low 1: Active high	R/W*1
b5	OLSG2B	MTIOC4D/GTIOC2B (P76) Pin Active Level Setting	0: Active low 1: Active high	R/W*1
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	OLSEN	Active Level Setting Enable	0: Disabled 1: Enabled	R/W*1
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset.

The ALR1 register specifies the active levels of the MTU and GPT outputs assigned to ports P71 to P76 for detection of simultaneous conduction of those outputs as reflected in the OCSR1 register.

OLSG0A Bit (MTIOC3B/GTIOC0A (P71) Pin Active Level Setting)

This bit sets the active level of the MTIOC3B and GTIOC0A outputs on P71. Specifically, setting the OLSG0A bit to 0

sets the low level and to 1 sets the high level as the active level for detection of simultaneous conduction.

OLSG0B Bit (MTIOC3D/GTIOC0B (P74) Pin Active Level Setting)

This bit sets the active level of the MTIOC3D and GTIOC0B outputs on P74. Specifically, setting the OLSG0B bit to 0 sets the low level and to 1 sets the high level as the active level for detection of simultaneous conduction.

OLSG1A Bit (MTIOC4A/GTIOC1A (P72) Pin Active Level Setting)

This bit sets the active level of the MTIOC4A and GTIOC1A outputs on P72. Specifically, setting the OLSG1A bit to 0 sets the low level and to 1 sets the high level as the active level for detection of simultaneous conduction.

OLSG1B Bit (MTIOC4C/GTIOC1B (P75) Pin Active Level Setting)

This bit sets the active level of the MTIOC4C and GTIOC1B outputs on P75. Specifically, setting the OLSG1B bit to 0 sets the low level and to 1 sets the high level as the active level for detection of simultaneous conduction.

OLSG2A Bit (MTIOC4B/GTIOC2A (P73) Pin Active Level Setting)

This bit sets the active level of the MTIOC4B and GTIOC2A outputs on P73. Specifically, setting the OLSG2A bit to 0 sets the low level and to 1 sets the high level as the active level for detection of simultaneous conduction.

OLSG2B Bit (MTIOC4D/GTIOC2B (P76) Pin Active Level Setting)

This bit sets the active level of the MTIOC4D and GTIOC2B outputs on P76. Specifically, setting the OLSG2B bit to 0 sets the low level and to 1 sets the high level as the active level for detection of simultaneous conduction.

OLSEN Bit (Active Level Setting Enable)

This bit enables or disables of the active-level settings in the OLSGnm bits (n = 0 to 2; m = A, B). Clearing the OLSEN bit to 0 disables the OLSGnm bits, in which case the active levels of the MTU output are determined by the MTU.TOCR1j and MTU.TOCR2j registers (j = A, B). Setting the OLSEN bit to 1 enables the OLSGnm bits, in which case the active levels of the MTU output are as selected by the OLSGnm bits in this register.
Active levels for the GPT output can only be set when the OLSEN bit is 1. When simultaneous conduction detection is to be used on the GPT outputs, set the OLSEN bit to 1 and then use the OLSGnm bits to set the active levels for the GPT outputs.

21.2.12 Active Level Setting Register 2 (ALR2)

Address(es): 0008 C4DEh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	OLSEN	—	OLSG6B	OLSG6A	OLSG5B	OLSG5A	OLSG4B	OLSG4A
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	OLSG4A	MTIOC6B Pin Active Level Setting	0: Active low 1: Active high	R/W*1
b1	OLSG4B	MTIOC6D Pin Active Level Setting	0: Active low 1: Active high	R/W*1
b2	OLSG5A	MTIOC7A Pin Active Level Setting	0: Active low 1: Active high	R/W*1
b3	OLSG5B	MTIOC7C Pin Active Level Setting	0: Active low 1: Active high	R/W*1
b4	OLSG6A	MTIOC7B Pin Active Level Setting	0: Active low 1: Active high	R/W*1
b5	OLSG6B	MTIOC7D Pin Active Level Setting	0: Active low 1: Active high	R/W*1
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	OLSEN	Active Level Setting Enable	0: Disabled 1: Enabled	R/W*1
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset.

The ALR2 register specifies the active levels of the MTU outputs for detection of simultaneous conduction of those outputs as reflected in the OCSR2 register.

OLSG4A Bit (MTIOC6B Pin Active Level Setting)

This bit sets the active level of the MTIOC6B output. Specifically, setting the OLSG4A bit to 0 sets the low level and to 1 sets the high level as the active level for detection of simultaneous conduction.

OLSG4B Bit (MTIOC6D Pin Active Level Setting)

This bit sets the active level of the MTIOC6D output. Specifically, setting the OLSG4B bit to 0 sets the low level and to 1 sets the high level as the active level for detection of simultaneous conduction.

OLSG5A Bit (MTIOC7A Pin Active Level Setting)

This bit sets the active level of the MTIOC7A output. Specifically, setting the OLSG5A bit to 0 sets the low level and to 1 sets the high level as the active level for detection of simultaneous conduction.

OLSG5B Bit (MTIOC7C Pin Active Level Setting)

This bit sets the active level of the MTIOC7C output. Specifically, setting the OLSG5B bit to 0 sets the low level and to 1 sets the high level as the active level for detection of simultaneous conduction.

OLSG6A Bit (MTIOC7B Pin Active Level Setting)

This bit sets the active level of the MTIOC7B output. Specifically, setting the OLSG6A bit to 0 sets the low level and to 1 sets the high level as the active level for detection of simultaneous conduction.

OLSG6B Bit (MTIOC7D Pin Active Level Setting)

This bit sets the active level of the MTIOC7D output. Specifically, setting the OLSG6B bit to 0 sets the low level and to 1 sets the high level as the active level for detection of simultaneous conduction.

OLSEN Bit (Active Level Setting Enable)

This bit enables or disables the active-level settings in the OLSGnm bits (n = 4 to 6; m = A, B). Clearing the OLSEN bit to 0 disables the OLSGnm bits, in which case the active levels of the MTU output are determined by the registers MTU.TOCR1j and MTU.TOCR2j (j = A, B). Setting the OLSEN bit to 1 enables the OLSGnm bits, in which case the active levels of the MTU output are as selected by the OLSGnm bits in this register.

21.2.13 Active Level Setting Register 3 (ALR3)

Address(es): 0008 C4ECh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	OLSEN	—	OLSG2B	OLSG2A	OLSG1B	OLSG1A	OLSG0B	OLSG0A
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	OLSG0A	MTIOC3B/GTIOC0A (P12) Pin Active Level Setting	0: Active low 1: Active high	R/W*1
b1	OLSG0B	MTIOC3D/GTIOC0B (P15) Pin Active Level Setting	0: Active low 1: Active high	R/W*1
b2	OLSG1A	MTIOC4A/GTIOC1A (P13) Pin Active Level Setting	0: Active low 1: Active high	R/W*1
b3	OLSG1B	MTIOC4C/GTIOC1B (P16) Pin Active Level Setting	0: Active low 1: Active high	R/W*1
b4	OLSG2A	MTIOC4B/GTIOC2A (P14) Pin Active Level Setting	0: Active low 1: Active high	R/W*1
b5	OLSG2B	MTIOC4D/GTIOC2B (P17) Pin Active Level Setting	0: Active low 1: Active high	R/W*1
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	OLSEN	Active Level Setting Enable	0: Disabled 1: Enabled	R/W*1
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset.

The ALR3 register specifies the active levels of the MTU and GPT outputs assigned to ports P12 to P17 for detection of simultaneous conduction of those outputs as reflected in the OCSR3 register.

OLSG0A Bit (MTIOC3B/GTIOC0A (P12) Pin Active Level Setting)

This bit sets the active level of the MTIOC3B and GTIOC0A outputs on P12. Specifically, setting the OLSG0A bit to 0 sets the low level and to 1 sets the high level as the active level for detection of simultaneous conduction.

OLSG0B Bit (MTIOC3D/GTIOC0B (P15) Pin Active Level Setting)

This bit sets the active level of the MTIOC3D and GTIOC0B outputs on P15. Specifically, setting the OLSG0B bit to 0 sets the low level and to 1 sets the high level as the active level for detection of simultaneous conduction.

OLSG1A Bit (MTIOC4A/GTIOC1A (P13) Pin Active Level Setting)

This bit sets the active level of the MTIOC4A and GTIOC1A outputs on P13. Specifically, setting the OLSG1A bit to 0 sets the low level and to 1 sets the high level as the active level for detection of simultaneous conduction.

OLSG1B Bit (MTIOC4C/GTIOC1B (P16) Pin Active Level Setting)

This bit sets the active level of the MTIOC4C and GTIOC1B outputs on P16. Specifically, setting the OLSG1B bit to 0 sets the low level and to 1 sets the high level as the active level for detection of simultaneous conduction.

OLSG2A Bit (MTIOC4B/GTIOC2A (P14) Pin Active Level Setting)

This bit sets the active level of the MTIOC4B and GTIOC2A outputs on P14. Specifically, setting the OLSG2A bit to 0 sets the low level and to 1 sets the high level as the active level for detection of simultaneous conduction.

OLSG2B Bit (MTIOC4D/GTIOC2B (P17) Pin Active Level Setting)

This bit sets the active level of the MTIOC4D and GTIOC2B outputs on P17. Specifically, setting the OLSG2B bit to 0 sets the low level and to 1 sets the high level as the active level for detection of simultaneous conduction.

OLSEN Bit (Active Level Setting Enable)

This bit enables or disables of the active-level settings in the OLSGnm bits (n = 0 to 2; m = A, B). Clearing the OLSEN bit to 0 disables the OLSGnm bits, in which case the active levels of the MTU output are determined by the MTU.TOCR1j and MTU.TOCR2j registers (j = A, B). Setting the OLSEN bit to 1 enables the OLSGnm bits, in which case the active levels of the MTU output are as selected by the OLSGnm bits in this register.
Active levels for the GPT output can only be set when the OLSEN bit is 1. When simultaneous conduction detection is to be used on the GPT outputs, set the OLSEN bit to 1 and then use the OLSGnm bits to set the active levels for the GPT outputs.

21.2.14 Software Port Output Enable Register (SPOER)

Address(es): 0008 C4CAh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	MTUCH9HIZ	—	GPT03HIZ	GPT02HIZ	MTUCH0HIZ	MTUCH67HIZ	MTUCH34HIZ
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	MTUCH34HIZ	MTU3 and MTU4 or GPT0 to GPT2 Pin Output Disable	0: Does not disable the outputs. 1: Disable the outputs.	R/W
b1	MTUCH67HIZ	MTU6 and MTU7 Pin Output Disable	0: Does not disable the output. 1: Disable the output.	R/W
b2	MTUCH0HIZ	MTU0 Pin Output Disable	0: Does not disable the outputs. 1: Disable the outputs.	R/W
b3	GPT02HIZ	GPT0 to GPT2 or MTU3 and MTU4 Pin Output Disable	0: Does not disable the output. 1: Disable the output.	R/W
b4	GPT03HIZ	GPT0 to GPT3 Pin Output Disable	0: Does not disable the output. 1: Disable the output.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	MTUCH9HIZ	MTU9 Pin Output Disable	0: Does not disable the output. 1: Disable the output.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

The SPOER register is used to disable the outputs of the corresponding pins.

MTUCH34HIZ Bit (MTU3 and MTU4 or GPT0 to GPT2 Pin Output Disable)

This bit specifies whether to disable the outputs of the MTU complementary PWM output pins (MTIOC3B, MTIOC3D, MTIOC4A, MTIOC4B, MTIOC4C, and MTIOC4D) or the GPT output pins (GTIOC0A, GTIOC0B, GTIOC1A, GTIOC1B, GTIOC2A, and GTIOC2B) of P71 to P76.

[Setting condition]

- By writing 1 to the MTUCH34HIZ bit

[Clearing conditions]

- Reset
- By writing 0 to the MTUCH34HIZ bit after reading MTUCH34HIZ = 1

MTUCH67HIZ Bit (MTU6 and MTU7 Pin Output Disable)

This bit specifies whether to disable the outputs of the MTU complementary PWM output pins (MTIOC6B, MTIOC6D, MTIOC7A, MTIOC7B, MTIOC7C, and MTIOC7D).

[Setting condition]

- By writing 1 to the MTUCH67HIZ bit

[Clearing conditions]

- Reset
- By writing 0 to the MTUCH67HIZ bit after reading MTUCH67HIZ = 1

MTUCH0HIZ Bit (MTU0 Pin Output Disable)

This bit specifies whether to disable the outputs of the MTU0 pins.

[Setting condition]

- By writing 1 to the MTUCH0HIZ bit

[Clearing conditions]

- Reset
- By writing 0 to the MTUCH0HIZ bit after reading MTUCH0HIZ = 1

GPT02HIZ Bit (GPT0 to GPT2 or MTU3 and MTU4 Pin Output Disable)

This bit specifies whether to disable the outputs of the GPT0 to GPT2 pins (GTIOC0A, GTIOC0B, GTIOC1A, GTIOC1B, GTIOC2A, and GTIOC2B) or MTU complementary PWM output pins (MTIOC3B, MTIOC3D, MTIOC4A, MTIOC4B, MTIOC4C, and MTIOC4D) of P12 to P17.

[Setting condition]

- By writing 1 to the GPT02HIZ bit

[Clearing conditions]

- Reset
- By writing 0 to the GPT02HIZ bit after reading GPT02HIZ = 1

GPT03HIZ Bit (GPT0 to GPT3 Pin Output Disable)

This bit specifies whether to disable the outputs of the GPT0 to GPT3 pins (GTIOC0A, GTIOC0B, GTIOC1A, GTIOC1B, GTIOC2A, GTIOC2B, GTIOC3A, and GTIOC3B) of PB5 to PB7, PD0 to PD2, PD6, and PD7.

[Setting condition]

- By writing 1 to the GPT03HIZ bit

[Clearing conditions]

- Reset
- By writing 0 to the GPT03HIZ bit after reading GPT03HIZ = 1

MTUCH9HIZ Bit (MTU9 Pin Output Disable)

This bit specifies whether to disable the outputs of the MTU9 pins.

[Setting condition]

- By writing 1 to the MTUCH9HIZ bit

[Clearing conditions]

- Reset
- By writing 0 to the MTUCH9HIZ bit after reading MTUCH9HIZ = 1

21.2.15 Port Output Enable Control Register 1 (POECR1)

Address(es): 0008 C4CBh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	MTU0B1ZE	MTU0A1ZE	MTU0DZE	MTU0CZE	MTU0BZE	MTU0AZE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	MTU0AZE	MTIOC0A (PB3) Pin High-Impedance Enable	0: Does not switch the pin to high-impedance state. 1: Switch the pin to high-impedance state.	R/W*1
b1	MTU0BZE	MTIOC0B (PB2) Pin High-Impedance Enable	0: Does not switch the pin to high-impedance state. 1: Switch the pin to high-impedance state.	R/W*1
b2	MTU0CZE	MTIOC0C Pin High-Impedance Enable	0: Does not switch the pin to high-impedance state. 1: Switch the pin to high-impedance state.	R/W*1
b3	MTU0DZE	MTIOC0D Pin High-Impedance Enable	0: Does not switch the pin to high-impedance state. 1: Switch the pin to high-impedance state.	R/W*1
b4	MTU0A1ZE	MTIOC0A (P31) Pin High-Impedance Enable	0: Does not switch the pin to high-impedance state. 1: Switch the pin to high-impedance state.	R/W*1
b5	MTU0B1ZE	MTIOC0B (P30) Pin High-Impedance Enable	0: Does not switch the pin to high-impedance state. 1: Switch the pin to high-impedance state.	R/W*1
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset.

The POECR1 register controls high-impedance state of the MTU0 pins.

MTU0AZE Bit (MTIOC0A (PB3) Pin High-Impedance Enable)

This bit specifies whether to switch the MTIOC0A output of PB3 to the high-impedance state when any of the ICSR3.POE8F flag, SPOER.MTUCH0HIZ bit, and ICSR6.OSTSTF flag (when the OSTSTE bit is 1), or, as additionally specified in the POECR5 register, the ICSRn.POEmF flag (n = 1, 2, 4, 5, 7; m = 0, 4, 10, 11, 12), or POECMPFR.CnFLAG flag (n = 0 to 3), is set to 1.
Set the PMMCR0.MTU0AME bit to 0 when setting this bit to 1.

MTU0BZE Bit (MTIOC0B (PB2) Pin High-Impedance Enable)

This bit specifies whether to switch the MTIOC0B output of PB2 to the high-impedance state when any of the ICSR3.POE8F flag, SPOER.MTUCH0HIZ bit, and ICSR6.OSTSTF flag (when the OSTSTE bit is 1), or, as additionally specified in the POECR5 register, the ICSRn.POEmF flag (n = 1, 2, 4, 5, 7; m = 0, 4, 10, 11, 12), or POECMPFR.CnFLAG flag (n = 0 to 3), is set to 1.
Set the PMMCR0.MTU0BME bit to 0 when setting this bit to 1.

MTU0CZE Bit (MTIOC0C Pin High-Impedance Enable)

This bit specifies whether to switch the MTIOC0C output to the high-impedance state when any of the ICSR3.POE8F flag, SPOER.MTUCH0HIZ bit, and ICSR6.OSTSTF flag (when the OSTSTE bit is 1), or, as additionally specified in the POECR5 register, the ICSRn.POEmF flag (n = 1, 2, 4, 5, 7; m = 0, 4, 10, 11, 12), or POECMPFR.CnFLAG flag (n = 0 to 3), is set to 1.
Set the PMMCR0.MTU0CME bit to 0 when setting this bit to 1.

MTU0DZE Bit (MTIOC0D Pin High-Impedance Enable)

This bit specifies whether to switch the MTIOC0D output to the high-impedance state when any of the ICSR3.POE8F flag, SPOER.MTUCH0HIZ bit, and ICSR6.OSTSTF flag (when the OSTSTE bit is 1), or, as additionally specified in the

POECR5 register, the ICSRn.POEmF flag (n = 1, 2, 4, 5, 7; m = 0, 4, 10, 11, 12), or POECMPFR.CnFLAG flag (n = 0 to 3), is set to 1.
Set the PMMCR0.MTU0DME bit to 0 when setting this bit to 1.

MTU0A1ZE Bit (MTIOC0A (P31) Pin High-Impedance Enable)

This bit specifies whether to switch the MTIOC0A output of P31 to the high-impedance state when any of the ICSR3.POE8F flag, SPOER.MTUCH0HIZ bit, and ICSR6.OSTSTF flag (when the OSTSTE bit is 1), or, as additionally specified in the POECR5 register, the ICSRn.POEmF flag (n = 1, 2, 4, 5, 7; m = 0, 4, 10, 11, 12), or POECMPFR.CnFLAG flag (n = 0 to 3), is set to 1.
Set the PMMCR0.MTU0A1ME bit to 0 when setting this bit to 1.

MTU0B1ZE Bit (MTIOC0B (P30) Pin High-Impedance Enable)

This bit specifies whether to switch the MTIOC0B output of P30 to the high-impedance state when any of the ICSR3.POE8F flag, SPOER.MTUCH0HIZ bit, and ICSR6.OSTSTF flag (when the OSTSTE bit is 1), or, as additionally specified in the POECR5 register, the ICSRn.POEmF flag (n = 1, 2, 4, 5, 7; m = 0, 4, 10, 11, 12), or POECMPFR.CnFLAG flag (n = 0 to 3), is set to 1.
Set the PMMCR0.MTU0B1ME bit to 0 when setting this bit to 1.

21.2.16 Port Output Enable Control Register 2 (POECR2)

Address(es): 0008 C4CCh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	MTU3BDZE	MTU4ACZE	MTU4BDZE	—	—	—	—	—	MTU6BDZE	MTU7ACZE	MTU7BDZE
Value after reset:	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b0	MTU7BDZE	MTIOC7B/MTIOC7D Pin High-Impedance Enable*2	0: Does not switch the pins to high-impedance state. 1: Switch the pins to high-impedance state.	R/W*1
b1	MTU7ACZE	MTIOC7A/MTIOC7C Pin High-Impedance Enable*2	0: Does not switch the pins to high-impedance state. 1: Switch the pins to high-impedance state.	R/W*1
b2	MTU6BDZE	MTIOC6B/MTIOC6D Pin High-Impedance Enable*2	0: Does not switch the pins to high-impedance state. 1: Switch the pins to high-impedance state.	R/W*1
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	MTU4BDZE	MTIOC4B/MTIOC4D (P73/P76) Pin High-Impedance Enable	0: Does not switch the pins to high-impedance state. 1: Switch the pins to high-impedance state.	R/W*1
b9	MTU4ACZE	MTIOC4A/MTIOC4C (P72/P75) Pin High-Impedance Enable	0: Does not switch the pins to high-impedance state. 1: Switch the pins to high-impedance state.	R/W*1
b10	MTU3BDZE	MTIOC3B/MTIOC3D (P71/P74) Pin High-Impedance Enable	0: Does not switch the pins to high-impedance state. 1: Switch the pins to high-impedance state.	R/W*1
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset.
Note 2. Set this bit to 0 when MTU6 or MTU7 is not used.

The POECR2 register controls high-impedance state of the MTU complementary PWM output pins (MTU3, MTU4, MTU6, and MTU7 pins) or the GPT output pins (GPT0 to GPT2 pins).

MTU7BDZE Bit (MTIOC7B/MTIOC7D Pin High-Impedance Enable)

This bit specifies whether to switch the MTIOC7B output and MTIOC7D output to the high-impedance state when at least one of the OCSR2.OSF2 flag, ICSR2.POE4F flag, SPOER.MTUCH67HIZ bit, ICSR6.OSTSTF flag (when the OSTSTE bit is 1), or, as additionally specified in the POECR4 register, the ICSRn.POEmF flag (n = 1, 3 to 5, 7; m = 0, 8, 10, 11, 12), or POECMPFR.CnFLAG flag (n = 0 to 3) is set to 1.
Set the PMMCR1.MTU7BME and PMMCR1.MTU7DME bits to 0 when setting this bit to 1.

MTU7ACZE Bit (MTIOC7A/MTIOC7C Pin High-Impedance Enable)

This bit specifies whether to switch the MTIOC7A output and MTIOC7C output to the high-impedance state when at least one of the OCSR2.OSF2 flag, ICSR2.POE4F flag, SPOER.MTUCH67HIZ bit, ICSR6.OSTSTF flag (when the OSTSTE bit is 1), or, as additionally specified in the POECR4 register, the ICSRn.POEmF flag (n = 1, 3 to 5, 7; m = 0, 8, 10, 11, 12), or POECMPFR.CnFLAG flag (n = 0 to 3) is set to 1.
Set the PMMCR1.MTU7AME and PMMCR1.MTU7CME bits to 0 when setting this bit to 1.

MTU6BDZE Bit (MTIOC6B/MTIOC6D Pin High-Impedance Enable)

This bit specifies whether to switch the MTIOC6B output and MTIOC6D output to the high-impedance state when at least one of the OCSR2.OSF2 flag, ICSR2.POE4F flag, SPOER.MTUCH67HIZ bit, ICSR6.OSTSTF flag (when the OSTSTE bit is 1), or, as additionally specified in the POECR4 register, the ICSRn.POEmF flag (n = 1, 3 to 5, 7; m = 0, 8, 10, 11, 12), or POECMPFR.CnFLAG flag (n = 0 to 3) is set to 1.
Set the PMMCR1.MTU6BME and PMMCR1.MTU6DME bits to 0 when setting this bit to 1.

MTU4BDZE Bit (MTIOC4B/MTIOC4D (P73/P76) Pin High-Impedance Enable)

This bit specifies whether to switch the MTIOC4B/GTIOC2A output of P73 and MTIOC4D/GTIOC2B output of P76 to the high-impedance state when at least one of the OCSR1.OSF1 flag, ICSR1.POE0F flag, SPOER.MTUCH34HIZ bit, ICSR6.OSTSTF flag (when the OSTSTE bit is 1), or, as additionally specified in the POECR4 register, the ICSRn.POEmF flag (n = 2 to 5, 7; m = 4, 8, 10, 11, 12), or POECMPFR.CnFLAG flag (n = 0 to 3) is set to 1.
Set the PMMCR1.MTU4BME and PMMCR1.MTU4DME bits to 0 when setting this bit to 1.

MTU4ACZE Bit (MTIOC4A/MTIOC4C (P72/P75) Pin High-Impedance Enable)

This bit specifies whether to switch the MTIOC4A/GTIOC1A output of P72 and MTIOC4C/GTIOC1B output of P75 to the high-impedance state when at least one of the OCSR1.OSF1 flag, ICSR1.POE0F flag, SPOER.MTUCH34HIZ bit, ICSR6.OSTSTF flag (when the OSTSTE bit is 1), or, as additionally specified in the POECR4 register, the ICSRn.POEmF flag (n = 2 to 5, 7; m = 4, 8, 10, 11, 12), or POECMPFR.CnFLAG flag (n = 0 to 3) is set to 1.
Set the PMMCR1.MTU4AME and PMMCR1.MTU4CME bits to 0 when setting this bit to 1.

MTU3BDZE Bit (MTIOC3B/MTIOC3D (P71/P74) Pin High-Impedance Enable)

This bit specifies whether to switch the MTIOC3B/GTIOC0A output of P71 and MTIOC3D/GTIOC0B output of P74 to the high-impedance state when at least one of the OCSR1.OSF1 flag, ICSR1.POE0F flag, SPOER.MTUCH34HIZ bit, ICSR6.OSTSTF flag (when the OSTSTE bit is 1), or, as additionally specified in the POECR4 register, the ICSRn.POEmF flag (n = 2 to 5, 7; m = 4, 8, 10, 11, 12), or POECMPFR.CnFLAG flag (n = 0 to 3) is set to 1.
Set the PMMCR1.MTU3BME and PMMCR1.MTU3DME bits to 0 when setting this bit to 1.

21.2.17 Port Output Enable Control Register 3 (POECR3)

Address(es): 0008 C4CEh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	GPT3B1ZE	GPT3A1ZE	GPT2B1ZE	GPT2A1ZE	GPT1B1ZE	GPT1A1ZE	GPT0B1ZE	GPT0A1ZE	—	—	GPT2BZE	GPT2AZE	GPT1BZE	GPT1AZE	GPT0BZE	GPT0AZE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	GPT0AZE	GTIOC0A (P12) Pin High-Impedance Enable	0: Does not switch the pin to high-impedance state. 1: Switch the pin to high-impedance state.	R/W*1
b1	GPT0BZE	GTIOC0B (P15) Pin High-Impedance Enable	0: Does not switch the pin to high-impedance state. 1: Switch the pin to high-impedance state.	R/W*1
b2	GPT1AZE	GTIOC1A (P13) Pin High-Impedance Enable	0: Does not switch the pin to high-impedance state. 1: Switch the pin to high-impedance state.	R/W*1
b3	GPT1BZE	GTIOC1B (P16) Pin High-Impedance Enable	0: Does not switch the pin to high-impedance state. 1: Switch the pin to high-impedance state.	R/W*1
b4	GPT2AZE	GTIOC2A (P14) Pin High-Impedance Enable	0: Does not switch the pin to high-impedance state. 1: Switch the pin to high-impedance state.	R/W*1
b5	GPT2BZE	GTIOC2B (P17) Pin High-Impedance Enable	0: Does not switch the pin to high-impedance state. 1: Switch the pin to high-impedance state.	R/W*1
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	GPT0A1ZE	GTIOC0A (PD2) Pin High-Impedance Enable	0: Does not switch the pin to high-impedance state. 1: Switch the pin to high-impedance state.	R/W*1
b9	GPT0B1ZE	GTIOC0B (PD1) Pin High-Impedance Enable	0: Does not switch the pin to high-impedance state. 1: Switch the pin to high-impedance state.	R/W*1
b10	GPT1A1ZE	GTIOC1A (PD0) Pin High-Impedance Enable	0: Does not switch the pin to high-impedance state. 1: Switch the pin to high-impedance state.	R/W*1
b11	GPT1B1ZE	GTIOC1B (PB7) Pin High-Impedance Enable	0: Does not switch the pin to high-impedance state. 1: Switch the pin to high-impedance state.	R/W*1
b12	GPT2A1ZE	GTIOC2A (PB6) Pin High-Impedance Enable	0: Does not switch the pin to high-impedance state. 1: Switch the pin to high-impedance state.	R/W*1
b13	GPT2B1ZE	GTIOC2B (PB5) Pin High-Impedance Enable	0: Does not switch the pin to high-impedance state. 1: Switch the pin to high-impedance state.	R/W*1
b14	GPT3A1ZE	GTIOC3A High-Impedance Enable	0: Does not switch the pin to high-impedance state. 1: Switch the pin to high-impedance state.	R/W*1
b15	GPT3B1ZE	GTIOC3B High-Impedance Enable	0: Does not switch the pin to high-impedance state. 1: Switch the pin to high-impedance state.	R/W*1

Note 1. Can be modified only once after a reset.

The POECR3 register controls high-impedance state of the GPT pins (GPT0 to GPT3) and the MTU complementary PWM output pins (MTU3 and MTU4).

GPT0AZE Bit (GTIOC0A (P12) Pin High-Impedance Enable)

This bit specifies whether to switch the GTIOC0A and MTIOC3B outputs of P12 to the high-impedance state when at least one of the OCSR3.OSF3 flag, ICSR4.POE10F flag, SPOER.GPT02HIZ bit, ICSR6.OSTSTF flag (when the OSTSTE bit is 1), or, as additionally specified in the POECR6 register, the ICSRn.POEmF flag (n = 1 to 3, 5, 7; m = 0, 4, 8, 11, 12), is set to 1.

Set the PMMCR2.GPT0AME bit to 0 when setting this bit to 1.

GPT0BZE Bit (GTIOC0B (P15) Pin High-Impedance Enable)

This bit specifies whether to switch the GTIOC0B and MTIOC3D outputs of P15 to the high-impedance state when at

least one of the OCSR3.OSF3 flag, ICSR4.POE10F flag, SPOER.GPT02HIZ bit, ICSR6.OSTSTF flag (when the OSTSTE bit is 1), or, as additionally specified in the POECR6 register, the ICSRn.POEmF flag (n = 1 to 3, 5, 7; m = 0, 4, 8, 11, 12), is set to 1.
Set the PMMCR2.GPT0BME bit to 0 when setting this bit to 1.

GPT1AZE Bit (GTIOC1A (P13) Pin High-Impedance Enable)

This bit specifies whether to switch the GTIOC1A and MTIOC4A outputs of P13 to the high-impedance state when at least one of the OCSR3.OSF3 flag, ICSR4.POE10F flag, SPOER.GPT02HIZ bit, ICSR6.OSTSTF flag (when the OSTSTE bit is 1), or, as additionally specified in the POECR6 register, the ICSRn.POEmF flag (n = 1 to 3, 5, 7; m = 0, 4, 8, 11, 12), is set to 1.
Set the PMMCR2.GPT1AME bit to 0 when setting this bit to 1.

GPT1BZE Bit (GTIOC1B (P16) Pin High-Impedance Enable)

This bit specifies whether to switch the GTIOC1B and MTIOC4C outputs of P16 to the high-impedance state when at least one of the OCSR3.OSF3 flag, ICSR4.POE10F flag, SPOER.GPT02HIZ bit, ICSR6.OSTSTF flag (when the OSTSTE bit is 1), or, as additionally specified in the POECR6 register, the ICSRn.POEmF flag (n = 1 to 3, 5, 7; m = 0, 4, 8, 11, 12), is set to 1.
Set the PMMCR2.GPT1BME bit to 0 when setting this bit to 1.

GPT2AZE Bit (GTIOC2A (P14) Pin High-Impedance Enable)

This bit specifies whether to switch the GTIOC2A and MTIOC4B outputs of P14 to the high-impedance state when at least one of the OCSR3.OSF3 flag, ICSR4.POE10F flag, SPOER.GPT02HIZ bit, ICSR6.OSTSTF flag (when the OSTSTE bit is 1), or, as additionally specified in the POECR6 register, the ICSRn.POEmF flag (n = 1 to 3, 5, 7; m = 0, 4, 8, 11, 12), is set to 1.
Set the PMMCR2.GPT2AME bit to 0 when setting this bit to 1.

GPT2BZE Bit (GTIOC2B (P17) Pin High-Impedance Enable)

This bit specifies whether to switch the GTIOC2B and MTIOC4D outputs of P17 to the high-impedance state when at least one of the OCSR3.OSF3 flag, ICSR4.POE10F flag, SPOER.GPT02HIZ bit, ICSR6.OSTSTF flag (when the OSTSTE bit is 1), or, as additionally specified in the POECR6 register, the ICSRn.POEmF flag (n = 1 to 3, 5, 7; m = 0, 4, 8, 11, 12), is set to 1.
Set the PMMCR2.GPT2BME bit to 0 when setting this bit to 1.

GPT0A1ZE Bit (GTIOC0A (PD2) Pin High-Impedance Enable)

This bit specifies whether to switch the GTIOC0A outputs of PD2 to the high-impedance state when at least one of the ICSR5.POE11F flag, SPOER.GPT03HIZ bit, ICSR6.OSTSTF flag (when the OSTSTE bit is 1), or, as additionally specified in the POECR6 register, the ICSRn.POEmF flag (n = 1 to 4, 7; m = 0, 4, 8, 10, 12), is set to 1.
Set the PMMCR2.GPT0A1ME bit to 0 when setting this bit to 1.

GPT0B1ZE Bit (GTIOC0B (PD1) Pin High-Impedance Enable)

This bit specifies whether to switch the GTIOC0B outputs of PD1 to the high-impedance state when at least one of the ICSR5.POE11F flag, SPOER.GPT03HIZ bit, ICSR6.OSTSTF flag (when the OSTSTE bit is 1), or, as additionally specified in the POECR6 register, the ICSRn.POEmF flag (n = 1 to 4, 7; m = 0, 4, 8, 10, 12), is set to 1.
Set the PMMCR2.GPT0B1ME bit to 0 when setting this bit to 1.

GPT1A1ZE Bit (GTIOC1A (PD0) Pin High-Impedance Enable)

This bit specifies whether to switch the GTIOC1A outputs of PD0 to the high-impedance state when at least one of the ICSR5.POE11F flag, SPOER.GPT03HIZ bit, ICSR6.OSTSTF flag (when the OSTSTE bit is 1), or, as additionally specified in the POECR6 register, the ICSRn.POEmF flag (n = 1 to 4, 7; m = 0, 4, 8, 10, 12), is set to 1.

Set the PMMCR2.GPT1A1ME bit to 0 when setting this bit to 1.

GPT1B1ZE Bit (GTIOC1B (PB7) Pin High-Impedance Enable)

This bit specifies whether to switch the GTIOC1B outputs of PB7 to the high-impedance state when at least one of the ICSR5.POE11F flag, SPOER.GPT03HIZ bit, ICSR6.OSTSTF flag (when the OSTSTE bit is 1), or, as additionally specified in the POECR6 register, the ICSRn.POEmF flag (n = 1 to 4, 7; m = 0, 4, 8, 10, 12), is set to 1.
Set the PMMCR2.GPT1B1ME bit to 0 when setting this bit to 1.

GPT2A1ZE Bit (GTIOC2A (PB6) Pin High-Impedance Enable)

This bit specifies whether to switch the GTIOC2A outputs of PB6 to the high-impedance state when at least one of the ICSR5.POE11F flag, SPOER.GPT03HIZ bit, ICSR6.OSTSTF flag (when the OSTSTE bit is 1), or, as additionally specified in the POECR6 register, the ICSRn.POEmF flag (n = 1 to 4, 7; m = 0, 4, 8, 10, 12), is set to 1.
Set the PMMCR2.GPT2A1ME bit to 0 when setting this bit to 1.

GPT2B1ZE Bit (GTIOC2B (PB5) Pin High-Impedance Enable)

This bit specifies whether to switch the GTIOC2B outputs of PB5 to the high-impedance state when at least one of the ICSR5.POE11F flag, SPOER.GPT03HIZ bit, ICSR6.OSTSTF flag (when the OSTSTE bit is 1), or, as additionally specified in the POECR6 register, the ICSRn.POEmF flag (n = 1 to 4, 7; m = 0, 4, 8, 10, 12), is set to 1.
Set the PMMCR2.GPT2B1ME bit to 0 when setting this bit to 1.

GPT3A1ZE Bit (GTIOC3A High-Impedance Enable)

This bit specifies whether to switch the GTIOC3A outputs to the high-impedance state when at least one of the ICSR5.POE11F flag, SPOER.GPT03HIZ bit, ICSR6.OSTSTF flag (when the OSTSTE bit is 1), or, as additionally specified in the POECR6 register, the ICSRn.POEmF flag (n = 1 to 4, 7; m = 0, 4, 8, 10, 12), is set to 1.
Set the PMMCR2.GPT3A1ME bit to 0 when setting this bit to 1.

GPT3B1ZE Bit (GTIOC3B High-Impedance Enable)

This bit specifies whether to switch the GTIOC3B outputs to the high-impedance state when at least one of the ICSR5.POE11F flag, SPOER.GPT03HIZ bit, ICSR6.OSTSTF flag (when the OSTSTE bit is 1), or, as additionally specified in the POECR6 register, the ICSRn.POEmF flag (n = 1 to 4, 7; m = 0, 4, 8, 10, 12), is set to 1.
Set the PMMCR2.GPT3B1ME bit to 0 when setting this bit to 1.

21.2.18 Port Output Enable Control Register 4 (POECR4)

Address(es): 0008 C4D0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	IC6ADDMT67ZE	IC5ADDMT67ZE	IC4ADDMT67ZE	IC3ADDMT67ZE	—	IC1ADDMT67ZE	CMADDMT67ZE	—	IC6ADDMT34ZE	IC5ADDMT34ZE	IC4ADDMT34ZE	IC3ADDMT34ZE	IC2ADDMT34ZE	—	CMADDMT34ZE
Value after reset:	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0

Bit	Symbol	Bit Name	Description	R/W
b0	CMADDMT34ZE	MTU3 and MTU4 Output Disabling Condition CFLAG Add	0: Does not add the flags to the conditions to disable the output. 1: Adds the flags to the conditions to disable the output.	R/W*1
b1	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b2	IC2ADDMT34ZE	MTU3 and MTU4 Output Disabling Condition POE4F Add	0: Does not add the flag to the conditions to disable the output. 1: Adds the flag to the conditions to disable the output.	R/W*1
b3	IC3ADDMT34ZE	MTU3 and MTU4 Output Disabling Condition POE8F Add	0: Does not add the flag to the conditions to disable the output. 1: Adds the flag to the conditions to disable the output.	R/W*1
b4	IC4ADDMT34ZE	MTU3 and MTU4 Output Disabling Condition POE10F Add	0: Does not add the flag to the conditions to disable the output. 1: Adds the flag to the conditions to disable the output.	R/W*1
b5	IC5ADDMT34ZE	MTU3 and MTU4 Output Disabling Condition POE11F Add	0: Does not add the flag to the conditions to disable the output. 1: Adds the flag to the conditions to disable the output.	R/W*1
b6	IC6ADDMT34ZE	MTU3 and MTU4 Output Disabling Condition POE12F Add	0: Does not add the flag to the conditions to disable the output. 1: Adds the flag to the conditions to disable the output.	R/W*1
b7	—	Reserved	This bit is read as 0. The write value should be 0	R/W
b8	CMADDMT67ZE	MTU6 and MTU7 Output Disabling Condition CFLAG Add	0: Does not add the flags to the conditions to disable the output. 1: Adds the flags to the conditions to disable the output.	R/W*1
b9	IC1ADDMT67ZE	MTU6 and MTU7 Output Disabling Condition POE0F Add	0: Does not add the flag to the conditions to disable the output. 1: Adds the flag to the conditions to disable the output.	R/W*1
b10	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b11	IC3ADDMT67ZE	MTU6 and MTU7 Output Disabling Condition POE8F Add	0: Does not add the flag to the conditions to disable the output. 1: Adds the flag to the conditions to disable the output.	R/W*1
b12	IC4ADDMT67ZE	MTU6 and MTU7 Output Disabling Condition POE10F Add	0: Does not add the flag to the conditions to disable the output. 1: Adds the flag to the conditions to disable the output.	R/W*1
b13	IC5ADDMT67ZE	MTU6 and MTU7 Output Disabling Condition POE11F Add	0: Does not add the flag to the conditions to disable the output. 1: Adds the flag to the conditions to disable the output.	R/W*1
b14	IC6ADDMT67ZE	MTU6 and MTU7 Output Disabling Condition POE12F Add	0: Does not add the flag to the conditions to disable the output. 1: Adds the flag to the conditions to disable the output.	R/W*1
b15	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset.

The POECR4 register is used to extend the control conditions to disable the output of the MTU complementary PWM output pins (MTU3, MTU4, MTU6, and MTU7) and the GPT output pins (GPT0 to GPT2).

CMADDMT34ZE Bit (MTU3 and MTU4 Output Disabling Condition CFLAG Add)

Adds the POECMPFR.CnFLAG flag (n = 0 to 3) to the output disabling control conditions for the MTU3, MTU4, and GPT0 to GPT2 pins of P71 to P76 (MTIOC3B/GTIOC0A, MTIOC3D/GTIOC0B, MTIOC4A/GTIOC1A, MTIOC4C/GTIOC1B, MTIOC4B/GTIOC2A, MTIOC4D/GTIOC2B).

However, when the pins are disabled by the flag, an OEIn interrupt (n = 1 to 5) will not be generated.

IC2ADDMT34ZE Bit (MTU3 and MTU4 Output Disabling Condition POE4F Add)

Adds the ICSR2.POE4F flag to the output disabling control conditions for the MTU3, MTU4, and GPT0 to GPT2 pins of P71 to P76 (MTIOC3B/GTIOC0A, MTIOC3D/GTIOC0B, MTIOC4A/GTIOC1A, MTIOC4C/GTIOC1B, MTIOC4B/GTIOC2A, MTIOC4D/GTIOC2B).

IC3ADDMT34ZE Bit (MTU3 and MTU4 Output Disabling Condition POE8F Add)

Adds the ICSR3.POE8F flag to the output disabling control conditions for the MTU3, MTU4, and GPT0 to GPT2 pins of P71 to P76 (MTIOC3B/GTIOC0A, MTIOC3D/GTIOC0B, MTIOC4A/GTIOC1A, MTIOC4C/GTIOC1B, MTIOC4B/GTIOC2A, MTIOC4D/GTIOC2B).

IC4ADDMT34ZE Bit (MTU3 and MTU4 Output Disabling Condition POE10F Add)

Adds the ICSR4.POE10F flag to the output disabling control conditions for the MTU3,MTU4, and GPT0 to GPT2 pins of P71 to P76 (MTIOC3B/GTIOC0A, MTIOC3D/GTIOC0B, MTIOC4A/GTIOC1A, MTIOC4C/GTIOC1B, MTIOC4B/GTIOC2A, MTIOC4D/GTIOC2B).

IC5ADDMT34ZE Bit (MTU3 and MTU4 Output Disabling Condition POE11F Add)

Adds the ICSR5.POE11F flag to the output disabling control conditions for the MTU3, MTU4, and GPT0 to GPT2 pins of P71 to P76 (MTIOC3B/GTIOC0A, MTIOC3D/GTIOC0B, MTIOC4A/GTIOC1A, MTIOC4C/GTIOC1B, MTIOC4B/GTIOC2A, MTIOC4D/GTIOC2B).

IC6ADDMT34ZE Bit (MTU3 and MTU4 Output Disabling Condition POE12F Add)

Adds the ICSR7.POE12F flag to the output disabling control conditions for the MTU3, MTU4, and GPT0 to GPT2 pins of P71 to P76 (MTIOC3B/GTIOC0A, MTIOC3D/GTIOC0B, MTIOC4A/GTIOC1A, MTIOC4C/GTIOC1B, MTIOC4B/GTIOC2A, MTIOC4D/GTIOC2B).

CMADDMT67ZE Bit (MTU6 and MTU7 Output Disabling Condition CFLAG Add)

Adds the POECMPFR.CnFLAG flag (n = 0 to 3) to the output disabling control conditions for the MTU6 and MTU7 pins (MTIOC6B, MTIOC6D, MTIOC7A, MTIOC7C, MTIOC7B, MTIOC7D).

However, when the pins are disabled by the flag, an OEIn interrupt (n = 1 to 5) will not be generated.

IC1ADDMT67ZE Bit (MTU6 and MTU7 Output Disabling Condition POE0F Add)

Adds the ICSR1.POE0F flag to the output disabling control conditions for the MTU6 and MTU7 pins (MTIOC6B, MTIOC6D, MTIOC7A, MTIOC7C, MTIOC7B, MTIOC7D).

IC3ADDMT67ZE Bit (MTU6 and MTU7 Output Disabling Condition POE8F Add)

Adds the ICSR3.POE8F flag to the output disabling control conditions for the MTU6 and MTU7 pins (MTIOC6B, MTIOC6D, MTIOC7A, MTIOC7C, MTIOC7B, MTIOC7D).

IC4ADDMT67ZE Bit (MTU6 and MTU7 Output Disabling Condition POE10F Add)

Adds the ICSR4.POE10F flag to the output disabling control conditions for the MTU6 and MTU7 pins (MTIOC6B, MTIOC6D, MTIOC7A, MTIOC7C, MTIOC7B, MTIOC7D).

IC5ADDMT67ZE Bit (MTU6 and MTU7 Output Disabling Condition POE11F Add)

Adds the ICSR5.POE11F flag to the output disabling control conditions for the MTU6 and MTU7 pins (MTIOC6B, MTIOC6D, MTIOC7A, MTIOC7C, MTIOC7B, MTIOC7D).

IC6ADDMT67ZE Bit (MTU6 and MTU7 Output Disabling Condition POE12F Add)

Adds the ICSR7.POE12F flag to the output disabling control conditions for the MTU6 and MTU7 pins (MTIOC6B, MTIOC6D, MTIOC7A, MTIOC7C, MTIOC7B, MTIOC7D).

21.2.19 Port Output Enable Control Register 5 (POECR5)

Address(es): 0008 C4D2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	IC6ADDMT0ZE	IC5ADDMT0ZE	IC4ADDMT0ZE	—	IC2ADDMT0ZE	IC1ADDMT0ZE	CMADDMT0ZE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CMADDMT0ZE	MTU0 Output Disabling Condition CFLAG Add	0: Does not add the flags to the conditions to disable the output. 1: Adds the flags to the conditions to disable the output.	R/W*1
b1	IC1ADDMT0ZE	MTU0 Output Disabling Condition POE0F Add	0: Does not add the flag to the conditions to disable the output. 1: Adds the flag to the conditions to disable the output.	R/W*1
b2	IC2ADDMT0ZE	MTU0 Output Disabling Condition POE4F Add	0: Does not add the flag to the conditions to disable the output. 1: Adds the flag to the conditions to disable the output.	R/W*1
b3	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b4	IC4ADDMT0ZE	MTU0 Output Disabling Condition POE10F Add	0: Does not add the flag to the conditions to disable the output. 1: Adds the flag to the conditions to disable the output.	R/W*1
b5	IC5ADDMT0ZE	MTU0 Output Disabling Condition POE11F Add	0: Does not add the flag to the conditions to disable the output. 1: Adds the flag to the conditions to disable the output.	R/W*1
b6	IC6ADDMT0ZE	MTU0 Output Disabling Condition POE12F Add	0: Does not add the flag to the conditions to disable the output. 1: Adds the flag to the conditions to disable the output.	R/W*1
b15 to b7	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset.

The POECR5 register is used to extend the control conditions to disable the output of the MTU0 pins.

CMADDMT0ZE Bit (MTU0 Output Disabling Condition CFLAG Add)

Adds the POECMPFR.CnFLAG flag (n = 0 to 3) to the output disabling control conditions for the MTU0 pin (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D).
However, when the pins are disabled by the flag, an OEIn interrupt (n = 1 to 5) will not be generated.

IC1ADDMT0ZE Bit (MTU0 Output Disabling Condition POE0F Add)

Adds the ICSR1.POE0F flag to the output disabling control conditions for the MTU0 pin (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D).

IC2ADDMT0ZE Bit (MTU0 Output Disabling Condition POE4F Add)

Adds the ICSR2.POE4F flag to the output disabling control conditions for the MTU0 pin (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D).

IC4ADDMT0ZE Bit (MTU0 Output Disabling Condition POE10F Add)

Adds the ICSR4.POE10F flag to the output disabling control conditions for the MTU0 pin (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D).

IC5ADDMT0ZE Bit (MTU0 Output Disabling Condition POE11F Add)

Adds the ICSR5.POE11F flag to the output disabling control conditions for the MTU0 pin (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D).

IC6ADDMT0ZE Bit (MTU0 Output Disabling Condition POE12F Add)

Adds the ICSR7.POE12F flag to the output disabling control conditions for the MTU0 pin (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D).

21.2.20 Port Output Enable Control Register 6 (POECR6)

Address(es): 0008 C4D4h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	IC6ADDGPT03ZE	—	IC4ADDGPT03ZE	IC3ADDGPT03ZE	IC2ADDGPT03ZE	IC1ADDGPT03ZE	CMADDGPT03ZE	—	IC6ADDGPT02ZE	IC5ADDGPT02ZE	—	IC3ADDGPT02ZE	IC2ADDGPT02ZE	IC1ADDGPT02ZE	CMADDGPT02ZE
Value after reset:	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CMADDGPT02ZE	GPT0 to GPT2 Output Disabling Condition CFLAG Add	0: Does not add the flags to the conditions to disable the output. 1: Adds the flags to the conditions to disable the output.	R/W*1
b1	IC1ADDGPT02ZE	GPT0 to GPT2 Output Disabling Condition POE0F Add	0: Does not add the flag to the conditions to disable the output. 1: Adds the flag to the conditions to disable the output.	R/W*1
b2	IC2ADDGPT02ZE	GPT0 to GPT2 Output Disabling Condition POE4F Add	0: Does not add the flag to the conditions to disable the output. 1: Adds the flag to the conditions to disable the output.	R/W*1
b3	IC3ADDGPT02ZE	GPT0 to GPT2 Output Disabling Condition POE8F Add	0: Does not add the flag to the conditions to disable the output. 1: Adds the flag to the conditions to disable the output.	R/W*1
b4	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b5	IC5ADDGPT02ZE	GPT0 to GPT2 Output Disabling Condition POE11F Add	0: Does not add the flag to the conditions to disable the output. 1: Adds the flag to the conditions to disable the output.	R/W*1
b6	IC6ADDGPT02ZE	GPT0 to GPT2 Output Disabling Condition POE12F Add	0: Does not add the flag to the conditions to disable the output. 1: Adds the flag to the conditions to disable the output.	R/W*1
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b8	CMADDGPT03ZE	GPT0 to GPT3 Output Disabling Condition CFLAG Add	0: Does not add the flags to the conditions to disable the output. 1: Adds the flags to the conditions to disable the output.	R/W*1
b9	IC1ADDGPT03ZE	GPT0 to GPT3 Output Disabling Condition POE0F Add	0: Does not add the flag to the conditions to disable the output. 1: Adds the flag to the conditions to disable the output.	R/W*1
b10	IC2ADDGPT03ZE	GPT0 to GPT3 Output Disabling Condition POE4F Add	0: Does not add the flag to the conditions to disable the output. 1: Adds the flag to the conditions to disable the output.	R/W*1
b11	IC3ADDGPT03ZE	GPT0 to GPT3 Output Disabling Condition POE8F Add	0: Does not add the flag to the conditions to disable the output. 1: Adds the flag to the conditions to disable the output.	R/W*1
b12	IC4ADDGPT03ZE	GPT0 to GPT3 Output Disabling Condition POE10F Add	0: Does not add the flag to the conditions to disable the output. 1: Adds the flag to the conditions to disable the output.	R/W*1
b13	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b14	IC6ADDGPT03ZE	GPT0 to GPT3 Output Disabling Condition POE12F Add	0: Does not add the flag to the conditions to disable the output. 1: Adds the flag to the conditions to disable the output.	R/W*1
b15	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset.

The POECR6 register is used to extend the control conditions to disable the output of the GPT0 to GPT3 pins and the MTU complementary PWM output pins (MTU3 and MTU4).

CMADDGPT02ZE Bit (GPT0 to GPT2 Output Disabling Condition CFLAG Add)

Adds the POECMPFR.CnFLAG flag (n = 0 to 3) to the output disabling control conditions for the MTU3, MTU4, and GPT0 to GPT2 pins of P12 to P17 (MTIOC3B/GTIOC0A, MTIOC3D/GTIOC0B, MTIOC4A/GTIOC1A, MTIOC4C/GTIOC1B, MTIOC4B/GTIOC2A, MTIOC4D/GTIOC2B).

However, when the pins are disabled by the flag, an OEIn interrupt (n = 1 to 5) will not be generated.

IC1ADDGPT02ZE Bit (GPT0 to GPT2 Output Disabling Condition POE0F Add)

Adds the ICSR1.POE0F flag to the output disabling control conditions for the MTU3, MTU4, and GPT0 to GPT2 pins of P12 to P17 (MTIOC3B/GTIOC0A, MTIOC3D/GTIOC0B, MTIOC4A/GTIOC1A, MTIOC4C/GTIOC1B, MTIOC4B/GTIOC2A, MTIOC4D/GTIOC2B).

IC2ADDGPT02ZE Bit (GPT0 to GPT2 Output Disabling Condition POE4F Add)

Adds the ICSR2.POE4F flag to the output disabling control conditions for the MTU3, MTU4, and GPT0 to GPT2 pins of P12 to P17 (MTIOC3B/GTIOC0A, MTIOC3D/GTIOC0B, MTIOC4A/GTIOC1A, MTIOC4C/GTIOC1B, MTIOC4B/GTIOC2A, MTIOC4D/GTIOC2B).

IC3ADDGPT02ZE Bit (GPT0 to GPT2 Output Disabling Condition POE8F Add)

Adds the ICSR3.POE8F flag to the output disabling control conditions for the MTU3, MTU4, and GPT0 to GPT2 pins of P12 to P17 (MTIOC3B/GTIOC0A, MTIOC3D/GTIOC0B, MTIOC4A/GTIOC1A, MTIOC4C/GTIOC1B, MTIOC4B/GTIOC2A, MTIOC4D/GTIOC2B).

IC5ADDGPT02ZE Bit (GPT0 to GPT2 Output Disabling Condition POE11F Add)

Adds the ICSR5.POE11F flag to the output disabling control conditions for the MTU3, MTU4, and GPT0 to GPT2 pins of P12 to P17 (MTIOC3B/GTIOC0A, MTIOC3D/GTIOC0B, MTIOC4A/GTIOC1A, MTIOC4C/GTIOC1B, MTIOC4B/GTIOC2A, MTIOC4D/GTIOC2B).

IC6ADDGPT02ZE Bit (GPT0 to GPT2 Output Disabling Condition POE12F Add)

Adds the ICSR7.POE12F flag to the output disabling control conditions for the MTU3, MTU4, and GPT0 to GPT2 pins of P12 to P17 (MTIOC3B/GTIOC0A, MTIOC3D/GTIOC0B, MTIOC4A/GTIOC1A, MTIOC4C/GTIOC1B, MTIOC4B/GTIOC2A, MTIOC4D/GTIOC2B).

CMADDGPT03ZE Bit (GPT0 to GPT3 Output Disabling Condition CFLAG Add)

Adds the POECMPFR.CnFLAG flag (n = 0 to 3) to the output disabling control conditions for the GPT0 to GPT3 pins of PB5 to PB7, PD0 to PD2, PD6, and PD7 (GTIOC0A, GTIOC0B, GTIOC1A, GTIOC1B, GTIOC2A, GTIOC2B, GTIOC3A, GTIOC3B).

However, when the pins are disabled by the flag, an OEIn interrupt (n = 1 to 5) will not be generated.

IC1ADDGPT03ZE Bit (GPT0 to GPT3 Output Disabling Condition POE0F Add)

Adds the ICSR1.POE0F flag to the output disabling control conditions for the GPT0 to GPT3 pins of PB5 to PB7, PD0 to PD2, PD6, and PD7 (GTIOC0A, GTIOC0B, GTIOC1A, GTIOC1B, GTIOC2A, GTIOC2B, GTIOC3A, GTIOC3B).

IC2ADDGPT03ZE Bit (GPT0 to GPT3 Output Disabling Condition POE4F Add)

Adds the ICSR2.POE4F flag to the output disabling control conditions for the GPT0 to GPT3 pins of PB5 to PB7, PD0 to PD2, PD6, and PD7 (GTIOC0A, GTIOC0B, GTIOC1A, GTIOC1B, GTIOC2A, GTIOC2B, GTIOC3A, GTIOC3B).

IC3ADDGPT03ZE Bit (GPT0 to GPT3 Output Disabling Condition POE8F Add)

Adds the ICSR3.POE8F flag to the output disabling control conditions for the GPT0 to GPT3 pins of PB5 to PB7, PD0 to PD2, PD6, and PD7 (GTIOC0A, GTIOC0B, GTIOC1A, GTIOC1B, GTIOC2A, GTIOC2B, GTIOC3A, GTIOC3B).

IC4ADDGPT03ZE Bit (GPT0 to GPT3 Output Disabling Condition POE10F Add)

Adds the ICSR4.POE10F flag to the output disabling control conditions for the GPT0 to GPT3 pins of PB5 to PB7, PD0 to PD2, PD6, and PD7 (GTIOC0A, GTIOC0B, GTIOC1A, GTIOC1B, GTIOC2A, GTIOC2B, GTIOC3A, GTIOC3B).

IC6ADDGPT03ZE Bit (GPT0 to GPT3 Output Disabling Condition POE12F Add)

Adds the ICSR7.POE12F flag to the output disabling control conditions for the GPT0 to GPT3 pins of PB5 to PB7, PD0 to PD2, PD6, and PD7 (GTIOC0A, GTIOC0B, GTIOC1A, GTIOC1B, GTIOC2A, GTIOC2B, GTIOC3A, GTIOC3B).

21.2.21 Port Output Enable Control Register 7 (POECR7)

Address(es): 0008 C4E2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	MTU9C2ZE	—	MTU9A2ZE	MTU9D1ZE	MTU9C1ZE	MTU9B1ZE	MTU9A1ZE	MTU9DZE	MTU9CZE	MTU9BZE	MTU9AZE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	MTU9AZE	MTIOC9A (PD7) Pin High-Impedance Enable	0: Does not switch the pin to high-impedance state. 1: Switch the pin to high-impedance state.	R/W*1
b1	MTU9BZE	MTIOC9B (PE0) Pin High-Impedance Enable	0: Does not switch the pin to high-impedance state. 1: Switch the pin to high-impedance state.	R/W*1
b2	MTU9CZE	MTIOC9C (PD6) Pin High-Impedance Enable	0: Does not switch the pin to high-impedance state. 1: Switch the pin to high-impedance state.	R/W*1
b3	MTU9DZE	MTIOC9D (PE1) Pin High-Impedance Enable	0: Does not switch the pin to high-impedance state. 1: Switch the pin to high-impedance state.	R/W*1
b4	MTU9A1ZE	MTIOC9A (P21) Pin High-Impedance Enable	0: Does not switch the pin to high-impedance state. 1: Switch the pin to high-impedance state.	R/W*1
b5	MTU9B1ZE	MTIOC9B (P10) Pin High-Impedance Enable	0: Does not switch the pin to high-impedance state. 1: Switch the pin to high-impedance state.	R/W*1
b6	MTU9C1ZE	MTIOC9C (P20) Pin High-Impedance Enable	0: Does not switch the pin to high-impedance state. 1: Switch the pin to high-impedance state.	R/W*1
b7	MTU9D1ZE	MTIOC9D (P02) Pin High-Impedance Enable	0: Does not switch the pin to high-impedance state. 1: Switch the pin to high-impedance state.	R/W*1
b8	MTU9A2ZE	MTIOC9A (P26) Pin High-Impedance Enable	0: Does not switch the pin to high-impedance state. 1: Switch the pin to high-impedance state.	R/W*1
b9	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b10	MTU9C2ZE	MTIOC9C (P25) Pin High-Impedance Enable	0: Does not switch the pin to high-impedance state. 1: Switch the pin to high-impedance state.	R/W*1
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset.

The POECR7 register controls high-impedance state of the MTU9 pins.

MTU9AZE Bit (MTIOC9A (PD7) Pin High-Impedance Enable)

This bit specifies whether to switch the MTIOC9A output for the MTU9 pin of PD7 to high-impedance state when any of the ICSR7.POE12F flag, SPOER.MTUCH9HIZ bit, and ICSR6.OSTSTF flag (when the OSTSTE bit is 1), or, as additionally specified in the POECR8 register, the ICSRn.POEmF flag (n = 1 to 5; m = 0, 4, 8, 10, 11), or POECMPFR.CnFLAG flag (n = 0 to 3), is set to 1.
Set the PMMCR3.MTU9AME bit to 0 when setting this bit to 1.

MTU9BZE Bit (MTIOC9B (PE0) Pin High-Impedance Enable)

This bit specifies whether to switch the MTIOC9B output for the MTU9 pin of PE0 to high-impedance state when any of the ICSR7.POE12F flag, SPOER.MTUCH9HIZ bit, and ICSR6.OSTSTF flag (when the OSTSTE bit is 1), or, as additionally specified in the POECR8 register, the ICSRn.POEmF flag (n = 1 to 5; m = 0, 4, 8, 10, 11), or POECMPFR.CnFLAG flag (n = 0 to 3), is set to 1.
Set the PMMCR3.MTU9BME bit to 0 when setting this bit to 1.

MTU9CZE Bit (MTIOC9C (PD6) Pin High-Impedance Enable)

This bit specifies whether to switch the MTIOC9C output for the MTU9 pin of PD6 to high-impedance state when any of the ICSR7.POE12F flag, SPOER.MTUCH9HIZ bit, and ICSR6.OSTSTF flag (when the OSTSTE bit is 1), or, as additionally specified in the POECR8 register, the ICSRn.POEmF flag (n = 1 to 5; m = 0, 4, 8, 10, 11), or POECMPFR.CnFLAG flag (n = 0 to 3), is set to 1.
Set the PMMCR3.MTU9CME bit to 0 when setting this bit to 1.

MTU9DZE Bit (MTIOC9D (PE1) Pin High-Impedance Enable)

This bit specifies whether to switch the MTIOC9D output for the MTU9 pin of PE1 to high-impedance state when any of the ICSR7.POE12F flag, SPOER.MTUCH9HIZ bit, and ICSR6.OSTSTF flag (when the OSTSTE bit is 1), or, as additionally specified in the POECR8 register, the ICSRn.POEmF flag (n = 1 to 5; m = 0, 4, 8, 10, 11), or POECMPFR.CnFLAG flag (n = 0 to 3), is set to 1.
Set the PMMCR3.MTU9DME bit to 0 when setting this bit to 1.

MTU9A1ZE Bit (MTIOC9A (P21) Pin High-Impedance Enable)

This bit specifies whether to switch the MTIOC9A output for the MTU9 pin of P21 to high-impedance state when any of the ICSR7.POE12F flag, SPOER.MTUCH9HIZ bit, and ICSR6.OSTSTF flag (when the OSTSTE bit is 1), or, as additionally specified in the POECR8 register, the ICSRn.POEmF flag (n = 1 to 5; m = 0, 4, 8, 10, 11), or POECMPFR.CnFLAG flag (n = 0 to 3), is set to 1.
Set the PMMCR3.MTU9A1ME bit to 0 when setting this bit to 1.

MTU9B1ZE Bit (MTIOC9B (P10) Pin High-Impedance Enable)

This bit specifies whether to switch the MTIOC9B output for the MTU9 pin of P10 to high-impedance state when any of the ICSR7.POE12F flag, SPOER.MTUCH9HIZ bit, and ICSR6.OSTSTF flag (when the OSTSTE bit is 1), or, as additionally specified in the POECR8 register, the ICSRn.POEmF flag (n = 1 to 5; m = 0, 4, 8, 10, 11), or POECMPFR.CnFLAG flag (n = 0 to 3), is set to 1.
Set the PMMCR3.MTU9B1ME bit to 0 when setting this bit to 1.

MTU9C1ZE Bit (MTIOC9C (P20) Pin High-Impedance Enable)

This bit specifies whether to switch the MTIOC9C output for the MTU9 pin of P20 to high-impedance state when any of the ICSR7.POE12F flag, SPOER.MTUCH9HIZ bit, and ICSR6.OSTSTF flag (when the OSTSTE bit is 1), or, as additionally specified in the POECR8 register, the ICSRn.POEmF flag (n = 1 to 5; m = 0, 4, 8, 10, 11), or POECMPFR.CnFLAG flag (n = 0 to 3), is set to 1.
Set the PMMCR3.MTU9C1ME bit to 0 when setting this bit to 1.

MTU9D1ZE Bit (MTIOC9D (P02) Pin High-Impedance Enable)

This bit specifies whether to switch the MTIOC9D output for the MTU9 pin of P02 to high-impedance state when any of the ICSR7.POE12F flag, SPOER.MTUCH9HIZ bit, and ICSR6.OSTSTF flag (when the OSTSTE bit is 1), or, as additionally specified in the POECR8 register, the ICSRn.POEmF flag (n = 1 to 5; m = 0, 4, 8, 10, 11), or POECMPFR.CnFLAG flag (n = 0 to 3), is set to 1.
Set the PMMCR3.MTU9D1ME bit to 0 when setting this bit to 1.

MTU9A2ZE Bit (MTIOC9A (P26) Pin High-Impedance Enable)

This bit specifies whether to switch the MTIOC9A output for the MTU9 pin of P26 to high-impedance state when any of the ICSR7.POE12F flag, SPOER.MTUCH9HIZ bit, and ICSR6.OSTSTF flag (when the OSTSTE bit is 1), or, as additionally specified in the POECR8 register, the ICSRn.POEmF flag (n = 1 to 5; m = 0, 4, 8, 10, 11), or POECMPFR.CnFLAG flag (n = 0 to 3), is set to 1.
Set the PMMCR3.MTU9A2ME bit to 0 when setting this bit to 1.

MTU9C2ZE Bit (MTIOC9C (P25) Pin High-Impedance Enable)

This bit specifies whether to switch the MTIOC9C output for the MTU9 pin of P25 to high-impedance state when any of the ICSR7.POE12F flag, SPOER.MTUCH9HIZ bit, and ICSR6.OSTSTF flag (when the OSTSTE bit is 1), or, as additionally specified in the POECR8 register, the ICSRn.POEmF flag (n = 1 to 5; m = 0, 4, 8, 10, 11), or POECMPFR.CnFLAG flag (n = 0 to 3), is set to 1.
Set the PMMCR3.MTU9C2ME bit to 0 when setting this bit to 1.

21.2.22 Port Output Enable Control Register 8 (POECR8)

Address(es): 0008 C4E4h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	IC5ADDMT9ZE	IC4ADDMT9ZE	IC3ADDMT9ZE	IC2ADDMT9ZE	IC1ADDMT9ZE	CMADDMT9ZE
Value after reset:	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CMADDMT9ZE	MTU9 Output Disabling Condition CFLAG Add	0: Does not add the flags to the conditions to disable the output. 1: Adds the flags to the conditions to disable the output.	R/W*1
b1	IC1ADDMT9ZE	MTU9 Output Disabling Condition POE0F Add	0: Does not add the flag to the conditions to disable the output. 1: Adds the flag to the conditions to disable the output.	R/W*1
b2	IC2ADDMT9ZE	MTU9 Output Disabling Condition POE4F Add	0: Does not add the flag to the conditions to disable the output. 1: Adds the flag to the conditions to disable the output.	R/W*1
b3	IC3ADDMT9ZE	MTU9 Output Disabling Condition POE8F Add	0: Does not add the flag to the conditions to disable the output. 1: Adds the flag to the conditions to disable the output.	R/W*1
b4	IC4ADDMT9ZE	MTU9 Output Disabling Condition POE10F Add	0: Does not add the flag to the conditions to disable the output. 1: Adds the flag to the conditions to disable the output.	R/W*1
b5	IC5ADDMT9ZE	MTU9 Output Disabling Condition POE11F Add	0: Does not add the flag to the conditions to disable the output. 1: Adds the flag to the conditions to disable the output.	R/W*1
b6	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b15 to b7	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset.

The POECR8 register is used to extend the control conditions to disable the output of the MTU9 pins.

CMADDMT9ZE Bit (MTU9 Output Disabling Condition CFLAG Add)

Adds the POECMPFR.CnFLAG flag (n = 0 to 3) to the output disabling control conditions for the MTU9 pin (MTIOC9A, MTIOC9B, MTIOC9C, MTIOC9D).
However, when the pins are disabled by the flag, an OEIn interrupt (n = 1 to 5) will not be generated.

IC1ADDMT9ZE Bit (MTU9 Output Disabling Condition POE0F Add)

Adds the ICSR1.POE0F flag to the output disabling control conditions for the MTU9 pin (MTIOC9A, MTIOC9B, MTIOC9C, MTIOC9D).

IC2ADDMT9ZE Bit (MTU9 Output Disabling Condition POE4F Add)

Adds the ICSR2.POE4F flag to the output disabling control conditions for the MTU9 pin (MTIOC9A, MTIOC9B, MTIOC9C, MTIOC9D).

IC3ADDMT9ZE Bit (MTU9 Output Disabling Condition POE8F Add)

Adds the ICSR3.POE8F flag to the output disabling control conditions for the MTU9 pin (MTIOC9A, MTIOC9B, MTIOC9C, MTIOC9D).

IC4ADDMT9ZE Bit (MTU9 Output Disabling Condition POE10F Add)

Adds the ICSR4.POE10F flag to the output disabling control conditions for the MTU9 pin (MTIOC9A, MTIOC9B, MTIOC9C, MTIOC9D).

IC5ADDMT9ZE Bit (MTU9 Output Disabling Condition POE11F Add)

Adds the ICSR5.POE11F flag to the output disabling control conditions for the MTU9 pin (MTIOC9A, MTIOC9B, MTIOC9C, MTIOC9D).

21.2.23 Port Mode Mask Control Register 0 (PMMCR0)

Address(es): 0008 C4F0h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	MTU0B1ME	MTU0A1ME	MTU0DME	MTU0CME	MTU0BME	MTU0AME
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	MTU0AME	MTIOC0A (PB3) Pin Port Mode Mask Enable	0: Switching to the general I/O port pin is disabled. 1: Switching to the general I/O port pin is enabled.	R/W*1
b1	MTU0BME	MTIOC0B (PB2) Pin Port Mode Mask Enable	0: Switching to the general I/O port pin is disabled. 1: Switching to the general I/O port pin is enabled.	R/W*1
b2	MTU0CME	MTIOC0C Pin Port Mode Mask Enable	0: Switching to the general I/O port pin is disabled. 1: Switching to the general I/O port pin is enabled.	R/W*1
b3	MTU0DME	MTIOC0D Pin Port Mode Mask Enable	0: Switching to the general I/O port pin is disabled. 1: Switching to the general I/O port pin is enabled.	R/W*1
b4	MTU0A1ME	MTIOC0A (P31) Pin Port Mode Mask Enable	0: Switching to the general I/O port pin is disabled. 1: Switching to the general I/O port pin is enabled.	R/W*1
b5	MTU0B1ME	MTIOC0B (P30) Pin Port Mode Mask Enable	0: Switching to the general I/O port pin is disabled. 1: Switching to the general I/O port pin is enabled.	R/W*1
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset.

The PMMCR0 register is used to mask the settings of the PMR register related to the MTU0 pin.

MTU0AME Bit (MTIOC0A (PB3) Pin Port Mode Mask Enable)

This bit specifies whether switching the MTIOC0A pin of PB3 to the general I/O port when one of the following flags and bit is set to 1: the ICSR3.POE8F flag, the SPOER.MTUCH0HIZ bit, the ICSR6.OSTSTF flag (when the ICSR6.OSTSTE bit is 1), the ICSRn.POEmF flag (n = 1, 2, 4, 5, 7; m = 0, 4, 10, 11, 12) additionally selected in the POECR5 register, and the POECMPFR.CnFLAG flag (n = 0 to 3).

When setting this bit to 1, set the POECR1.MTU0AZE bit to 0. When the POECR1.MTU0AZE bit is 1, the setting of the bit is ignored.

MTU0BME Bit (MTIOC0B (PB2) Pin Port Mode Mask Enable)

This bit specifies whether switching the MTIOC0B pin of PB2 to the general I/O port when one of the following flags and bit is set to 1: the ICSR3.POE8F flag, the SPOER.MTUCH0HIZ bit, the ICSR6.OSTSTF flag (when the ICSR6.OSTSTE bit is 1), the ICSRn.POEmF flag (n = 1, 2, 4, 5, 7; m = 0, 4, 10, 11, 12) additionally selected in the POECR5 register, and the POECMPFR.CnFLAG flag (n = 0 to 3).

When setting this bit to 1, set the POECR1.MTU0BZE bit to 0. When the POECR1.MTU0BZE bit is 1, the setting of the bit is ignored.

MTU0CME Bit (MTIOC0C Pin Port Mode Mask Enable)

This bit specifies whether switching the MTIOC0C pin to the general I/O port when one of the following flags and bit is set to 1: the ICSR3.POE8F flag, the SPOER.MTUCH0HIZ bit, the ICSR6.OSTSTF flag (when the ICSR6.OSTSTE bit is 1), the ICSRn.POEmF flag (n = 1, 2, 4, 5, 7; m = 0, 4, 10, 11, 12) additionally selected in the POECR5 register, and the POECMPFR.CnFLAG flag (n = 0 to 3).

When setting this bit to 1, set the POECR1.MTU0CZE bit to 0. When the POECR1.MTU0CZE bit is 1, the setting of the bit is ignored.

MTU0DME Bit (MTIOC0D Pin Port Mode Mask Enable)

This bit specifies whether switching the MTIOC0D pin to the general I/O port when one of the following flags and bit is set to 1: the ICSR3.POE8F flag, the SPOER.MTUCH0HIZ bit, the ICSR6.OSTSTF flag (when the ICSR6.OSTSTE bit is 1), the ICSRn.POEmF flag (n = 1, 2, 4, 5, 7; m = 0, 4, 10, 11, 12) additionally selected in the POECR5 register, and the POECMPFR.CnFLAG flag (n = 0 to 3).

When setting this bit to 1, set the POECR1.MTU0DZE bit to 0. When the POECR1.MTU0DZE bit is 1, the setting of the bit is ignored.

MTU0A1ME Bit (MTIOC0A (P31) Pin Port Mode Mask Enable)

This bit specifies whether switching the MTIOC0A pin of P31 to the general I/O port when one of the following flags and bit is set to 1: the ICSR3.POE8F flag, the SPOER.MTUCH0HIZ bit, the ICSR6.OSTSTF flag (when the ICSR6.OSTSTE bit is 1), the ICSRn.POEmF flag (n = 1, 2, 4, 5, 7; m = 0, 4, 10, 11, 12) additionally selected in the POECR5 register, and the POECMPFR.CnFLAG flag (n = 0 to 3).

When setting this bit to 1, set the POECR1.MTU0A1ZE bit to 0. When the POECR1.MTU0A1ZE bit is 1, the setting of the bit is ignored.

MTU0B1ME Bit (MTIOC0B (P30) Pin Port Mode Mask Enable)

This bit specifies whether switching the MTIOC0B pin of P30 to the general I/O port when one of the following flags and bit is set to 1: the ICSR3.POE8F flag, the SPOER.MTUCH0HIZ bit, the ICSR6.OSTSTF flag (when the ICSR6.OSTSTE bit is 1), the ICSRn.POEmF flag (n = 1, 2, 4, 5, 7; m = 0, 4, 10, 11, 12) additionally selected in the POECR5 register, and the POECMPFR.CnFLAG flag (n = 0 to 3).

When setting this bit to 1, set the POECR1.MTU0B1ZE bit to 0. When the POECR1.MTU0B1ZE bit is 1, the setting of the bit is ignored.

21.2.24 Port Mode Mask Control Register 1 (PMMCR1)

Address(es): 0008 C4F2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	MTU3DME	MTU4CME	MTU4DME	MTU3BME	MTU4AME	MTU4BME	—	—	MTU6DME	MTU7CME	MTU7DME	MTU6BME	MTU7AME	MTU7BME
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	MTU7BME	MTIOC7B Pin Port Mode Mask Enable	0: Switching to the general I/O port pin is disabled. 1: Switching to the general I/O port pin is enabled.	R/W*1
b1	MTU7AME	MTIOC7A Pin Port Mode Mask Enable	0: Switching to the general I/O port pin is disabled. 1: Switching to the general I/O port pin is enabled.	R/W*1
b2	MTU6BME	MTIOC6B Pin Port Mode Mask Enable	0: Switching to the general I/O port pin is disabled. 1: Switching to the general I/O port pin is enabled.	R/W*1
b3	MTU7DME	MTIOC7D Pin Port Mode Mask Enable	0: Switching to the general I/O port pin is disabled. 1: Switching to the general I/O port pin is enabled.	R/W*1
b4	MTU7CME	MTIOC7C Pin Port Mode Mask Enable	0: Switching to the general I/O port pin is disabled. 1: Switching to the general I/O port pin is enabled.	R/W*1
b5	MTU6DME	MTIOC6D Pin Port Mode Mask Enable	0: Switching to the general I/O port pin is disabled. 1: Switching to the general I/O port pin is enabled.	R/W*1
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	MTU4BME	MTIOC4B/GTIOC2A (P73) Pin Port Mode Mask Enable	0: Switching to the general I/O port pin is disabled. 1: Switching to the general I/O port pin is enabled.	R/W*1
b9	MTU4AME	MTIOC4A/GTIOC1A (P72) Pin Port Mode Mask Enable	0: Switching to the general I/O port pin is disabled. 1: Switching to the general I/O port pin is enabled.	R/W*1
b10	MTU3BME	MTIOC3B/GTIOC0A (P71) Pin Port Mode Mask Enable	0: Switching to the general I/O port pin is disabled. 1: Switching to the general I/O port pin is enabled.	R/W*1
b11	MTU4DME	MTIOC4D/GTIOC2B (P76) Pin Port Mode Mask Enable	0: Switching to the general I/O port pin is disabled. 1: Switching to the general I/O port pin is enabled.	R/W*1
b12	MTU4CME	MTIOC4C/GTIOC1B (P75) Pin Port Mode Mask Enable	0: Switching to the general I/O port pin is disabled. 1: Switching to the general I/O port pin is enabled.	R/W*1
b13	MTU3DME	MTIOC3D/GTIOC0B (P74) Pin Port Mode Mask Enable	0: Switching to the general I/O port pin is disabled. 1: Switching to the general I/O port pin is enabled.	R/W*1
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset.

The PMMCR1 register is used to mask the settings of the PMR register related to the MTU complementary PWM output pins (MTU3, MTU4, MTU6, MTU7) or GPT output pins (GPT0 to GPT2) of P71 to P76 and P90 to P95.

MTU7BME Bit (MTIOC7B Pin Port Mode Mask Enable)

This bit specifies whether switching the MTIOC7B pin to the general I/O port when one of the following flags and bit is set to 1: the OCSR2.OSF2 flag, the ICSR2.POE4F flag, the SPOER.MTUCH67HIZ bit, the ICSR6.OSTSTF flag (when the ICSR6.OSTSTE bit is 1), the ICSRn.POEmF flag (n = 1, 3 to 5, 7; m = 0, 8, 10, 11, 12) additionally selected in the POECR4 register, and the POECMPFR.CnFLAG flag (n = 0 to 3).
When setting this bit to 1, set the POECR2.MTU7BDZE bit to 0. When the POECR2.MTU7BDZE bit is 1, the setting of the bit is ignored.

MTU7AME Bit (MTIOC7A Pin Port Mode Mask Enable)

This bit specifies whether switching the MTIOC7A pin to the general I/O port when one of the following flags and bit is set to 1: the OCSR2.OSF2 flag, the ICSR2.POE4F flag, the SPOER.MTUCH67HIZ bit, the ICSR6.OSTSTF flag (when

the ICSR6.OSTSTE bit is 1), the ICSRn.POEmF flag (n = 1, 3 to 5, 7; m = 0, 8, 10, 11, 12) additionally selected in the POECR4 register, and the POECMPFR.CnFLAG flag (n = 0 to 3).
When setting this bit to 1, set the POECR2.MTU7ACZE bit to 0. When the POECR2.MTU7ACZE bit is 1, the setting of the bit is ignored.

MTU6BME Bit (MTIOC6B Pin Port Mode Mask Enable)

This bit specifies whether switching the MTIOC6B pin to the general I/O port when one of the following flags and bit is set to 1: the OCSR2.OSF2 flag, the ICSR2.POE4F flag, the SPOER.MTUCH67HIZ bit, the ICSR6.OSTSTF flag (when the ICSR6.OSTSTE bit is 1), the ICSRn.POEmF flag (n = 1, 3 to 5, 7; m = 0, 8, 10, 11, 12) additionally selected in the POECR4 register, and the POECMPFR.CnFLAG flag (n = 0 to 3).
When setting this bit to 1, set the POECR2.MTU6BDZE bit to 0. When the POECR2.MTU6BDZE bit is 1, the setting of the bit is ignored.

MTU7DME Bit (MTIOC7D Pin Port Mode Mask Enable)

This bit specifies whether switching the MTIOC7D pin to the general I/O port when one of the following flags and bit is set to 1: the OCSR2.OSF2 flag, the ICSR2.POE4F flag, the SPOER.MTUCH67HIZ bit, the ICSR6.OSTSTF flag (when the ICSR6.OSTSTE bit is 1), the ICSRn.POEmF flag (n = 1, 3 to 5, 7; m = 0, 8, 10, 11, 12) additionally selected in the POECR4 register, and the POECMPFR.CnFLAG flag (n = 0 to 3).
When setting this bit to 1, set the POECR2.MTU7BDZE bit to 0. When the POECR2.MTU7BDZE bit is 1, the setting of the bit is ignored.

MTU7CME Bit (MTIOC7C Pin Port Mode Mask Enable)

This bit specifies whether switching the MTIOC7C pin to the general I/O port when one of the following flags and bit is set to 1: the OCSR2.OSF2 flag, the ICSR2.POE4F flag, the SPOER.MTUCH67HIZ bit, the ICSR6.OSTSTF flag (when the ICSR6.OSTSTE bit is 1), the ICSRn.POEmF flag (n = 1, 3 to 5, 7; m = 0, 8, 10, 11, 12) additionally selected in the POECR4 register, and the POECMPFR.CnFLAG flag (n = 0 to 3).
When setting this bit to 1, set the POECR2.MTU7ACZE bit to 0. When the POECR2.MTU7ACZE bit is 1, the setting of the bit is ignored.

MTU6DME Bit (MTIOC6D Pin Port Mode Mask Enable)

This bit specifies whether switching the MTIOC6D pin to the general I/O port when one of the following flags and bit is set to 1: the OCSR2.OSF2 flag, the ICSR2.POE4F flag, the SPOER.MTUCH67HIZ bit, the ICSR6.OSTSTF flag (when the ICSR6.OSTSTE bit is 1), the ICSRn.POEmF flag (n = 1, 3 to 5, 7; m = 0, 8, 10, 11, 12) additionally selected in the POECR4 register, and the POECMPFR.CnFLAG flag (n = 0 to 3).
When setting this bit to 1, set the POECR2.MTU6BDZE bit to 0. When the POECR2.MTU6BDZE bit is 1, the setting of the bit is ignored.

MTU4BME Bit (MTIOC4B/GTIOC2A (P73) Pin Port Mode Mask Enable)

This bit specifies whether switching the MTIOC4B/GTIOC2A pin of P73 to the general I/O port when one of the following flags and bit is set to 1: the OCSR1.OSF1 flag, the ICSR1.POE0F flag, the SPOER.MTUCH34HIZ bit, the ICSR6.OSTSTF flag (when the ICSR6.OSTSTE bit is 1), the ICSRn.POEmF flag (n = 2 to 5, 7; m = 4, 8, 10, 11, 12) additionally selected in the POECR4 register, and the POECMPFR.CnFLAG flag (n = 0 to 3).
When setting this bit to 1, set the POECR2.MTU4BDZE bit to 0. When the POECR2.MTU4BDZE bit is 1, the setting of the bit is ignored.

MTU4AME Bit (MTIOC4A/GTIOC1A (P72) Pin Port Mode Mask Enable)

This bit specifies whether switching the MTIOC4A/GTIOC1A pin of P72 to the general I/O port when one of the following flags and bit is set to 1: the OCSR1.OSF1 flag, the ICSR1.POE0F flag, the SPOER.MTUCH34HIZ bit, the ICSR6.OSTSTF flag (when the ICSR6.OSTSTE bit is 1), the ICSRn.POEmF flag (n = 2 to 5, 7; m = 4, 8, 10, 11, 12)

additionally selected in the POECR4 register, and the POECMPFR.CnFLAG flag (n = 0 to 3).
When setting this bit to 1, set the POECR2.MTU4ACZE bit to 0. When the POECR2.MTU4ACZE bit is 1, the setting of the bit is ignored.

MTU3BME Bit (MTIOC3B/GTIOC0A (P71) Pin Port Mode Mask Enable)

This bit specifies whether switching the MTIOC3B/GTIOC0A pin of P71 to the general I/O port when one of the following flags and bit is set to 1: the OCSR1.OSF1 flag, the ICSR1.POE0F flag, the SPOER.MTUCH34HIZ bit, the ICSR6.OSTSTF flag (when the ICSR6.OSTSTE bit is 1), the ICSRn.POEmF flag (n = 2 to 5, 7; m = 4, 8, 10, 11, 12) additionally selected in the POECR4 register, and the POECMPFR.CnFLAG flag (n = 0 to 3).
When setting this bit to 1, set the POECR2.MTU3BDZE bit to 0. When the POECR2.MTU3BDZE bit is 1, the setting of the bit is ignored.

MTU4DME Bit (MTIOC4D/GTIOC2B (P76) Pin Port Mode Mask Enable)

This bit specifies whether switching the MTIOC4D/GTIOC2B pin of P76 to the general I/O port when one of the following flags and bit is set to 1: the OCSR1.OSF1 flag, the ICSR1.POE0F flag, the SPOER.MTUCH34HIZ bit, the ICSR6.OSTSTF flag (when the ICSR6.OSTSTE bit is 1), the ICSRn.POEmF flag (n = 2 to 5, 7; m = 4, 8, 10, 11, 12) additionally selected in the POECR4 register, and the POECMPFR.CnFLAG flag (n = 0 to 3).
When setting this bit to 1, set the POECR2.MTU4BDZE bit to 0. When the POECR2.MTU4BDZE bit is 1, the setting of the bit is ignored.

MTU4CME Bit (MTIOC4C/GTIOC1B (P75) Pin Port Mode Mask Enable)

This bit specifies whether switching the MTIOC4C/GTIOC1B pin of P75 to the general I/O port when one of the following flags and bit is set to 1: the OCSR1.OSF1 flag, the ICSR1.POE0F flag, the SPOER.MTUCH34HIZ bit, the ICSR6.OSTSTF flag (when the ICSR6.OSTSTE bit is 1), the ICSRn.POEmF flag (n = 2 to 5, 7; m = 4, 8, 10, 11, 12) additionally selected in the POECR4 register, and the POECMPFR.CnFLAG flag (n = 0 to 3).
When setting this bit to 1, set the POECR2.MTU4ACZE bit to 0. When the POECR2.MTU4ACZE bit is 1, the setting of the bit is ignored.

MTU3DME Bit (MTIOC3D/GTIOC0B (P74) Pin Port Mode Mask Enable)

This bit specifies whether switching the MTIOC3D/GTIOC0B pin of P74 to the general I/O port when one of the following flags and bit is set to 1: the OCSR1.OSF1 flag, the ICSR1.POE0F flag, the SPOER.MTUCH34HIZ bit, the ICSR6.OSTSTF flag (when the ICSR6.OSTSTE bit is 1), the ICSRn.POEmF flag (n = 2 to 5, 7; m = 4, 8, 10, 11, 12) additionally selected in the POECR4 register, and the POECMPFR.CnFLAG flag (n = 0 to 3).
When setting this bit to 1, set the POECR2.MTU3BDZE bit to 0. When the POECR2.MTU3BDZE bit is 1, the setting of the bit is ignored.

21.2.25 Port Mode Mask Control Register 2 (PMMCR2)

Address(es): 0008 C4F4h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	GPT3B 1ME	GPT3A 1ME	GPT2B 1ME	GPT2A 1ME	GPT1B 1ME	GPT1A 1ME	GPT0B 1ME	GPT0A 1ME	—	—	GPT2B ME	GPT2A ME	GPT1B ME	GPT1A ME	GPT0B ME	GPT0A ME
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	GPT0AME	GTIOC0A/MTIOC3B (P12) Pin Port Mode Mask Enable	0: Switching to the general I/O port pin is disabled. 1: Switching to the general I/O port pin is enabled.	R/W*1
b1	GPT0BME	GTIOC0B/MTIOC3D (P15) Pin Port Mode Mask Enable	0: Switching to the general I/O port pin is disabled. 1: Switching to the general I/O port pin is enabled.	R/W*1
b2	GPT1AME	GTIOC1A/MTIOC4A (P13) Pin Port Mode Mask Enable	0: Switching to the general I/O port pin is disabled. 1: Switching to the general I/O port pin is enabled.	R/W*1
b3	GPT1BME	GTIOC1B/MTIOC4C (P16) Pin Port Mode Mask Enable	0: Switching to the general I/O port pin is disabled. 1: Switching to the general I/O port pin is enabled.	R/W*1
b4	GPT2AME	GTIOC2A/MTIOC4B (P14) Pin Port Mode Mask Enable	0: Switching to the general I/O port pin is disabled. 1: Switching to the general I/O port pin is enabled.	R/W*1
b5	GPT2BME	GTIOC2B/MTIOC4D (P17) Pin Port Mode Mask Enable	0: Switching to the general I/O port pin is disabled. 1: Switching to the general I/O port pin is enabled.	R/W*1
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	GPT0A1ME	GTIOC0A (PD2) Pin Port Mode Mask Enable	0: Switching to the general I/O port pin is disabled. 1: Switching to the general I/O port pin is enabled.	R/W*1
b9	GPT0B1ME	GTIOC0B (PD1) Pin Port Mode Mask Enable	0: Switching to the general I/O port pin is disabled. 1: Switching to the general I/O port pin is enabled.	R/W*1
b10	GPT1A1ME	GTIOC1A (PD0) Pin Port Mode Mask Enable	0: Switching to the general I/O port pin is disabled. 1: Switching to the general I/O port pin is enabled.	R/W*1
b11	GPT1B1ME	GTIOC1B (PB7) Pin Port Mode Mask Enable	0: Switching to the general I/O port pin is disabled. 1: Switching to the general I/O port pin is enabled.	R/W*1
b12	GPT2A1ME	GTIOC2A (PB6) Pin Port Mode Mask Enable	0: Switching to the general I/O port pin is disabled. 1: Switching to the general I/O port pin is enabled.	R/W*1
b13	GPT2B1ME	GTIOC2B (PB5) Pin Port Mode Mask Enable	0: Switching to the general I/O port pin is disabled. 1: Switching to the general I/O port pin is enabled.	R/W*1
b14	GPT3A1ME	GTIOC3A/MTIOC9A (PD7) Pin Port Mode Mask Enable	0: Switching to the general I/O port pin is disabled. 1: Switching to the general I/O port pin is enabled.	R/W*1
b15	GPT3B1ME	GTIOC3B/MTIOC9C (PD6) Pin Port Mode Mask Enable	0: Switching to the general I/O port pin is disabled. 1: Switching to the general I/O port pin is enabled.	R/W*1

Note 1. Can be modified only once after a reset.

The PMMCR2 register is used to mask the settings of the PMR register related to the GPT output pins (GPT0 to GPT2) or MTU complementary PWM output pins (MTU3, MTU4, MTU6, MTU7) of P12 to P17, and GPT output pins (GPT0 to GPT3) of PB5 to PB7, PD0 to PD2, and PD6 to PD7.

GPT0AME Bit (GTIOC0A/MTIOC3B (P12) Pin Port Mode Mask Enable)

This bit specifies whether switching the GTIOC0A/MTIOC3B pin of P12 to the general I/O port when one of the following flags and bit is set to 1: the OCSR3.OSF3 flag, the ICSR4.POE10F flag, the SPOER.GPT02HIZ bit, the ICSR6.OSTSTF flag (when the ICSR6.OSTSTE bit is 1), the ICSRn.POEmF flag (n = 1 to 3, 5, 7; m = 0, 4, 8, 11, 12) additionally selected in the POECR6 register.

When setting this bit to 1, set the POECR3.GPT0AZE bit to 0. When the POECR3.GPT0AZE bit is 1, the setting of the bit is ignored.

GPT0BME Bit (GTIOC0B/MTIOC3D (P15) Pin Port Mode Mask Enable)

This bit specifies whether switching the GTIOC0B/MTIOC3D pin of P15 to the general I/O port when one of the following flags and bit is set to 1: the OCSR3.OSF3 flag, the ICSR4.POE10F flag, the SPOER.GPT02HIZ bit, the ICSR6.OSTSTF flag (when the ICSR6.OSTSTE bit is 1), the ICSRn.POEmF flag (n = 1 to 3, 5, 7; m = 0, 4, 8, 11, 12) additionally selected in the POECR6 register.
When setting this bit to 1, set the POECR3.GPT0BZE bit to 0. When the POECR3.GPT0BZE bit is 1, the setting of the bit is ignored.

GPT1AME Bit (GTIOC1A/MTIOC4A (P13) Pin Port Mode Mask Enable)

This bit specifies whether switching the GTIOC1A/MTIOC4A pin of P13 to the general I/O port when one of the following flags and bit is set to 1: the OCSR3.OSF3 flag, the ICSR4.POE10F flag, the SPOER.GPT02HIZ bit, the ICSR6.OSTSTF flag (when the ICSR6.OSTSTE bit is 1), the ICSRn.POEmF flag (n = 1 to 3, 5, 7; m = 0, 4, 8, 11, 12) additionally selected in the POECR6 register.
When setting this bit to 1, set the POECR3.GPT1AZE bit to 0. When the POECR3.GPT1AZE bit is 1, the setting of the bit is ignored.

GPT1BME Bit (GTIOC1B/MTIOC4C (P16) Pin Port Mode Mask Enable)

This bit specifies whether switching the GTIOC1B/MTIOC4C pin of P16 to the general I/O port when one of the following flags and bit is set to 1: the OCSR3.OSF3 flag, the ICSR4.POE10F flag, the SPOER.GPT02HIZ bit, the ICSR6.OSTSTF flag (when the ICSR6.OSTSTE bit is 1), the ICSRn.POEmF flag (n = 1 to 3, 5, 7; m = 0, 4, 8, 11, 12) additionally selected in the POECR6 register.
When setting this bit to 1, set the POECR3.GPT1BZE bit to 0. When the POECR3.GPT1BZE bit is 1, the setting of the bit is ignored.

GPT2AME Bit (GTIOC2A/MTIOC4B (P14) Pin Port Mode Mask Enable)

This bit specifies whether switching the GTIOC2A/MTIOC4B pin of P14 to the general I/O port when one of the following flags and bit is set to 1: the OCSR3.OSF3 flag, the ICSR4.POE10F flag, the SPOER.GPT02HIZ bit, the ICSR6.OSTSTF flag (when the ICSR6.OSTSTE bit is 1), the ICSRn.POEmF flag (n = 1 to 3, 5, 7; m = 0, 4, 8, 11, 12) additionally selected in the POECR6 register.
When setting this bit to 1, set the POECR3.GPT2AZE bit to 0. When the POECR3.GPT2AZE bit is 1, the setting of the bit is ignored.

GPT2BME Bit (GTIOC2B/MTIOC4D (P17) Pin Port Mode Mask Enable)

This bit specifies whether switching the GTIOC2B/MTIOC4D pin of P17 to the general I/O port when one of the following flags and bit is set to 1: the OCSR3.OSF3 flag, the ICSR4.POE10F flag, the SPOER.GPT02HIZ bit, the ICSR6.OSTSTF flag (when the ICSR6.OSTSTE bit is 1), the ICSRn.POEmF flag (n = 1 to 3, 5, 7; m = 0, 4, 8, 11, 12) additionally selected in the POECR6 register.
When setting this bit to 1, set the POECR3.GPT2BZE bit to 0. When the POECR3.GPT2BZE bit is 1, the setting of the bit is ignored.

GPT0A1ME Bit (GTIOC0A (PD2) Pin Port Mode Mask Enable)

This bit specifies whether switching the GTIOC0A pin of PD2 to the general I/O port when one of the following flags and bit is set to 1: the ICSR5.POE11F flag, the SPOER.GPT03HIZ bit, the ICSR6.OSTSTF flag (when the ICSR6.OSTSTE bit is 1), the ICSRn.POEmF flag (n = 1 to 4, 7; m = 0, 4, 8, 10, 12) additionally selected in the POECR6 register.
When setting this bit to 1, set the POECR3.GPT0A1ZE bit to 0. When the POECR3.GPT0A1ZE bit is 1, the setting of the bit is ignored.

GPT0B1ME Bit (GTIOC0B (PD1) Pin Port Mode Mask Enable)

This bit specifies whether switching the GTIOC0B pin of PD1 to the general I/O port when one of the following flags and bit is set to 1: the ICSR5.POE11F flag, the SPOER.GPT03HIZ bit, the ICSR6.OSTSTF flag (when the ICSR6.OSTSTE bit is 1), the ICSRn.POEmF flag (n = 1 to 4, 7; m = 0, 4, 8, 10, 12) additionally selected in the POECR6 register.

When setting this bit to 1, set the POECR3.GPT0B1ZE bit to 0. When the POECR3.GPT0B1ZE bit is 1, the setting of the bit is ignored.

GPT1A1ME Bit (GTIOC1A (PD0) Pin Port Mode Mask Enable)

This bit specifies whether switching the GTIOC1A pin of PD0 to the general I/O port when one of the following flags and bit is set to 1: the ICSR5.POE11F flag, the SPOER.GPT03HIZ bit, the ICSR6.OSTSTF flag (when the ICSR6.OSTSTE bit is 1), the ICSRn.POEmF flag (n = 1 to 4, 7; m = 0, 4, 8, 10, 12) additionally selected in the POECR6 register.

When setting this bit to 1, set the POECR3.GPT1A1ZE bit to 0. When the POECR3.GPT1A1ZE bit is 1, the setting of the bit is ignored.

GPT1B1ME Bit (GTIOC1B (PB7) Pin Port Mode Mask Enable)

This bit specifies whether switching the GTIOC1B pin of PB7 to the general I/O port when one of the following flags and bit is set to 1: the ICSR5.POE11F flag, the SPOER.GPT03HIZ bit, the ICSR6.OSTSTF flag (when the ICSR6.OSTSTE bit is 1), the ICSRn.POEmF flag (n = 1 to 4, 7; m = 0, 4, 8, 10, 12) additionally selected in the POECR6 register.

When setting this bit to 1, set the POECR3.GPT1B1ZE bit to 0. When the POECR3.GPT1B1ZE bit is 1, the setting of the bit is ignored.

GPT2A1ME Bit (GTIOC2A (PB6) Pin Port Mode Mask Enable)

This bit specifies whether switching the GTIOC2A pin of PB6 to the general I/O port when one of the following flags and bit is set to 1: the ICSR5.POE11F flag, the SPOER.GPT03HIZ bit, the ICSR6.OSTSTF flag (when the ICSR6.OSTSTE bit is 1), the ICSRn.POEmF flag (n = 1 to 4, 7; m = 0, 4, 8, 10, 12) additionally selected in the POECR6 register.

When setting this bit to 1, set the POECR3.GPT2A1ZE bit to 0. When the POECR3.GPT2A1ZE bit is 1, the setting of the bit is ignored.

GPT2B1ME Bit (GTIOC2B (PB5) Pin Port Mode Mask Enable)

This bit specifies whether switching the GTIOC2B pin of PB5 to the general I/O port when one of the following flags and bit is set to 1: the ICSR5.POE11F flag, the SPOER.GPT03HIZ bit, the ICSR6.OSTSTF flag (when the ICSR6.OSTSTE bit is 1), the ICSRn.POEmF flag (n = 1 to 4, 7; m = 0, 4, 8, 10, 12) additionally selected in the POECR6 register.

When setting this bit to 1, set the POECR3.GPT2B1ZE bit to 0. When the POECR3.GPT2B1ZE bit is 1, the setting of the bit is ignored.

GPT3A1ME Bit (GTIOC3A/MTIOC9A (PD7) Pin Port Mode Mask Enable)

This bit specifies whether switching the GTIOC3A/MTIOC9A pin of PD7 to the general I/O port when one of the following flags and bit is set to 1: the ICSR5.POE11F flag, the SPOER.GPT03HIZ bit, the ICSR6.OSTSTF flag (when the ICSR6.OSTSTE bit is 1), the ICSRn.POEmF flag (n = 1 to 4, 7; m = 0, 4, 8, 10, 12) additionally selected in the POECR6 register.

When setting this bit to 1, set the POECR3.GPT3A1ZE bit to 0. When the POECR3.GPT3A1ZE bit is 1, the setting of the bit is ignored.

GPT3B1ME Bit (GTIOC3B/MTIOC9C (PD6) Pin Port Mode Mask Enable)

This bit specifies whether switching the GTIOC3B/MTIOC9C pin of PD6 to the general I/O port when one of the following flags and bit is set to 1: the ICSR5.POE11F flag, the SPOER.GPT03HIZ bit, the ICSR6.OSTSTF flag (when the ICSR6.OSTSTE bit is 1), the ICSRn.POEmF flag (n = 1 to 4, 7; m = 0, 4, 8, 10, 12) additionally selected in the POECR6 register.

When setting this bit to 1, set the POECR3.GPT3B1ZE bit to 0. When the POECR3.GPT3B1ZE bit is 1, the setting of the bit is ignored.

21.2.26 Port Mode Mask Control Register 3 (PMMCR3)

Address(es): 0008 C4F6h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	MTU9C2ME	—	MTU9A2ME	MTU9D1ME	MTU9C1ME	MTU9B1ME	MTU9A1ME	MTU9DME	MTU9CME	MTU9BME	MTU9AME
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	MTU9AME	MTIOC9A/GTIOC3A (PD7) Pin Port Mode Mask Enable	0: Switching to the general I/O port pin is disabled. 1: Switching to the general I/O port pin is enabled.	R/W*1
b1	MTU9BME	MTIOC9B (PE0) Pin Port Mode Mask Enable	0: Switching to the general I/O port pin is disabled. 1: Switching to the general I/O port pin is enabled.	R/W*1
b2	MTU9CME	MTIOC9C/GTIOC3B (PD6) Pin Port Mode Mask Enable	0: Switching to the general I/O port pin is disabled. 1: Switching to the general I/O port pin is enabled.	R/W*1
b3	MTU9DME	MTIOC9D (PE1) Pin Port Mode Mask Enable	0: Switching to the general I/O port pin is disabled. 1: Switching to the general I/O port pin is enabled.	R/W*1
b4	MTU9A1ME	MTIOC9A (P21) Pin Port Mode Mask Enable	0: Switching to the general I/O port pin is disabled. 1: Switching to the general I/O port pin is enabled.	R/W*1
b5	MTU9B1ME	MTIOC9B (P10) Pin Port Mode Mask Enable	0: Switching to the general I/O port pin is disabled. 1: Switching to the general I/O port pin is enabled.	R/W*1
b6	MTU9C1ME	MTIOC9C (P20) Pin Port Mode Mask Enable	0: Switching to the general I/O port pin is disabled. 1: Switching to the general I/O port pin is enabled.	R/W*1
b7	MTU9D1ME	MTIOC9D (P02) Pin Port Mode Mask Enable	0: Switching to the general I/O port pin is disabled. 1: Switching to the general I/O port pin is enabled.	R/W*1
b8	MTU9A2ME	MTIOC9A (P26) Pin Port Mode Mask Enable	0: Switching to the general I/O port pin is disabled. 1: Switching to the general I/O port pin is enabled.	R/W*1
b9	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b10	MTU9C2ME	MTIOC9C (P25) Pin Port Mode Mask Enable	0: Switching to the general I/O port pin is disabled. 1: Switching to the general I/O port pin is enabled.	R/W*1
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset.

The PMMCR3 register is used to mask the settings of the PMR register related to the MTU9 pin.

MTU9AME Bit (MTIOC9A/GTIOC3A (PD7) Pin Port Mode Mask Enable)

This bit specifies whether switching the MTIOC9A/GTIOC3A pin of PD7 to the general I/O port when one of the following flags and bit is set to 1: the ICSR7.POE12F flag, the SPOER.MTUCH9HIZ bit, the ICSR6.OSTSTF flag (when the ICSR6.OSTSTE bit is 1), the ICSRn.POEmF flag (n = 1 to 5; m = 0, 4, 8, 10, 11) additionally selected in the POECR8 register, and the POECMPFR.CnFLAG flag (n = 0 to 3).
When setting this bit to 1, set the POECR7.MTU9AZE bit to 0. When the POECR7.MTU9AZE bit is 1, the setting of the bit is ignored.

MTU9BME Bit (MTIOC9B (PE0) Pin Port Mode Mask Enable)

This bit specifies whether switching the MTIOC9B pin of PE0 to the general I/O port when one of the following flags and bit is set to 1: the ICSR7.POE12F flag, the SPOER.MTUCH9HIZ bit, the ICSR6.OSTSTF flag (when the ICSR6.OSTSTE bit is 1), the ICSRn.POEmF flag (n = 1 to 5; m = 0, 4, 8, 10, 11) additionally selected in the POECR8 register, and the POECMPFR.CnFLAG flag (n = 0 to 3).
When setting this bit to 1, set the POECR7.MTU9BZE bit to 0. When the POECR7.MTU9BZE bit is 1, the setting of the bit is ignored.

MTU9CME Bit (MTIOC9C/GTIOC3B (PD6) Pin Port Mode Mask Enable)

This bit specifies whether switching the MTIOC9C/GTIOC3B pin of PD6 to the general I/O port when one of the following flags and bit is set to 1: the ICSR7.POE12F flag, the SPOER.MTUCH9HIZ bit, the ICSR6.OSTSTF flag (when the ICSR6.OSTSTE bit is 1), the ICSRn.POEmF flag (n = 1 to 5; m = 0, 4, 8, 10, 11) additionally selected in the POECR8 register, and the POECMPFR.CnFLAG flag (n = 0 to 3).
When setting this bit to 1, set the POECR7.MTU9CZE bit to 0. When the POECR7.MTU9CZE bit is 1, the setting of the bit is ignored.

MTU9DME Bit (MTIOC9D (PE1) Pin Port Mode Mask Enable)

This bit specifies whether switching the MTIOC9D pin of PE1 to the general I/O port when one of the following flags and bit is set to 1: the ICSR7.POE12F flag, the SPOER.MTUCH9HIZ bit, the ICSR6.OSTSTF flag (when the ICSR6.OSTSTE bit is 1), the ICSRn.POEmF flag (n = 1 to 5; m = 0, 4, 8, 10, 11) additionally selected in the POECR8 register, and the POECMPFR.CnFLAG flag (n = 0 to 3).
When setting this bit to 1, set the POECR7.MTU9DZE bit to 0. When the POECR7.MTU9DZE bit is 1, the setting of the bit is ignored.

MTU9A1ME Bit (MTIOC9A (P21) Pin Port Mode Mask Enable)

This bit specifies whether switching the MTIOC9A pin of P21 to the general I/O port when one of the following flags and bit is set to 1: the ICSR7.POE12F flag, the SPOER.MTUCH9HIZ bit, the ICSR6.OSTSTF flag (when the ICSR6.OSTSTE bit is 1), the ICSRn.POEmF flag (n = 1 to 5; m = 0, 4, 8, 10, 11) additionally selected in the POECR8 register, and the POECMPFR.CnFLAG flag (n = 0 to 3).
When setting this bit to 1, set the POECR7.MTU9A1ZE bit to 0. When the POECR7.MTU9A1ZE bit is 1, the setting of the bit is ignored.

MTU9B1ME Bit (MTIOC9B (P10) Pin Port Mode Mask Enable)

This bit specifies whether switching the MTIOC9B pin of P10 to the general I/O port when one of the following flags and bit is set to 1: the ICSR7.POE12F flag, the SPOER.MTUCH9HIZ bit, the ICSR6.OSTSTF flag (when the ICSR6.OSTSTE bit is 1), the ICSRn.POEmF flag (n = 1 to 5; m = 0, 4, 8, 10, 11) additionally selected in the POECR8 register, and the POECMPFR.CnFLAG flag (n = 0 to 3).
When setting this bit to 1, set the POECR7.MTU9B1ZE bit to 0. When the POECR7.MTU9B1ZE bit is 1, the setting of the bit is ignored.

MTU9C1ME Bit (MTIOC9C (P20) Pin Port Mode Mask Enable)

This bit specifies whether switching the MTIOC9C pin of P20 to the general I/O port when one of the following flags and bit is set to 1: the ICSR7.POE12F flag, the SPOER.MTUCH9HIZ bit, the ICSR6.OSTSTF flag (when the ICSR6.OSTSTE bit is 1), the ICSRn.POEmF flag (n = 1 to 5; m = 0, 4, 8, 10, 11) additionally selected in the POECR8 register, and the POECMPFR.CnFLAG flag (n = 0 to 3).
When setting this bit to 1, set the POECR7.MTU9C1ZE bit to 0. When the POECR7.MTU9C1ZE bit is 1, the setting of the bit is ignored.

MTU9D1ME Bit (MTIOC9D (P02) Pin Port Mode Mask Enable)

This bit specifies whether switching the MTIOC9D pin of P02 to the general I/O port when one of the following flags and bit is set to 1: the ICSR7.POE12F flag, the SPOER.MTUCH9HIZ bit, the ICSR6.OSTSTF flag (when the ICSR6.OSTSTE bit is 1), the ICSRn.POEmF flag (n = 1 to 5; m = 0, 4, 8, 10, 11) additionally selected in the POECR8 register, and the POECMPFR.CnFLAG flag (n = 0 to 3).
When setting this bit to 1, set the POECR7.MTU9D1ZE bit to 0. When the POECR7.MTU9D1ZE bit is 1, the setting of the bit is ignored.

MTU9A2ME Bit (MTIOC9A (P26) Pin Port Mode Mask Enable)

This bit specifies whether switching the MTIOC9A pin of P26 to the general I/O port when one of the following flags and bit is set to 1: the ICSR7.POE12F flag, the SPOER.MTUCH9HIZ bit, the ICSR6.OSTSTF flag (when the ICSR6.OSTSTE bit is 1), the ICSRn.POEmF flag (n = 1 to 5; m = 0, 4, 8, 10, 11) additionally selected in the POECR8 register, and the POECMPFR.CnFLAG flag (n = 0 to 3).

When setting this bit to 1, set the POECR7.MTU9A2ZE bit to 0. When the POECR7.MTU9A2ZE bit is 1, the setting of the bit is ignored.

MTU9C2ME Bit (MTIOC9C (P25) Pin Port Mode Mask Enable)

This bit specifies whether switching the MTIOC9C pin of P25 to the general I/O port when one of the following flags and bit is set to 1: the ICSR7.POE12F flag, the SPOER.MTUCH9HIZ bit, the ICSR6.OSTSTF flag (when the ICSR6.OSTSTE bit is 1), the ICSRn.POEmF flag (n = 1 to 5; m = 0, 4, 8, 10, 11) additionally selected in the POECR8 register, and the POECMPFR.CnFLAG flag (n = 0 to 3).

When setting this bit to 1, set the POECR7.MTU9C2ZE bit to 0. When the POECR7.MTU9C2ZE bit is 1, the setting of the bit is ignored.

21.2.27 Port Output Enable Comparator Output Detection Flag Register (POECMPFR)

Address(es): 0008 C4E6h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	C3FLAG	C2FLAG	C1FLAG	C0FLAG
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	C0FLAG	Comparator Channel 0 Output Detection Flag	0: Comparator output not detected 1: Comparator output detected	R/(W)*1
b1	C1FLAG	Comparator Channel 1 Output Detection Flag	0: Comparator output not detected 1: Comparator output detected	R/(W)*1
b2	C2FLAG	Comparator Channel 2 Output Detection Flag	0: Comparator output not detected 1: Comparator output detected	R/(W)*1
b3	C3FLAG	Comparator Channel 3 Output Detection Flag	0: Comparator output not detected 1: Comparator output detected	R/(W)*1
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The flag can only be set to 0 by writing 0 after reading 1.

CnFLAG Flag (Comparator Channel n Output Detection Flag) (n = 0 to 3)

This flag indicates whether each comparator output is detected or not detected.

[Setting condition]

- A change from low level to high level in the comparator output is detected.
  - When the comparator is set to non-inverted output, the input voltage changes from lower to higher than the reference voltage
  - When the comparator is set to inverted output, the input voltage changes from higher to lower than the reference voltage

[Clearing condition]

- By writing 0 to the CnFLAG flag after reading CnFLAG = 1

21.2.28 Port Output Enable Comparator Request Select Register (POECMPSEL)

Address(es): 0008 C4E8h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	POEREQ3	POEREQ2	POEREQ1	POEREQ0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	POEREQ0	Comparator Channel 0 Output Disabling Request Enable	0: Disables output disabling request generation upon comparator output detection. 1: Enables output disabling request generation upon comparator output detection.	R/W*1
b1	POEREQ1	Comparator Channel 1 Output Disabling Request Enable	0: Disables output disabling request generation upon comparator output detection. 1: Enables output disabling request generation upon comparator output detection.	R/W*1
b2	POEREQ2	Comparator Channel 2 Output Disabling Request Enable	0: Disables output disabling request generation upon comparator output detection. 1: Enables output disabling request generation upon comparator output detection.	R/W*1
b3	POEREQ3	Comparator Channel 3 Output Disabling Request Enable	0: Disables output disabling request generation upon comparator output detection. 1: Enables output disabling request generation upon comparator output detection.	R/W*1
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset.

The POECMPSEL register sets a comparator output detection flag to use as a control condition to disable the outputs.

POEREQn Bit (Comparator Channel n Output Disabling Request Enable) (n = 0 to 3)

This bit disables or enables output disabling request generation in response to each comparator output detection. An output disabling request is generated when one of the comparator outputs is detected.

21.2.29 Port Output Enable Comparator Request Extended Selection Register m (POECMPEXm) (m = 0 to 5)

Address(es): POE.POECMPEX0 0008 C4F8h, POE.POECMPEX1 0008 C4F9h, POE.POECMPEX2 0008 C4FAh, POE.POECMPEX3 0008 C4FBh, POE.POECMPEX4 0008 C4FCh, POE.POECMPEX5 0008 C4FDh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	POEREQ3	POEREQ2	POEREQ1	POEREQ0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	POEREQ0	Comparator Channel 0 Output Disabling Request Enable	0: Disables output disabling request generation upon comparator output detection. 1: Enables output disabling request generation upon comparator output detection.	R/W *1
b1	POEREQ1	Comparator Channel 1 Output Disabling Request Enable	0: Disables output disabling request generation upon comparator output detection. 1: Enables output disabling request generation upon comparator output detection.	R/W *1
b2	POEREQ2	Comparator Channel 2 Output Disabling Request Enable	0: Disables output disabling request generation upon comparator output detection. 1: Enables output disabling request generation upon comparator output detection.	R/W *1
b3	POEREQ3	Comparator Channel 3 Output Disabling Request Enable	0: Disables output disabling request generation upon comparator output detection. 1: Enables output disabling request generation upon comparator output detection.	R/W *1
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset.

The POECMPEXm register specifies the comparator output detection flag to use as a control condition to disable the outputs.
The register can select a source for each output pin group whereas the POECMPSEL register selects the source for all pins. Table 21.4 lists the output pin groups and the corresponding POECMPEXm registers.

Table 21.4 Output Pin Groups and Corresponding POECMPEXm Registers

Output Pin Group	Corresponding POECMPEXm Register	Corresponding CFLAG add bit
MTU3, MTU4, GPT0 to GPT2 (P71 to P76)	POECMPEX0	POECR4.CMADDMT34ZE
MTU6, MTU7 (P90 to P95)	POECMPEX1	POECR4,CMADDMT67ZE
MTU0 (PB0 to PB3, P30, P31)	POECMPEX2	POECR5.CMADDMT0ZE
MTU3, MTU4, GPT0 to GPT2 (P12 to P17)	POECMPEX3	POECR6.CMADDGPT02ZE
GPT0 to GPT3 (PB5 to PB7, PD0 to PD2, PD6, PD7)	POECMPEX4	POECR6.CMADDGPT03ZE
MTU9 (P02, P10, P20, P21, P25, P26, PD6, PD7, PE0, PE1)	POECMPEX5	POECR8.CMADDMT9ZE

POEREQn Bit (Comparator Channel n Output Disabling Request Enable) (n = 0 to 3)

This bit disables or enables output disabling request generation in response to each comparator output detection. An output disabling request is generated when one of the comparator outputs is detected.

21.3 Operation

The following shows the target pins and conditions for output disabling control.

(1) MTU3 pins or GPT0 pins P71 and P74 (MTIOC3B/GTIOC0A, MTIOC3D/GTIOC0B)

When one of the following conditions is satisfied while the POECR2.MTU3BDZE bit is 1, the pins become high-impedance. Furthermore, when the POECR2.MTU3BDZE bit is 0 and the PMMCR1.MTU3BME and MTU3DME bits are 1 and when one of the following conditions is satisfied, the pins are switched to general I/O port pins.

- Operation for detection of the POE0# input level
  When the ICSR1.POE0F flag becomes 1.
- Operation for comparison of the output levels on the MTIOC3B and MTIOC3D or GTIOC0A and GTIOC0B pins
  When the OCSR1.OSF1 flag becomes 1 while the OCSR1.OCE1 bit is 1.
- SPOER setting
  When the SPOER.MTUCH34HIZ bit is set to 1.
- Conditions added by POECR4
  When the ICSR2.POE4F flag becomes 1 while the POECR4.IC2ADDMT34ZE bit is 1.
  When the ICSR3.POE8F flag becomes 1 while the POECR4.IC3ADDMT34ZE bit and the ICSR3.POE8E bit are 1.
  When the ICSR4.POE10F flag becomes 1 while the POECR4.IC4ADDMT34ZE bit and the ICSR4.POE10E bit are 1.
  When the ICSR5.POE11F flag becomes 1 while the POECR4.IC5ADDMT34ZE bit and the ICSR5.POE11E bit are 1.
  When the ICSR7.POE12F flag becomes 1 while the POECR4.IC6ADDMT34ZE bit and the ICSR7.POE12E bit are 1.
- Comparator output detection
  When the POECMPFR.C0FLAG flag becomes 1 while the POECR4.CMADDMT34ZE bit is 1 and the POECMPEX0.POEREQ0 bit or the POECMPSEL.POEREQ0 bit is 1.
  When the POECMPFR.C1FLAG flag becomes 1 while the POECR4.CMADDMT34ZE bit is 1 and the POECMPEX0.POEREQ1 bit or the POECMPSEL.POEREQ1 bit is 1.
  When the POECMPFR.C2FLAG flag becomes 1 while the POECR4.CMADDMT34ZE bit is 1 and the POECMPEX0.POEREQ2 bit or the POECMPSEL.POEREQ2 bit is 1.
  When the POECMPFR.C3FLAG flag becomes 1 while the POECR4.CMADDMT34ZE bit is 1 and the POECMPEX0.POEREQ3 bit or the POECMPSEL.POEREQ3 bit is 1.
- Detection of oscillation stop
  When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(2) MTU4 pins or GPT1 pins P72 and P75 (MTIOC4A/GTIOC1A, MTIOC4C/GTIOC1B)

When one of the following conditions is satisfied while the POECR2.MTU4ACZE bit is 1, the pins become high-impedance. Furthermore, when the POECR2.MTU4ACZE bit is 0 and the PMMCR1.MTU4AME and MTU4CME bits are 1 and when one of the following conditions is satisfied, the pins are switched to general I/O port pins.

- Operation for detection of the POE0# input level
  When the ICSR1.POE0F flag becomes 1.
- Operation for comparison of the output levels on the MTIOC4A and MTIOC4C or GTIOC1A and GTIOC1B pins
  When the OCSR1.OSF1 flag becomes 1 while the OCSR1.OCE1 bit is 1.
- SPOER setting
  When the SPOER.MTUCH34HIZ bit is set to 1.
- Conditions added by POECR4
  When the ICSR2.POE4F flag becomes 1 while the POECR4.IC2ADDMT34ZE bit is 1.
  When the ICSR3.POE8F flag becomes 1 while the POECR4.IC3ADDMT34ZE bit and the ICSR3.POE8E bit are 1.
  When the ICSR4.POE10F flag becomes 1 while the POECR4.IC4ADDMT34ZE bit and the ICSR4.POE10E bit are

1.
When the ICSR5.POE11F flag becomes 1 while the POECR4.IC5ADDMT34ZE bit and the ICSR5.POE11E bit are 1.
When the ICSR7.POE12F flag becomes 1 while the POECR4.IC6ADDMT34ZE bit and the ICSR7.POE12E bit are 1.

- Comparator output detection
When the POECMPFR.C0FLAG flag becomes 1 while the POECR4.CMADDMT34ZE bit is 1 and the POECMPEX0.POEREQ0 bit or the POECMPSEL.POEREQ0 bit is 1.
When the POECMPFR.C1FLAG flag becomes 1 while the POECR4.CMADDMT34ZE bit is 1 and the POECMPEX0.POEREQ1 bit or the POECMPSEL.POEREQ1 bit is 1.
When the POECMPFR.C2FLAG flag becomes 1 while the POECR4.CMADDMT34ZE bit is 1 and the POECMPEX0.POEREQ2 bit or the POECMPSEL.POEREQ2 bit is 1.
When the POECMPFR.C3FLAG flag becomes 1 while the POECR4.CMADDMT34ZE bit is 1 and the POECMPEX0.POEREQ3 bit or the POECMPSEL.POEREQ3 bit is 1.
- Detection of oscillation stop
When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(3) MTU4 pins or GPT2 pins P73 and P76 (MTIOC4B/GTIOC2A, MTIOC4D/GTIOC2B)

When one of the following conditions is satisfied while the POECR2.MTU4BDZE bit is 1, the pins become high-impedance. Furthermore, when the POECR2.MTU4BDZE bit is 0 and the PMMCR1.MTU4BME and MTU4DME bits are 1 and when one of the following conditions is satisfied, the pins are switched to general I/O port pins.

- Operation for detection of the POE0# input level
When the ICSR1.POE0F flag becomes 1.
- Operation for comparison of the output levels on the MTIOC4B and MTIOC4D or GTIOC2A and GTIOC2B pins
When the OCSR1.OSF1 flag becomes 1 while the OCSR1.OCE1 bit is 1.
- SPOER setting
When the SPOER.MTUCH34HIZ bit is set to 1.
- Conditions added by POECR4
When the ICSR2.POE4F flag becomes 1 while the POECR4.IC2ADDMT34ZE bit is 1.
When the ICSR3.POE8F flag becomes 1 while the POECR4.IC3ADDMT34ZE bit and the ICSR3.POE8E bit are 1.
When the ICSR4.POE10F flag becomes 1 while the POECR4.IC4ADDMT34ZE bit and the ICSR4.POE10E bit are 1.
When the ICSR5.POE11F flag becomes 1 while the POECR4.IC5ADDMT34ZE bit and the ICSR5.POE11E bit are 1.
When the ICSR7.POE12F flag becomes 1 while the POECR4.IC6ADDMT34ZE bit and the ICSR7.POE12E bit are 1.
- Comparator output detection
When the POECMPFR.C0FLAG flag becomes 1 while the POECR4.CMADDMT34ZE bit is 1 and the POECMPEX0.POEREQ0 bit or the POECMPSEL.POEREQ0 bit is 1.
When the POECMPFR.C1FLAG flag becomes 1 while the POECR4.CMADDMT34ZE bit is 1 and the POECMPEX0.POEREQ1 bit or the POECMPSEL.POEREQ1 bit is 1.
When the POECMPFR.C2FLAG flag becomes 1 while the POECR4.CMADDMT34ZE bit is 1 and the POECMPEX0.POEREQ2 bit or the POECMPSEL.POEREQ2 bit is 1.
When the POECMPFR.C3FLAG flag becomes 1 while the POECR4.CMADDMT34ZE bit is 1 and the POECMPEX0.POEREQ3 bit or the POECMPSEL.POEREQ3 bit is 1.
- Detection of oscillation stop
When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(4) MTU6 pins (MTIOC6B, MTIOC6D)

When one of the following conditions is satisfied while the POECR2.MTU6BDZE bit is 1, the pins become high-impedance. Furthermore, when the POECR2.MTU6BDZE bit is 0 and the PMMCR1.MTU6BME and MTU6DME bits are 1 and when one of the following conditions is satisfied, the pins are switched to general I/O port pins.

- Operation for detection of the POE4# input level
  When the ICSR2.POE4F flag becomes 1.
- Operation for comparison of the output levels on the MTIOC6B and MTIOC6D pins
  When the OCSR2.OSF2 flag becomes 1 while the OCSR2.OCE2 bit is 1.
- SPOER setting
  When the SPOER.MTUCH67HIZ bit is set to 1.
- Conditions added by POECR4
  When the ICSR1.POE0F flag becomes 1 while the POECR4.IC1ADDMT67ZE bit is 1.
  When the ICSR3.POE8F flag becomes 1 while the POECR4.IC3ADDMT67ZE bit and the ICSR3.POE8E bit are 1.
  When the ICSR4.POE10F flag becomes 1 while the POECR4.IC4ADDMT67ZE bit and the ICSR4.POE10E bit are 1.
  When the ICSR5.POE11F flag becomes 1 while the POECR4.IC5ADDMT67ZE bit and the ICSR5.POE11E bit are 1.
  When the ICSR7.POE12F flag becomes 1 while the POECR4.IC6ADDMT67ZE bit and the ICSR7.POE12E bit are 1.
- Comparator output detection
  When the POECMPFR.C0FLAG flag becomes 1 while the POECR4.CMADDMT67ZE bit is 1 and the POECMPEX1.POEREQ0 bit or the POECMPSEL.POEREQ0 bit is 1.
  When the POECMPFR.C1FLAG flag becomes 1 while the POECR4.CMADDMT67ZE bit is 1 and the POECMPEX1.POEREQ1 bit or the POECMPSEL.POEREQ1 bit is 1.
  When the POECMPFR.C2FLAG flag becomes 1 while the POECR4.CMADDMT67ZE bit is 1 and the POECMPEX1.POEREQ2 bit or the POECMPSEL.POEREQ2 bit is 1.
  When the POECMPFR.C3FLAG flag becomes 1 while the POECR4.CMADDMT67ZE bit is 1 and the POECMPEX1.POEREQ3 bit or the POECMPSEL.POEREQ3 bit is 1.
- Detection of oscillation stop
  When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(5) MTU7 pins (MTIOC7A, MTIOC7C)

When one of the following conditions is satisfied while the POECR2.MTU7ACZE bit is 1, the pins become high-impedance. Furthermore, when the POECR2.MTU7ACZE bit is 0 and the PMMCR1.MTU7AME and MTU7CME bits are 1 and when one of the following conditions is satisfied, the pins are switched to general I/O port pins.

- Operation for detection of the POE4# input level
  When the ICSR2.POE4F flag becomes 1.
- Operation for comparison of the output levels on the MTIOC7A and MTIOC7C pins
  When the OCSR2.OSF2 flag becomes 1 while the OCSR2.OCE2 bit is 1.
- SPOER setting
  When the SPOER.MTUCH67HIZ bit is set to 1.
- Conditions added by POECR4
  When the ICSR1.POE0F flag becomes 1 while the POECR4.IC1ADDMT67ZE bit is 1.
  When the ICSR3.POE8F flag becomes 1 while the POECR4.IC3ADDMT67ZE bit and the ICSR3.POE8E bit are 1.
  When the ICSR4.POE10F flag becomes 1 while the POECR4.IC4ADDMT67ZE bit and the ICSR4.POE10E bit are 1.
  When the ICSR5.POE11F flag becomes 1 while the POECR4.IC5ADDMT67ZE bit and the ICSR5.POE11E bit are 1.

When the ICSR7.POE12F flag becomes 1 while the POECR4.IC6ADDMT67ZE bit and the ICSR7.POE12E bit are 1.

- Comparator output detection
  When the POECMPFR.C0FLAG flag becomes 1 while the POECR4.CMADDMT67ZE bit is 1 and the POECMPEX1.POEREQ0 bit or the POECMPSEL.POEREQ0 bit is 1.
  When the POECMPFR.C1FLAG flag becomes 1 while the POECR4.CMADDMT67ZE bit is 1 and the POECMPEX1.POEREQ1 bit or the POECMPSEL.POEREQ1 bit is 1.
  When the POECMPFR.C2FLAG flag becomes 1 while the POECR4.CMADDMT67ZE bit is 1 and the POECMPEX1.POEREQ2 bit or the POECMPSEL.POEREQ2 bit is 1.
  When the POECMPFR.C3FLAG flag becomes 1 while the POECR4.CMADDMT67ZE bit is 1 and the POECMPEX1.POEREQ3 bit or the POECMPSEL.POEREQ3 bit is 1.
- Detection of oscillation stop
  When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(6) MTU7 pins (MTIOC7B, MTIOC7D)

When one of the following conditions is satisfied while the POECR2.MTU7BDZE bit is 1, the pins become high-impedance. Furthermore, when the POECR2.MTU7BDZE bit is 0 and the PMMCR1.MTU7BME and MTU7DME bits are 1 and when one of the following conditions is satisfied, the pins are switched to general I/O port pins.

- Operation for detection of the POE4# input level
  When the ICSR2.POE4F flag becomes 1.
- Operation for comparison of the output levels on the MTIOC7B and MTIOC7D pins
  When the OCSR2.OSF2 flag becomes 1 while the OCSR2.OCE2 bit is 1.
- SPOER setting
  When the SPOER.MTUCH67HIZ bit is set to 1.
- Conditions added by POECR4
  When the ICSR1.POE0F flag becomes 1 while the POECR4.IC1ADDMT67ZE bit is 1.
  When the ICSR3.POE8F flag becomes 1 while the POECR4.IC3ADDMT67ZE bit and the ICSR3.POE8E bit are 1.
  When the ICSR4.POE10F flag becomes 1 while the POECR4.IC4ADDMT67ZE bit and the ICSR4.POE10E bit are 1.
  When the ICSR5.POE11F flag becomes 1 while the POECR4.IC5ADDMT67ZE bit and the ICSR5.POE11E bit are 1.
  When the ICSR7.POE12F flag becomes 1 while the POECR4.IC6ADDMT67ZE bit and the ICSR7.POE12E bit are 1.
- Comparator output detection
  When the POECMPFR.C0FLAG flag becomes 1 while the POECR4.CMADDMT67ZE bit is 1 and the POECMPEX1.POEREQ0 bit or the POECMPSEL.POEREQ0 bit is 1.
  When the POECMPFR.C1FLAG flag becomes 1 while the POECR4.CMADDMT67ZE bit is 1 and the POECMPEX1.POEREQ1 bit or the POECMPSEL.POEREQ1 bit is 1.
  When the POECMPFR.C2FLAG flag becomes 1 while the POECR4.CMADDMT67ZE bit is 1 and the POECMPEX1.POEREQ2 bit or the POECMPSEL.POEREQ2 bit is 1.
  When the POECMPFR.C3FLAG flag becomes 1 while the POECR4.CMADDMT67ZE bit is 1 and the POECMPEX1.POEREQ3 bit or the POECMPSEL.POEREQ3 bit is 1.
- Detection of oscillation stop
  When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(7) MTU0 pin PB3 (MTIOC0A)

When one of the following conditions is satisfied while the POECR1.MTU0AZE bit is 1, the pin becomes high-impedance. Furthermore, when the POECR1.MTU0AZE bit is 0 and the PMMCR1.MTU0AME bit is 1 and when one of

the following conditions is satisfied, the pin is switched to general I/O port pin.

- Operation for detection of the POE8# input level
  When the ICSR3.POE8F flag becomes 1 while the ICSR3.POE8E bit is 1.
- SPOER setting
  When the SPOER.MTUCH0HIZ bit is set to 1.
- Conditions added by POECR5
  When the ICSR1.POE0F flag becomes 1 while the POECR5.IC1ADDMT0ZE bit is 1.
  When the ICSR2.POE4F flag becomes 1 while the POECR5.IC2ADDMT0ZE bit is 1.
  When the ICSR4.POE10F flag becomes 1 while the POECR5.IC4ADDMT0ZE bit and the ICSR4.POE10E bit are 1.
  When the ICSR5.POE11F flag becomes 1 while the POECR5.IC5ADDMT0ZE bit and the ICSR5.POE11E bit are 1.
  When the ICSR7.POE12F flag becomes 1 while the POECR5.IC6ADDMT0ZE bit and the ICSR7.POE12E bit are 1.
- Comparator output detection
  When the POECMPFR.C0FLAG flag becomes 1 while the POECR5.CMADDMT0ZE bit is 1 and the POECMPEX2.POEREQ0 bit or the POECMPSEL.POEREQ0 bit is 1.
  When the POECMPFR.C1FLAG flag becomes 1 while the POECR5.CMADDMT0ZE bit is 1 and the POECMPEX2.POEREQ1 bit or the POECMPSEL.POEREQ1 bit is 1.
  When the POECMPFR.C2FLAG flag becomes 1 while the POECR5.CMADDMT0ZE bit is 1 and the POECMPEX2.POEREQ2 bit or the POECMPSEL.POEREQ2 bit is 1.
  When the POECMPFR.C3FLAG flag becomes 1 while the POECR5.CMADDMT0ZE bit is 1 and the POECMPEX2.POEREQ3 bit or the POECMPSEL.POEREQ3 bit is 1.
- Detection of oscillation stop
  When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(8) MTU0 pin P31 (MTIOC0A)

When one of the following conditions is satisfied while the POECR1.MTU0A1ZE bit is 1, the pin becomes high-impedance. Furthermore, when the POECR1.MTU0A1ZE bit is 0 and the PMMCR1.MTU0A1ME bit is 1 and when one of the following conditions is satisfied, the pin is switched to general I/O port pin.

- Operation for detection of the POE8# input level
  When the ICSR3.POE8F flag becomes 1 while the ICSR3.POE8E bit is 1.
- SPOER setting
  When the SPOER.MTUCH0HIZ bit is set to 1.
- Conditions added by POECR5
  When the ICSR1.POE0F flag becomes 1 while the POECR5.IC1ADDMT0ZE bit is 1.
  When the ICSR2.POE4F flag becomes 1 while the POECR5.IC2ADDMT0ZE bit is 1.
  When the ICSR4.POE10F flag becomes 1 while the POECR5.IC4ADDMT0ZE bit and the ICSR4.POE10E bit are 1.
  When the ICSR5.POE11F flag becomes 1 while the POECR5.IC5ADDMT0ZE bit and the ICSR5.POE11E bit are 1.
  When the ICSR7.POE12F flag becomes 1 while the POECR5.IC6ADDMT0ZE bit and the ICSR7.POE12E bit are 1.
- Comparator output detection
  When the POECMPFR.C0FLAG flag becomes 1 while the POECR5.CMADDMT0ZE bit is 1 and the POECMPEX2.POEREQ0 bit or the POECMPSEL.POEREQ0 bit is 1.
  When the POECMPFR.C1FLAG flag becomes 1 while the POECR5.CMADDMT0ZE bit is 1 and the POECMPEX2.POEREQ1 bit or the POECMPSEL.POEREQ1 bit is 1.

When the POECMPFR.C2FLAG flag becomes 1 while the POECR5.CMADDMT0ZE bit is 1 and the POECMPEX2.POEREQ2 bit or the POECMPSEL.POEREQ2 bit is 1.
When the POECMPFR.C3FLAG flag becomes 1 while the POECR5.CMADDMT0ZE bit is 1 and the POECMPEX2.POEREQ3 bit or the POECMPSEL.POEREQ3 bit is 1.

- Detection of oscillation stop
  When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(9) MTU0 pin PB2 (MTIOC0B)

When one of the following conditions is satisfied while the POECR1.MTU0BZE bit is 1, the pin becomes high-impedance. Furthermore, when the POECR1.MTU0BZE bit is 0 and the PMMCR1.MTU0BME bit is 1 and when one of the following conditions is satisfied, the pin is switched to general I/O port pin.

- Operation for detection of the POE8# input level
  When the ICSR3.POE8F flag becomes 1 while the ICSR3.POE8E bit is 1.
- SPOER setting
  When the SPOER.MTUCH0HIZ bit is set to 1.
- Conditions added by POECR5
  When the ICSR1.POE0F flag becomes 1 while the POECR5.IC1ADDMT0ZE bit is 1.
  When the ICSR2.POE4F flag becomes 1 while the POECR5.IC2ADDMT0ZE bit is 1.
  When the ICSR4.POE10F flag becomes 1 while the POECR5.IC4ADDMT0ZE bit and the ICSR4.POE10E bit are 1.
  When the ICSR5.POE11F flag becomes 1 while the POECR5.IC5ADDMT0ZE bit and the ICSR5.POE11E bit are 1.
  When the ICSR7.POE12F flag becomes 1 while the POECR5.IC6ADDMT0ZE bit and the ICSR7.POE12E bit are 1.
- Comparator output detection
  When the POECMPFR.C0FLAG flag becomes 1 while the POECR5.CMADDMT0ZE bit is 1 and the POECMPEX2.POEREQ0 bit or the POECMPSEL.POEREQ0 bit is 1.
  When the POECMPFR.C1FLAG flag becomes 1 while the POECR5.CMADDMT0ZE bit is 1 and the POECMPEX2.POEREQ1 bit or the POECMPSEL.POEREQ1 bit is 1.
  When the POECMPFR.C2FLAG flag becomes 1 while the POECR5.CMADDMT0ZE bit is 1 and the POECMPEX2.POEREQ2 bit or the POECMPSEL.POEREQ2 bit is 1.
  When the POECMPFR.C3FLAG flag becomes 1 while the POECR5.CMADDMT0ZE bit is 1 and the POECMPEX2.POEREQ3 bit or the POECMPSEL.POEREQ3 bit is 1.
- Detection of oscillation stop
  When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(10) MTU0 pin P30 (MTIOC0B)

When one of the following conditions is satisfied while the POECR1.MTU0B1ZE bit is 1, the pin becomes high-impedance. Furthermore, when the POECR1.MTU0B1ZE bit is 0 and the PMMCR1.MTU0B1ME bit is 1 and when one of the following conditions is satisfied, the pin is switched to general I/O port pin.

- Operation for detection of the POE8# input level
  When the ICSR3.POE8F flag becomes 1 while the ICSR3.POE8E bit is 1.
- SPOER setting
  When the SPOER.MTUCH0HIZ bit is set to 1.
- Conditions added by POECR5
  When the ICSR1.POE0F flag becomes 1 while the POECR5.IC1ADDMT0ZE bit is 1.
  When the ICSR2.POE4F flag becomes 1 while the POECR5.IC2ADDMT0ZE bit is 1.
  When the ICSR4.POE10F flag becomes 1 while the POECR5.IC4ADDMT0ZE bit and the ICSR4.POE10E bit are

1.
When the ICSR5.POE11F flag becomes 1 while the POECR5.IC5ADDMT0ZE bit and the ICSR5.POE11E bit are 1.
When the ICSR7.POE12F flag becomes 1 while the POECR5.IC6ADDMT0ZE bit and the ICSR7.POE12E bit are 1.

- Comparator output detection
When the POECMPFR.C0FLAG flag becomes 1 while the POECR5.CMADDMT0ZE bit is 1 and the POECMPEX2.POEREQ0 bit or the POECMPSEL.POEREQ0 bit is 1.
When the POECMPFR.C1FLAG flag becomes 1 while the POECR5.CMADDMT0ZE bit is 1 and the POECMPEX2.POEREQ1 bit or the POECMPSEL.POEREQ1 bit is 1.
When the POECMPFR.C2FLAG flag becomes 1 while the POECR5.CMADDMT0ZE bit is 1 and the POECMPEX2.POEREQ2 bit or the POECMPSEL.POEREQ2 bit is 1.
When the POECMPFR.C3FLAG flag becomes 1 while the POECR5.CMADDMT0ZE bit is 1 and the POECMPEX2.POEREQ3 bit or the POECMPSEL.POEREQ3 bit is 1.
- Detection of oscillation stop
When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(11) MTU0 pin (MTIOC0C)

When one of the following conditions is satisfied while the POECR1.MTU0CZE bit is 1, the pin becomes high-impedance. Furthermore, when the POECR1.MTU0CZE bit is 0 and the PMMCR1.MTU0CME bit is 1 and when one of the following conditions is satisfied, the pin is switched to general I/O port pin.

- Operation for detection of the POE8# input level
When the ICSR3.POE8F flag becomes 1 while the ICSR3.POE8E bit is 1.
- SPOER setting
When the SPOER.MTUCH0HIZ bit is set to 1.
- Conditions added by POECR5
When the ICSR1.POE0F flag becomes 1 while the POECR5.IC1ADDMT0ZE bit is 1.
When the ICSR2.POE4F flag becomes 1 while the POECR5.IC2ADDMT0ZE bit is 1.
When the ICSR4.POE10F flag becomes 1 while the POECR5.IC4ADDMT0ZE bit and the ICSR4.POE10E bit are 1.
When the ICSR5.POE11F flag becomes 1 while the POECR5.IC5ADDMT0ZE bit and the ICSR5.POE11E bit are 1.
When the ICSR7.POE12F flag becomes 1 while the POECR5.IC6ADDMT0ZE bit and the ICSR7.POE12E bit are 1.
- Comparator output detection
When the POECMPFR.C0FLAG flag becomes 1 while the POECR5.CMADDMT0ZE bit is 1 and the POECMPEX2.POEREQ0 bit or the POECMPSEL.POEREQ0 bit is 1.
When the POECMPFR.C1FLAG flag becomes 1 while the POECR5.CMADDMT0ZE bit is 1 and the POECMPEX2.POEREQ1 bit or the POECMPSEL.POEREQ1 bit is 1.
When the POECMPFR.C2FLAG flag becomes 1 while the POECR5.CMADDMT0ZE bit is 1 and the POECMPEX2.POEREQ2 bit or the POECMPSEL.POEREQ2 bit is 1.
When the POECMPFR.C3FLAG flag becomes 1 while the POECR5.CMADDMT0ZE bit is 1 and the POECMPEX2.POEREQ3 bit or the POECMPSEL.POEREQ3 bit is 1.
- Detection of oscillation stop
When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(12) MTU0 pin (MTIOC0D)

When one of the following conditions is satisfied while the POECR1.MTU0DZE bit is 1, the pin becomes high-impedance. Furthermore, when the POECR1.MTU0DZE bit is 0 and the PMMCR1.MTU0DME bit is 1 and when one of

the following conditions is satisfied, the pin is switched to general I/O port pin.

- Operation for detection of the POE8# input level
  When the ICSR3.POE8F flag becomes 1 while the ICSR3.POE8E bit is 1.
- SPOER setting
  When the SPOER.MTUCH0HIZ bit is set to 1.
- Conditions added by POECR5
  When the ICSR1.POE0F flag becomes 1 while the POECR5.IC1ADDMT0ZE bit is 1.
  When the ICSR2.POE4F flag becomes 1 while the POECR5.IC2ADDMT0ZE bit is 1.
  When the ICSR4.POE10F flag becomes 1 while the POECR5.IC4ADDMT0ZE bit and the ICSR4.POE10E bit are 1.
  When the ICSR5.POE11F flag becomes 1 while the POECR5.IC5ADDMT0ZE bit and the ICSR5.POE11E bit are 1.
  When the ICSR7.POE12F flag becomes 1 while the POECR5.IC6ADDMT0ZE bit and the ICSR7.POE12E bit are 1.
- Comparator output detection
  When the POECMPFR.C0FLAG flag becomes 1 while the POECR5.CMADDMT0ZE bit is 1 and the POECMPEX2.POEREQ0 bit or the POECMPSEL.POEREQ0 bit is 1.
  When the POECMPFR.C1FLAG flag becomes 1 while the POECR5.CMADDMT0ZE bit is 1 and the POECMPEX2.POEREQ1 bit or the POECMPSEL.POEREQ1 bit is 1.
  When the POECMPFR.C2FLAG flag becomes 1 while the POECR5.CMADDMT0ZE bit is 1 and the POECMPEX2.POEREQ2 bit or the POECMPSEL.POEREQ2 bit is 1.
  When the POECMPFR.C3FLAG flag becomes 1 while the POECR5.CMADDMT0ZE bit is 1 and the POECMPEX2.POEREQ3 bit or the POECMPSEL.POEREQ3 bit is 1.
- Detection of oscillation stop
  When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(13) MTU9 pin PD7 (MTIOC9A)

When one of the following conditions is satisfied while the POECR7.MTU9AZE bit is 1, the pin becomes high-impedance. Furthermore, when the POECR7.MTU9AZE bit is 0 and the PMMCR3.MTU9AME bit is 1 and when one of the following conditions is satisfied, the pin is switched to general I/O port pin.

- Operation for detection of the POE12# input level
  When the ICSR7.POE12F flag becomes 1 while the ICSR7.POE12E bit is 1.
- SPOER setting
  When the SPOER.MTUCH9HIZ bit is set to 1.
- Conditions added by POECR8
  When the ICSR1.POE0F flag becomes 1 while the POECR8.IC1ADDMT9ZE bit is 1.
  When the ICSR2.POE4F flag becomes 1 while the POECR8.IC2ADDMT9ZE bit is 1.
  When the ICSR3.POE8F flag becomes 1 while the POECR8.IC3ADDMT9ZE bit and the ICSR3.POE8E bit are 1.
  When the ICSR4.POE10F flag becomes 1 while the POECR8.IC4ADDMT9ZE bit and the ICSR4.POE10E bit are 1.
  When the ICSR5.POE11F flag becomes 1 while the POECR8.IC5ADDMT9ZE bit and the ICSR5.POE11E bit are 1.
- Comparator output detection
  When the POECMPFR.C0FLAG flag becomes 1 while the POECR8.CMADDMT9ZE bit is 1 and the POECMPEX5.POEREQ0 bit or the POECMPSEL.POEREQ0 bit is 1.
  When the POECMPFR.C1FLAG flag becomes 1 while the POECR8.CMADDMT9ZE bit is 1 and the POECMPEX5.POEREQ1 bit or the POECMPSEL.POEREQ1 bit is 1.
  When the POECMPFR.C2FLAG flag becomes 1 while the POECR8.CMADDMT9ZE bit is 1 and the

POECMPEX5.POEREQ2 bit or the POECMPSEL.POEREQ2 bit is 1.
When the POECMPFR.C3FLAG flag becomes 1 while the POECR8.CMADDMT9ZE bit is 1 and the POECMPEX5.POEREQ3 bit or the POECMPSEL.POEREQ3 bit is 1.

- Detection of oscillation stop
  When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(14) MTU9 pin P21 (MTIOC9A)

When one of the following conditions is satisfied while the POECR7.MTU9A1ZE bit is 1, the pin becomes high-impedance. Furthermore, when the POECR7.MTU9A1ZE bit is 0 and the PMMCR3.MTU9A1ME bit is 1 and when one of the following conditions is satisfied, the pin is switched to general I/O port pin.

- Operation for detection of the POE12# input level
  When the ICSR7.POE12F flag becomes 1 while the ICSR7.POE12E bit is 1.
- SPOER setting
  When the SPOER.MTUCH9HIZ bit is set to 1.
- Conditions added by POECR8
  When the ICSR1.POE0F flag becomes 1 while the POECR8.IC1ADDMT9ZE bit is 1.
  When the ICSR2.POE4F flag becomes 1 while the POECR8.IC2ADDMT9ZE bit is 1.
  When the ICSR3.POE8F flag becomes 1 while the POECR8.IC3ADDMT9ZE bit and the ICSR3.POE8E bit are 1.
  When the ICSR4.POE10F flag becomes 1 while the POECR8.IC4ADDMT9ZE bit and the ICSR4.POE10E bit are 1.
  When the ICSR5.POE11F flag becomes 1 while the POECR8.IC5ADDMT9ZE bit and the ICSR5.POE11E bit are 1.
- Comparator output detection
  When the POECMPFR.C0FLAG flag becomes 1 while the POECR8.CMADDMT9ZE bit is 1 and the POECMPEX5.POEREQ0 bit or the POECMPSEL.POEREQ0 bit is 1.
  When the POECMPFR.C1FLAG flag becomes 1 while the POECR8.CMADDMT9ZE bit is 1 and the POECMPEX5.POEREQ1 bit or the POECMPSEL.POEREQ1 bit is 1.
  When the POECMPFR.C2FLAG flag becomes 1 while the POECR8.CMADDMT9ZE bit is 1 and the POECMPEX5.POEREQ2 bit or the POECMPSEL.POEREQ2 bit is 1.
  When the POECMPFR.C3FLAG flag becomes 1 while the POECR8.CMADDMT9ZE bit is 1 and the POECMPEX5.POEREQ3 bit or the POECMPSEL.POEREQ3 bit is 1.
- Detection of oscillation stop
  When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(15) MTU9 pin P26 (MTIOC9A)

When one of the following conditions is satisfied while the POECR7.MTU9A2ZE bit is 1, the pin becomes high-impedance. Furthermore, when the POECR7.MTU9A2ZE bit is 0 and the PMMCR3.MTU9A2ME bit is 1 and when one of the following conditions is satisfied, the pin is switched to general I/O port pin.

- Operation for detection of the POE12# input level
  When the ICSR7.POE12F flag becomes 1 while the ICSR7.POE12E bit is 1.
- SPOER setting
  When the SPOER.MTUCH9HIZ bit is set to 1.
- Conditions added by POECR8
  When the ICSR1.POE0F flag becomes 1 while the POECR8.IC1ADDMT9ZE bit is 1.
  When the ICSR2.POE4F flag becomes 1 while the POECR8.IC2ADDMT9ZE bit is 1.
  When the ICSR3.POE8F flag becomes 1 while the POECR8.IC3ADDMT9ZE bit and the ICSR3.POE8E bit are 1.
  When the ICSR4.POE10F flag becomes 1 while the POECR8.IC4ADDMT9ZE bit and the ICSR4.POE10E bit are 1.

When the ICSR5.POE11F flag becomes 1 while the POECR8.IC5ADDMT9ZE bit and the ICSR5.POE11E bit are 1.

- Comparator output detection
  When the POECMPFR.C0FLAG flag becomes 1 while the POECR8.CMADDMT9ZE bit is 1 and the POECMPEX5.POEREQ0 bit or the POECMPSEL.POEREQ0 bit is 1.
  When the POECMPFR.C1FLAG flag becomes 1 while the POECR8.CMADDMT9ZE bit is 1 and the POECMPEX5.POEREQ1 bit or the POECMPSEL.POEREQ1 bit is 1.
  When the POECMPFR.C2FLAG flag becomes 1 while the POECR8.CMADDMT9ZE bit is 1 and the POECMPEX5.POEREQ2 bit or the POECMPSEL.POEREQ2 bit is 1.
  When the POECMPFR.C3FLAG flag becomes 1 while the POECR8.CMADDMT9ZE bit is 1 and the POECMPEX5.POEREQ3 bit or the POECMPSEL.POEREQ3 bit is 1.
- Detection of oscillation stop
  When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(16) MTU9 pin PE0 (MTIOC9B)

When one of the following conditions is satisfied while the POECR7.MTU9BZE bit is 1, the pin becomes high-impedance. Furthermore, when the POECR7.MTU9BZE bit is 0 and the PMMCR3.MTU9BME bit is 1 and when one of the following conditions is satisfied, the pin is switched to general I/O port pin.

- Operation for detection of the POE12# input level
  When the ICSR7.POE12F flag becomes 1 while the ICSR7.POE12E bit is 1.
- SPOER setting
  When the SPOER.MTUCH9HIZ bit is set to 1.
- Conditions added by POECR8
  When the ICSR1.POE0F flag becomes 1 while the POECR8.IC1ADDMT9ZE bit is 1.
  When the ICSR2.POE4F flag becomes 1 while the POECR8.IC2ADDMT9ZE bit is 1.
  When the ICSR3.POE8F flag becomes 1 while the POECR8.IC3ADDMT9ZE bit and the ICSR3.POE8E bit are 1.
  When the ICSR4.POE10F flag becomes 1 while the POECR8.IC4ADDMT9ZE bit and the ICSR4.POE10E bit are 1.
  When the ICSR5.POE11F flag becomes 1 while the POECR8.IC5ADDMT9ZE bit and the ICSR5.POE11E bit are 1.
- Comparator output detection
  When the POECMPFR.C0FLAG flag becomes 1 while the POECR8.CMADDMT9ZE bit is 1 and the POECMPEX5.POEREQ0 bit or the POECMPSEL.POEREQ0 bit is 1.
  When the POECMPFR.C1FLAG flag becomes 1 while the POECR8.CMADDMT9ZE bit is 1 and the POECMPEX5.POEREQ1 bit or the POECMPSEL.POEREQ1 bit is 1.
  When the POECMPFR.C2FLAG flag becomes 1 while the POECR8.CMADDMT9ZE bit is 1 and the POECMPEX5.POEREQ2 bit or the POECMPSEL.POEREQ2 bit is 1.
  When the POECMPFR.C3FLAG flag becomes 1 while the POECR8.CMADDMT9ZE bit is 1 and the POECMPEX5.POEREQ3 bit or the POECMPSEL.POEREQ3 bit is 1.
- Detection of oscillation stop
  When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(17) MTU9 pin P10 (MTIOC9B)

When one of the following conditions is satisfied while the POECR7.MTU9B1ZE bit is 1, the pin becomes high-impedance. Furthermore, when the POECR7.MTU9B1ZE bit is 0 and the PMMCR3.MTU9B1ME bit is 1 and when one of the following conditions is satisfied, the pin is switched to general I/O port pin.

- Operation for detection of the POE12# input level
  When the ICSR7.POE12F flag becomes 1 while the ICSR7.POE12E bit is 1.

- SPOER setting
  When the SPOER.MTUCH9HIZ bit is set to 1.
- Conditions added by POECR8
  When the ICSR1.POE0F flag becomes 1 while the POECR8.IC1ADDMT9ZE bit is 1.
  When the ICSR2.POE4F flag becomes 1 while the POECR8.IC2ADDMT9ZE bit is 1.
  When the ICSR3.POE8F flag becomes 1 while the POECR8.IC3ADDMT9ZE bit and the ICSR3.POE8E bit are 1.
  When the ICSR4.POE10F flag becomes 1 while the POECR8.IC4ADDMT9ZE bit and the ICSR4.POE10E bit are 1.
  When the ICSR5.POE11F flag becomes 1 while the POECR8.IC5ADDMT9ZE bit and the ICSR5.POE11E bit are 1.
- Comparator output detection
  When the POECMPFR.C0FLAG flag becomes 1 while the POECR8.CMADDMT9ZE bit is 1 and the POECMPEX5.POEREQ0 bit or the POECMPSEL.POEREQ0 bit is 1.
  When the POECMPFR.C1FLAG flag becomes 1 while the POECR8.CMADDMT9ZE bit is 1 and the POECMPEX5.POEREQ1 bit or the POECMPSEL.POEREQ1 bit is 1.
  When the POECMPFR.C2FLAG flag becomes 1 while the POECR8.CMADDMT9ZE bit is 1 and the POECMPEX5.POEREQ2 bit or the POECMPSEL.POEREQ2 bit is 1.
  When the POECMPFR.C3FLAG flag becomes 1 while the POECR8.CMADDMT9ZE bit is 1 and the POECMPEX5.POEREQ3 bit or the POECMPSEL.POEREQ3 bit is 1.
- Detection of oscillation stop
  When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(18) MTU9 pin PD6 (MTIOC9C)

When one of the following conditions is satisfied while the POECR7.MTU9CZE bit is 1, the pin becomes high-impedance. Furthermore, when the POECR7.MTU9CZE bit is 0 and the PMMCR3.MTU9CME bit is 1 and when one of the following conditions is satisfied, the pin is switched to general I/O port pin.

- Operation for detection of the POE12# input level
  When the ICSR7.POE12F flag becomes 1 while the ICSR7.POE12E bit is 1.
- SPOER setting
  When the SPOER.MTUCH9HIZ bit is set to 1.
- Conditions added by POECR8
  When the ICSR1.POE0F flag becomes 1 while the POECR8.IC1ADDMT9ZE bit is 1.
  When the ICSR2.POE4F flag becomes 1 while the POECR8.IC2ADDMT9ZE bit is 1.
  When the ICSR3.POE8F flag becomes 1 while the POECR8.IC3ADDMT9ZE bit and the ICSR3.POE8E bit are 1.
  When the ICSR4.POE10F flag becomes 1 while the POECR8.IC4ADDMT9ZE bit and the ICSR4.POE10E bit are 1.
  When the ICSR5.POE11F flag becomes 1 while the POECR8.IC5ADDMT9ZE bit and the ICSR5.POE11E bit are 1.
- Comparator output detection
  When the POECMPFR.C0FLAG flag becomes 1 while the POECR8.CMADDMT9ZE bit is 1 and the POECMPEX5.POEREQ0 bit or the POECMPSEL.POEREQ0 bit is 1.
  When the POECMPFR.C1FLAG flag becomes 1 while the POECR8.CMADDMT9ZE bit is 1 and the POECMPEX5.POEREQ1 bit or the POECMPSEL.POEREQ1 bit is 1.
  When the POECMPFR.C2FLAG flag becomes 1 while the POECR8.CMADDMT9ZE bit is 1 and the POECMPEX5.POEREQ2 bit or the POECMPSEL.POEREQ2 bit is 1.
  When the POECMPFR.C3FLAG flag becomes 1 while the POECR8.CMADDMT9ZE bit is 1 and the POECMPEX5.POEREQ3 bit or the POECMPSEL.POEREQ3 bit is 1.
- Detection of oscillation stop

When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(19) MTU9 pin P20 (MTIOC9C)

When one of the following conditions is satisfied while the POECR7.MTU9C1ZE bit is 1, the pin becomes high-impedance. Furthermore, when the POECR7.MTU9C1ZE bit is 0 and the PMMCR3.MTU9C1ME bit is 1 and when one of the following conditions is satisfied, the pin is switched to general I/O port pin.

- Operation for detection of the POE12# input level
  When the ICSR7.POE12F flag becomes 1 while the ICSR7.POE12E bit is 1.
- SPOER setting
  When the SPOER.MTUCH9HIZ bit is set to 1.
- Conditions added by POECR8
  When the ICSR1.POE0F flag becomes 1 while the POECR8.IC1ADDMT9ZE bit is 1.
  When the ICSR2.POE4F flag becomes 1 while the POECR8.IC2ADDMT9ZE bit is 1.
  When the ICSR3.POE8F flag becomes 1 while the POECR8.IC3ADDMT9ZE bit and the ICSR3.POE8E bit are 1.
  When the ICSR4.POE10F flag becomes 1 while the POECR8.IC4ADDMT9ZE bit and the ICSR4.POE10E bit are 1.
  When the ICSR5.POE11F flag becomes 1 while the POECR8.IC5ADDMT9ZE bit and the ICSR5.POE11E bit are 1.
- Comparator output detection
  When the POECMPFR.C0FLAG flag becomes 1 while the POECR8.CMADDMT9ZE bit is 1 and the POECMPEX5.POEREQ0 bit or the POECMPSEL.POEREQ0 bit is 1.
  When the POECMPFR.C1FLAG flag becomes 1 while the POECR8.CMADDMT9ZE bit is 1 and the POECMPEX5.POEREQ1 bit or the POECMPSEL.POEREQ1 bit is 1.
  When the POECMPFR.C2FLAG flag becomes 1 while the POECR8.CMADDMT9ZE bit is 1 and the POECMPEX5.POEREQ2 bit or the POECMPSEL.POEREQ2 bit is 1.
  When the POECMPFR.C3FLAG flag becomes 1 while the POECR8.CMADDMT9ZE bit is 1 and the POECMPEX5.POEREQ3 bit or the POECMPSEL.POEREQ3 bit is 1.
- Detection of oscillation stop
  When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(20) MTU9 pin P25 (MTIOC9C)

When one of the following conditions is satisfied while the POECR7.MTU9C2ZE bit is 1, the pin becomes high-impedance. Furthermore, when the POECR7.MTU9C2ZE bit is 0 and the PMMCR3.MTU9C2ME bit is 1 and when one of the following conditions is satisfied, the pin is switched to general I/O port pin.

- Operation for detection of the POE12# input level
  When the ICSR7.POE12F flag becomes 1 while the ICSR7.POE12E bit is 1.
- SPOER setting
  When the SPOER.MTUCH9HIZ bit is set to 1.
- Conditions added by POECR8
  When the ICSR1.POE0F flag becomes 1 while the POECR8.IC1ADDMT9ZE bit is 1.
  When the ICSR2.POE4F flag becomes 1 while the POECR8.IC2ADDMT9ZE bit is 1.
  When the ICSR3.POE8F flag becomes 1 while the POECR8.IC3ADDMT9ZE bit and the ICSR3.POE8E bit are 1.
  When the ICSR4.POE10F flag becomes 1 while the POECR8.IC4ADDMT9ZE bit and the ICSR4.POE10E bit are 1.
  When the ICSR5.POE11F flag becomes 1 while the POECR8.IC5ADDMT9ZE bit and the ICSR5.POE11E bit are 1.
- Comparator output detection
  When the POECMPFR.C0FLAG flag becomes 1 while the POECR8.CMADDMT9ZE bit is 1 and the

POECMPEX5.POEREQ0 bit or the POECMPSEL.POEREQ0 bit is 1.
When the POECMPFR.C1FLAG flag becomes 1 while the POECR8.CMADDMT9ZE bit is 1 and the POECMPEX5.POEREQ1 bit or the POECMPSEL.POEREQ1 bit is 1.
When the POECMPFR.C2FLAG flag becomes 1 while the POECR8.CMADDMT9ZE bit is 1 and the POECMPEX5.POEREQ2 bit or the POECMPSEL.POEREQ2 bit is 1.
When the POECMPFR.C3FLAG flag becomes 1 while the POECR8.CMADDMT9ZE bit is 1 and the POECMPEX5.POEREQ3 bit or the POECMPSEL.POEREQ3 bit is 1.

- Detection of oscillation stop
  When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(21) MTU9 pin PE1 (MTIOC9D)

When one of the following conditions is satisfied while the POECR7.MTU9DZE bit is 1, the pin becomes high-impedance. Furthermore, when the POECR7.MTU9DZE bit is 0 and the PMMCR3.MTU9DME bit is 1 and when one of the following conditions is satisfied, the pin is switched to general I/O port pin.

- Operation for detection of the POE12# input level
  When the ICSR7.POE12F flag becomes 1 while the ICSR7.POE12E bit is 1.
- SPOER setting
  When the SPOER.MTUCH9HIZ bit is set to 1.
- Conditions added by POECR8
  When the ICSR1.POE0F flag becomes 1 while the POECR8.IC1ADDMT9ZE bit is 1.
  When the ICSR2.POE4F flag becomes 1 while the POECR8.IC2ADDMT9ZE bit is 1.
  When the ICSR3.POE8F flag becomes 1 while the POECR8.IC3ADDMT9ZE bit and the ICSR3.POE8E bit are 1.
  When the ICSR4.POE10F flag becomes 1 while the POECR8.IC4ADDMT9ZE bit and the ICSR4.POE10E bit are 1.
  When the ICSR5.POE11F flag becomes 1 while the POECR8.IC5ADDMT9ZE bit and the ICSR5.POE11E bit are 1.
- Comparator output detection
  When the POECMPFR.C0FLAG flag becomes 1 while the POECR8.CMADDMT9ZE bit is 1 and the POECMPEX5.POEREQ0 bit or the POECMPSEL.POEREQ0 bit is 1.
  When the POECMPFR.C1FLAG flag becomes 1 while the POECR8.CMADDMT9ZE bit is 1 and the POECMPEX5.POEREQ1 bit or the POECMPSEL.POEREQ1 bit is 1.
  When the POECMPFR.C2FLAG flag becomes 1 while the POECR8.CMADDMT9ZE bit is 1 and the POECMPEX5.POEREQ2 bit or the POECMPSEL.POEREQ2 bit is 1.
  When the POECMPFR.C3FLAG flag becomes 1 while the POECR8.CMADDMT9ZE bit is 1 and the POECMPEX5.POEREQ3 bit or the POECMPSEL.POEREQ3 bit is 1.
- Detection of oscillation stop
  When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(22) MTU9 pin P02 (MTIOC9D)

When one of the following conditions is satisfied while the POECR7.MTU9D1ZE bit is 1, the pin becomes high-impedance. Furthermore, when the POECR7.MTU9D1ZE bit is 0 and the PMMCR3.MTU9D1ME bit is 1 and when one of the following conditions is satisfied, the pin is switched to general I/O port pin.

- Operation for detection of the POE12# input level
  When the ICSR7.POE12F flag becomes 1 while the ICSR7.POE12E bit is 1.
- SPOER setting
  When the SPOER.MTUCH9HIZ bit is set to 1.
- Conditions added by POECR8
  When the ICSR1.POE0F flag becomes 1 while the POECR8.IC1ADDMT9ZE bit is 1.

When the ICSR2.POE4F flag becomes 1 while the POECR8.IC2ADDMT9ZE bit is 1.
When the ICSR3.POE8F flag becomes 1 while the POECR8.IC3ADDMT9ZE bit and the ICSR3.POE8E bit are 1.
When the ICSR4.POE10F flag becomes 1 while the POECR8.IC4ADDMT9ZE bit and the ICSR4.POE10E bit are 1.
When the ICSR5.POE11F flag becomes 1 while the POECR8.IC5ADDMT9ZE bit and the ICSR5.POE11E bit are 1.

- Comparator output detection
  When the POECMPFR.C0FLAG flag becomes 1 while the POECR8.CMADDMT9ZE bit is 1 and the POECMPEX5.POEREQ0 bit or the POECMPSEL.POEREQ0 bit is 1.
  When the POECMPFR.C1FLAG flag becomes 1 while the POECR8.CMADDMT9ZE bit is 1 and the POECMPEX5.POEREQ1 bit or the POECMPSEL.POEREQ1 bit is 1.
  When the POECMPFR.C2FLAG flag becomes 1 while the POECR8.CMADDMT9ZE bit is 1 and the POECMPEX5.POEREQ2 bit or the POECMPSEL.POEREQ2 bit is 1.
  When the POECMPFR.C3FLAG flag becomes 1 while the POECR8.CMADDMT9ZE bit is 1 and the POECMPEX5.POEREQ3 bit or the POECMPSEL.POEREQ3 bit is 1.
- Detection of oscillation stop
  When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(23) GPT0 pin or MTU3 pin P12 (GTIOC0A/MTIOC3B)

When one of the following conditions is satisfied while the POECR3.GPT0AZE bit is 1, the pin becomes high-impedance. Furthermore, when one of the following conditions is satisfied while the POECR3.GPT0AZE bit is 0 and the PMMCR2.GPT0AME bit is 1, the pin is switched to general I/O port pin.

- Operation for detection of the POE10# input level
  When the ICSR4.POE10F flag becomes 1 while the ICSR4.POE10E bit is 1.
- Operation for comparison of the output levels on the MTIOC3B and MTIOC3D or GTIOC0A and GTIOC0B pins
  When the OCSR3.OSF3 flag becomes 1 while the OCSR3.OCE3 bit is 1.
- SPOER setting
  When the SPOER.GPT02HIZ bit is set to 1.
- Conditions added by POECR6
  When the ICSR1.POE0F flag becomes 1 while the POECR6.IC1ADDGPT02ZE bit is 1.
  When the ICSR2.POE4F flag becomes 1 while the POECR6.IC2ADDGPT02ZE bit is 1.
  When the ICSR3.POE8F flag becomes 1 while the POECR6.IC3ADDGPT02ZE bit and the ICSR3.POE8E bit are 1.
  When the ICSR5.POE11F flag becomes 1 while the POECR6.IC5ADDGPT02ZE bit and the ICSR5.POE11E bit are 1.
  When the ICSR7.POE12F flag becomes 1 while the POECR6.IC6ADDGPT02ZE bit and the ICSR7.POE12E bit are 1.
- Comparator output detection
  When the POECMPFR.C0FLAG flag becomes 1 while the POECR6.CMADDGPT02ZE bit is 1 and the POECMPEX3.POEREQ0 bit or the POECMPSEL.POEREQ0 bit is 1.
  When the POECMPFR.C1FLAG flag becomes 1 while the POECR6.CMADDGPT02ZE bit is 1 and the POECMPEX3.POEREQ1 bit or the POECMPSEL.POEREQ1 bit is 1.
  When the POECMPFR.C2FLAG flag becomes 1 while the POECR6.CMADDGPT02ZE bit is 1 and the POECMPEX3.POEREQ2 bit or the POECMPSEL.POEREQ2 bit is 1.
  When the POECMPFR.C3FLAG flag becomes 1 while the POECR6.CMADDGPT02ZE bit is 1 and the POECMPEX3.POEREQ3 bit or the POECMPSEL.POEREQ3 bit is 1.
- Detection of oscillation stop
  When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(24) GPT0 pin or MTU3 pin P15 (GTIOC0B/MTIOC3D)

When one of the following conditions is satisfied while the POECR3.GPT0BZE bit is 1, the pin becomes high-impedance. Furthermore, when one of the following conditions is satisfied while the POECR3.GPT0BZE bit is 0 and the PMMCR2.GPT0BME bit is 1, the pin is switched to general I/O port pin.

- Operation for detection of the POE10# input level
  When the ICSR4.POE10F flag becomes 1 while the ICSR4.POE10E bit is 1.
- Operation for comparison of the output levels on the MTIOC3B and MTIOC3D or GTIOC0A and GTIOC0B pins
  When the OCSR3.OSF3 flag becomes 1 while the OCSR3.OCE3 bit is 1.
- SPOER setting
  When the SPOER.GPT02HIZ bit is set to 1.
- Conditions added by POECR6
  When the ICSR1.POE0F flag becomes 1 while the POECR6.IC1ADDGPT02ZE bit is 1.
  When the ICSR2.POE4F flag becomes 1 while the POECR6.IC2ADDGPT02ZE bit is 1.
  When the ICSR3.POE8F flag becomes 1 while the POECR6.IC3ADDGPT02ZE bit and the ICSR3.POE8E bit are 1.
  When the ICSR5.POE11F flag becomes 1 while the POECR6.IC5ADDGPT02ZE bit and the ICSR5.POE11E bit are 1.
  When the ICSR7.POE12F flag becomes 1 while the POECR6.IC6ADDGPT02ZE bit and the ICSR7.POE12E bit are 1.
- Comparator output detection
  When the POECMPFR.C0FLAG flag becomes 1 while the POECR6.CMADDGPT02ZE bit is 1 and the POECMPEX3.POEREQ0 bit or the POECMPSEL.POEREQ0 bit is 1.
  When the POECMPFR.C1FLAG flag becomes 1 while the POECR6.CMADDGPT02ZE bit is 1 and the POECMPEX3.POEREQ1 bit or the POECMPSEL.POEREQ1 bit is 1.
  When the POECMPFR.C2FLAG flag becomes 1 while the POECR6.CMADDGPT02ZE bit is 1 and the POECMPEX3.POEREQ2 bit or the POECMPSEL.POEREQ2 bit is 1.
  When the POECMPFR.C3FLAG flag becomes 1 while the POECR6.CMADDGPT02ZE bit is 1 and the POECMPEX3.POEREQ3 bit or the POECMPSEL.POEREQ3 bit is 1.
- Detection of oscillation stop
  When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(25) GPT1 pin or MTU4 pin P13 (GTIOC1A/MTIOC4A)

When one of the following conditions is satisfied while the POECR3.GPT1AZE bit is 1, the pin becomes high-impedance. Furthermore, when one of the following conditions is satisfied while the POECR3.GPT1AZE bit is 0 and the PMMCR2.GPT1AME bit is 1, the pin is switched to general I/O port pin.

- Operation for detection of the POE10# input level
  When the ICSR4.POE10F flag becomes 1 while the ICSR4.POE10E bit is 1.
- Operation for comparison of the output levels on the MTIOC4A and MTIOC4C or GTIOC1A and GTIOC1B pins
  When the OCSR3.OSF3 flag becomes 1 while the OCSR3.OCE3 bit is 1.
- SPOER setting
  When the SPOER.GPT02HIZ bit is set to 1.
- Conditions added by POECR6
  When the ICSR1.POE0F flag becomes 1 while the POECR6.IC1ADDGPT02ZE bit is 1.
  When the ICSR2.POE4F flag becomes 1 while the POECR6.IC2ADDGPT02ZE bit is 1.
  When the ICSR3.POE8F flag becomes 1 while the POECR6.IC3ADDGPT02ZE bit and the ICSR3.POE8E bit are 1.
  When the ICSR5.POE11F flag becomes 1 while the POECR6.IC5ADDGPT02ZE bit and the ICSR5.POE11E bit

are 1.
When the ICSR7.POE12F flag becomes 1 while the POECR6.IC6ADDGPT02ZE bit and the ICSR7.POE12E bit are 1.

- Comparator output detection
When the POECMPFR.C0FLAG flag becomes 1 while the POECR6.CMADDGPT02ZE bit is 1 and the POECMPEX3.POEREQ0 bit or the POECMPSEL.POEREQ0 bit is 1.
When the POECMPFR.C1FLAG flag becomes 1 while the POECR6.CMADDGPT02ZE bit is 1 and the POECMPEX3.POEREQ1 bit or the POECMPSEL.POEREQ1 bit is 1.
When the POECMPFR.C2FLAG flag becomes 1 while the POECR6.CMADDGPT02ZE bit is 1 and the POECMPEX3.POEREQ2 bit or the POECMPSEL.POEREQ2 bit is 1.
When the POECMPFR.C3FLAG flag becomes 1 while the POECR6.CMADDGPT02ZE bit is 1 and the POECMPEX3.POEREQ3 bit or the POECMPSEL.POEREQ3 bit is 1.
- Detection of oscillation stop
When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(26) GPT1 pin or MTU4 pin P16 (GTIOC1B/MTIOC4C)

When one of the following conditions is satisfied while the POECR3.GPT1BZE bit is 1, the pin becomes high-impedance. Furthermore, when one of the following conditions is satisfied while the POECR3.GPT1BZE bit is 0 and the PMMCR2.GPT1BME bit is 1, the pin is switched to general I/O port pin.

- Operation for detection of the POE10# input level
When the ICSR4.POE10F flag becomes 1 while the ICSR4.POE10E bit is 1.
- Operation for comparison of the output levels on the MTIOC4A and MTIOC4C or GTIOC1A and GTIOC1B pins
When the OCSR3.OSF3 flag becomes 1 while the OCSR3.OCE3 bit is 1.
- SPOER setting
When the SPOER.GPT02HIZ bit is set to 1.
- Conditions added by POECR6
When the ICSR1.POE0F flag becomes 1 while the POECR6.IC1ADDGPT02ZE bit is 1.
When the ICSR2.POE4F flag becomes 1 while the POECR6.IC2ADDGPT02ZE bit is 1.
When the ICSR3.POE8F flag becomes 1 while the POECR6.IC3ADDGPT02ZE bit and the ICSR3.POE8E bit are 1.
When the ICSR5.POE11F flag becomes 1 while the POECR6.IC5ADDGPT02ZE bit and the ICSR5.POE11E bit are 1.
When the ICSR7.POE12F flag becomes 1 while the POECR6.IC6ADDGPT02ZE bit and the ICSR7.POE12E bit are 1.
- Comparator output detection
When the POECMPFR.C0FLAG flag becomes 1 while the POECR6.CMADDGPT02ZE bit is 1 and the POECMPEX3.POEREQ0 bit or the POECMPSEL.POEREQ0 bit is 1.
When the POECMPFR.C1FLAG flag becomes 1 while the POECR6.CMADDGPT02ZE bit is 1 and the POECMPEX3.POEREQ1 bit or the POECMPSEL.POEREQ1 bit is 1.
When the POECMPFR.C2FLAG flag becomes 1 while the POECR6.CMADDGPT02ZE bit is 1 and the POECMPEX3.POEREQ2 bit or the POECMPSEL.POEREQ2 bit is 1.
When the POECMPFR.C3FLAG flag becomes 1 while the POECR6.CMADDGPT02ZE bit is 1 and the POECMPEX3.POEREQ3 bit or the POECMPSEL.POEREQ3 bit is 1.
- Detection of oscillation stop
When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(27) GPT2 pin or MTU4 pin P14 (GTIOC2A/MTIOC4B)

When one of the following conditions is satisfied while the POECR3.GPT2AZE bit is 1, the pin becomes high-

impedance. Furthermore, when one of the following conditions is satisfied while the POECR3.GPT2AZE bit is 0 and the PMMCR2.GPT2AME bit is 1, the pin is switched to general I/O port pin.

- Operation for detection of the POE10# input level
  When the ICSR4.POE10F flag becomes 1 while the ICSR4.POE10E bit is 1.
- Operation for comparison of the output levels on the MTIOC4B and MTIOC4D or GTIOC2A and GTIOC2B pins
  When the OCSR3.OSF3 flag becomes 1 while the OCSR3.OCE3 bit is 1.
- SPOER setting
  When the SPOER.GPT02HIZ bit is set to 1.
- Conditions added by POECR6
  When the ICSR1.POE0F flag becomes 1 while the POECR6.IC1ADDGPT02ZE bit is 1.
  When the ICSR2.POE4F flag becomes 1 while the POECR6.IC2ADDGPT02ZE bit is 1.
  When the ICSR3.POE8F flag becomes 1 while the POECR6.IC3ADDGPT02ZE bit and the ICSR3.POE8E bit are 1.
  When the ICSR5.POE11F flag becomes 1 while the POECR6.IC5ADDGPT02ZE bit and the ICSR5.POE11E bit are 1.
  When the ICSR7.POE12F flag becomes 1 while the POECR6.IC6ADDGPT02ZE bit and the ICSR7.POE12E bit are 1.
- Comparator output detection
  When the POECMPFR.C0FLAG flag becomes 1 while the POECR6.CMADDGPT02ZE bit is 1 and the POECMPEX3.POEREQ0 bit or the POECMPSEL.POEREQ0 bit is 1.
  When the POECMPFR.C1FLAG flag becomes 1 while the POECR6.CMADDGPT02ZE bit is 1 and the POECMPEX3.POEREQ1 bit or the POECMPSEL.POEREQ1 bit is 1.
  When the POECMPFR.C2FLAG flag becomes 1 while the POECR6.CMADDGPT02ZE bit is 1 and the POECMPEX3.POEREQ2 bit or the POECMPSEL.POEREQ2 bit is 1.
  When the POECMPFR.C3FLAG flag becomes 1 while the POECR6.CMADDGPT02ZE bit is 1 and the POECMPEX3.POEREQ3 bit or the POECMPSEL.POEREQ3 bit is 1.
- Detection of oscillation stop
  When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(28) GPT2 pin or MTU4 pin P17 (GTIOC2B/MTIOC4D)

When one of the following conditions is satisfied while the POECR3.GPT2BZE bit is 1, the pin becomes high-impedance. Furthermore, when one of the following conditions is satisfied while the POECR3.GPT2BZE bit is 0 and the PMMCR2.GPT2BME bit is 1, the pin is switched to general I/O port pin.

- Operation for detection of the POE10# input level
  When the ICSR4.POE10F flag becomes 1 while the ICSR4.POE10E bit is 1.
- Operation for comparison of the output levels on the MTIOC4B and MTIOC4D or GTIOC2A and GTIOC2B pins
  When the OCSR3.OSF3 flag becomes 1 while the OCSR3.OCE3 bit is 1.
- SPOER setting
  When the SPOER.GPT02HIZ bit is set to 1.
- Conditions added by POECR6
  When the ICSR1.POE0F flag becomes 1 while the POECR6.IC1ADDGPT02ZE bit is 1.
  When the ICSR2.POE4F flag becomes 1 while the POECR6.IC2ADDGPT02ZE bit is 1.
  When the ICSR3.POE8F flag becomes 1 while the POECR6.IC3ADDGPT02ZE bit and the ICSR3.POE8E bit are 1.
  When the ICSR5.POE11F flag becomes 1 while the POECR6.IC5ADDGPT02ZE bit and the ICSR5.POE11E bit are 1.
  When the ICSR7.POE12F flag becomes 1 while the POECR6.IC6ADDGPT02ZE bit and the ICSR7.POE12E bit are 1.

- Comparator output detection
  When the POECMPFR.C0FLAG flag becomes 1 while the POECR6.CMADDGPT02ZE bit is 1 and the POECMPEX3.POEREQ0 bit or the POECMPSEL.POEREQ0 bit is 1.
  When the POECMPFR.C1FLAG flag becomes 1 while the POECR6.CMADDGPT02ZE bit is 1 and the POECMPEX3.POEREQ1 bit or the POECMPSEL.POEREQ1 bit is 1.
  When the POECMPFR.C2FLAG flag becomes 1 while the POECR6.CMADDGPT02ZE bit is 1 and the POECMPEX3.POEREQ2 bit or the POECMPSEL.POEREQ2 bit is 1.
  When the POECMPFR.C3FLAG flag becomes 1 while the POECR6.CMADDGPT02ZE bit is 1 and the POECMPEX3.POEREQ3 bit or the POECMPSEL.POEREQ3 bit is 1.
- Detection of oscillation stop
  When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(29) GPT0 pin PD2 (GTIOC0A)

When one of the following conditions is satisfied while the POECR3.GPT0A1ZE bit is 1, the pin becomes high-impedance. Furthermore, when one of the following conditions is satisfied while the POECR3.GPT0A1ZE bit is 0 and the PMMCR2.GPT0A1ME bit is 1, the pin is switched to general I/O port pin.

- Operation for detection of the POE11# input level
  When the ICSR5.POE11F flag becomes 1 while the ICSR5.POE11E bit is 1.
- SPOER setting
  When the SPOER.GPT03HIZ bit is set to 1.
- Conditions added by POECR6
  When the ICSR1.POE0F flag becomes 1 while the POECR6.IC1ADDGPT03ZE bit is 1.
  When the ICSR2.POE4F flag becomes 1 while the POECR6.IC2ADDGPT03ZE bit is 1.
  When the ICSR3.POE8F flag becomes 1 while the POECR6.IC3ADDGPT03ZE bit and the ICSR3.POE8E bit are 1.
  When the ICSR4.POE10F flag becomes 1 while the POECR6.IC4ADDGPT03ZE bit and the ICSR4.POE10E bit are 1.
  When the ICSR7.POE12F flag becomes 1 while the POECR6.IC6ADDGPT03ZE bit and the ICSR7.POE12E bit are 1.
- Comparator output detection
  When the POECMPFR.C0FLAG flag becomes 1 while the POECR6.CMADDGPT03ZE bit is 1 and the POECMPEX4.POEREQ0 bit or the POECMPSEL.POEREQ0 bit is 1.
  When the POECMPFR.C1FLAG flag becomes 1 while the POECR6.CMADDGPT03ZE bit is 1 and the POECMPEX4.POEREQ1 bit or the POECMPSEL.POEREQ1 bit is 1.
  When the POECMPFR.C2FLAG flag becomes 1 while the POECR6.CMADDGPT03ZE bit is 1 and the POECMPEX4.POEREQ2 bit or the POECMPSEL.POEREQ2 bit is 1.
  When the POECMPFR.C3FLAG flag becomes 1 while the POECR6.CMADDGPT03ZE bit is 1 and the POECMPEX4.POEREQ3 bit or the POECMPSEL.POEREQ3 bit is 1.
- Detection of oscillation stop
  When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(30) GPT0 pin PD1 (GTIOC0B)

When one of the following conditions is satisfied while the POECR3.GPT0B1ZE bit is 1, the pin becomes high-impedance. Furthermore, when one of the following conditions is satisfied while the POECR3.GPT0B1ZE bit is 0 and the PMMCR2.GPT0B1ME bit is 1, the pin is switched to general I/O port pin.

- Operation for detection of the POE11# input level
  When the ICSR5.POE11F flag becomes 1 while the ICSR5.POE11E bit is 1.
- SPOER setting

When the SPOER.GPT03HIZ bit is set to 1.

- Conditions added by POECR6
  When the ICSR1.POE0F flag becomes 1 while the POECR6.IC1ADDGPT03ZE bit is 1.
  When the ICSR2.POE4F flag becomes 1 while the POECR6.IC2ADDGPT03ZE bit is 1.
  When the ICSR3.POE8F flag becomes 1 while the POECR6.IC3ADDGPT03ZE bit and the ICSR3.POE8E bit are 1.
  When the ICSR4.POE10F flag becomes 1 while the POECR6.IC4ADDGPT03ZE bit and the ICSR4.POE10E bit are 1.
  When the ICSR7.POE12F flag becomes 1 while the POECR6.IC6ADDGPT03ZE bit and the ICSR7.POE12E bit are 1.
- Comparator output detection
  When the POECMPFR.C0FLAG flag becomes 1 while the POECR6.CMADDGPT03ZE bit is 1 and the POECMPEX4.POEREQ0 bit or the POECMPSEL.POEREQ0 bit is 1.
  When the POECMPFR.C1FLAG flag becomes 1 while the POECR6.CMADDGPT03ZE bit is 1 and the POECMPEX4.POEREQ1 bit or the POECMPSEL.POEREQ1 bit is 1.
  When the POECMPFR.C2FLAG flag becomes 1 while the POECR6.CMADDGPT03ZE bit is 1 and the POECMPEX4.POEREQ2 bit or the POECMPSEL.POEREQ2 bit is 1.
  When the POECMPFR.C3FLAG flag becomes 1 while the POECR6.CMADDGPT03ZE bit is 1 and the POECMPEX4.POEREQ3 bit or the POECMPSEL.POEREQ3 bit is 1.
- Detection of oscillation stop
  When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(31) GPT1 pin PD0 (GTIOC1A)

When one of the following conditions is satisfied while the POECR3.GPT1A1ZE bit is 1, the pin becomes high-impedance. Furthermore, when one of the following conditions is satisfied while the POECR3.GPT1A1ZE bit is 0 and the PMMCR2.GPT1A1ME bit is 1, the pin is switched to general I/O port pin.

- Operation for detection of the POE11# input level
  When the ICSR5.POE11F flag becomes 1 while the ICSR5.POE11E bit is 1.
- SPOER setting
  When the SPOER.GPT03HIZ bit is set to 1.
- Conditions added by POECR6
  When the ICSR1.POE0F flag becomes 1 while the POECR6.IC1ADDGPT03ZE bit is 1.
  When the ICSR2.POE4F flag becomes 1 while the POECR6.IC2ADDGPT03ZE bit is 1.
  When the ICSR3.POE8F flag becomes 1 while the POECR6.IC3ADDGPT03ZE bit and the ICSR3.POE8E bit are 1.
  When the ICSR4.POE10F flag becomes 1 while the POECR6.IC4ADDGPT03ZE bit and the ICSR4.POE10E bit are 1.
  When the ICSR7.POE12F flag becomes 1 while the POECR6.IC6ADDGPT03ZE bit and the ICSR7.POE12E bit are 1.
- Comparator output detection
  When the POECMPFR.C0FLAG flag becomes 1 while the POECR6.CMADDGPT03ZE bit is 1 and the POECMPEX4.POEREQ0 bit or the POECMPSEL.POEREQ0 bit is 1.
  When the POECMPFR.C1FLAG flag becomes 1 while the POECR6.CMADDGPT03ZE bit is 1 and the POECMPEX4.POEREQ1 bit or the POECMPSEL.POEREQ1 bit is 1.
  When the POECMPFR.C2FLAG flag becomes 1 while the POECR6.CMADDGPT03ZE bit is 1 and the POECMPEX4.POEREQ2 bit or the POECMPSEL.POEREQ2 bit is 1.
  When the POECMPFR.C3FLAG flag becomes 1 while the POECR6.CMADDGPT03ZE bit is 1 and the POECMPEX4.POEREQ3 bit or the POECMPSEL.POEREQ3 bit is 1.

- Detection of oscillation stop
  When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(32) GPT1 pin PB7 (GTIOC1B)

When one of the following conditions is satisfied while the POECR3.GPT1B1ZE bit is 1, the pin becomes high-impedance. Furthermore, when one of the following conditions is satisfied while the POECR3.GPT1B1ZE bit is 0 and the PMMCR2.GPT1B1ME bit is 1, the pin is switched to general I/O port pin.

- Operation for detection of the POE11# input level
  When the ICSR5.POE11F flag becomes 1 while the ICSR5.POE11E bit is 1.
- SPOER setting
  When the SPOER.GPT03HIZ bit is set to 1.
- Conditions added by POECR6
  When the ICSR1.POE0F flag becomes 1 while the POECR6.IC1ADDGPT03ZE bit is 1.
  When the ICSR2.POE4F flag becomes 1 while the POECR6.IC2ADDGPT03ZE bit is 1.
  When the ICSR3.POE8F flag becomes 1 while the POECR6.IC3ADDGPT03ZE bit and the ICSR3.POE8E bit are 1.
  When the ICSR4.POE10F flag becomes 1 while the POECR6.IC4ADDGPT03ZE bit and the ICSR4.POE10E bit are 1.
  When the ICSR7.POE12F flag becomes 1 while the POECR6.IC6ADDGPT03ZE bit and the ICSR7.POE12E bit are 1.
- Comparator output detection
  When the POECMPFR.C0FLAG flag becomes 1 while the POECR6.CMADDGPT03ZE bit is 1 and the POECMPEX4.POEREQ0 bit or the POECMPSEL.POEREQ0 bit is 1.
  When the POECMPFR.C1FLAG flag becomes 1 while the POECR6.CMADDGPT03ZE bit is 1 and the POECMPEX4.POEREQ1 bit or the POECMPSEL.POEREQ1 bit is 1.
  When the POECMPFR.C2FLAG flag becomes 1 while the POECR6.CMADDGPT03ZE bit is 1 and the POECMPEX4.POEREQ2 bit or the POECMPSEL.POEREQ2 bit is 1.
  When the POECMPFR.C3FLAG flag becomes 1 while the POECR6.CMADDGPT03ZE bit is 1 and the POECMPEX4.POEREQ3 bit or the POECMPSEL.POEREQ3 bit is 1.
- Detection of oscillation stop
  When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(33) GPT2 pin PB6 (GTIOC2A)

When one of the following conditions is satisfied while the POECR3.GPT2A1ZE bit is 1, the pin becomes high-impedance. Furthermore, when one of the following conditions is satisfied while the POECR3.GPT2A1ZE bit is 0 and the PMMCR2.GPT2A1ME bit is 1, the pin is switched to general I/O port pin.

- Operation for detection of the POE11# input level
  When the ICSR5.POE11F flag becomes 1 while the ICSR5.POE11E bit is 1.
- SPOER setting
  When the SPOER.GPT03HIZ bit is set to 1.
- Conditions added by POECR6
  When the ICSR1.POE0F flag becomes 1 while the POECR6.IC1ADDGPT03ZE bit is 1.
  When the ICSR2.POE4F flag becomes 1 while the POECR6.IC2ADDGPT03ZE bit is 1.
  When the ICSR3.POE8F flag becomes 1 while the POECR6.IC3ADDGPT03ZE bit and the ICSR3.POE8E bit are 1.
  When the ICSR4.POE10F flag becomes 1 while the POECR6.IC4ADDGPT03ZE bit and the ICSR4.POE10E bit are 1.
  When the ICSR7.POE12F flag becomes 1 while the POECR6.IC6ADDGPT03ZE bit and the ICSR7.POE12E bit

are 1.

- Comparator output detection
  When the POECMPFR.C0FLAG flag becomes 1 while the POECR6.CMADDGPT03ZE bit is 1 and the POECMPEX4.POEREQ0 bit or the POECMPSEL.POEREQ0 bit is 1.
  When the POECMPFR.C1FLAG flag becomes 1 while the POECR6.CMADDGPT03ZE bit is 1 and the POECMPEX4.POEREQ1 bit or the POECMPSEL.POEREQ1 bit is 1.
  When the POECMPFR.C2FLAG flag becomes 1 while the POECR6.CMADDGPT03ZE bit is 1 and the POECMPEX4.POEREQ2 bit or the POECMPSEL.POEREQ2 bit is 1.
  When the POECMPFR.C3FLAG flag becomes 1 while the POECR6.CMADDGPT03ZE bit is 1 and the POECMPEX4.POEREQ3 bit or the POECMPSEL.POEREQ3 bit is 1.
- Detection of oscillation stop
  When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(34) GPT2 pin PB5 (GTIOC2B)

When one of the following conditions is satisfied while the POECR3.GPT2B1ZE bit is 1, the pin becomes high-impedance. Furthermore, when one of the following conditions is satisfied while the POECR3.GPT2B1ZE bit is 0 and the PMMCR2.GPT2B1ME bit is 1, the pin is switched to general I/O port pin.

- Operation for detection of the POE11# input level
  When the ICSR5.POE11F flag becomes 1 while the ICSR5.POE11E bit is 1.
- SPOER setting
  When the SPOER.GPT03HIZ bit is set to 1.
- Conditions added by POECR6
  When the ICSR1.POE0F flag becomes 1 while the POECR6.IC1ADDGPT03ZE bit is 1.
  When the ICSR2.POE4F flag becomes 1 while the POECR6.IC2ADDGPT03ZE bit is 1.
  When the ICSR3.POE8F flag becomes 1 while the POECR6.IC3ADDGPT03ZE bit and the ICSR3.POE8E bit are 1.
  When the ICSR4.POE10F flag becomes 1 while the POECR6.IC4ADDGPT03ZE bit and the ICSR4.POE10E bit are 1.
  When the ICSR7.POE12F flag becomes 1 while the POECR6.IC6ADDGPT03ZE bit and the ICSR7.POE12E bit are 1.
- Comparator output detection
  When the POECMPFR.C0FLAG flag becomes 1 while the POECR6.CMADDGPT03ZE bit is 1 and the POECMPEX4.POEREQ0 bit or the POECMPSEL.POEREQ0 bit is 1.
  When the POECMPFR.C1FLAG flag becomes 1 while the POECR6.CMADDGPT03ZE bit is 1 and the POECMPEX4.POEREQ1 bit or the POECMPSEL.POEREQ1 bit is 1.
  When the POECMPFR.C2FLAG flag becomes 1 while the POECR6.CMADDGPT03ZE bit is 1 and the POECMPEX4.POEREQ2 bit or the POECMPSEL.POEREQ2 bit is 1.
  When the POECMPFR.C3FLAG flag becomes 1 while the POECR6.CMADDGPT03ZE bit is 1 and the POECMPEX4.POEREQ3 bit or the POECMPSEL.POEREQ3 bit is 1.
- Detection of oscillation stop
  When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(35) GPT3 pin PD7 (GTIOC3A)

When one of the following conditions is satisfied while the POECR3.GPT3A1ZE bit is 1, the pin becomes high-impedance. Furthermore, when one of the following conditions is satisfied while the POECR3.GPT3A1ZE bit is 0 and the PMMCR2.GPT3A1ME bit is 1, the pin is switched to general I/O port pin.

- Operation for detection of the POE11# input level
  When the ICSR5.POE11F flag becomes 1 while the ICSR5.POE11E bit is 1.

- SPOER setting
  When the SPOER.GPT03HIZ bit is set to 1.
- Conditions added by POECR6
  When the ICSR1.POE0F flag becomes 1 while the POECR6.IC1ADDGPT03ZE bit is 1.
  When the ICSR2.POE4F flag becomes 1 while the POECR6.IC2ADDGPT03ZE bit is 1.
  When the ICSR3.POE8F flag becomes 1 while the POECR6.IC3ADDGPT03ZE bit and the ICSR3.POE8E bit are 1.
  When the ICSR4.POE10F flag becomes 1 while the POECR6.IC4ADDGPT03ZE bit and the ICSR4.POE10E bit are 1.
  When the ICSR7.POE12F flag becomes 1 while the POECR6.IC6ADDGPT03ZE bit and the ICSR7.POE12E bit are 1.
- Comparator output detection
  When the POECMPFR.C0FLAG flag becomes 1 while the POECR6.CMADDGPT03ZE bit is 1 and the POECMPEX4.POEREQ0 bit or the POECMPSEL.POEREQ0 bit is 1.
  When the POECMPFR.C1FLAG flag becomes 1 while the POECR6.CMADDGPT03ZE bit is 1 and the POECMPEX4.POEREQ1 bit or the POECMPSEL.POEREQ1 bit is 1.
  When the POECMPFR.C2FLAG flag becomes 1 while the POECR6.CMADDGPT03ZE bit is 1 and the POECMPEX4.POEREQ2 bit or the POECMPSEL.POEREQ2 bit is 1.
  When the POECMPFR.C3FLAG flag becomes 1 while the POECR6.CMADDGPT03ZE bit is 1 and the POECMPEX4.POEREQ3 bit or the POECMPSEL.POEREQ3 bit is 1.
- Detection of oscillation stop
  When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(36) GPT2 pin PD6 (GTIOC3B)

When one of the following conditions is satisfied while the POECR3.GPT3B1ZE bit is 1, the pin becomes high-impedance. Furthermore, when one of the following conditions is satisfied while the POECR3.GPT3B1ZE bit is 0 and the PMMCR2.GPT3B1ME bit is 1, the pin is switched to general I/O port pin.

- Operation for detection of the POE11# input level
  When the ICSR5.POE11F flag becomes 1 while the ICSR5.POE11E bit is 1.
- SPOER setting
  When the SPOER.GPT03HIZ bit is set to 1.
- Conditions added by POECR6
  When the ICSR1.POE0F flag becomes 1 while the POECR6.IC1ADDGPT03ZE bit is 1.
  When the ICSR2.POE4F flag becomes 1 while the POECR6.IC2ADDGPT03ZE bit is 1.
  When the ICSR3.POE8F flag becomes 1 while the POECR6.IC3ADDGPT03ZE bit and the ICSR3.POE8E bit are 1.
  When the ICSR4.POE10F flag becomes 1 while the POECR6.IC4ADDGPT03ZE bit and the ICSR4.POE10E bit are 1.
  When the ICSR7.POE12F flag becomes 1 while the POECR6.IC6ADDGPT03ZE bit and the ICSR7.POE12E bit are 1.
- Comparator output detection
  When the POECMPFR.C0FLAG flag becomes 1 while the POECR6.CMADDGPT03ZE bit is 1 and the POECMPEX4.POEREQ0 bit or the POECMPSEL.POEREQ0 bit is 1.
  When the POECMPFR.C1FLAG flag becomes 1 while the POECR6.CMADDGPT03ZE bit is 1 and the POECMPEX4.POEREQ1 bit or the POECMPSEL.POEREQ1 bit is 1.
  When the POECMPFR.C2FLAG flag becomes 1 while the POECR6.CMADDGPT03ZE bit is 1 and the POECMPEX4.POEREQ2 bit or the POECMPSEL.POEREQ2 bit is 1.
  When the POECMPFR.C3FLAG flag becomes 1 while the POECR6.CMADDGPT03ZE bit is 1 and the POECMPEX4.POEREQ3 bit or the POECMPSEL.POEREQ3 bit is 1.

- Detection of oscillation stop
  When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

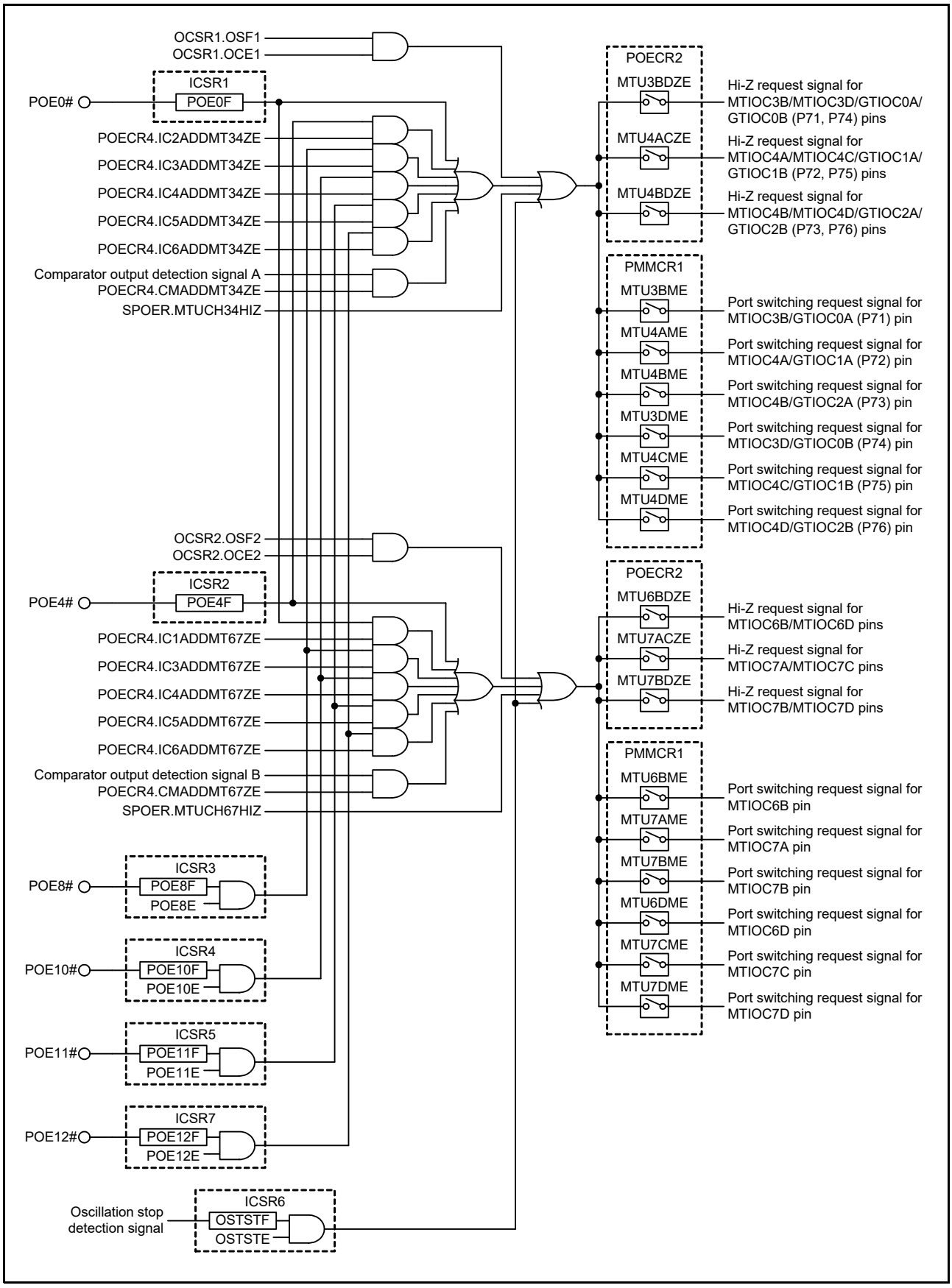


Figure 21.2 Target Pins and Conditions for High-Impedance Control (1)

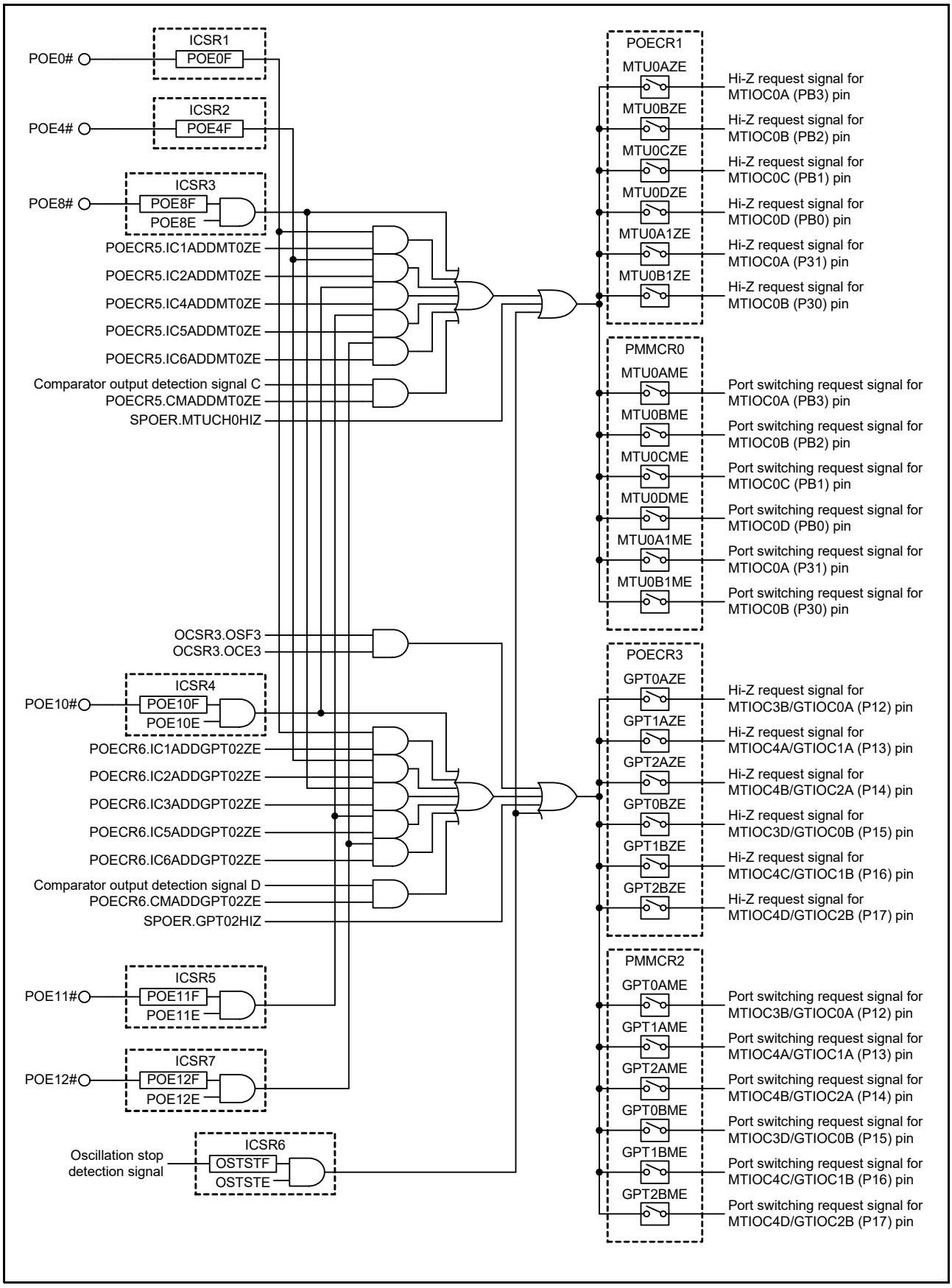


Figure 21.3 Target Pins and Conditions for High-Impedance Control (2)

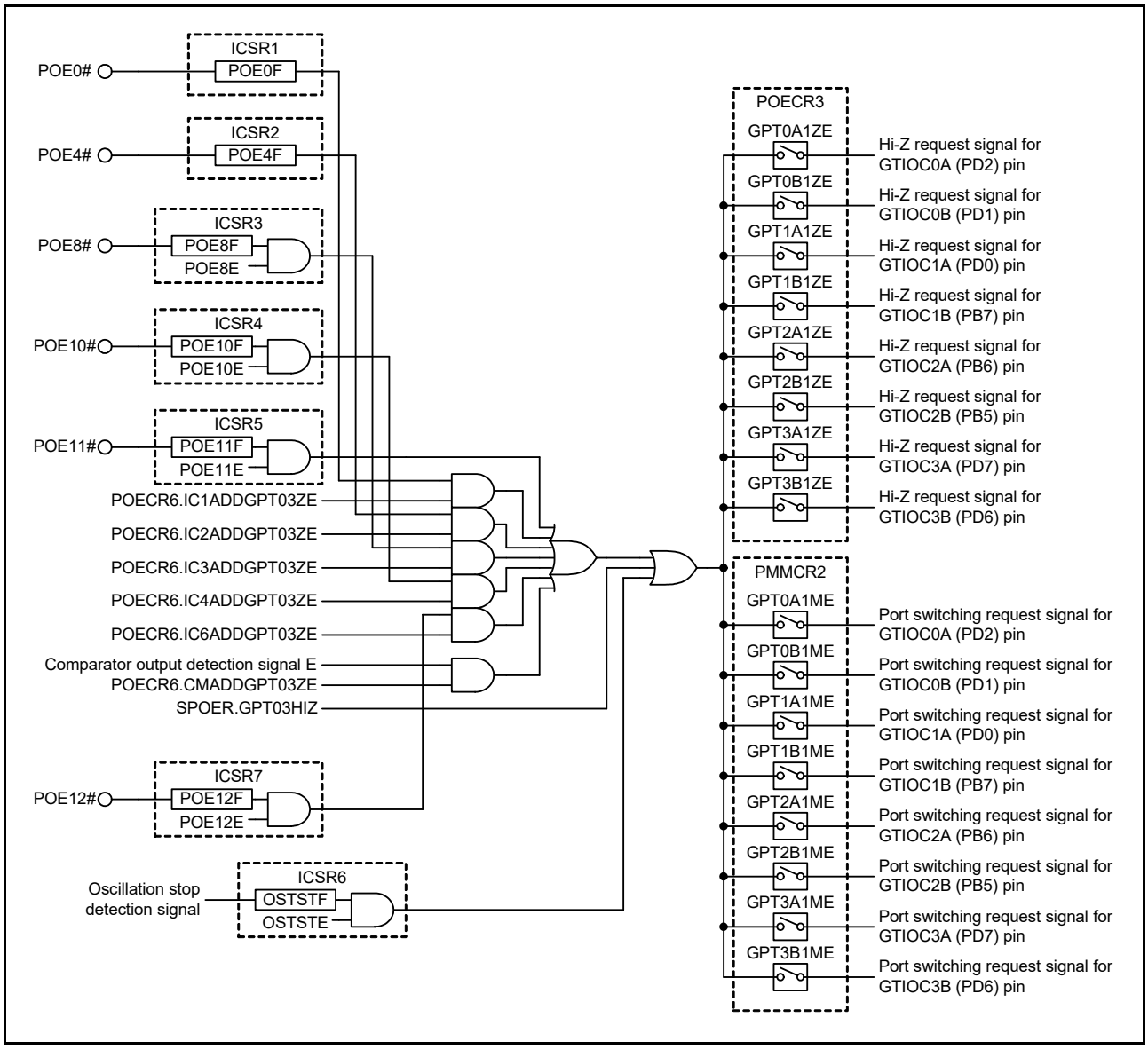


Figure 21.4 Target Pins and Conditions for High-Impedance Control (3)

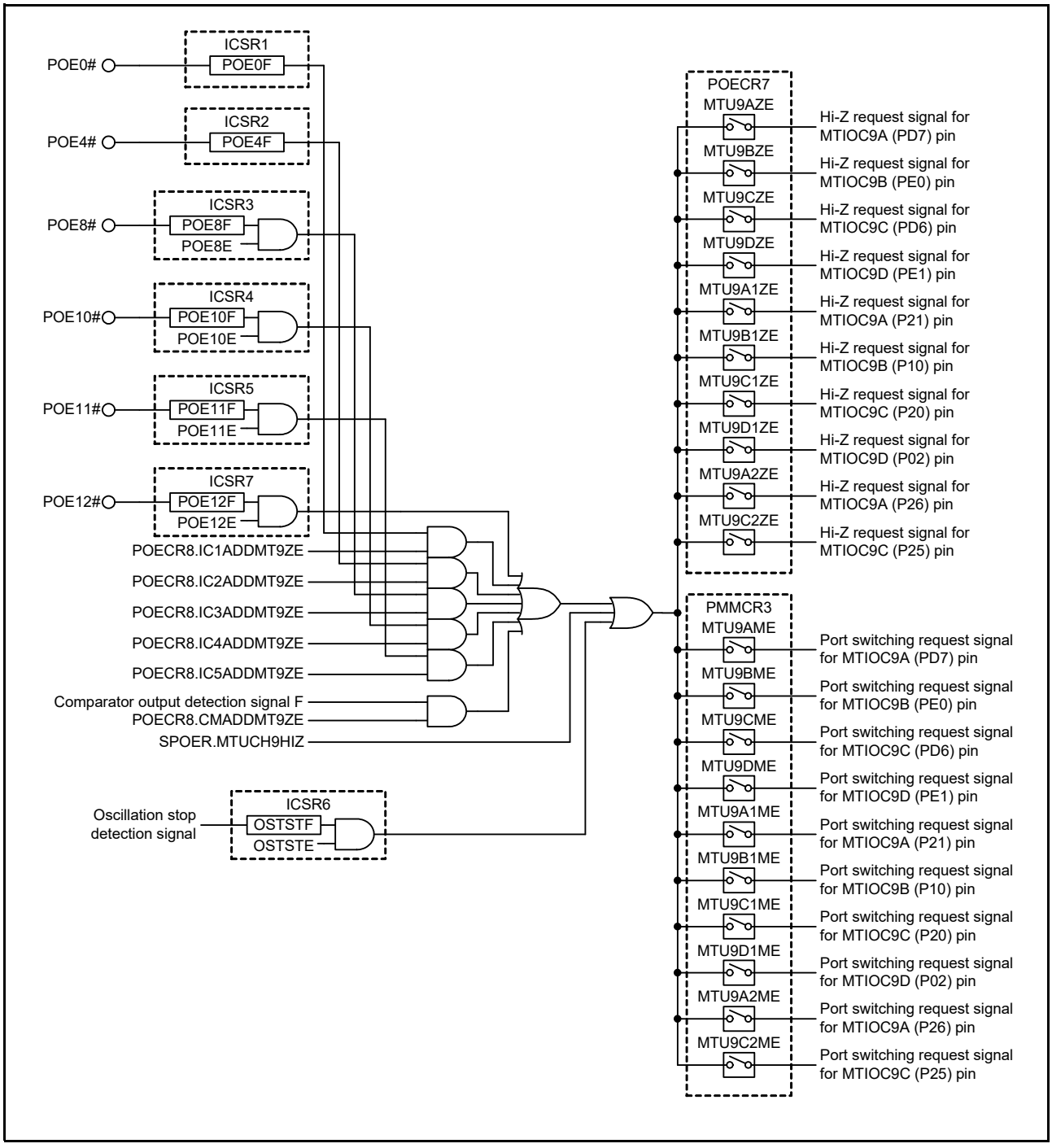


Figure 21.5 Target Pins and Conditions for High-Impedance Control (4)

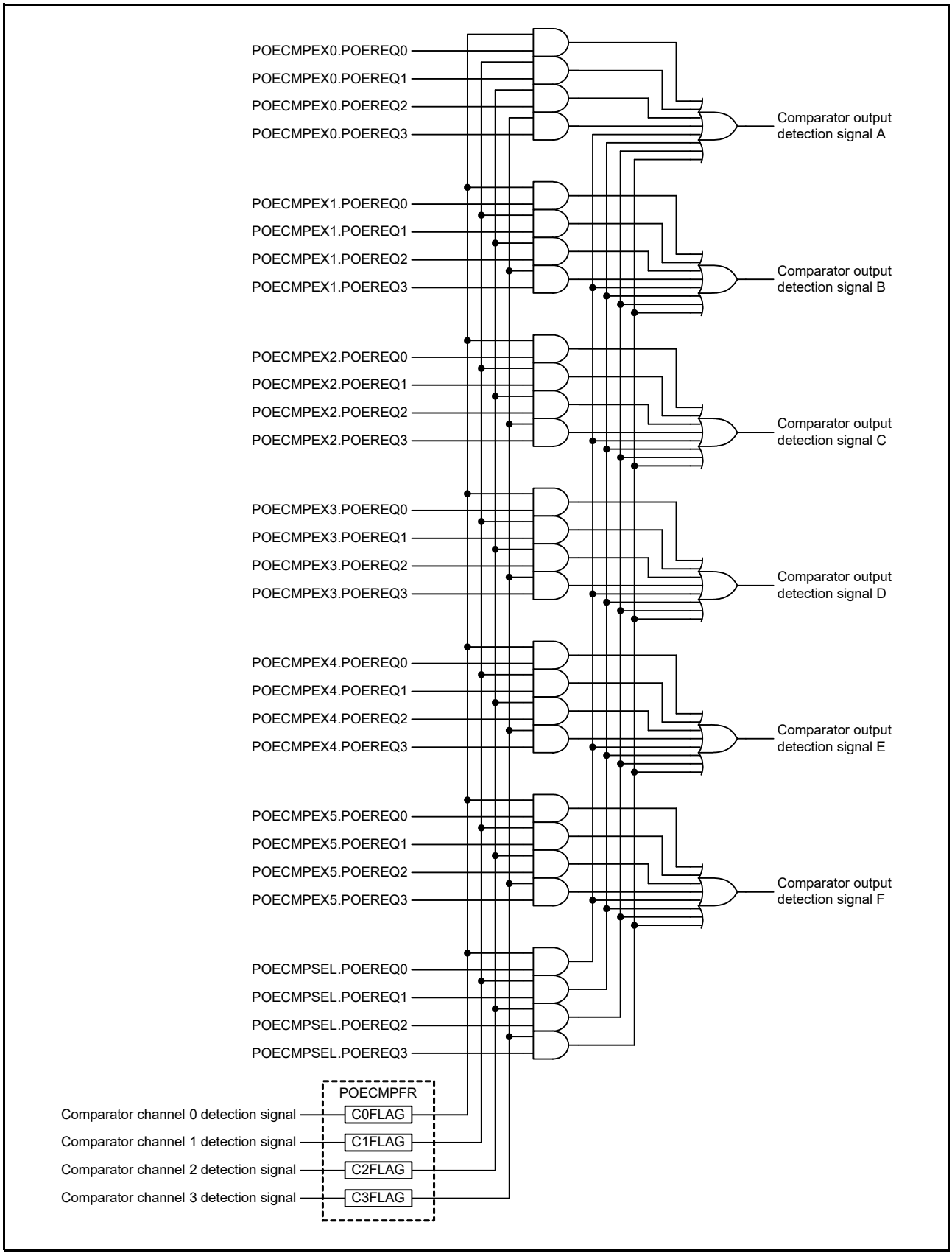


Figure 21.6 Comparator Output Detection Signal Generator Block Diagram

21.3.1 Input-Level Detection Operation

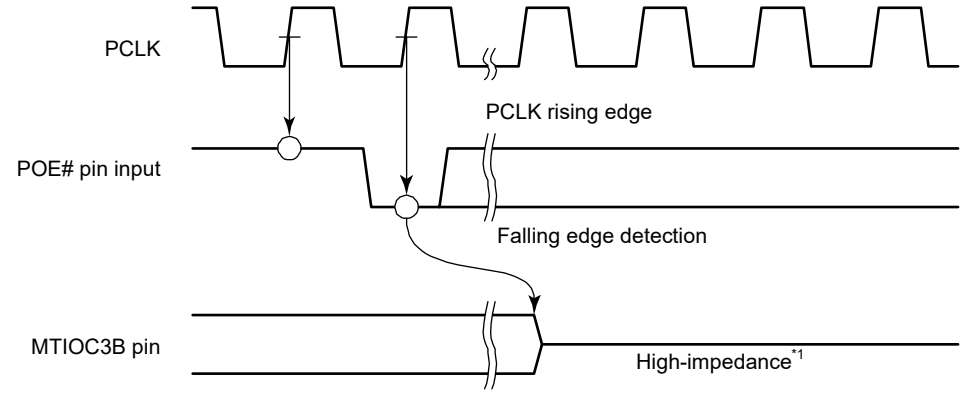
If the input conditions set by ICSR1 to ICSR5 and ICSR7 occur on the POE0#, POE4#, POE8#, POE10#, POE11#, and POE12# pins, the outputs of the MTU complementary PWM output pins (MTU3 and MTU4 or MTU6 and MTU7), MTU0 pins, MTU9 pins, and GPT pins are disabled. Note however, that these outputs are still disabled even when the MTU and GPT functions are not selected for the pins.

(1) Falling Edge Detection

When a change from a high to low level is input to the POE0#, POE4#, POE8#, POE10#, POE11#, and POE12# pins, the outputs of the pins multiplexed with MTU complementary PWM output pins, MTU0 pins, MTU9 pins, and GPT pins are disabled.

The falling edge is detected after the level is sampled with PCLK. Input a low level for at least one PCLK clock to the POE0#, POE4#, POE8#, POE10#, POE11#, and POE12# pins.

Figure 21.7 shows a sample timing after the level changes in input to the POE0#, POE4#, POE8#, POE10#, POE11#, and POE12# pins until the respective pins become high-impedance.



Note 1. Other pins also become high-impedance at the same timing.

Figure 21.7 Operation when A Falling Edge Detection and High-Impedance are Selected

(2) Low-Level Detection

Figure 21.8 shows an example of operation when a pin is placed in the high-impedance state in response to low-level detection. When 16 continuous low levels are sampled with the sampling clock selected by the ICSR1 to ICSR5 and ICSR7 registers, the low level is recognized and the outputs of the MTU complementary PWM output pins, MTU0 pins, MTU9 pins, and GPT pins are disabled. If even one high level is detected during this interval, the low level is not recognized.

The timing when the outputs of the MTU complementary PWM output pins, MTU0 pins, MTU9 pins, and GPT pins are disabled after the sampling clock is input is the same in both falling-edge detection and in low-level detection.

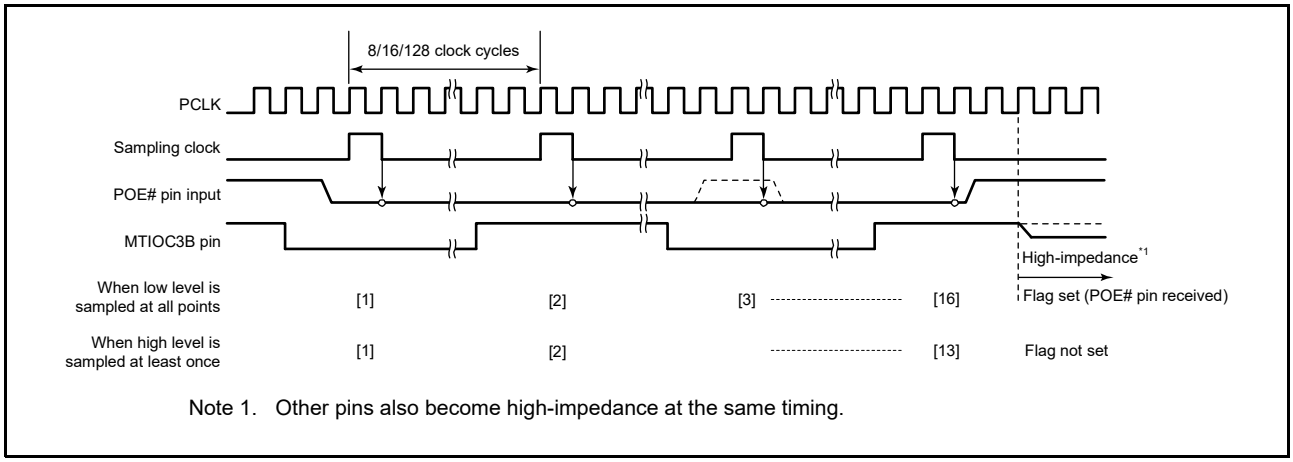


Figure 21.8 Operation when A Low-Level Detection and High-Impedance are Selected

21.3.2 Output-Level Compare Operation

Figure 21.9 shows an example of the output-level compare operation for the combination of MTIOC3B and MTIOC3D. The operation is the same for the other pin combinations and switching to general I/O ports.

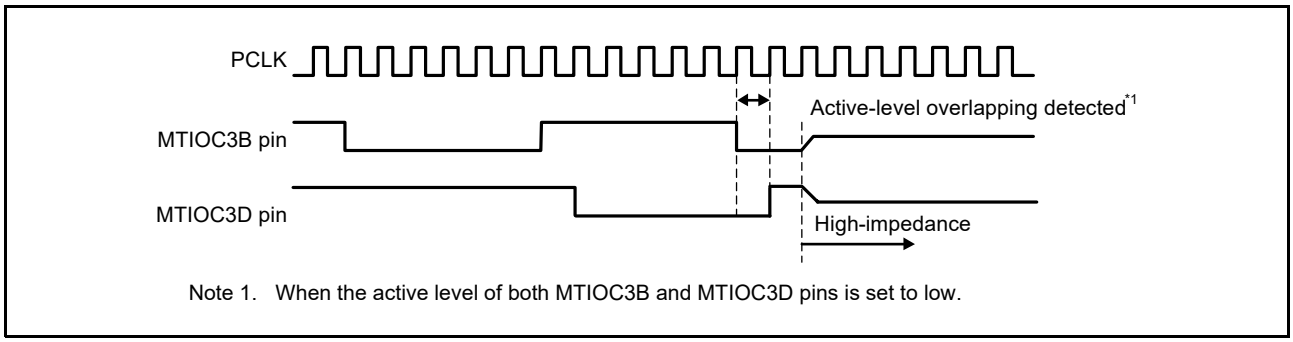


Figure 21.9 Output-Level Compare Operation

21.3.3 Output Disabling Control Using Registers

The output disabling request of the MTU pins (MTU0, MTU3, MTU4, MTU6, MTU7, and MTU9) and the GPT pins can be directly controlled by using the SPOER register.
For instance, setting the SPOER.MTUCH34HIZ bit to 1 switches the MTU3 and MTU4 pins specified by the POECR2 register to the high-impedance state.
The output disabling request of other pins can also be controlled by setting the appropriate bits in the SPOER register.

21.3.4 Output Disabling Control through Detection of Oscillation Stop

When oscillation stop is detected by the oscillation stop detection function of the clock generator while the ICSR6.OSTSTE bit is 1, the MTU complementary PWM output pins specified by the POECR2 register, the MTU0 pins specified by the POECR1 register, the MTU9 pins specified by the POECR7 register, and the GPT pins specified by the POECR3 register are switched to the high-impedance state, and the MTU complementary PWM output pins, MTU0 pins, MTU9 pins, and GPT pins specified by the PMMCR0 to PMMCR3 registers are switched to the general I/O port pins.

21.3.5 Output Disabling Control through Detection of the Comparator Output

The outputs of the MTU complementary PWM output pins, MTU0, MTU9, and GPT pins can be disabled in response to detection of the output from the comparator.
For instance, when the POECMPFR.CnFLAG flag (n = 0 to 3) is added to the output disabling control conditions for the MTU3 and MTU4 pins by setting the POECR4.CMADDMT34ZE bit to 1, the MTU3 and MTU4 pins specified by the POECR2 register become high-impedance and the MTU3 and MTU4 pins specified by the PMMCR1 register are switched to general I/O port pins on comparator output detection.
The output disabling control of other pins can be controlled by the POECR1 to POECR8 registers and the PMMCR0 to PMMCR3 registers.

21.3.6 Additional Functions for Output Disabling Control

Output disabling control conditions for the MTU complementary PWM output pins, MTU0 pins, MTU9 pins, and GPT pins can be added by setting the POECR4 to POECR6, and POECR8 registers.
For instance, the settings listed below can be added as output disabling control conditions for the MTU3 and MTU4 pins.

- Setting the POECR4.CMADDMT34ZE bit to 1 adds comparator output detection
- Setting the POECR4.IC2ADDMT34ZE bit to 1 adds the input-level detection by the POE4# pin
- Setting the POECR4.IC3ADDMT34ZE bit to 1 and adds the input-level detection by the POE8# pin
- Setting the POECR4.IC4ADDMT34ZE bit to 1 and adds the input-level detection by the POE10# pin
- Setting the POECR4.IC5ADDMT34ZE bit to 1 and adds the input-level detection by the POE11# pin
- Setting the POECR4.IC6ADDMT34ZE bit to 1 and adds the input-level detection by the POE12# pin

The output disabling control of other pins can also be controlled by setting the appropriate bits in the POECR4 to POECR6, and POECR8 registers.

21.3.7 Control in Response to an Output Disabling Request

When a request to disable outputs is generated due to one of source conditions above being satisfied, those pins for which the corresponding bits of the POECR1 to POECR3, and POECR7 registers is set to 1 become high-impedance and those pins for which the corresponding bits of the PMMCR0 to PMMCR3 registers are set to 1 are switched to general I/O port pins.
When both bits are set to 1 for the same pin, the settings of the POECR1 to POECR3 and POECR7 registers take priority and the pins become high-impedance.
After a pin is switched to a general I/O port pin, the settings of the corresponding bits in the PDR and PODR registers determine the state of the pin.

21.3.8 Recover from Output Disabled State

The outputs which have been disabled due to input-level detection can be recovered from the state either by returning them to their initial state with a reset, or by clearing all of the ICSR1.POE0F, ICSR2.POE4F, ICSR3.POE8F, ICSR4.POE10F, ICSR5.POE11F, and ICSR7.POE12F flags. However, note that when low-level sampling is selected with the ICSR1.POE0M[1:0], ICSR2.POE4M[1:0], ICSR3.POE8M[1:0], ICSR4.POE10M[1:0], ICSR5.POE11M[1:0], and ICSR7.POE12#[1:0] bits, just writing 0 to a flag is ignored (the flag is not set to 0); flags can be cleared by writing 0 to it only after a high level is input to the POE0#, POE4#, POE8#, POE10#, POE11#, and POE12# pins and is detected.
The outputs which have been disabled due to output-level detection can be recovered from the state either by returning them to their initial state with a reset, or by setting the OCSR1.OSF1 flag, the OCSR2.OSF2 flag, or the OCSR3.OSF3 flag to 0. However, note that just writing 0 to a flag is ignored (the flag is not set to 0); the flags can be cleared by writing 0 to it only after setting the inactive level to be output from the pin. In the MTU, the inactive level (initial output level) can be output by stopping the count operation. In the GPT, the inactive level can be output in accordance with the procedure described in section 22.7.2, Pin Initialization Due to Error during Operation.
The outputs which have been disabled due to comparator output detection can be recovered from the state either by returning them to their initial state with a reset or by setting the POECMPFR.CnFLAG flag (n = 0 to 3) to 0.
When setting the POECMPFR.CnFLAG flag to 0, be sure to confirm that the analog input signal that triggered comparator output detection has returned to a normal value by performing A/D conversion and so on.
Note that the above POECMPFR.CnFLAG flag is not set to 1 again in the following cases:
- This flag is cleared without confirmation that the analog input signal has returned to a normal value, and
 1. the analog input signal remains above the reference voltage when the comparator is set to non-inverted output, or
 2. the analog input signal remains below the reference voltage when the comparator is set to inverted output.

The outputs which have been disabled due to oscillation stop detection can be recovered from the state either by returning them to their initial state with a reset or by setting the SYSTEM.OSTDSR.OSTDF flag to 0 to set the ICSR6.OSTSTF flag to 0.

21.4 POE Setting Procedure

Figure 21.10 shows the procedure for setting the POE. It illustrates an example of high-impedance control in response to comparison of the output levels on the MTU3 pins (MTIOC3B/MTIOC3D). In the figure, P71 is used as the MTIOC3B pin and P74 is used as the MTIOC3D pin.

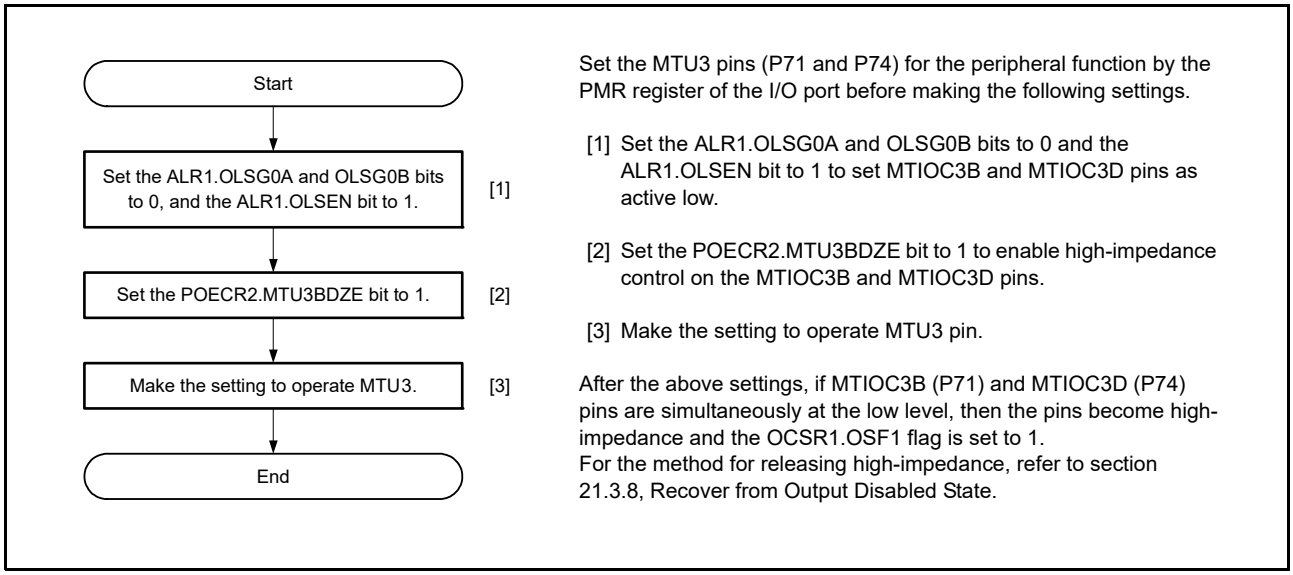


Figure 21.10 Procedure for Setting the POE

21.5 Interrupts

The POE issues a request to generate an interrupt when the specified condition is satisfied during input-level detection or output-level comparison. Table 21.5 shows the interrupt sources and their conditions.

Table 21.5 Interrupt Sources and Conditions

Name	Interrupt Source	Interrupt Flag	Condition
OEI1	Output enable interrupt 1	POE0F OSF1	When the ICSR1.POE0F flag becomes 1 while the ICSR1.PIE1 bit is 1 or when the OCSR1.OSF1 flag becomes 1 while the OCSR1.OIE1 bit is 1
OEI2	Output enable interrupt 2	POE4F OSF2	When the ICSR2.POE4F flag becomes 1 while the ICSR2.PIE2 bit is 1 or when the OCSR2.OSF2 flag becomes 1 while the OCSR2.OIE2 bit is 1
OEI3	Output enable interrupt 3	POE8F	When the ICSR3.POE8F flag becomes 1 while the ICSR3.PIE3 bit is 1
OEI4	Output enable interrupt 4	POE10F POE11F OSF3	When the ICSR4.POE10F flag is set to 1 while the ICSR4.PIE4 bit is 1, when the ICSR5.POE11F flag becomes 1 while the ICSR5.PIE5 bit is 1, or when the OCSR3.OSF3 flag becomes 1 while the OCSR3.OIE3 bit is 1
OEI5	Output enable interrupt 5	POE4F POE12F	When the ICSR2.POE4F flag becomes 1 while the ICSR2.PIE2 bit is 1 or when the ICSR7.POE12F flag becomes 1 while the ICSR7.PIE7 bit is 1

21.6 Usage Notes

21.6.1 Transition to Low Power Consumption Mode

When the POE is used, do not make a transition to software standby mode. In this mode, the POE stops and thus the output disabling control of pins cannot operate.

21.6.2 Output Disabling Control When the MTU and GPT Pins are Not Selected

If output disabling control for a pin having a multiplexed MTU or GPT pin function is enabled by setting the POECR1 to POECR3, and POECR7 registers or the PMMCR0 to PMMCR3 registers and the output disabling control condition is satisfied, the output is to be disabled even if the MTU/GPT function is not selected for the pin on which it is multiplexed. To avoid unintended output disabling, ensure that there are no differences between the settings for MTU and GPT pin selection in the PmnPFS registers of the MPC and for MTU and GPT pin selection in the pin select register of the POE.

21.6.3 When the POE is Not Used

The output disabling control of some pins can be enabled using the POE after a reset. When the POE is not used, write 0 to the target bits in the POECR1 to POECR3, and POECR7 registers and the PMMCR0 to PMMCR3 registers.

21.6.4 Active Level Setting with MTU Inversion Output Setting

In this MCU, non-inverted or inverted output can be selected for the MTU by the setting of the MPC.PmnPFS register. If inverted output is selected, the active level set in the MTU.TOCR1j and MTU.TOCR2j registers (j = A, B) and the active level of the signals output to the pins are inverted. In this case, if detection of simultaneous conduction is to be used, set the active levels based on those of the signals output to the pins by the ALR1 to ALR3 registers.

22. General PWM Timer (GPTB)

This MCU has a general PWM timer (GPTB) consisting of a four-channel 16-bit timer.
The GPT operates at a maximum of 80 MHz.

22.1 Overview

Table 22.1 lists the specifications for the GPT, and Table 22.2 shows the functions of the GPT. Figure 22.1 shows a block diagram of the GPT.

Table 22.1 GPT Specifications

Item	Description
Functions	• Selectable from 16 bits × 4 channels, 16 bits × 2 channels + 32 bits × 1 channel, and 32 bits × 2 channels • Up-counting or down-counting (saw waves) or up/down-counting (triangle waves) for each counter. • Operating mode Saw-wave PWM mode Saw-wave one-shot pulse mode Triangle-wave PWM mode 1 Triangle-wave PWM mode 2 Triangle-wave PWM mode 3 • Clock sources (nine internal clocks and four external clocks) independently selectable for each channel • Two I/O pins per channel • Noise filter can be set on each input path. • Two output compare/input capture registers per channel • For the two output compare/input capture registers of each channel, four registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at crests or troughs, enabling the generation of laterally asymmetric PWM waveforms. • Registers for setting up frame cycles in each channel (with capability for generating interrupts at overflow or underflow) • Synchronous operation of the several counters • Synchronous operation modes: simultaneous start or phase shifting start by desired times • Generation of dead times in PWM operation • Through combination of three counters, generation of three-phase PWM waveforms incorporating dead times • Starting, clearing, and stopping counters in response to external or internal triggers (hardware sources) • Internal trigger sources: comparator output, MTU count start, software, and compare match

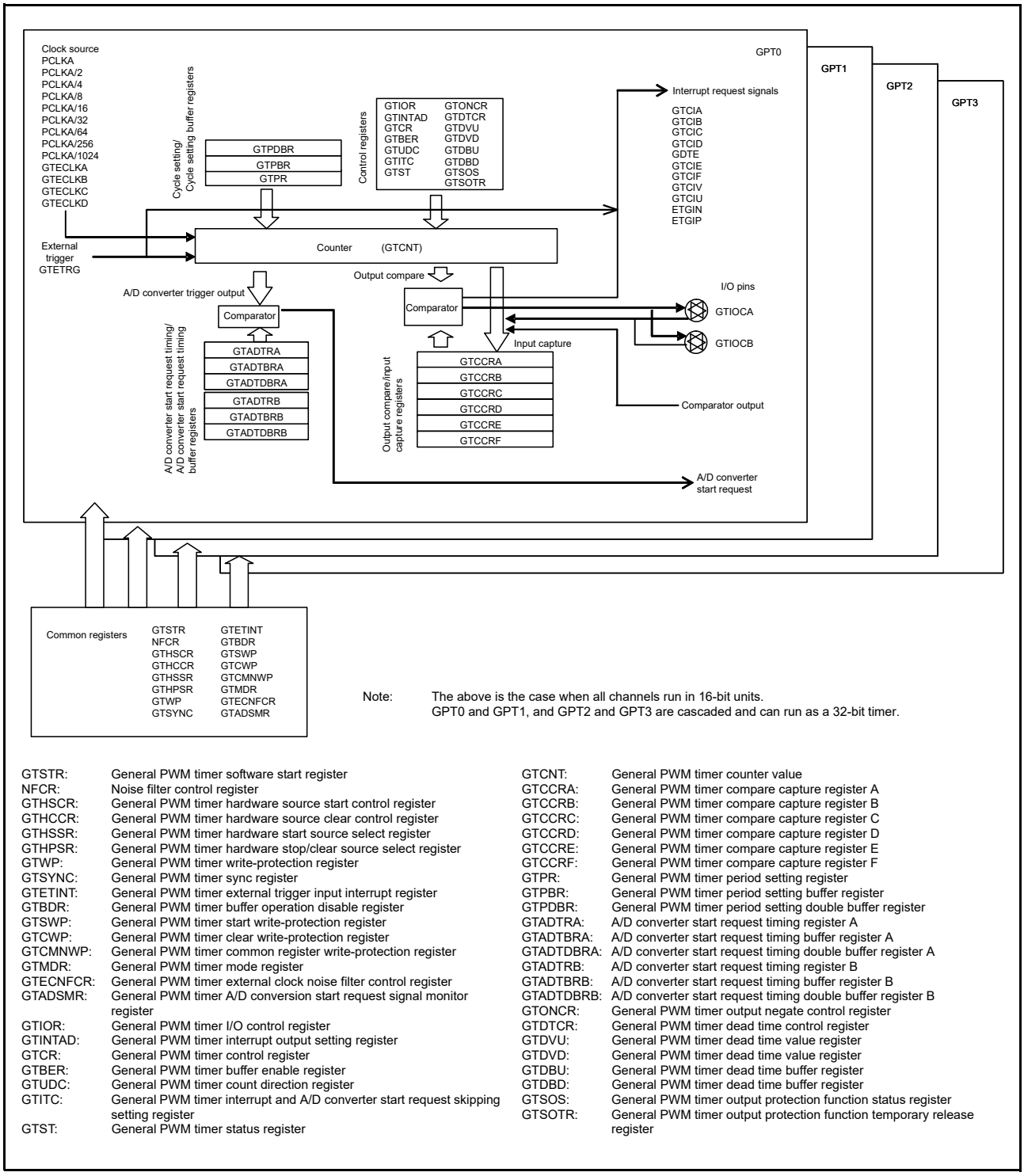
Table 22.2 GPT Functions (1/2)

	GTMDR.LWA01 = 0		LWA01 = 1	GTMDR.LWA23 = 0		LWA23 = 1
Item	**GPT0**	**GPT1**	**GPT01**	**GPT2**	**GPT3**	**GPT23**
Count clocks	PCLKA PCLKA/2 PCLKA/4 PCLKA/8 PCLKA/16 PCLKA/32 PCLKA/64 PCLKA/256 PCLKA/1024 GTECLKA GTECLKB GTECLKC GTECLKD	PCLKA PCLKA/2 PCLKA/4 PCLKA/8 PCLKA/16 PCLKA/32 PCLKA/64 PCLKA/256 PCLKA/1024 GTECLKA GTECLKB GTECLKC GTECLKD	PCLKA PCLKA/2 PCLKA/4 PCLKA/8 PCLKA/16 PCLKA/32 PCLKA/64 PCLKA/256 PCLKA/1024 GTECLKA GTECLKB GTECLKC GTECLKD	PCLKA PCLKA/2 PCLKA/4 PCLKA/8 PCLKA/16 PCLKA/32 PCLKA/64 PCLKA/256 PCLKA/1024 GTECLKA GTECLKB GTECLKC GTECLKD	PCLKA PCLKA/2 PCLKA/4 PCLKA/8 PCLKA/16 PCLKA/32 PCLKA/64 PCLKA/256 PCLKA/1024 GTECLKA GTECLKB GTECLKC GTECLKD	PCLKA PCLKA/2 PCLKA/4 PCLKA/8 PCLKA/16 PCLKA/32 PCLKA/64 PCLKA/256 PCLKA/1024 GTECLKA GTECLKB GTECLKC GTECLKD
Output compare/ input capture registers (GTCCR)	GTCCRA GTCCRB	GTCCRA GTCCRB	GTCCRALW GTCCRBLW	GTCCRA GTCCRB	GTCCRA GTCCRB	GTCCRALW GTCCRBLW
Compare/buffer registers	GTCCRC GTCCRD GTCCRE GTCCRF	GTCCRC GTCCRD GTCCRE GTCCRF	GTCCRCLW GTCCRDLW GTCCRELW GTCCRFLW	GTCCRC GTCCRD GTCCRE GTCCRF	GTCCRC GTCCRD GTCCRE GTCCRF	GTCCRCLW GTCCRDLW GTCCRELW GTCCRFLW
PWM period setting register	GTPR	GTPR	GTPRLW	GTPR	GTPR	GTPRLW
PWM period setting buffer registers	GTPBR GTPDBR	GTPBR GTPDBR	GTPBRLW GTPDBRLW	GTPBR GTPDBR	GTPBR GTPDBR	GTPBRLW GTPDBRLW
I/O pins	GTIOC0A GTIOC0B	GTIOC1A GTIOC1B	GTIOC1A GTIOC1B	GTIOC2A GTIOC2B	GTIOC3A GTIOC3B	GTIOC3A GTIOC3B
External trigger input pin	GTETRG					
Counter clear sources	GTPR register compare match, input capture, comparator output, GTETRG pin input, GTIOC3A/GTIOC3B pin input, and GTIOC3A/GTIOC3B internal output (output compare)					
Compare match output: Low output	✓	✓	✓	✓	✓	✓
Compare match output: High output	✓	✓	✓	✓	✓	✓
Compare match output: Toggle output	✓	✓	✓	✓	✓	✓
Input capture function	✓	✓	✓	✓	✓	✓
Synchronous operation	✓	✓	✓	✓	✓	✓
Phase shift start	✓	✓	✓	✓	✓	✓
Automatic addition of dead time	✓	✓	✓	✓	✓	✓
PWM mode	✓	✓	✓	✓	✓	✓
Buffer operation	✓	✓	✓	✓	✓	✓
One-shot operation	✓	✓	✓	✓	✓	✓
DTC activation	All interrupt sources except for external trigger rising input interrupt, external trigger falling input interrupt, and the dead time error interrupts					
A/D converter start trigger	Compare match of GTADTRA or GTADTRB	Compare match of GTADTRA or GTADTRB	Compare match of GTADTRALW or GTADTRBLW	Compare match of GTADTRA or GTADTRB	Compare match of GTADTRA or GTADTRB	Compare match of GTADTRALW or GTADTRBLW

Table 22.2 GPT Functions (2/2)

	GTMDR.LWA01 = 0		LWA01 = 1	GTMDR.LWA23 = 0		LWA23 = 1
Item	**GPT0**	**GPT1**	**GPT01**	**GPT2**	**GPT3**	**GPT23**
Interrupt sources	Nine sources • GTCCRA compare match/ input capture (GTCIA0) • GTCCRB compare match/ input capture (GTCIB0) • GTCCRC compare match (GTCIC0) • GTCCRD compare match (GTCID0) • Dead time error (GDTE0) • GTCCRE compare match (GTCIE0) • GTCCRF compare match (GTCIF0) • GTCNT overflow (GTPR compare match) (GTCIV0) • GTCNT underflow (GTCIU0)	Nine sources • GTCCRA compare match/ input capture (GTCIA1) • GTCCRB compare match/ input capture (GTCIB1) • GTCCRC compare match (GTCIC1) • GTCCRD compare match (GTCID1) • Dead time error (GDTE1) • GTCCRE compare match (GTCIE1) • GTCCRF compare match (GTCIF1) • GTCNT overflow (GTPR compare match) (GTCIV1) • GTCNT underflow (GTCIU1)	Nine sources • GTCCRALW compare match/ input capture (GTCIA1) • GTCCRBLW compare match/ input capture (GTCIB1) • GTCCRCLW compare match (GTCIC1) • GTCCRDLW compare match (GTCID1) • Dead time error (GDTE1) • GTCCRELW compare match (GTCIE1) • GTCCRFLW compare match (GTCIF1) • GTCNTLW overflow (GTPR compare match) (GTCIV1) • GTCNTLW underflow (GTCIU1)	Nine sources • GTCCRA compare match/ input capture (GTCIA2) • GTCCRB compare match/ input capture (GTCIB2) • GTCCRC compare match (GTCIC2) • GTCCRD compare match (GTCID2) • Dead time error (GDTE2) • GTCCRE compare match (GTCIE2) • GTCCRF compare match (GTCIF2) • GTCNT overflow (GTPR compare match) (GTCIV2) • GTCNT underflow (GTCIU2)	Nine sources • GTCCRA compare match/ input capture (GTCIA3) • GTCCRB compare match/ input capture (GTCIB3) • GTCCRC compare match (GTCIC3) • GTCCRD compare match (GTCID3) • Dead time error (GDTE3) • GTCCRE compare match (GTCIE3) • GTCCRF compare match (GTCIF3) • GTCNT overflow (GTPR compare match) (GTCIV3) • GTCNT underflow (GTCIU3)	Nine sources • GTCCRALW compare match/ input capture (GTCIA3) • GTCCRBLW compare match/ input capture (GTCIB3) • GTCCRCLW compare match (GTCIC3) • GTCCRDLW compare match (GTCID3) • Dead time error (GDTE3) • GTCCRELW compare match (GTCIE3) • GTCCRFLW compare match (GTCIF3) • GTCNTLW overflow (GTPR compare match) (GTCIV3) • GTCNTLW underflow (GTCIU3)
Common interrupt source	External trigger					
Interrupt skipping function	Skips GTCNT overflows (GTPR compare match) (GTCIV0)/GTCNT underflow (GTCIU0) interrupts (with interlocking function for other interrupts or A/D conversion requests).	Skips GTCNT overflows (GTPR compare match) (GTCIV1)/GTCNT underflow (GTCIU1) interrupts (with interlocking function for other interrupts or A/D conversion requests).	Skips GTCNTLW overflows (GTPRLW compare match) (GTCIV1)/ GTCNTLW underflow (GTCIU1) interrupts (with interlocking function for other interrupts or A/D conversion requests).	Skips GTCNT overflows (GTPR compare match) (GTCIV2)/GTCNT underflow (GTCIU2) interrupts (with interlocking function for other interrupts or A/D conversion requests).	Skips GTCNT overflows (GTPR compare match) (GTCIV3)/GTCNT underflow (GTCIU3) interrupts (with interlocking function for other interrupts or A/D conversion requests).	Skips GTCNTLW overflows (GTPRLW compare match) (GTCIV3)/ GTCNTLW underflow (GTCIU3) interrupts (with interlocking function for other interrupts or A/D conversion requests).
Noise filter function	✓	✓	✓	✓	✓	✓

✓: Possible



Note: The above is the case when all channels run in 16-bit units.
GPT0 and GPT1, and GPT2 and GPT3 are cascaded and can run as a 32-bit timer.

GTSTR:	General PWM timer software start register
NFCR:	Noise filter control register
GTHSCR:	General PWM timer hardware source start control register
GTHCCR:	General PWM timer hardware source clear control register
GTHSSR:	General PWM timer hardware start source select register
GTHPSR:	General PWM timer hardware stop/clear source select register
GTWP:	General PWM timer write-protection register
GTSYNC:	General PWM timer sync register
GTETINT:	General PWM timer external trigger input interrupt register
GTBDR:	General PWM timer buffer operation disable register
GTSWP:	General PWM timer start write-protection register
GTCWP:	General PWM timer clear write-protection register
GTCMNWP:	General PWM timer common register write-protection register
GTMDR:	General PWM timer mode register
GTECNFCR:	General PWM timer external clock noise filter control register
GTADSMR:	General PWM timer A/D conversion start request signal monitor register
GTIOR:	General PWM timer I/O control register
GTINTAD:	General PWM timer interrupt output setting register
GTCR:	General PWM timer control register
GTBER:	General PWM timer buffer enable register
GTUDC:	General PWM timer count direction register
GTITC:	General PWM timer interrupt and A/D converter start request skipping setting register
GTST:	General PWM timer status register
GTCNT:	General PWM timer counter value
GTCCRA:	General PWM timer compare capture register A
GTCCRB:	General PWM timer compare capture register B
GTCCRC:	General PWM timer compare capture register C
GTCCRD:	General PWM timer compare capture register D
GTCCRE:	General PWM timer compare capture register E
GTCCRF:	General PWM timer compare capture register F
GTPR:	General PWM timer period setting register
GTPBR:	General PWM timer period setting buffer register
GTPDBR:	General PWM timer period setting double buffer register
GTADTRA:	A/D converter start request timing register A
GTADTBRA:	A/D converter start request timing buffer register A
GTADTDBRA:	A/D converter start request timing double buffer register A
GTADTRB:	A/D converter start request timing register B
GTADTBRB:	A/D converter start request timing buffer register B
GTADTDBRB:	A/D converter start request timing double buffer register B
GTONCR:	General PWM timer output negate control register
GTDTCR:	General PWM timer dead time control register
GTDVU:	General PWM timer dead time value register
GTDVD:	General PWM timer dead time value register
GTDBU:	General PWM timer dead time buffer register
GTDBD:	General PWM timer dead time buffer register
GTSOS:	General PWM timer output protection function status register
GTSOTR:	General PWM timer output protection function temporary release register

Figure 22.1 GPT Block Diagram

Table 22.3 lists the I/O pins used in the GPT.

Table 22.3 GPT I/O Pins

Channel	Pin Name	I/O	Function
GPT	GTECLKA	Input	External clock A input pin
	GTECLKB	Input	External clock B input pin
	GTECLKC	Input	External clock C input pin
	GTECLKD	Input	External clock D input pin
	GTETRG	Input	External trigger input pin
	GTADSM0	Output	A/D conversion start request monitor 0 output pin
	GTADSM1	Output	A/D conversion start request monitor 1 output pin
GPT0	GTIOC0A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC0B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT1 (GPT01)	GTIOC1A	I/O	GTCCRA (GTCCRALW) register input capture input/output compare output/PWM output pin
	GTIOC1B	I/O	GTCCRB (GTCCRBLW) register input capture input/output compare output/PWM output pin
GPT2	GTIOC2A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC2B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT3 (GPT23)	GTIOC3A	I/O	GTCCRA (GTCCRALW) register input capture input/output compare output/PWM output pin
	GTIOC3B	I/O	GTCCRB (GTCCRBLW) register input capture input/output compare output/PWM output pin

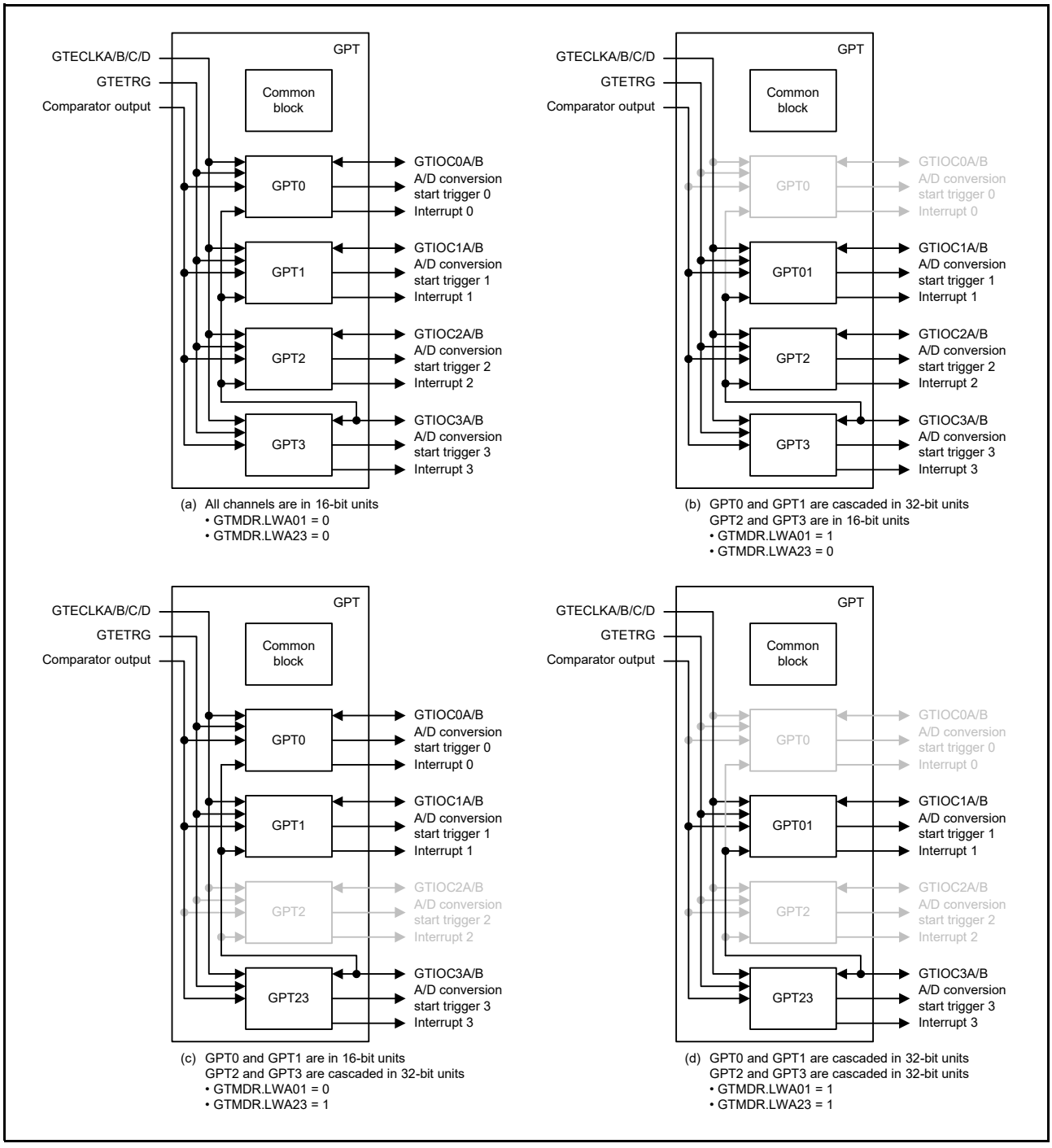


Figure 22.2 Timer Configurations

22.2 Register Descriptions

22.2.1 General PWM Timer Software Start Register (GTSTR)

Address(es): GPT.GTSTR 000C 2000h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	CST3	CST2	CST1	CST0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CST0	GPT0.GTCNT Count Start*1, *2	0: Count operation is stopped 1: Count operation is started	R/W
b1	CST1	GPT1.GTCNT/GPT01.GTCNTLW Count Start*1		R/W
b2	CST2	GPT2.GTCNT Count Start*3, *4		R/W
b3	CST3	GPT3.GTCNT/GPT23.GTCNTLW Count Start*3		R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. When changing the value of the GTMDR.LWA01 bit, the bit becomes 0.
Note 2. When the GTMDR.LWA01 bit is 1, the CST0 bit cannot be set to 1.
Note 3. When changing the value of the GTMDR.LWA23 bit, the bit becomes 0.
Note 4. When the GTMDR.LWA23 bit is 1, the CST2 bit cannot be set to 1.

The GTSTR register starts or stops the GPTn.GTCNT counter (n = 0 to 3), the GPT01.GTCNTLW counter, and the GPT23.GTCNTLW counter.

CSTn Bit (GPTn.GTCNT Count Start) (n = 0 to 3)

This bit starts or stops the GPTn.GTCNT counter, the GPT01.GTCNTLW counter, and the GPT23.GTCNTLW counter. If the GTSWP.SWPn bit is set to disable writing to the CSTn bit, writing to the CSTn bit is ignored.
The counter can also be started or stopped by a hardware source by setting the GTHSCR register. When count operation is started by a hardware source, this bit is automatically set to 1, and when count operation is stopped by a hardware source, this bit is automatically set to 0.

22.2.2 Noise Filter Control Register (NFCR)

Address(es): GPT.NFCR 000C 2002h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	NFCS3[1:0]		NFCS2[1:0]		NFCS1[1:0]		NFCS0[1:0]		NFB3EN	NFA3EN	NFB2EN	NFA2EN	NFB1EN	NFA1EN	NFB0EN	NFA0EN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	NFA0EN	Noise Filter 0A Enable*1, *2	0: The noise filter for the GTIOC0A pin is disabled. 1: The noise filter for the GTIOC0A pin is enabled.	R/W
b1	NFB0EN	Noise Filter 0B Enable*1, *2	0: The noise filter for the GTIOC0B pin is disabled. 1: The noise filter for the GTIOC0B pin is enabled.	R/W
b2	NFA1EN	Noise Filter 1A Enable*1	0: The noise filter for the GTIOC1A pin is disabled. 1: The noise filter for the GTIOC1A pin is enabled.	R/W
b3	NFB1EN	Noise Filter 1B Enable*1	0: The noise filter for the GTIOC1B pin is disabled. 1: The noise filter for the GTIOC1B pin is enabled.	R/W
b4	NFA2EN	Noise Filter 2A Enable*3, *4	0: The noise filter for the GTIOC2A pin is disabled. 1: The noise filter for the GTIOC2A pin is enabled.	R/W
b5	NFB2EN	Noise Filter 2B Enable*3, *4	0: The noise filter for the GTIOC2B pin is disabled. 1: The noise filter for the GTIOC2B pin is enabled.	R/W
b6	NFA3EN	Noise Filter 3A Enable*3	0: The noise filter for the GTIOC3A pin is disabled. 1: The noise filter for the GTIOC3A pin is enabled.	R/W
b7	NFB2EN	Noise Filter 3B Enable*3	0: The noise filter for the GTIOC3B pin is disabled. 1: The noise filter for the GTIOC3B pin is enabled.	R/W
b9, b8	NFCS0[1:0]	GPT0 Noise Filter Sampling Clock Select*2, *5	b9 b8 0 0: PCLKA/1 0 1: PCLKA/4 1 0: PCLKA/32 1 1: Clock source for counting	R/W
b11, b10	NFCS1[1:0]	GPT1 Noise Filter Sampling Clock Select*5	b11 b10 0 0: PCLKA/1 0 1: PCLKA/4 1 0: PCLKA/32 1 1: Clock source for counting	R/W
b13, b12	NFCS2[1:0]	GPT2 Noise Filter Sampling Clock Select*4, *6	b13 b12 0 0: PCLKA/1 0 1: PCLKA/4 1 0: PCLKA/32 1 1: Clock source for counting	R/W
b15, b14	NFCS3[1:0]	GPT3 Noise Filter Sampling Clock Select*6	b15 b14 0 0: PCLKA/1 0 1: PCLKA/4 1 0: PCLKA/32 1 1: Clock source for counting	R/W

Note 1. When changing the value of the GTMDR.LWA01 bit, the bit becomes 0.
Note 2. When the GTMDR.LWA01 bit is 1, the value of the bit cannot be changed.
Note 3. When changing the value of the GTMDR.LWA23 bit, the bit becomes 0.
Note 4. When the GTMDR.LWA23 bit is 1, the value of the bit cannot be changed.
Note 5. When changing the value of the GTMDR.LWA01 bit, the bits become 00b.
Note 6. When changing the value of the GTMDR.LWA23 bit, the bits become 00b.

The NFCR register controls enabling and disabling of the noise filters and selects the sampling clocks for the noise filters.

NFAnEN Bit (Noise Filter nA Enable) (n = 0 to 3)

This bit disables or enables the noise filter for input from the GTIOCnA pin. Since changing the value of the bit may lead

to the internal generation of an unexpected edge, select the output compare function for the relevant pin in the GTIOR register before doing so.

NFBnEN Bit (Noise Filter nB Enable) (n = 0 to 3)

This bit disables or enables the noise filter for input from the GTIOCnB pin. Since changing the value of this bit may lead to the internal generation of an unexpected edge, select the output compare function for the relevant pin in the GTIOR register before changing the value of the bit.

NFCSn[1:0] Bits (GPTn Noise Filter Sampling Clock Select) (n = 0 to 3)

These bits set the sampling clock for the noise filter. When changing the setting of these bits, set the corresponding pin function of the GTIOR register to output compare. After these bits are set, wait for two cycles of the selected sampling interval before setting the input capture function of the GTIOR register.

22.2.3 General PWM Timer Hardware Source Start/Stop Control Register (GTHSCR)

Address(es): GPT.GTHSCR 000C 2004h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CPHW3[1:0]		CPHW2[1:0]		CPHW1[1:0]		CPHW0[1:0]		CSHW3[1:0]		CSHW2[1:0]		CSHW1[1:0]		CSHW0[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	CSHW0[1:0]	GPT0.GTCNT Hardware Source Count Start*1, *2	b1 b0 0 0: Count operation is not started by a hardware source. 0 1: Count operation is started at the rising edge of a hardware source. 1 0: Count operation is started at the falling edge of a hardware source. 1 1: Count operation is started at both rising and falling edges of a hardware source.	R/W
b3, b2	CSHW1[1:0]	GPT1.GTCNT/GPT01.GTCNTLW Hardware Source Count Start*1	b3 b2 0 0: Count operation is not started by a hardware source. 0 1: Count operation is started at the rising edge of a hardware source. 1 0: Count operation is started at the falling edge of a hardware source. 1 1: Count operation is started at both rising and falling edges of a hardware source.	R/W
b5, b4	CSHW2[1:0]	GPT2.GTCNT Hardware Source Count Start*3, *4	b5 b4 0 0: Count operation is not started by a hardware source. 0 1: Count operation is started at the rising edge of a hardware source. 1 0: Count operation is started at the falling edge of a hardware source. 1 1: Count operation is started at both rising and falling edges of a hardware source.	R/W
b7, b6	CSHW3[1:0]	GPT3.GTCNT/GPT23.GTCNTLW Hardware Source Count Start*3	b7 b6 0 0: Count operation is not started by a hardware source. 0 1: Count operation is started at the rising edge of a hardware source. 1 0: Count operation is started at the falling edge of a hardware source. 1 1: Count operation is started at both rising and falling edges of a hardware source.	R/W
b9, b8	CPHW0[1:0]	GPT0.GTCNT Hardware Source Count Stop*1, *2	b9 b8 0 0: Count operation is not stopped by a hardware source. 0 1: Count operation is stopped at the rising edge of a hardware source. 1 0: Count operation is stopped at the falling edge of a hardware source. 1 1: Count operation is stopped at both rising and falling edges of a hardware source.	R/W
b11, b10	CPHW1[1:0]	GPT1.GTCNT/GPT01.GTCNTLW Hardware Source Count Stop*1	b11 b10 0 0: Count operation is not stopped by a hardware source. 0 1: Count operation is stopped at the rising edge of a hardware source. 1 0: Count operation is stopped at the falling edge of a hardware source. 1 1: Count operation is stopped at both rising and falling edges of a hardware source.	R/W

Bit	Symbol	Bit Name	Description	R/W
b13, b12	CPHW2[1:0]	GPT2.GTCNT Hardware Source Count Stop*3, *4	b13 b12 0 0: Count operation is not stopped by a hardware source. 0 1: Count operation is stopped at the rising edge of a hardware source. 1 0: Count operation is stopped at the falling edge of a hardware source. 1 1: Count operation is stopped at both rising and falling edges of a hardware source.	R/W
b15, b14	CPHW3[1:0]	GPT3.GTCNT/GPT23.GTCNTLW Hardware Source Count Stop*3	b15 b14 0 0: Count operation is not stopped by a hardware source. 0 1: Count operation is stopped at the rising edge of a hardware source. 1 0: Count operation is stopped at the falling edge of a hardware source. 1 1: Count operation is stopped at both rising and falling edges of a hardware source.	R/W

Note 1. When changing the value of the GTMDR.LWA01 bit, the bits become 00b.
Note 2. When the GTMDR.LWA01 bit is 1, the value of the bits cannot be changed.
Note 3. When changing the value of the GTMDR.LWA23 bit, the bits become 00b.
Note 4. When the GTMDR.LWA23 bit is 1, the value of the bits cannot be changed.

The GTHSCR register sets a hardware source to start or stop the GPTn.GTCNT counter (n = 0 to 3), the GPT01.GTCNTLW counter, and the GPT23.GTCNTLW counter.
When starting and stopping the GPTn.GTCNT counter, the GPT01.GTCNTLW counter, or the GPT23.GTCNTLW counter by a hardware source occur simultaneously, counter start is given priority.

CSHWn[1:0] Bits (GPTn.GTCNT Hardware Source Count Start) (n = 0 to 3)

The GPTn.GTCNT counter, the GPT01.GTCNTLW counter, or the GPT23.GTCNTLW counter is started by a hardware source.
When the count operation is started by a hardware source, the corresponding bit in GTSTR automatically becomes 1.
The hardware source can be selected by GTHSSR.

CPHWn[1:0] Bits (GPTn.GTCNT Hardware Source Count Stop) (n = 0 to 3)

The GPTn.GTCNT counter, the GPT01.GTCNTLW counter, or the GPT23.GTCNTLW counter is stopped by a hardware source.
When the count operation is stopped by a hardware source, the corresponding bit in GTSTR automatically becomes 0.
The hardware source can be selected by GTHPSR.

22.2.4 General PWM Timer Hardware Source Clear Control Register (GTHCCR)

Address(es): GPT.GTHCCR 000C 2006h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	CCSW3	CCSW2	CCSW1	CCSW0	CCHW3[1:0]		CCHW2[1:0]		CCHW1[1:0]		CCHW0[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	CCHW0[1:0]	GPT0.GTCNT Hardware Source Counter Clear*1, *2	b1 b0 0 0: Counter is not cleared by a hardware source. 0 1: Counter is cleared at the rising edge of a hardware source. 1 0: Counter is cleared at the falling edge of a hardware source. 1 1: Counter is cleared at both rising and falling edges of a hardware source.	R/W
b3, b2	CCHW1[1:0]	GPT1.GTCNT/GPT01.GTCNTLW Hardware Source Counter Clear*1	b3 b2 0 0: Counter is not cleared by a hardware source. 0 1: Counter is cleared at the rising edge of a hardware source. 1 0: Counter is cleared at the falling edge of a hardware source. 1 1: Counter is cleared at both rising and falling edges of a hardware source.	R/W
b5, b4	CCHW2[1:0]	GPT2.GTCNT Hardware Source Counter Clear*3, *4	b5 b4 0 0: Counter is not cleared by a hardware source. 0 1: Counter is cleared at the rising edge of a hardware source. 1 0: Counter is cleared at the falling edge of a hardware source. 1 1: Counter is cleared at both rising and falling edges of a hardware source.	R/W
b7, b6	CCHW3[1:0]	GPT3.GTCNT/GPT23.GTCNTLW Hardware Source Counter Clear*3	b7 b6 0 0: Counter is not cleared by a hardware source. 0 1: Counter is cleared at the rising edge of a hardware source. 1 0: Counter is cleared at the falling edge of a hardware source. 1 1: Counter is cleared at both rising and falling edges of a hardware source.	R/W
b8	CCSW0	GPT0.GTCNT Counter Clear*2, *5	When 1 is written to this bit, the counter is cleared. This bit automatically returns to 0 after the writing of 1. These bits are read as 0.	R/W
b9	CCSW1	GPT1.GTCNT/GPT01.GTCNTLW Counter Clear*5	When 1 is written to this bit, the counter is cleared. This bit automatically returns to 0 after the writing of 1. These bits are read as 0.	R/W
b10	CCSW2	GPT2.GTCNT Counter Clear*4, *6	When 1 is written to this bit, the counter is cleared. This bit automatically returns to 0 after the writing of 1. These bits are read as 0.	R/W
b11	CCSW3	GPT3.GTCNT/GPT23.GTCNTLW Counter Clear*6	When 1 is written to this bit, the counter is cleared. This bit automatically returns to 0 after the writing of 1. These bits are read as 0.	R/W
b15 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. When changing the value of the GTMDR.LWA01 bit, the bits become 00b.
Note 2. When the GTMDR.LWA01 bit is 1, the value of the bit cannot be changed.
Note 3. When changing the value of the GTMDR.LWA23 bit, the bits become 00b.
Note 4. When the GTMDR.LWA23 bit is 1, the value of the bit cannot be changed.
Note 5. When changing the value of the GTMDR.LWA01 bit, the bit becomes 0.
Note 6. When changing the value of the GTMDR.LWA23 bit, the bit becomes 0.

The GTHCCR register sets a hardware source to clear the GPTn.GTCNT counter (n = 0 to 3), the GPT01.GTCNTLW counter, and the GPT23.GTCNTLW counter.
Once the clearing of GPTn.GTCNT counter, the GPT01.GTCNTLW counter, or the GPT23.GTCNTLW counter by a hardware source is set, counter clearing by the hardware source is executed whether the GPTn.GTCNT counter, the GPT01.GTCNTLW counter, or the GPT23.GTCNTLW counter is started (GTSTR.CSTn = 1; n = 0 to 3) or stopped (GTSTR.CSTn = 0; n = 0 to 3).
When the count direction is down-counting (GTST.TUCF flag is 0) in saw-wave mode, the GPTn.GTCNT counter is set to the value set in the GTPR register (the GTPBR register in buffer operation), the GPT01.GTCNTLW counter and the GPT23.GTCNTLW counter are set to the value set in the GTPRLW register (the GTPBRLW register in buffer operation). In other cases, the GPTn.GTCNT counter is set to 0000h and the GPT01.GTCNTLW counter and the GPT23.GTCNTLW counter are set to 00000000h when counter clearing is executed.

CCHWn[1:0] Bits (GPTn.GTCNT Hardware Source Count Clear) (n = 0 to 3)

The GPTn.GTCNT, the GPT01.GTCNTLW counter, or the GPT23.GTCNTLW counter is cleared by a hardware source. The hardware source can be selected by GTHPSR. The hardware source is accepted repeatedly when the CCHWn[1:0] bits are set to 01b, 10b, or 11b.

CCSWn Bit (GPTn.GTCNT Counter Clear) (n = 0 to 3)

When 1 is written to this bit, the GPTn.GTCNT counter, the GPT01.GTCNTLW counter, or the GPT23.GTCNTLW counter is cleared. This bit automatically returns to 0 after the writing of 1. This bit is read as 0.

22.2.5 General PWM Timer Hardware Start Source Select Register (GTHSSR)

Address(es): GPT.GTHSSR 000C 2008h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CSHSL3[3:0]				CSHSL2[3:0]				CSHSL1[3:0]				CSHSL0[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	CSHSL0[3:0]	GPT0.GTCNT Hardware Count Start Source Select*1, *2	b3 b0 0 0 0 0: CMPC0 comparator output 0 0 0 1: CMPC1 comparator output 0 0 1 0: MTU0 count start 0 0 1 1: MTU1 count start 0 1 0 0: CMPC2 comparator output 0 1 0 1: CMPC3 comparator output 0 1 1 0: MTU2 count start 0 1 1 1: MTU4 count start 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output (output compare) 1 0 1 1: GTIOC3B internal output (output compare) 1 1 0 0: GTETRG pin input 1 1 0 1: MTU7 count start 1 1 1 0: MTU9 count start Settings other than the above are prohibited when count operation is started by a hardware source.	R/W
b7 to b4	CSHSL1[3:0]	GPT1.GTCNT/GPT01.GTCNTLW Hardware Count Start Source Select*1	b7 b4 0 0 0 0: CMPC0 comparator output 0 0 0 1: CMPC1 comparator output 0 0 1 0: MTU0 count start 0 0 1 1: MTU1 count start 0 1 0 0: CMPC2 comparator output 0 1 0 1: CMPC3 comparator output 0 1 1 0: MTU2 count start 0 1 1 1: MTU4 count start 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output (output compare) 1 0 1 1: GTIOC3B internal output (output compare) 1 1 0 0: GTETRG pin input 1 1 0 1: MTU7 count start 1 1 1 0: MTU9 count start Settings other than the above are prohibited when count operation is started by a hardware source.	R/W
b11 to b8	CSHSL2[3:0]	GPT2.GTCNT Hardware Count Start Source Select*3, *4	b11 b8 0 0 0 0: CMPC0 comparator output 0 0 0 1: CMPC1 comparator output 0 0 1 0: MTU0 count start 0 0 1 1: MTU1 count start 0 1 0 0: CMPC2 comparator output 0 1 0 1: CMPC3 comparator output 0 1 1 0: MTU2 count start 0 1 1 1: MTU4 count start 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output (output compare) 1 0 1 1: GTIOC3B internal output (output compare) 1 1 0 0: GTETRG pin input 1 1 0 1: MTU7 count start 1 1 1 0: MTU9 count start Settings other than the above are prohibited when count operation is started by a hardware source.	R/W

Bit	Symbol	Bit Name	Description	R/W
b15 to b12	CSHSL3[3:0]	GPT3.GTCNT/GPT23.GTCNTLW Hardware Count Start Source Select*3	b15 b12 0 0 0 0: CMPC0 comparator output 0 0 0 1: CMPC1 comparator output 0 0 1 0: MTU0 count start 0 0 1 1: MTU1 count start 0 1 0 0: CMPC2 comparator output 0 1 0 1: CMPC3 comparator output 0 1 1 0: MTU2 count start 0 1 1 1: MTU4 count start 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 1 0 0: GTETRG pin input 1 1 0 1: MTU7 count start 1 1 1 0: MTU9 count start Settings other than the above are prohibited when count operation is started by a hardware source.	R/W

Note 1. When changing the value of the GTMDR.LWA01 bit, the bits become 0000b.
Note 2. When the GTMDR.LWA01 bit is 1, the value of the bits cannot be changed.
Note 3. When changing the value of the GTMDR.LWA23 bit, the bits become 0000b.
Note 4. When the GTMDR.LWA23 bit is 1, the value of the bits cannot be changed.

The GTHSSR register sets the hardware source to start the GPTn.GTCNT counter (n = 0 to 3), the GPT01.GTCNTLW counter, and the GPT23.GTCNTLW counter.
Use the GTHSCR register to set the edge polarity of the hardware source.
To change the source, set the GTHSCR.CSHWn[1:0] bits to 00b before changing the source.

CSHSLn[3:0] Bits (GPTn.GTCNT Hardware Count Start Source Select) (n = 0 to 3)

These bits select the hardware source to start the GPTn.GTCNT, the GPT01.GTCNTLW counter, and the GPT23.GTCNTLW counter.
When 1000b is selected as the hardware source, set the GPT3.GTIOR.GTIOA[5] bit and the GPT3.GTONCR.OAE bit to 0. When 1001b is selected as the hardware source, set the GPT3.GTIOR.GTIOB[5] bit and the GPT3.GTONCR.OBE bit to 0.
When selecting the MTU count start as the hardware source, set the GTHSCR.CSHWn[1:0] bits to 01b (rising edge).
When selecting the comparator output as the hardware source, set the GTHSCR.CSHWn[1:0] bits in accordance with the comparator output polarity. Table 22.4 lists the setting values of the GTHSCR.CSHWn[1:0] bits for the comparator settings.
If a hardware source to start count operation is not selected in the GTHSCR register, it is not necessary to change the value of these bits from their initial value.

Table 22.4 Settings of the GTHSCR.CSHWn[1:0] Bits When the Comparator Output is Selected

Count Start Source	Comparator Output Polarity	Setting of the GTHSCR.CSHWn[1:0] Bits
When the input voltage rises above the reference voltage	Not inverted	01b (rising edge)
	Inverted	10b (falling edge)
When the input voltage falls below the reference voltage	Not inverted	10b (falling edge)
	Inverted	01b (rising edge)

22.2.6 General PWM Timer Hardware Stop/Clear Source Select Register (GTHPSR)

Address(es): GPT.GTHPSR 000C 200Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CSHPL3[3:0]				CSHPL2[3:0]				CSHPL1[3:0]				CSHPL0[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	CSHPL0[3:0]	GPT0.GTCNT Hardware Count Stop/ Clear Source Select*1, *2	b3 b0 0 0 0 0: CMPC0 comparator output 0 0 0 1: CMPC1 comparator output 0 1 0 0: CMPC2 comparator output 0 1 0 1: CMPC3 comparator output 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output (output compare) 1 0 1 1: GTIOC3B internal output (output compare) 1 1 0 0: GTETRG pin input Settings other than the above are prohibited when counter is stopped or cleared by a hardware source.	R/W
b7 to b4	CSHPL1[3:0]	GPT1.GTCNT/GPT01.GTCNTLW Hardware Count Stop/Clear Source Select*1	b7 b4 0 0 0 0: CMPC0 comparator output 0 0 0 1: CMPC1 comparator output 0 1 0 0: CMPC2 comparator output 0 1 0 1: CMPC3 comparator output 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output (output compare) 1 0 1 1: GTIOC3B internal output (output compare) 1 1 0 0: GTETRG pin input Settings other than the above are prohibited when counter is stopped or cleared by a hardware source.	R/W
b11 to b8	CSHPL2[3:0]	GPT2.GTCNT Hardware Count Stop/ Clear Source Select*3, *4	b11 b8 0 0 0 0: CMPC0 comparator output 0 0 0 1: CMPC1 comparator output 0 1 0 0: CMPC2 comparator output 0 1 0 1: CMPC3 comparator output 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output (output compare) 1 0 1 1: GTIOC3B internal output (output compare) 1 1 0 0: GTETRG pin input Settings other than the above are prohibited when counter is stopped or cleared by a hardware source.	R/W
b15 to b12	CSHPL3[3:0]	GPT3.GTCNT/GPT23.GTCNTLW Hardware Count Stop/Clear Source Select*3	b15 b12 0 0 0 0: CMPC0 comparator output 0 0 0 1: CMPC1 comparator output 0 1 0 0: CMPC2 comparator output 0 1 0 1: CMPC3 comparator output 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output (output compare) 1 0 1 1: GTIOC3B internal output (output compare) 1 1 0 0: GTETRG pin input Settings other than the above are prohibited when counter is stopped or cleared by a hardware source.	R/W

Note 1. When changing the value of the GTMDR.LWA01 bit, the bits become 0000b.
Note 2. When the GTMDR.LWA01 bit is 1, the value of the bits cannot be changed.
Note 3. When changing the value of the GTMDR.LWA23 bit, the bits become 0000b.
Note 4. When the GTMDR.LWA23 bit is 1, the value of the bits cannot be changed.

The GTHPSR register sets the hardware source to stop or clear the GPTn.GTCNT counter (n = 0 to 3), the

GPT01.GTCNTLW counter, and the GPT23.GTCNTLW counter.
Use the GTHSCR register to set the edge polarity of the hardware source to stop count operation. Use the GTHCCR register to set the edge polarity of the hardware source to clear the counter.
To change the source, set the GTHSCR.CPHWn[1:0] bits and GTHCCR.CCHWn[1:0] bits to 00b before changing the source.

CSHPLn[3:0] Bits (GPTn.GTCNT Hardware Count Stop/Clear Source Select) (n = 0 to 3)

This bit selects the hardware source to stop or clear the GPTn.GTCNT counter, the GPT01.GTCNTLW counter, and the GPT23.GTCNTLW counter.
When 1000b is selected as the hardware source, set the GPT3.GTIOR.GTIOA[5] bit and the GPT3.GTONCR.OAE bit to 0. When 1001b is selected as the hardware source, set the GPT3.GTIOR.GTIOB[5] bit and the GPT3.GTONCR.OBE bit to 0.
When selecting the comparator output as the hardware source, set the GTHSCR.CPHWn[1:0] bits and GTHCCR.CCHWn[1:0] bits in accordance with the comparator output polarity. Table 22.5 lists the setting values of the GTHSCR.CPHWn[1:0] bits and GTHCCR.CCHWn[1:0] bits for the comparator settings.
If a hardware source to stop or clear the counter is not selected in the GTHSCR or GTHCCR register, it is not necessary to change the value of these bits from their initial value.

Table 22.5 Settings of the GTHSCR.CPHWn[1:0] Bits and GTHCCR.CCHWn[1:0] Bits When the Comparator Output is Selected

Count Stop/Clear Source	Comparator Output Polarity	Setting of the GTHSCR.CPHWn[1:0] Bits and GTHCCR.CCHWn[1:0] Bits
When the input voltage rises above the reference voltage	Not inverted	01b (rising edge)
	Inverted	10b (falling edge)
When the input voltage falls below the reference voltage	Not inverted	10b (falling edge)
	Inverted	01b (rising edge)

22.2.7 General PWM Timer Write-Protection Register (GTWP)

Address(es): GPT.GTWP 000C 200Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	WP3	WP2	WP1	WP0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	WP0	GPT0 Register Write Disable*1, *2	0: Write to the register is enabled 1: Write to the register is disabled	R/W
b1	WP1	GPT1/GPT01 Register Write Disable*3	0: Write to the register is enabled 1: Write to the register is disabled	R/W
b2	WP2	GPT2 Register Write Disable*4, *5	0: Write to the register is enabled 1: Write to the register is disabled	R/W
b3	WP3	GPT3/GPT23 Register Write Disable*6	0: Write to the register is enabled 1: Write to the register is disabled	R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Changing the GTMDR.LWA01 bit to 1 sets the bit to 1, and changing the LWA01 bit from 1 to 0 sets the bit to 0.
Note 2. When the GTMDR.LWA01 bit is 1, the value of the bit cannot be changed.
Note 3. When changing the value of the GTMDR.LWA01 bit, the bit becomes 0.
Note 4. Changing the GTMDR.LWA23 bit to 1 sets the bit to 1, and changing the LWA23 bit from 1 to 0 sets the bit to 0.
Note 5. When the GTMDR.LWA23 bit is 1, the value of the bit cannot be changed.
Note 6. When changing the value of the GTMDR.LWA23 bit, the bit becomes 0.

GTWP enables or disables writing to registers to prevent accidental modification.
For registers that are write enabled or disabled depending on the setting of the GPWP register, see section 22.6.1, Write-Protection for Registers.

22.2.8 General PWM Timer Sync Register (GTSYNC)

Address(es): GPT.GTSYNC 000C 200Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	SYNC3[1:0]		—	—	SYNC2[1:0]		—	—	SYNC1[1:0]		—	—	SYNC0[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	SYNC0[1:0]	GPT0.GTCNT Counter Synchronous Clear Source Select*1, *2	b1 b0 0 0: Synchronous clear is not performed. 0 1: GPT0.GTCNT is synchronously cleared by a GPT1 clearing source. 1 0: GPT0.GTCNT is synchronously cleared by a GPT2 clearing source.*3 1 1: GPT0.GTCNT is synchronously cleared by a GPT3/GPT23 clearing source.	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5, b4	SYNC1[1:0]	GPT1.GTCNT/ GPT01.GTCNTLW Counter Synchronous Clear Source Select*1	b5 b4 0 0: GPT1.GTCNT is synchronously cleared by a GPT0 clearing source.*4 0 1: Synchronous clear is not performed. 1 0: GPT1.GTCNT/GPT01.GTCNTLW is synchronously cleared by a GPT2 clearing source.*3 1 1: GPT1.GTCNT/GPT01.GTCNTLW is synchronously cleared by a GPT3/GPT23 clearing source.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b9, b8	SYNC2[1:0]	GPT2.GTCNT Counter Synchronous Clear Source Select*5, *6	b9 b8 0 0: GPT2.GTCNT is synchronously cleared by a GPT0 clearing source.*4 0 1: GPT2.GTCNT is synchronously cleared by a GPT1/GPT01 clearing source. 1 0: Synchronous clear is not performed. 1 1: GPT2.GTCNT is synchronously cleared by a GPT3 clearing source.	R/W
b11, b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13, b12	SYNC3[1:0]	GPT3.GTCNT/ GPT23.GTCNTLW Counter Synchronous Clear Source Select*5	b13 b12 0 0: GPT3.GTCNT/GPT23.GTCNTLW is synchronously cleared by a GPT0 clearing source.*4 0 1: GPT3.GTCNT/GPT23.GTCNTLW is synchronously cleared by a GPT1/GPT01 clearing source. 1 0: GPT3.GTCNT is synchronously cleared by a GPT2 clearing source.*3 1 1: Synchronous clear is not performed	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. When changing the value of the GTMDR.LWA01 bit, the bits become 00b.
Note 2. When the GTMDR.LWA01 bit is 1, the value of the bits cannot be changed.
Note 3. When the GTMDR.LWA23 bit is 1, synchronous clearing is not performed.
Note 4. When the GTMDR.LWA01 bit is 1, synchronous clearing is not performed.
Note 5. When changing the value of the GTMDR.LWA23 bit, the bits become 00b.
Note 6. When the GTMDR.LWA23 bit is 1, the value of the bits cannot be changed.

GTSYNC sets the clearing source of the GPTn.GTCNT counter, the GPT01.GTCNTLW counter, and the GPT23.GTCNTLW counter for synchronous clearing/synchronous operation. This register should be modified while the GPTn.GTCNT counter, the GPT01.GTCNTLW counter, and the GPT23.GTCNTLW counter are stopped (n = 0 to 3).

SYNCn[1:0] Bits (GPTn.GTCNT Counter Synchronous Clear Source Select) (n = 0 to 3)

These bits select which channel's counter clearing source is used to clear the GPTn.GTCNT counter, the

GPT01.GTCNTLW counter, and the GPT23.GTCNTLW counter. When setting the SYNCn[1:0] bits, first set the GPTn.GTCR.CCLR[1:0] bits to 11b (cleared by counter clearing in another channel performing synchronous clearing/ synchronous operation).

22.2.9 General PWM Timer External Trigger Input Interrupt Register (GTETINT)

Address(es): GPT.GTETINT 000C 2010h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	GTETRGEN	GTENFCS[1:0]		—	—	—	—	—	—	—	—	—	—	—	ETINEN	ETIPEN
Value after reset:	0	0	0	0	0	0	x	x	0	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b0	ETIPEN	External Trigger Rising Input Interrupt Request Enable	0: Interrupt request is disabled 1: Interrupt request is enabled	R/W
b1	ETINEN	External Trigger Falling Input Interrupt Request Enable	0: Interrupt request is disabled 1: Interrupt request is enabled	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b9, b8	—	Reserved	The read value is undefined. The write value should be 1.	R/W
b12 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b14, b13	GTENFCS[1:0]	GTETRG Noise Filter Sampling Clock Select	b14 b13 0 0: PCLKA/1 0 1: PCLKA/2 1 0: PCLKA/4 1 1: PCLKA/32	R/W
b15	GTETRGEN	GTETRG Noise Filter Enable	0: The noise filter for the GTETRG pin is disabled. 1: The noise filter for the GTETRG pin is enabled.	R/W

GTETINT enables or disables interrupts through the external trigger input pin (GTETRG).

ETIPEN Bit (External Trigger Rising Input Interrupt Request Enable)

This bit enables or disables an interrupt request generated at the rising edge of an external trigger input.

ETINEN Bit (External Trigger Falling Input Interrupt Request Enable)

This bit enables or disables an interrupt request generated at the falling edge of an external trigger input.

GTENFCS[1:0] Bits (GTETRG Noise Filter Sampling Clock Select)

These bits set the sampling interval for the noise filters. After setting these bits, wait for two selected sampling periods, set the GTHSCR, GTHCCR, and GTHSSR registers to enable the counter operation by a hardware source of GTETRG.

GTETRGEN Bit (GTETRG Noise Filter Enable)

This bit disables or enables the noise filter for input from the GTETRG pin. Since changing the value of the bit may lead to the internal generation of an unexpected edge, set the GTHSCR, GTHCCR, and GTHSSR registers to disable the counter operation by a hardware source of GTETRG before changing the value.

22.2.10 General PWM Timer Buffer Operation Disable Register (GTBDR)

Address(es): GPT.GTBDR 000C 2014h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BD33	BD32	BD31	BD30	BD23	BD22	BD21	BD20	BD13	BD12	BD11	BD10	BD03	BD02	BD01	BD00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	BD00	GPT0.GTCCR Buffer Operation Disable*1, *2	0: Buffer operation is enabled 1: Buffer operation is disabled	R/W
b1	BD01	GPT0.GTPR Buffer Operation Disable*1, *2	0: Buffer operation is enabled 1: Buffer operation is disabled	R/W
b2	BD02	GPT0.GTADTR Buffer Operation Disable*1, *2	0: Buffer operation is enabled 1: Buffer operation is disabled	R/W
b3	BD03	GPT0.GTDV Buffer Operation Disable*1, *2	0: Buffer operation is enabled 1: Buffer operation is disabled	R/W
b4	BD10	GPT1.GTCCR/GPT01.GTCCRLW Buffer Operation Disable*1	0: Buffer operation is enabled 1: Buffer operation is disabled	R/W
b5	BD11	GPT1.GTPR/GPT01.GTPRLW Buffer Operation Disable*1	0: Buffer operation is enabled 1: Buffer operation is disabled	R/W
b6	BD12	GPT1.GTADTR/GPT01.GTADTRLW Buffer Operation Disable*1	0: Buffer operation is enabled 1: Buffer operation is disabled	R/W
b7	BD13	GPT1.GTDV/GPT01.GTDVLW Buffer Operation Disable*1	0: Buffer operation is enabled 1: Buffer operation is disabled	R/W
b8	BD20	GPT2.GTCCR Buffer Operation Disable*3, *4	0: Buffer operation is enabled 1: Buffer operation is disabled	R/W
b9	BD21	GPT2.GTPR Buffer Operation Disable*3, *4	0: Buffer operation is enabled 1: Buffer operation is disabled	R/W
b10	BD22	GPT2.GTADTR Buffer Operation Disable*3, *4	0: Buffer operation is enabled 1: Buffer operation is disabled	R/W
b11	BD23	GPT2.GTDV Buffer Operation Disable*3, *4	0: Buffer operation is enabled 1: Buffer operation is disabled	R/W
b12	BD30	GPT3.GTCCR/GPT23.GTCCRLW Buffer Operation Disable*3	0: Buffer operation is enabled 1: Buffer operation is disabled	R/W
b13	BD31	GPT3.GTPR/GPT23.GTPRLW Buffer Operation Disable*3	0: Buffer operation is enabled 1: Buffer operation is disabled	R/W
b14	BD32	GPT3.GTADTR/GPT23.GTADTRLW Buffer Operation Disable*3	0: Buffer operation is enabled 1: Buffer operation is disabled	R/W
b15	BD33	GPT3.GTDV/GPT23.GTDVLW Buffer Operation Disable*3	0: Buffer operation is enabled 1: Buffer operation is disabled	R/W

Note 1. When changing the value of the GTMDR.LWA01 bit, the bit becomes 0.
Note 2. When the GTMDR.LWA01 bit is 1, the value of the bit cannot be changed.
Note 3. When changing the value of the GTMDR.LWA23 bit, the bit becomes 0.
Note 4. When the GTMDR.LWA23 bit is 1, the value of the bit cannot be changed.

The GTBDR register collectively enables or disables buffer operation of each channel. Even though a bit in the GTBDR register is set to 0 (buffer operation is enabled), buffer operation is not performed unless buffer operation is enabled by the GTBER register.

BDn0 Bit (GPTn.GTCCR Buffer Operation Disable) (n = 0 to 3)

This bit disables buffer operation using the GTCCRA(LW), GTCCRC(LW), and GTCCRD(LW) registers of GPTn together and buffer operation using the GTCCRB(LW), GTCCRE(LW), and GTCCRF(LW) registers of GPTn together.

BDn1 Bit (GPTn.GTPR Buffer Operation Disable) (n = 0 to 3)

This bit disables buffer operation using the GTPR(LW), GTPBR(LW), and GTPDBR(LW) registers of GPTn together.

BDn2 Bit (GPTn.GTADTR Buffer Operation Disable) (n = 0 to 3)

This bit disables buffer operation using the GTADTRA(LW), GTADTBRA(LW), and GTADTDBRA(LW) registers of GPTn together and buffer operation using the GTADTRB(LW), GTADTBRB(LW), and GTADTDBRB(LW) registers of GPTn together.

BDn3 Bit (GPTn.GTDV Buffer Operation Disable) (n = 0 to 3)

This bit disables buffer operation using the GTDVU(LW) and GTDBU(LW) registers of GPTn together and buffer operation using the GTDVD(LW) and GTDBD(LW) registers of GPTn together.

22.2.11 General PWM Timer Start Write-Protection Register (GTSWP)

Address(es): GPT.GTSWP 000C 2018h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	SWP3	SWP2	SWP1	SWP0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SWP0	GTSTR.CST0 Bit Write Disable*1, *2	0: Writing to the register bit is enabled 1: Writing to the register bit is disabled	R/W
b1	SWP1	GTSTR.CST1 Bit Write Disable*3	0: Writing to the register bit is enabled 1: Writing to the register bit is disabled	R/W
b2	SWP2	GTSTR.CST2 Bit Write Disable*4, *5	0: Writing to the register bit is enabled 1: Writing to the register bit is disabled	R/W
b3	SWP3	GTSTR.CST3 Bit Write Disable*6	0: Writing to the register bit is enabled 1: Writing to the register bit is disabled	R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Changing the GTMDR.LWA01 bit to 1 sets the bit to 1, and changing the LWA01 bit from 1 to 0 sets the bit to 0.
Note 2. When the GTMDR.LWA01 bit is 1, the value of the bit cannot be changed.
Note 3. When changing the value of the GTMDR.LWA01 bit, the bit becomes 0.
Note 4. Changing the GTMDR.LWA23 bit to 1 sets the bit to 1, and changing the LWA23 bit from 1 to 0 sets the bit to 0.
Note 5. When the GTMDR.LWA23 bit is 1, the value of the bit cannot be changed.
Note 6. When changing the value of the GTMDR.LWA23 bit, the bit becomes 0.

The GTSWP register enables or disables writing to the GTSTR register to prevent accidental modification.

SWPn Bit (GTSTR.CSTn Bit Write Disable) (n = 0 to 3)

This bit enables or disables writing to the GTSTR.CSTn bit.
When this bit is set to disable writing, writing to the GTSTR.CSTn bit is ignored.
However, if the GTHSCR register is set to start or stop count operation by a hardware source, the status of count operation (started or stopped by a hardware source) is written to the GTSTR.CSTn bit even if the SWPn bit is set to disable writing to GTSTR.CSTn bit.

22.2.12 General PWM Timer Clearing Write-Protection Register (GTCWP)

Address(es): GPT.GTCWP 000C 201Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	CWP3	CWP2	CWP1	CWP0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CWP0	GTHCCR.CCSW0 Bit Write Disabling*1, *2	0: Writing to the CCSW0 bit is enabled. 1: Writing to the CCSW0 bit is disabled.	R/W
b1	CWP1	GTHCCR.CCSW1 Bit Write Disabling*3	0: Writing to the CCSW1 bit is enabled. 1: Writing to the CCSW1 bit is disabled.	R/W
b2	CWP2	GTHCCR.CCSW2 Bit Write Disabling*4, *5	0: Writing to the CCSW2 bit is enabled. 1: Writing to the CCSW2 bit is disabled.	R/W
b3	CWP3	GTHCCR.CCSW3 Bit Write Disabling*6	0: Writing to the CCSW3 bit is enabled. 1: Writing to the CCSW3 bit is disabled.	R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Changing the GTMDR.LWA01 bit to 1 sets the bit to 1, and changing the LWA01 bit from 1 to 0 sets the bit to 0.
Note 2. When the GTMDR.LWA01 bit is 1, the value of the bit cannot be changed.
Note 3. When changing the value of the GTMDR.LWA01 bit, the bit becomes 0.
Note 4. Changing the GTMDR.LWA23 bit to 1 sets the bit to 1, and changing the LWA23 bit from 1 to 0 sets the bit to 0.
Note 5. When the GTMDR.LWA23 bit is 1, the value of the bit cannot be changed.
Note 6. When changing the value of the GTMDR.LWA23 bit, the bit becomes 0.

This register enables or disables writing to the GTHCCR.CCSWn bit to prevent accidental modification.

CWPn Bit (GTHCCR.CCSWn Bit Write Disabling) (n = 0 to 3)

This bit enables or disables writing to the GTHCCR.CCSWn bit.
When the setting of a bit for writing is disabled, writing to the corresponding GTHCCR.CCSWn bit is ignored.

22.2.13 General PWM Timer Common Register Write-Protection Register (GTCMNWP)

Address(es): GPT.GTCMNWP 000C 2020h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CMNWP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CMNWP	Common Register Write Disabling	0: Writing to the common registers is enabled. 1: Writing to the common registers is disabled.	R/W
b15 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

This register enables or disables writing to the common registers to prevent accidental modification of their values.

CMNWP Bit (Common Register Write Disabling)

This bit enables or disables writing to the NFCR register, the GTHSCR register, the GTHCCR.CCHWn[1:0] bits (n = 0 to 3), the GTHSSR register, the GTHPSR register, the GTSYNC register, the GTETINT register, the GTBDR register, the GTMDR register, the GTECNFCR register, and the GTADSMR register.

When the setting of the bit for writing is disabled, writing to the registers is ignored.

This control is not applied to the GTSTR register, the GTHCCR.CCSWn bit (n = 0 to 3), the GTWP register, the GTSWP register, and the GTCWP register.

22.2.14 General PWM Timer Mode Register (GTMDR)

Address(es): GPT.GTMDR 000C 2024h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LWA23	LWA01
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	LWA01	GPT01 Cascaded Connection Enabling	0: Cascaded connection between GPT0 and GPT1 is disabled. 1: Cascaded connection between GPT0 and GPT1 is enabled.	R/W
b1	LWA23	GPT23 Cascaded Connection Enabling	0: Cascaded connection between GPT2 and GPT3 is disabled. 1: Cascaded connection between GPT2 and GPT3 is enabled.	R/W
b15 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

This register enables or disables cascaded connection of the counter.
Set the register while the counter is stopped before setting other registers.
Changing the setting of the LWA01 or LWA23 bit (from disabling to enabling or from enabling to disabling) resets some registers for the target channels and control bits of the target channels in registers common to the given pair of channels. A reset does not apply when the same value is overwritten.

LWA01 Bit (GPT01 Cascaded Connection Enabling)

This bit enables or disable cascaded connection of the counter of GPT0 and GPT1.

[Operation when the LWA01 bit is enabled]
With GPT0 and GPT1 cascade-connected to operate as the timer channel GPT01, the counter, comparison value to trigger capture, period setting, setting for the timing of requests to start A/D conversion, and dead-time value all operate as 32-bit units.
The channel GPT01 is controlled by the GPT1 registers (GPT1.GTIOR, GPT1.GTINTAD, GPT1.GTCR, GPT1.GTBER, GPT1.GTUDC, GPT1.GTITC, GPT1.GTST, GPT1.GTONCR, GPT1.GTDTCR, GPT1.GTSOS, and GPT1.GTSOTR). In this case, writing to the registers corresponding to GPT0 is ignored and the value after a reset is read when they are read.
The GPT01 registers (GTCNTLW, GTCCRALW, GTCCRBLW, GTCCRCLW, GTCCRDLW, GTCCRELW, GTCCRFLW, GTPRLW, GTPBRLW, GTPDBRLW, GTADTRALW, GTADTBRALW, GTADTDBRALW, GTADTRBLW, GTADTBRBLW, GTADTDBRBLW, GTDVULW, GTDVDLW, GTDBULW, and GTDVDLW) are used the registers for the counter, comparison value to trigger capture, period setting, setting for the timing of requests to start A/D conversion, and dead-time value. Writing to the GPT1 registers (GTCNT, GTCCRA, GTCCRB, GTCCRC, GTCCRD, GTCCRE, GTCCRF, GTPR, GTPBR, GTPDBR, GTADTRA, GTADTBRA, GTADTDBRA, GTADTRB, GTADTBRB, GTADTDBRB, GTDVU, GTDVD, GTDBU, and GTDVD) is ignored. The value after a reset is read when they are read.
The control bit of GPT1 is used for GPT01 to control by the common registers. Writing to the control bit for GPT0 is ignored. When it is read, the value after a reset is read (however, the GTWP.WP0, GTSWP.SWP0, GTCWP.CWP0 bits are read as 1).

[Operation when the LWA01 bit is disabled]
The values and settings of the registers of GPT0 and GPT1 and of the control bits of registers common to GPT0 and GPT1 are all valid. Registers in the GPT01 become all invalid. Writing to the registers is ignored. The value after a reset is read when they are read.

LWA23 Bit (GPT23 Cascaded Connection Enabling)

This bit enables or disable cascaded connection of the GPT2 and GPT3 counters. The operation is the same as that of the LWA01 bit.

22.2.15 General PWM Timer External Clock Noise Filter Control Register (GTECNFCR)

Address(es): GPT.GTECNFCR 000C 2028h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	NFCSECD[1:0]		NFCSECC[1:0]		NFCSECB[1:0]		NFCSECA[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	INVECD	INVECC	INVECB	INVECA	—	—	—	—	NFENECD	NFENECC	NFENECB	NFENECA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	NFENECA	GTECLKA Noise Filter Enabling	0: The noise filter for the GTECLKA pin is stopped. 1: The noise filter for the GTECLKA pin is enabled.	R/W
b1	NFENECB	GTECLKB Noise Filter Enabling	0: The noise filter for the GTECLKB pin is stopped. 1: The noise filter for the GTECLKB pin is enabled.	R/W
b2	NFENECC	GTECLKC Noise Filter Enabling	0: The noise filter for the GTECLKC pin is stopped. 1: The noise filter for the GTECLKC pin is enabled.	R/W
b3	NFENECD	GTECLKD Noise Filter Enabling	0: The noise filter for the GTECLKD pin is stopped. 1: The noise filter for the GTECLKD pin is enabled.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	INVECA	GTECLKA Polarity Inversion	0: The polarity of the GTECLKA pin is not changed. 1: The polarity of the GTECLKA pin is inverted.	R/W
b9	INVECB	GTECLKB Polarity Inversion	0: The polarity of the GTECLKB pin is not changed. 1: The polarity of the GTECLKB pin is inverted.	R/W
b10	INVECC	GTECLKC Polarity Inversion	0: The polarity of the GTECLKC pin is not changed. 1: The polarity of the GTECLKC pin is inverted.	R/W
b11	INVECD	GTECLKD Polarity Inversion	0: The polarity of the GTECLKD pin is not changed. 1: The polarity of the GTECLKD pin is inverted.	R/W
b15 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b17 to b16	NFCSECA[1:0]	GTECLKA Noise Filter Sampling Clock Selection	b17 b16 0 0: PCLKA/1 0 1: PCLKA/2 1 0: PCLKA/4 1 1: PCLKA/32	R/W
b19 to b18	NFCSECB[1:0]	GTECLKB Noise Filter Sampling Clock Selection	b19 b18 0 0: PCLKA/1 0 1: PCLKA/2 1 0: PCLKA/4 1 1: PCLKA/32	R/W
b21 to b20	NFCSECC[1:0]	GTECLKC Noise Filter Sampling Clock Selection	b21 b20 0 0: PCLKA/1 0 1: PCLKA/2 1 0: PCLKA/4 1 1: PCLKA/32	R/W
b23 to b22	NFCSECD[1:0]	GTECLKD Noise Filter Sampling Clock Selection	b23 b22 0 0: PCLKA/1 0 1: PCLKA/2 1 0: PCLKA/4 1 1: PCLKA/32	R/W
b31 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

This register controls the noise filters on the inputs for the externally input clock signals.

NFENECx Bit (GTECLKx Noise Filter Enabling) (x = A to D)

This bit enables or disables the noise filter of the GTECLKx pin.
Writing a new value to the bit may lead to an unintended edge on the internal signal, so only do so while the setting of the GTCR.TPCS[3:0] bits is other than for an external clock.

INVECx Bit (GTECLKx Polarity Inversion) (x = A to D)

This bit inverts the polarity of the input of the GTECLKx pin.
When the external clock is selected by the GTCR.TPCS[3:0] bits, the count clock has a rising edge after the signal is inverted.

NFCSECx[1:0] Bit (GTECLKx Noise Filter Sampling Clock Selection) (x = A to D)

These bits specify the sampling period of the noise filter of the GTECLKx pin.
Wait for 2 cycles of the specified sampling period after setting of the bit, and then set an external clock in the GTCR.TPCS[3:0] bits.

22.2.16 General PWM Timer A/D Conversion Start Request Signal Monitor Register (GTADSMR)

Address(es): GPT.GTADSMR 000C 202Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	ADSMEN1	—	—	—	—	ADSMS1[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	ADSMEN0	—	—	—	—	ADSMS0[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	ADSMS0[3:0]	A/D Conversion Start Request Signal Monitor 0 Selection	b3 b0 0 0 0 0: A/D conversion start request signal generated by the GPT0.GTADTRA register during up-counting*1 0 0 0 1: A/D conversion start request signal generated by the GPT0.GTADTRA register during down-counting*1 0 0 1 0: A/D conversion start request signal generated by the GPT0.GTADTRB register during up-counting*1 0 0 1 1: A/D conversion start request signal generated by the GPT0.GTADTRB register during down-counting*1 0 1 0 0: A/D conversion start request signal generated by the GPT1.GTADTRA/GPT01.GTADTRALW register during up-counting 0 1 0 1: A/D conversion start request signal generated by the GPT1.GTADTRA/GPT01.GTADTRALW register during down-counting 0 1 1 0: A/D conversion start request signal generated by the GPT1.GTADTRB/GPT01.GTADTRBLW register during up-counting 0 1 1 1: A/D conversion start request signal generated by the GPT1.GTADTRB/GPT01.GTADTRBLW register during down-counting 1 0 0 0: A/D conversion start request signal generated by the GPT2.GTADTRA register during up-counting*2 1 0 0 1: A/D conversion start request signal generated by the GPT2.GTADTRA register during down-counting*2 1 0 1 0: A/D conversion start request signal generated by the GPT2.GTADTRB register during up-counting*2 1 0 1 1: A/D conversion start request signal generated by the GPT2.GTADTRB register during down-counting*2 1 1 0 0: A/D conversion start request signal generated by the GPT3.GTADTRA/GPT23.GTADTRALW register during up-counting 1 1 0 1: A/D conversion start request signal generated by the GPT3.GTADTRA/GPT23.GTADTRALW register during down-counting 1 1 1 0: A/D conversion start request signal generated by the GPT3.GTADTRB/GPT23.GTADTRBLW register during up-counting 1 1 1 1: A/D conversion start request signal generated by the GPT3.GTADTRB/GPT23.GTADTRBLW register during down-counting	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	ADSMEN0	A/D Conversion Start Request Signal Monitor 0 Output Enabling	0: Output of A/D conversion start request signal monitor 0 is disabled. 1: Output of A/D conversion start request signal monitor 0 is enabled.	R/W
b15 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Bit Name	Description	R/W
b19 to b16	ADSMS1[3:0]	A/D Conversion Start Request Signal Monitor 1 Selection	b19 b16 0 0 0 0: A/D conversion start request signal generated by the GPT0.GTADTRA register during up-counting*1 0 0 0 1: A/D conversion start request signal generated by the GPT0.GTADTRA register during down-counting*1 0 0 1 0: A/D conversion start request signal generated by the GPT0.GTADTRB register during up-counting*1 0 0 1 1: A/D conversion start request signal generated by the GPT0.GTADTRB register during down-counting*1 0 1 0 0: A/D conversion start request signal generated by the GPT1.GTADTRA/GPT01.GTADTRALW register during up-counting 0 1 0 1: A/D conversion start request signal generated by the GPT1.GTADTRA/GPT01.GTADTRALW register during down-counting 0 1 1 0: A/D conversion start request signal generated by the GPT1.GTADTRB/GPT01.GTADTRBLW register during up-counting 0 1 1 1: A/D conversion start request signal generated by the GPT1.GTADTRB/GPT01.GTADTRBLW register during down-counting 1 0 0 0: A/D conversion start request signal generated by the GPT2.GTADTRA register during up-counting*2 1 0 0 1: A/D conversion start request signal generated by the GPT2.GTADTRA register during down-counting*2 1 0 1 0: A/D conversion start request signal generated by the GPT2.GTADTRB register during up-counting*2 1 0 1 1: A/D conversion start request signal generated by the GPT2.GTADTRB register during down-counting*2 1 1 0 0: A/D conversion start request signal generated by the GPT3.GTADTRA/GPT23.GTADTRALW register during up-counting 1 1 0 1: A/D conversion start request signal generated by the GPT3.GTADTRA/GPT23.GTADTRALW register during down-counting 1 1 1 0: A/D conversion start request signal generated by the GPT3.GTADTRB/GPT23.GTADTRBLW register during up-counting 1 1 1 1: A/D conversion start request signal generated by the GPT3.GTADTRB/GPT23.GTADTRBLW register during down-counting	R/W
b23 to b20	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b24	ADSMEN1	A/D Conversion Start Request Signal Monitor 1 Output Enabling	0: Output of A/D conversion start request signal monitor 1 is disabled. 1: Output of A/D conversion start request signal monitor 1 is enabled.	R/W
b31 to b25	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Changing the value of the GTMDR.LWA01 bit or GTMDR.LWA23 bit sets this register to 0000 0000h.
Note 1. When the GTMDR.LWA01 bit is 1, this setting is invalid.
Note 2. When the GTMDR.LWA23 bit is 1, this setting is invalid.

This register is used to control monitors for the A/D conversion start request signal that is synchronized with a frame.

ADSMSk[3:0] Bit (A/D Conversion Start Request Signal Monitor k Selection) (k = 0, 1)

These bits are used to select A/D conversion start request signal synchronized with a frame which is monitored by the GTADSMk pin.

ADSMENk Bit (A/D Conversion Start Request Signal Monitor k Output Enabling) (k = 0, 1)

This bit enables or disables the monitor output to the GTADSMk pin.
When the output is disabled, the GTADSMk pin goes to the low level.

When the bit is 1, the signal on the GTADSMk pin goes to the high level on assertion of the signal to request to the start of A/D conversion selected by the ADSMSk[3:0] bits and returns to the low level at the end of the current cycle of the timer for the channel that generated the given signal to request the start of A/D conversion. When the counter stops, the value when the counter stopped is retained for output. Set the ADSMENk bit to 0 to output the low level.
When a signal to request the start of A/D conversion is generated at the end of a timer period, the generation of this signal has priority in terms of monitoring output and the output remains at the high level till the end of the next cycle.

22.2.17 General PWM Timer I/O Control Register (GTIOR)

Address(es): GPT0.GTIOR 000C 2100h, GPT1.GTIOR 000C 2180h, GPT2.GTIOR 000C 2200h, GPT3.GTIOR 000C 2280h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OBHLD	OBDFLT	GTIOB[5:0]						OAHLD	OADFLT	GTIOA[5:0]					
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	GTIOA[5:0]	GTIOCnA Pin Function Select	See Table 22.6.	R/W
b6	OADFLT	GTIOCnA Pin Output Value Setting at the Count Stop	0: The GTIOCnA pin outputs low when counting is stopped. 1: The GTIOCnA pin outputs high when counting is stopped.	R/W
b7	OAHLD	GTIOCnA Pin Output Setting at the Start/Stop Count	0: The GTIOCnA pin output level at start/stop of counting depends on the register setting. 1: The GTIOCnA pin output level is retained at start/stop of counting.	R/W
b13 to b8	GTIOB[5:0]	GTIOCnB Pin Function Select	See Table 22.6.	R/W
b14	OBDFLT	GTIOCnB Pin Output Value Setting at the Count Stop	0: The GTIOCnB pin outputs low when counting is stopped. 1: The GTIOCnB pin outputs high when counting is stopped.	R/W
b15	OBHLD	GTIOCnB Pin Output Setting at the Start/Stop Count	0: The GTIOCnB pin output level at start/stop of counting depends on the register setting. 1: The GTIOCnB pin output level is retained at start/stop of counting.	R/W

n = 0 to 3
Note: When changing the value of the GTMDR.LWA01 bit, the GPT0.GTIOR register and GPT1.GTIOR register become 0000h.
Note: When the GTMDR.LWA01 bit is 1, the value of the GPT0.GTIOR register cannot be changed.
Note: When changing the value of the GTMDR.LWA23 bit, the GPT2.GTIOR register and GPT3.GTIOR register become 0000h.
Note: When the GTMDR.LWA23 bit is 1, the value of the GPT2.GTIOR register cannot be changed.

GPTn.GTIOR sets the functions of the GTIOCnA and GTIOCnB pins (n = 0 to 3).
Each channel has one GTIOCnA pin and one GTIOCnB pin. Values written to the GTIOR register of the relevant channel in which write access is disabled by the GTWP.WPn bit are ignored.

GTIOA[5:0] Bits (GTIOCnA Pin Function Select)

These bits select the GTIOCnA pin function. For details, see Table 22.6.

OADFLT Bit (GTIOCnA Pin Output Value Setting at the Count Stop)

This bit sets whether the GTIOCnA pin outputs high or low when counting is stopped.

OAHLD Bit (GTIOCnA Pin Output Setting at the Start/Stop Count)

This bit specifies whether the GTIOCnA pin output level is retained or the level depends on the register setting when counting is started or stopped.
[When the OAHLD bit is set to 0]

- The value specified by the GTIOA[4] bit is output when counting starts.
- The value specified by the OADFLT bit is output when counting stops.
- If the OADFLT bit is modified while counting is stopped, it is immediately reflected in the output.

[When the OAHLD bit is set to 1]

- The output is retained when counting starts or stops.

GTIOB[5:0] Bits (GTIOCnB Pin Function Select)

These bits select the GTIOCnB pin function. For details, see Table 22.6.

OBDFLT Bit (GTIOCnB Pin Output Value Setting at the Count Stop)

This bit sets whether the GTIOCnB pin outputs high or low when counting is stopped.

OBHLD Bit (GTIOCnB Pin Output Setting at the Start/Stop Count)

This bit specifies whether the GTIOCnB pin output level is retained or the level depends on the register setting when counting is started or stopped.

[When the OBHLD bit is set to 0]

- The value specified by the GTIOB[4] bit is output when counting starts.
- The value specified by the OBDFLT bit is output when counting stops.
- If the OBDFLT bit is modified while counting is stopped, it is immediately reflected in the output.

[When the OBHLD bit is set to 1]

- The output is retained when counting starts or stops.

Table 22.6 Settings of GTIOA[5:0] Bits (GTIOB[5:0] Bits) (1/2)

GTIOA[5:0]/GTIOB[5:0] Bits						Function			
b5	b4	b3	b2	b1	b0	b5	b4	b3, b2	b1, b0
0	0	0	0	0	0	Compare match	Initial output is Low.	Output retained at the end of a cycle	Output retained at GPTn.GTCCRA(LW)/ GTCCRB(LW) compare match
0	0	0	0	0	1				Low output at GPTn.GTCCRA(LW)/ GTCCRB(LW) compare match
0	0	0	0	1	0				High output at GPTn.GTCCRA(LW)/ GTCCRB(LW) compare match
0	0	0	0	1	1				Output toggled at GPTn.GTCCRA(LW)/ GTCCRB(LW) compare match
0	0	0	1	0	0			Low output at the end of a cycle	Output retained at GPTn.GTCCRA(LW)/ GTCCRB(LW) compare match
0	0	0	1	0	1				Low output at GPTn.GTCCRA(LW)/ GTCCRB(LW) compare match
0	0	0	1	1	0				High output at GPTn.GTCCRA(LW)/ GTCCRB(LW) compare match
0	0	0	1	1	1				Output toggled at GPTn.GTCCRA(LW)/ GTCCRB(LW) compare match
0	0	1	0	0	0			High output at the end of a cycle	Output retained at GPTn.GTCCRA(LW)/ GTCCRB(LW) compare match
0	0	1	0	0	1				Low output at GPTn.GTCCRA(LW)/ GTCCRB(LW) compare match
0	0	1	0	1	0				High output at GPTn.GTCCRA(LW)/ GTCCRB(LW) compare match
0	0	1	0	1	1				Output toggled at GPTn.GTCCRA(LW)/ GTCCRB(LW) compare match
0	0	1	1	0	0			Output toggled at the end of a cycle	Output retained at GPTn.GTCCRA(LW)/ GTCCRB(LW) compare match
0	0	1	1	0	1				Low output at GPTn.GTCCRA(LW)/ GTCCRB(LW) compare match
0	0	1	1	1	0				High output at GPTn.GTCCRA(LW)/ GTCCRB(LW) compare match
0	0	1	1	1	1				Output toggled at GPTn.GTCCRA(LW)/ GTCCRB(LW) compare match

Table 22.6 Settings of GTIOA[5:0] Bits (GTIOB[5:0] Bits) (2/2)

GTIOA[5:0]/GTIOB[5:0] Bits						Function			
b5	b4	b3	b2	b1	b0	b5	b4	b3, b2	b1, b0
0	1	0	0	0	0	Compare match	Initial output is High.	Output retained at the end of a cycle	Output retained at GPTn.GTCCRA(LW)/ GTCCRB(LW) compare match
0	1	0	0	0	1				Low output at GPTn.GTCCRA(LW)/ GTCCRB(LW) compare match
0	1	0	0	1	0				High output at GPTn.GTCCRA(LW)/ GTCCRB(LW) compare match
0	1	0	0	1	1				Output toggled at GPTn.GTCCRA(LW)/ GTCCRB(LW) compare match
0	1	0	1	0	0			Low output at the end of a cycle	Output retained at GTPn.GTCCRA(LW)/ GTCCRB(LW) compare match
0	1	0	1	0	1				Low output at GTPn.GTCCRA(LW)/ GTCCRB(LW) compare match
0	1	0	1	1	0				High output at GPTn.GTCCRA(LW)/ GTCCRB(LW) compare match
0	1	0	1	1	1				Output toggled at GPTn.GTCCRA(LW)/ GTCCRB(LW) compare match
0	1	1	0	0	0			High output at the end of a cycle	Output retained at GTPn.GTCCRA(LW)/ GTCCRB(LW) compare match
0	1	1	0	0	1				Low output at GPTn.GTCCRA(LW)/ GTCCRB(LW) compare match
0	1	1	0	1	0				High output at GPTn.GTCCRA(LW)/ GTCCRB(LW) compare match
0	1	1	0	1	1				Output toggled at GPTn.GTCCRA(LW)/ GTCCRB(LW) compare match
0	1	1	1	0	0			Output toggled at the end of a cycle	Output retained at GTPn.GTCCRA(LW)/ GTCCRB(LW) compare match
0	1	1	1	0	1				Low output at GPTn.GTCCRA(LW)/ GTCCRB(LW) compare match
0	1	1	1	1	0				High output at GPTn.GTCCRA(LW)/ GTCCRB(LW) compare match
0	1	1	1	1	1				Output toggled at GPTn.GTCCRA(LW)/ GTCCRB(LW) compare match
1	x	x	x	0	0	Input capture	—	—	Input capture at rising edge
1	x	x	x	0	1				Input capture at falling edge
1	x	x	x	1	0				Input capture at both edges
1	x	x	x	1	1				

x: Don't care

Note: In saw-wave mode, “end of a cycle” refers to an overflow (the value of the GTCNT(LW) counter changing from that of the GTPR(LW) register to 0000h (0000 0000h) in up-counting), an underflow (the value of the GTCNT(LW) counter changing from 0000h (0000 0000h) to that of the GTPR(LW) register in down-counting), or counter clearing by a hardware source, software, or synchronous clearing. It refers to a trough in triangle-wave mode (the value of the GTCNT(LW) counter changing from 0000h (0000 0000h) to 0001h (0000 0001h)).

Note: When the timing of an end of a cycle and the timing of a GTCCRA(LW)/GTCCRB(LW) compare match are the same in a compare-match operation, the b3 and b2 settings are given priority in saw-wave PWM mode, and the b1 and b0 settings are given priority in any other mode.

Note: Even though a compare match is set in GTIOR, output will not be made to the pins. GTONCR needs to be set separately.

22.2.18 General PWM Timer Interrupt Output Setting Register (GTINTAD)

Address(es): GPT0.GTINTAD 000C 2102h, GPT1.GTINTAD 000C 2182h, GPT2.GTINTAD 000C 2202h, GPT3.GTINTAD 000C 2282h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ADTRBDEN	ADTRBUEN	ADTRADEN	ADTRAUEN	EINT	—	—	—	GTINTPR[1:0]		GTINTF	GTINTE	GTINTD	GTINTC	GTINTB	GTINTA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	GTINTA	GTCCRA(LW) Compare Match/Input Capture Interrupt Enable	0: Interrupt request is disabled. 1: Interrupt request is enabled.	R/W
b1	GTINTB	GTCCRB(LW) Compare Match/Input Capture Interrupt Enable	0: Interrupt request is disabled. 1: Interrupt request is enabled.	R/W
b2	GTINTC	GTCCRC(LW) Compare Match Interrupt Enable	0: Interrupt request is disabled. 1: Interrupt request is enabled.	R/W
b3	GTINTD	GTCCRD(LW) Compare Match Interrupt Enable	0: Interrupt request is disabled. 1: Interrupt request is enabled.	R/W
b4	GTINTE	GTCCRE(LW) Compare Match Interrupt Enable	0: Interrupt request is disabled. 1: Interrupt request is enabled.	R/W
b5	GTINTF	GTCCRF(LW) Compare Match Interrupt Enable	0: Interrupt request is disabled. 1: Interrupt request is enabled.	R/W
b7, b6	GTINTPR[1:0]	GTPR(LW) Compare Match Interrupt Enable	b7 b6 0 0: Interrupt request is disabled. 0 1: In saw-wave mode, interrupt requests are enabled at overflows. In triangle-wave mode, interrupt requests are enabled at crests. 1 0: In saw-wave mode, interrupt requests are enabled at underflows. In triangle-wave mode, interrupt requests are enabled at troughs. 1 1: In saw-wave mode, interrupt requests are enabled at both overflows and underflows. In triangle-wave mode, interrupt requests are enabled at both crests and troughs.	R/W
b10 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b11	EINT	Dead Time Error Interrupt Enable	0: Interrupt request is disabled. 1: Interrupt request is enabled.	R/W
b12	ADTRAUEN	GTADTRA(LW) Compare Match (Up-Counting) A/D Converter Start Request Enable	0: A/D converter start request is disabled. 1: A/D converter start request is enabled.	R/W
b13	ADTRADEN	GTADTRA(LW) Compare Match (Down-Counting) A/D Converter Start Request Enable	0: A/D converter start request is disabled. 1: A/D converter start request is enabled.	R/W
b14	ADTRBUEN	GTADTRB(LW) Compare Match (Up-Counting) A/D Converter Start Request Enable	0: A/D converter start request is disabled. 1: A/D converter start request is enabled.	R/W
b15	ADTRBDEN	GTADTRB(LW) Compare Match (Down-Counting) A/D Converter Start Request Enable	0: A/D converter start request is disabled. 1: A/D converter start request is enabled.	R/W

Note: When changing the value of the GTMDR.LWA01 bit, the GPT0.GTINTAD register and GPT1.GTINTAD register become 0000h.
Note: When the GTMDR.LWA01 bit is 1, the value of the GPT0.GTINTAD register cannot be changed.
Note: When changing the value of the GTMDR.LWA23 bit, the GPT2.GTINTAD register and GPT3.GTINTAD register become 0000h.
Note: When the GTMDR.LWA23 bit is 1, the value of the GPT2.GTINTAD register cannot be changed.

The GTINTAD register enables or disables interrupt requests and A/D converter start requests. Values written to the GTINTAD register of the relevant channel in which write access is disabled by the GTWP.WPn bit (n = 0 to 3) are

ignored.

GTINTA Bit (GTCCRA(LW) Compare Match/Input Capture Interrupt Enable)

This bit enables or disables interrupt requests by GTCCRA(LW) compare match/input capture (GTCIA).

GTINTB Bit (GTCCRB(LW) Compare Match/Input Capture Interrupt Enable)

This bit enables or disables interrupt requests by GTCCRB(LW) compare match/input capture (GTCIB).

GTINTC Bit (GTCCRC(LW) Compare Match Interrupt Enable)

This bit enables or disables interrupt requests by GTCCRC(LW) compare match (GTCIC).

GTINTD Bit (GTCCRD(LW) Compare Match Interrupt Enable)

This bit enables or disables interrupt requests by GTCCRD(LW) compare match (GTCIC).

GTINTE Bit (GTCCRE(LW) Compare Match Interrupt Enable)

This bit enables or disables interrupt requests by GTCCRE(LW) compare match (GTCIE).

GTINTF Bit (GTCCRF(LW) Compare Match Interrupt Enable)

This bit enables or disables interrupt requests by GTCCRF(LW) compare match (GTCIE).

GTINTPR[1:0] Bits (GTPR(LW) Compare Match Interrupt Enable)

These bits enable or disable interrupt requests by a GTPR(LW) compare match (GTCNT(LW) counter overflow) and those by a GTCNT(LW) counter underflow (GTCIV/GTCIU).

EINT Bit (Dead Time Error Interrupt Enable)

This bit enables or disables interrupt requests by a dead time error (GDTE).

ADTRAUEN Bit (GTADTRA(LW) Compare Match (Up-Counting) A/D Converter Start Request Enable)

This bit enables or disables A/D converter start requests generated by GTADTRA(LW) compare matches during GTCNT(LW) up-counting.

ADTRADEN Bit (GTADTRA(LW) Compare Match (Down-Counting) A/D Converter Start Request Enable)

This bit enables or disables A/D converter start requests generated by GTADTRA(LW) compare matches during GTCNT(LW) down-counting.

ADTRBUEN Bit (GTADTRB(LW) Compare Match (Up-Counting) A/D Converter Start Request Enable)

This bit enables or disables A/D converter start requests generated by GTADTRB(LW) compare matches during GTCNT(LW) up-counting.

ADTRBDEN Bit (GTADTRB(LW) Compare Match (Down-Counting) A/D Converter Start Request Enable)

This bit enables or disables A/D converter start requests generated by GTADTRB(LW) compare matches during GTCNT(LW) down-counting.

22.2.19 General PWM Timer Control Register (GTCR)

Address(es): GPT0.GTCR 000C 2104h, GPT1.GTCR 000C 2184h, GPT2.GTCR 000C 2204h, GPT3.GTCR 000C 2284h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CCLR[1:0]		TPCS[3:0]				—	—	—	—	—	MD[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	MD[2:0]	Mode Select	b2 b0 0 0 0: Saw-wave PWM mode (single buffer or double buffer possible) 0 0 1: Saw-wave one-shot pulse mode (fixed buffer operation) 0 1 0: Setting prohibited 0 1 1: Setting prohibited 1 0 0: Triangle-wave PWM mode 1 (16-bit transfer at crest) (single buffer or double buffer possible) 1 0 1: Triangle-wave PWM mode 2 (16-bit transfer at crest and trough) (single buffer or double buffer possible) 1 1 0: Triangle-wave PWM mode 3 (32-bit transfer at trough) fixed buffer operation) 1 1 1: Setting prohibited	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b11 to b8	TPCS[3:0]	Timer Prescaler Select	b11 b8 0 0 0 0: PCLKA 0 0 0 1: PCLKA/2 0 0 1 0: PCLKA/4 0 0 1 1: PCLKA/8 0 1 0 0: PCLKA/16 0 1 0 1: PCLKA/32 0 1 1 0: PCLKA/64 0 1 1 1: PCLKA/256 1 0 0 0: PCLKA/1024 1 0 0 1: Setting prohibited 1 0 1 0: Setting prohibited 1 0 1 1: Setting prohibited 1 1 0 0: GTECLKA 1 1 0 1: GTECLKB 1 1 1 0: GTECLKC 1 1 1 1: GTECLKD	R/W
b13, b12	CCLR[1:0]	Counter Clear Source Select	b13 b12 0 0: None of the following clearing sources is specified. 0 1: Cleared by GTCCRA(LW) input capture 1 0: Cleared by GTCCRB(LW) input capture 1 1: Cleared by counter clearing in another channel performing synchronous clearing/synchronous operation	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: When changing the value of the GTMDR.LWA01 bit, the GPT0.GTCR register and GPT1.GTCR register become 0000h.
Note: When the GTMDR.LWA01 bit is 1, the value of the GPT0.GTCR register cannot be changed.
Note: When changing the value of the GTMDR.LWA23 bit, the GPT2.GTCR register and GPT3.GTCR register become 0000h.
Note: When the GTMDR.LWA23 bit is 1, the value of the GPT2.GTCR register cannot be changed.

The GTCR register controls the GTCNT(LW) counter. The GTCR register should be set while the GTCNT(LW) counter is stopped. Values written to the GTCR register of the relevant channel in which write access is disabled by the GTWP.WPn bit (n = 0 to 3) are ignored.

MD[2:0] Bits (Mode Select)

These bits select the GPT operating mode.

TPCS[3:0] Bits (Timer Prescaler Select)

These bits select a clock for the GTCNT(LW) counter. The clock source can be selected independently for each channel.
When an internal clock is selected as the clock to drive counting (by settings in the range from 0000b to 1000b), the first cycle of the count clock leads to the initial output specified by the GTIOR register on the GTIOCnA and GTIOCnB pins after the counter is started (the GTSTR.CSTn bit is 1), but the GTCNT(LW)) counter is not updated. Updating of the GTCNT(LW) counter begins from the next count clock.
When an external clock is selected (by settings in the range from 1100b to 1111b), the initial output on the GTIOCnA and GTIOCnB pins is produced at the start of counting (the GTSTR.CSTn bit is 1) and the GTCNT(LW) counter is updated from the first cycle of the count clock.

CCLR[1:0] Bits (Counter Clear Source Select)

These bits select a clearing source for the GTCNT(LW) counter. The source selected by these bits is added besides counter clearing by a hardware source and software.
When clearing in response to input capture is selected, transfer from the buffer registers to the GTCCRA(LW) and GTCCRB(LW) registers proceeds in response to by the counter clearing and input capture are performed, and other buffer transfer does not proceed. If clearing by a hardware source or software is occurs at the same time as clearing by input capture, other buffer transfer proceeds.
When synchronous clearing is selected in saw-wave mode, this is handled as clearing in response to the given counter overflow or underflow and the pin output and buffer transfers proceed. Even if the GTINTAD.GTINTPR[1:0] bits are set to 01b, 10b, or 11b at this time, the GTCIV or GTCIU interrupt is not requested. In triangle-wave mode, counter clearing is only performed and pin output and buffer transfer are not performed. The counter value becomes 0000h (0000 0000h), but it is not treated as a trough.
When 01b, 10b, or 11b is selected as a counter clear source, counter clearing by the source is executed whether the GPTn.GTCNT(LW) counter is running (the GTSTR.CSTn bit is 1 (n = 0 to 3)) or stopped (the GTSTR.CSTn bit is 0 (n = 0 to 3)).
When the count direction is down-counting (the GTST.TUCF flag is 0) in saw-wave mode, the GTCNT(LW) counter is set to the value set in the GTPR(LW) register by executing counter clearing. In other cases, the GTCNT(LW) counter is set to 0000h (0000 0000h).

22.2.20 General PWM Timer Buffer Enable Register (GTBER)

Address(es): GPT0.GTBER 000C 2106h, GPT1.GTBER 000C 2186h, GPT2.GTBER 000C 2206h, GPT3.GTBER 000C 2286h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	ADTDB	ADTTB[1:0]		—	ADTDA	ADTTA[1:0]		—	CCRSWT	PR[1:0]		CCRB[1:0]		CCRA[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	CCRA[1:0]	GTCCRA(LW) Buffer Operation	b1 b0 0 0: Buffer operation is not performed 0 1: Single buffer operation (GTCCRA(LW) ⇔ GTCCRC(LW)) 1 x: Double buffer operation (GTCCRA(LW) ⇔ GTCCRC(LW) ⇔ GTCCRD(LW))	R/W
b3, b2	CCRB[1:0]	GTCCRB(LW) Buffer Operation	b3 b2 0 0: Buffer operation is not performed 0 1: Single buffer operation (GTCCRB(LW) ⇔ GTCCRE(LW)) 1 x: Double buffer operation (GTCCRB(LW) ⇔ GTCCRE(LW) ⇔ GTCCRF(LW))	R/W
b5, b4	PR[1:0]	GTPR(LW) Buffer Operation	b5 b4 0 0: Buffer operation is not performed 0 1: Single buffer operation (GTPBR(LW) ⇒ GTPR(LW)) 1 x: Double buffer operation (GTPDBR(LW) ⇒ GTPBR(LW) ⇒ GTPR(LW))	R/W
b6	CCRSWT	GTCCRA(LW) and GTCCRB(LW) Forcible Buffer Operation	Writing 1 to this bit forcibly performs buffer transfer of GTCCRA(LW) and GTCCRB(LW). This bit automatically returns to 0 after the writing of 1. This bit is read as 0.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b9, b8	ADTTA[1:0]	GTADTRA(LW) Buffer Transfer Timing Select	• Triangle waves b9 b8 0 0: No transfer 0 1: Transfer at crest 1 0: Transfer at trough 1 1: Transfer at both crest and trough • Saw waves b9 b8 0 0: No transfer Values other than 0 0: Transfer at underflow (during down-counting), overflow (during up-counting), or counter clearing	R/W
b10	ADTDA	GTADTRA(LW) Double Buffer Operation	0: Single buffer operation (GTADTBRA(LW) ⇒ GTADTRA(LW)) 1: Double buffer operation (GTADTDBRA(LW) ⇒ GTADTBRA(LW) ⇒ GTADTRA(LW))	R/W
b11	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b13, b12	ADTTB[1:0]	GTADTRB(LW) Buffer Transfer Timing Select	• Triangle waves b13 b12 0 0: No transfer 0 1: Transfer at crest 1 0: Transfer at trough 1 1: Transfer at both crest and trough • Saw waves b13 b12 0 0: No transfer Values other than 0 0: Transfer at underflow (during down-counting), overflow (during up-counting), or counter clearing	R/W
b14	ADTDB	GTADTRB(LW) Double Buffer Operation	0: Single buffer operation (GTADTBRB(LW) ⇒ GTADTRB(LW)) 1: Double buffer operation (GTADTDBRB(LW) ⇒ GTADTBRB(LW) ⇒ GTADTRB(LW))	R/W
b15	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note: When changing the value of the GTMDR.LWA01 bit, the GPT0.GTBER register and GPT1.GTBER register become 0000h.

Note: When the GTMDR.LWA01 bit is 1, the value of the GPT0.GTBER register cannot be changed.
Note: When changing the value of the GTMDR.LWA23 bit, the GPT2.GTBER register and GPT3.GTBER register become 0000h.
Note: When the GTMDR.LWA23 bit is 1, the value of the GPT2.GTBER register cannot be changed.

The GTBER register makes settings for buffer operation.
The GTBER register should be set while the GTCNT(LW) counter is stopped. Values written to the GTBER register of the relevant channel in which write access is disabled by the GTWP.WPn bit (n = 0 to 3) are ignored.

CCRA[1:0] Bits (GTCCRA(LW) Buffer Operation)

These bits set buffer operation with the GTCCRA(LW), GTCCRC(LW), and GTCCRD(LW) registers combined. When buffer operation is restricted by the operating mode set in the GTCR register, the GTCR setting is given priority.*1

CCRB[1:0] Bits (GTCCRB(LW) Buffer Operation)

These bits set buffer operation with the GTCCRB(LW), GTCCRE(LW), and GTCCRF(LW) registers combined. When buffer operation is restricted by the operating mode set in the GTCR register, the GTCR setting is given priority.*1

PR[1:0] Bits (GTPR(LW) Buffer Operation)

These bits set buffer operation with the GTPR(LW), GTPBR(LW), and GTPDBR(LW) registers combined.

CCRSWT Bit (GTCCRA(LW) and GTCCRB(LW) Forcible Buffer Operation)

Writing 1 to the CCRSWT bit forcibly performs buffer transfer of the GTCCRA(LW) and GTCCRB(LW) registers. This bit automatically returns to 0 after the writing of 1. This bit is read as 0.
This bit is valid only when counting is stopped with compare match operation specified.
In saw-wave one-shot pulse mode and triangle-wave PWM mode 3, buffer transfer from the GTCCRD(LW) register to temporary register A(LW) and the GTCCRF(LW) register to temporary register B(LW) is performed using the forcible buffer operation while counting is stopped.

ADTTA[1:0] Bits (GTADTRA(LW) Buffer Transfer Timing Select)

These bits set the transfer timing for buffer operation of the GTADTRA(LW), GTADTBRA(LW), and GTADTDBRA(LW) registers.
When a buffer transfer is performed in saw-wave mode, the source of counter clearing is a hardware source, software, or synchronous clearing. During clearing by input capture, buffer transfer does not proceed.

ADTDA Bit (GTADTRA(LW) Double Buffer Operation)

These bits set buffer operation with the GTADTRA(LW), GTADTBRA(LW), and GTADTDBRA(LW) registers combined.

ADTTB[1:0] Bits (GTADTRB(LW) Buffer Transfer Timing Select)

These bits set the transfer timing for buffer operation of the GTADTRB(LW), GTADTBRB(LW), and GTADTDBRB(LW) registers.
When a buffer transfer is performed in saw-wave mode, the source of counter clearing is a hardware source, software, or synchronous clearing. During clearing by input capture, buffer transfer does not proceed.

ADTDB Bit (GTADTRB(LW) Double Buffer Operation)

These bits set buffer operation with the GTADTRB(LW), GTADTBRB(LW), and GTADTDBRB(LW) registers combined.

Note 1. The buffer operation mode is fixed in saw-wave one-shot pulse mode or triangle-wave PWM mode 3 (32-bit transfer at trough).

22.2.21 General PWM Timer Count Direction Register (GTUDC)

Address(es): GPT0.GTUDC 000C 2108h, GPT1.GTUDC 000C 2188h, GPT2.GTUDC 000C 2208h, GPT3.GTUDC 000C 2288h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OBDTYR	OBDTYF	OBDTY[1:0]		OADTYR	OADTYF	OADTY[1:0]		—	—	—	—	—	—	UDF	UD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	UD	Count Direction Setting	0: GTCNT(LW) counts down. 1: GTCNT(LW) counts up.	R/W
b1	UDF	Forcible Count Direction Setting	0: Not forcibly set 1: Forcibly set	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b9, b8	OADTY[1:0]	GTIOCA Pin Output Duty Setting	b9 b8 0 x: Compare matches determine the duty cycle of the output on the GTIOCA pin. 1 0: The duty cycle of the output on the GTIOCA pin is 0%. 1 1: The duty cycle of the output on the GTIOCA pin is 100%.	R/W
b10	OADTYF	GTIOCA Pin Output Duty Forced Setting	0: Duty of the GTIOCA pin output is not forcibly set. 1: Duty of the GTIOCA pin output is forcibly set.	R/W
b11	OADTYR	Output after Release of GTIOCA Pin Output 0%/100% Duty Cycle Settings	0: The function selected by the GTIOA[3:2] bits is applied to the output value when the duty cycle is set after release from the 0 or 100% duty-cycle setting. 1: The function selected by the GTIOA[3:2] bits is applied to the compare match output value which is masked after release from the 0 or 100% duty-cycle setting.	R/W
b13, b12	OBDTY[1:0]	GTIOCB Pin Output Duty Setting	b13 b12 0 x: Compare matches determine the duty cycle of the output on the GTIOCB pin 1 0: The duty cycle of the output on the GTIOCB pin is 0%. 1 1: The duty cycle of the output on the GTIOCB pin is 100%.	R/W
b14	OBDTYF	GTIOCB Pin Output Duty Forced Setting	0: Duty of the GTIOCB pin output is not forcibly set. 1: Duty of the GTIOCB pin output is forcibly set.	R/W
b15	OBDTYR	Output after Release of GTIOCB Pin Output 0%/100% Duty Cycle Settings	0: The function selected by the GTIOB[3:2] bits is applied to the output value when the duty cycle is set after release from the 0 or 100% duty-cycle setting. 1: The function selected by the GTIOB[3:2] bits is applied to the compare match output value which is masked after release from the 0 or 100% duty-cycle setting.	R/W

x: Don't care

Note: When changing the value of the GTMDR.LWA01 bit, the GPT0.GTUDC register and GPT1.GTUDC register become 0000h.
Note: When the GTMDR.LWA01 bit is 1, the value of the GPT0.GTUDC register cannot be changed.
Note: When changing the value of the GTMDR.LWA23 bit, the GPT2.GTUDC register and GPT3.GTUDC register become 0000h.
Note: When the GTMDR.LWA23 bit is 1, the value of the GPT2.GTUDC register cannot be changed.

The GTUDC register sets the direction in which the GTCNT(LW) counter counts (up-counting or down-counting). Values written to the GTUDC register of the relevant channel in which write access is disabled by the GTWP.WPn bit (n = 0 to 3) are ignored.

(1) Setting of Count Direction

- In saw-wave mode

When the UD value is set to 0 during up-counting, the count direction is changed at an overflow (count clock when GTCNT(LW) counter value is equal to the GTPR(LW) value). When the UD value is set to 1 during down-counting, the count direction is changed at an underflow (count clock when GTCNT(LW) counter value is equal to 0000h (0000 0000h)).

If the UD value is changed from 1 to 0 with the UDF bit being 0 and while counting is stopped, the counter starts up-counting and the count direction is changed at an overflow (count clock when GTCNT(LW) counter value is equal to GTPR(LW) value).
If the UD value is changed from 0 to 1 with the UDF bit being 0 and while counting is stopped, the counter starts down-counting and the count direction is changed at an underflow (count clock when GTCNT(LW) counter value is equal to 0000h (0000 0000h)).
When the UDF bit is set to 1 while counting is stopped, the UD bit value at that time is reflected in the count direction when counting starts.

- In triangle-wave mode

Even if the UD value is changed during counting, the change will not be reflected in the count direction.
If the UD value is modified while the UDF bit is 0 and counting is stopped, the change will not be reflected in the count direction when counting starts. If the UDF bit is set to 1 while counting is stopped, the UD bit value at that time is reflected in the count direction when counting starts.

UD Bit (Count Direction Setting)

This bit sets the count direction (up-counting or down-counting) for the GTCNT(LW) counter.

UDF Bit (Forcible Count Direction Setting)

This bit forcibly sets the count direction when the GTCNT(LW) counter starts operation as the UD value.
Only 0 should be written to this bit during count operation.
When 1 has been written to this bit while counting is stopped, this bit should be returned to 0 before counting starts.

(2) Setting of Output Duty

- In saw-wave mode

When the OADTY[1:0]/OBDTY[1:0] bits are changed during up-count operation, the duty setting changed at an overflow is reflected.
When the OADTY[1:0]/OBDTY[1:0] bits are changed during down-count operation, the duty setting changed at an underflow is reflected.
When the OADTYF/OBDTYF bit is 0 while count operation is stopped and the OADTY[1:0]/OBDTY[1:0] bits are changed, the change in the duty-cycle setting is not reflected in the first count operation, but the change is reflected on an overflow in the case of counting up and on an underflow in the case of counting down.
When the OADTYF/OBDTYF bit is 1 while count operation is stopped and the OADTY[1:0]/OBDTY[1:0] bits are changed, the change in the duty-cycle setting is immediately reflected during the first count operation.

- In triangle-wave mode

When the OADTY[1:0]/OBDTY[1:0] bits are changed during count operation, the duty-cycle setting changed at an underflow is reflected.
When the OADTYF/OBDTYF bit is 0 during count operation and the OADTY[1:0]/OBDTY[1:0] bits are changed, the duty-cycle setting changed during the first count operation is not reflected, the duty-cycle setting changed at an underflow is reflected.
When the OADTYF/OBDTYF bit is 1 while count operation is stopped and the OADTY[1:0]/OBDTY[1:0] bits are changed, the change in the duty-cycle setting is immediately reflected during the first count operation.

OmDTY[1:0] Bits (GTIOCm Pin Output Duty Cycle Setting) (m = A, B)

These bits set the output of the duty cycle (0%, 100% or compare match control) on the GTIOCm pin.

OmDTYF Bit (GTIOCm Pin Output Duty Forced Setting) (m = A, B)

This bit forcibly specifies the duty cycle at the start of the GTCNT(LW) counter in the OmDTY[1:0] bits.
Always write 0 to the bit during count operation.
When writing 1 to the bit while count operation is stopped, set the bit back to 0 by the end of the first cycle after the count operation started and specify the next cycle.

OmDTYR Bit (GTIOCm Pin Output 0%/100% Duty Setting Release Output) (m = A, B)

When the setting of a GTIOCm pin for a 0% or 100% duty cycle is forcibly changed due to a compare match, the output level on the pin is maintained after the period has elapsed if the value of the GTIOR.GTIOm[3:2] bits is 00b, but maintenance and a value to control toggling are selected after the period has elapsed if the output has become toggled and the setting is 11b.
The GPT internally continues to perform compare match operation during duty-cycle 0% or 100% operation. When the OmDTYR bit is 1, the value after the period has elapsed due this compare match operation is target for the GTIOR.GTIOm[3:2] bits.

22.2.22 General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register (GTITC)

Address(es): GPT0.GTITC 000C 210Ah, GPT1.GTITC 000C 218Ah, GPT2.GTITC 000C 220Ah, GPT3.GTITC 000C 228Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	ADTBL	—	ADTAL	—	IVTT[2:0]			IVTC[1:0]		ITLF	ITLE	ITLD	ITLC	ITLB	ITLA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ITLA	GTCCRA(LW) Compare Match/Input Capture Interrupt Link	0: Not linked with GTCIV/GTCIU interrupt skipping function. 1: Linked with GTCIV/GTCIU interrupt skipping function.	R/W
b1	ITLB	GTCCRB(LW) Compare Match/Input Capture Interrupt Link	0: Not linked with GTCIV/GTCIU interrupt skipping function. 1: Linked with GTCIV/GTCIU interrupt skipping function.	R/W
b2	ITLC	GTCCRC(LW) Compare Match Interrupt Link	0: Not linked with GTCIV/GTCIU interrupt skipping function. 1: Linked with GTCIV/GTCIU interrupt skipping function.	R/W
b3	ITLD	GTCCRD(LW) Compare Match Interrupt Link	0: Not linked with GTCIV/GTCIU interrupt skipping function. 1: Linked with GTCIV/GTCIU interrupt skipping function.	R/W
b4	ITLE	GTCCRE(LW) Compare Match Interrupt Link	0: Not linked with GTCIV/GTCIU interrupt skipping function. 1: Linked with GTCIV/GTCIU interrupt skipping function.	R/W
b5	ITLF	GTCCRF(LW) Compare Match Interrupt Link	0: Not linked with GTCIV/GTCIU interrupt skipping function. 1: Linked with GTCIV/GTCIU interrupt skipping function.	R/W
b7, b6	IVTC[1:0]	GTCIV/GTCIU Interrupt Skipping Function Select	b7 b6 0 0: Skipping is not performed 0 1: Both overflow and underflow for saw waves and crest for triangle waves are counted and skipped. 1 0: Both overflow and underflow for saw waves and trough for triangle waves are counted and skipped. 1 1: Both overflow and underflow for saw waves and both crest and trough for triangle waves are counted and skipped	R/W
b10 to b8	IVTT[2:0]	GTCIV/GTCIU Interrupt Skipping Count Select	b10 b8 0 0 0: Skipping is not performed 0 0 1: Skipping count of 1 0 1 0: Skipping count of 2 0 1 1: Skipping count of 3 1 0 0: Skipping count of 4 1 0 1: Skipping count of 5 1 1 0: Skipping count of 6 1 1 1: Skipping count of 7	R/W
b11	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b12	ADTAL	GTADTRA A/D Converter Start Request Link	0: Not linked with GTCIV/GTCIU interrupt skipping function. 1: Linked with GTCIV/GTCIU interrupt skipping function.	R/W
b13	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b14	ADTBL	GTADTRB A/D Converter Start Request Link	0: Not linked with GTCIV/GTCIU interrupt skipping function. 1: Linked with GTCIV/GTCIU interrupt skipping function.	R/W
b15	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note: When changing the value of the GTMDR.LWA01 bit, the GPT0.GTITC register and GPT1.GTITC register become 0000h.
Note: When the GTMDR.LWA01 bit is 1, the value of the GPT0.GTITC register cannot be changed.
Note: When changing the value of the GTMDR.LWA23 bit, the GPT2.GTITC register and GPT3.GTITC register become 0000h.
Note: When the GTMDR.LWA23 bit is 1, the value of the GPT2.GTITC register cannot be changed.

GTITC sets the skipping function for the GTCNT(LW) counter overflow (GTPR(LW) compare match) interrupt (GTCIV) and underflow interrupt (GTCIU) and also sets whether to link the other interrupts and A/D converter start requests with the GTCIV/GTCIU interrupt skipping function. Note that dead time error interrupts cannot be linked with

the GTCIV/GTCIU interrupt skipping function. Values written to the GTITC register of the relevant channel in which write access is disabled by the GTWP.WPn bit (n = 0 to 3) are ignored.

ITLA Bit (GTCCRA(LW) Compare Match/Input Capture Interrupt Link)

This bit specifies whether to link the GTCCRA(LW) compare match/input capture interrupt (GTCIA) with the GTCIV/GTCIU interrupt skipping function.

ITLB Bit (GTCCRB(LW) Compare Match/Input Capture Interrupt Link)

This bit specifies whether to link the GTCCRB(LW) compare match/input capture interrupt (GTCIB) with the GTCIV/GTCIU interrupt skipping function.

ITLC Bit (GTCCRC(LW) Compare Match Interrupt Link)

This bit specifies whether to link the GTCCRC(LW) compare match interrupt (GTCIC) with the GTCIV/GTCIU interrupt skipping function.

ITLD Bit (GTCCRD(LW) Compare Match Interrupt Link)

This bit specifies whether to link the GTCCRD(LW) compare match interrupt (GTCID) with the GTCIV/GTCIU interrupt skipping function.

ITLE Bit (GTCCRE(LW) Compare Match Interrupt Link)

This bit specifies whether to link the GTCCRE(LW) compare match interrupt (GTCIE) with the GTCIV/GTCIU interrupt skipping function.

ITLF Bit (GTCCRF(LW) Compare Match Interrupt Link)

This bit specifies whether to link the GTCCRF(LW) compare match interrupt (GTCIF) with the GTCIV/GTCIU interrupt skipping function.

IVTC[1:0] Bits (GTCIV/GTCIU Interrupt Skipping Function Select)

These bits set the skipping function for the GTPR(LW) compare match (GTCNT(LW) counter overflow) interrupt (GTCIV) and GTCNT(LW) counter underflow interrupt (GTCIU).

IVTT[2:0] Bits (GTCIV/GTCIU Interrupt Skipping Count Select)

These bits set the skipping count for the GTPR(LW) compare match (GTCNT(LW) counter overflow) interrupt (GTCIV) and GTCNT(LW) counter underflow interrupt (GTCIU).
When modifying the IVTT[2:0] bits, first set the IVTC[1:0] bits to 00b.

ADTAL Bit (GTADTRA A/D Converter Start Request Link)

This bit specifies whether to link the GTADTRA(LW) A/D converter start request with GTCIVn/GTCIUn interrupt skipping function (n = 0 to 3).

ADTBL Bit (GTADTRB A/D Converter Start Request Link)

This bit specifies whether to link the GTADTRB(LW) A/D converter start request with GTCIVn/GTCIUn interrupt skipping function (n = 0 to 3).

22.2.23 General PWM Timer Status Register (GTST)

Address(es): GPT0.GTST 000C 210Ch, GPT1.GTST 000C 218Ch, GPT2.GTST 000C 220Ch, GPT3.GTST 000C 228Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TUCF	—	—	—	DTEF	ITCNT[2:0]			—	—	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	—	Reserved	The read value is undefined. The write value should be 1.	R/W
b10 to b8	ITCNT[2:0]	GTCIV/GTCIU Interrupt Skipping Count Counter	Counter for counting the number of times a timer interrupt has been skipped.	R
b11	DTEF	Dead Time Error Flag	0: No dead time error has occurred. 1: A dead time error has occurred.	R
b14 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	TUCF	Count Direction Flag	0: The GTCNT(LW) counter counts downward. 1: The GTCNT(LW) counter counts upward.	R

Note: When changing the value of the GTMDR.LWA01 bit, the GPT0.GTST register and GPT1.GTST register become 0000h.
Note: When the GTMDR.LWA01 bit is 1, the value of the GPT0.GTST register cannot be changed.
Note: When changing the value of the GTMDR.LWA23 bit, the GPT2.GTST register and GPT3.GTST register become 0000h.
Note: When the GTMDR.LWA23 bit is 1, the value of the GPT2.GTST register cannot be changed.

GTST indicates the status of the GPT. Values written to the GTST register of the relevant channel in which write access is disabled by the GTWP.WPn bit (n = 0 to 3) are ignored.

ITCNT[2:0] Bits (GTCIV/GTCIU Interrupt Skipping Count Counter)

When the GTCIV/GTCIU interrupt skipping function is used (the GTITC.IVTC[1:0] bits are set to a value other than 00b), the counter is incremented by 1 every time the GTCIV/GTCIU interrupt source is generated.
[Clearing conditions]

- The GTCIV/GTCIU interrupt skipping function is not used (the GTITC.IVTT[2:0] bits are 000b when the GTITC.IVTC[1:0] bits are 00b).
- The GTCIV/GTCIU interrupt skipping count matches the specified count (the ITCNT[2:0] bits match the skipping count specified by the GTITC.IVTT[2:0] bits).

DTEF Flag (Dead Time Error Flag)

This flag indicates that the timer output toggle point after the automatic addition of dead time has exceeded the count period.
This flag returns to 0 when the timer output toggle point after the automatic addition of dead time is back within the period. This flag can only be read from. (Writing 0 to clear the flag is not allowed.)
When an interrupt by the DTEF flag is enabled (the GTINTAD.EINT bit is 1), a GDTE interrupt is generated every time the DTEF flag changes from 0 to 1.
[Setting condition]

- When a change point of the waveform after the automatic setting of dead time has exceeded the count period (in the following cases)
  Up-counting in triangle-wave mode: GTCCRA(LW) – GTDVU(LW) ≤ 0
  Down-counting in triangle-wave mode: GTCCRA(LW) – GTDVD(LW) < 0
  Up-counting in saw-wave one-shot pulse mode:
  When GTCCRA(LW) – GTDVU(LW) < 0, or GTCCRA(LW) + GTDVD(LW) > GTPR(LW)
  Down-counting in saw-wave one-shot pulse mode:

When GTCCRA(LW) + GTDVU(LW) > GTPR(LW), or GTCCRA(LW) – GTDVD(LW) < 0

[Clearing condition]

- The timer output toggle point after the automatic addition of dead time is within the count period.

TUCF Flag (Count Direction Flag)

This flag indicates the count direction of the GTCNT(LW) counter.

When the GTUDC.UDF bit is set to 1 while the count operation is stopped, the value of the GTUDC.UD bit at that time is set to the flag.

In triangle-wave mode whether count operation is stopped or in progress, the flag is set to 1 by clearing (a hardware source, software, input capture, or synchronous clearing). In saw-wave mode, the TUCF flag is not updated by clearing.

In saw-wave mode during count operation, the value of the GTUDC.UD bit is set to the TUCF flag at an overflow in up-counting or an underflow in down-counting. In triangle-wave mode, the flag is set to 0 at a crest, to 1 at a trough, and to 0 when a value larger than the value of the GTCNT(LW) counter is set to the GTPR(LW) register.

22.2.24 General PWM Timer Counter (GTCNT)

Address(es): GPT0.GTCNT 000C 210Eh, GPT1.GTCNT 000C 218Eh, GPT2.GTCNT 000C 220Eh, GPT3.GTCNT 000C 228Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note: When changing the value of the GTMDR.LWA01 bit, the GPT0.GTCNT register and GPT1.GTCNT register become 0000h.
Note: When the GTMDR.LWA01 bit is 1, the value of the GPT0.GTCNT register cannot be changed.
Note: When changing the value of the GTMDR.LWA23 bit, the GPT2.GTCNT register and GPT3.GTCNT register become 0000h.
Note: When the GTMDR.LWA23 bit is 1, the value of the GPT2.GTCNT register cannot be changed.

The GTCNT counter is a 16-bit readable/writable counter. There is one GTCNT counter for each channel. The GTCNT counter can be written only when count operation is stopped and cannot be written during count operation.

Access in 8-bit units to the GTCNT counter is prohibited, and it should be accessed in 16-bit units. Values written to the GTCNT counter of the relevant channel in which write access is disabled by the GTWP.WPn bit (n = 0 to 3) are ignored.

22.2.25 General PWM Timer Longword Counter (GTCNTLW)

Address(es): GPT01.GTCNTLW 000C 2300h, GPT23.GTCNTLW 000C 2380h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note: When changing the value of the GTMDR.LWA01 bit, the GPT01.GTCNTLW register becomes 0000 0000h.
Note: When the GTMDR.LWA01 bit is 0, the value of the GPT01.GTCNTLW register cannot be changed.
Note: When changing the value of the GTMDR.LWA23 bit, the GPT23.GTCNTLW register becomes 0000 0000h.
Note: When the GTMDR.LWA23 bit is 0, the value of the GPT23.GTCNTLW register cannot be changed.

The GTCNTLW counter is a 32-bit readable/writable counter.
The GTCNTLW counter can be written only when count operation is stopped and cannot be written during count operation. Access in 8- or 16-bit units to the GTCNTLW counter is prohibited, and it should be accessed in 32-bit units. Values written to the GTCNTLW counter of the relevant channel in which write access is disabled by the GTWP.WPn bit (n = 1, 3) are ignored.

22.2.26 General PWM Timer Compare Capture Register m (GTCCRm) (m = A to F)

Address(es): GPT0.GTCCRA 000C 2110h, GPT1.GTCCRA 000C 2190h, GPT2.GTCCRA 000C 2210h, GPT3.GTCCRA 000C 2290h,
GPT0.GTCCRB 000C 2112h, GPT1.GTCCRB 000C 2192h, GPT2.GTCCRB 000C 2212h, GPT3.GTCCRB 000C 2292h,
GPT0.GTCCRC 000C 2114h, GPT1.GTCCRC 000C 2194h, GPT2.GTCCRC 000C 2214h, GPT3.GTCCRC 000C 2294h,
GPT0.GTCCRD 000C 2116h, GPT1.GTCCRD 000C 2196h, GPT2.GTCCRD 000C 2216h, GPT3.GTCCRD 000C 2296h,
GPT0.GTCCRE 000C 2118h, GPT1.GTCCRE 000C 2198h, GPT2.GTCCRE 000C 2218h, GPT3.GTCCRE 000C 2298h,
GPT0.GTCCRF 000C 211Ah, GPT1.GTCCRF 000C 219Ah, GPT2.GTCCRF 000C 221Ah, GPT3.GTCCRF 000C 229Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: When changing the value of the GTMDR.LWA01 bit, the GPT0.GTCCRm registers and GPT1.GTCCRm registers become FFFFh.
Note: When the GTMDR.LWA01 bit is 1, the value of the GPT0.GTCCRm registers cannot be changed.
Note: When changing the value of the GTMDR.LWA23 bit, the GPT2.GTCCRm registers and GPT3.GTCCRm registers become FFFFh.
Note: When the GTMDR.LWA23 bit is 1, the value of the GPT2.GTCCRm registers cannot be changed.

The GTCCRm registers are 16-bit readable/writable registers. There are six GTCCRm registers for each channel.
The GTCCRA and GTCCRB registers are registers used for both output compare and input capture.
The GTCCRC and GTCCRE registers are compare match registers, and can also function as buffer registers for the GTCCRA and GTCCRB registers.
The GTCCRD and GTCCRF registers are compare match registers, and can also function as buffer registers for the GTCCRC and GTCCRE registers (double buffer registers for the GTCCRA and GTCCRB registers). Values written to the GTCCRm register of the relevant channel in which write access is disabled by the GTWP.WPn bit (n = 0 to 3) are ignored.

22.2.27 General PWM Timer Longword Compare Capture Register m (GTCCRmLW) (m = A to F)

Address(es): GPT01.GTCCRALW 000C 2304h, GPT01.GTCCRBLW 000C 2308h, GPT01.GTCCRCLW 000C 230Ch,
GPT01.GTCCRDLW 000C 2310h, GPT01.GTCCRELW 000C 2314h, GPT01.GTCCRFLW 000C 2318h,
GPT23.GTCCRALW 000C 2384h, GPT23.GTCCRBLW 000C 2388h, GPT23.GTCCRCLW 000C 238Ch,
GPT23.GTCCRDLW 000C 2390h, GPT23.GTCCRELW 000C 2394h, GPT23.GTCCRFLW 000C 2398h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: When changing the value of the GTMDR.LWA01 bit, the GPT01.GTCCRmLW registers become FFFF FFFFh.
Note: When the GTMDR.LWA01 bit is 0, the value of the GPT01.GTCCRm registers cannot be changed.

Note: When changing the value of the GTMDR.LWA23 bit, the GPT23.GTCCRm registers become FFFF FFFFh.
Note: When the GTMDR.LWA23 bit is 0, the value of the GPT23.GTCCRm registers cannot be changed.

The GTCCRmLW registers are 32-bit readable/writable registers.
The GTCCRALW and GTCCRBLW registers are registers used for both output compare and input capture.
The GTCCRCLW and GTCCRELW registers are compare match registers, and can also function as buffer registers for the GTCCRALW and GTCCRBLW registers.
The GTCCRDLW and GTCCRFLW registers are compare match registers, and can also function as buffer registers for the GTCCRCLW and GTCCRELW registers (double buffer registers for the GTCCRALW and GTCCRBLW registers).
Values written to the GTCCRmLW register of the relevant channel in which write access is disabled by the GTWP.WPn bit (n = 1, 3) are ignored.

22.2.28 General PWM Timer Period Setting Register (GTPR)

Address(es): GPT0.GTPR 000C 211Ch, GPT1.GTPR 000C 219Ch, GPT2.GTPR 000C 221Ch, GPT3.GTPR 000C 229Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: When changing the value of the GTMDR.LWA01 bit, the GPT0.GTPR register and GPT1.GTPR register become FFFFh.
Note: When the GTMDR.LWA01 bit is 1, the value of the GPT0.GTPR register cannot be changed.
Note: When changing the value of the GTMDR.LWA23 bit, the GPT2.GTPR register and GPT3.GTPR register become FFFFh.
Note: When the GTMDR.LWA23 bit is 1, the value of the GPT2.GTPR register cannot be changed.

The GTPR register is a 16-bit readable/writable register that sets the maximum count value of the GTCNT counter. There is one GTPR register for each channel.
In saw-wave mode, the value of (GTPR + 1) is the count period. In triangle-wave mode, the value of (GTPR value × 2) is the count period. Values written to the GTPR register of the relevant channel in which write access is disabled by the GTWP.WPn bit (n = 0 to 3) are ignored.

22.2.29 General PWM Timer Longword Period Setting Register (GTPRLW)

Address(es): GPT01.GTPRLW 000C 231Ch, GPT23.GTPRLW 000C 239Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: When changing the value of the GTMDR.LWA01 bit, the GPT01.GTPRLW register becomes FFFF FFFFh.
Note: When the GTMDR.LWA01 bit is 0, the value of the GPT01.GTPRLW register cannot be changed.
Note: When changing the value of the GTMDR.LWA23 bit, the GPT23.GTPRLW register becomes FFFF FFFFh.
Note: When the GTMDR.LWA23 bit is 0, the value of the GPT23.GTPRLW register cannot be changed.

The GTPRLW register is a 32-bit readable/writable register that sets the maximum count value of the GTCNTLW counter.

In saw-wave mode, the value of (GTPRLW + 1) is the count period. In triangle-wave mode, the value of (GTPRLW value × 2) is the count period.
Values written to the GTPRLW register of the relevant channel in which write access is disabled by the GTWP.WPn bit (n = 1, 3) are ignored.

22.2.30 General PWM Timer Period Setting Buffer Register (GTPBR)

Address(es): GPT0.GTPBR 000C 211Eh, GPT1.GTPBR 000C 219Eh, GPT2.GTPBR 000C 221Eh, GPT3.GTPBR 000C 229Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: When changing the value of the GTMDR.LWA01 bit, the GPT0.GTPBR register and GPT1.GTPBR register become FFFFh.
Note: When the GTMDR.LWA01 bit is 1, the value of the GPT0.GTPBR register cannot be changed.
Note: When changing the value of the GTMDR.LWA23 bit, the GPT2.GTPBR register and GPT3.GTPBR register become FFFFh.
Note: When the GTMDR.LWA23 bit is 1, the value of the GPT2.GTPBR register cannot be changed.

The GTPBR register is a 16-bit readable/writable register that functions as a buffer register for the GTPR register. There is one GTPBR register for each channel. Values written to the GTPBR register of the relevant channel in which write access is disabled by the GTWP.WPn bit (n = 0 to 3) are ignored.

22.2.31 General PWM Timer Longword Period Setting Buffer Register (GTPBRLW)

Address(es): GPT01.GTPBRLW 000C 2320h, GPT23.GTPBRLW 000C 23A0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: When changing the value of the GTMDR.LWA01 bit, the GPT01.GTPBRLW register becomes FFFF FFFFh.
Note: When the GTMDR.LWA01 bit is 0, the value of the GPT01.GTPBRLW register cannot be changed.
Note: When changing the value of the GTMDR.LWA23 bit, the GPT23.GTPBRLW register becomes FFFF FFFFh.
Note: When the GTMDR.LWA23 bit is 0, the value of the GPT23.GTPBRLW register cannot be changed.

The GTPBRLW register is a 32-bit readable/writable register that functions as a buffer register for the GTPRLW register. Values written to the GTPBRLW register of the relevant channel in which write access is disabled by the GTWP.WPn bit (n = 1, 3) are ignored.

22.2.32 General PWM Timer Period Setting Double Buffer Register (GTPDBR)

Address(es): GPT0.GTPDBR 000C 2120h, GPT1.GTPDBR 000C 21A0h, GPT2.GTPDBR 000C 2220h, GPT3.GTPDBR 000C 22A0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: When changing the value of the GTMDR.LWA01 bit, the GPT0.GTPDBR register and GPT1.GTPDBR register become FFFFh.
Note: When the GTMDR.LWA01 bit is 1, the value of the GPT0.GTPDBR register cannot be changed.
Note: When changing the value of the GTMDR.LWA23 bit, the GPT2.GTPDBR register and GPT3.GTPDBR register become FFFFh.
Note: When the GTMDR.LWA23 bit is 1, the value of the GPT2.GTPDBR register cannot be changed.

The GTPDBR register is a 16-bit readable/writable register that functions as a buffer register for the GTPBR register (a double buffer register for the GTPR register). There is one GTPDBR register for each channel. Values written to the GTPDBR register of the relevant channel in which write access is disabled by the GTWP.WPn bit (n = 0 to 3) are ignored.

22.2.33 General PWM Timer Longword Period Setting Double Buffer Register (GTPDBRLW)

Address(es): GPT01.GTPDBRLW 000C 2324h, GPT23.GTPDBRLW 000C 23A4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: When changing the value of the GTMDR.LWA01 bit, the GPT01.GTPDBRLW register becomes FFFF FFFFh.
Note: When the GTMDR.LWA01 bit is 0, the value of the GPT01.GTPDBRLW register cannot be changed.
Note: When changing the value of the GTMDR.LWA23 bit, the GPT23.GTPDBRLW register becomes FFFF FFFFh.
Note: When the GTMDR.LWA23 bit is 0, the value of the GPT23.GTPDBRLW register cannot be changed.

The GTPDBRLW register is a 32-bit readable/writable register that functions as a buffer register for the GTPBRLW register (a double buffer register for the GTPRLW register). Values written to the GTPDBRLW register of the relevant channel in which write access is disabled by the GTWP.WPn bit (n = 1, 3) are ignored.

22.2.34 A/D Converter Start Request Timing Register m (GTADTRm) (m = A, B)

Address(es): GPT0.GTADTRA 000C 2124h, GPT1.GTADTRA 000C 21A4h, GPT2.GTADTRA 000C 2224h, GPT3.GTADTRA 000C 22A4h, GPT0.GTADTRB 000C 212Ch, GPT1.GTADTRB 000C 21Ach, GPT2.GTADTRB 000C 222Ch, GPT3.GTADTRB 000C 22ACh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: When changing the value of the GTMDR.LWA01 bit, the GPT0.GTADTRm registers and GPT1.GTADTRm registers become

FFFFh.
Note: When the GTMDR.LWA01 bit is 1, the value of the GPT0.GTADTRm registers cannot be changed.
Note: When changing the value of the GTMDR.LWA23 bit, the GPT2.GTADTRm registers and GPT3.GTADTRm registers become FFFFh.
Note: When the GTMDR.LWA23 bit is 1, the value of the GPT2.GTADTRm registers cannot be changed.

The GTADTRm registers are 16-bit readable/writable registers that set the timing of A/D converter start request generation. When the GTADTRm value matches the GTCNT counter value, an A/D converter start request is generated. There are two GTADTRm registers for each channel.
Access in 8-bit units to the GTADTRm registers is prohibited, and they should be accessed in 16-bit units. Values written to the GTADTRm register of the relevant channel in which write access is disabled by the GTWP.WPn bit (n = 0 to 3) are ignored.

22.2.35 Longword A/D Converter Start Request Timing Register m (GTADTRmLW) (m = A, B)

Address(es): GPT01.GTADTRALW 000C 2328h, GPT01.GTADTRBLW 000C 2334h, GPT23.GTADTRALW 000C 23A8h, GPT23.GTADTRBLW 000C 23B4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: When changing the value of the GTMDR.LWA01 bit, the GPT01.GTADTRmLW registers become FFFF FFFFh.
Note: When the GTMDR.LWA01 bit is 0, the value of the GPT01.GTADTRmLW registers cannot be changed.
Note: When changing the value of the GTMDR.LWA23 bit, the GPT23.GTADTRmLW registers become FFFF FFFFh.
Note: When the GTMDR.LWA23 bit is 0, the value of the GPT23.GTADTRmLW registers cannot be changed.

The GTADTRmLW registers are 32-bit readable/writable registers that set the timing of A/D converter start request generation. When the GTADTRmLW value matches the GTCNTLW counter value, an A/D converter start request is generated.
Access in 8- or 16-bit units to the GTADTRmLW registers is prohibited, and they should be accessed in 32-bit units. Values written to the GTADTRmLW register of the relevant channel in which write access is disabled by the GTWP.WPn bit (n = 1, 3) are ignored.

22.2.36 A/D Converter Start Request Timing Buffer Register m (GTADTBRm) (m = A, B)

Address(es): GPT0.GTADTBRA 000C 2126h, GPT1.GTADTBRA 000C 21A6h, GPT2.GTADTBRA 000C 2226h, GPT3.GTADTBRA 000C 22A6h, GPT0.GTADTBRB 000C 212Eh, GPT1.GTADTBRB 000C 21AEh, GPT2.GTADTBRB 000C 222Eh, GPT3.GTADTBRB 000C 22AEh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: When changing the value of the GTMDR.LWA01 bit, the GPT0.GTADTBRm registers and GPT1.GTADTBRm registers become FFFFh.

Note: When the GTMDR.LWA01 bit is 1, the value of the GPT0.GTADTBRm registers cannot be changed.
Note: When changing the value of the GTMDR.LWA23 bit, the GPT2.GTADTBRm registers and GPT3.GTADTBRm registers become FFFFh.
Note: When the GTMDR.LWA23 bit is 1, the value of the GPT2.GTADTBRm registers cannot be changed.

The GTADTBRm registers are 16-bit readable/writable registers that function as buffer registers for the GTADTRm register. There are two GTADTBRm registers for each channel.
Access in 8-bit units to the GTADTBRm registers is prohibited, and they should be accessed in 16-bit units. Values written to the GTADTBRm register of the relevant channel in which write access is disabled by the GTWP.WPn bit (n = 0 to 3) are ignored.

22.2.37 Longword A/D Converter Start Request Timing Buffer Register m (GTADTBRmLW) (m = A, B)

Address(es): GPT01.GTADTBRALW 000C 232Ch, GPT01.GTADTBRBLW 000C 2338h, GPT23.GTADTBRALW 000C 23ACh, GPT23.GTADTBRBLW 000C 23B8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: When changing the value of the GTMDR.LWA01 bit, the GPT01.GTADTDBRmLW registers become FFFF FFFFh.
Note: When the GTMDR.LWA01 bit is 0, the value of the GPT01.GTADTDBRmLW registers cannot be changed.
Note: When changing the value of the GTMDR.LWA23 bit, the GPT23.GTADTDBRmLW registers become FFFF FFFFh.
Note: When the GTMDR.LWA23 bit is 0, the value of the GPT23.GTADTDBRmLW registers cannot be changed.

The GTADTBRmLW registers are 32-bit readable/writable registers that function as buffer registers for the GTADTRmLW register.
Access in 8- or 16-bit units to the GTADTBRmLW registers is prohibited, and they should be accessed in 32-bit units. Values written to the GTADTBRmLW register of the relevant channel in which write access is disabled by the GTWP.WPn bit (n = 1, 3) are ignored.

22.2.38 A/D Converter Start Request Timing Double Buffer Register m (GTADTDBRm) (m = A, B)

Address(es): GPT0.GTADTDBRA 000C 2128h, GPT1.GTADTDBRA 000C 21A8h, GPT2.GTADTDBRA 000C 2228h, GPT3.GTADTDBRA 000C 22A8h, GPT0.GTADTDBRB 000C 2130h, GPT1.GTADTDBRB 000C 21B0h, GPT2.GTADTDBRB 000C 2230h, GPT3.GTADTDBRB 000C 22B0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: When changing the value of the GTMDR.LWA01 bit, the GPT0.GTADTDBRm registers and GPT1.GTADTDBRm registers become FFFFh.
Note: When the GTMDR.LWA01 bit is 1, the value of the GPT0.GTADTDBRm registers cannot be changed.
Note: When changing the value of the GTMDR.LWA23 bit, the GPT2.GTADTDBRm registers and GPT3.GTADTDBRm registers

become FFFFh.
Note: When the GTMDR.LWA23 bit is 1, the value of the GPT2.GTADTDBRm registers cannot be changed.

The GTADTDBRm registers are 16-bit readable/writable registers that function as buffer registers for the GTADTBRm registers (double buffer registers for the GTADTRm registers). There are two GTADTDBRm registers for each channel. Access in 8-bit units to the GTADTDBRm registers is prohibited, and they should be accessed in 16-bit units. Values written to the GTADTDBRm register of the relevant channel in which write access is disabled by the GTWP.WPn bit (n = 0 to 3) are ignored.

22.2.39 Longword A/D Converter Start Request Timing Double Buffer Register m (GTADTDBRmLW) (m = A, B)

Address(es): GPT01.GTADTDBRALW 000C 2330h, GPT01.GTADTDBRBLW 000C 233Ch, GPT23.GTADTDBRALW 000C 23B0h, GPT23.GTADTDBRBLW 000C 23BCh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: When changing the value of the GTMDR.LWA01 bit, the GPT01.GTADTDBRmLW registers become FFFF FFFFh.
Note: When the GTMDR.LWA01 bit is 0, the value of the GPT01.GTADTDBRmLW registers cannot be changed.
Note: When changing the value of the GTMDR.LWA23 bit, the GPT23.GTADTDBRmLW registers become FFFF FFFFh.
Note: When the GTMDR.LWA23 bit is 0, the value of the GPT23.GTADTDBRmLW registers cannot be changed.

The GTADTDBRmLW registers are 32-bit readable/writable registers that function as buffer registers for the GTADTBRmLW registers (double buffer registers for the GTADTRmLW registers).
Access in 8- or 16-bit units to the GTADTDBRmLW registers is prohibited, and they should be accessed in 32-bit units. Values written to the GTADTDBRmLW register of the relevant channel in which write access is disabled by the GTWP.WPn bit (n = 1, 3) are ignored.

22.2.40 General PWM Timer Output Negate Control Register (GTONCR)

Address(es): GPT0.GTONCR 000C 2134h, GPT1.GTONCR 000C 21B4h, GPT2.GTONCR 000C 2234h, GPT3.GTONCR 000C 22B4h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OBE	OAE	—	SWN	—	—	—	NFV	NFS[3:0]				NVB	NVA	NEB	NEA
Value after reset:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	NEA	GTIOCnA Pin Negate Control Enable	0: Negate is disabled 1: Negate is enabled	R/W
b1	NEB	GTIOCnB Pin Negate Control Enable	0: Negate is disabled 1: Negate is enabled	R/W

Bit	Symbol	Bit Name	Description	R/W
b2	NVA	GTIOCnA Pin Negate Value Setting	0: GTIOCnA pin is set to 0 when negate control is performed. 1: GTIOCnA pin is set to 1 when negate control is performed.	R/W
b3	NVB	GTIOCnB Pin Negate Value Setting	0: GTIOCnB pin is set to 0 when negate control is performed. 1: GTIOCnB pin is set to 1 when negate control is performed.	R/W
b7 to b4	NFS[3:0]	GTIOC Output Negate Source Select	b7 b4 0 0 0 0: CMPC0 comparator output 0 0 0 1: CMPC1 comparator output 0 1 0 0: CMPC2 comparator output 0 1 0 1: CMPC3 comparator output 0 1 1 1: GTETRG pin input 1 x x x: Software control (control through SWN bit) Settings other than the above are prohibited when negate control is enabled by the NEA or NEB bit.	R/W
b8	NFV	Negate Source Polarity Select	0: Negate control is provided when the negate source has become 0. 1: Negate control is provided when the negate source has become 1.	R/W
b11 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12	SWN	Software Negate Control	When NFV bit is 0: 0: Negate control is provided. 1: Negate control is not provided. When NFV bit is 1: 0: Negate control is not provided. 1: Negate control is provided.	R/W
b13	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b14	OAE	GTIOCnA Pin Output Enable	0: Output is disabled 1: Output is enabled	R/W
b15	OBE	GTIOCnB Pin Output Enable	0: Output is disabled 1: Output is enabled	R/W

n = 0 to 3

Note: When changing the value of the GTMDR.LWA01 bit, the GPT0.GTONCR register and GPT1.GTONCR register become 0100h.
Note: When the GTMDR.LWA01 bit is 1, the value of the GPT0.GTONCR register cannot be changed.
Note: When changing the value of the GTMDR.LWA23 bit, the GPT2.GTONCR register and GPT3.GTONCR register become 0100h.
Note: When the GTMDR.LWA23 bit is 1, the value of the GPT2.GTONCR register cannot be changed.

The GTONCR register controls negate of the GTIOCnA pin output and GTIOCnB pin output. Values written to the GTONCR register of the relevant channel in which write access is disabled by the GTWP.WPn bit (n = 0 to 3) are ignored.

NEA Bit (GTIOCnA Pin Negate Control Enable)

This bit enables negate control of the GTIOCnA pin output.

NEB Bit (GTIOCnB Pin Negate Control Enable)

This bit enables negate control of the GTIOCnB pin output.

NVA Bit (GTIOCnA Pin Negate Value Setting)

This bit sets the output value of the GTIOCnA pin at negate control.

NVB Bit (GTIOCnB Pin Negate Value Setting)

This bit sets the output value of the GTIOCnB pin at negate control.

NFS[3:0] Bits (GTIOC Output Negate Source Select)

These bits select the negate source for the GTIOCnA pin output and GTIOCnB pin output.
If negate control is not enabled by the NEA or NEB bit, it is not necessary to change the value of these bits from their

initial value.

NFV Bit (Negate Source Polarity Select)

This bit selects the negate source polarity for the GTIOCnA pin output and GTIOCnB pin output.

SWN Bit (Software Negate Control)

This bit specifies whether to provide negate control for the GTIOCnA pin output and GTIOCnB pin output.
This bit setting is valid when software control is selected as the negate source (NFS[3] bit is set to 1).

OAE Bit (GTIOCnA Pin Output Enable)

This bit selects whether to output the GTIOCnA pin output. This bit setting is valid only when compare match has been set (the GTIOR.GTIOA[5] bit is 0).

OBE Bit (GTIOCnB Pin Output Enable)

This bit selects whether to output the GTIOCnB pin output.This bit setting is valid only when compare match has been set (the GTIOR.GTIOB[5] bit is 0).

22.2.41 General PWM Timer Dead Time Control Register (GTDTCR)

Address(es): GPT0.GTDTCR 000C 2136h, GPT1.GTDTCR 000C 21B6h, GPT2.GTDTCR 000C 2236h, GPT3.GTDTCR 000C 22B6h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	TDFER	—	—	TDBDE	TDBUE	—	—	—	TDE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TDE	Negative-Phase Waveform Setting	0: GTCCRB(LW) is set without using GTDVU(LW) and GTDVD(LW). 1: GTDVU(LW) and GTDVD(LW) are used to set the compare match value for negative-phase waveform with dead time automatically in GTCCRB(LW).	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	TDBUE	GTDVU(LW) Buffer Operation Enable	0: GTDVU(LW) buffer operation is disabled 1: GTDVU(LW) buffer operation is enabled	R/W
b5	TDBDE	GTDVD(LW) Buffer Operation Enable	0: GTDVD(LW) buffer operation is disabled 1: GTDVD(LW) buffer operation is enabled	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	TDFER	GTDVD(LW) Setting	0: GTDVU(LW) and GTDVD(LW) are set separately. 1: The value written to GTDVU(LW) is automatically set to GTDVD(LW).	R/W
b15 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: When changing the value of the GTMDR.LWA01 bit, the GPT0.GTDTCR register and GPT1.GTDTCR register become 0000h.
Note: When the GTMDR.LWA01 bit is 1, the value of the GPT0.GTDTCR register cannot be changed.
Note: When changing the value of the GTMDR.LWA23 bit, the GPT2.GTDTCR register and GPT3.GTDTCR register become 0000h.
Note: When the GTMDR.LWA23 bit is 1, the value of the GPT2.GTDTCR register cannot be changed.

The GTDTCR register enables automatic setting of a compare match value for negative-phase waveform with dead time. Values written to the GTDTCR register of the relevant channel in which write access is disabled by the GTWP.WPn bit (n = 0 to 3) are ignored.

TDE Bit (Negative-Phase Waveform Setting)

This bit sets whether to use the GTDVU(LW) and GTDVD(LW) registers. When the GTDVU(LW) and GTDVD(LW) registers are used, the compare match value for a negative-phase waveform with dead time that was obtained by the compare match value of a positive-phase waveform (GTCCRA(LW)) and the dead time value (GTDVU(LW) and GTDVD(LW)) is automatically set in the GTCCRB(LW) register.
This bit is enabled in saw-wave one-shot pulse mode and all triangle-wave PWM modes. The TDE bit setting is ignored in saw-wave PWM mode, and automatic setting does not take place.

The automatically set GTCCRB(LW) value has the following upper and lower limit values.

- Saw-wave one-shot pulse mode
  Upper limit value: the value set in the GTPR(LW) register
  Lower limit value: 0000h (0000 0000h)
- Triangle wave PWM mode
  Upper limit value: the value set in the GTPR(LW) register - 1
  Lower limit value: 0001h (0000 0001h) in up-counting, 0000h (0000 0000h) in down-counting

If the obtained GTCCRB(LW) value is not within the range between the upper and lower limits, the upper or lower limit is set in the GTCCRB(LW) register. However, when [GTCCRA(LW) – GTDVU(LW)] is greater than GTPR(LW) during up-counting in saw-wave mode, or when [GTCCRA(LW) – GTDVD(LW)] is greater than GTPR(LW) during down-

counting in saw-wave mode, the obtained value is set in the GTCCRB(LW) register.
If the obtained value is outside the limit range and the upper or lower limit is set, the GTST.DTEF flag becomes 1. However, if the obtained GTCCRB(LW) value exceeds the upper limit in triangle-wave PWM mode, the GTST.DTEF flag becomes 0.

TDBUE Bit (GTDVU(LW) Buffer Operation Enable)

This bit enables buffer operation with the GTDVU(LW) and GTDBU(LW) registers combined.
The buffer transfer timing is at an overflow or underflow for saw waves, and the trough for triangle waves.

TDBDE Bit (GTDVD(LW) Buffer Operation Enable)

This bit enables buffer operation with the GTDVD(LW) and GTDBD(LW) registers combined.
The buffer transfer timing is at an overflow or underflow for saw waves, and the trough for triangle waves.
When this bit and the TDFER bit are set to 1 simultaneously, the TDFER bit setting is given priority.

TDFER Bit (GTDVD(LW) Setting)

This bit sets whether or not the value written to the GTDVU(LW) register is also set to the GTDVD(LW) register automatically.

22.2.42 General PWM Timer Dead Time Value Register m (GTDVm) (m = U, D)

Address(es): GPT0.GTDVU 000C 2138h, GPT1.GTDVU 000C 21B8h, GPT2.GTDVU 000C 2238h, GPT3.GTDVU 000C 22B8h, GPT0.GTDVD 000C 213Ah, GPT1.GTDVD 000C 21Bah, GPT2.GTDVD 000C 223Ah, GPT3.GTDVD 000C 22BAh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: When changing the value of the GTMDR.LWA01 bit, the GPT0.GTDVm registers and GPT1.GTDVm registers become FFFFh.
Note: When the GTMDR.LWA01 bit is 1, the value of the GPT0.GTDVm registers cannot be changed.
Note: When changing the value of the GTMDR.LWA23 bit, the GPT2.GTDVm registers and GPT3.GTDVm registers become FFFFh.
Note: When the GTMDR.LWA23 bit is 1, the value of the GPT2.GTDVm registers cannot be changed.

The GTDVm registers are 16-bit readable/writable registers that set the dead time for generating PWM waveforms with dead time.
There are two GTDVm registers for each channel: the GTDVU register used for up-counting and the GTDVD register used for down-counting.
Do not set a value greater than or equal to the setting value of the GTPR register in the GTDVm register.
In addition, when using the dead-time automatic setting function, do not set a value that makes a change point of the waveform exceeding the count period. The change point of the negative-phase waveform, which is automatically calculated, is obtained by reading the GTCCRB register. When using the GTDVm register, writing to the GTCCRB register is prohibited. When setting this register to 0000h, waveforms without dead time are output.
Access in 8-bit units to the GTDVm registers is prohibited, and they should be accessed in 16-bit units. Values written to the GTDVm register of the relevant channel in which write access is disabled by the GTWP.WPn bit (n = 0 to 3) are ignored.

22.2.43 General PWM Timer Longword Dead Time Value Register m (GTDVmLW) (m = U, D)

Address(es): GPT01.GTDVULW 000C 2340h, GPT01.GTDVDLW 000C 2344h, GPT23.GTDVULW 000C 23C0h, GPT23.GTDVDLW 000C 23C4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: When changing the value of the GTMDR.LWA01 bit, the GPT01.GTDVmLW registers become FFFF FFFFh.
Note: When the GTMDR.LWA01 bit is 0, the value of the GPT01.GTDVmLW registers cannot be changed.
Note: When changing the value of the GTMDR.LWA23 bit, the GPT23.GTDVmLW registers become FFFF FFFFh.
Note: When the GTMDR.LWA23 bit is 0, the value of the GPT23.GTDVmLW registers cannot be changed.

The GTDVmLW registers are 32-bit readable/writable registers that set the dead time for generating PWM waveforms with dead time. The GTDVULW register is used for up-counting and the GTDVDLW register is used for down-counting.
Do not set the value that exceeds the value set in the GTPRLW register in the GTDVmLW register.
Do not set a value greater than or equal to the setting value of the GTPRLW register in the GTDVmLW register.
In addition, when using the dead-time automatic setting function, do not set a value that makes a change point of the waveform exceeding the count period. The change point of the negative-phase waveform, which is automatically calculated, is obtained by reading the GTCCRBLW register. When using the GTDVmLW register, writing to the GTCCRBLW register is prohibited. When setting this register to 0000 0000h, waveforms without dead time are output.
Access in 8- or 16-bit units to the GTDVmLW registers is prohibited, and they should be accessed in 16-bit units. Values written to the GTDVmLW register of the relevant channel in which write access is disabled by the GTWP.WPn bit (n = 1, 3) are ignored.

22.2.44 General PWM Timer Dead Time Buffer Register m (GTDBm) (m = U, D)

Address(es): GPT0.GTDBU 000C 213Ch, GPT1.GTDBU 000C 21BCh, GPT2.GTDBU 000C 223Ch, GPT3.GTDBU 000C 22BCh, GPT0.GTDBD 000C 213Eh, GPT1.GTDBD 000C 21BEh, GPT2.GTDBD 000C 223Eh, GPT3.GTDBD 000C 22BEh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: When changing the value of the GTMDR.LWA01 bit, the GPT0.GTDBm registers and GPT1.GTDBm registers become FFFFh.
Note: When the GTMDR.LWA01 bit is 1, the value of the GPT0.GTDBm registers cannot be changed.
Note: When changing the value of the GTMDR.LWA23 bit, the GPT2.GTDBm registers and GPT3.GTDBm registers become FFFFh.
Note: When the GTMDR.LWA23 bit is 1, the value of the GPT2.GTDBm registers cannot be changed.

The GTDBm registers are 16-bit readable/writable registers that function as buffer registers for the GTDVm registers. There are two GTDBm registers for each channel.
Values written to the GTDBm register of the relevant channel in which write access is disabled by the GTWP.WPn bit (n = 0 to 3) are ignored.

22.2.45 General PWM Timer Longword Dead Time Buffer Register m (GTDBmLW) (m = U, D)

Address(es): GPT01.GTDBULW 000C 2348h, GPT01.GTDBDLW 000C 234Ch, GPT23.GTDBULW 000C 23C8h, GPT23.GTDBDLW 000C 23CCh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: When changing the value of the GTMDR.LWA01 bit, the GPT0.GTDBmLW registers become FFFF FFFFh.
Note: When the GTMDR.LWA01 bit is 0, the value of the GPT0.GTDBmLW registers cannot be changed.
Note: When changing the value of the GTMDR.LWA23 bit, the GPT2.GTDBmLW registers become FFFF FFFFh.
Note: When the GTMDR.LWA23 bit is 0, the value of the GPT2.GTDBmLW registers cannot be changed.

The GTDBmLW registers are 32-bit readable/writable registers that function as buffer registers for the GTDVmLW registers.
Values written to the GTDBmLW register of the relevant channel in which write access is disabled by the GTWP.WPn bit (n = 1, 3) are ignored.

22.2.46 General PWM Timer Output Protection Function Status Register (GTSOS)

Address(es): GPT0.GTSOS 000C 2140h, GPT1.GTSOS 000C 21C0h, GPT2.GTSOS 000C 2240h, GPT3.GTSOS 000C 22C0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SOS[1:0]	
Value after reset:	0	0	0	0	0	0	x	x	0	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b1, b0	SOS[1:0]	Output Protection Function Status	b1 b0 0 0: Normal operation 0 1: Protected state (GTCCRA(LW) = 0 is set during transfer at trough or crest) 1 0: Protected state (GTCCRA(LW) ≥ GTPR(LW) is set during transfer at trough) 1 1: Protected state (GTCCRA(LW) ≥ GTPR(LW) is set during transfer at crest)	R
b7 to b2	—	Reserved	These bits are read as 0 and cannot be modified.	R
b9, b8	—	Reserved	The read value is undefined. These bits cannot be modified.	R
b15 to b10	—	Reserved	These bits are read as 0 and cannot be modified.	R

Note: When changing the value of the GTMDR.LWA01 bit, the GPT0.GTSOS register and GPT1.GTSOS register become 0000 00xx 0000 0000b.
Note: When changing the value of the GTMDR.LWA23 bit, the GPT2.GTSOS register and GPT3.GTSOS register become 0000 00xx 0000 0000b.

The GTSOS register is a status register that indicates the status of the output protection function. The output protection function is enabled only when the dead time is automatically set (the GTDTCR.TDE bit is 1) in triangle-wave mode.

SOS[1:0] Bits (Output Protection Function Status)

This bit indicates the status of the output protection function in triangle-wave PWM mode. For details of the output protection function, see section 22.6.4, Output Protection Function for GTIOC Pin Output.

22.2.47 General PWM Timer Output Protection Function Temporary Release Register (GTSOTR)

Address(es): GPT0.GTSOTR 000C 2142h, GPT1.GTSOTR 000C 21C2h, GPT2.GTSOTR 000C 2242h, GPT3.GTSOTR 000C 22C2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SOTR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SOTR	Output Protection Function Temporary Release	0: Protected state is not released 1: Protected state is released	R/W
b15 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: When changing the value of the GTMDR.LWA01 bit, the GPT0.GTSOTR register and GPT1.GTSOTR register become 0000h.
Note: When the GTMDR.LWA01 bit is 1, the value of the GPT0.GTSOTR register cannot be changed.
Note: When changing the value of the GTMDR.LWA23 bit, the GPT2.GTSOTR register and GPT3.GTSOTR register become 0000h.
Note: When the GTMDR.LWA23 bit is 1, the value of the GPT2.GTSOTR register cannot be changed.

The GTSOTR register temporarily releases the protected state of GTIOCnB pin output when output protection has been set.

The protected state can be released only for the case of the GTSOS.SOS[1:0] bits are 10b (protected state in which GTCCRA(LW) ≥ GTPR(LW) has occurred during transfer at trough). The protected state cannot be released for any other case. Values written to the GTSOTR register of the relevant channel in which write access is disabled by the GTWP.WPn bit (n = 0 to 3) are ignored.

SOTR Bit (Output Protection Function Temporary Release)

This bit sets whether to temporarily release the protected state of the GTIOCnB pin output in an output protected state. After the SOTR bit has been set to 1, the output protection function is canceled from the first trough. After the SOTR bit has been set to 0, output protection is resumed from the first trough.

22.3 Operation

22.3.1 Basic Operation

Each channel has a GTCNT(LW) counter, GTPR(LW) register, and GTCCRm(LW) register (m = A to F). The GTCNT(LW) counter performs up-counting, down-counting, or up-/down-counting, available for periodic count operation. The timer period is set by the GTPR(LW) register.
In this section, up-counting and down-counting operation is referred to as saw-wave (half-wave) operation. Up-/down-counting operation is referred to as triangle-wave (full-wave) operation.

22.3.1.1 Counter Operation

(1) Periodic Count Operation (in Up-Counting)

The GTCNT(LW) counter in each channel starts up-counting when the corresponding GTSTS.CSTn bit is set to 1. When the GTCNT(LW) counter value changes from the GTPR(LW) register value to 0000h (0000 0000h) (overflow), a GTCIV interrupt is requested if the GTINTAD.GTINTPR[0] bit is 1. After GTCNT(LW) overflows, up-counting is resumed from 0000h (0000 0000h).
Figure 22.3 shows an example of periodic count operation in up-counting.

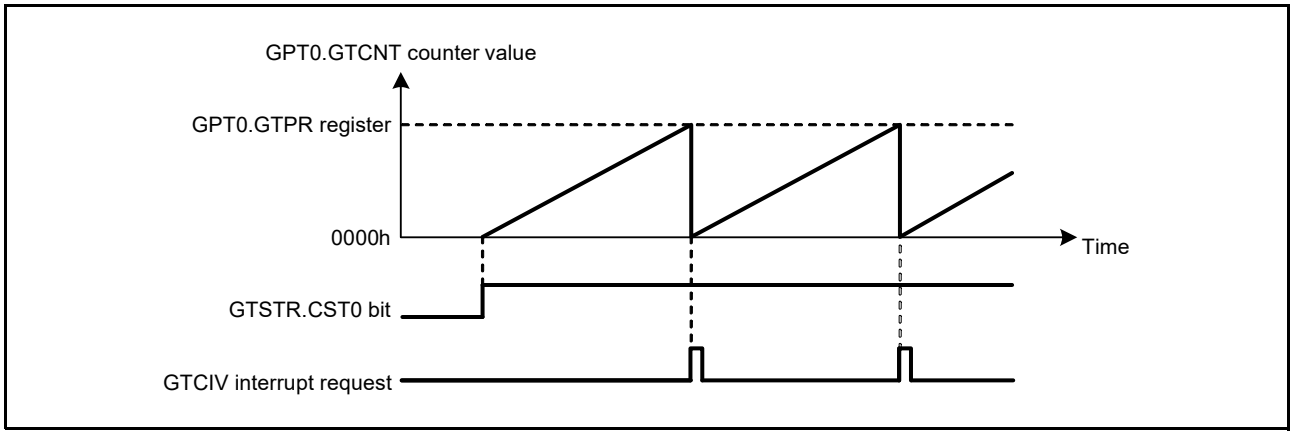


Figure 22.3 Example of Periodic Count Operation (in Up-Counting)

Figure 22.4 shows an example for setting periodic count operation in up-counting.

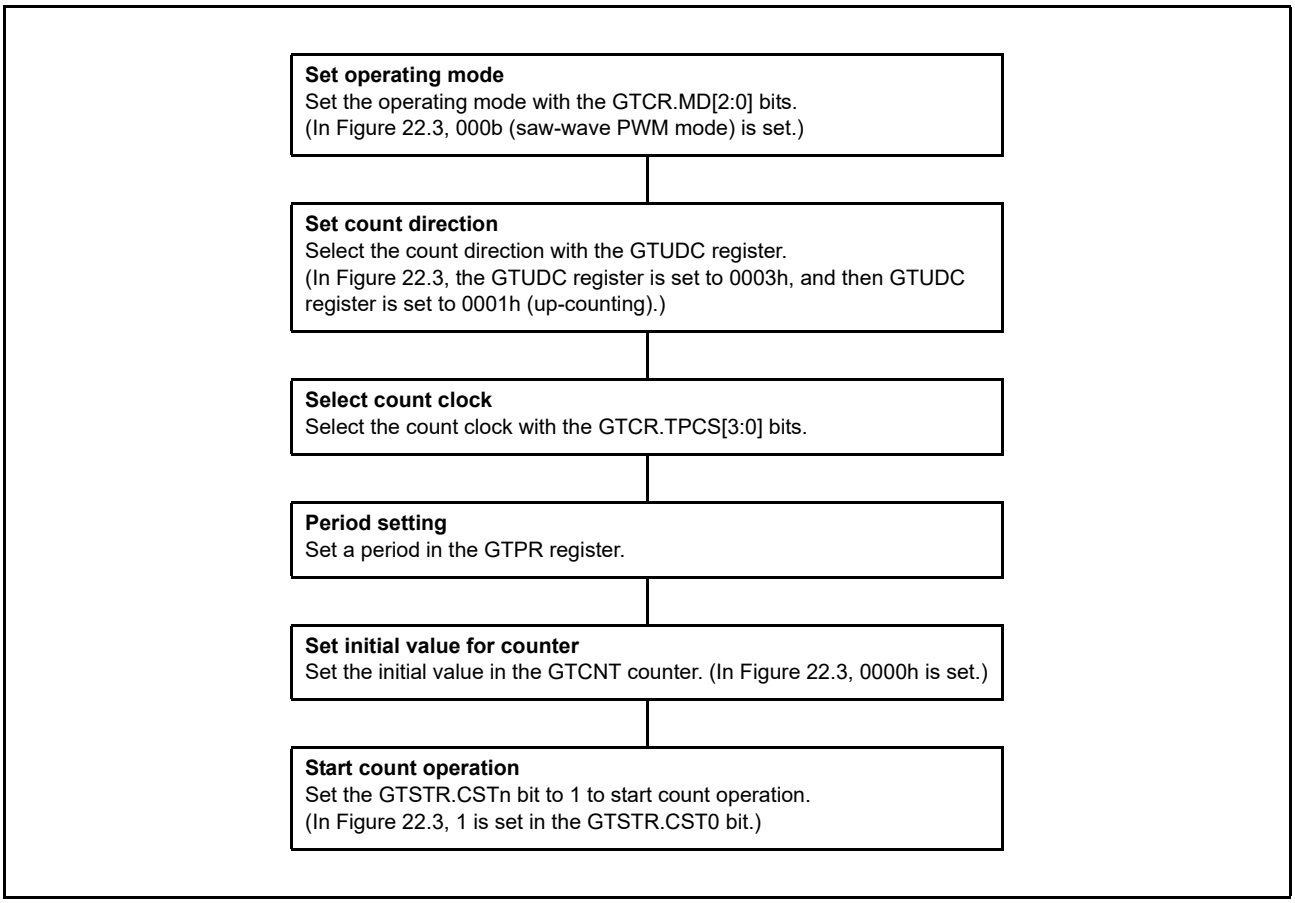


Figure 22.4 Example for Setting Periodic Count Operation (in Up-Counting)

(2) Periodic Count Operation (in Down-Counting)

The GTCNT(LW) counter in each channel can perform down-counting by setting GTUDC.
When the GTCNT(LW) counter value changes from 0000h (0000 0000h) to the GTPR(LW) register value (underflow), a GTCIU interrupt is requested if the GTINTAD.GTINTPR[1] bit is 1. After the GTCNT(LW) counter underflows, down-counting is resumed from the GTPR(LW) value.
Figure 22.5 shows an example of periodic count operation in down-counting.

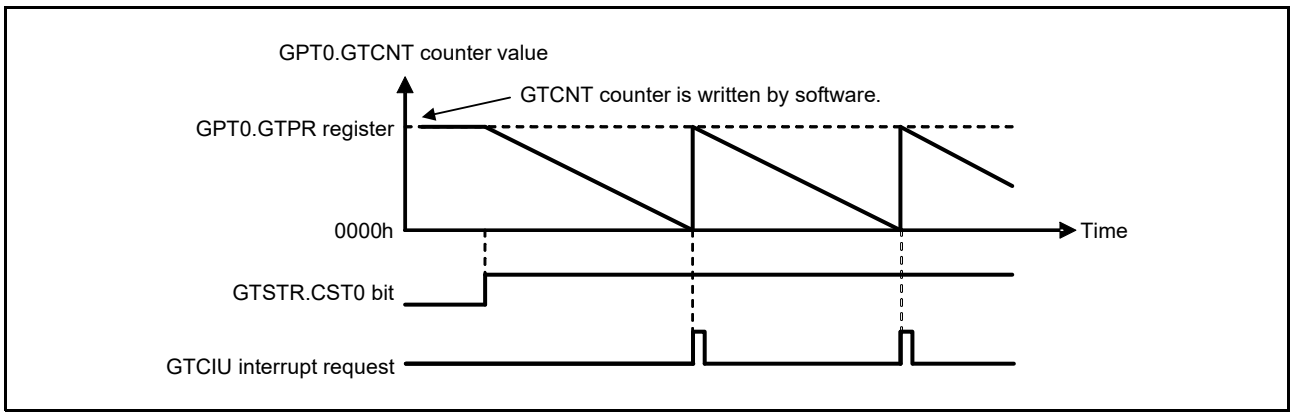


Figure 22.5 Example of Periodic Count Operation (in Down-Counting)

Figure 22.6 shows an example for setting periodic count operation in down-counting.

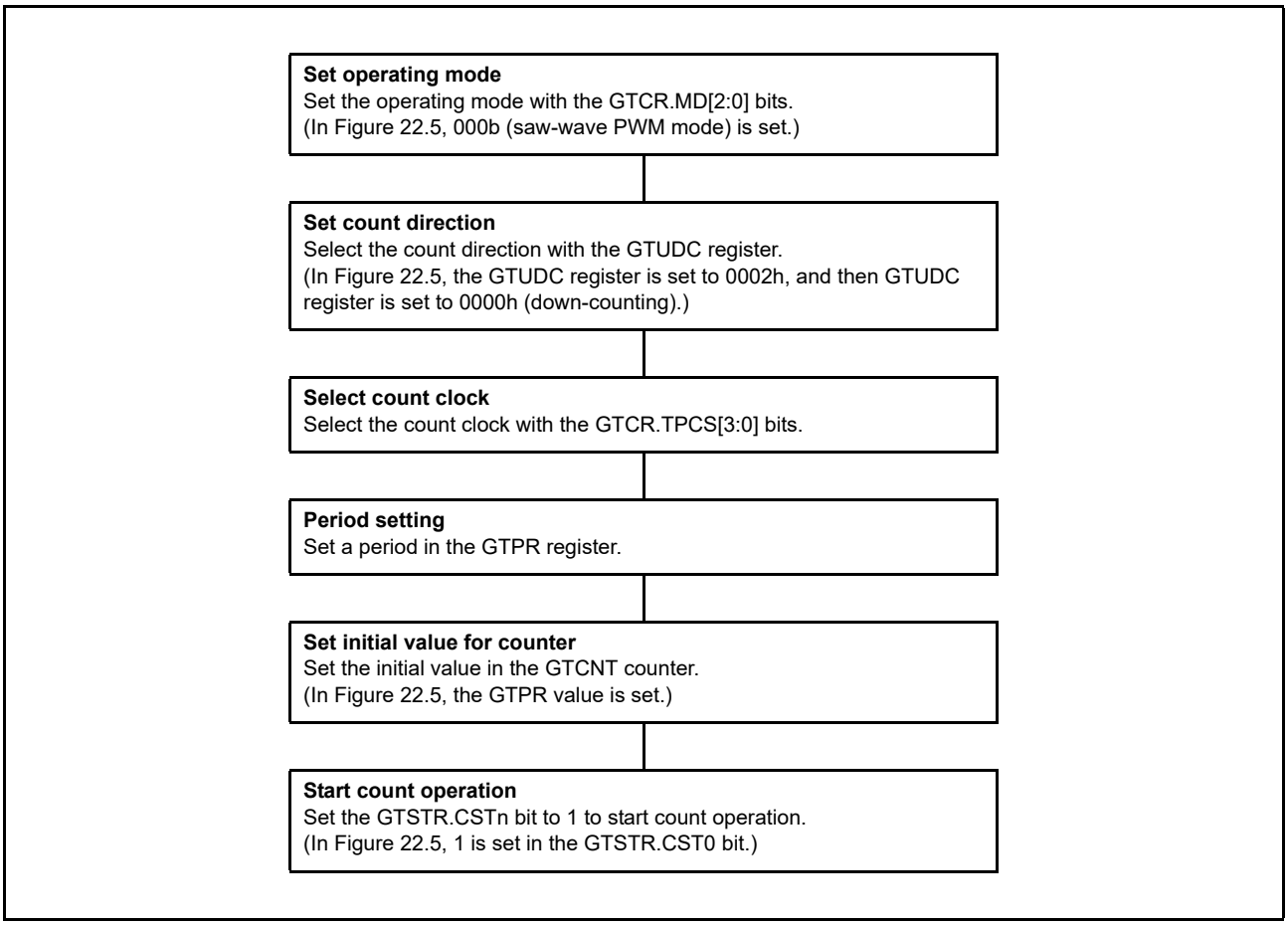


Figure 22.6 Example for Setting Periodic Count Operation (in Down-Counting)

22.3.1.2 Waveform Output by Compare Match

Compare match refers to when the GPTn.GTCNT(LW) counter value matches the GPTn.GTCCRA(LW) or GPTn.GTCCRB(LW) register value (n = 0 to 3). Low, high, or toggle output can be performed from the GTIOCnA or GTIOCnB pin in synchronization with the count clock after a compare match occurs.
In addition, the GTIOCnA or GTIOCnB pin output can be low, high, or toggled at the “end of the cycle” which is determined by the GPTn.GTPR(LW) register.
The end of the cycle is:

- For saw waves in up-counting: When the GPTn.GTCNT(LW) counter value changes from the GPTn.GTPR(LW) register value to 0 (overflow)
- For saw waves in down-counting: When the GPTn.GTCNT(LW) counter value changes from 0000h (0000 0000h) to the GPTn.GTPR(LW) register value (underflow)
- For triangle waves: When the GPTn.GTCNT(LW) counter value changes from 0000h (0000 0000h) to 0001h (0000 0001h) (trough)

(1) Low Output and High Output

Figure 22.7 shows an example of low output and high output operation by a compare match of GTCCRA and GTCCRB.
In this example, the GPT0.GTCNT counter performs up-counting, and settings have been made so that high is output from the GTIOC0A pin by a GPT0.GTCCRA compare match, and low is output from the GTIOC0B pin by a GPT0.GTCCRB compare match. The pin level does not change when the specified level and pin level match.

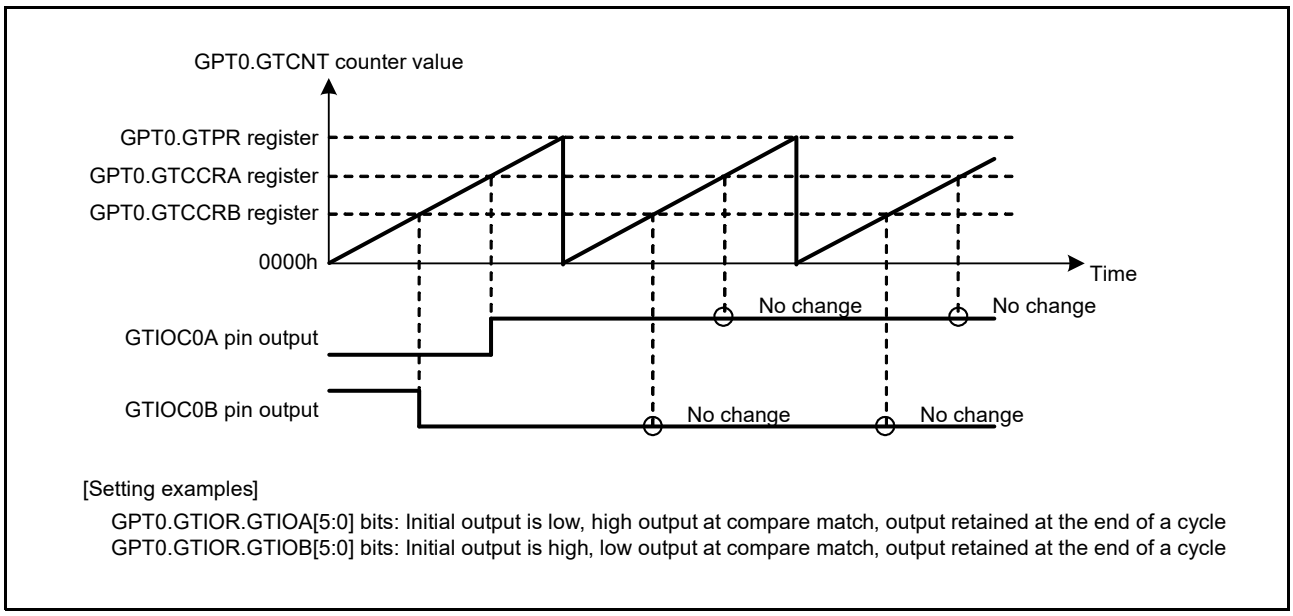


Figure 22.7 Example of Low Output and High Output Operation

Figure 22.8 shows an example for setting low output and high output operation.

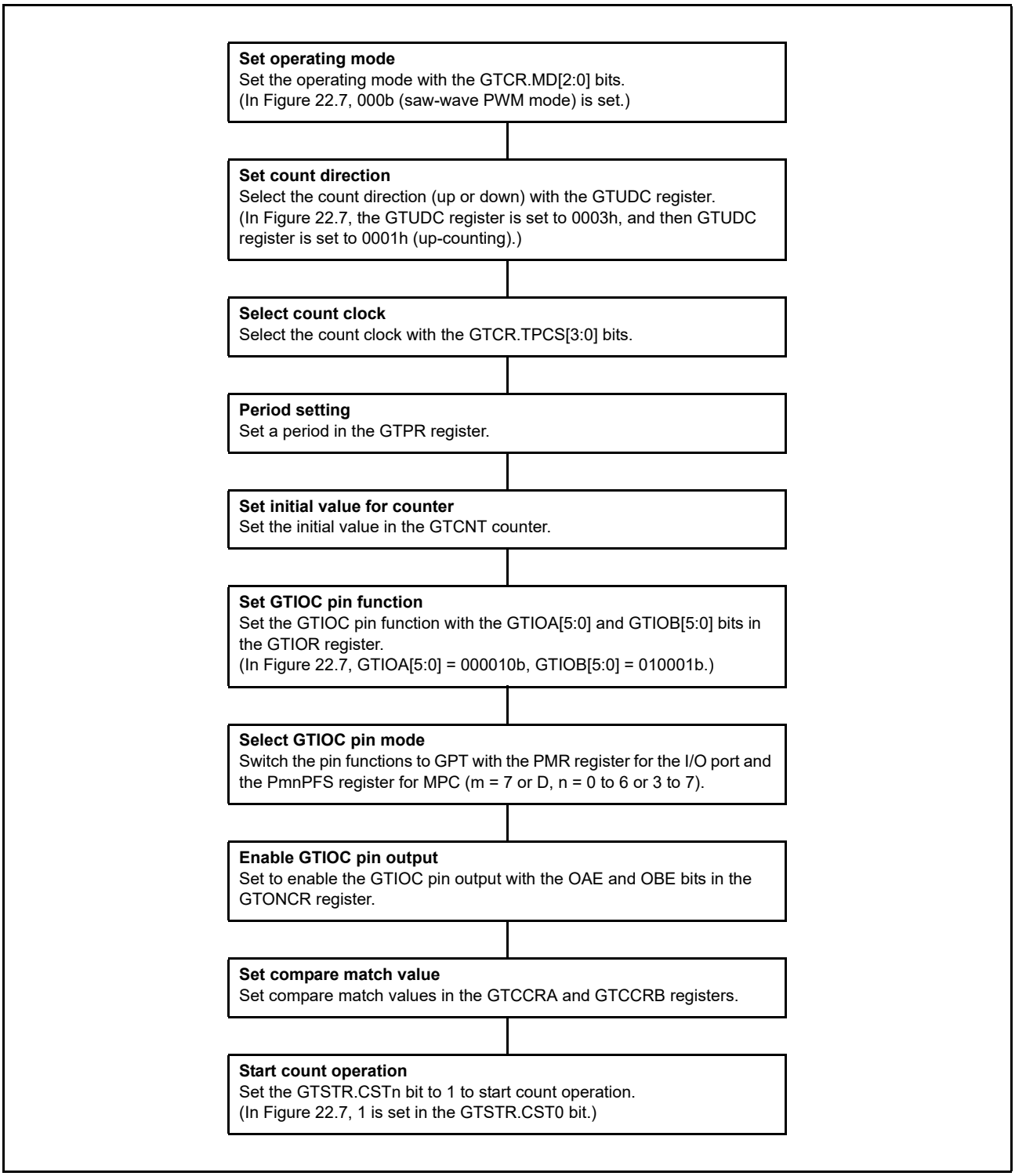


Figure 22.8 Example for Setting Low Output and High Output Operation

(2) Toggled Output

Figure 22.9 and Figure 22.10 show examples of toggled output operation by compare matches of GTCCRA and GTCCRB. In Figure 22.9, the GPT0.GTCNT counter performs up-counting, and settings have been made so that the GTIOC0A pin output by a GPT0.GTCCRA compare match and GTIOC0B pin output by a GPT0n.GTCCRB compare match are toggled.

In Figure 22.10, the GPT0.GTCNT counter performs up-counting, and settings have been made so that the GTIOC0A output is toggled by a compare match of GPT0.GTCCRA and the GTIOC0B output is toggled at the end of the cycle.

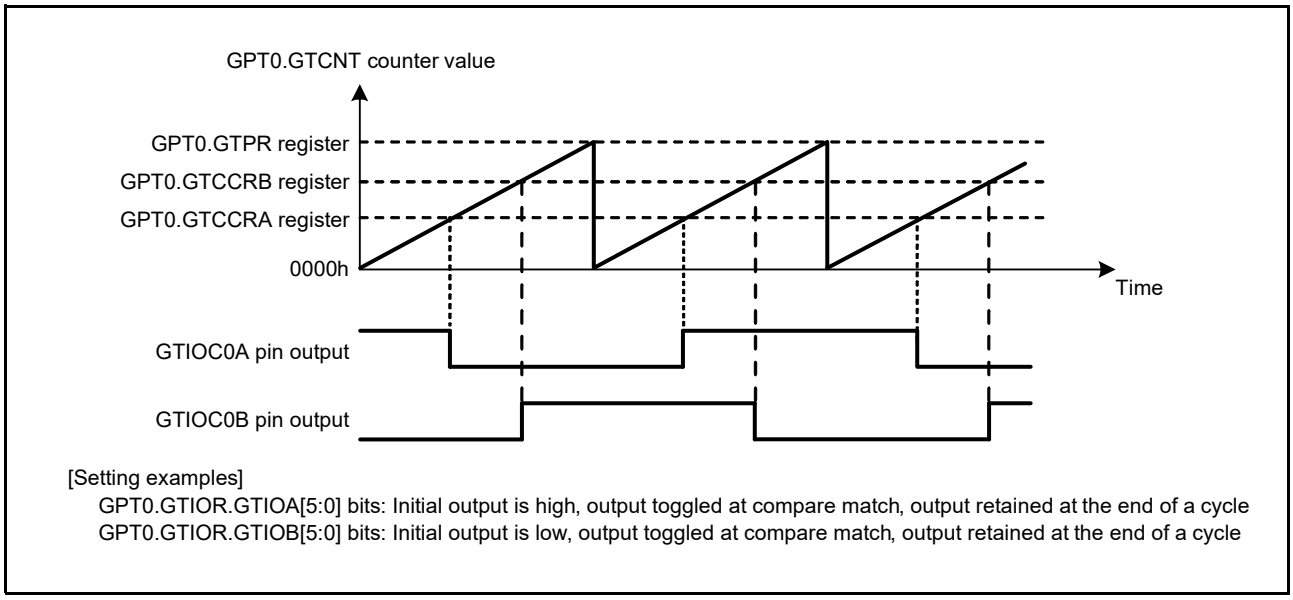


Figure 22.9 Example of Toggled Output Operation (1)

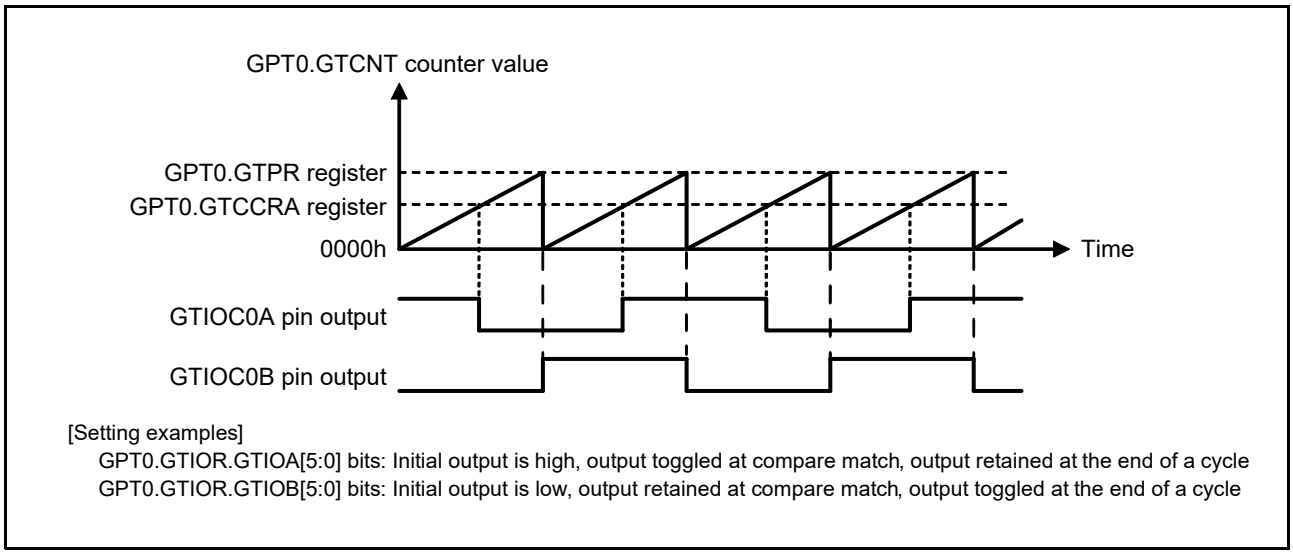


Figure 22.10 Example of Toggled Output Operation (2)

Figure 22.11 shows an example for setting toggled output operation.

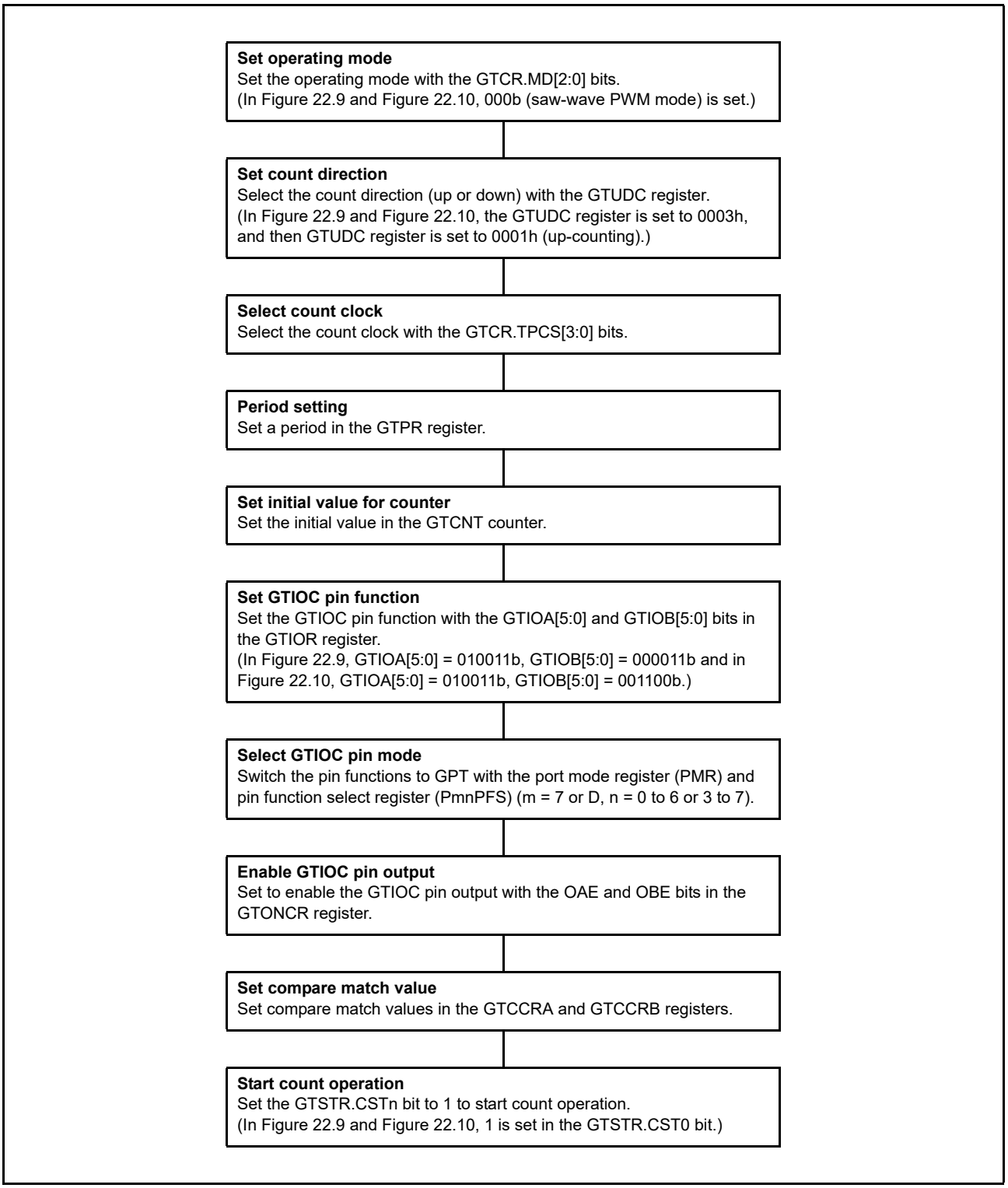


Figure 22.11 Example for Setting Toggled Output Operation

22.3.1.3 Input Capture Function

The GPTn.GTCNT(LW) counter value can be transferred to either GPTn.GTCCRA(LW) or GPTn.GTCCRB(LW) on detection of the input edge of the GTIOCnA input pin or GTIOCnB input pin, respectively (n = 0 to 3). The rising edge, falling edge, or both edges can be selected as the detection edge.

Figure 22.12 shows an example of the input capture function. In this example, the GPT0.GTCNT counter performs up-counting, and settings have been made so that an input capture is performed at both edges of the GTIOC0A input pin and at the rising edge of the GTIOC0B input pin.

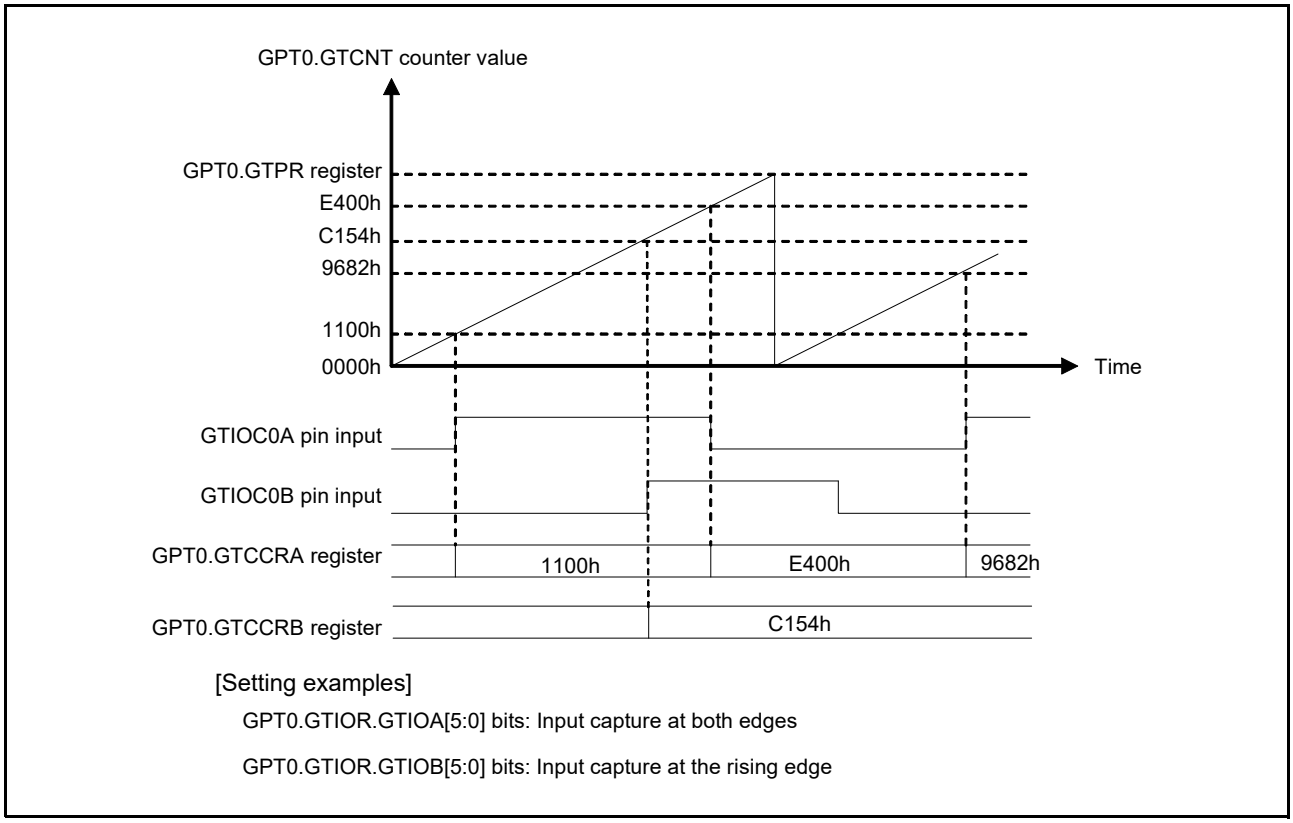


Figure 22.12 Example of Input Capture Operation

Figure 22.13 shows an example for setting input capture operation.

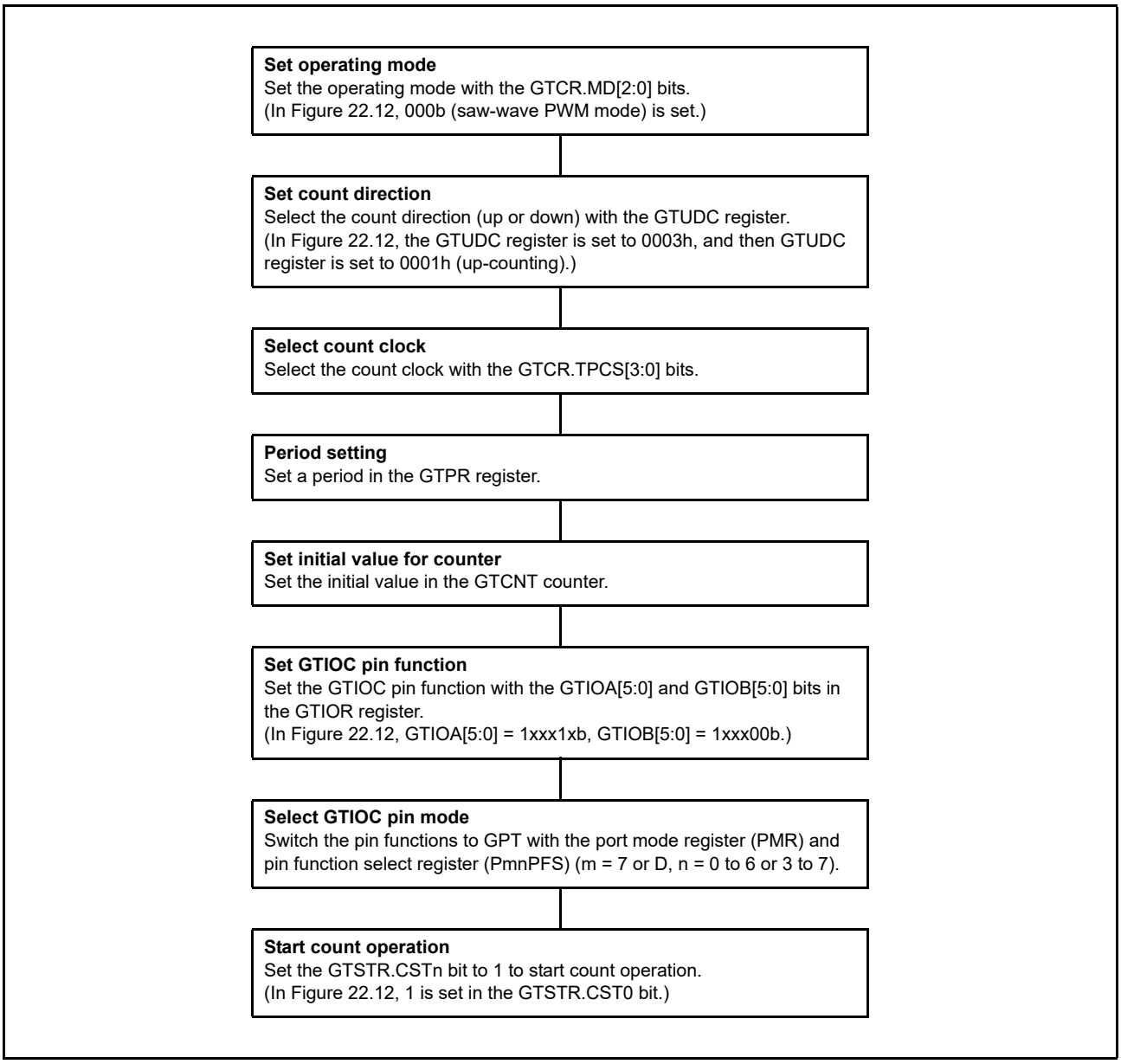


Figure 22.13 Example for Setting Input Capture Operation

22.3.2 Buffer Operation

The following buffer operation can be set with the GTBER register.

- Buffer operation with the GTPR(LW), GTPBR(LW), and GTPDBR(LW) registers used together
- Buffer operation with the GTCCRA(LW), GTCCRC(LW), and GTCCRD(LW) registers used together
- Buffer operation with the GTCCRB(LW), GTCCRE(LW), and GTCCRF(LW) registers used together
- Buffer operation with the GTADTRA(LW), GTADTBRA(LW), and GTADTDBRA(LW) registers used together
- Buffer operation with the GTADTRB(LW), GTADTBRB(LW), and GTADTDBRB(LW) registers used together

The following buffer operation can be set with the GTDTCR register.

- Buffer operation with the GTDVU(LW) and GTDBU(LW) registers used together
- Buffer operation with the GTDVD(LW) and GTDBD(LW) registers used together

22.3.2.1 GTPR Register Buffer Operation

The GTPBR(LW) register can function as a buffer register for the GTPR(LW) register, and the GTPDBR(LW) register can function as a buffer register for the GTPBR(LW) register (double buffer register for the GTPR(LW) register).
The buffer transfer is performed at an overflow (in up-counting), underflow (in down-counting), or counter clearing by hardware source, software source, or synchronous clearing in saw-wave mode, and at a trough in triangle-wave mode.
To set the GTPR(LW) register to function as double buffer, set the GTBER.PR[1:0] bits to 10b or 11b. For single buffer operation, set 01b. Not to function as buffer, set 00b.
Figure 22.14 to Figure 22.16 show examples of GTPR buffer operation and Figure 22.17 shows an example for setting GTPR buffer operation.

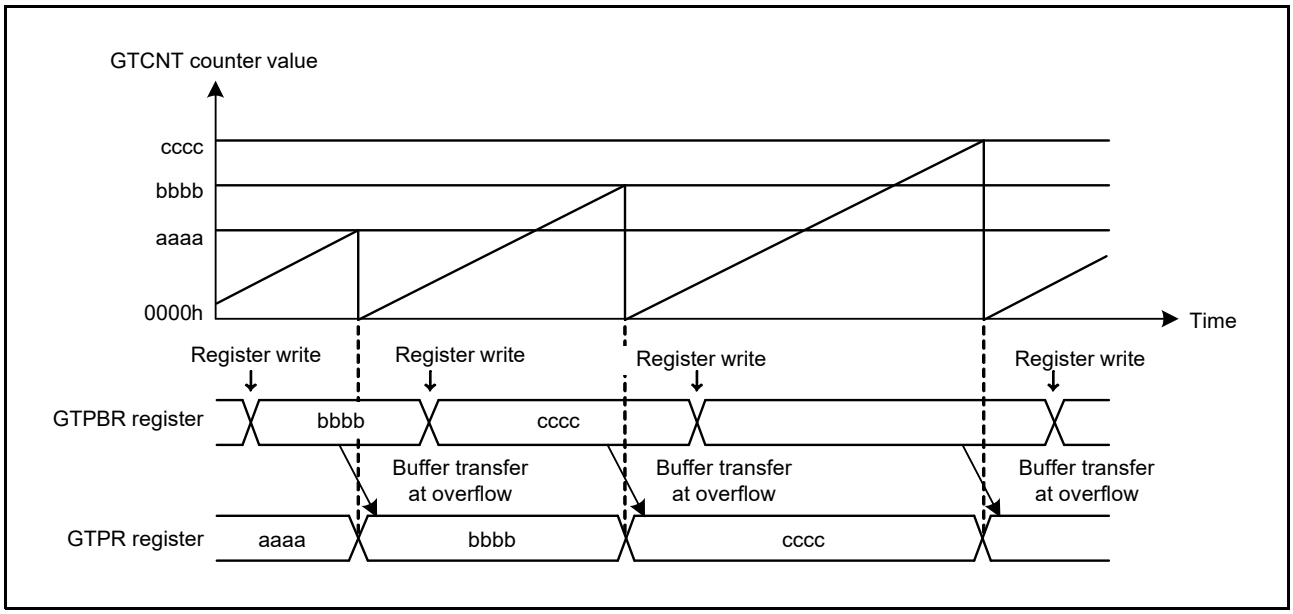


Figure 22.14 Example of GTPR Buffer Operation (Saw Waves in Up-Counting)

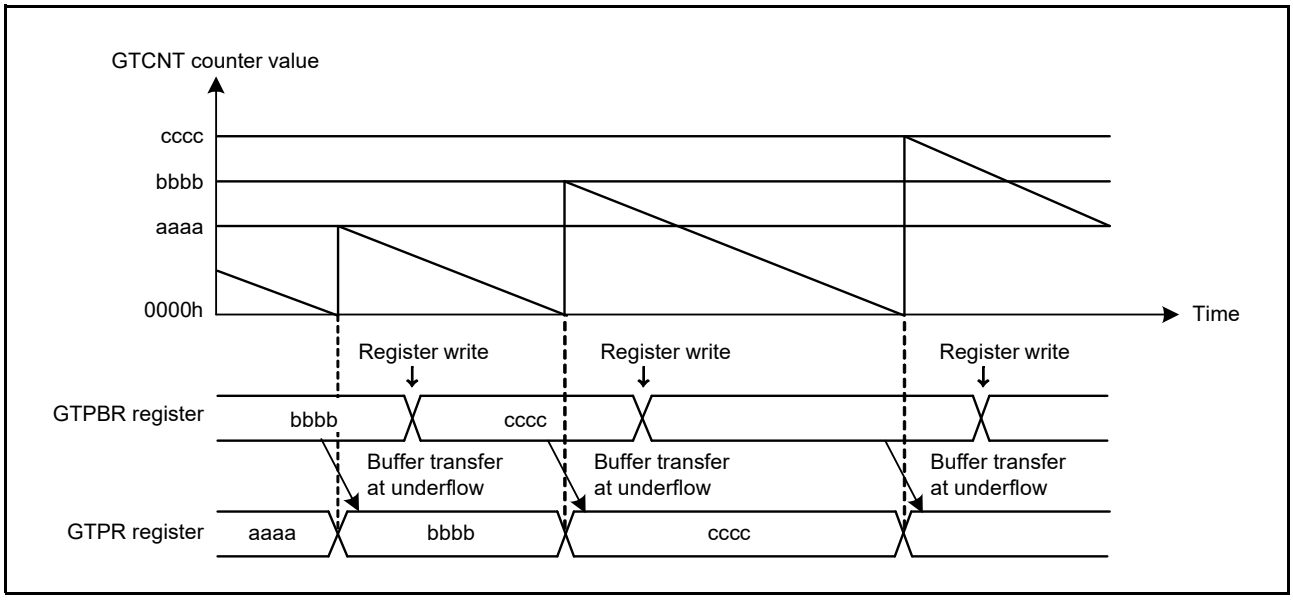


Figure 22.15 Example of GTPR Buffer Operation (Saw Waves in Down-Counting)

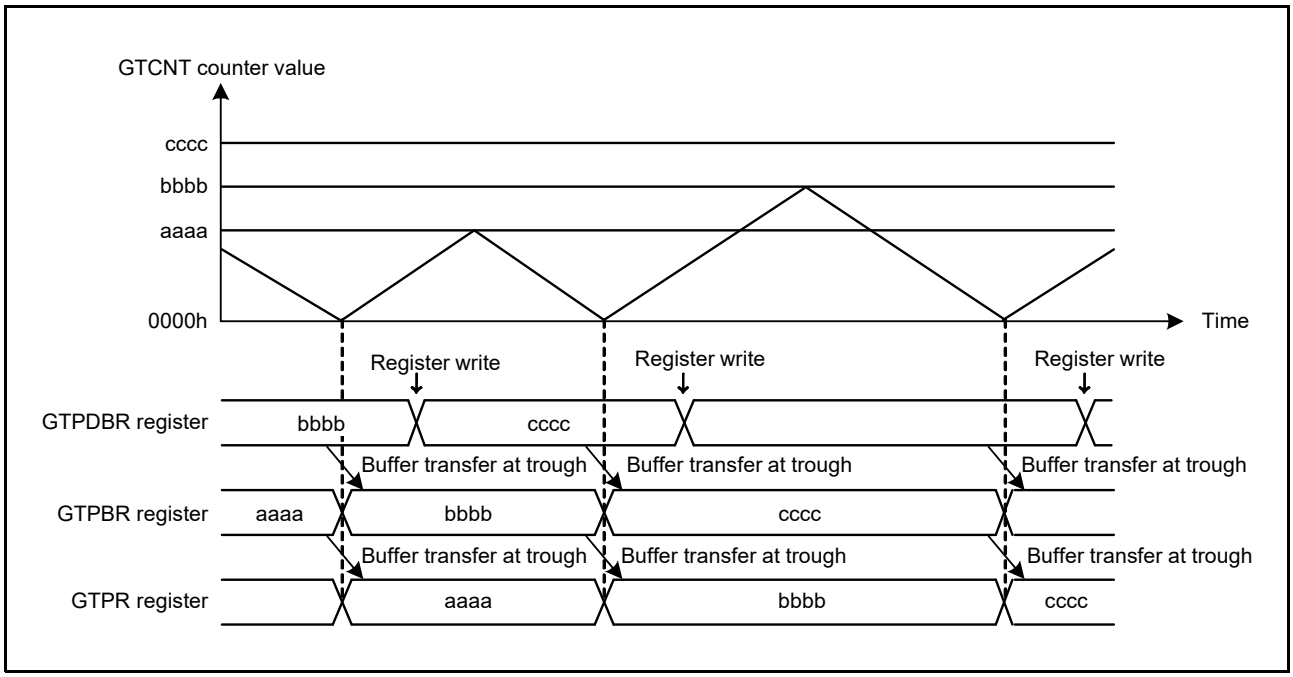


Figure 22.16 Example of GTPR Double Buffer Operation (Triangle Waves)

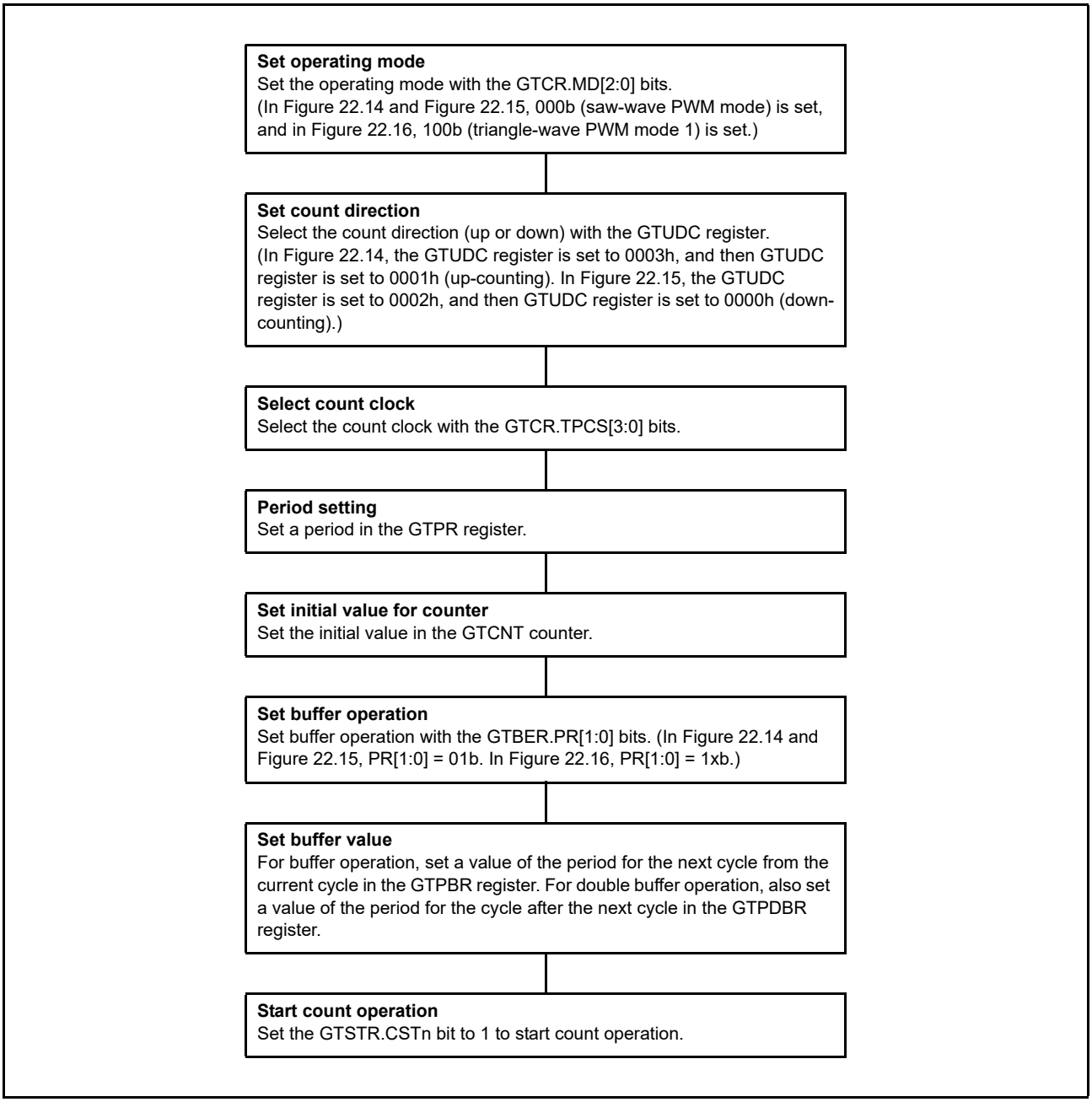


Figure 22.17 Example for Setting GTPR Buffer Operation

22.3.2.2 Buffer Operation for the GTCCRA(LW) and GTCCRB(LW) Registers

The GTCCRC(LW) register can function as the GTCCRA(LW) buffer register and the GTCCRD(LW) register can function as the GTCCRC(LW) buffer register (double buffer register for the GTCCRA(LW) register). Similarly, the GTCCRE(LW) register can function as the GTCCRB(LW) buffer register and the GTCCRF(LW) register can function as the GTCCRE(LW) buffer register (double buffer register for the GTCCRB(LW) register).
To set the GTCCRA(LW) or GTCCRB(LW) register to function as a double buffer, set the GTBER.CCRA[1:0] or GTBER.CCRB[1:0] bits to 10b or 11b. For single buffer operation, set 01b. Not to function as buffer, set 00b.
The following describes buffer operation during output compare and input capture operation.

(1) When the GTCCRA(LW) or GTCCRB(LW) Register Functions as Output Compare Register

Buffer transfer is performed at an overflow (in up-counting), underflow (in down-counting), counter clearing in saw-wave mode, and at a crest or trough in triangle-wave mode. In both saw-wave mode and triangle-wave mode, buffer transfer of the GTCCRA(LW) and GTCCRB(LW) registers is forcibly performed by writing 1 to the GTBER.CCRSWT bit while counting is stopped.
In saw-wave one-shot pulse mode and triangle-wave PWM mode 3, buffer transfer from the GTCCRD(LW) register to temporary register A(LW) and the GTCCRF(LW) register to temporary register B(LW) is performed using the forcible buffer operation while counting is stopped.
Figure 22.18 to Figure 22.20 show examples of GTCCRA and GTCCRB buffer operation and Figure 22.21 shows an example for setting GTCCRA and GTCCRB buffer operation.

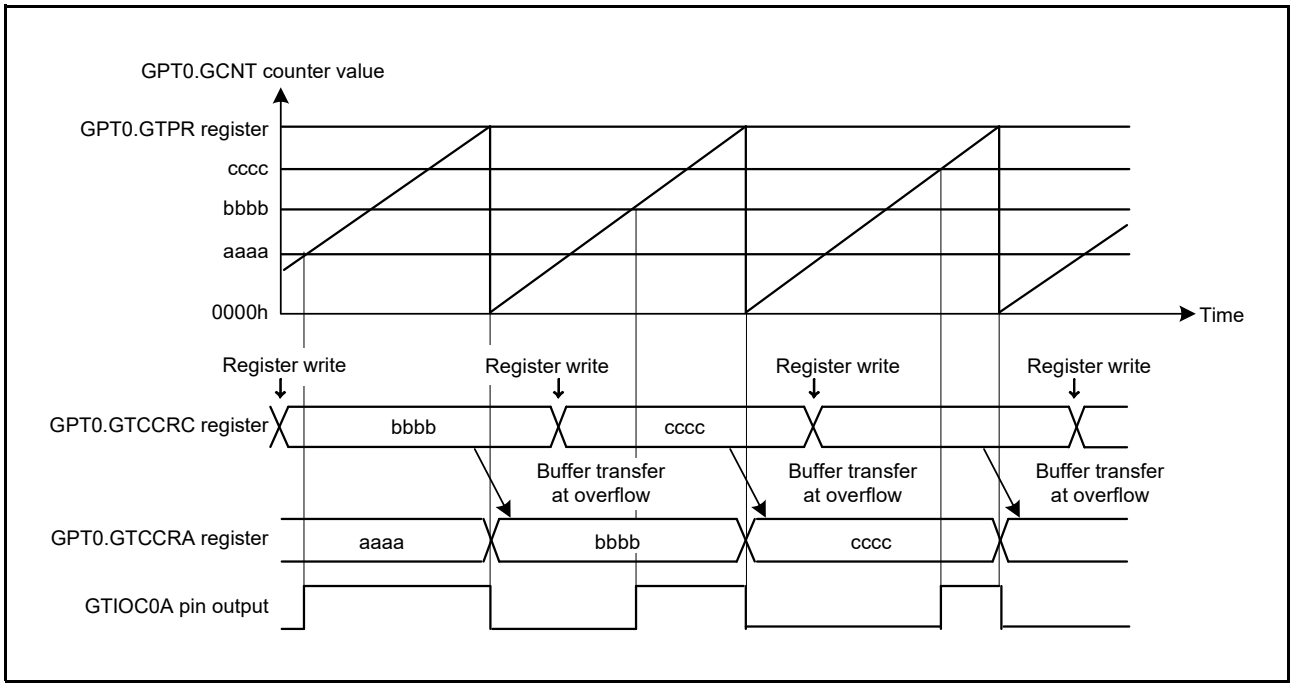


Figure 22.18 Example of GTCCRA and GTCCRB Buffer Operation (Output Compare, Saw Waves in Up-Counting, High Output at GTCCRA Compare Match, Low Output at the End of the Cycle)

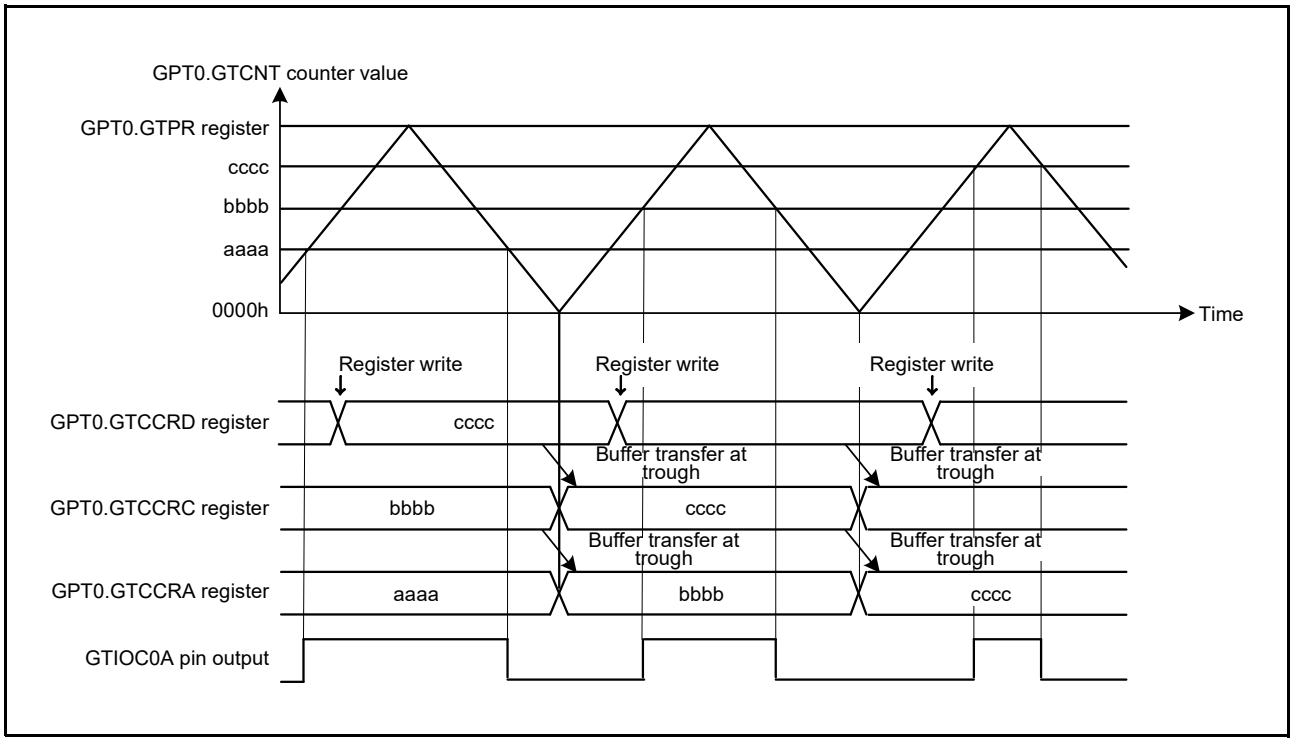


Figure 22.19 Example of GTCCRA and GTCCRB Double Buffer Operation (Output Compare, Triangle Waves, Buffer Operation at Trough, Output Toggled at GTCCRA Compare Match, Output Retained at the End of the Cycle)

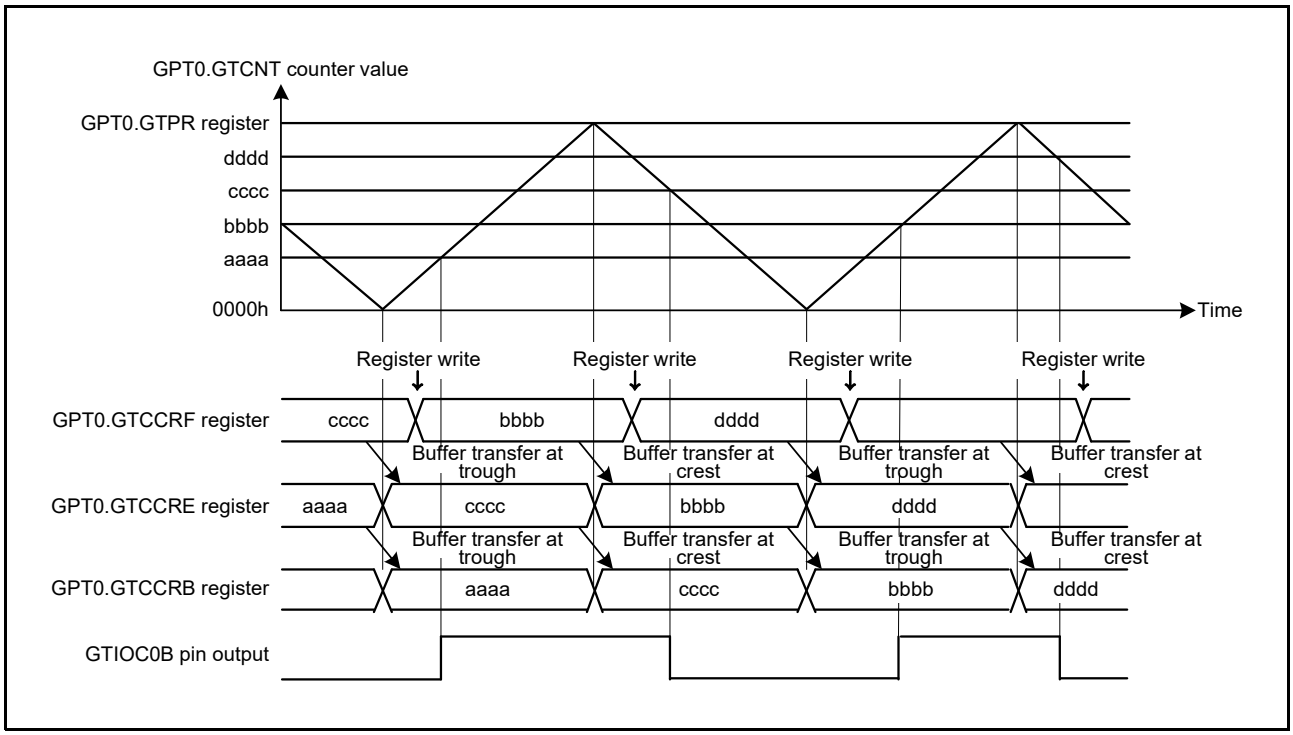


Figure 22.20 Example of GTCCRA and GTCCRB Double Buffer Operation (Output Compare, Triangle Waves, Buffer Operation at Both Troughs and Crests, Output Toggled at GTCCRB Compare Match, Output Retained at the End of the Cycle)

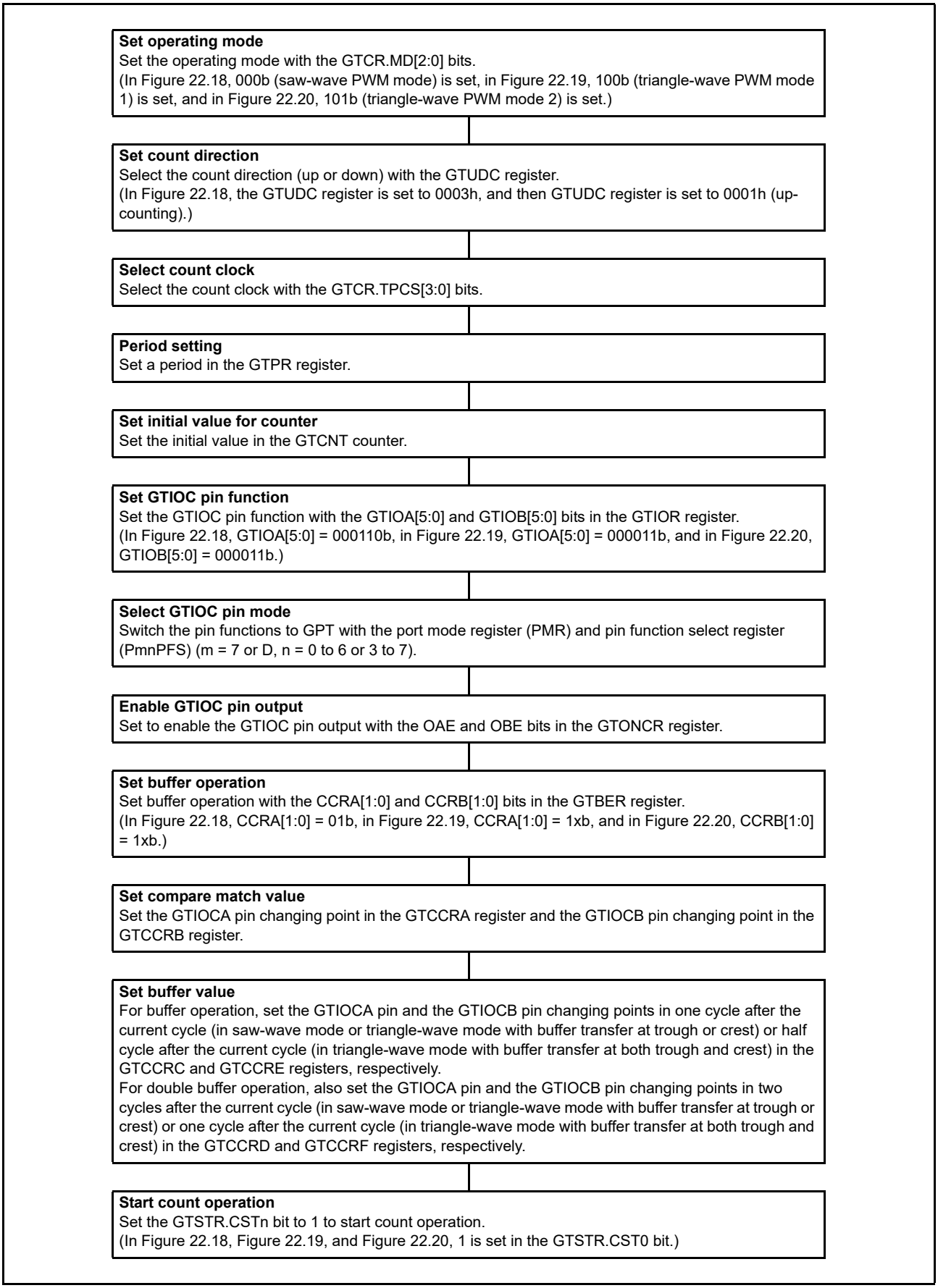


Figure 22.21 Example for Setting GTCCRA and GTCCRB Buffer Operation (for Output Compare)

(2) When the GTCCRA(LW) or GTCCRB(LW) Register Functions as Input Capture Register

When an input capture is generated, the GTCNT(LW) counter value is transferred to GTCCRA(LW) and GTCCRB(LW) and the stored GTCCRA(LW) and GTCCRB(LW) register values are transferred to buffer registers.
Figure 22.22 and Figure 22.23 show examples of GTCCRA and GTCCRB buffer operation and Figure 22.24 shows an example for setting GTCCRB buffer operation.

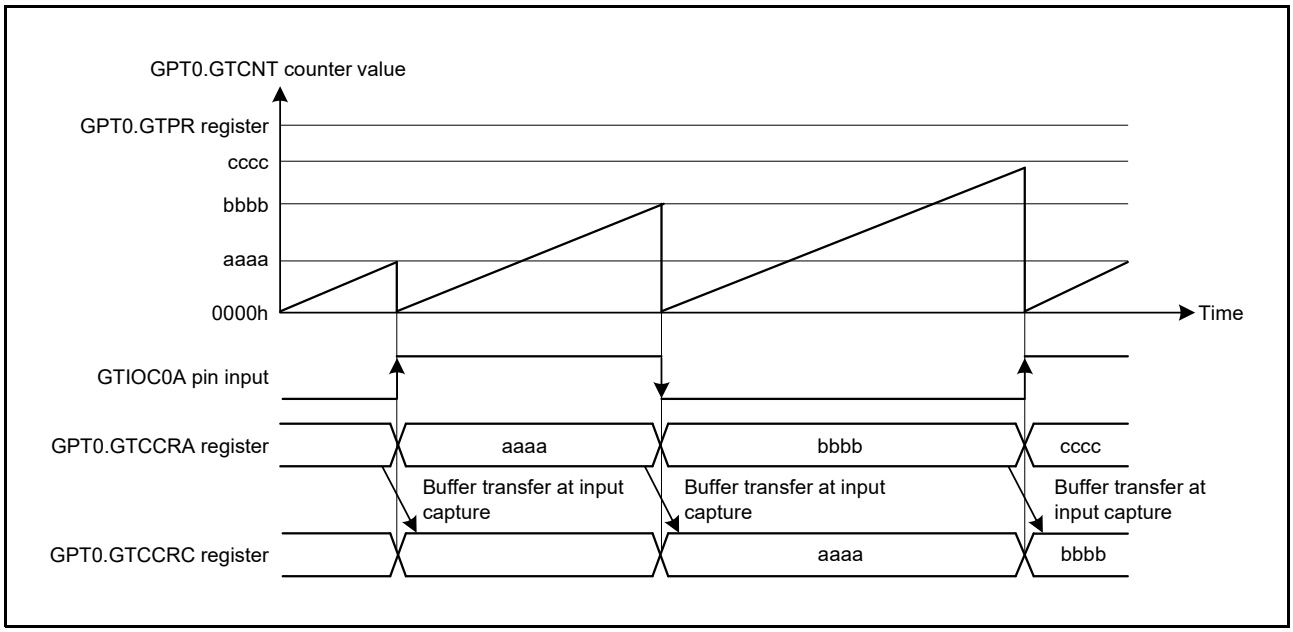


Figure 22.22 Example of GTCCRA and GTCCRB Buffer Operation (Input Capture at Both Edges of GTIOC0A Input, Saw Waves in Up-Counting, GTCNT Counter Cleared at GTCCRA Input Capture)

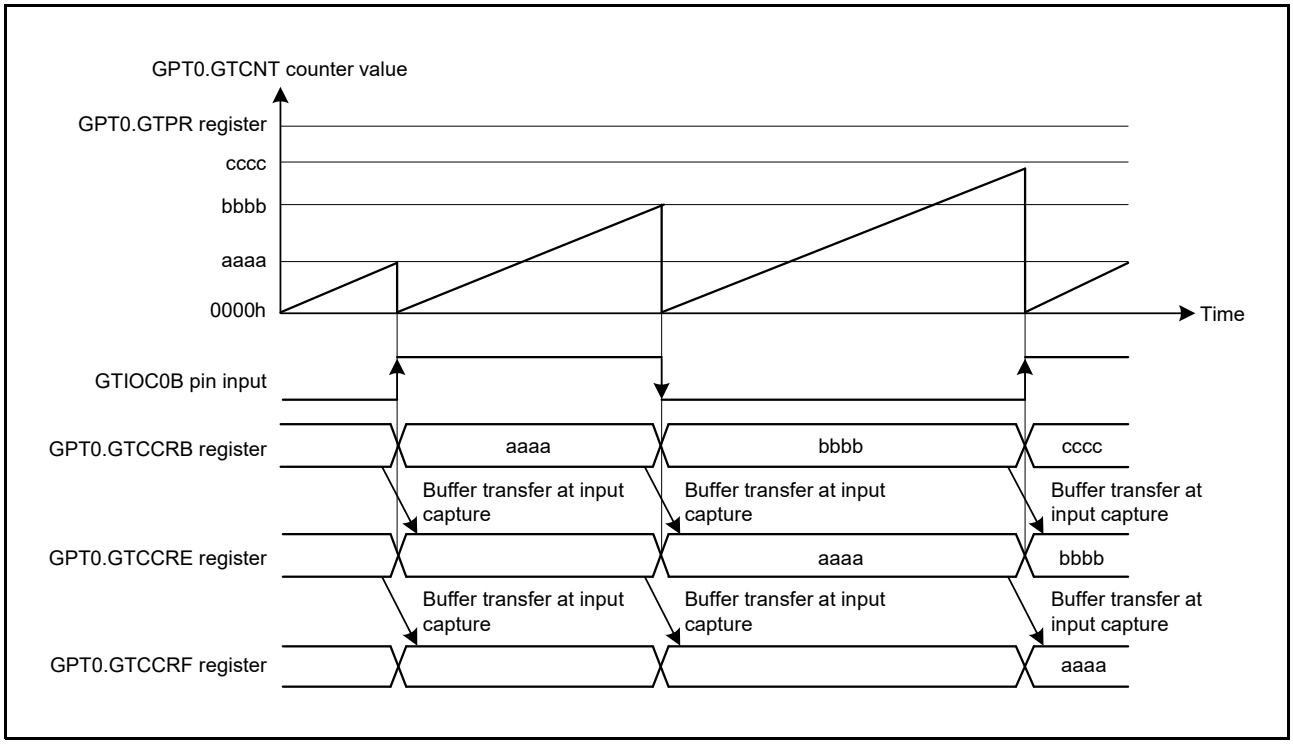


Figure 22.23 Example of GTCCRA and GTCCRB Double Buffer Operation (Input Capture at Both Edges of GTIOC0B Input, Saw Waves in Up-Counting, GTCNT Counter Cleared at GTCCRB Input Capture)

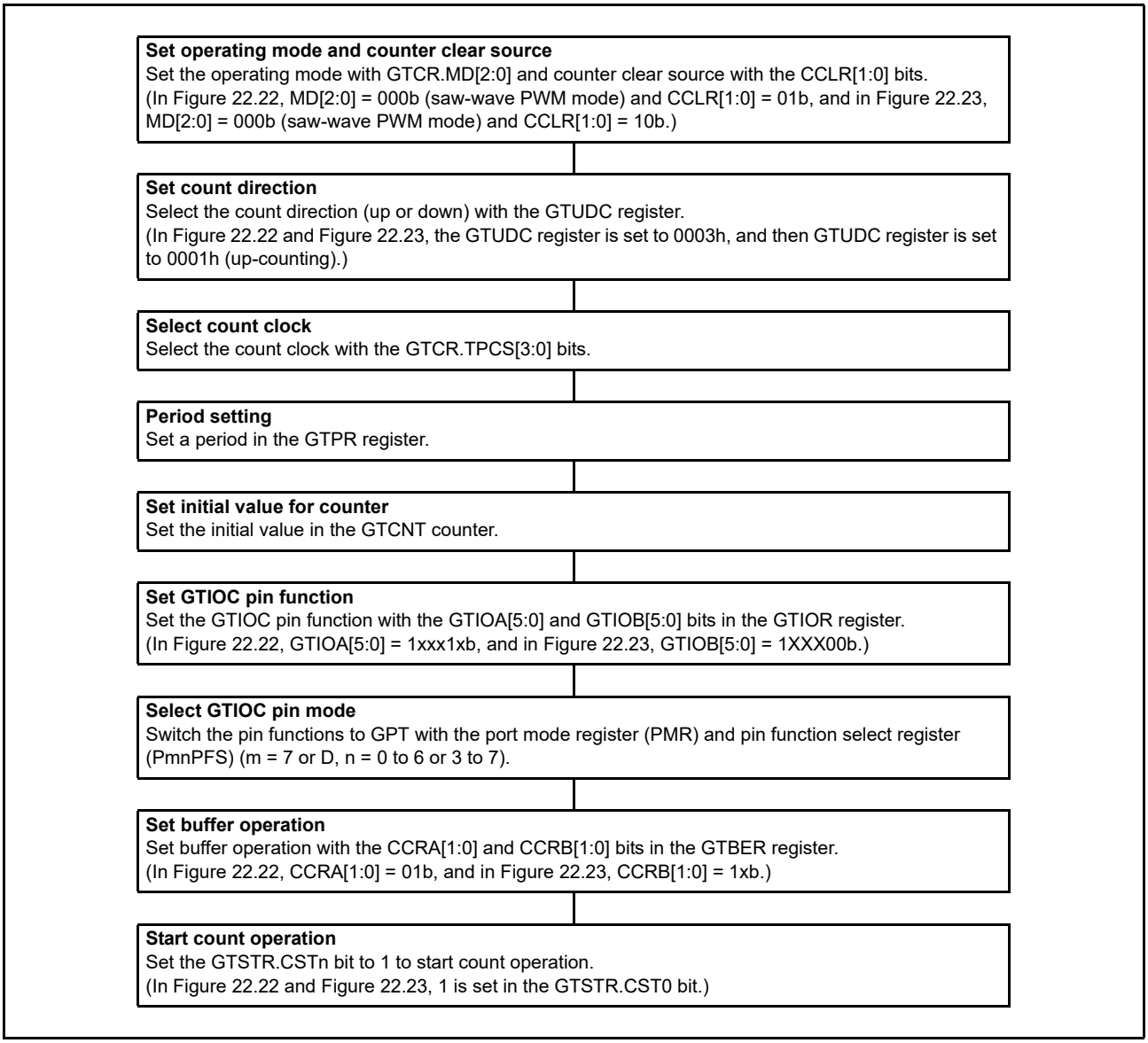


Figure 22.24 Example for Setting GTCCRA and GTCCRB Buffer Operation (for Input Capture)

22.3.2.3 Buffer Operation for the GTADTRA(LW) and GTADTRB(LW) Registers

The GTADTBRA(LW) register can function as the GTADTRA(LW) buffer register and the GTADTDBRA(LW) register can function as the GTADTBRA(LW) buffer register (double buffer register for the GTADTRA(LW) register). Similarly, the GTADTBRB(LW) register can function as the GTADTRB(LW) buffer register and the GTADTDBRB(LW) register can function as the GTADTBRB(LW) buffer register (double buffer register for the GTADTRB(LW) register).
To set the GTADTRA(LW) or GTADTRB(LW) register to function as a double buffer, set the GTBER.ADTDA or GTBER.ADTDB bit to 1. For single buffer operation, set 0. Not to function as buffer, set the GTBER.ADTTA[1:0] or GTBER.ADTTB[1:0] bits to 00b.
The buffer transfer timing can be set with the GTBER.ADTTn[1:0] bits. For saw waves, overflows (during up-counting), underflows (during down-counting), or counter clearing can be selected. For triangle waves, crests are selected when GTBER.ADTTn[1:0] = 01b, troughs are selected when GTBER.ADTTn[1:0] = 10b, and both crests and troughs are selected when GTBER.ADTTn[1:0] = 11b (n =A, B).
Figure 22.25 to Figure 22.27 show examples of GTADTRA and GTADTRB buffer operation and Figure 22.28 shows an example for setting GTDTRA and GTADTRB buffer operation.

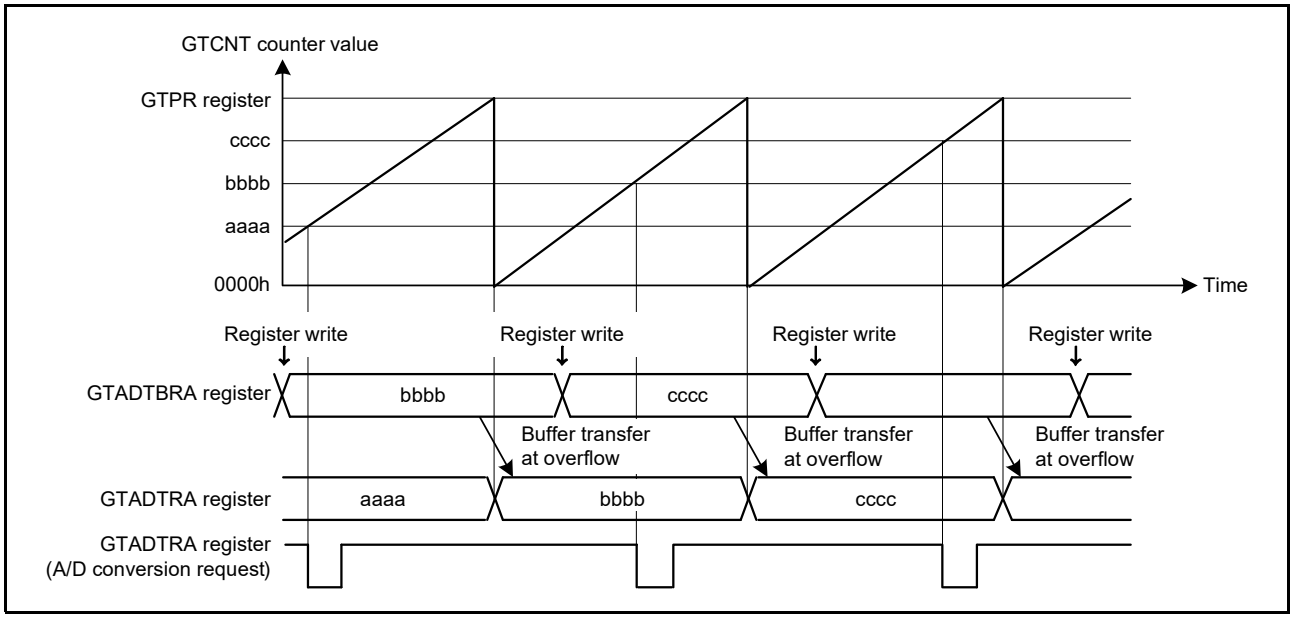


Figure 22.25 Example of GTADTRA and GTADTRB Buffer Operation (Saw Waves in Up-Counting, A/D Converter Start Request Generated by Up-Counting)

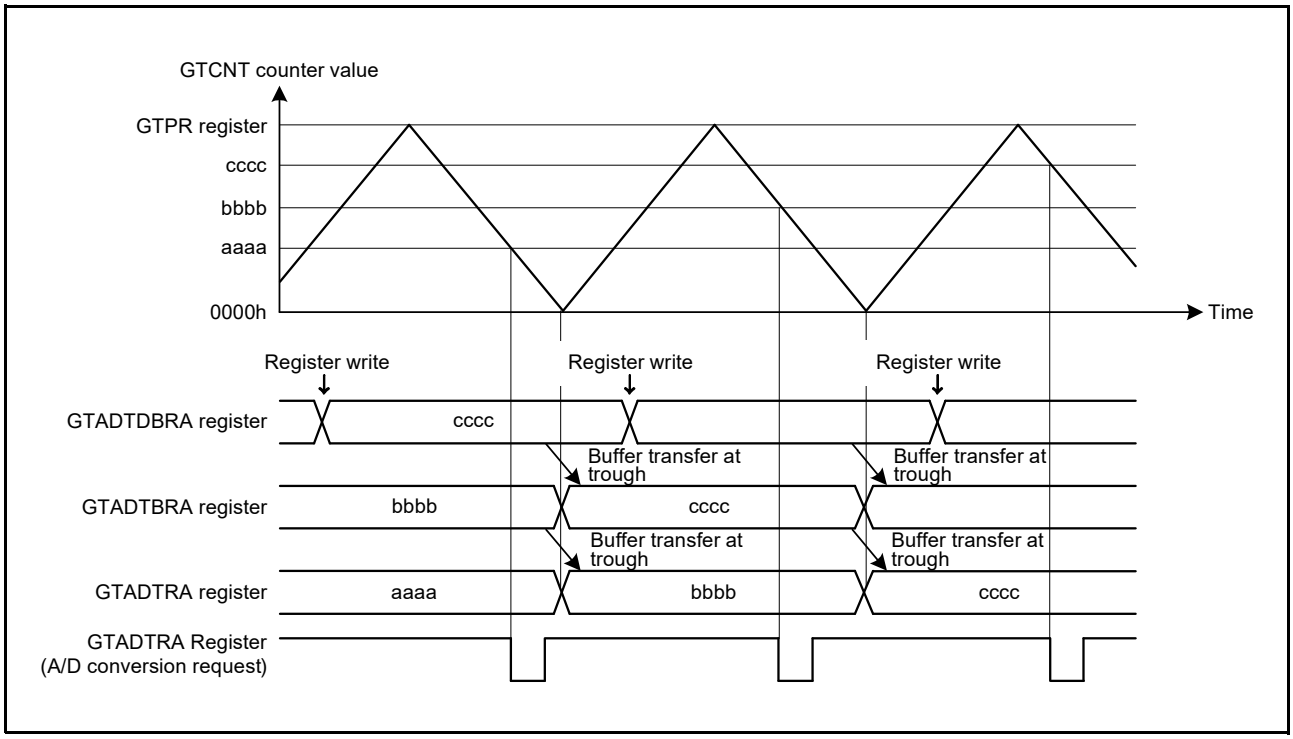


Figure 22.26 Example of GTADTRA and GTADTRB Double Buffer Operation (Triangle Waves, Buffer Transfer at Troughs, A/D Converter Start Request Generated by Down-Counting)

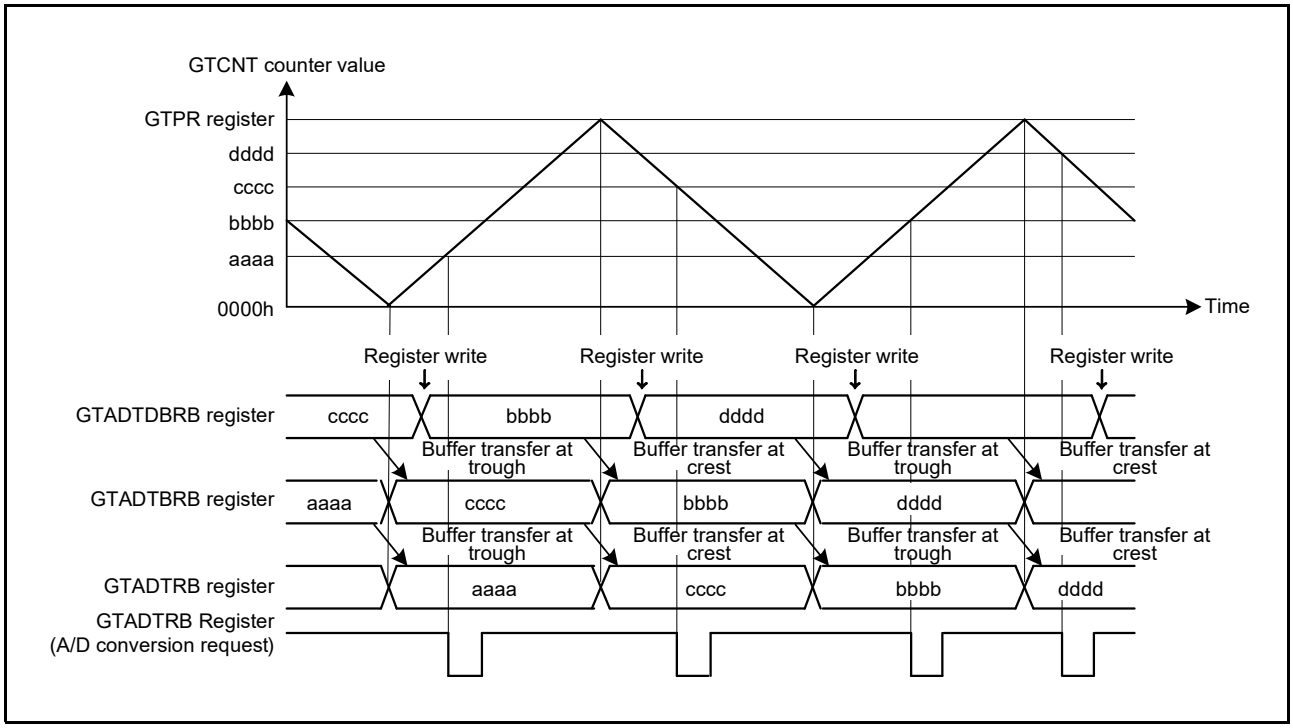


Figure 22.27 Example of GTADTRA and GTADTRB Double Buffer Operation (Triangle Waves, Buffer Transfer at Both Troughs and Crests, A/D Converter Start Request Generated by Both Up- and Down-Counting)

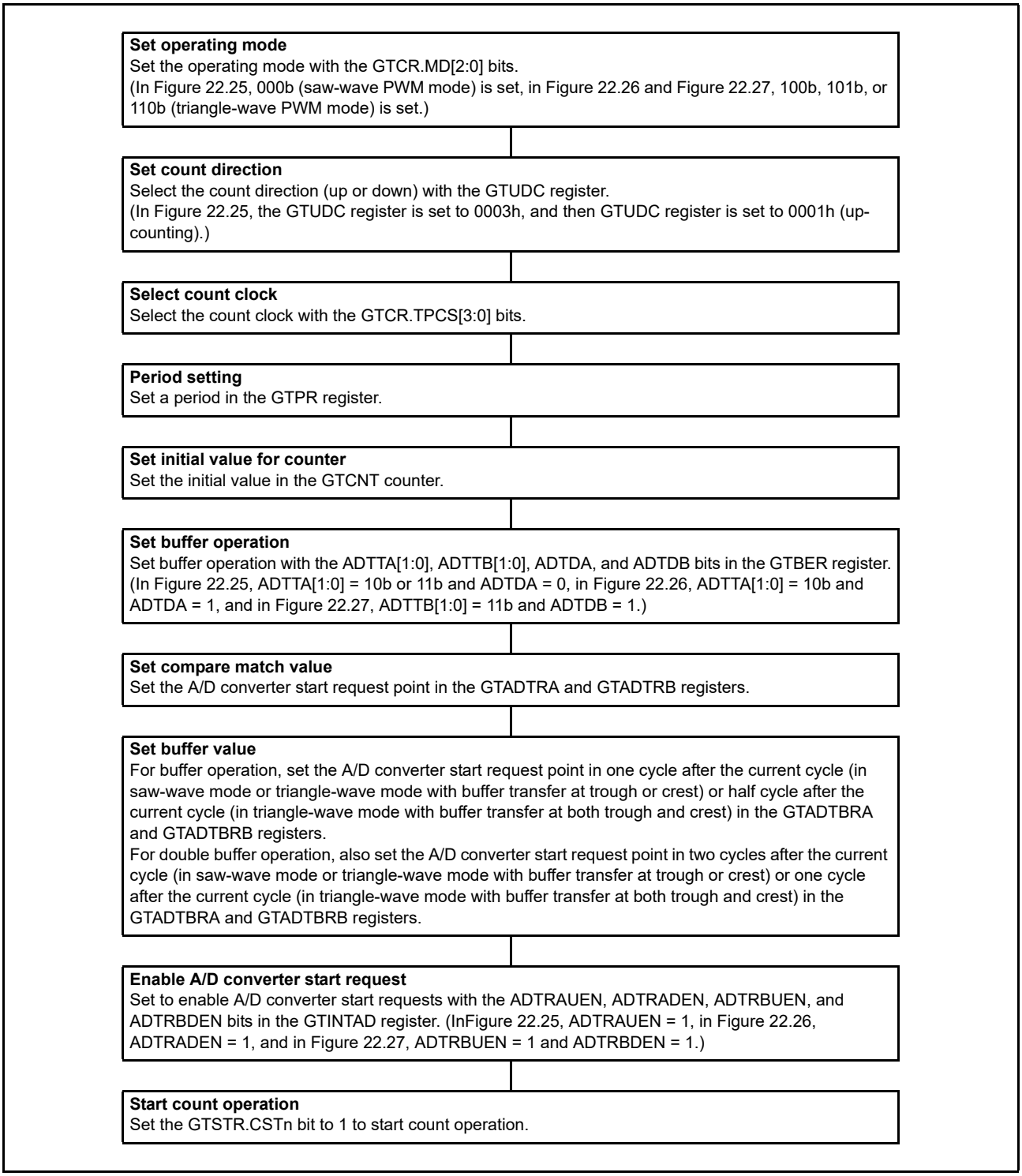


Figure 22.28 Example for Setting GTADTRA and GTADTRB Buffer Operation

22.3.3 PWM Output Operating Mode

The GPT can output PWM waveforms to the GTIOCnA pin or GTIOCnB pin by a compare match between the GPTn.GTCNT(LW) counter and the GPTn.GTCCRA(LW) or GPTn.GTCCRB(LW) register (n = 0 to 3). An operating mode can be set independently for each channel, and synchronous operation on channels is also possible.
By setting the GTDTCR, GTDVU(LW), and GTDVD(LW) registers, the compare match value for a negative-phase waveform with dead time can automatically be set to the GTCCRB(LW) register.

(1) Saw-Wave PWM Mode (GTCR.MD = 000b)

In saw-wave PWM mode, the GPTn.GTCNT(LW) counter performs saw-wave (half-wave) operation by setting the period in the GTPR(LW) register and a PWM waveform is output to the GTIOCnA or GTIOCnB pin when a GPTn.GTCCRA(LW) or GPTn.GTCCRB(LW) compare match occurs (n = 0 to 3). The pin output value can be selected from low output, high output, or toggle output separately for a compare match and for the end of the cycle according to the GTIOR setting
Figure 22.29 shows an example of saw-wave PWM mode operation, and Figure 22.30 shows an example for setting saw-wave PWM mode.

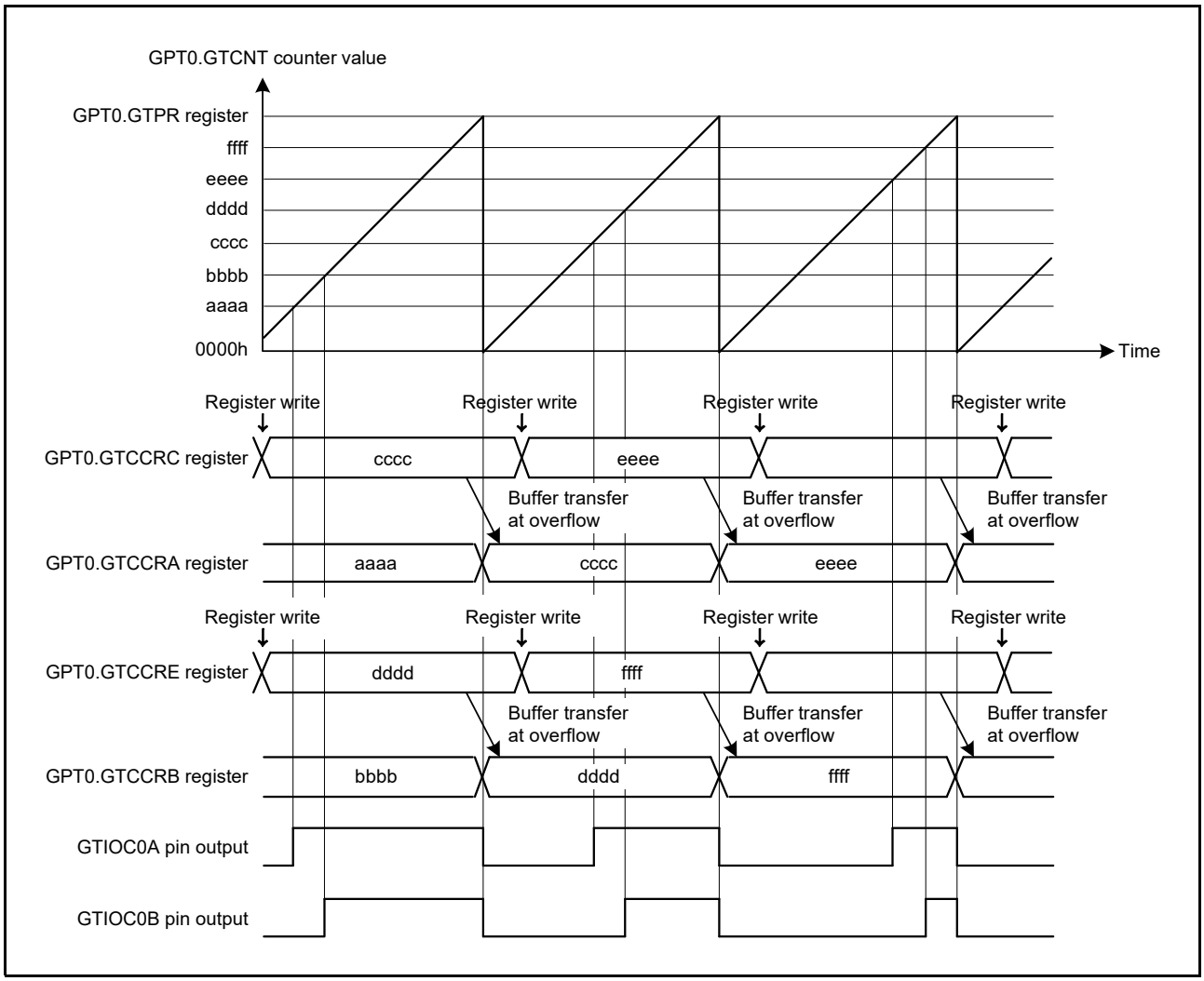


Figure 22.29 Example of Saw-Wave PWM Mode Operation (Up-Counting, Buffer Operation, High Output at GTCCRA/GTCCRB Compare Match, Low Output at the End of the Cycle)

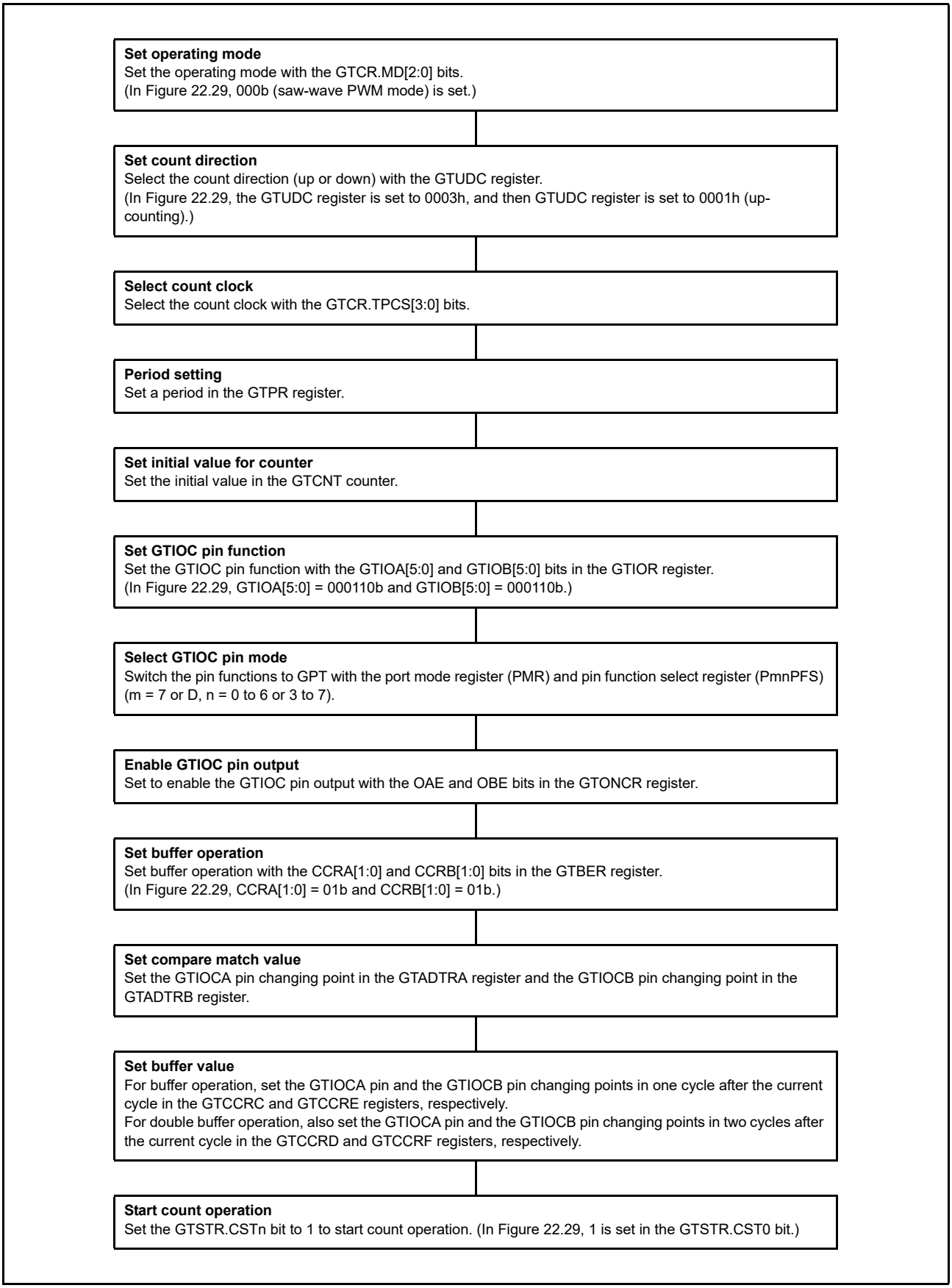


Figure 22.30 Example for Setting Saw-Wave PWM Mode

(2) Saw-Wave One-Shot Pulse Mode

The saw-wave one-shot pulse mode is a mode in which the period is set in the GPTn.GTPR(LW) register, the GPTn.GTCNT(LW) counter performs saw-wave (half-wave) operation and a PWM waveform is output to the GTIOCnA or GTIOCnB pin at a compare match of the GPTn.GTCCRA(LW) or GPTn.GTCCRB(LW) register with buffer operation fixed (n = 0 to 3).

Buffer operation in saw-wave one-shot pulse mode is different from the usual buffer operation. Buffer transfer is performed from GTCCRC(LW) to GTCCRA(LW), from GTCCRE(LW) to GTCCRB(LW), from GTCCRD(LW) to temporary register A(LW), and from GTCCRF(LW) to temporary register B(LW) at the end of the cycle, and from temporary register A(LW) to GTCCRA(LW) at a GTCCRA(LW) compare match and from temporary register B(LW) to GTCCRB(LW) at a GTCCRB(LW) compare match. The pin output value can be selected from low output, high output, or toggle output separately for a compare match and the end of the cycle according to the GTIOR setting.

By setting GTDTCR, GTDVU(LW), and GTDVD(LW), a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB(LW).

Figure 22.31 shows an example of saw-wave one-shot pulse mode operation, and Figure 22.32 shows an example for setting saw-wave one-shot pulse mode.

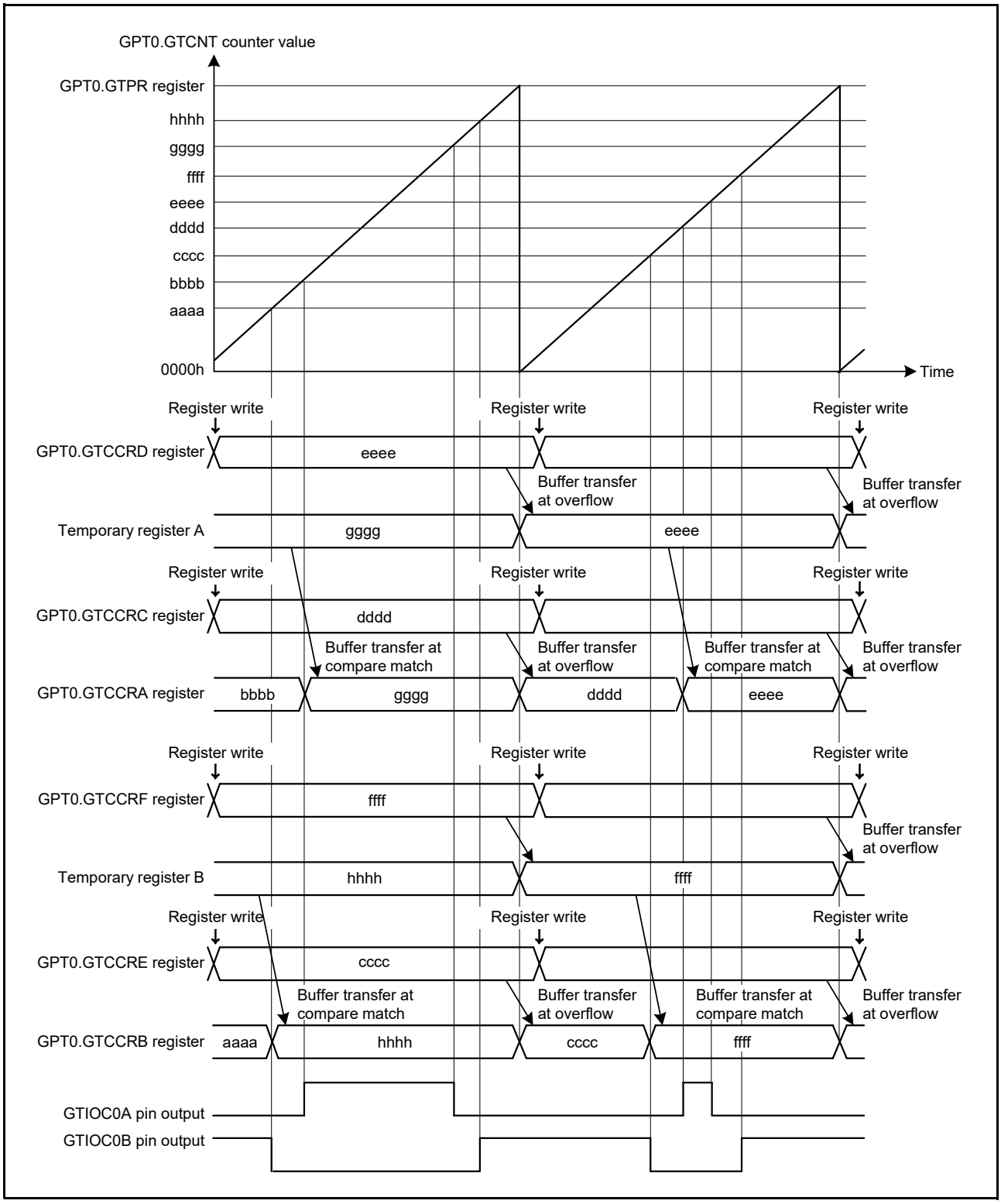


Figure 22.31 Example of Saw-Wave One-Shot Pulse Mode Operation (Up-Counting, Low Output from the GTIOC0A Pin and High Output from the GTIOC0B Pin at Initial Output, Output Toggled at GTCCRA/GTCCRB Compare Match, Output Retained at the End of the Cycle)

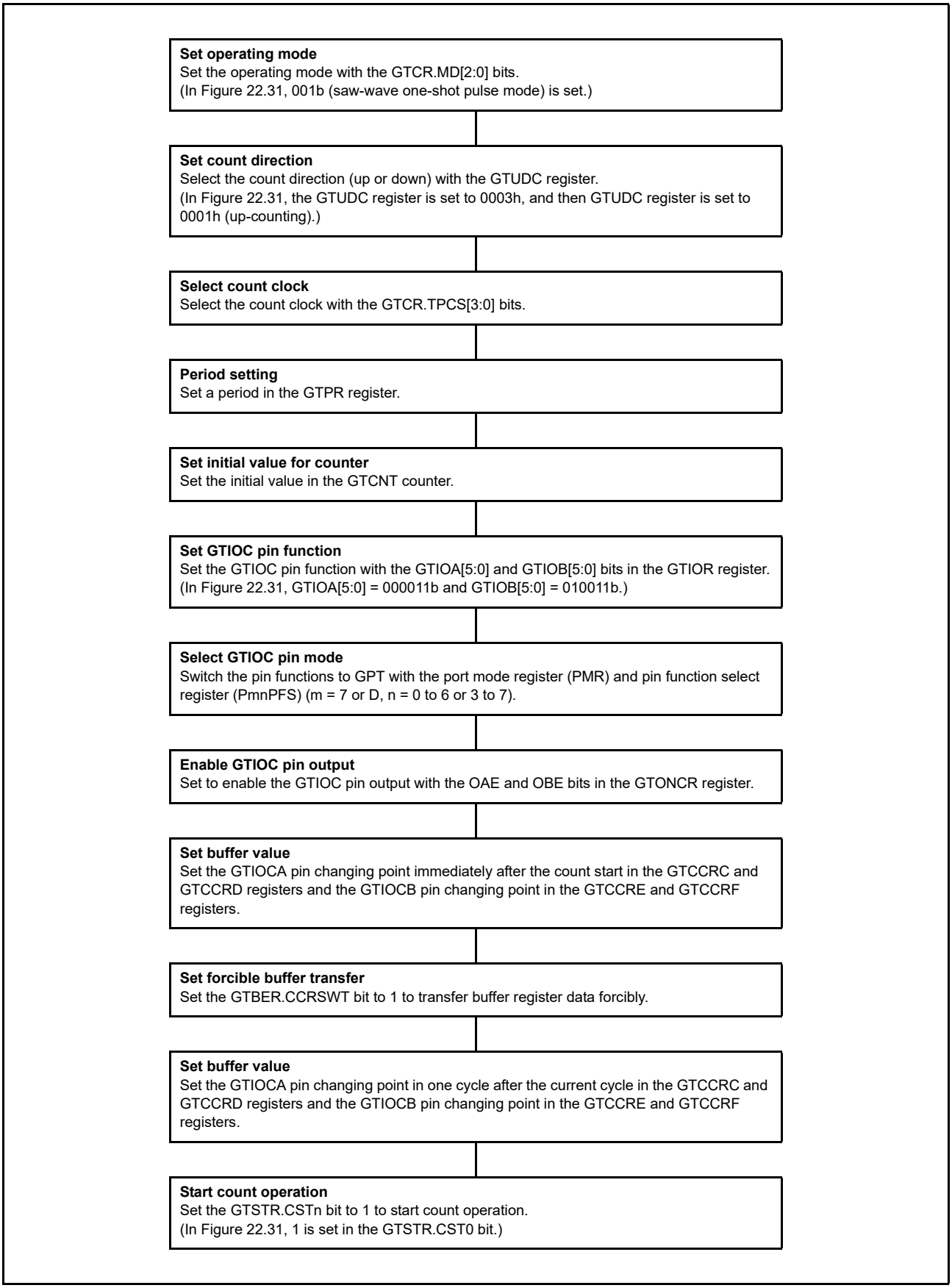


Figure 22.32 Example for Setting Saw-Wave One-Shot Pulse Mode

(3) Triangle-Wave PWM Mode 1 (16-Bit Transfer at Trough)

The triangle-wave PWM mode 1 is a mode in which the period is set in the GPTn.GTPR(LW) register, the GPTn.GTCNT(LW) counter performs triangle-wave (full-wave) operation, and a PWM waveform is output to the GTIOCnA or GTIOCnB pin when a GPTn.GTCCRA(LW) or GPTn.GTCCRB(LW) compare match occurs (n = 0 to 3). Buffer transfer is performed at the trough. The pin output value can be selected from low output, high output, or toggle output separately for a compare match and for the end of the cycle according to the GTIOR setting.
By setting the GTDTCR, GTDVU(LW), and GTDVD(LW) registers, a compare match value for a negative-phase waveform with dead time can automatically be set to the GTCCRB(LW) register.
Figure 22.33 shows an example of triangle-wave PWM mode 1 operation, and Figure 22.34 shows an example for setting triangle-wave PWM mode 1.

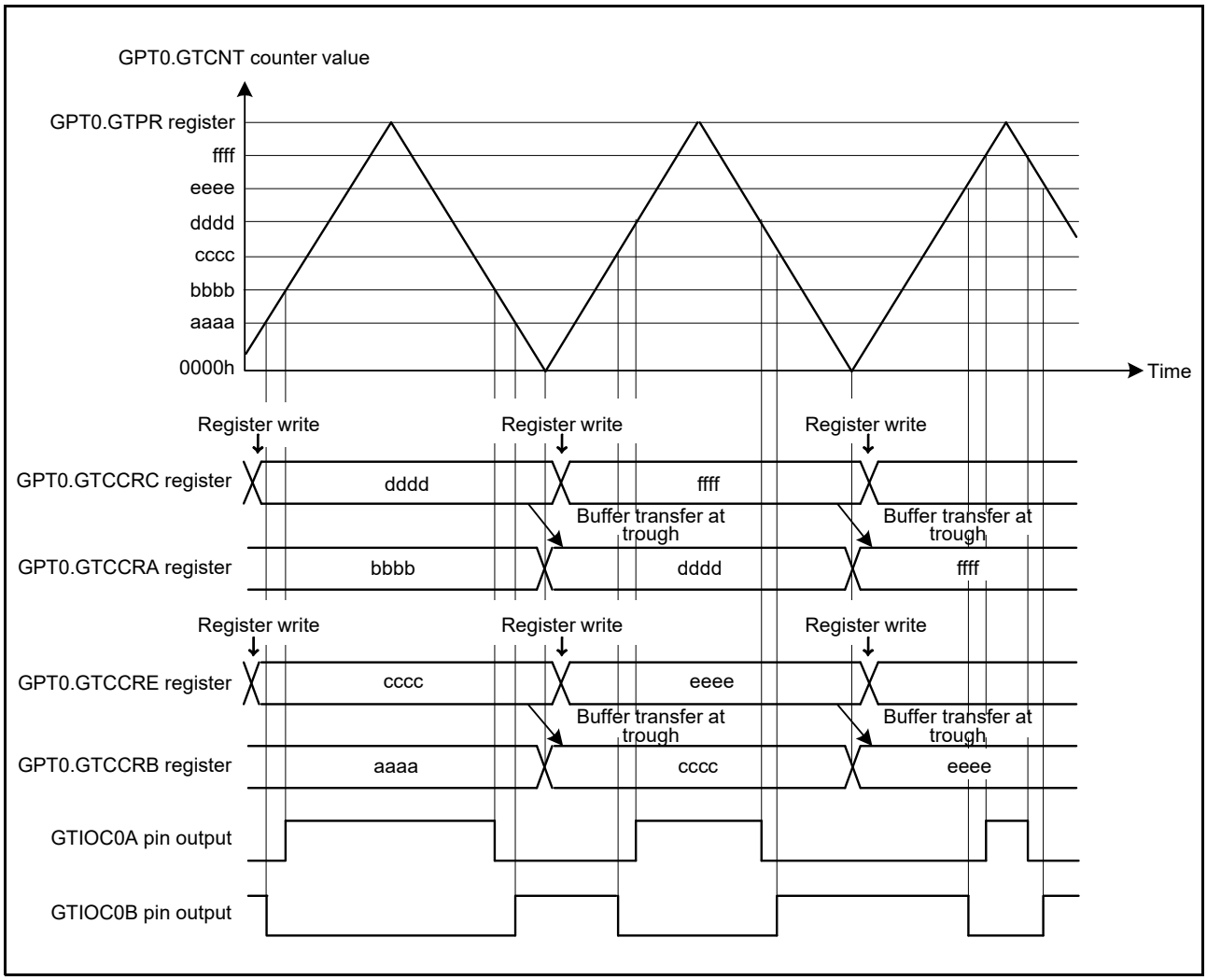


Figure 22.33 Example of Triangle-Wave PWM Mode 1 Operation (Buffer Operation, Low Output from the GTIOC0A Pin and High Output from the GTIOC0B Pin at Initial Output, Output Toggled at GTCCRA/GTCCRB Register Compare Match, Output Retained at the End of the Cycle)

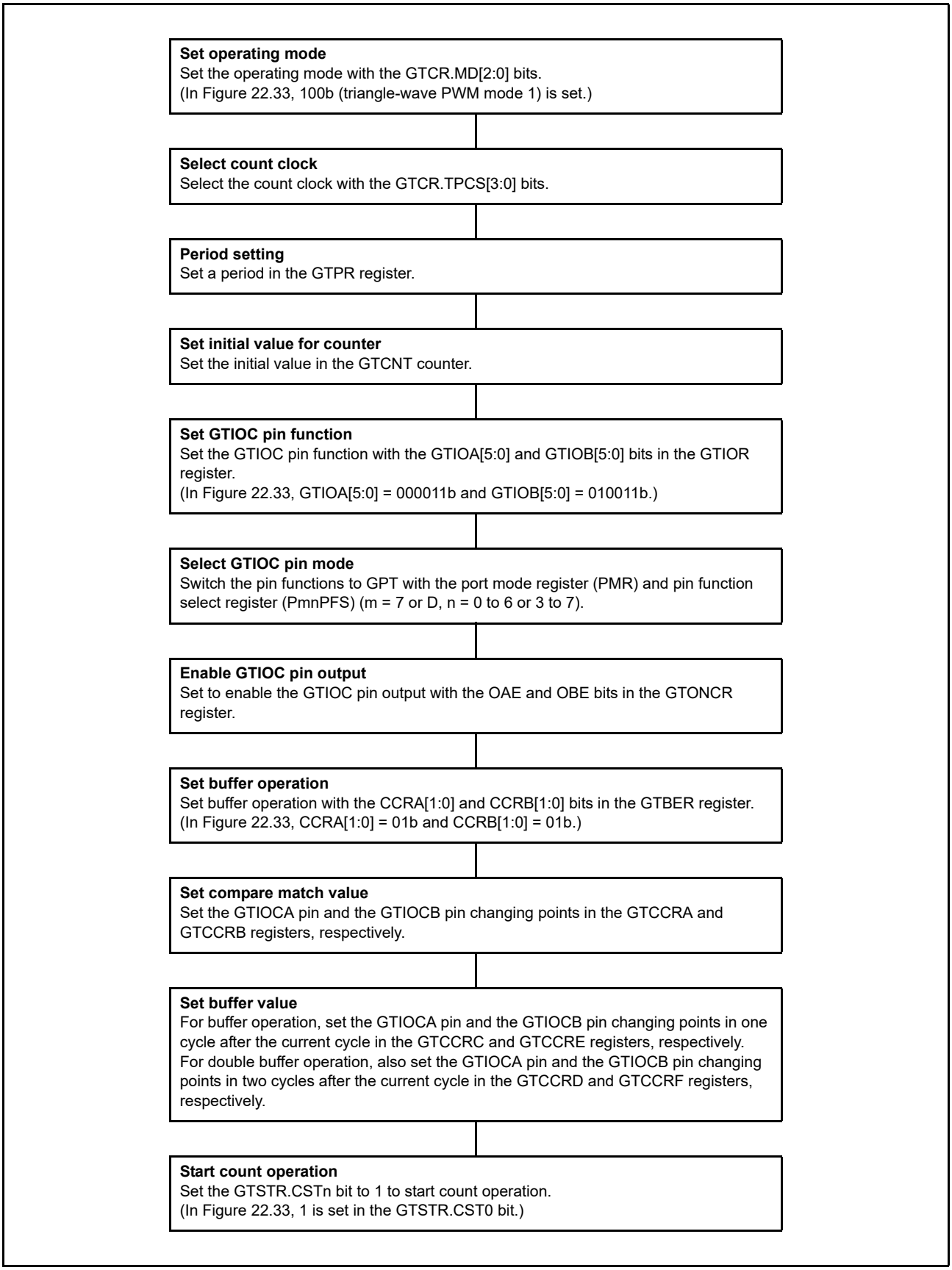


Figure 22.34 Example for Setting Triangle-Wave PWM Mode 1

(4) Triangle-Wave PWM Mode 2 (16-Bit Transfer at Crest and Trough)

Similarly to triangle-wave PWM mode 1, in triangle-wave PWM mode 2 the period is set in the GPTn.GTPR(LW) register, the GPTn.GTCNT(LW) counter performs triangle-wave (full-wave) operation, and a PWM waveform is output to the GTIOCnA or GTIOCnB pin when a GPTn.GTCCRA(LW) or GPTn.GTCCRB(LW) compare match occurs (n = 0 to 3). The buffer transfer is performed at both crests and troughs. The pin output value can be selected from low output, high output, or toggle output separately for a compare match and for the end of the cycle according to the GTIOR setting. By setting the GTDTCR, GTDVU(LW), and GTDVD(LW) registers, a compare match value for a negative-phase waveform with dead time can automatically be set to the GTCCRB(LW) register.

Figure 22.35 shows an example of triangle-wave PWM mode 2 operation, and Figure 22.36 shows an example for setting triangle-wave PWM mode 2.

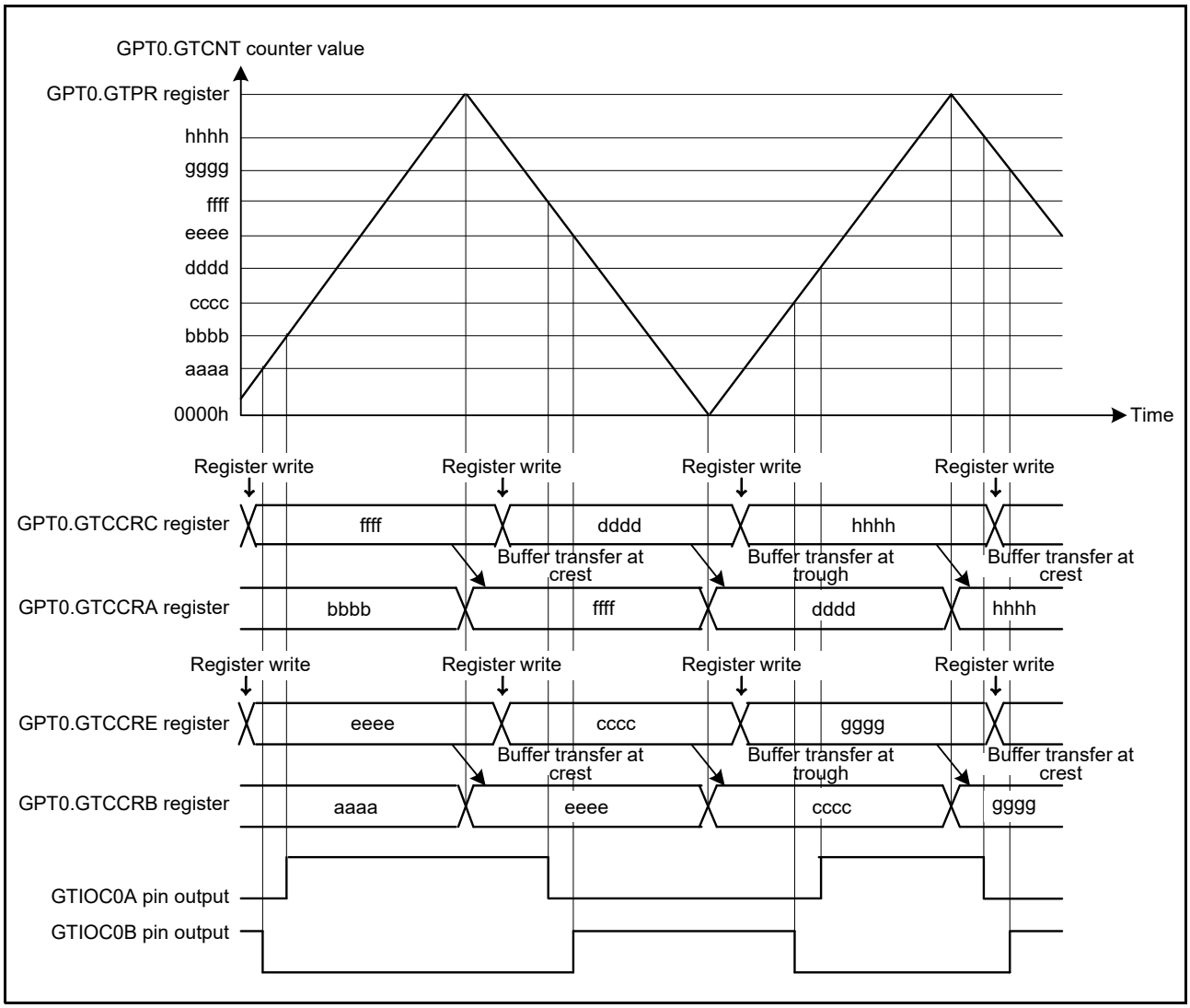


Figure 22.35 Example of Triangle-Wave PWM Mode 2 Operation (Buffer Operation, Low Output from the GTIOC0A Pin and High Output from the GTIOC0B Pin at Initial Output, Output Toggled at GTCCRA/GTCCRB Compare Match, Output Retained at the End of the Cycle)

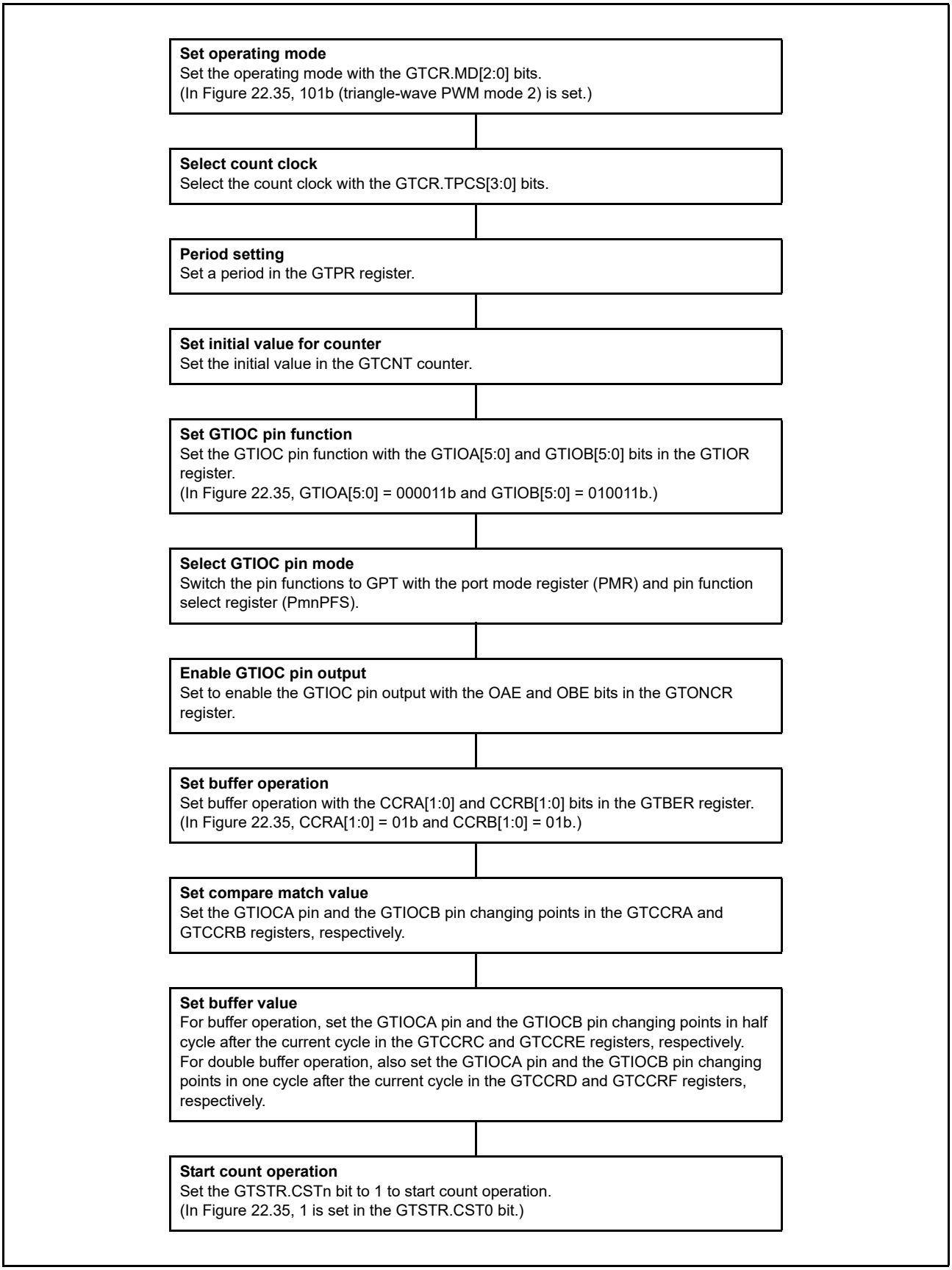


Figure 22.36 Example for Setting Triangle-Wave PWM Mode 2

(5) Triangle-Wave PWM Mode 3 (32-Bit Transfer at Trough)

The triangle-wave PWM mode 3 is a mode in which the period is set in the GPTn.GTPR(LW) register, the GPTn.GTCNT(LW) counter performs triangle-wave (full-wave) operation and a PWM waveform is output to the GTIOCnA or GTIOCnB pin at a compare match of the GPTn.GTCCRA(LW) or GPTn.GTCCRB(LW) register with buffer operation fixed (n = 0 to 3). Buffer operation in triangle-wave PWM mode 3 is different from the usual buffer operation. Buffer transfer is performed from the GTCCRC(LW) register to the GTCCRA(LW) register, from the GTCCRE(LW) register to the GTCCRB(LW) register, from the GTCCRD(LW) register to temporary register A(LW), and from the GTCCRF(LW) register to temporary register B(LW) at the trough, and from temporary register A(LW) to the GTCCRA(LW) register and from temporary register B(LW) to the GTCCRB(LW) register at the crest. The pin output value can be selected from low output, high output, or toggle output separately for a compare match and for the end of the cycle according to the GTIOR setting.

By setting the GTDTCR, GTDVU(LW), and GTDVD(LW) registers, a compare match value for a negative-phase waveform with dead time can automatically be set to the GTCCRB(LW) register.

Figure 22.37 shows an example of triangle-wave PWM mode 3 operation, and Figure 22.38 shows an example for setting triangle-wave PWM mode 3.

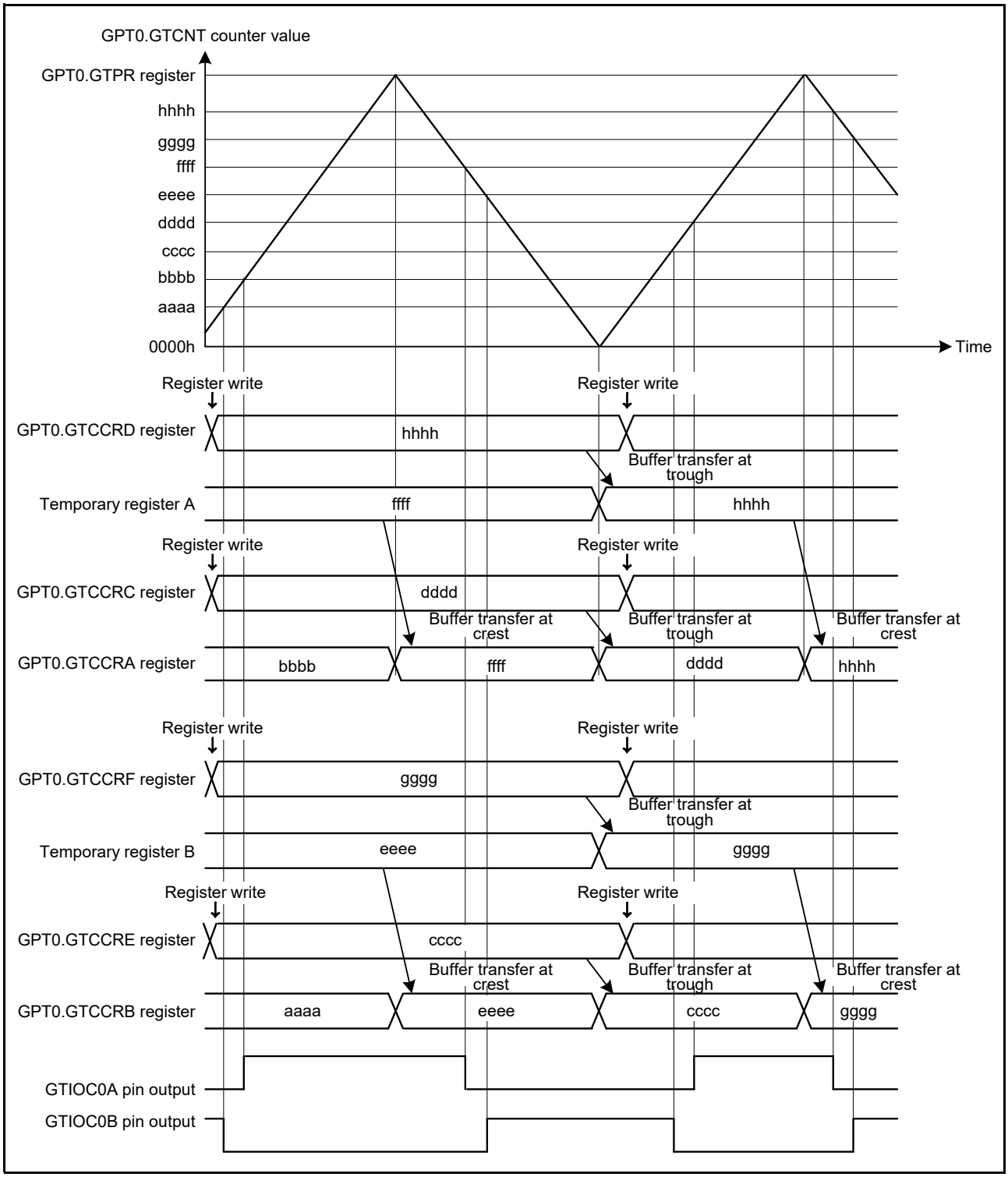


Figure 22.37 Example of Triangle-Wave PWM Mode 3 Operation (Low Output from the GTIOC0A Pin and High Output from the GTIOC0B Pin at Initial Output, Output Toggled at GTCCRA/GTCCRB Compare Match, Output Retained at the End of the Cycle)

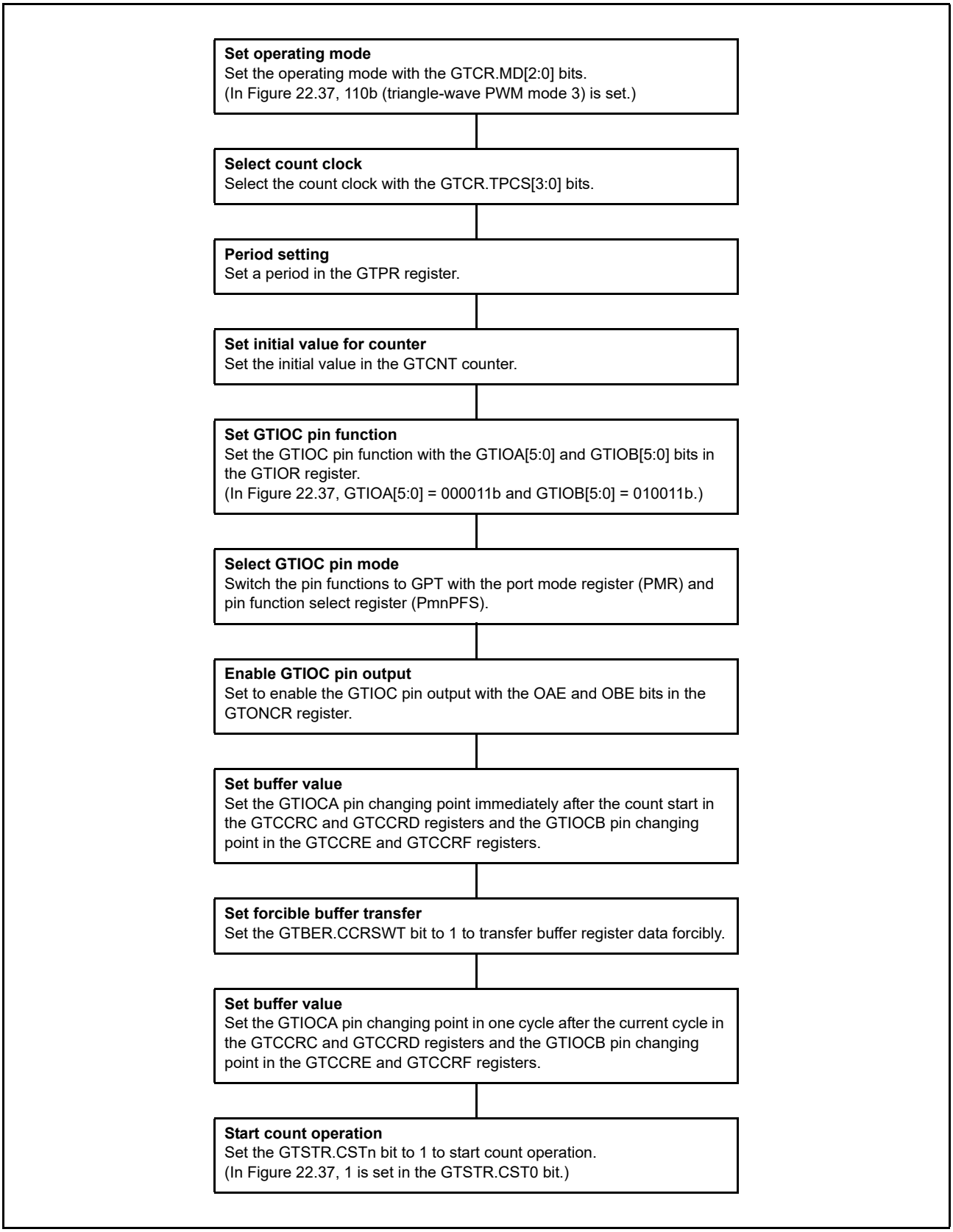


Figure 22.38 Example for Setting Triangle-Wave PWM Mode 3

22.3.4 Automatic Dead Time Setting Function

By setting the GTDTCR register, a compare match value for a negative waveform with dead time obtained by a compare match value for a positive waveform (the GTCCRA(LW) value) and specified dead time values (the GTDVU(LW) and GTDVD(LW) values) can automatically be set to the GTCCRB(LW) register.
The automatic dead time setting function can be used in saw-wave one-shot pulse mode and all the triangle PWM modes. Dead time can be separately set for the first half and second half of a waveform. Dead time for the changing point in the first half of a negative waveform is set in the GTDVU(LW) register and that in the second half is set in the GTDVD(LW) register. The same dead time can also be set for the first and second halves.
The GTDBU(LW) register can be used as a buffer register of the GTDVU(LW) register, and the GTDBD(LW) register can be used as a buffer register of the GTDVD(LW) register. Buffer transfer is performed at the end of the cycle (in saw-wave mode, either of an overflow of the GTCNT(LW) counter (up-counting), an underflow (down-counting), or counter clearing by a hardware source, software, or synchronous clearing; in triangle-wave mode, a trough).
The change point of the negative-phase waveform, which is automatically calculated, is obtained by reading the GTCCRB(LW) register. Writing to the GTCCRB(LW) register is prohibited when the automatic dead time setting function is used.

Do not set the dead-time that makes the change point of the waveform exceeding the count period. When any dead-time setting which would generate a dead-time error is made, adjust the change points of the positive- and negative-phase waveforms to generate waveforms with secured dead-time as shown in Table 22.7. The adjusted change point of the negative-phase waveform is automatically set in the GTCCRB(LW) register. An internal signal is used to judge the change point of the positive-phase waveform, thus the value of the GTCCRA(LW) register is not updated by the adjusted value.
If the order of the change point becomes inconsistent by adjustment of the waveform change point due to occurrence of dead time errors, or if the change point exceeds the count period even after the adjustment, the complementary relation between the positive- and negative-phases cannot be guaranteed.
If dead-time exceeds the count period by setting 0000h (0000 0000h) or a value greater than or equal to the setting value of the GTPR(LW) register is set in the GTCCRA(LW) register in triangle-wave PWM mode, output change is controlled by the output protection function (refer to section 22.6.4, Output Protection Function for GTIOC Pin Output).
When GTCCRA(LW) is greater than or equal to [GTPR(LW) + GTDVm(LW)], [GTPR(LW) – 1] is set in the GTCCRB(LW) register as the upper limit.

Table 22.7 Adjustment of the Waveform Change Point When a Dead-Time Error Occurs

Mode	Count Direction	Period	Condition for Dead-Time Error	Change Point of the Positive-Phase Waveform after Adjustment	Change Point of the Negative-Phase Waveform after Adjustment
Saw-wave one-shot pulse mode	Up-counting	First half	GTCCRA(LW) – GTDVU(LW) < 0	GTDVU(LW)	0
		Second half	GTCCRA(LW) + GTDVD(LW) > GTPR(LW)	GTPR(LW) – GTDVD(LW)	GTPR(LW)
	Down-counting	First half	GTCCRA(LW) + GTDVU(LW) > GTPR(LW)	GTPR(LW) – GTDVU(LW)	GTPR(LW)
		Second half	GTCCRA(LW) – GTDVD(LW) < 0	GTDVD(LW)	0
Triangle-wave PWM mode 1/2/3	Up-counting	(First half)	GTCCRA(LW) – GTDVU(LW) ≤ 0	GTDVU(LW) + 1	1
	Down-counting	(Second half)	GTCCRA(LW) – GTDVD(LW) < 0	GTDVD(LW)	0

Figure 22.39 to Figure 22.42 show examples of automatic dead time setting function operation. Figure 22.43 and Figure 22.44 show the setting examples.

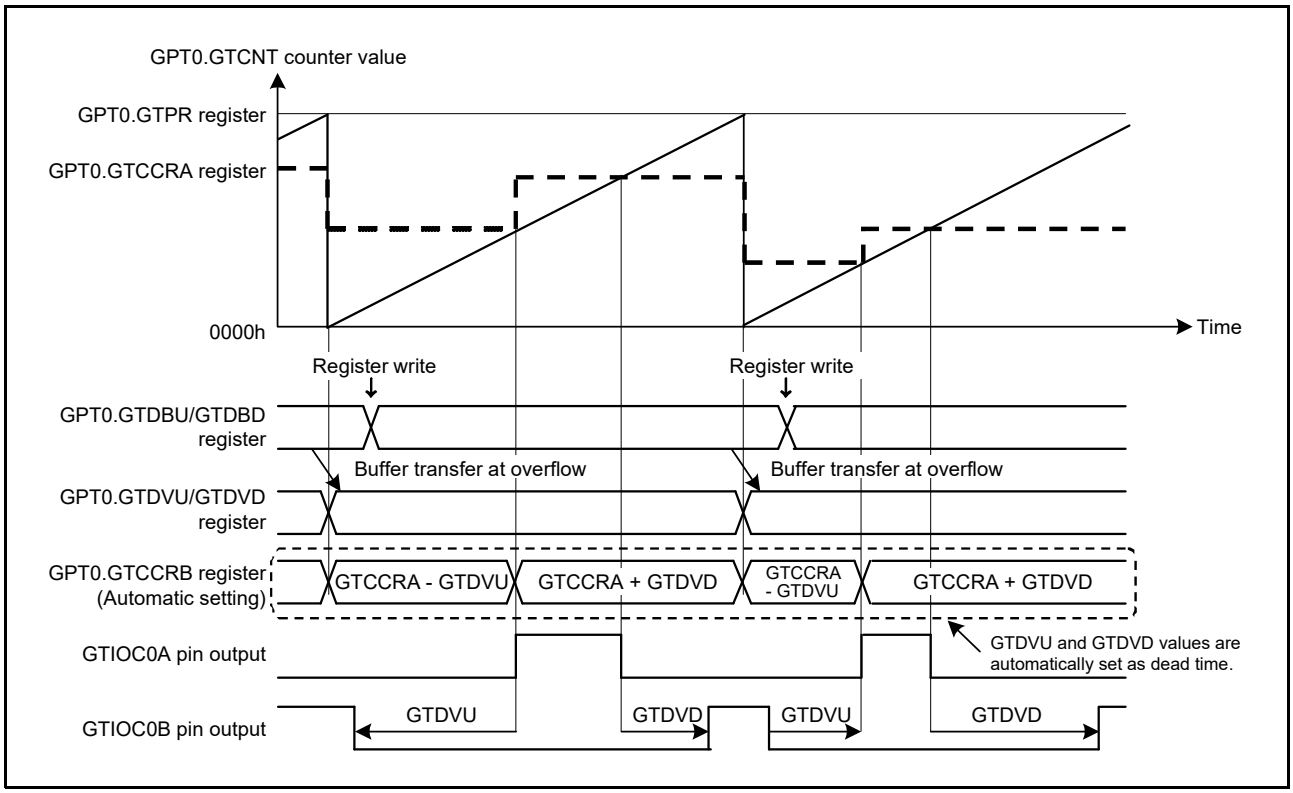


Figure 22.39 Example of Automatic Dead Time Setting Function Operation (Saw-Wave One-Shot Pulse Mode, Up-Counting, GTDVU and GTDVD Set to Buffer Operation, Active Level: High)

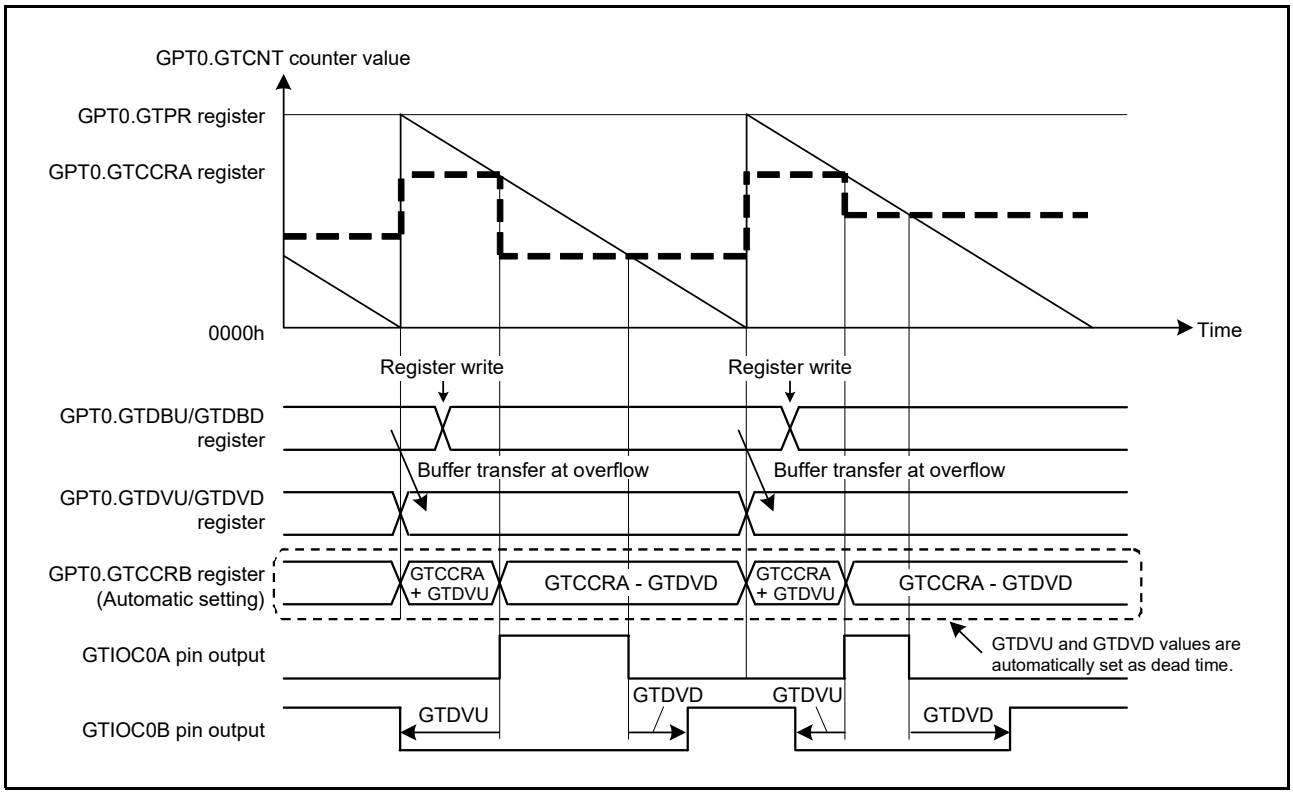


Figure 22.40 Example of Automatic Dead Time Setting Function Operation (Saw-Wave One-Shot Pulse Mode, Down-Counting, GTDVU and GTDVD Set to Buffer Operation, Active Level: High)

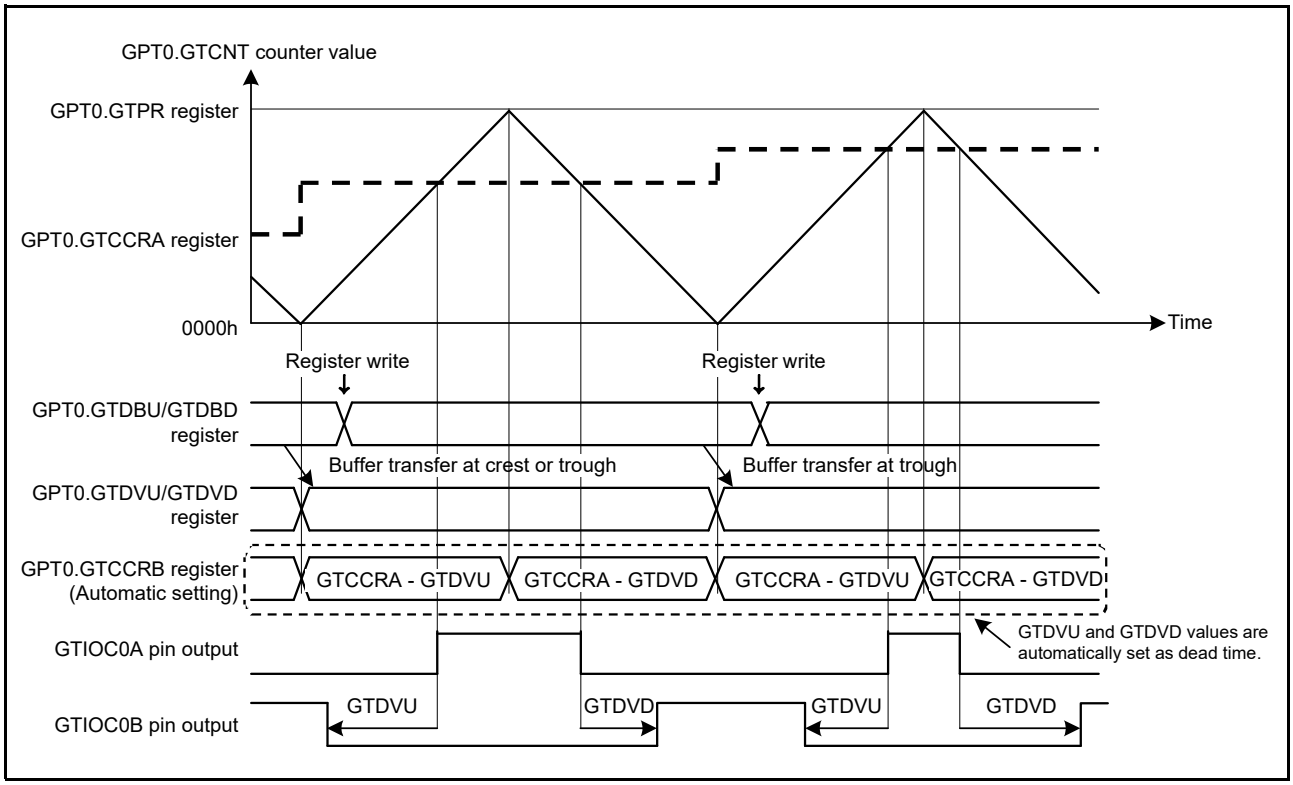


Figure 22.41 Example of Automatic Compare-Match Value Setting Function with Dead Time (Triangle-Wave PWM Mode 1, GTDVU and GTDVD Set to Buffer Operation, Active Level: High)

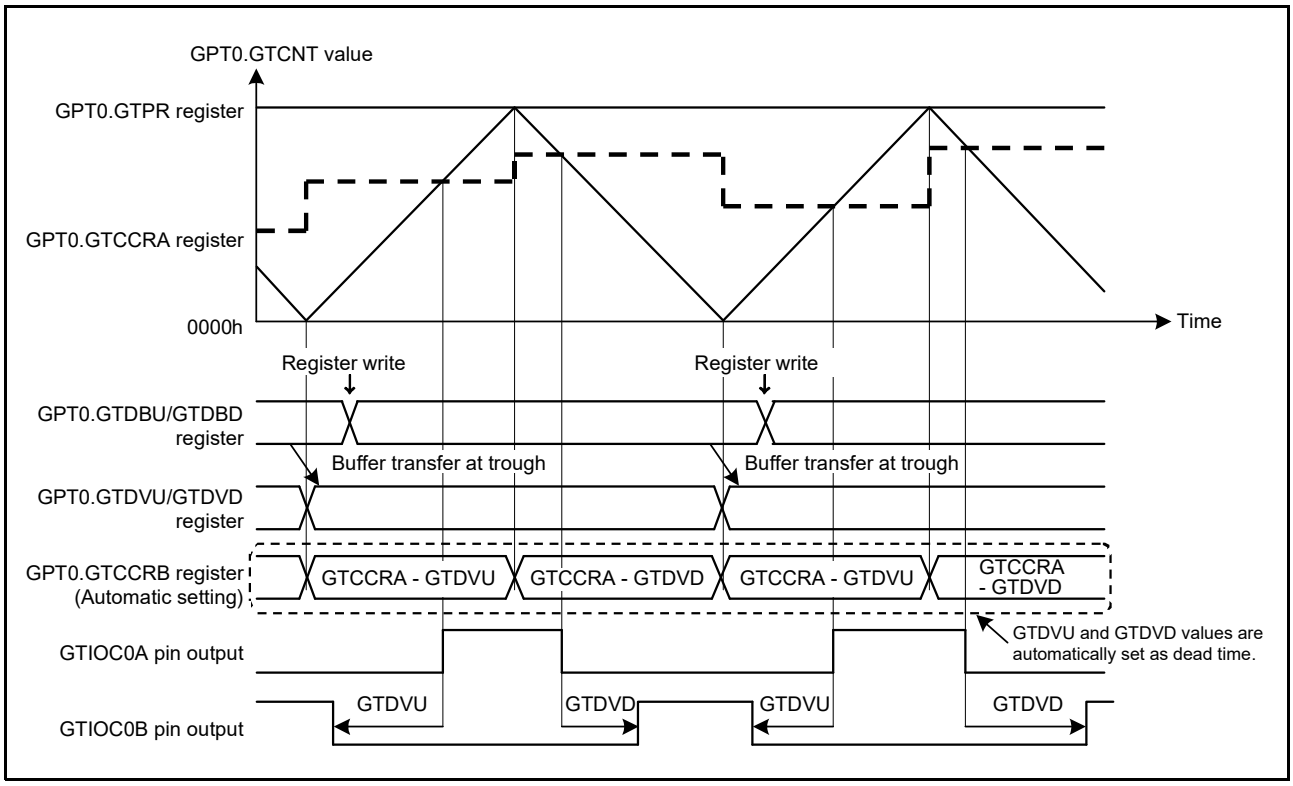


Figure 22.42 Example of Automatic Compare-Match Value Setting Function with Dead Time (Triangle-Wave PWM Mode 2 or 3, GTDVU and GTDVD Set to Buffer Operation, Active Level: High)

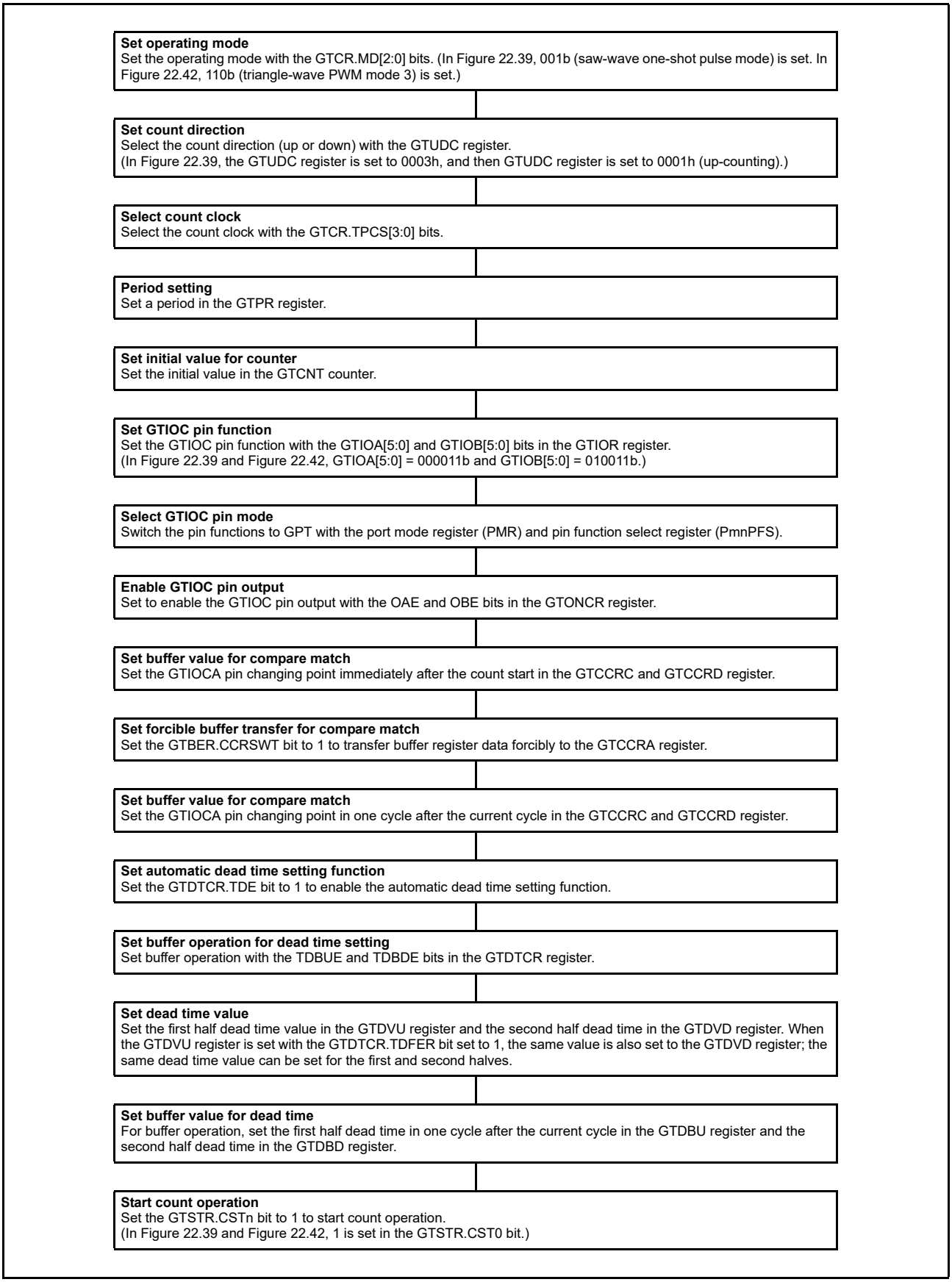


Figure 22.43 Example for Setting Automatic Dead Time Setting Function (Saw-Wave One-Shot Pulse Mode, Triangle-Wave PWM Mode 3)

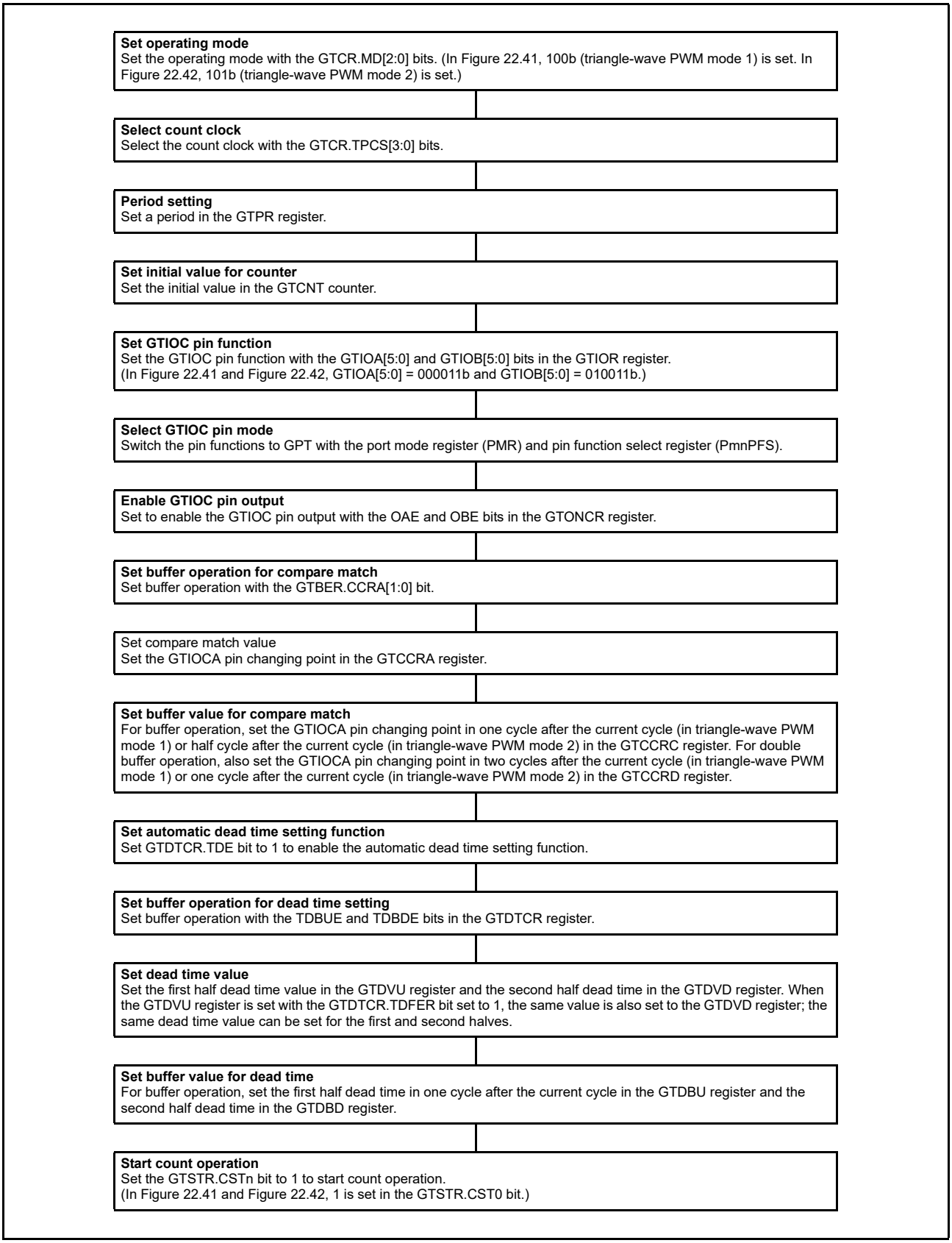


Figure 22.44 Example for Setting Automatic Dead Time Setting Function (Triangle-Wave PWM Mode 1 or 2)

22.3.5 Count Direction Changing Function

The count direction of the GTCNT(LW) counter can be changed by modifying the GTUDC.UD bit.
In saw-wave mode, if the GTUDC.UD bit is modified during count operation, the count direction is changed at an overflow (when modified during up-counting) or an underflow (when modified during down-counting). If the UD bit is modified while count operation is stopped and the GTUDC.UDF bit is 0, the UD bit modification is not reflected at the start of counting and the count direction is changed at an overflow or an underflow. If the UDF bit is set to 1 while count operation is stopped, the UD bit value at that time is reflected at the start of counting.
In triangle-wave mode, the count direction is not changed even though the GTUDC.UD bit is modified during count operation. Similarly, even though the UD bit is modified while count operation is stopped and UDF bit is 0, the UD bit value is not reflected to the count operation. If the UDF bit is set to 1 while count operation is stopped, the UD bit value at that time is reflected at the start of counting.
When counting direction is switched during count operation in saw-wave mode, the value of the GTPR(LW) register after start of up-counting is reflected to the count period in up-counting operation, and the value of the GTPR(LW) register before the start of down-counting is reflected to the count period in down-counting operation.

Figure 22.45 shows an example of count direction changing function operation.

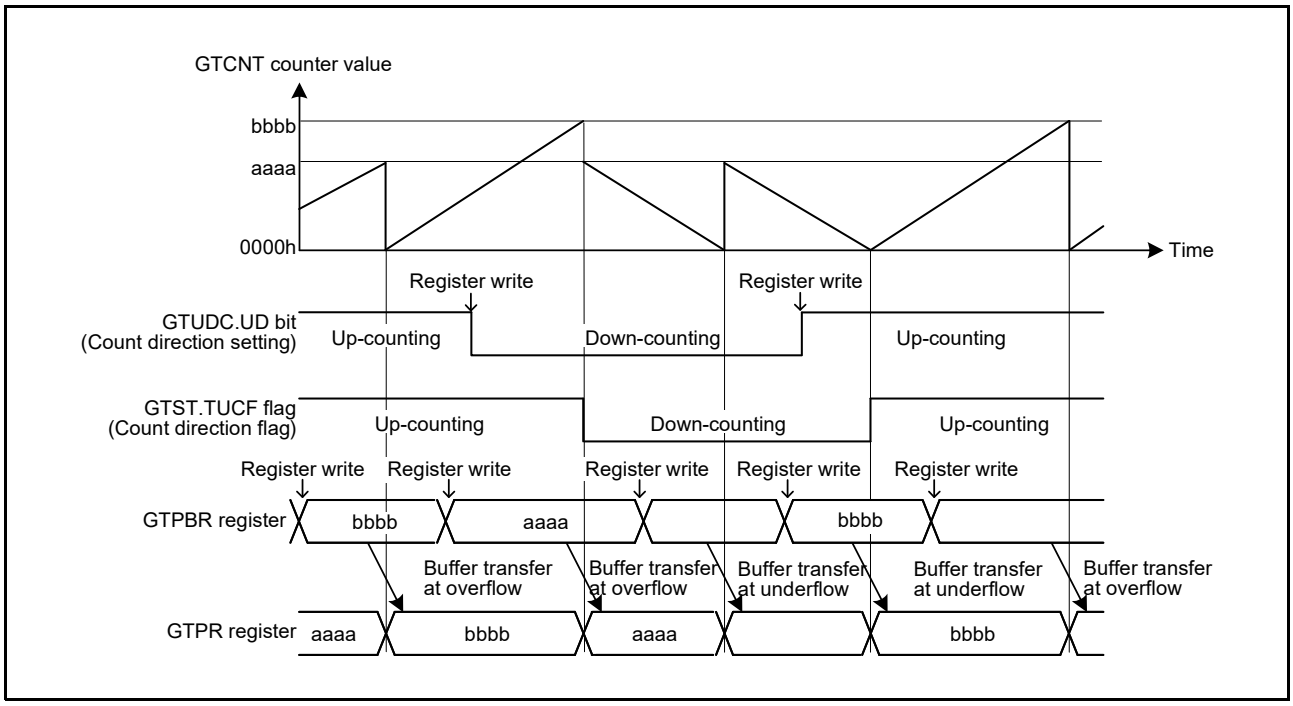


Figure 22.45 Example of Count Direction Changing Function Operation (during Buffer Operation)

22.3.6 Duty Cycle 0%/100% Output Function

Changing the value of the GTUDC.OADTY[1:0] bits and GTUDC.OBDTY[1:0] bits specifies the output duty setting on the GTIOCA and GTIOCB pins to 0% or 100%.

In saw-wave mode, if the value of the OADTY[1:0] bits or OBDTY[1:0] bits is changed during the count operation, the output duty-cycle setting is reflected at an overflow (when changed during up-counting) or an underflow (when changed during down-counting). When the GTUDC.OADTYF bit or GTUDC.OBDTYF bit is 0 while count operation is stopped and the value of the OADTY[1:0] bits or OBDTY[1:0] bits is changed, the output duty-cycle setting changed at the start of counting is not reflected, but the output duty-cycle setting changed at an overflow or underflow is reflected. When the OADTYF bit or OBDTYF bit is 1 while count operation is stopped and the value of the OADTY[1:0] bits or OBDTY[1:0] bits is changed, the value of the OADTY[1:0] bits or OBDTY[1:0] bits at that time is reflected at the start of counting.

In triangle-wave mode, if the value of the OADTY[1:0] bits or OBDTY[1:0] bits is changed during the count operation, the output duty-cycle setting changed at an underflow is reflected.

When the OADTYF bit or OBDTYF bit is 0 while count operation is stopped and the value of the OADTY[1:0] bits or OBDTY[1:0] bits is changed, the output duty-cycle setting changed at the start of counting is not reflected, but the output duty-cycle setting changed at an underflow is reflected. When the OADTYF bit or OBDTYF bit is 1 while count operation is stopped and the value of the OADTY[1:0] bits or OBDTY[1:0] bits is changed, the value of the OADTY[1:0] bits or OBDTY[1:0] bits at that time is reflected at the start of counting.

During operation with a duty cycle of 0% or 100%, the GPT internally continues with compare match operations, and the following occur in response to matches: setting of the compare match flag, interrupt output, and buffer operation.

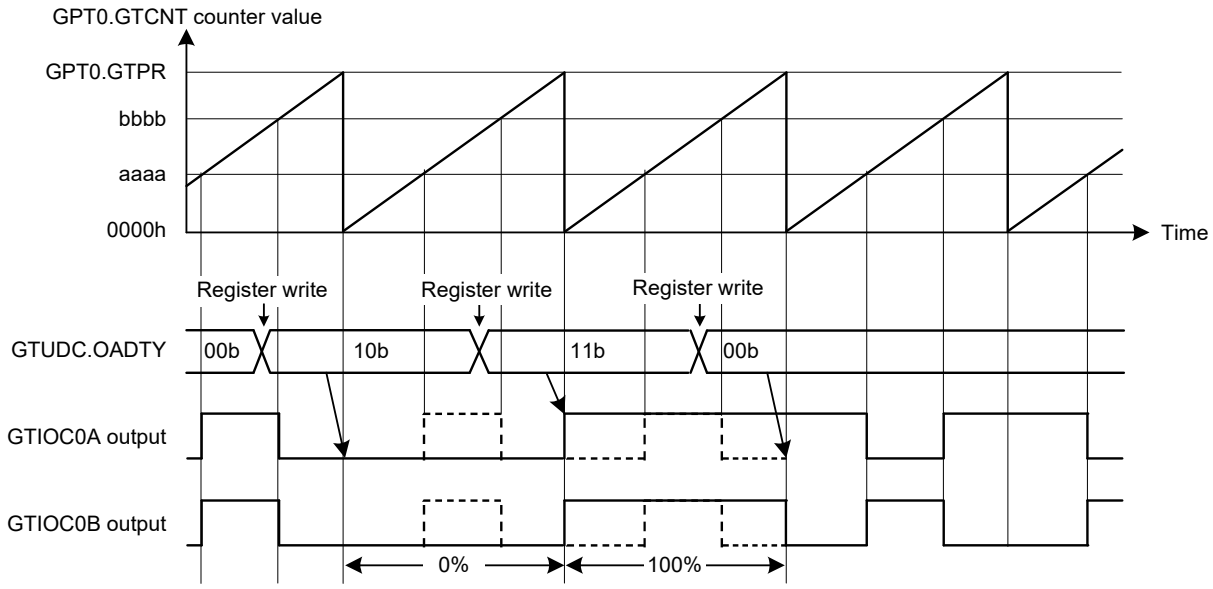
When the output duty setting is changed from 0% or 100% due to a compare match, the GTIOR.GTIOA[3:2] bits and the GTUDDTYC.OADTYR bit determine the level output on the GTIOCA pin and GTIOR.GTIOB[3:2] bits and GTUDC.OBDTYR bit determine the level output on the GTIOCB pin at the end of the cycle.

When the value of the GTIOA[3:2] bits or the GTIOB[3:2] bits is 01b, 0 is output at the end of the cycle. When the value is 10b, 1 is output at the end of cycle. When the value is 10b, 1 is output at the end of the cycle. The current level is maintained if the value is 00b (output retention at the end of the cycle) but maintenance or a value to control toggling is selected by the OADTYR and OBDTYR bits are selected after the period has elapsed if the output has become toggled and the setting is 11b (toggling the output at the end of the cycle). Table 22.8 lists the output values at the end of the cycle when the output setting is changed from duty 0% or 100% to compare match.

Table 22.8 Output Value after Release of Duty 0%/100% (m = A, B)

GTIOR.GTIOm[3:2]	Value at Compare Match Output at the End of the Cycle in the Case of Masking by a Duty Cycle 0% or 100%	The GTUDC.OADTYR Bit at Duty 0% Setting		The GTUDC.OBDTYR Bit at Duty 100% Setting	
		0	1	0	1
00b (Output retained at the end of the cycle)	0	0	0	1	0
	1	0	1	1	1
01b (0 is output at the end of the cycle)	—	0	0	0	0
10b (1 is output at the end of the cycle)	—	1	1	1	1
11b (Toggle output at the end of the cycle)	0	1	1	0	1
	1	1	0	0	0

Figure 22.46 shows an example of operation of the output of the duty cycle 0% or 100%.



[Examples of setting]

Setting of the GPT0.GTIOR.GTIOA[4:0] bits: 00011b
The initial output is 0, the output is toggled on a compare match, and the output is maintained at the end of the period.

Setting of the GPT0.GTUDC.OADTYR bit: 0
The function selected by the GTIOA[3:2] bits is applied to the output value when the duty cycle is set after release from 0 or 100% duty-cycle setting.

Setting of the GPT0.GTIOR.GTIOB[4:0] bits: 00011b
The initial output is 0, the output is toggled on a compare match, and the output is maintained at the end of the period.

Setting of the GPT0.GTUDC.OBDTYF bit: 1
The function of the GTIOB[3:2] bits is applied to the compare match output value which is masked after 0 or 100% duty setting release.

Figure 22.46 Example of Operation of Output of Duty Cycle 0% or 100%

22.3.7 Hardware Count Start/Count Stop and Clear Operation

The GTCNT(LW) counter can be started, stopped, or cleared by hardware sources in this MCU.
There are 5 types of hardware sources, including GTETRG pin input, comparator output, MTU count start (only count start control is enabled), GTIOC3A and GTIOC3B pin inputs, and GTIOC3A and GTIOC3B pin internal outputs (output compare).
The GTCNT(LW) counter can also be cleared by the GTCCRA(LW) or GTCCRB(LW) input capture.

22.3.7.1 Hardware Start Operation

The GTCNT(LW) counter can be started by a hardware source. Select a hardware source to start counting using the GTHSSR.CSHSLn[3:0] bits (n = 0 to 3), set the edge polarity for the hardware source with the GTHSCR.CSHWn[1:0] bits, and then enable to start counting.
Figure 22.47 shows an example of count start operation by a hardware source. Figure 22.48 shows the setting example.

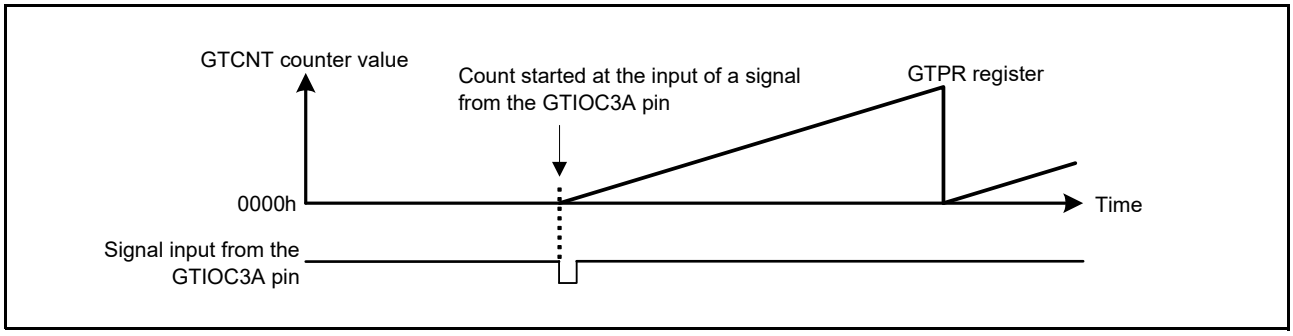


Figure 22.47 Example of Count Start Operation by Hardware Source (Started at Input of Signal from the GTIOC3A Pin)

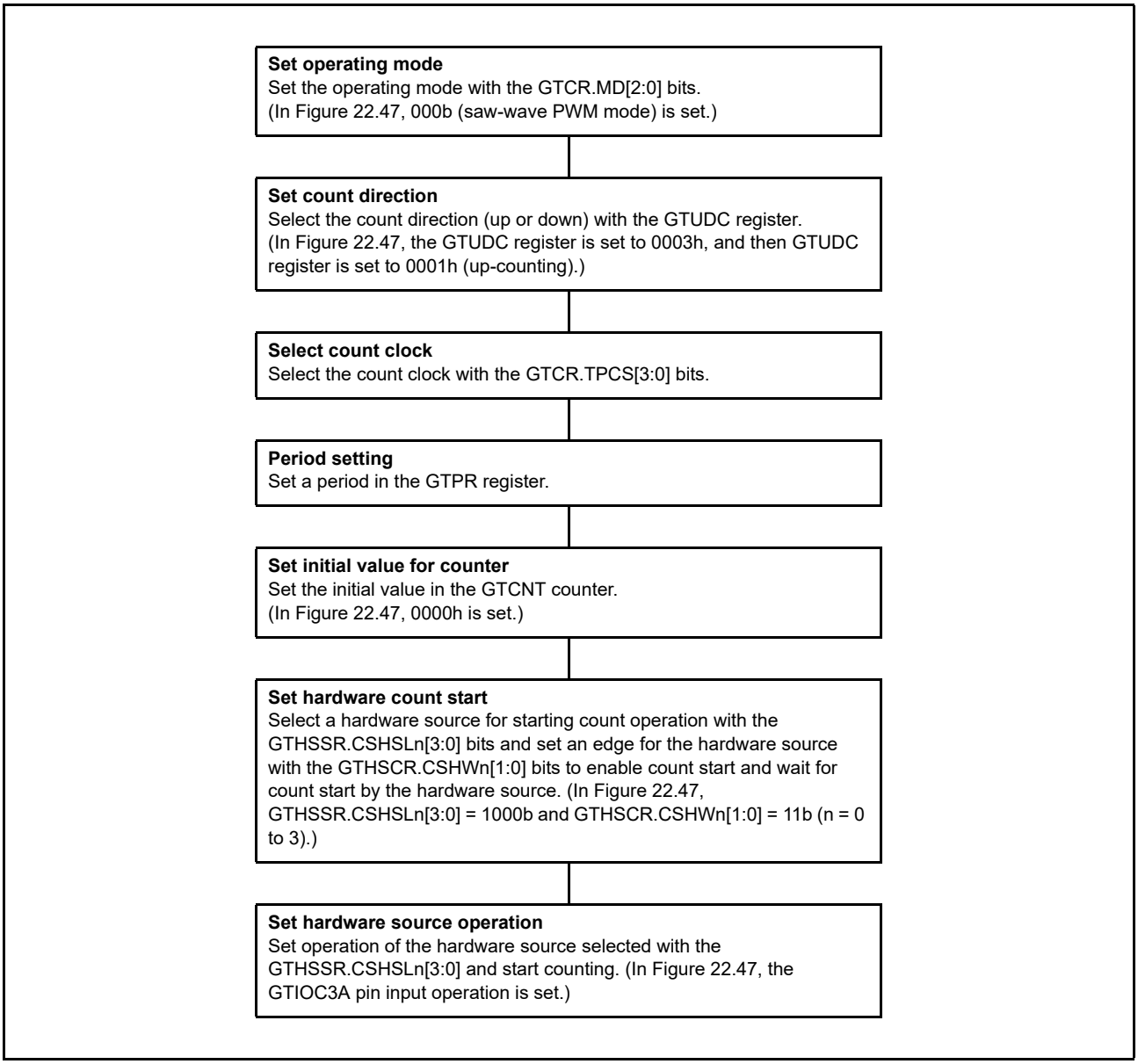


Figure 22.48 Example for Setting Count Start Operation by Hardware Source

22.3.7.2 Hardware Stop Operation

The GTCNT(LW) counter can be stopped by a hardware source. Select a hardware source to stop counting using the GTHPSR.CSHPLn[3:0] bits (n = 0 to 3), set the edge polarity for the hardware source with the GTHSCR.CPHWn[1:0] bit, and then enable to stop counting.

Figure 22.49 shows an example of count stop operation by a hardware source. Figure 22.50 shows the setting example. In this example, the count operation is stopped at both edges of the GTIOC3A pin internal output (output compare) and is restarted at both edges of the GTIOC3B pin internal output (output compare).

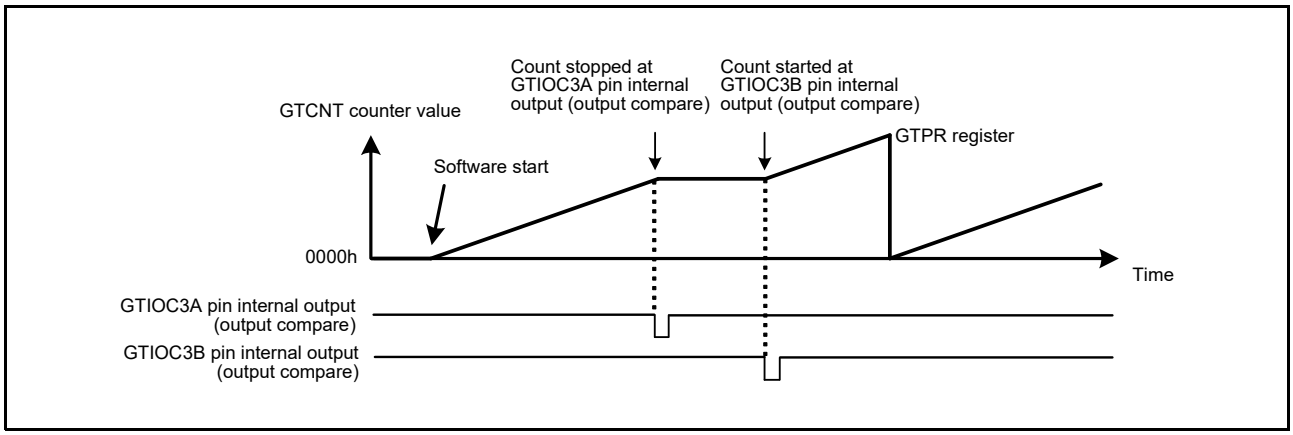


Figure 22.49 Example of Count Stop Operation by Hardware Source (Started by Software, Stopped at GTIOC3A Pin Internal Output (Output Compare), Restarted at GTIOC3B Pin Internal Output (Output Compare))

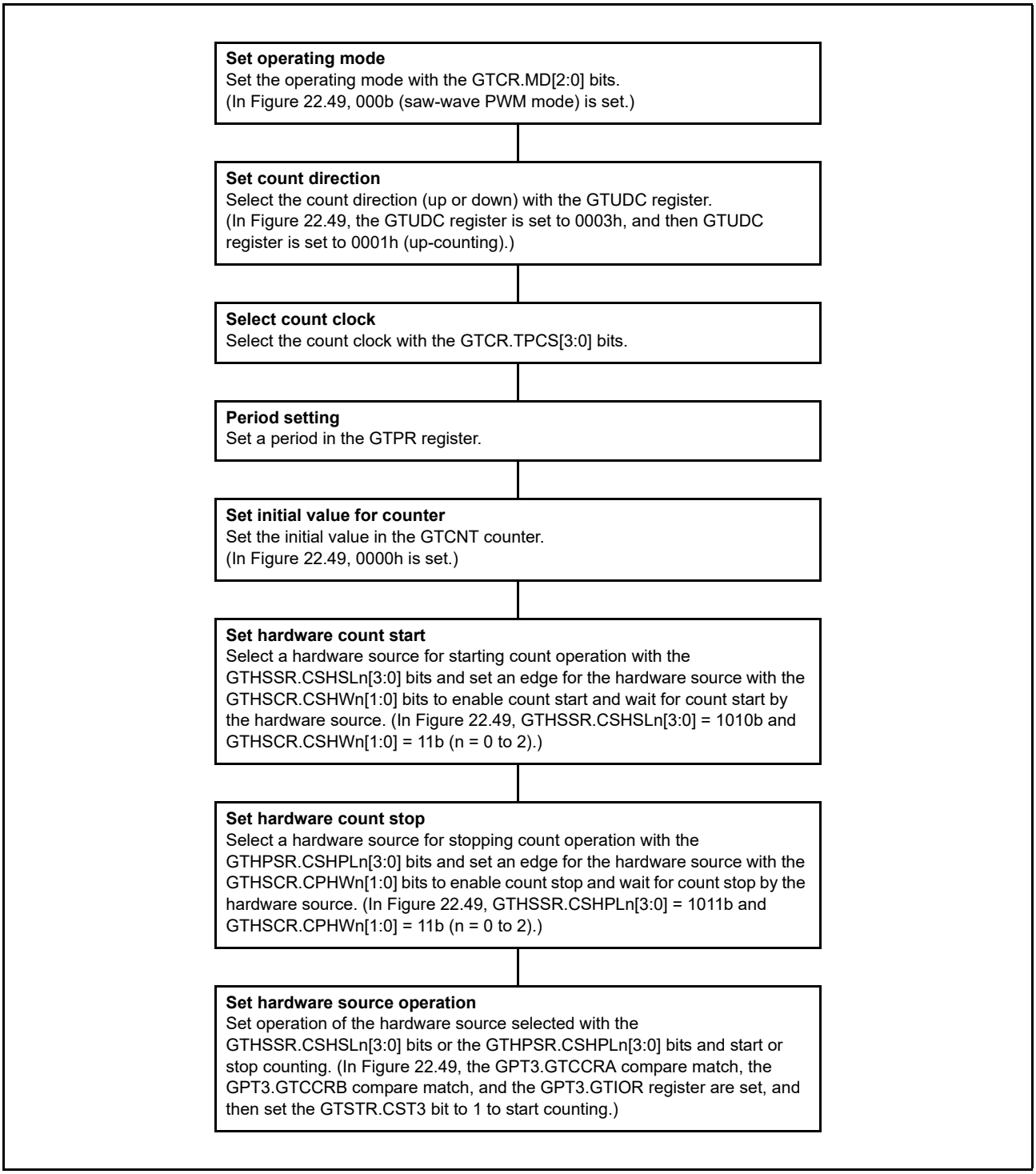


Figure 22.50 Example for Setting Count Stop Operation by Hardware Source

Figure 22.51 shows an example of count start/stop operation by a hardware source. Figure 22.52 shows the setting example. In this example, the counter operates during the high-level periods of the external trigger input GTETRG.

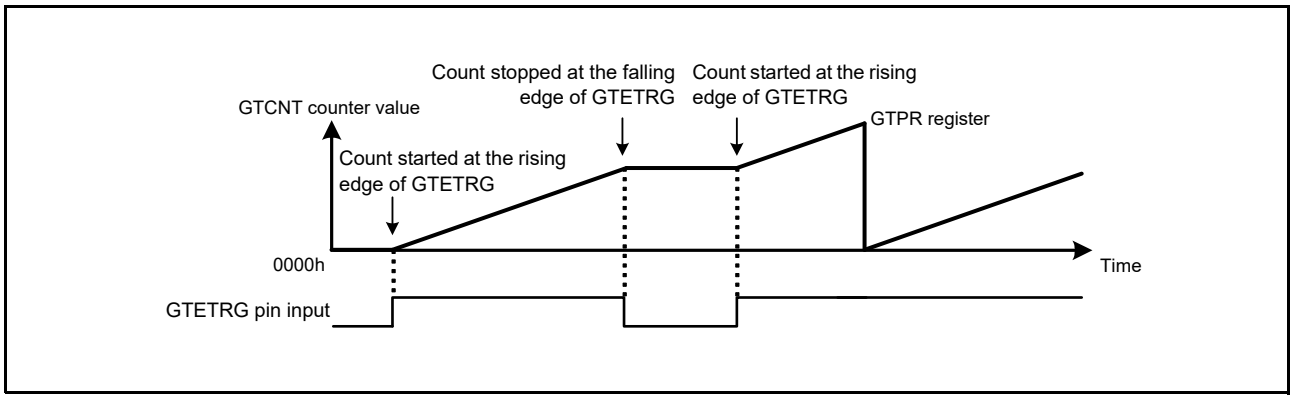


Figure 22.51 Example of Count Start/Stop Operation by Hardware Source (Started at Rising Edge of GTETRG Pin Input, Stopped at Falling Edge of GTETRG Pin Input)

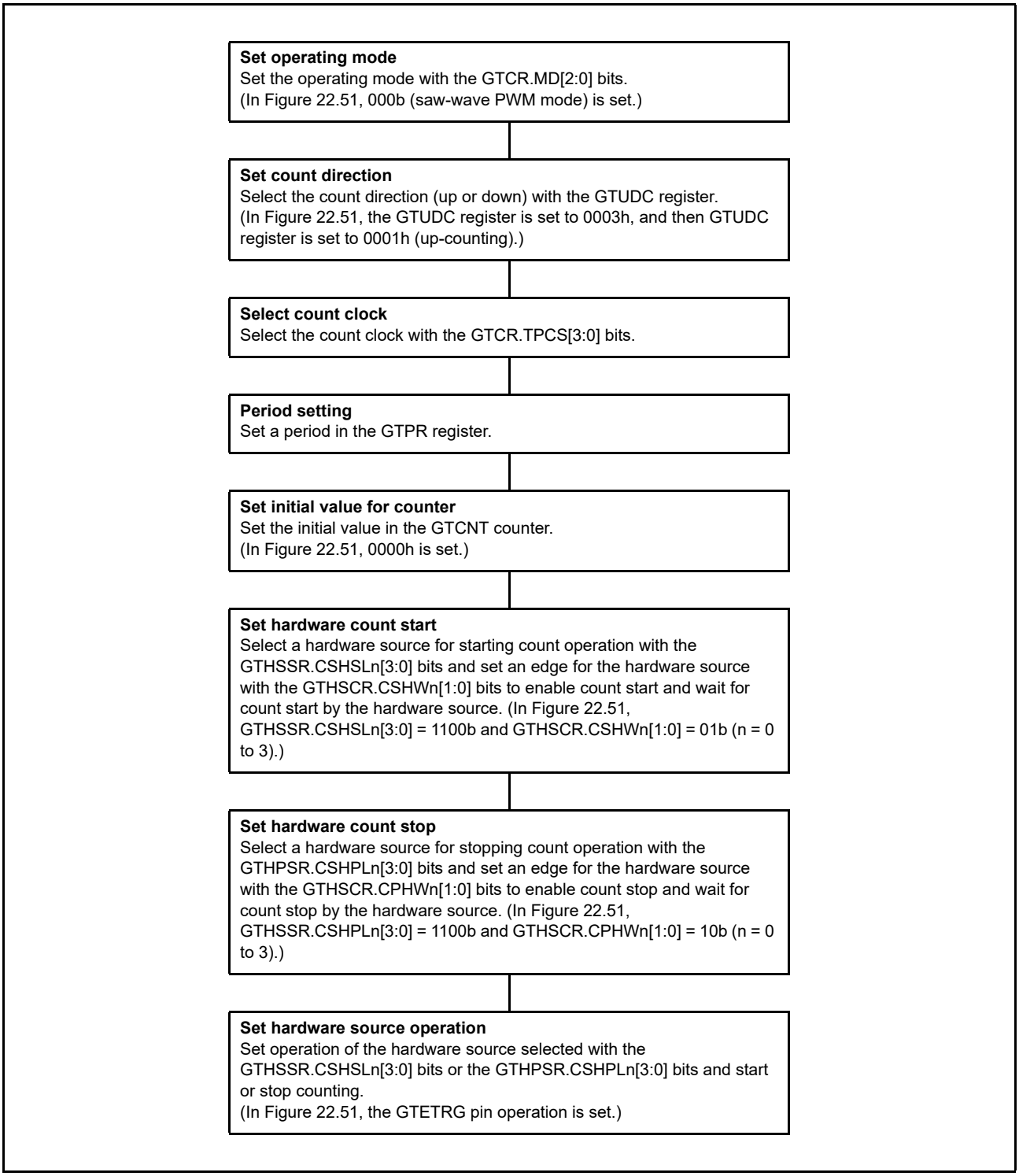


Figure 22.52 Example for Setting Count Start/Stop Operation by Hardware Source

22.3.7.3 Hardware Clear Operation

The GTCNT(LW) counter can be cleared by a hardware source. Select a hardware source to clear the counter using the GTHPSR.CSHPLn[3:0] bits (n = 0 to 3), set the edge polarity for the hardware source with the GTHCCR.CCHWn[1:0] bits, and enable clearing the counter.

The GTCNT(LW) counter can also be cleared by a GTCCRA(LW) or GTCCRB(LW) input capture by setting the GTCR.CCLR[1:0] bits.

When the count direction is down-counting (GTST.TUCF flag is 0) in saw-wave mode, the GTCNT(LW) counter is set to the value set in the GTPR(LW) register. In other cases, the GTCNT(LW) counter is set to 0000h when counter clearing is executed.

Note that the GTCIV/GTCIU interrupt (overflow/underflow interrupt) is not generated when the GTCNT(LW) counter is cleared by a hardware source or by software.

Figure 22.53 and Figure 22.54 show examples of the GTCNT counter clearing operation by a hardware source. Figure 22.55 shows the setting example. Figure 22.56 shows the relationship between counter clearing by a hardware source and the GTCIV/GTCIU interrupt. In this example, the GTCNT counter is started at both edges of the GTIOC3A pin, and the counter is stopped/cleared at both edges of the GTOC3B pin input.

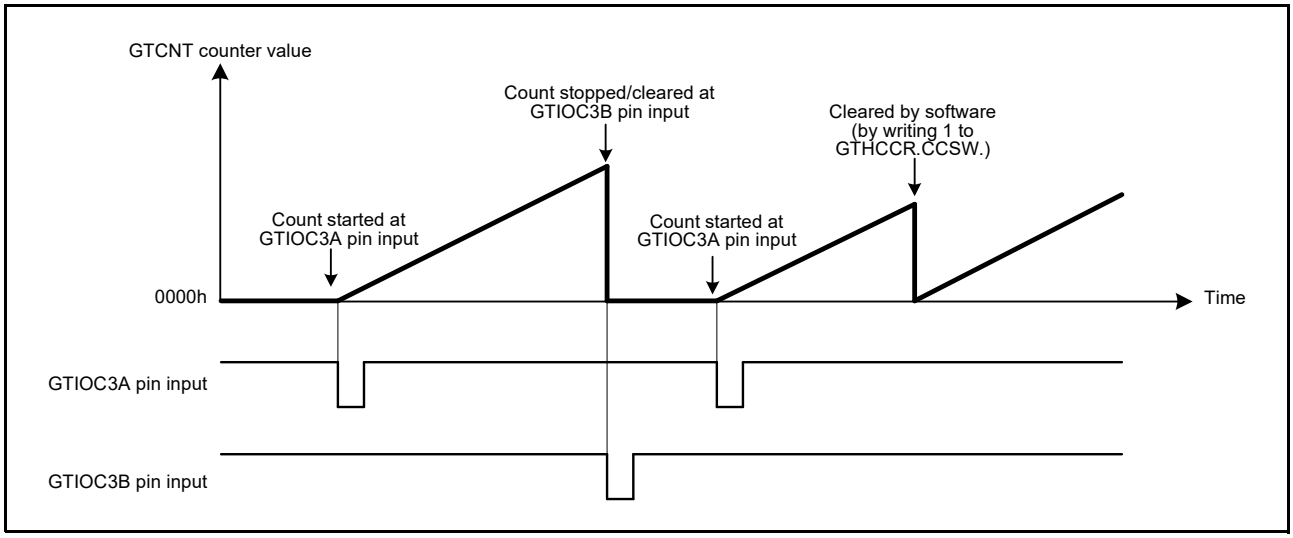


Figure 22.53 Examples of Counter Clearing Operation by Hardware Source (Saw-Wave Up-Counting, Started at GTIOC3A Pin Input, Count Stopped/Cleared at GTIOC3B Pin Input)

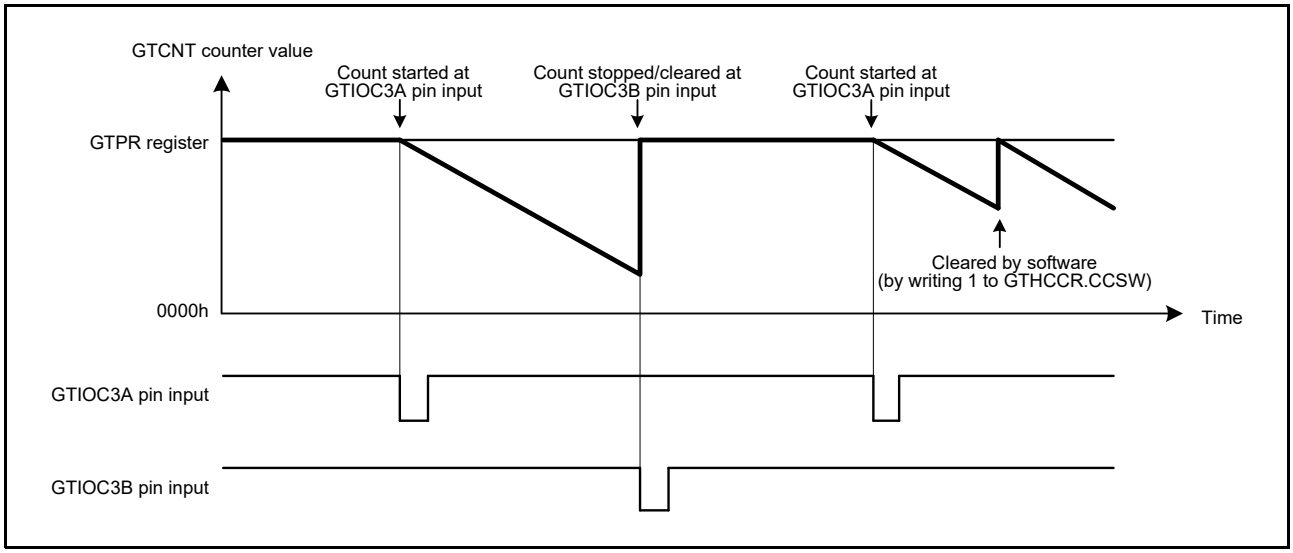


Figure 22.54 Examples of Counter Clearing Operation by Hardware Source (Saw-Wave Down-Counting, Started at GTIOC3A Pin Input, Count Stopped/Cleared at GTIOC3B Pin Input)

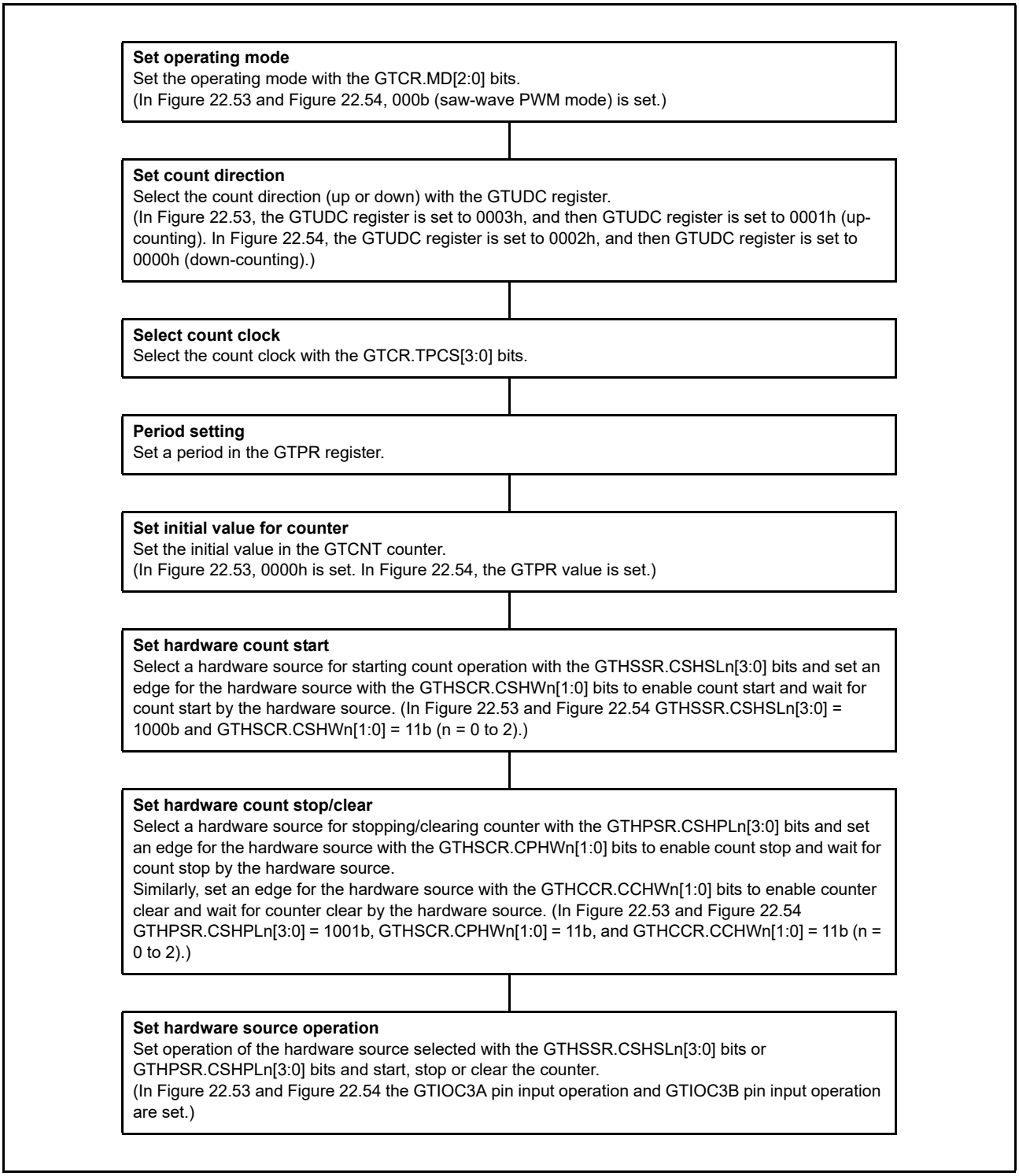


Figure 22.55 Example for Setting Counter Clearing Operation by Hardware Source

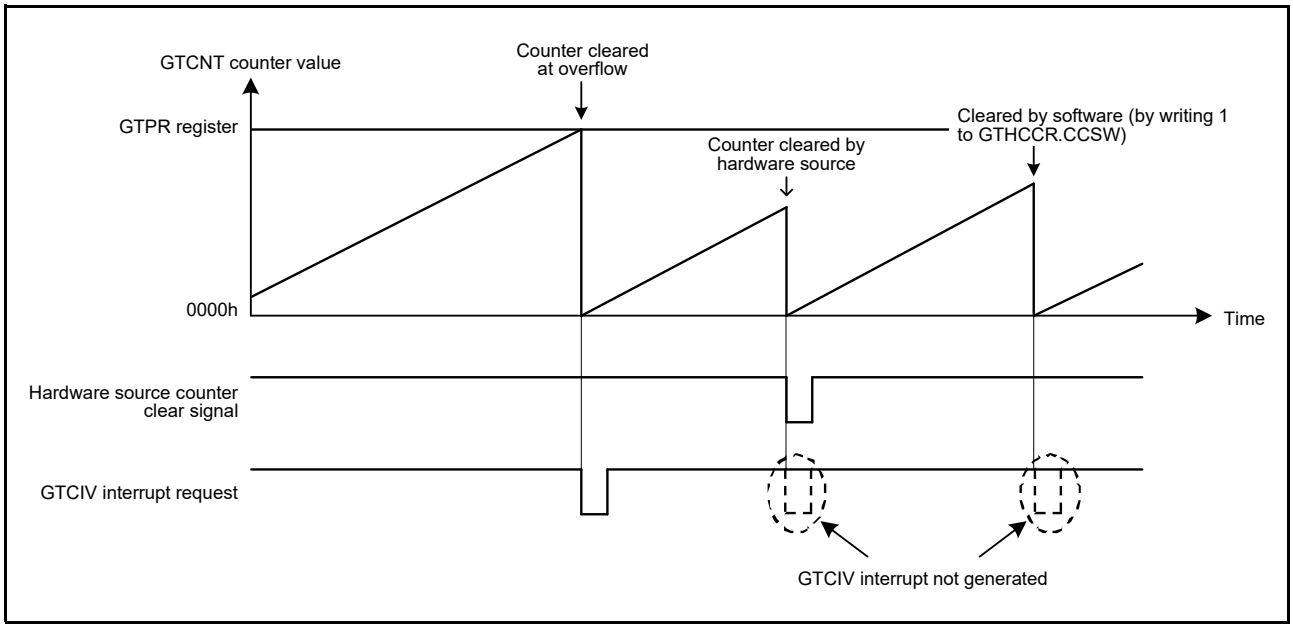


Figure 22.56 Relationship between Counter Clearing by Hardware Source and GTCIV Interrupt

22.3.8 Synchronous Operation

Synchronous operation on channels (synchronous clear operation, synchronous start operation) can be performed.

22.3.8.1 Synchronous Clear Operation

Synchronous clearing on channels can be controlled. Select which channels to be synchronously cleared by setting the GTCR.CCLR[1:0] bits of the pertinent channels to 11b and which channel clearing source to be used for synchronous clearing by setting the GTSYNC.SYNCn[1:0] bits (n = 0 to 3).

The sources used for synchronous clearing are a hardware source, software, input capture, an overflow of saw waves (up-counting) and an underflow (down-counting).

Figure 22.57 shows an example of synchronous clear operation, and Figure 22.59 shows the setting example. In this example, the GPT1.GTCNT and GPT2.GTCNT counters are synchronously cleared by the GPT0.GTCNT clearing source (overflow).

Synchronous clearing of channels by a clear source does not cause synchronous clearing of another channel by the same clear source. (Synchronous clearing is not transmitted.)

Figure 22.58 shows an operation example in which two channels are synchronously cleared by the clear source of one of the channels and another channel is synchronously cleared by the clear source of the other one of the two channels.

Figure 22.59 shows the setting example. In this example, the GPT1.GTCNT counter is synchronously cleared by the GPT0.GTCNT counter clearing source (overflow), and the GPT2.GTCNT counter is synchronously cleared by the GPT1.GTCNT counter clearing source (overflow). Although the GPT1.GTCNT counter is synchronously cleared by the GPT0.GTCNT counter clearing source (overflow), the GPT2.GTCNT counter is not synchronously cleared when the GPT1.GTCNT counter is cleared by the GPT0.GTCNT counter clearing source.

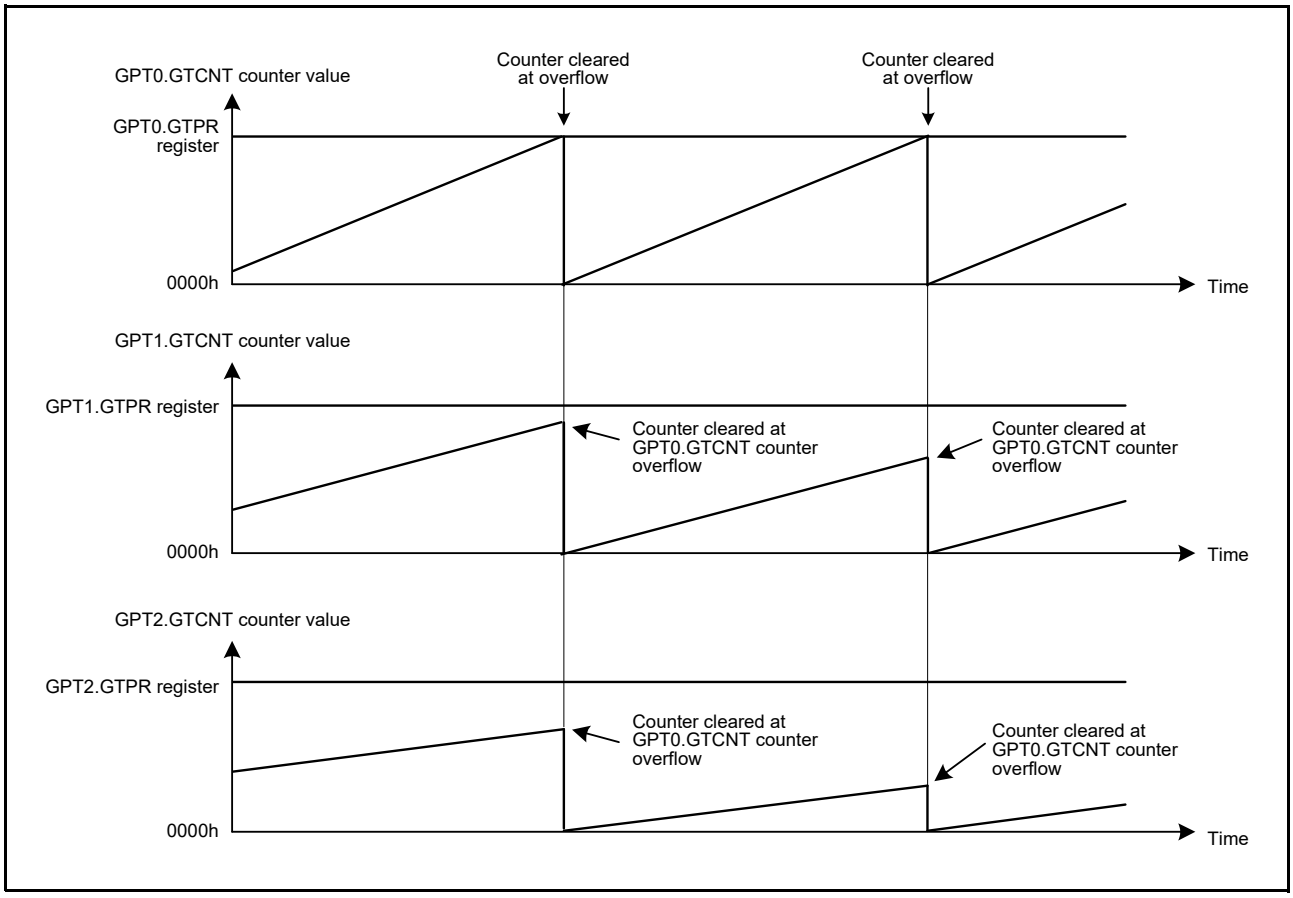


Figure 22.57 Example of Synchronous Clear Operation (GPT1.GTCNT and GPT2.GTCNT Counters are Synchronously Cleared by GPT0.GTCNT Counter Clearing Source)

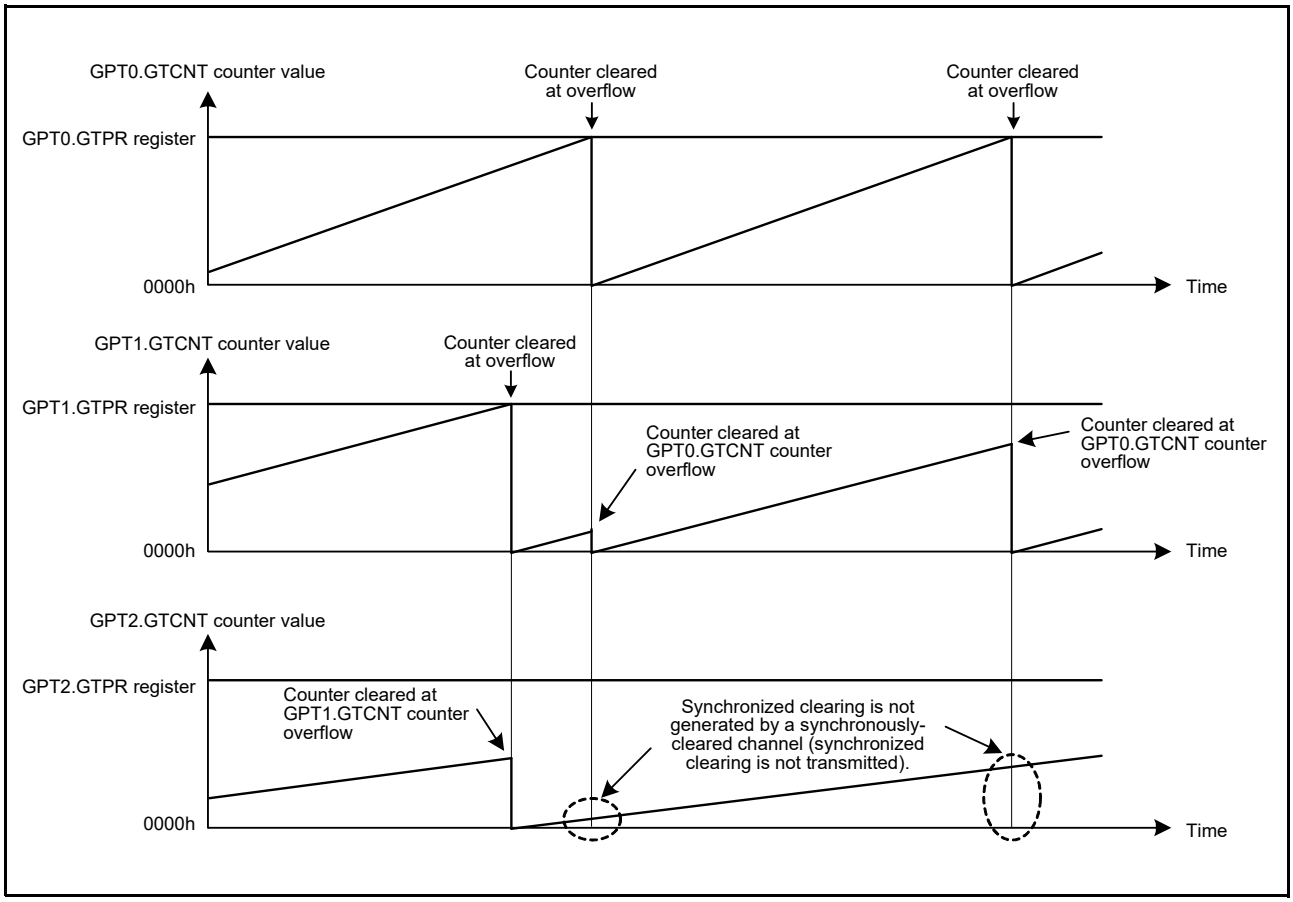


Figure 22.58 Example of Synchronous Clear Operation (GPT1.GTCNT Counter is Synchronously Cleared by GPT0.GTCNT Counter Clearing Source and GPT2.GTCNT Counter is Synchronously Cleared by GPT1.GTCNT Counter Clearing Source)

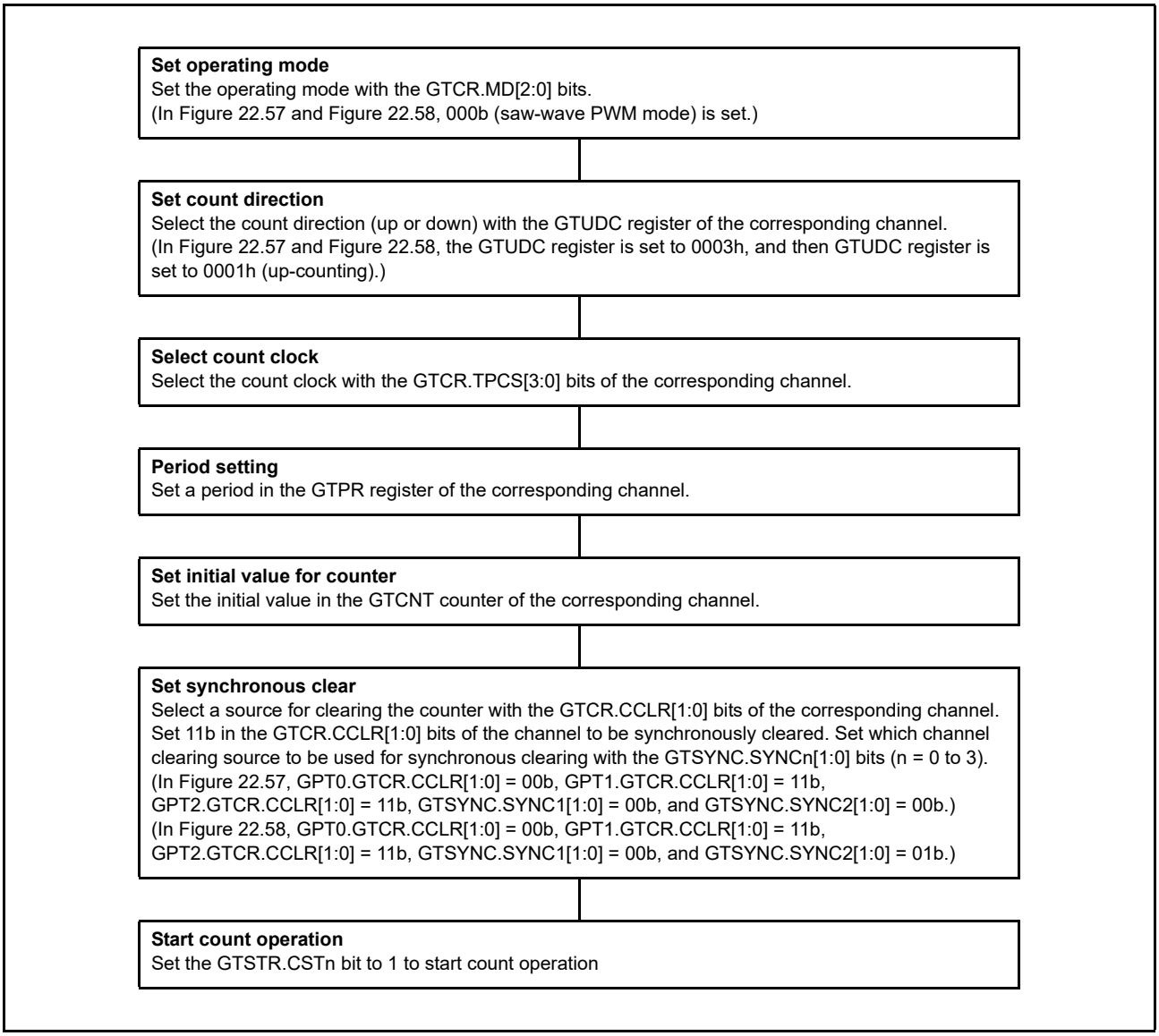


Figure 22.59 Example for Setting Synchronous Clear Operation

22.3.8.2 Synchronous Start Operation

(1) Simultaneous Start by Software

The GPTn.GTCNT(LW) counters can be started simultaneously on channels by simultaneously setting the GTSTR.CSTn bits which correspond to the channels to be started simultaneously to 1 (n = 0 to 3).
Figure 22.60 shows an example of simultaneous start by software.

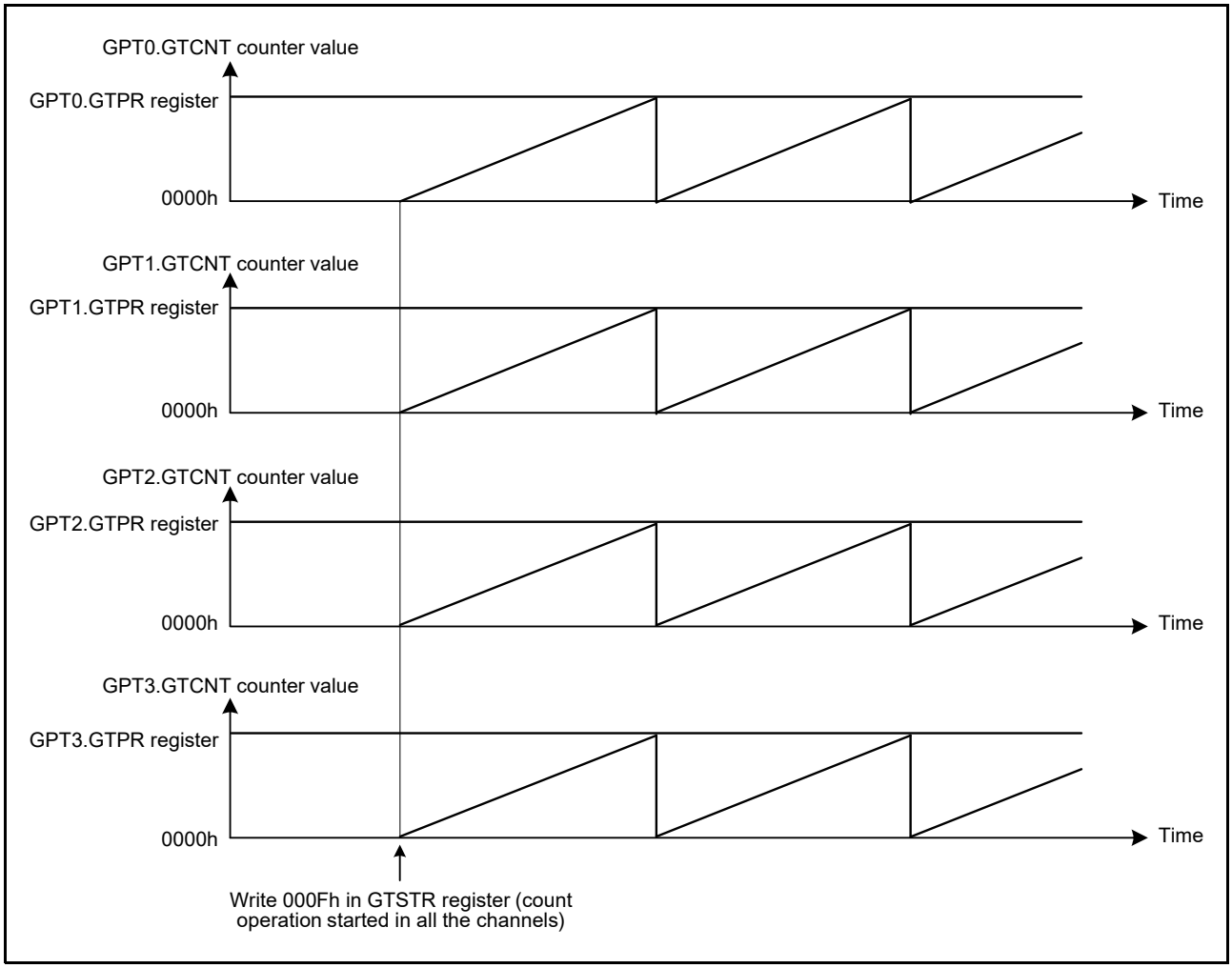


Figure 22.60 Example of Simultaneous Start by Software (with Same Count Period (GTPR Value))

(2) Phase Shift Start by Software

Count start with a phase difference is possible by setting the initial value in the GTCNT(LW) counter before counting starts and then simultaneously setting the GTSTR.CSTn bits which correspond to the channels to be started simultaneously to 1 (n = 0 to 3).

Figure 22.61 shows an example of phase shift start operation by software.

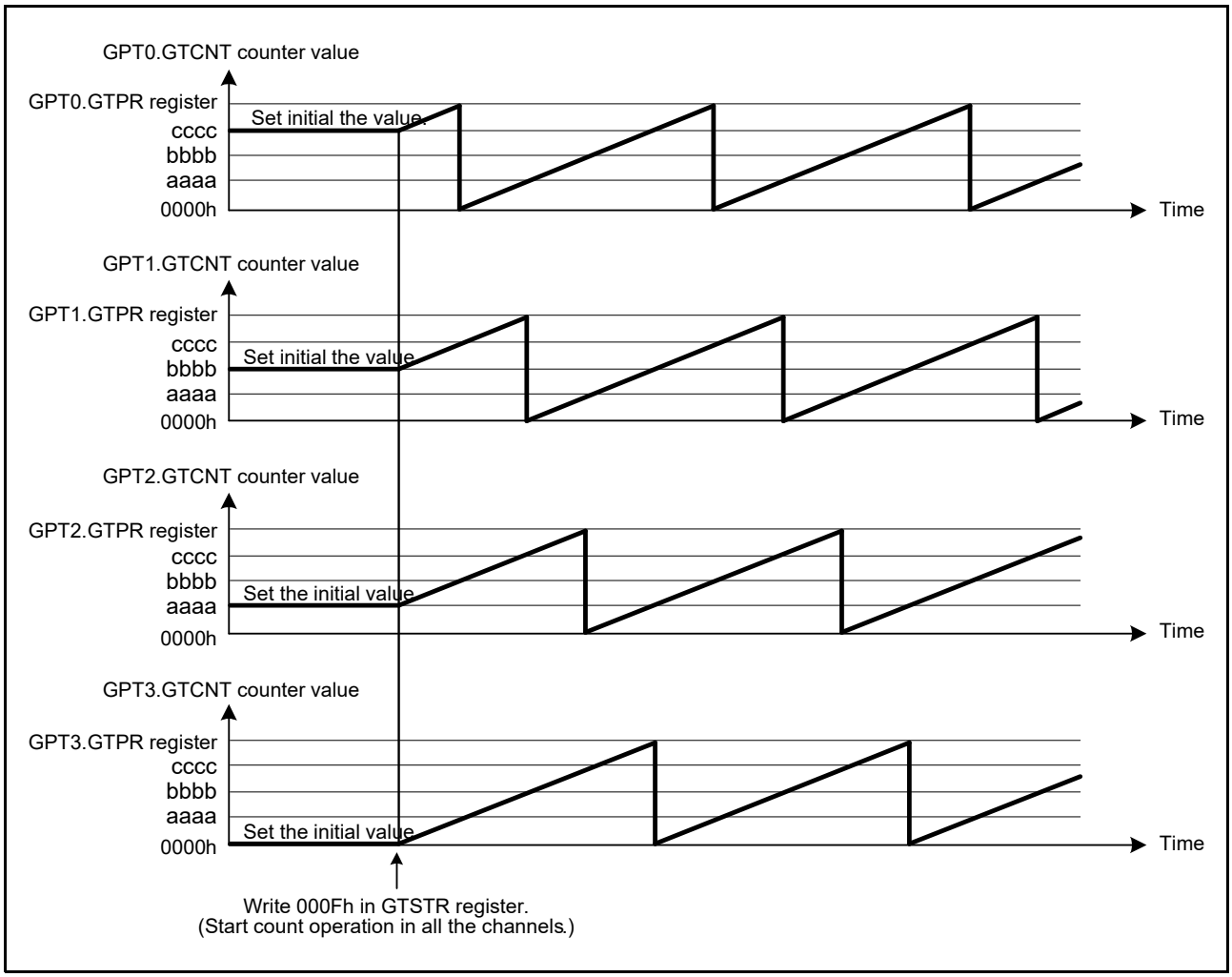


Figure 22.61 Example of Software Phase Shift Start (with Same Count Period (GTPR Register Value))

(3) Simultaneous Start by Hardware Source

The GPTn.GTCNT(LW) counters can be started simultaneously by following hardware sources: GTETRG pin input, comparator output, MTU count start (only count start control is enabled), GTIOC3A/GTIOC3B pin input, and GTIOC3A/GTIOC3B pin internal output (output compare) (n = 0 to 3).

Figure 22.62 shows an example of simultaneous start operation by a hardware source and Figure 22.63 shows the setting example. In this example, count operation is started in all the channels by the input of a signal from the GTIOC3A pin.

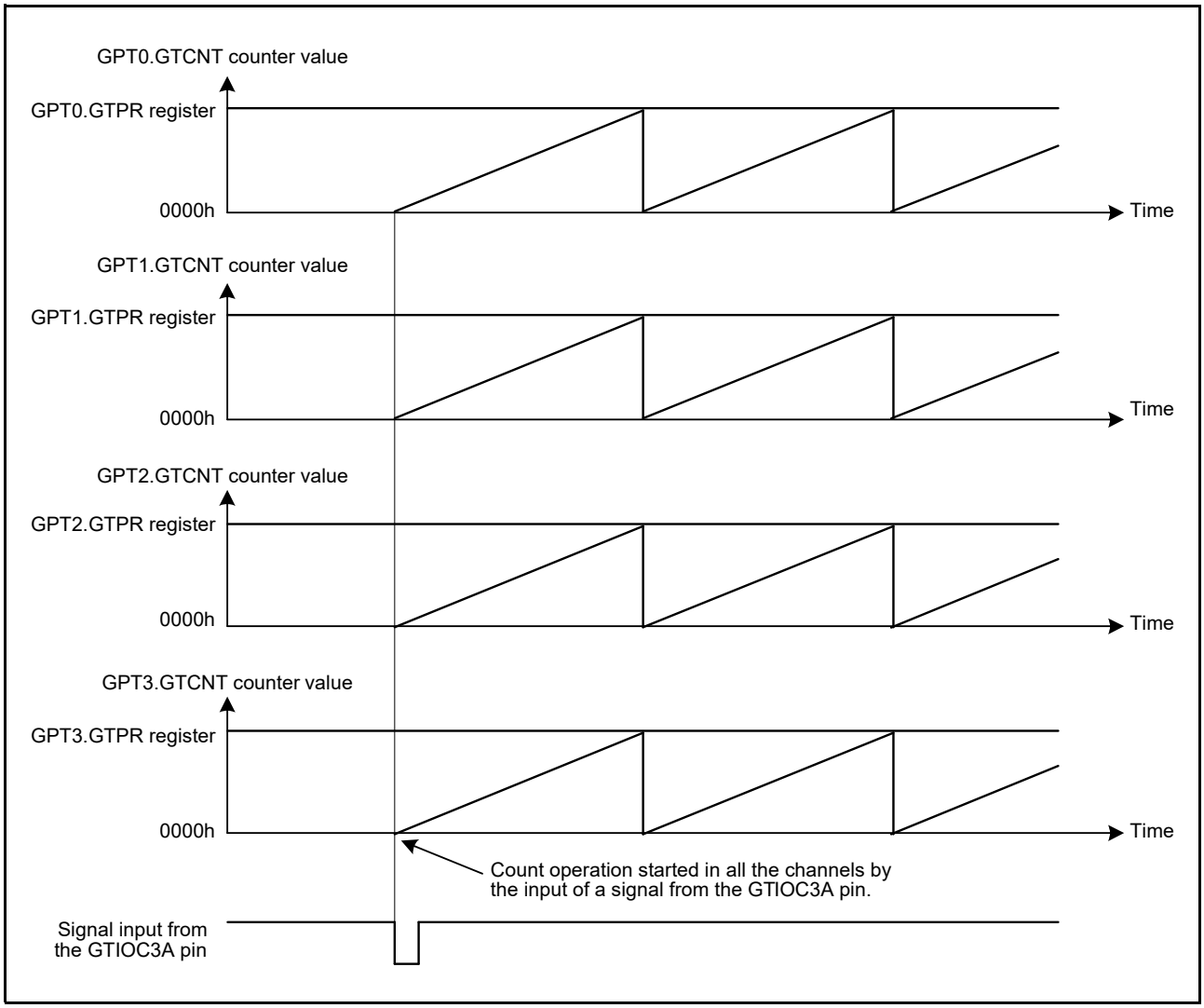


Figure 22.62 Example of Simultaneous Start Operation by Hardware Source (with Same Count Period (GTPR Value))

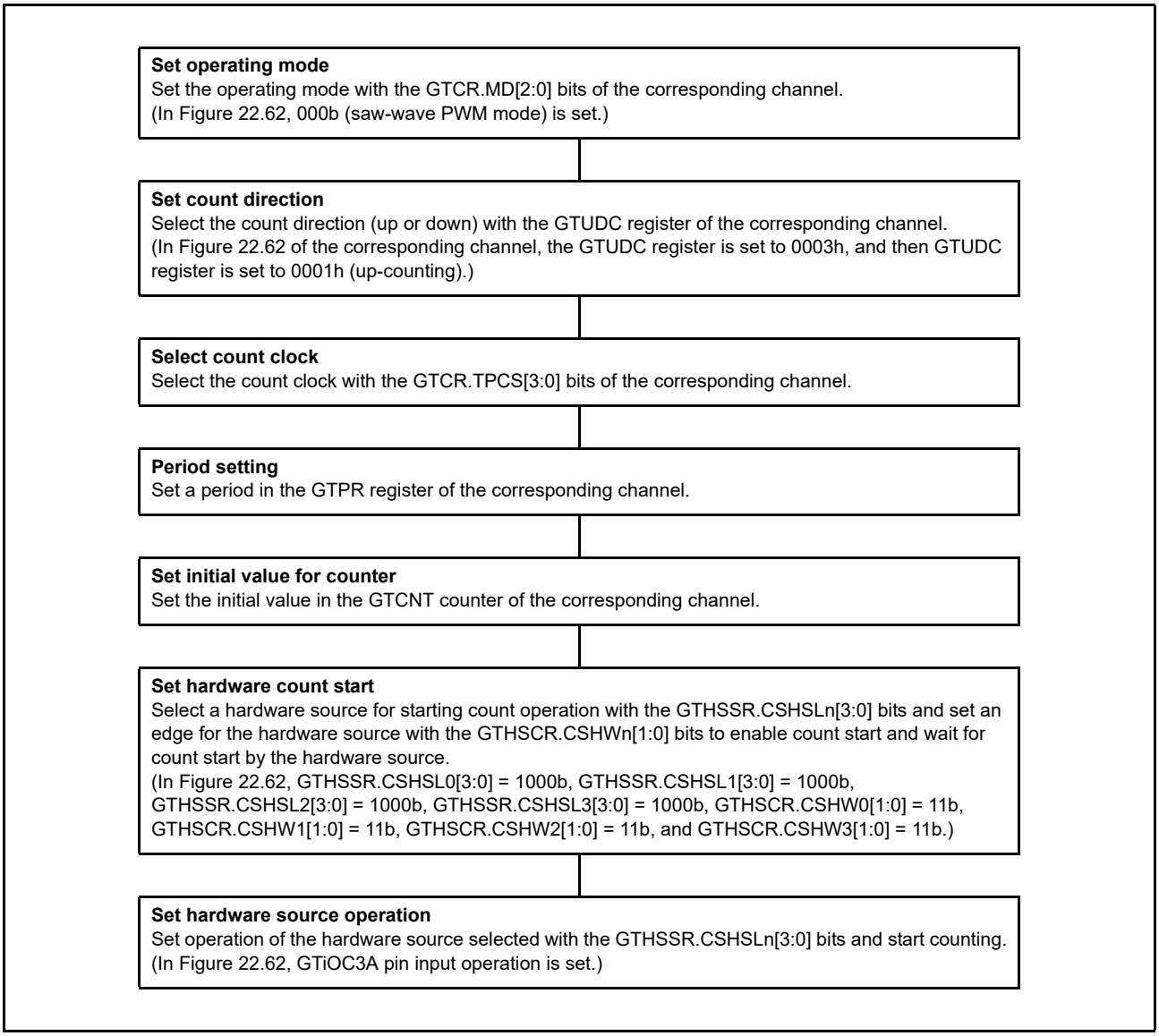


Figure 22.63 Example for Setting Simultaneous Start by Hardware Source

(4) Phase Shifting Start by Hardware Source

Count start with a phase difference is possible by following hardware sources: GTETRG pin input, comparator output, MTU count start (only count start control is enabled), GTIOC3A/GTIOC3B pin input, and GTIOC3A/GTIOC3B pin internal output (output compare).

Figure 22.64 shows an example of phase shifting start operation by a hardware source and Figure 22.65 shows the setting example. In this example, the GPT3.GTCNT and GPT0.GTCNT counters simultaneously start counting and the GPT1.GTCNT and GPT2.GTCNT counters start counting by the GTIOC3A and GTIOC3B pin internal outputs (output compare).

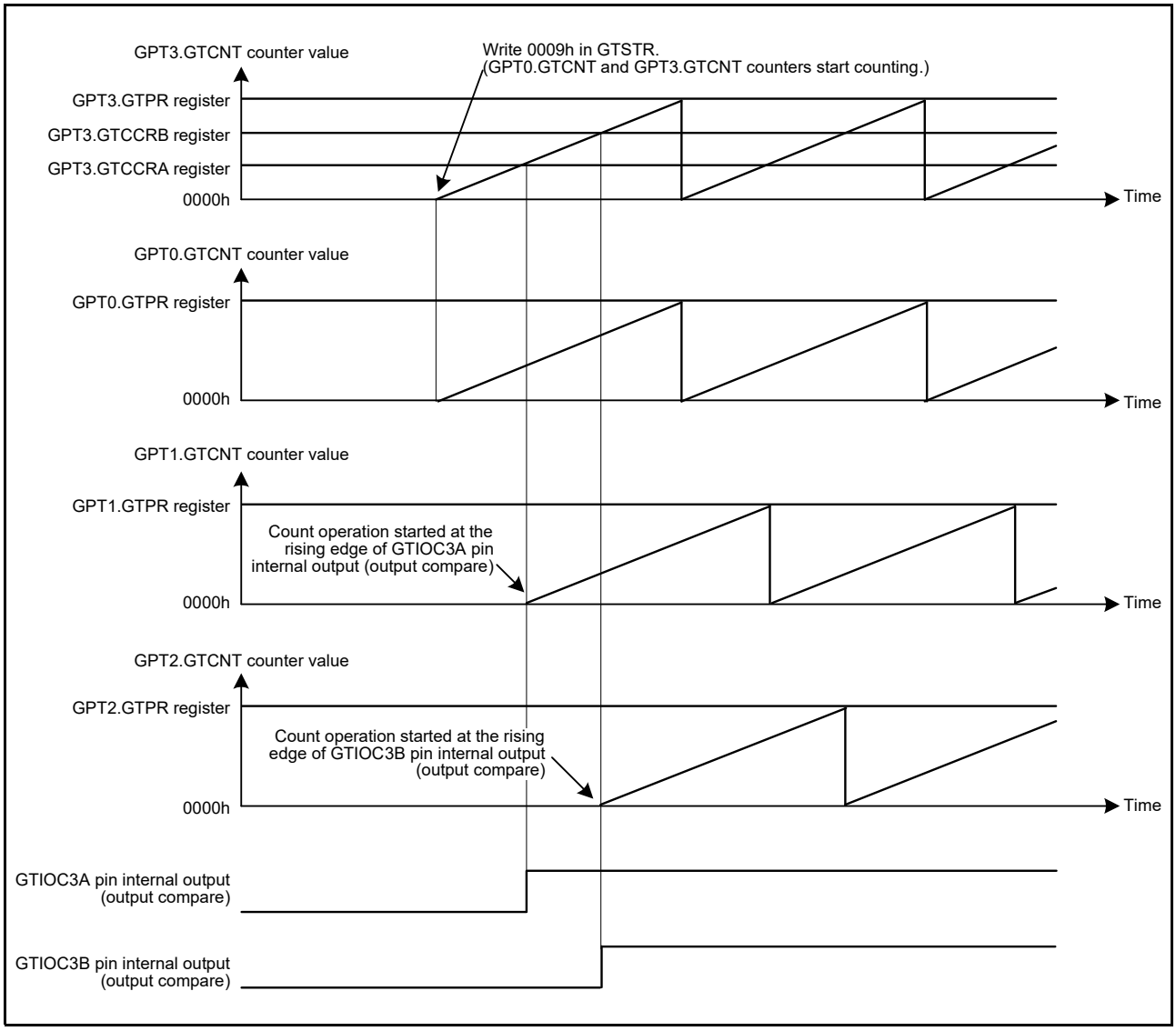


Figure 22.64 Example of Phase Shifting Start Operation by Hardware Source (with Same Count Period (GTPR Value))

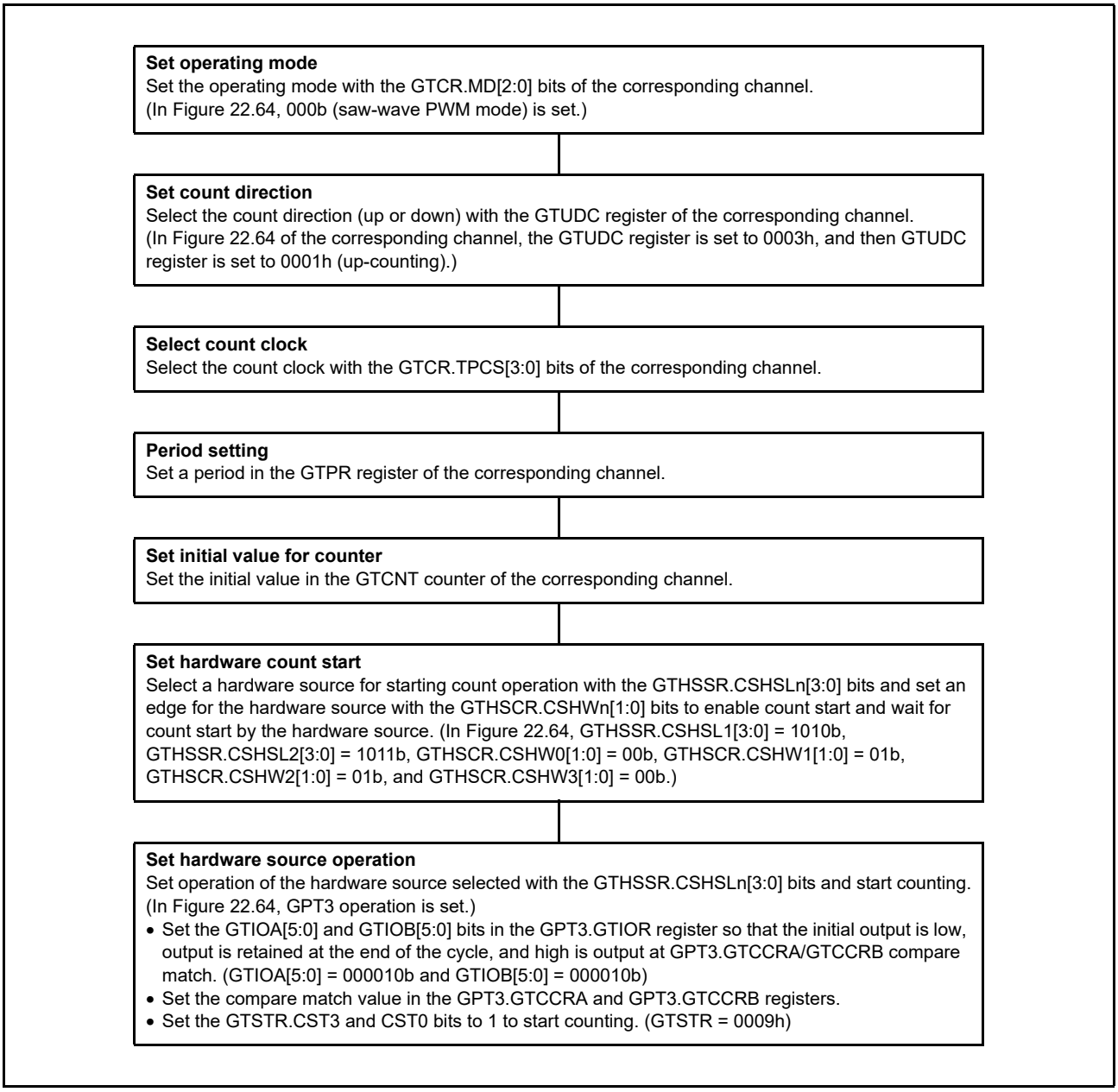


Figure 22.65 Example for Setting Phase Start by Hardware Source

22.3.9 PWM Output Operation Examples

(1) Synchronous PWM Output

The GPT can output eight phases of linked PWM waveforms for a maximum of four channels by synchronizing operation of the channels.

Figure 22.66 shows an example in which all the channels perform synchronous operation in saw-wave PWM mode and eight phases of PWM waveforms are output. The GTIOCnA pin is set so that it will output low as the initial output, high at a GTCCRA compare match, and low at the end of the cycle. The GTIOCnB pin is set so that it will output low as the initial output, high at a GTCCRB compare match, and low at the end of the cycle (n = 0 to 3).

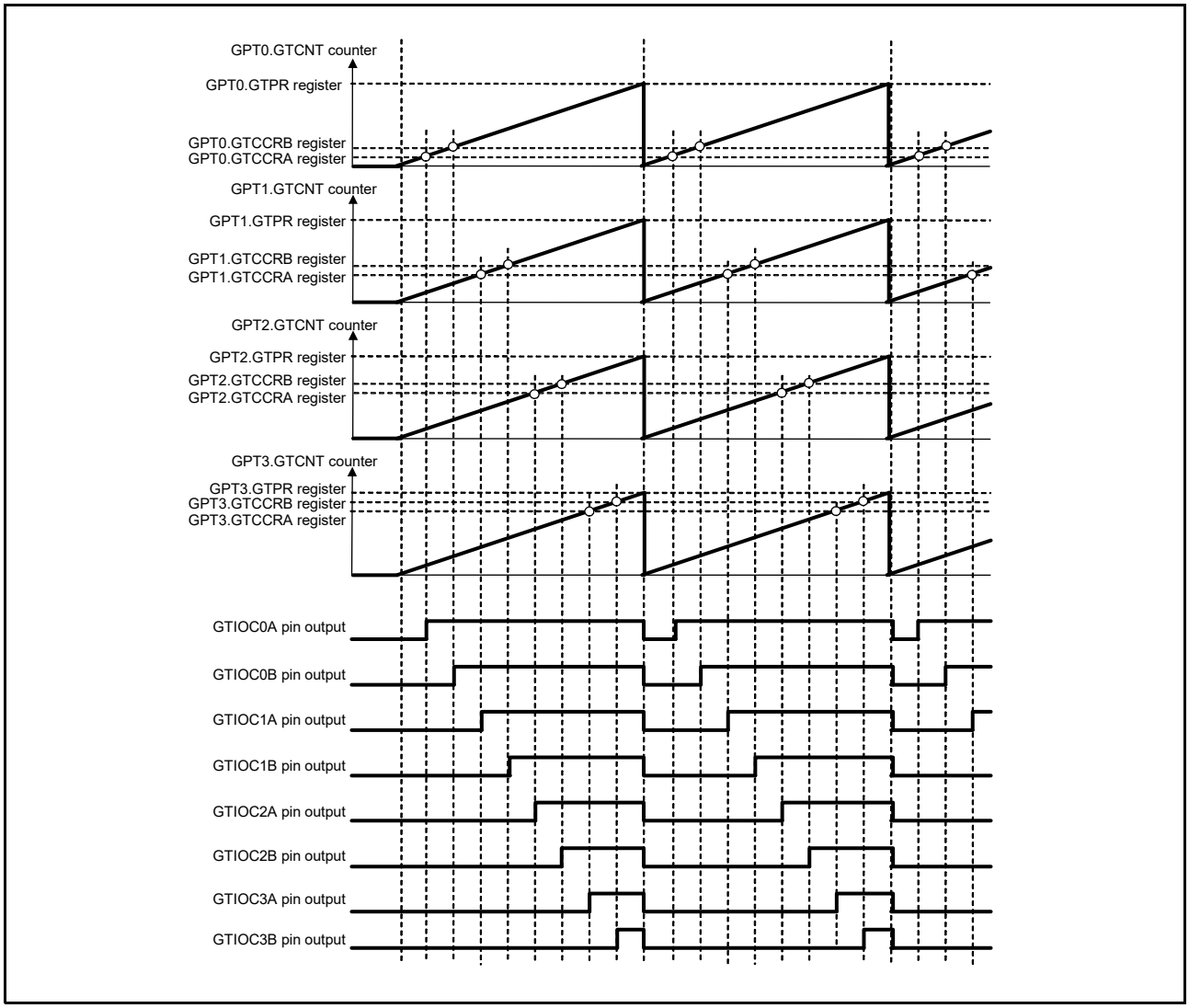


Figure 22.66 Example of Synchronous PWM Output

(2) Three-Phase Saw-Wave Complementary PWM Output

Figure 22.67 shows an example in which three channels perform synchronous operation in saw-wave PWM mode and three-phase complementary PWM waveforms are output. The GTIOCnA pin is set so that it will output low as the initial output, high at a GTCCRA compare match, and low at the end of the cycle. The GTIOCnB pin is set so that it will output high as the initial output, low at a GTCCRB compare match, and high at the end of the cycle.

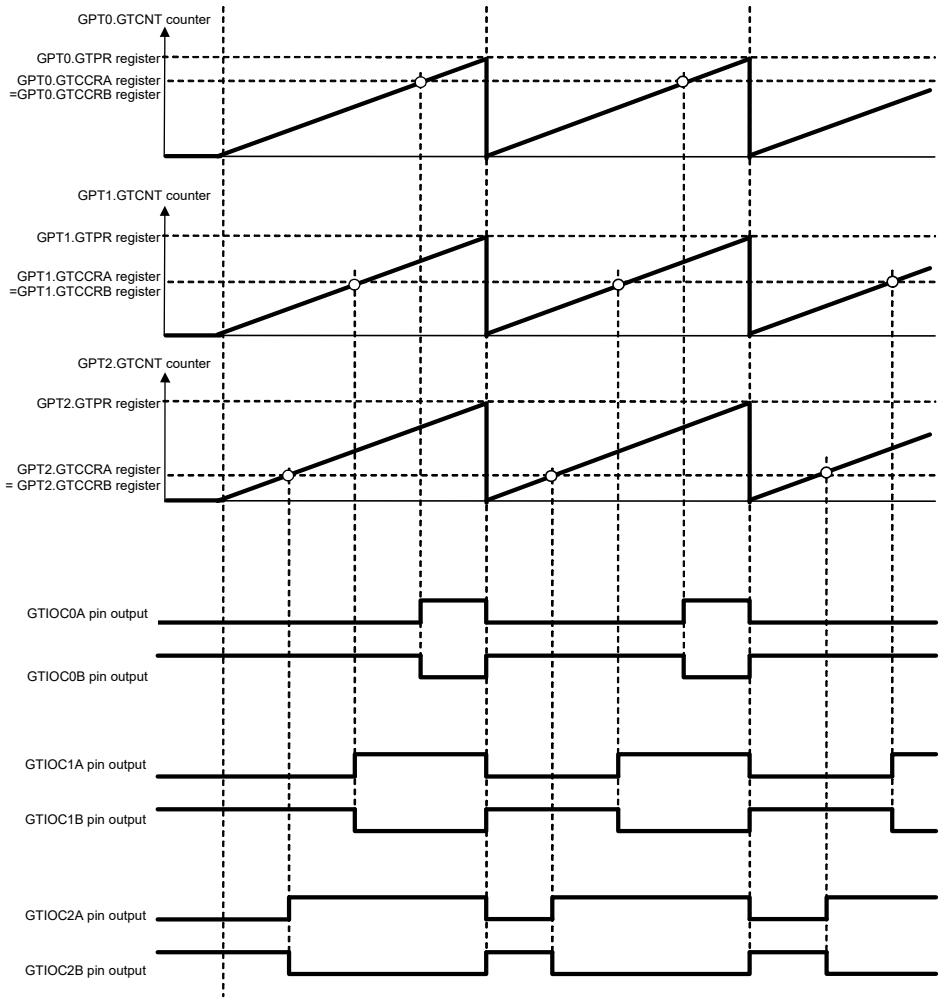


Figure 22.67 Example of Three-Phase Saw-Wave Complementary PWM Output

(3) Three-Phase Saw-Wave Complementary PWM Output with Automatic Dead Time Setting

Figure 22.68 shows an example in which three channels perform synchronous operation in saw-wave one-shot pulse mode with automatic dead time setting and three-phase complementary PWM waveforms are output. The GTIOCnA pin is set so that it will output low as the initial output, toggle the output at a GTCCRA compare match, and retain the output at the end of the cycle. The GTIOCnB pin is set so that it will output high as the initial output, toggle the output at a GTCCRB compare match, and retain the output at the end of the cycle.

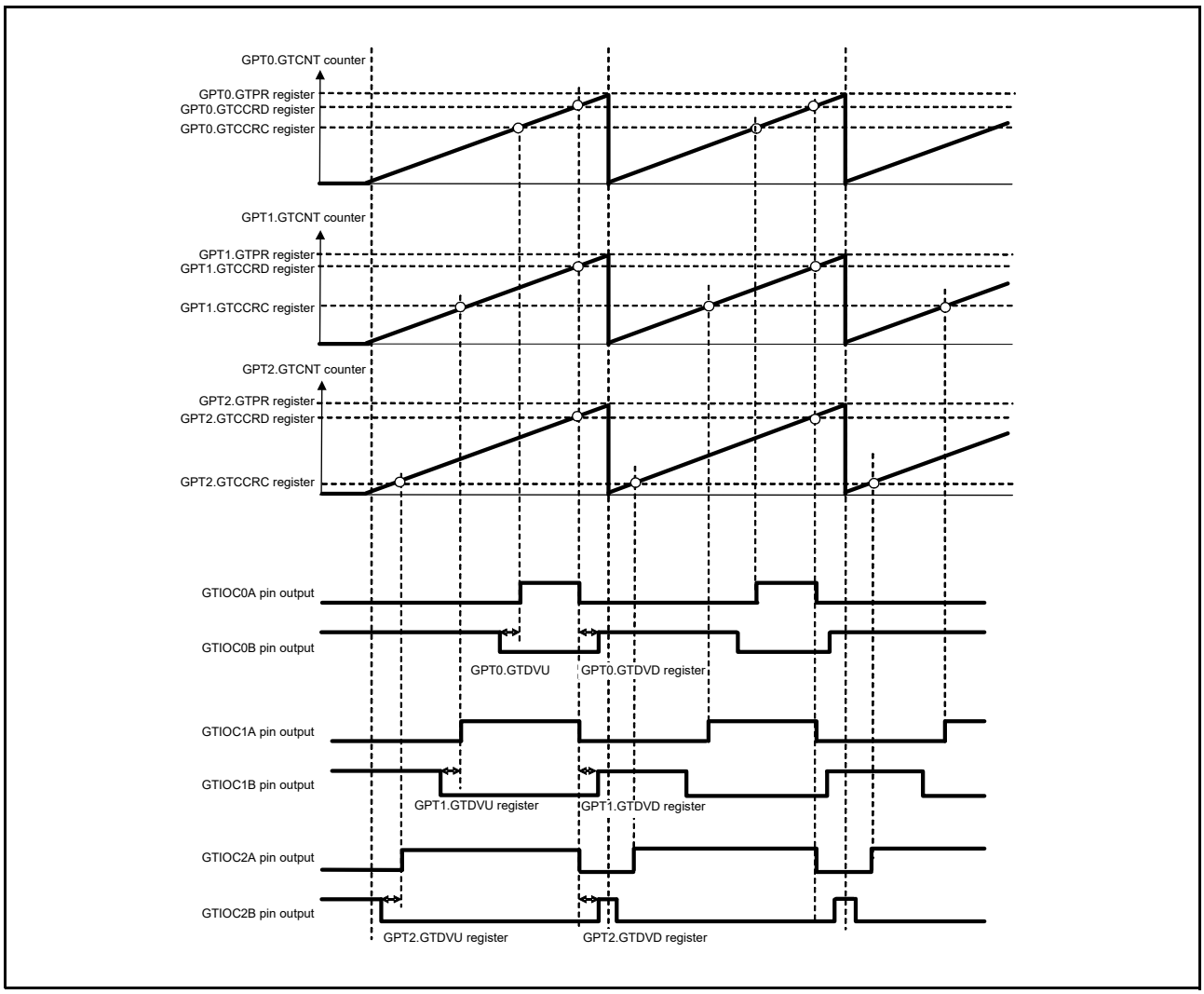


Figure 22.68 Example of Three-Phase Saw-Wave Complementary PWM Output with Automatic Dead Time Setting

(4) Three-Phase Triangle-Wave Complementary PWM Output

Figure 22.69 shows an example in which three channels perform synchronous operation in triangle-wave PWM mode 1 and three-phase complementary PWM waveforms are output. The GTIOCnA pin is set so that it will output low as the initial output, toggle the output at a GTCCRA compare match, and retain the output at the end of the cycle. The GTIOCnB pin is set so that it will output high as the initial output, toggle the output at a GTCCRB compare match, and retain the output at the end of the cycle.

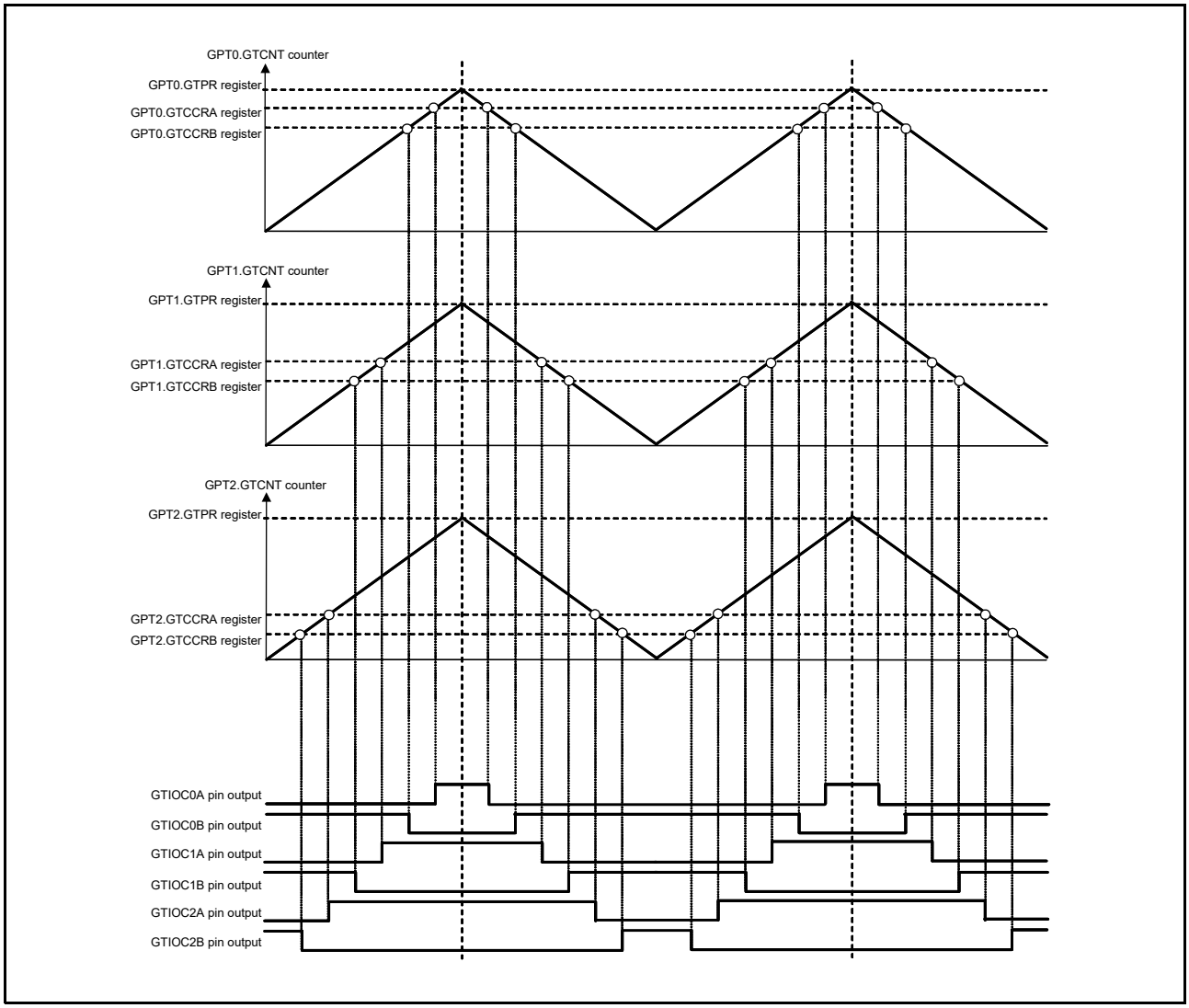


Figure 22.69 Example of Three-Phase Triangle-Wave Complementary PWM Output

(5) Three-Phase Triangle-Wave Complementary PWM Output with Automatic Dead Time Setting

Figure 22.70 shows an example in which three channels perform synchronous operation in triangle-wave PWM mode 1 with automatic dead time setting and three-phase complementary PWM waveforms are output. The GTIOCnA pin is set so that it will output low as the initial output, toggle the output at a GTCCRA compare match, and retain the output at the end of the cycle. The GTIOCnB pin is set so that it will output high as the initial output, toggle the output at a GTCCRB compare match, and retain the output at the end of the cycle.

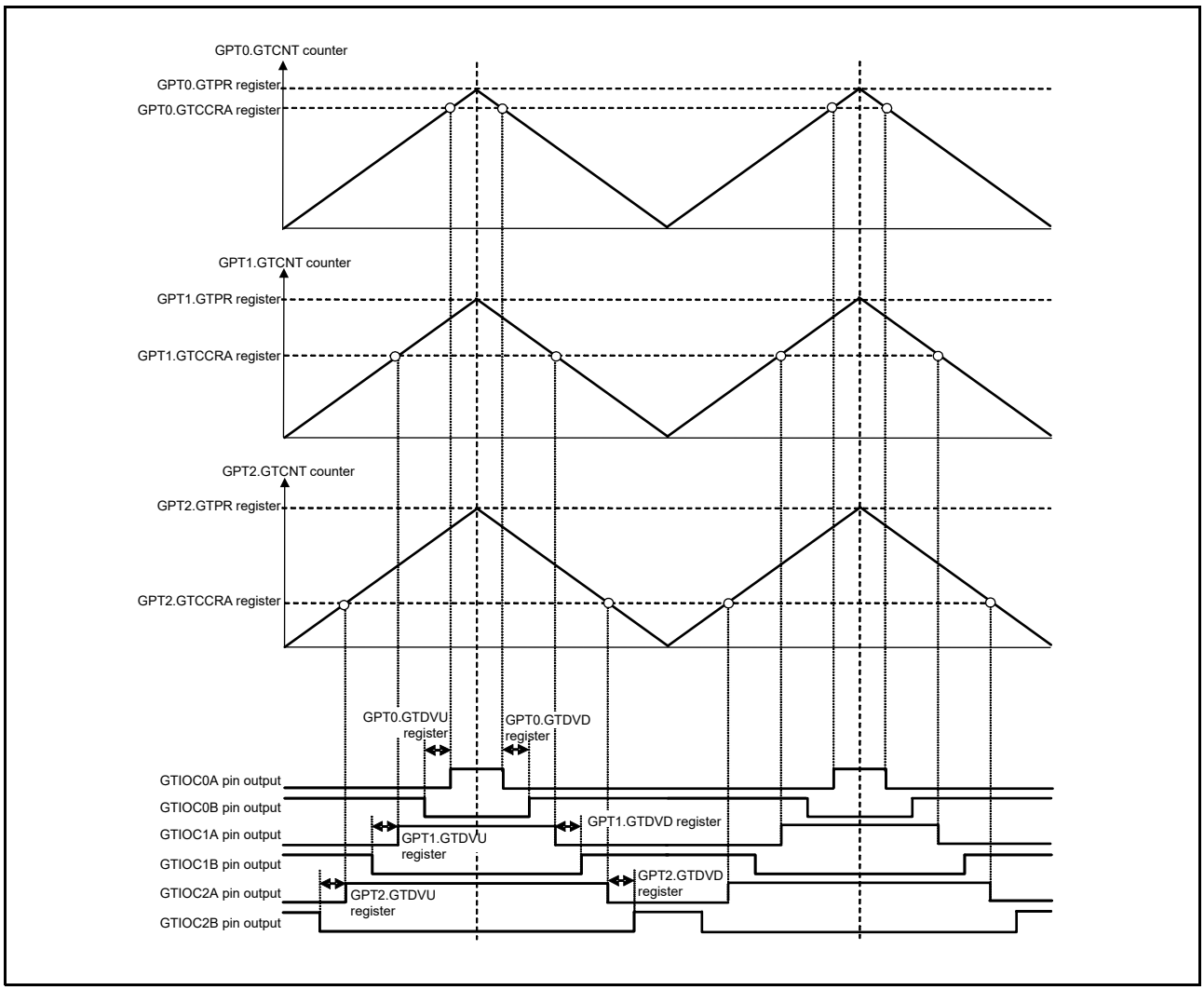


Figure 22.70 Example of Three-Phase Triangle-Wave Complementary PWM Output with Automatic Dead Time Setting

(6) Three-Phase Asymmetric Triangle-Wave Complementary PWM Output with Automatic Dead Time Setting

Figure 22.71 shows an example in which three channels perform synchronous operation in triangle-wave PWM mode 3 with automatic dead time setting and three-phase complementary PWM waveforms are output. The GTIOCnA is set so that it will output low as the initial output, toggle the output at a GTCCRA compare match, and retain the output at the end of the cycle. The GTIOCnB is set so that it will output high as the initial output, toggle the output at a GTCCRB compare match, and retain the output at the end of the cycle.

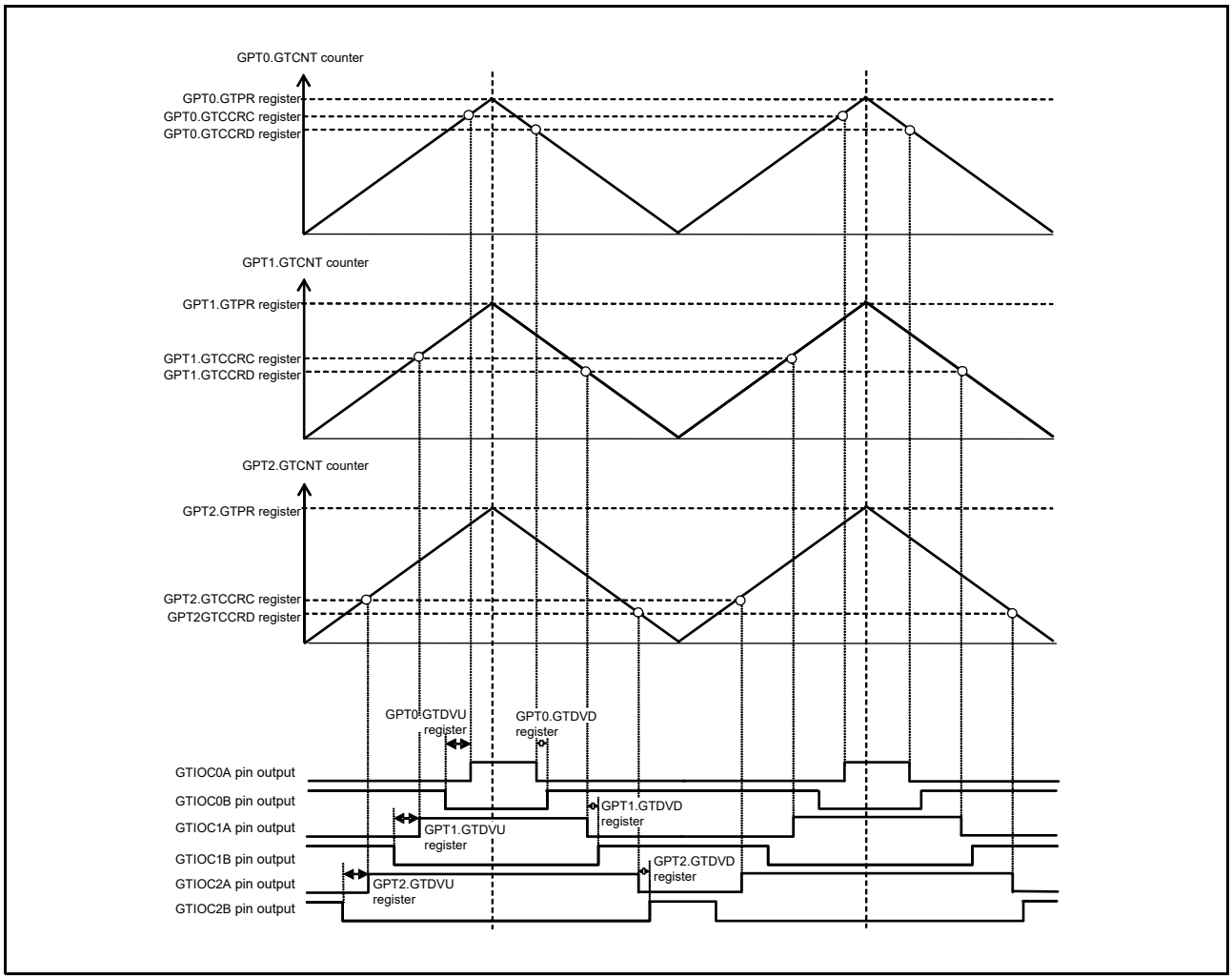


Figure 22.71 Example of Three-Phase Asymmetric Triangle-Wave Complementary PWM Output with Automatic Dead Time Setting

22.3.10 Noise Filter Function

Each pin for use in input capture, external trigger, and external clock input to the GPT is equipped with a noise filter. The noise filter samples input signals at the sampling clock and removes the pulses of which length is less than three sampling periods.

The noise filter functionality includes enabling and disabling of the noise filter for each pin and setting of the sampling clock for each channel. The NFCR register can be used to set the GTIOCnA and GTIOCnB pins. The GTETINT register can be used to set the GTETRG pin. The GTENFCR register can be used to set the GETCLKx pins (x = A to D).

Figure 22.72 shows the timing of noise filtering.

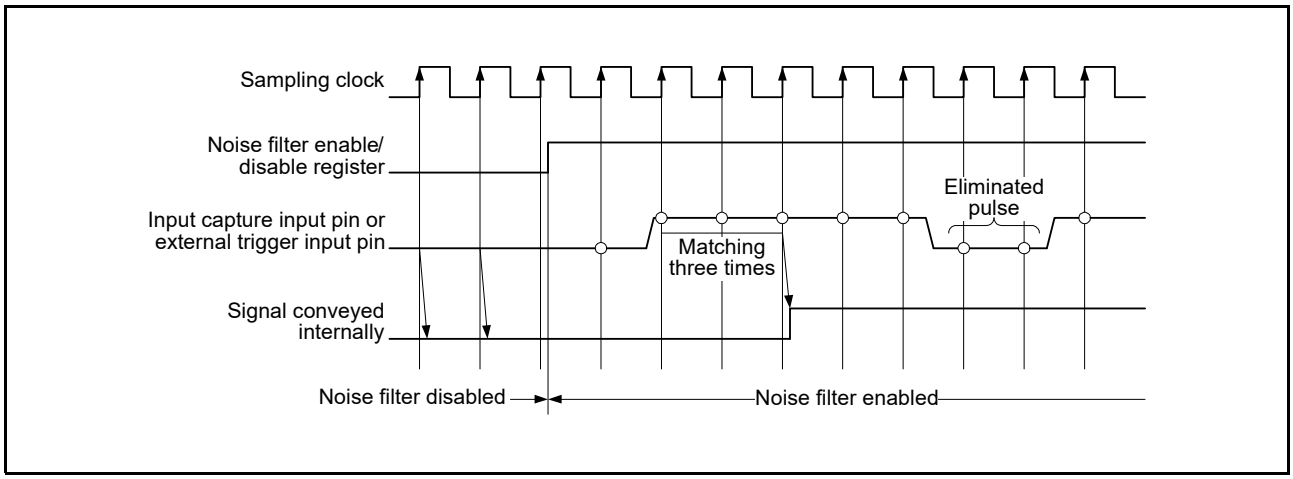


Figure 22.72 Timing of Noise Filtering

If noise filtering is enabled, input capture operation or external trigger operation is performed on the edges of noise-filtered signal after a delay of (minimum sampling interval × 2 + PCLKA) due to noise filtering for the input capture input or external trigger operation.

22.4 Interrupt Sources

22.4.1 Interrupt Sources and Priorities

Table 22.9 lists the interrupt sources.

Each interrupt source has a control bit for the respective dedicated interrupt request generation and enables or disables the generation of interrupt request independently.

The priority of channels can be changed by the interrupt controller settings. For details, see section 14, Interrupt Controller (ICUb).

Table 22.9 GPT Interrupt Sources

Channel	Name	Interrupt Source	DTC Activation
Common	ETGIN	External trigger falling input	Impossible
	ETGIP	External trigger rising input	Impossible
GPT0	GTCIA0	GPT0.GTCCRA input capture/compare match	Possible
	GTCIB0	GPT0.GTCCRB input capture/compare match	Possible
	GTCIC0	GPT0.GTCCRC compare match	Possible
	GTCID0	GPT0.GTCCRD compare match	Possible
	GDTE0	Dead time error	Impossible
	GTCIE0	GPT0.GTCCRE compare match	Possible
	GTCIF0	GPT0.GTCCRF compare match	Possible
	GTCIV0	GPT0.GTCNT overflow (GPT0.GTPR compare match)	Possible
	GTCIU0	GPT0.GTCNT underflow	Possible
GPT1 (GPT01)	GTCIA1	GPT1.GTCCRA (GPT01.GTCCRALW) input capture/compare match	Possible
	GTCIB1	GPT1.GTCCRB (GPT01.GTCCRBLW) input capture/compare match	Possible
	GTCIC1	GPT1.GTCCRC (GPT01.GTCCRCLW) compare match	Possible
	GTCID1	GPT1.GTCCRD (GPT01.GTCCRDLW) compare match	Possible
	GDTE1	Dead time error	Impossible
	GTCIE1	GPT1.GTCCRE (GPT01.GTCCRELW) compare match	Possible
	GTCIF1	GPT1.GTCCRF (GPT01.GTCCRFLW) compare match	Possible
	GTCIV1	GPT1.GTCNT (GPT01.GTCNTLW) overflow (GPT1.GTPR (GPT01.GTPRLW) compare match)	Possible
	GTCIU1	GPT1.GTCNT (GPT01.GTCNTLW) underflow	Possible
GPT2	GTCIA2	GPT2.GTCCRA input capture/compare match	Possible
	GTCIB2	GPT2.GTCCRB input capture/compare match	Possible
	GTCIC2	GPT2.GTCCRC compare match	Possible
	GTCID2	GPT2.GTCCRD compare match	Possible
	GDTE2	Dead time error	Impossible
	GTCIE2	GPT2.GTCCRE compare match	Possible
	GTCIF2	GPT2.GTCCRF compare match	Possible
	GTCIV2	GPT2.GTCNT overflow (GPT2.GTPR compare match)	Possible
	GTCIU2	GPT2.GTCNT underflow	Possible
GPT3 (GPT23)	GTCIA3	GPT3.GTCCRA (GPT23.GTCCRALW) input capture/compare match	Possible
	GTCIB3	GPT3.GTCCRB (GPT23.GTCCRBLW) input capture/compare match	Possible
	GTCIC3	GPT3.GTCCRC (GPT23.GTCCRCLW) compare match	Possible
	GTCID3	GPT3.GTCCRD (GPT23.GTCCRDLW) compare match	Possible
	GDTE3	Dead time error	Impossible
	GTCIE3	GPT3.GTCCRE (GPT23.GTCCRELW) compare match	Possible
	GTCIF3	GPT3.GTCCRF (GPT23.GTCCRFLW) compare match	Possible
	GTCIV3	GPT3.GTCNT (GPT23.GTCNTLW) overflow (GPT3.GTPR (GPT23.GTPRLW) compare match)	Possible
	GTCIU3	GPT3.GTCNT (GPT23.GTCNTLW) underflow	Possible

(1) GTCIAn interrupt (n = 0 to 3)

When the GTINTAD.GTINTA bit is 1, an interrupt request is generated under the following conditions.

- When the GTCCRA(LW) register functions as a compare match register, the GTCNT(LW) counter value matches with the GTCCRA(LW) register.
- When the GTCCRA(LW) register functions as an input capture register, the input-capture signal has caused transfer of the GTCNT(LW) counter value to the GTCCRA(LW) register.

(2) GTCIBn interrupt (n = 0 to 3)

When the GTINTAD.GTINTB bit is 1, an interrupt request is generated under the following conditions.

- When the GTCCRB(LW) register functions as a compare match register, the GTCNT(LW) counter value matches with the GTCCRB(LW) register.
- When the GTCCRB(LW) register functions as an input capture register, the input-capture signal has caused transfer of the GTCNT(LW) counter value to the GTCCRB(LW) register.

(3) GTCICn interrupt (n = 0 to 3)

When the GTINTAD.GTINTC bit is 1, an interrupt request is generated under the following condition.

- When the GTCCRC(LW) register functions as a compare match register, the GTCNT(LW) counter value matches with the GTCCRC(LW) register.

A compare match is not performed and thus interrupt is not requested under the following conditions.

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0] = 01b, 10b, 11b (buffer operation with the GTCCRC(LW) register)

(4) GTCIDn interrupt (n = 0 to 3)

When the GTINTAD.GTINTD bit is 1, an interrupt request is generated under the following condition.

- When the GTCCRD(LW) register functions as a compare match register, the GTCNT(LW) counter value matches with the GTCCRD(LW) register.

A compare match is not performed and thus interrupt is not requested under the following conditions.

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0] = 10b, 11b (buffer operation with the GTCCRD(LW) register)

(5) GTCIEn interrupt (n = 0 to 3)

When the GTINTAD.GTINTE bit is 1, an interrupt request is generated under the following condition.

- When the GTCCRE(LW) register functions as a compare match register, the GTCNT(LW) counter value matches with the GTCCRE(LW) register.

A compare match is not performed and thus interrupt is not requested under the following conditions.

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRB[1:0] = 01b, 10b, 11b (buffer operation with the GTCCRE(LW) register)

(6) GTCIFn interrupt (n = 0 to 3)

When the GTINTAD.GTINTF bit is 1, an interrupt request is generated under the following condition.

- When the GTCCRF(LW) register functions as a compare match register, the GTCNT(LW) counter value matches with the GTCCRF(LW) register.

A compare match is not performed and thus interrupt is not requested under the following conditions.

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRB[1:0] = 10b, 11b (buffer operation with the GTCCRF(LW) register)

(7) GTCIVn interrupt (n = 0 to 3)

When the GTINTAD.GTINTPR[0] bit is 1, an interrupt request is generated under the following conditions.

- In saw-wave mode, interrupt requests are enabled at overflows (GTCNT(LW) counter value changes from GTPR(LW) register value to 0000h (0000 0000h) during up-counting).
- In triangle-wave mode, interrupt requests are enabled at crests (GTCNT(LW) counter value changes from GTPR(LW) register value to GTPR(LW) register value minus 1).

(8) GTCIUn interrupt (n = 0 to 3)

When the GTINTAD.GTINTPR[1] bit is 1, an interrupt request is generated under the following conditions.

- In saw-wave mode, interrupt requests are enabled at underflows (GTCNT(LW) counter value changes from 0000h (0000 0000h) to GTPR(LW) register value during down-counting).
- In triangle-wave mode, interrupt requests are enabled at troughs (GTCNT(LW) counter value changes from 0000h (0000 0000h) to 0001h (0000 0001h)).

(9) ETGIP interrupt

When the GTETINT.ETIPEN bit is 1, an interrupt request is generated under the following condition.

- When the rising edge of an external trigger input is detected

(10) ETGIN interrupt

When the GTETINT.ETINEN bit is 1, an interrupt request is generated under the following condition.

- When the falling edge of an external trigger input is detected

(11) GDTEn interrupt (n = 0 to 3)

When automatic dead time setting has been made, the GTST.DTEF flag becomes 1 when the timer output toggle point with dead time added exceeds the count period. If GTINTAD.EINT is 1 at this time, a dead time error interrupt request (GDTE) is generated.

In addition, when the timer output toggle point with dead time added is back within the count period, the GTST.DTEF flag changes from 1 to 0.

22.4.2 DTC Activation

The DTC can be triggered by the interrupt request in each channel. For details, see section 14, Interrupt Controller (ICUb) and section 17, Data Transfer Controller (DTCa).

22.4.3 Interrupt and A/D Conversion Request Skipping Function

By setting the GTITC register, the GTCNT(LW) counter overflow (GTPR(LW) compare match) interrupt (GTCIV) and underflow interrupt (GTCIU) can be skipped. Other interrupts and A/D converter start request signals can be skipped in coordination with the GTCIV/GTCIU skipping function. However, the dead time error interrupts cannot be linked with the GTCIV/GTCIU skipping function.

When both troughs and crests are counted and skipped in triangle-wave mode, if the number of times of skipping is odd, GTCIV/GTCIU interrupt requests cannot be generated at troughs only or at crests only depending on the skipping counter start timing. Therefore, in order to count both troughs and crests and generate the GTCIV/GTCIU interrupts at troughs only or crests only in triangle-wave mode, the number of times of skipping should be even.

Similarly, in saw-wave mode, when both overflows and underflows are counted and skipped with the count direction changed, GTCIV/GTCIU interrupt requests cannot be generated at overflows only or at underflows only. Therefore, in order to count both overflows and underflows with the count direction changed and generate the GTCIV/GTCIU interrupts at overflows only or underflows only in saw wave mode, the skipping state should be carefully checked before using.

When changing the skipping count, be sure to release the skipping count setting (GTITC.IVTC[1:0] bits = 00b).

Figure 22.73 to Figure 22.78 show examples of skipping function operation.

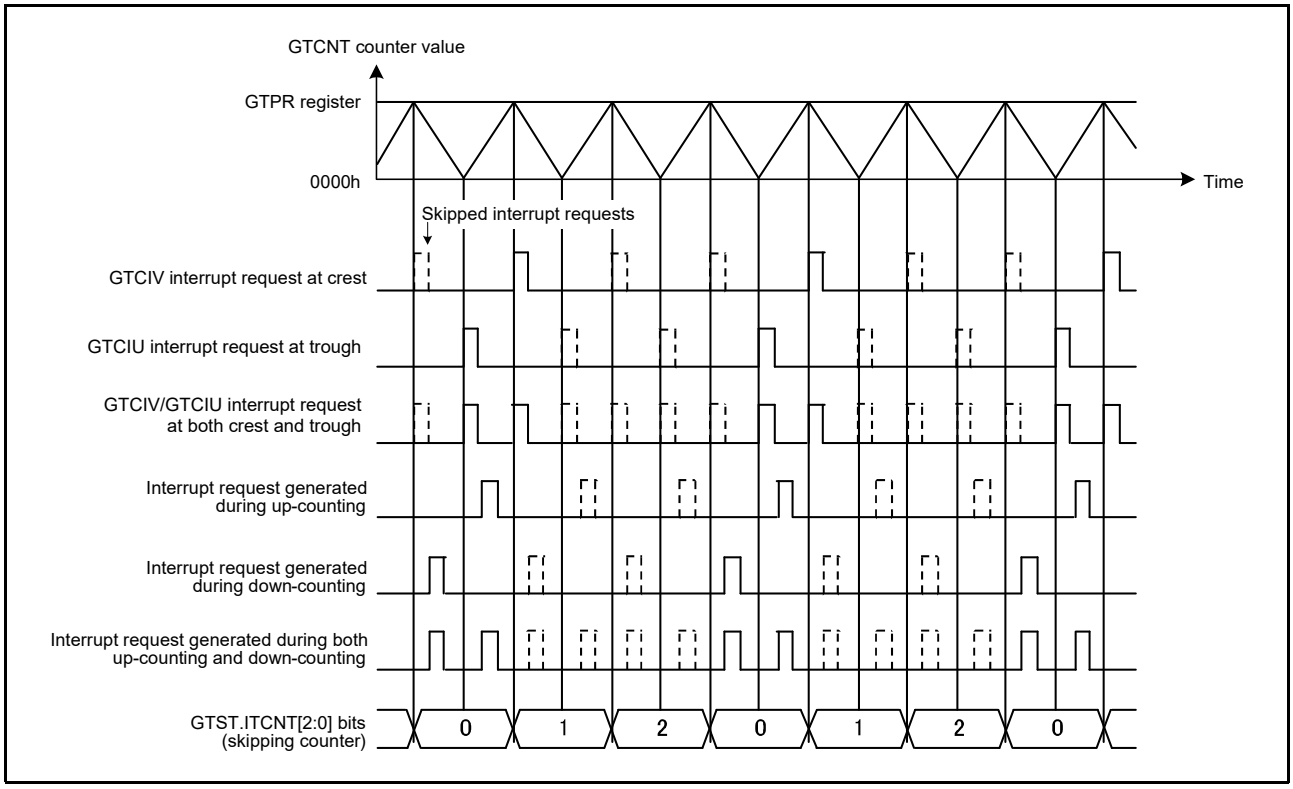


Figure 22.73 Example of Interrupt Skipping Function Operation (Triangle Waves, Counting and Skipping Crests, Skipping Count: 2)

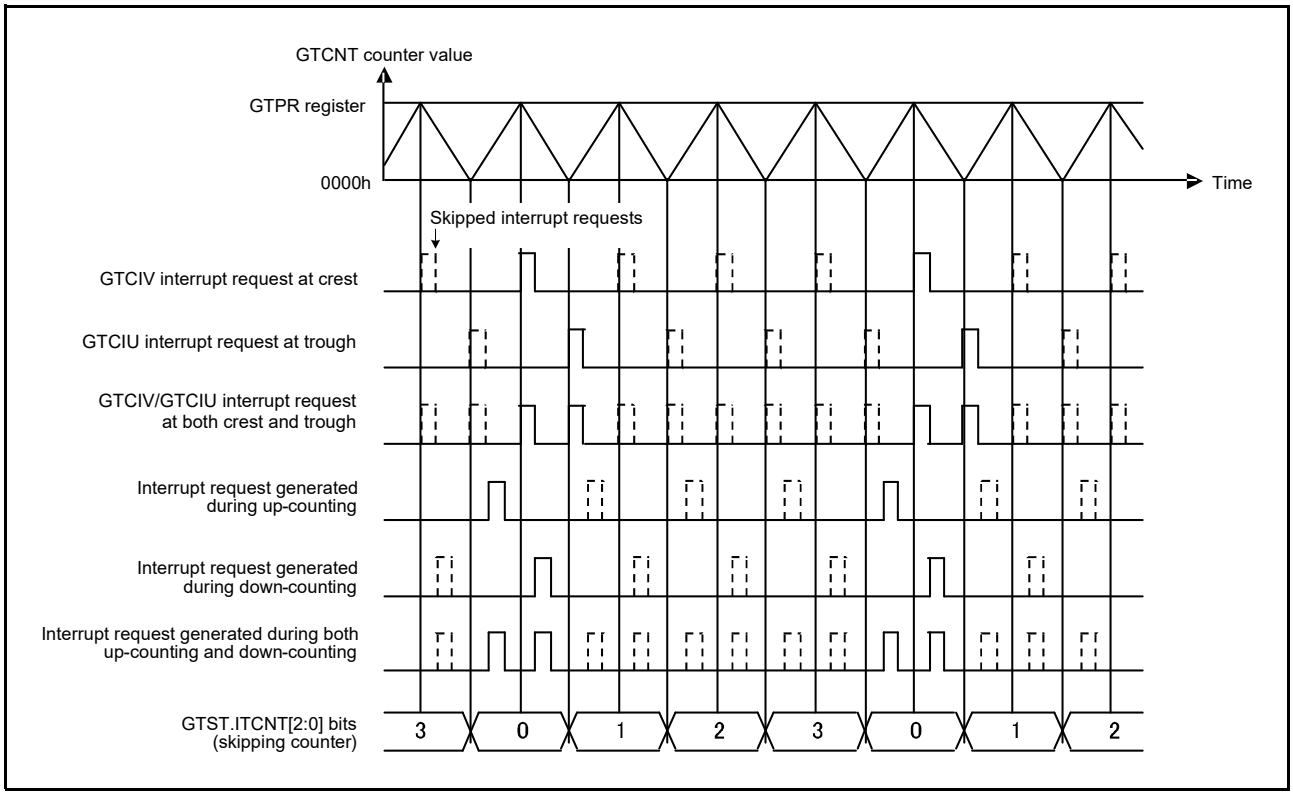


Figure 22.74 Example of Interrupt Skipping Function Operation (Triangle Waves, Counting and Skipping Troughs, Skipping Count: 3)

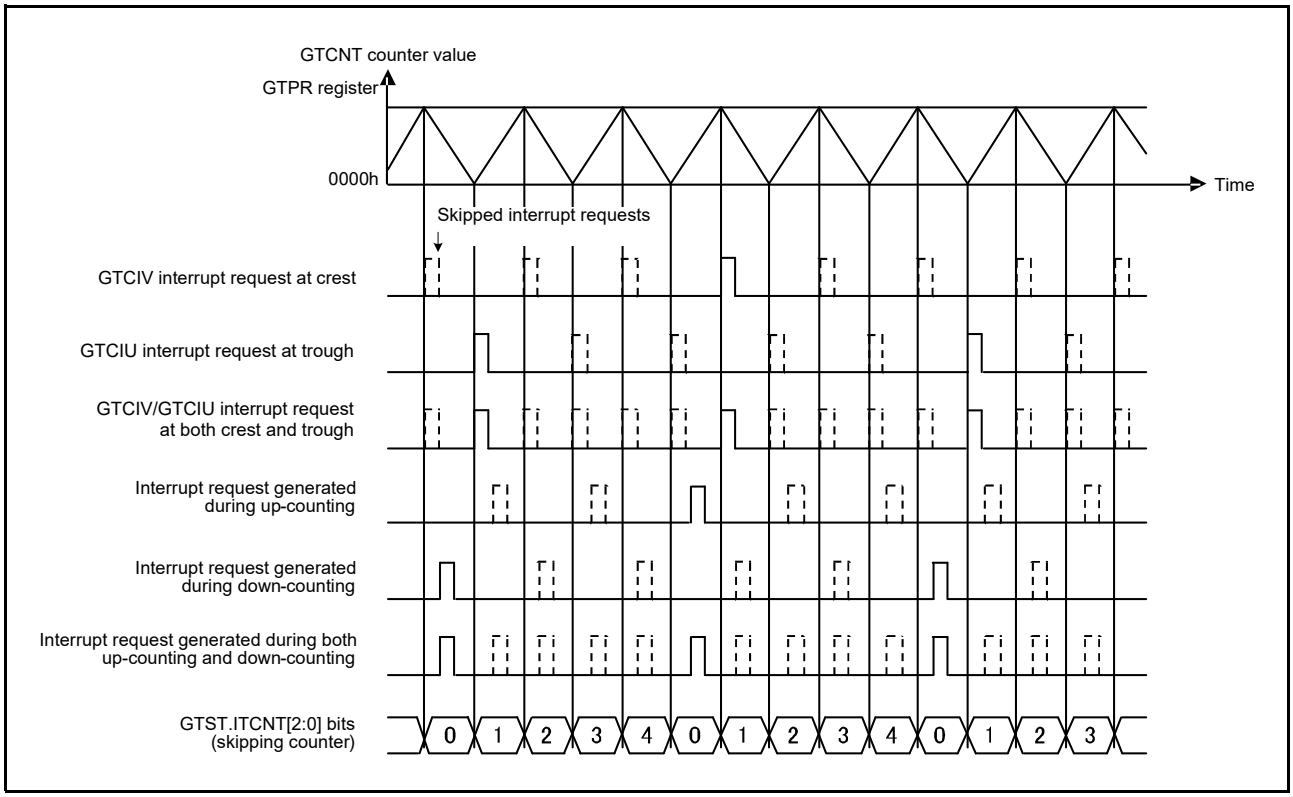


Figure 22.75 Example of Interrupt Skipping Function Operation (Triangle Waves, Counting and Skipping Both Troughs and Crests, Skipping Count: 4)

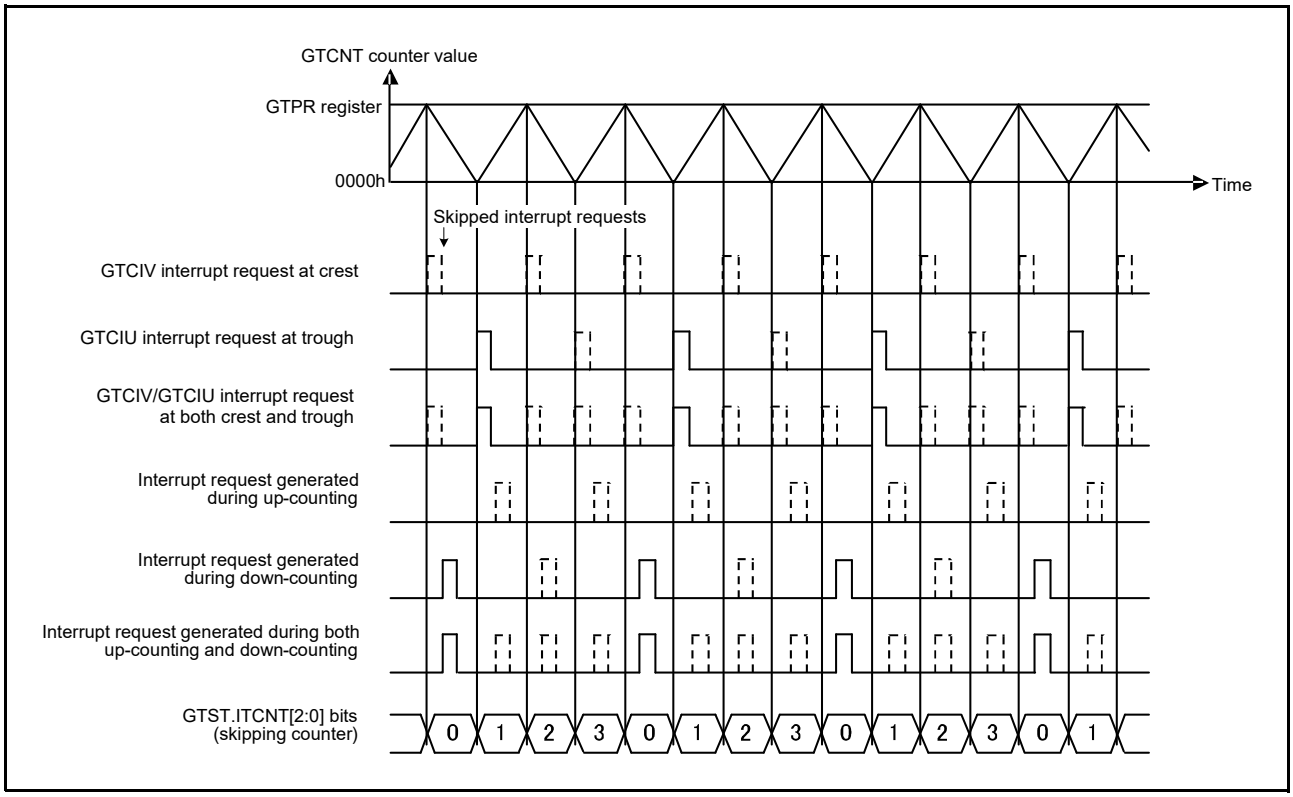


Figure 22.76 Example of Interrupt Skipping Function Operation (Triangle Waves, Counting and Skipping Both Troughs and Crests, Skipping Count: 3, Skipping Started at Up-Counting)

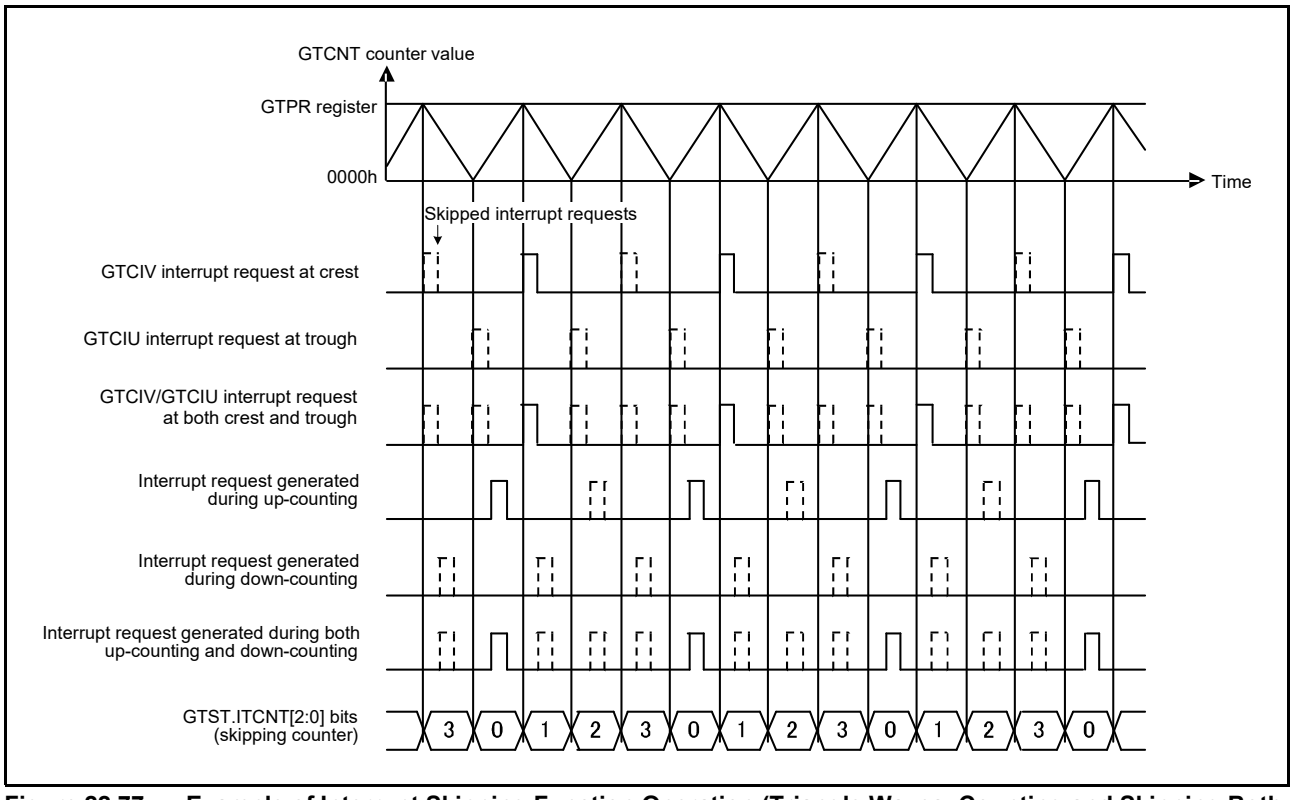


Figure 22.77 Example of Interrupt Skipping Function Operation (Triangle Waves, Counting and Skipping Both Troughs and Crests, Skipping Count: 3, Skipping Started at Down-Counting)

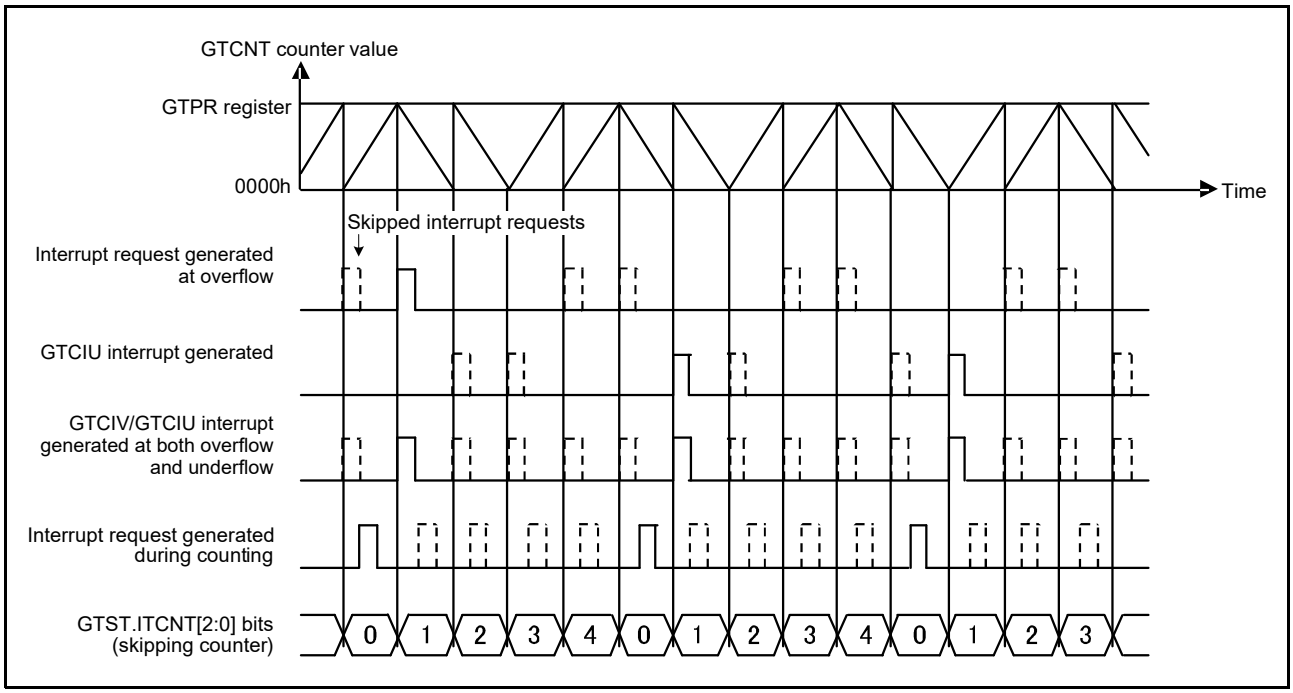


Figure 22.78 Example of Interrupt Skipping Function Operation (Saw Waves, Operation with Count Direction Changed, Counting and Skipping Both Overflows and Underflows, Skipping Count: 4)

22.5 A/D Converter Start Request

An A/D converter start request can be issued at a compare match between the GTCNT(LW) counter and the GTADTRA(LW) or GTADTRB(LW) register, up-counting only, down-counting only, or both up-counting and down-counting can be specified by setting the GTINTAD register.

The GTADTRA(LW) and GTADTRB(LW) registers each has two buffer registers. Buffer operation with the GTADTRA(LW) register used together with the GTADTBRA(LW) and GTADTDBRA(LW) registers, and buffer operation with the GTADTRB register used together with the GTADTBRB(LW) and GTADTDBRB(LW) registers can be performed.

The timing of the generation of requests to start A/D conversion can be monitored by an external pin. When the A/D conversion request signal to be monitored is selected by the GTADSMR.ADSMSk bit (k = 0, 1) and the output is enabled by the GTADSMR.ADSMENk pin, the output on the GTADSMk pin goes to the high level when the request signal is generated, and to the low level when the period of the timer used to generate the request signals has ended, leading to the output of a signal synchronized by the synchronizing frame of the timer. When a signal to request the start of A/D conversion is generated at the end of the cycle, the generation of this signal has priority in terms of monitoring output and the output remains at the high level till the end of the next cycle.

Figure 22.79 shows an example of A/D converter start request operation, and Figure 22.80 shows an example for setting A/D converter start request operation.

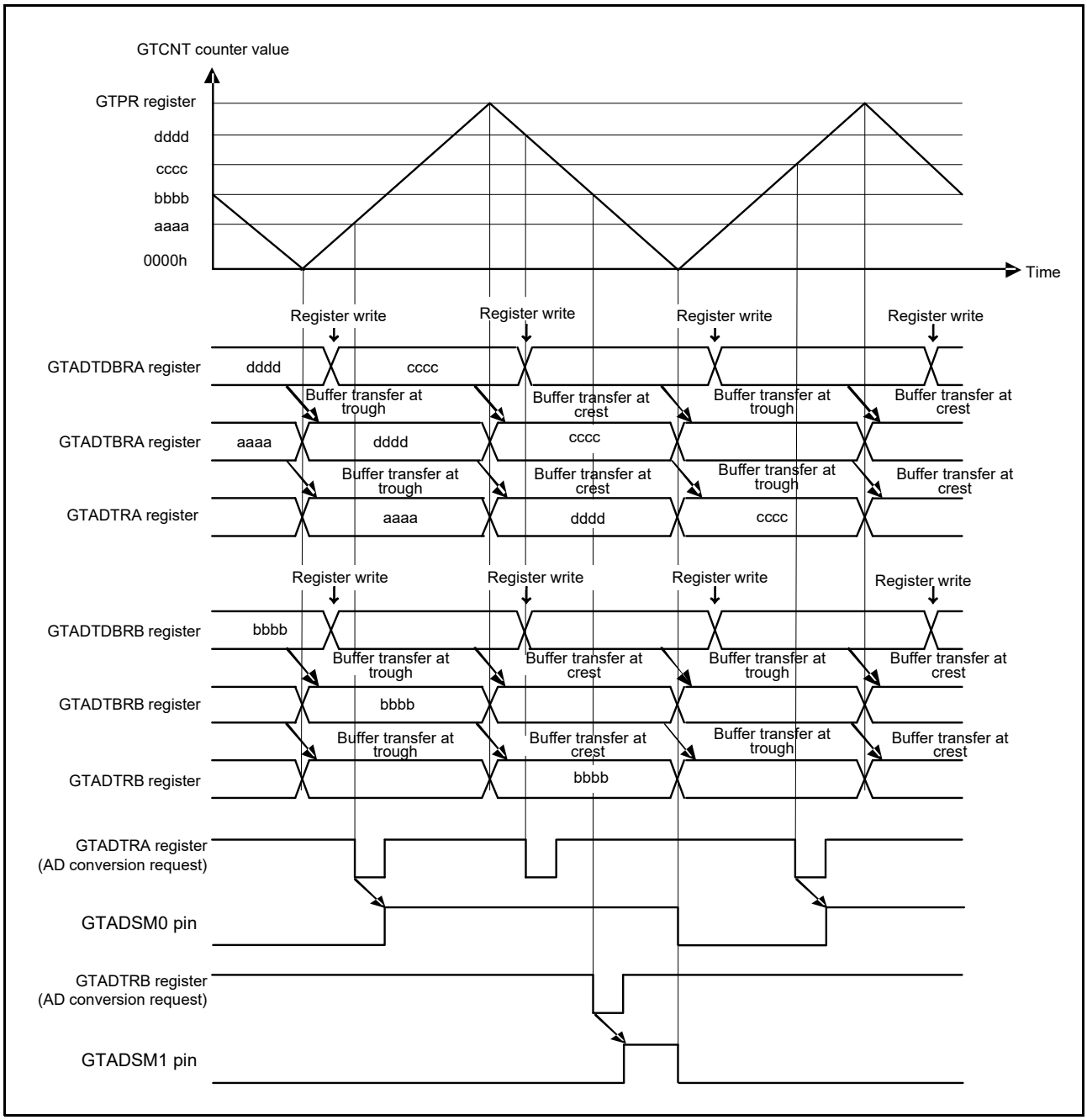


Figure 22.79 Example of A/D Converter Start Request Timing Operation (Triangle Waves, Double Buffer Operation, Buffer Transfer at Both Troughs and Crests, A/D Converter Start Requested by GTADTRA0 at Both Up-Counting and Down-Counting, A/D Converter Start Requested by GTADTRB0 at Down-Counting)

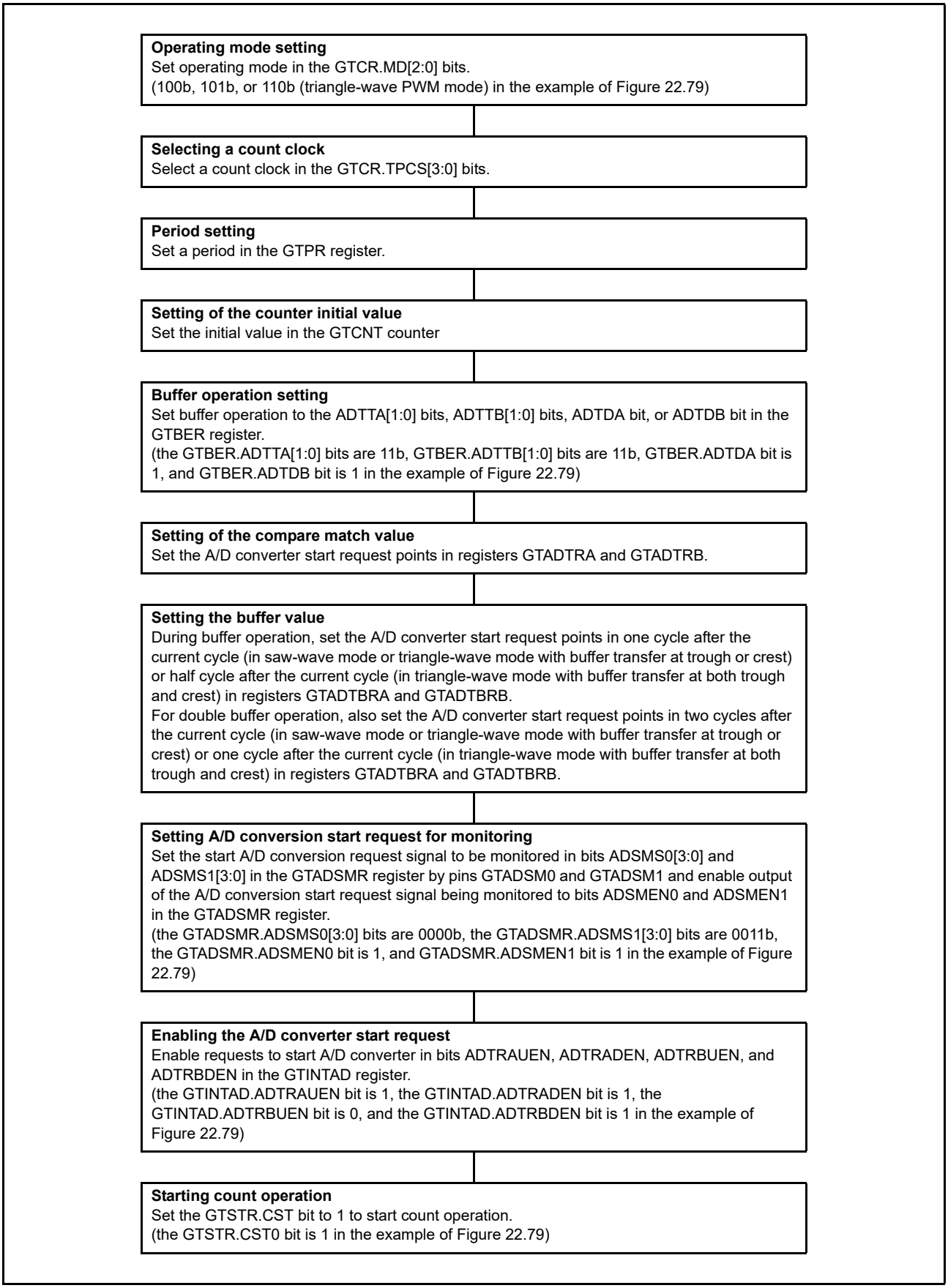


Figure 22.80 Example for Setting A/D Converter Start Request Timing Operation

22.6 Protection Function

22.6.1 Write-Protection for Registers

22.6.1.1 Write-Protection for Common Registers

Setting the GTCMNWP.CMNWP bit disables writing to the common registers to prevent accidental modification of their values.
This control is applied to the following registers and bits: the NFCR register, the GTHSCR registers, the GTHCCR.CCHWn[1:0] bits (n = 0 to 3), the GTHSSR register, the GTHPSR register, GTSYNC register, the GTETINT register, the GTBDR register, the GTMDR register, the GTECNFCR register, and the GTADSMR register.
In addition, even if the GTCMNWP.CMNWP bit is 0 (writing to the common registers is enabled), if the GTMDR.LWA01 bit or the GTMDR.LWA23 bit is 1 (cascaded connection), writing to the bits that controls GPT0 and GPT2 is ignored.
The GTSTR register that controls count start is not write-protected by the GTCMNWP.CMNWP bit, but it is write-protected by the GTSWP register.
The GTHCCR.CCSWn bit (n = 0 to 3) that controls counter clearing is not write-protected by the GTCMNWP.CMNWP bit, and it is write-protected by the GTCWP register.
Registers GTCMNWP, GTSWP, GTCWP, and GTWP, which are used to set up write protection, are not write-protected.

22.6.1.2 Write-Protection for Channel Registers

Registers can be write-protected per channel by setting the GTWP.WPn bit (n = 0 to 3) to prevent the values of the registers of each channel from being accidentally modified.
The write-protection can be set for the following registers:

Table 22.10 List of Write-Protected Registers

Register Symbol	Register Name
GTIOR	General PWM timer I/O control register
GTINTAD	General PWM timer interrupt output register
GTCR	General PWM timer control register
GTBER	General PWM timer buffer enable register
GTUDC	General PWM timer count direction register
GTITC	General PWM timer interrupt and A/D converter start request skipping setting register
GTST	General PWM timer status register
GTCNT(LW)	General PWM timer counter
GTCCRA(LW) to GTCCRF(LW)	General PWM timer compare capture registers A to F
GTPR(LW)	General PWM timer period setting register
GTPBR(LW)	General PWM timer period setting buffer register
GTPDBR(LW)	General PWM timer period setting double-buffer register
GTADTRA(LW), GTADTRB(LW)	A/D converter start request timing registers A and B
GTADTBRA(LW), GTADTBRB(LW)	A/D converter start request timing buffer registers A and B
GTADTDBRA(LW), GTADTDBRB(LW)	A/D converter start request timing double-buffer registers A and B
GTONCR	General PWM timer output negate control register
GTDTCR	General PWM timer dead time control register
GTDVU(LW), GTDVD(LW)	General PWM timer dead time value registers U and D
GTDBU(LW), GTDBD(LW)	General PWM timer dead time buffer registers U and D
GTSOTR	General PWM timer output protection function temporary release register

When the GTMDR.LWA01 bit is set to 1, the GTWP.WP0 bit is set to 1. The registers of GPT0 cannot be changed. In this case, the GTWP.WP0 bit cannot be set to 0. Furthermore, the GTWP.WP1 bit is used to control the registers of GPT01.
When the GTMDR.LWA23 bit is set to 1, the GTWP.WP2 bit is set to 1. Register of GPT2 cannot be changed. In this case, the GTWP.WP2 bit cannot be set to 0. Furthermore, the GTWP.WP3 bit is used to control the registers of GPT23.

22.6.2 Disabling of Buffer Operation

If the timing of buffer register write is too late for the buffer transfer timing, buffer operation can be suspended with the GTBDR setting. Specifically, buffer transfer can be temporarily disabled, even though a buffer transfer condition is generated during buffer register write, by setting the corresponding GTBDR bit to 1 (buffer operation disabled) before buffer register write and setting the bit to 0 (buffer operation enabled) after completion of writing to all the buffer registers.
Figure 22.81 shows an example of operation for disabling buffer operation

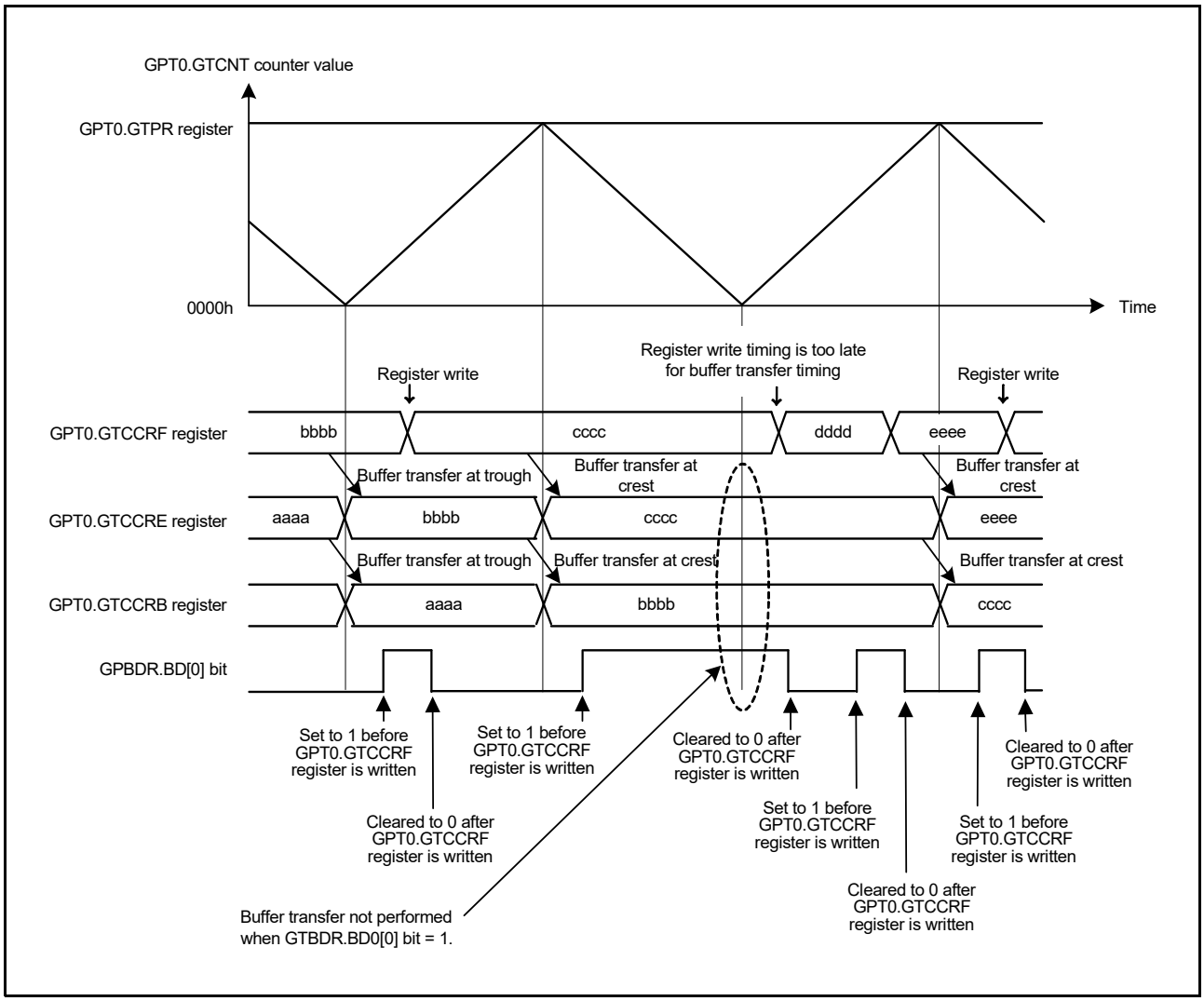


Figure 22.81 Example of Operation for Disabling Buffer Operation (Triangle Waves, Double Buffer Operation, Buffer Transfer at Both Troughs and Crests)

22.6.3 GTIOC Pin Output Negate Control

For protection from system failure, the negate control (deactivating the output level) is provided for GTIOC pin output. There are three negate control sources:comparator output, GTETRG pin input, and writing to the GTONCR.SWN bit. The negate control source can be selected by the GTONCR.NFS[3:0] bits, and the polarity of the negate source by the GTONCR.NFV bits. The inactive level to be output can be selected by the GTONCR.NVA and NAB bits.
When negate control is enabled by the GTONCR.NEA and NAB NEB bits, the inactive level selected by the GTONCR.NVA and NAB bits is output from the GTIOC pin.
Figure 22.82 shows an example of the GTIOC pin output negate control operation (when the GTONCR.NFV bit is set to 1 and the GTONCR.NVA bit is set to 0).
Note that once the negate control is performed, the negate control will not be released in the same cycle if the negate condition is no longer satisfied. The negate control is released in the next cycle.

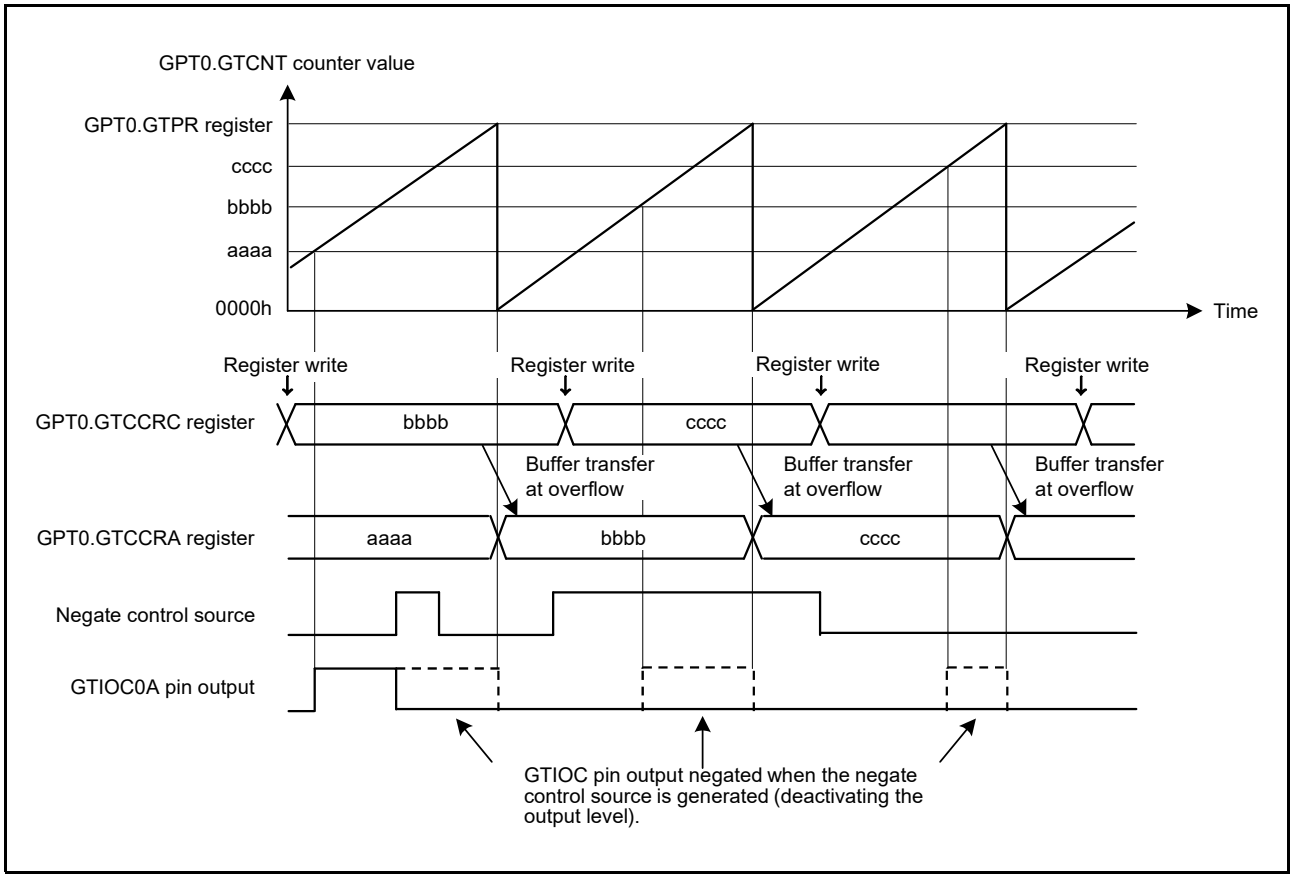


Figure 22.82 Example of GTIOC Pin Output Negate Control Operation (Saw-Wave Up-Counting, Buffer Operation, Active Level: 1, High Output at GTCCRA Compare Match, Low Output at the End of the Cycle)

22.6.4 Output Protection Function for GTIOC Pin Output

Under the automatic dead time setting (GTDTCR.TDE bit = 1) in triangle-wave PWM mode, if an incorrect value (0000h (0000 0000h) or a value greater than or equal to the GTPR(LW) value) is set in the GTCCRA(LW) register, the output protection function for the GTIOC pin output (disabling function) is activated.

The status of the output protection function can be read from the GTSOS.SOS[1:0] bits.

The output protection for the GTIOCnB pin can temporarily be released by setting the GTSOTR.SOTR bit to 1 only when an incorrect value (greater than or equal to the GTPR(LW) setting value) during buffer transfer at troughs is transferred to the GTCCRA(LW) register and output protection (disabling) is activated (the GTSOS.SOS[1:0] bits are 10b). After setting the GTSOTR.SOTR bit to 1, the output protection function is released from the first trough. When setting the GTSOTR.SOTR bit to 0 while the output protection function is released, the output protection function operates from the first trough.

Figure 22.83 shows the output protection function state transition.

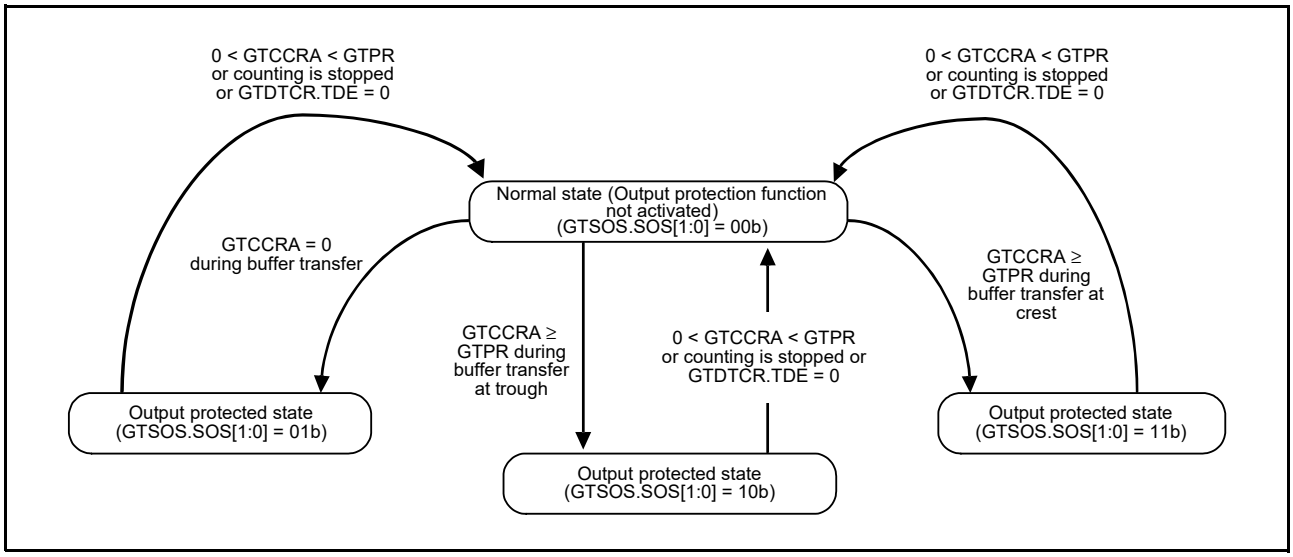
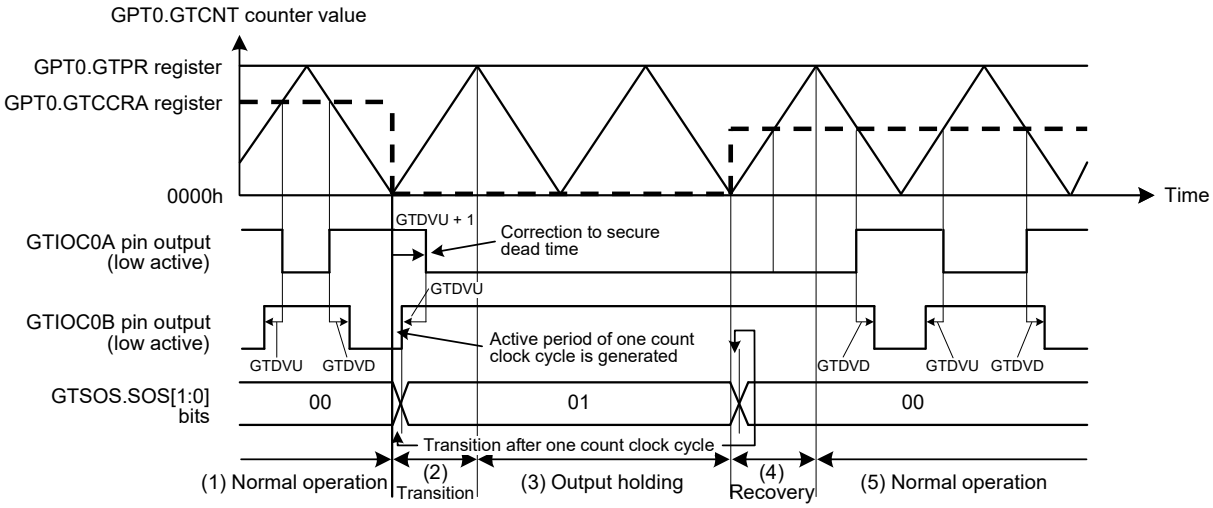


Figure 22.83 Output Protection Function

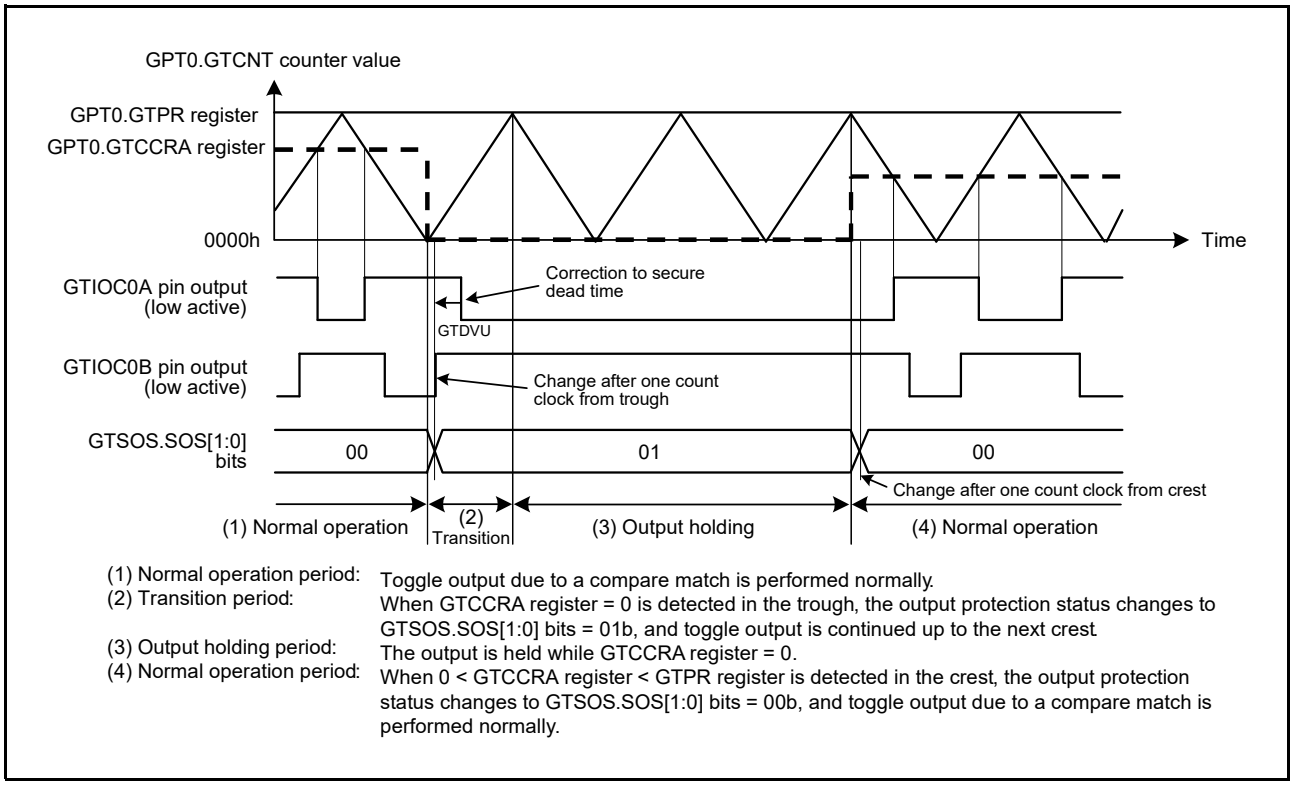
(1) Output Protection Function When the GTCCRA(LW) Register is Set to 0000h (0000 0000h) during Buffer Transfer

Figure 22.84 and Figure 22.85 show examples of output protection function operation when the GTCCRA register is set to 0000h during buffer transfer at troughs, and Figure 22.86 and Figure 22.87 show examples when the GTCCRA register is set to 0000h during buffer transfer at crests.



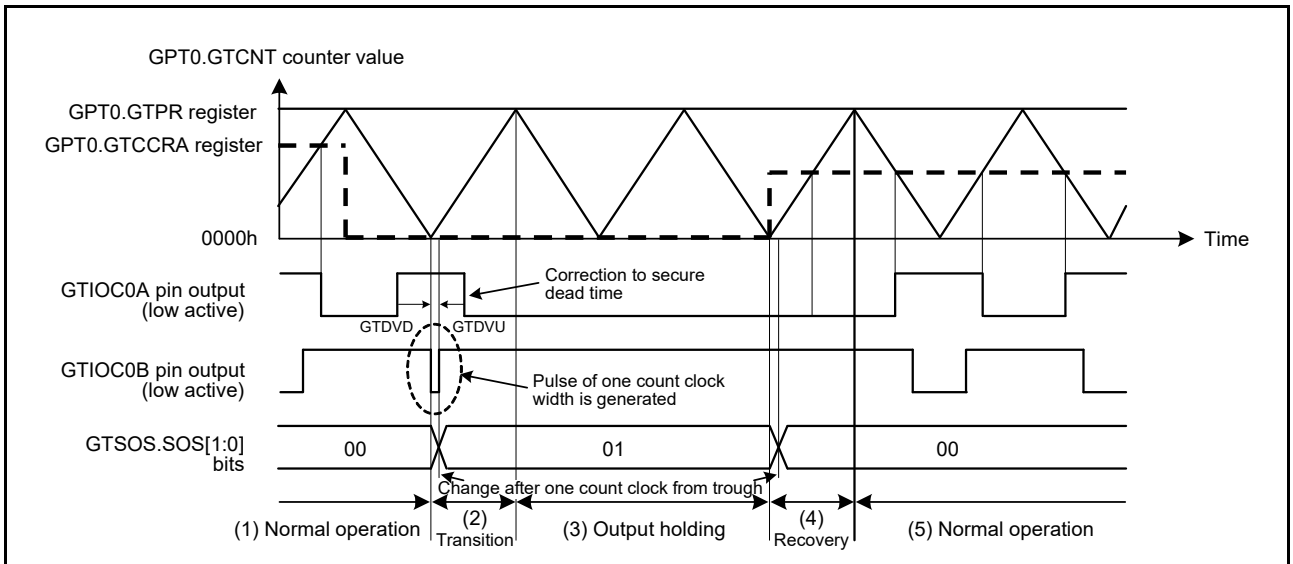
(1) Normal operation period: Toggle output due to a compare match is performed normally.
(2) Transition period: When GTCCRA register = 0 is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 01b, and toggle output is continued up to the next crest.
(3) Output holding period: The output is held while GTCCRA register = 0.
(4) Recovery period: When 0 < GTCCRA register < GTPR register is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 00b, and holding output is maintained up to the next crest.
(5) Normal operation period: Toggle output due to a compare match is performed normally.

Figure 22.84 Example of Output Protection Function Operation When the GTCCRA Register is Set to 0000h during Buffer Transfer at Troughs (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Troughs, Active Level: Low)



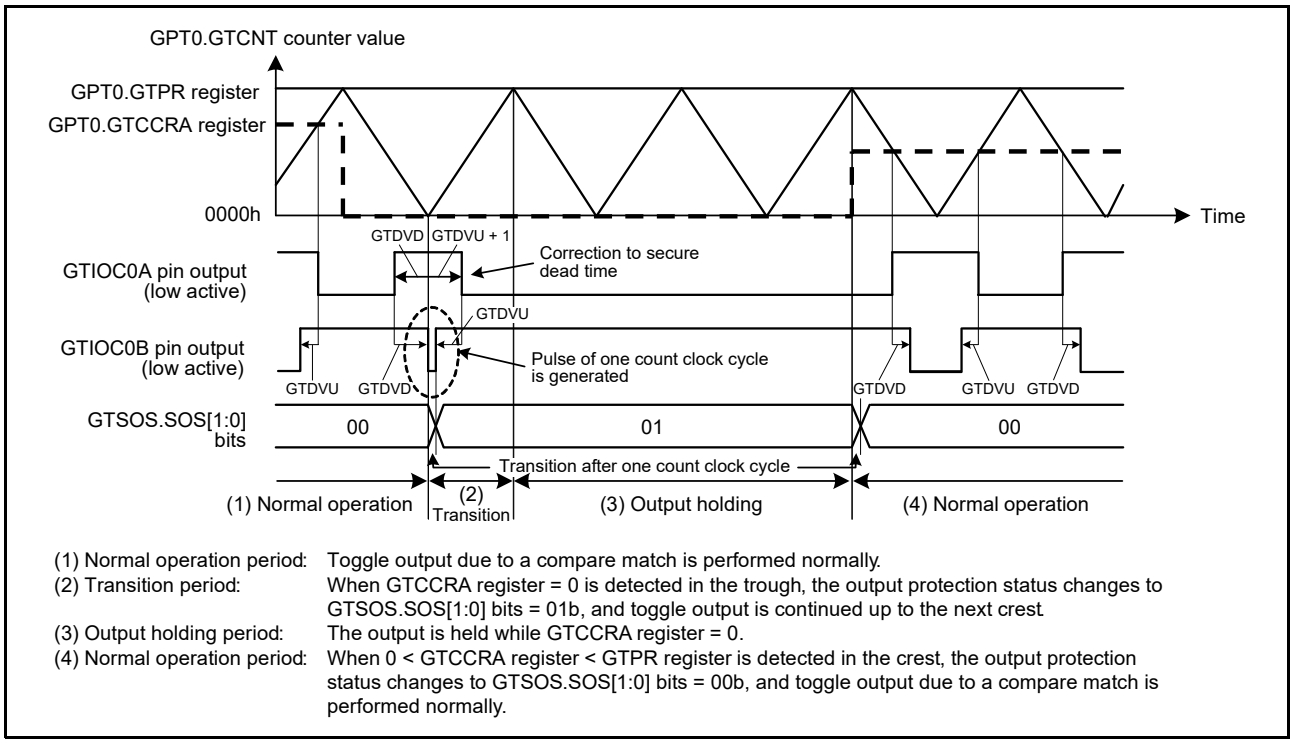
(1) Normal operation period: Toggle output due to a compare match is performed normally.
(2) Transition period: When GTCCRA register = 0 is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 01b, and toggle output is continued up to the next crest.
(3) Output holding period: The output is held while GTCCRA register = 0.
(4) Normal operation period: When 0 < GTCCRA register < GTPR register is detected in the crest, the output protection status changes to GTSOS.SOS[1:0] bits = 00b, and toggle output due to a compare match is performed normally.

Figure 22.85 Example of Output Protection Function Operation When the GTCCRA Register is Set to 0000h during Buffer Transfer at Troughs (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Crests, Active Level: Low)



(1) Normal operation period: Toggle output due to a compare match is performed normally.
(2) Transition period: When GTCCRA register = 0 is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 01b, and toggle output is continued up to the next crest.
(3) Output holding period: The output is held while GTCCRA register = 0.
(4) Recovery period: When 0 < GTCCRA register < GTPR register is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 00b, and holding output is maintained up to the next crest.
(5) Normal operation period: Toggle output due to a compare match is performed normally.

Figure 22.86 Example of Output Protection Function Operation When the GTCCRA Register is Set to 0000h during Buffer Transfer at Crests (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Troughs, Active Level: Low)

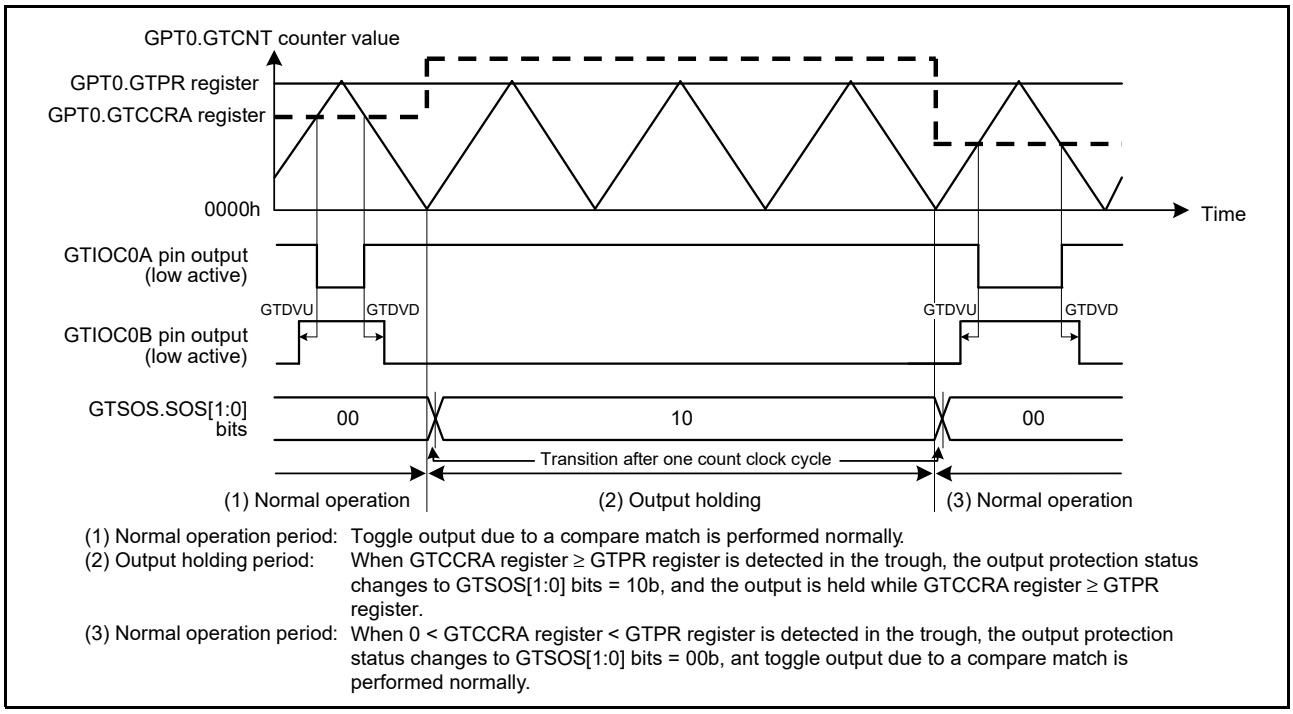


(1) Normal operation period: Toggle output due to a compare match is performed normally.
(2) Transition period: When GTCCRA register = 0 is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 01b, and toggle output is continued up to the next crest.
(3) Output holding period: The output is held while GTCCRA register = 0.
(4) Normal operation period: When 0 < GTCCRA register < GTPR register is detected in the crest, the output protection status changes to GTSOS.SOS[1:0] bits = 00b, and toggle output due to a compare match is performed normally.

Figure 22.87 Example of Output Protection Function Operation When the GTCCRA Register is Set to 0000h during Buffer Transfer at Crests (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Crests, Active Level: Low)

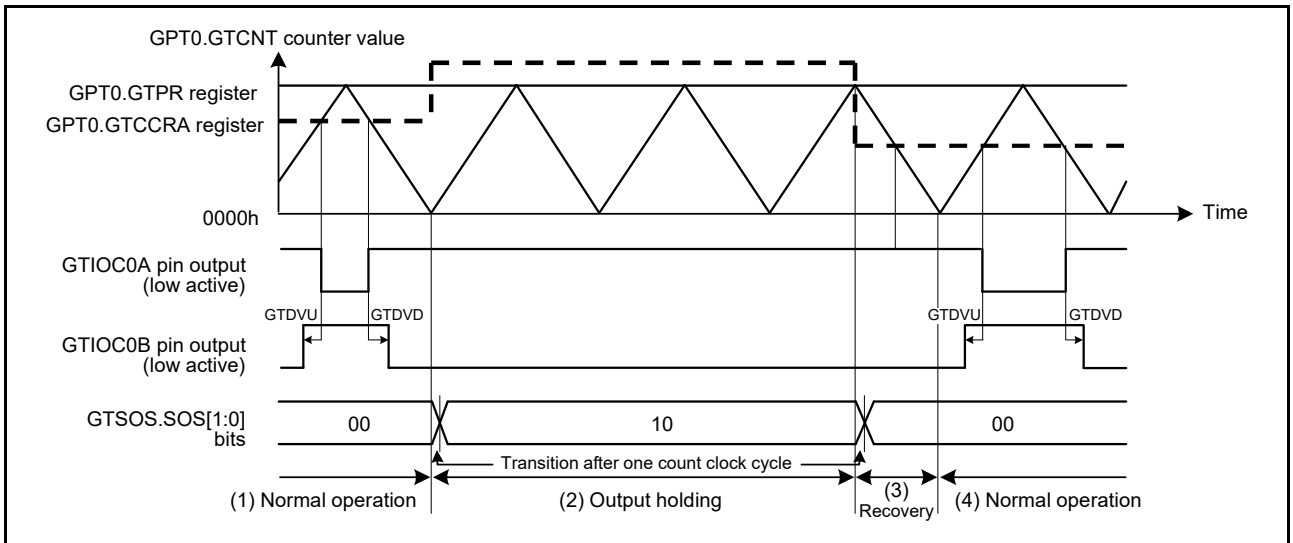
(2) Output Protection Function When GTCCRA(LW) ≥ GTPR(LW) is Set during Buffer Transfer at Troughs

Figure 22.88 and Figure 22.89 show examples of output protection function operation when GTCCRA ≥ GTPR is set during buffer transfer at troughs.



(1) Normal operation period: Toggle output due to a compare match is performed normally.
(2) Output holding period: When GTCCRA register ≥ GTPR register is detected in the trough, the output protection status changes to GTSOS[1:0] bits = 10b, and the output is held while GTCCRA register ≥ GTPR register.
(3) Normal operation period: When 0 < GTCCRA register < GTPR register is detected in the trough, the output protection status changes to GTSOS[1:0] bits = 00b, ant toggle output due to a compare match is performed normally.

Figure 22.88 Example of Output Protection Function Operation When GTCCRA ≥ GTPR is set during Buffer Transfer at Troughs (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Troughs, Active Level: Low)

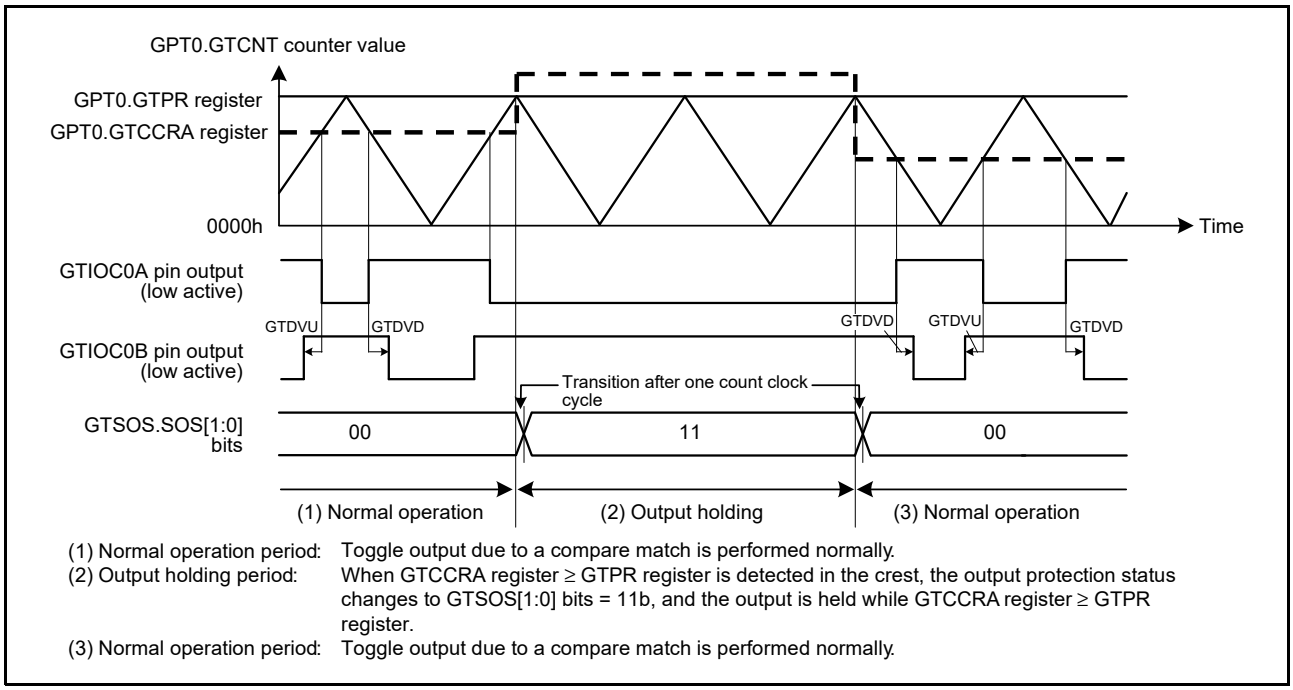


(1) Normal operation period: Toggle output due to a compare match is performed normally.
(2) Output holding period: When GTCCRA register ≥ GTPR register is detected in the trough, the output protection status changes to GTSOS[1:0] bits = 10b, and the output is held while GTCCRA register ≥ GTPR register.
(3) Recovery period: When 0 < GTCCRA register < GTPR register is detected in the crest, the output protection status changes to GTSOS.SOS[1:0] bits = 00b, and holding output is maintained up to the next trough.
(4) Normal operation period: Toggle output due to a compare match is performed normally.

Figure 22.89 Example of Output Protection Function Operation When GTCCRA ≥ GTPR is Set during Buffer Transfer at Troughs (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Crests, Active Level: Low)

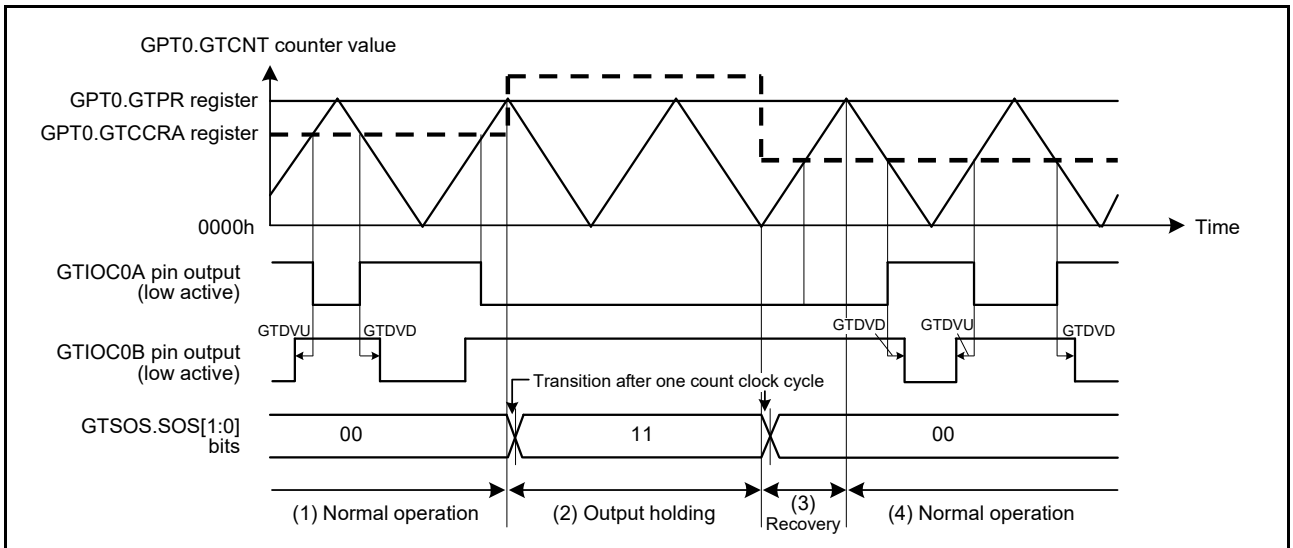
(3) Output Protection Function When GTCCRA(LW) ≥ GTPR(LW) is Set during Buffer Transfer at Crests

Figure 22.90 and Figure 22.91 show examples of output protection function operation when GTCCRA(LW) ≥ GTPR(LW) is set during buffer transfer at crests.



(1) Normal operation period: Toggle output due to a compare match is performed normally.
(2) Output holding period: When GTCCRA register ≥ GTPR register is detected in the crest, the output protection status changes to GTSOS[1:0] bits = 11b, and the output is held while GTCCRA register ≥ GTPR register.
(3) Normal operation period: Toggle output due to a compare match is performed normally.

Figure 22.90 Example of Output Protection Function Operation When GTCCRA ≥ GTPR is Set during Buffer Transfer at Crests (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Crests, Active Level: Low)



(1) Normal operation period: Toggle output due to a compare match is performed normally.
(2) Output holding period: When GTCCRA register ≥ GTPR register is detected in the crest, the output protection status changes to GTSOS.SOS[1:0] bits = 11b, and the output is held while GTCCRA register ≥ GTPR register.
(3) Recovery period: When 0 < GTCCRA register < GTPR register is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 00b, and holding output is maintained up to the next crest.
(4) Normal operation period: Toggle output due to a compare match is performed normally.

Figure 22.91 Example of Output Protection Function Operation When GTCCRA ≥ GTPR is Set during Buffer Transfer at Crests (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Troughs, Active Level: Low)

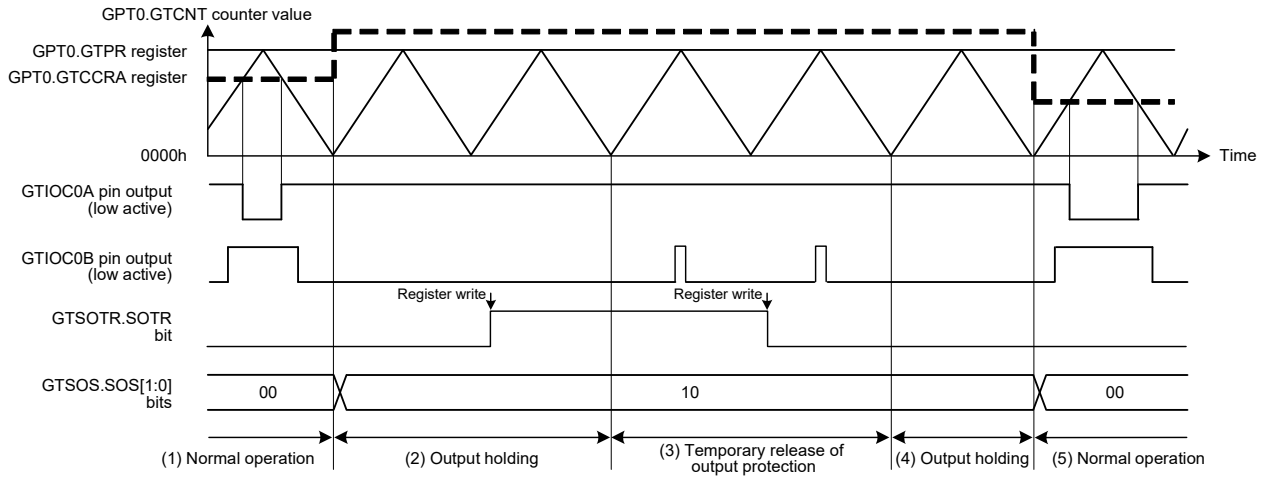
(4) Restricted Specification of Output Protection Function

Even if an incorrect value (0000h (0000 0000h) or a value greater than or equal to the GTPR(LW) value) is set in the GTCCRA(LW) register during count operation, the output protection functions in a specific way such that one of the positive- and negative-phase outputs becomes non-active. However, the following conditions are not satisfied, the output protection does not operate normally.

- When the GTCCRA(LW) value at the start of count operation is greater than 0000h (0000 0000h), and less than the setting value of the GTPR(LW) register
- When the condition [GTCCRA(LW) – GTDVU(LW) < GTPR(LW) – 1] is satisfied during buffer transfer at crests.
- When the condition [GTCCRA(LW) – GTDVU(LW) > 1] is satisfied when GTCCRA(LW) ≥ GTPR(LW) during buffer transfer at troughs.

(5) Temporary Release of Output Protection Function

When the GTSOS.SOS[1:0] bits = 10b (protected state in which GTCCRA(LW) ≥ GTPR(LW) has occurred during transfer at trough), the protected state of the GTIOCnBF pin output can be temporarily released by setting the GTSOTR.SOTR bit to 1. The GTSOS.SOS[1:0] bits retain 10b even if the output protection function is released. When the SOTR bit is set to 0, the GTIOCnB pin output protection can be restarted.
Figure 22.92 shows an example of output protection function operation when GTCCRA ≥ GTPR is set during buffer transfer at troughs.



(1) Normal operation period:	Toggle output due to a compare match is performed normally.
(2) Output holding period:	When GTCCRA register ≥ GTPR register is detected in the trough, the output protection status changes to GTSOS[1:0] bits = 10b, and the output is held while GTCCRA register ≥ GTPR register.
(3) Output protection temporary release period:	Even when the GTSOTR.SOTR bit is set to 1, the GTIOCOB pin output is held until the first trough.
(4) Output holding period:	After the GTSOTR.SOTR bit is set to 1, the GTIOCOB pin output is performed normally from the first trough. The output is held until 0 < GTCCRA register < GTPR register is detected in the tough.
(5) Normal operation period:	When 0 < GTCCRA register < GTPR register is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 00b, and toggle output due to a compare match is performed normally.

Figure 22.92 Example of Output Protection Function Operation When GTCCRA ≥ GTPR is Set during Buffer Transfer at Troughs (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Troughs, Active Level: Low)

22.6.5 High-Impedance Control of GTIOC Pin Output by POE Function

For protection from system failure, the high-impedance state of the GTIOC pin output can be controlled by the port output enable (POE) function.
For details, see section 21, Port Output Enable 3 (POE3A).

22.7 Initialization Method of Output Pins

22.7.1 Pin Settings after Reset

The GPT registers are initialized at a reset. Start counting after selecting the port mode (PMR and PmnPFS), setting the GTIOR register and the OAE and OBE bits in the GTONCR register and outputting the GPT function to external pins.

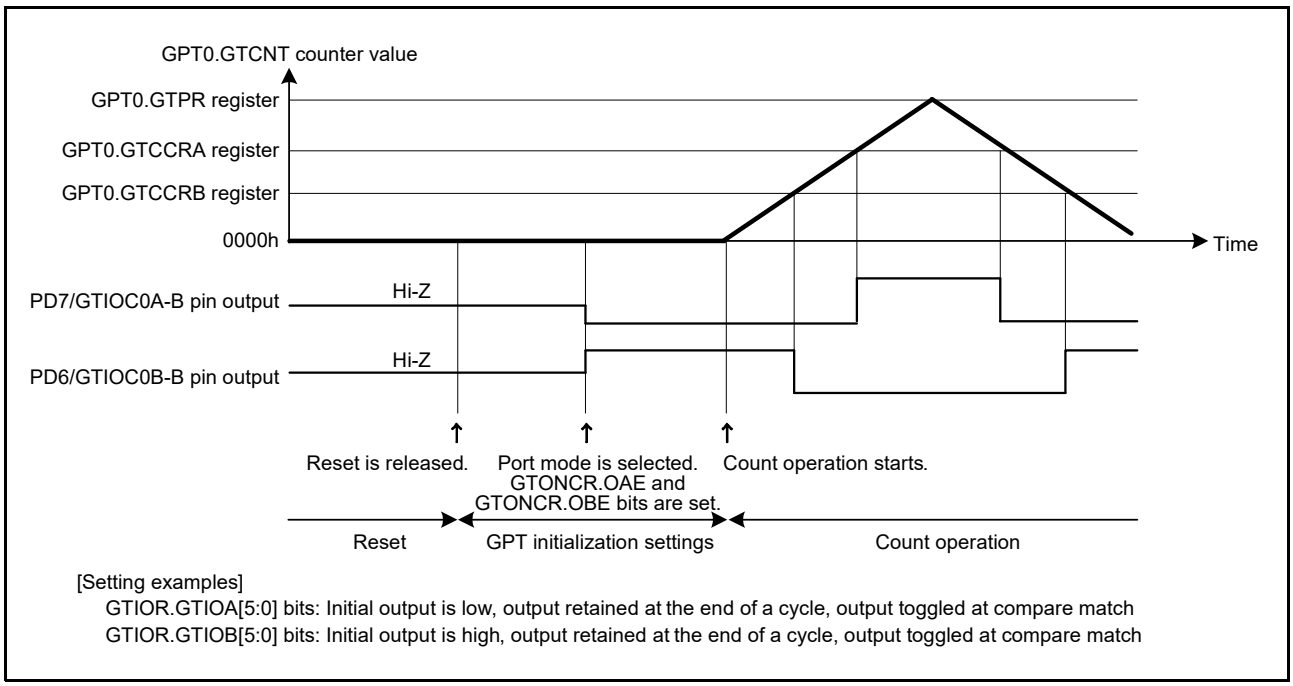


Figure 22.93 Example of Pin Settings after Reset

22.7.2 Pin Initialization Due to Error during Operation

If an error occurs during GPT operation, the following four types of pin processing can be performed before pin initialization.

(1) Set OAHLD and OBHLD bits in the GTIOR register to 1 and retain the outputs at count stop.

(2) Set OAHLD and OBHLD bits in the GTIOR register to 0, specify arbitrary output values at OADFLT and OBDFLT in the GTIOR register, and output the arbitrary values at count stop.

(3) Set the pin to output an arbitrary value as a general output port by setting the PDR, PODR, and PMR registers of the I/O port in advance. Set the OAE and OBE bits in the GTONCR register to 0 and the control bit in PMR that corresponds to the pin to 0 to allow the arbitrary values to be output from the pin set as a general output port when an error occurs.

(4) Drive the output to a high impedance state using the POE function.

When automatic dead time setting has been made, set the GTDTCR.TDE bit to 0 once after counting is stopped.

When counting is stopped, only the values of registers that are changed by a GPT external source will change. If counting is resumed, operation will carry on from where it was stopped.
If counting was stopped, registers should be initialized before counting is started.

22.8 Usage Notes

22.8.1 Module Stop Function Setting

Operation of the GPT can be disabled or enabled by the module stop control register. The initial setting is for operation of the GPT to be halted. Register access is enabled by clearing module stop state. For details, see section 11, Low Power Consumption.

22.8.2 Settings of the GTCCRm(LW) Register during Compare Match Operation (m = A to F)

(1) When automatic dead time setting has been made in triangle-wave PWM mode

The GTCCRA(LW) register should satisfy the following conditions:

GTCCRA(LW) > GTDVU(LW),
GTCCRA(LW) > GTDVD(LW), and
GTCCRA(LW) < GTPR(LW).

When the GTCCRA(LW) register is set to 0000h (0000 0000h) or a value greater than or equal to the GTPR(LW) value during count operation, the output protection function is activated.
However, if the following conditions are not satisfied, the output protection does not operate normally.

- When the GTCCRA(LW) value at the start of count operation is greater than 0000h (0000 0000h), and less than the setting value of the GTPR(LW) register
- When the condition [GTCCRA(LW) – GTDVU(LW) < GTPR(LW) – 1] is satisfied during buffer transfer at crests.
- When the condition [GTCCRA(LW) – GTDVU(LW) > 1] is satisfied when GTCCRA(LW) ≥ GTPR(LW) during buffer transfer at troughs.

For details, refer to section 22.6.4, Output Protection Function for GTIOC Pin Output.

(2) When automatic dead time setting has not been made in triangle-wave PWM mode

Set a value greater than 0000h (0000 0000h), and less than the setting value of the GTPR(LW) register in the GTCCRA(LW) register. When 0000h (0000 0000h) or the same value as that of the GTPR(LW) register is set in the GTCCRA(LW) register, compare match is generated in one cycle only when [GTCCRA(LW) = 0000h (0000 0000h)] or [GTCCRA(LW) = GTPR(LW)] is met. Furthermore, a value exceeding the setting value of the GTPR(LW) register is set in the GTCCRA(LW) register, compare match does not occur.
Similarly, set a value greater than 0000h (0000 0000h), and less than the setting value of the GTPR(LW) register in the GTCCRB(LW) register. When 0000h (0000 0000h) or the same value as that of the GTPR(LW) register is set in the GTCCRB(LW) register, compare match is generated in one cycle only when [GTCCRB(LW) = 0000h (0000 0000h)] or [GTCCRB(LW) = GTPR(LW)] is met. Furthermore, a value exceeding the setting value of the GTPR(LW) register is set in the GTCCRB(LW) register, compare match does not occur.

(3) When automatic dead time setting has been made in saw-wave one-shot pulse mode

The GTCCRC(LW) and GTCCRD(LW) registers should be set to satisfy the following restrictions. If the restrictions are not satisfied, correct output waveforms with secured dead time may not be obtained.

- In up-counting:
  GTCCRC(LW) < GTCCRD(LW)
  GTCCRC(LW) > GTDVU(LW)
  GTCCRD(LW) < GTPR(LW) – GTDVD(LW)
- In down-counting:
  GTCCRC(LW) > GTCCRD(LW)
  GTCCRC(LW) < GTPR(LW) – GTDVU(LW)
  GTCCRD(LW) > GTDVD(LW)

(4) When automatic dead time setting has not been made in saw-wave one-shot pulse mode

The GTCCRC(LW) and GTCCRD(LW) registers should be set to satisfy the following restrictions. If the restrictions are not satisfied, two compare matches do not occur and pulse output cannot be performed.

- In up-counting: 0 < GTCCRC(LW) < GTCCRD(LW) < GTPR(LW)
- In down-counting: GTPR(LW) > GTCCRC(LW) > GTCCRD(LW) > 0

Similarly, GTCCRE and GTCCRF should be set to satisfy the following restrictions. If the restrictions are not satisfied, two compare matches do not occur and pulse output cannot be performed.

- In up-counting: 0 < GTCCRE(LW) < GTCCRF(LW) < GTPR(LW)
- In down-counting: GTPR(LW) > GTCCRE(LW) > GTCCRF(LW) > 0

(5) In saw-wave PWM mode

The GTCCRA register should be set with the range of 0 < GTCCRA(LW) < GTPR(LW). If GTCCRA(LW) = 0000h (0000 0000h) or GTCCRA(LW) = GTPR(LW) is set, a compare match occurs within the cycle only when GTCCRA(LW) = 0000h (0000 0000h) or GTCCRA(LW) = GTPR(LW) is satisfied. If GTCCRA(LW) > GTPR(LW) is set, no compare match occurs.
Similarly, GTCCRB should be set with the range of 0 < GTCCRB(LW) < GTPR. If GTCCRB(LW) = 0000h (0000 0000h) or GTCCRB(LW) = GTPR(LW) is set, a compare match occurs within the cycle only when GTCCRB(LW) = 0000h (0000 0000h) or GTCCRB(LW) = GTPR(LW) is satisfied. If GTCCRB(LW) > GTPR(LW) is set, no compare match occurs.

22.8.3 Stopping the Timer in the Safe Way

When the timer stopping by the GTSTR register writing and the GPT compare match interrupt conflict, an interrupt may be generated after the GTSTR register writing.
Therefore, stop the timer in the following order. Then, a compare match interrupt is not generated after the timer has been stopped, and the timer can be stopped in the safe way.

(1) Disable the GPT interrupt request by the IER register of the ICU.
(2) Disable the interrupt request by the GTINTAD register.
(3) Set the GTSTR.CSTn bit to 0.

22.8.4 Order of Priority in Event Counter Operation

(1) Contention between writing to and clearing of the GTCNT(LW) counter

If the counter clearing signal is generated during a cycle of writing to the GTCNT(LW) counter, writing to the GTCNT(LW) counter takes priority over clearing of the GTCNT(LW) counter.

(2) Contention between writing to the GTSTR.CSTn bit and a hardware source

If a hardware source is generated in a cycle of writing to the GTSTR.CSTn bit (n = 0 to 3), writing to the CSTn bit takes priority over an automatic set or reset of the CSTn bit due to the hardware source.

(3) Contention between a set and a reset by a hardware source to the GTSTR.CSTn bit

When a set and a reset by a hardware source to the GTSTR.CSTn bit (n = 0 to 3) occurs at the same time, an automatic set takes priority.

(4) Contention between access to the GTCCRm(LW) register and input capture/buffer transfer

In case of contention between the writing to the GTCCRm(LW) register (m = A to F) and input capture or buffer transfer, writing to the GTCCRm(LW) register takes priority over input capture or buffer transfer.

If reading from the GTCCRm(LW) register and input capture or buffer transfer are in contention, the data before an update is read.

(5) Contention between access to the GTPR(LW) register and buffer transfer

If writing to the GTPR(LW) register and buffer transfer are in contention, writing to the GTPR(LW) register takes priority over buffer transfer.
If reading from the GTPR(LW) register and buffer transfer are in contention, the data before an update is read.

(6) Contention between access to the GTADTRm(LW) register and buffer transfer

If writing to the GTADTRm(LW) register (m = A, B) and buffer transfer are in contention, writing to the GTADTRm(LW) register takes priority over the buffer transfer.
If reading from the GTADTRm(LW) register and buffer transfer are in contention, the data before an update is read.

(7) Contention between access to the GTDVm(LW) register and buffer transfer

If writing to the GTDVm(LW) register (m = U, D) and buffer transfer are in contention, writing to the GTDVm(LW) register takes priority over the buffer transfer.
If reading from the GTDVm(LW) register and buffer transfer are in contention, the data before an update is read.

22.8.5 Setting the GTMDR Register

Overwriting the value of the GTMDR.LWA01 bit results in a reset of some registers of the GPT0, GPT1, and GPT01 and the bits that control GPT0, GPT1, and GPT01 of the common registers.
Overwriting the value of the GTMDR.LWA23 bit results in a reset of some registers of the GPT0, GPT1, and GPT01 and the bits that control GPT0, GPT1, and GPT01 of the common registers.
Change the channel configuration by writing to the GTMDR register while the counter is stopped before setting other registers.

22.8.6 Pin Outputs While the Counter is Stopped

The levels output on pins while the counter is stopped are set in the GTIOR register, and the outputs change to the specified levels in synchronization with the clock signal specified in the GTCR.TPCS[3:0] bits.
When the frequency of the selected clock is low, the outputs may not change before counting is restarted even if the GTIOR register is overwritten while counting is stopped. In this case, set the GTCR.TPCS[3:0] bits to 0000b, set the GTIOR register, and then re-specify the actual desired value in the TPCS[3:0] bits.

23. 8-Bit Timer (TMR)

This MCU has four units (unit 0, unit 1, unit 2, unit 3) of an on-chip 8-bit timer (TMR) module that comprise two 8-bit counter channels, totaling eight channels. The 8-bit timer module can be used to count external events and also be used as a multi-function timer in a variety of applications, such as generation of counter reset signal, interrupt requests, and pulse output with a desired duty cycle using a compare-match signal with two registers.
Unit 0, unit 1, unit 2, and unit 3 have the same functions, and unit 0 and unit 1 can generate a baud rate clock for the SCI.
In this section, “PCLK” is used to refer to PCLKB.

23.1 Overview

Table 23.1 lists the specifications of the TMR. Table 23.2 and Table 23.3 list the TMR functions.
Figure 23.1 shows a block diagram of the 8-bit timer module (unit 0), Figure 23.2 shows that of the 8-bit timer module (unit 1), Figure 23.3 shows that of the 8-bit timer module (unit 2), and Figure 23.3 shows that of the 8-bit timer module (unit 3).

Table 23.1 Specifications of TMR

Item	Description
Count clock	• Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192 • External clock: external count clock
Number of channels	(8 bits × 2 channels) × 4 units
Compare match	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)
Counter clear	Selected by compare match A or B, or an external counter reset signal.
Timer output	Output pulses with a desired duty cycle or PWM output
Cascading of two channels	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits, TMR4 for the upper 8 bits and TMR5 for the lower 8 bits, TMR6 for the upper 8 bits and TMR7 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches, TMR5 can be used to count TMR4 compare matches, TMR7 can be used to count TMR6 compare matches).
Interrupt sources	Compare match A, compare match B, and overflow
DTC activation	DTC can be activated by compare match A interrupts or compare match B interrupts.
A/D conversion start trigger of the A/D converter	Compare match A of TMR0, TMR2, TMR4, and TMR6
Capable of generating baud rate clock for SCI	Generates baud rate clock for SCI.*1
Low power consumption function	Each unit can be placed in a module stop state

Note 1. For details, see section 26, Serial Communications Interface (SCIg).

Table 23.2 TMR Functions (1)

Item		Unit 0			Unit 1		
Counter mode		8 Bits		16 Bits	8 Bits		16 Bits
Channel		TMR0	TMR1	TMR0 + TMR1	TMR2	TMR3	TMR2 + TMR3
Count clock		PCLK/1 PCLK/2 PCLK/8 PCLK/32 PCLK/64 PCLK/1024 PCLK/8192 TMCI0	PCLK/1 PCLK/2 PCLK/8 PCLK/32 PCLK/64 PCLK/1024 PCLK/8192 TMCI1	PCLK/1 PCLK/2 PCLK/8 PCLK/32 PCLK/64 PCLK/1024 PCLK/8192 TMCI1	PCLK/1 PCLK/2 PCLK/8 PCLK/32 PCLK/64 PCLK/1024 PCLK/8192 TMCI2	PCLK/1 PCLK/2 PCLK/8 PCLK/32 PCLK/64 PCLK/1024 PCLK/8192 TMCI3	PCLK/1 PCLK/2 PCLK/8 PCLK/32 PCLK/64 PCLK/1024 PCLK/8192 TMCI3
Counter clear		TMR0.TCORA TMR0.TCORB TMRI0	TMR1.TCORA TMR1.TCORB TMRI1	TMR0.TCORA + TMR1.TCORA TMR0.TCORB + TMR1.TCORB TMRI0	TMR2.TCORA TMR2.TCORB TMRI2	TMR3.TCORA TMR3.TCORB TMRI3	TMR2.TCORA + TMR3.TCORA TMR2.TCORB + TMR3.TCORB TMRI2
Compare match	Compare match A	○	○	○	○	○	○
	Compare match B	○	○	○	○	○	○
Timer output	Low output	○	○	○	○	○	○
	High output	○	○	○	○	○	○
	Toggle output	○	○	○	○	○	○
DTC activation	Compare match A	○	○	○	○	○	○
	Compare match B	○	○	○	○	○	○
	TCNT overflow	—	—	—	—	—	—
Interrupt	Compare match A	CMIA0	CMIA1	CMIA0	CMIA2	CMIA3	CMIA2
	Compare match B	CMIB0	CMIB1	CMIB0	CMIB2	CMIB3	CMIB2
	TCNT overflow	OVI0	OVI1	OVI0	OVI2	OVI3	OVI2
Cascaded connection		TMR1 overflow	TMR0 compare match A	—	TMR3 overflow	TMR2 compare match A	—
A/D conversion start trigger of the A/D converter*1		○	—	○	○	—	○
SCI baud rate clock generation*2		○		—	○		—
Module stop setting*3		MSTPCRA.MSTPA5 bit (unit 0), MSTPCRA.MSTPA4 bit (unit 1)					

Table 23.3 TMR Functions (2)

Item		Unit 2			Unit 3		
Counter mode		8 Bits		16 Bits	8 Bits		16 Bits
Channel		TMR4	TMR5	TMR4 + TMR5	TMR6	TMR7	TMR6 + TMR7
Count clock		PCLK/1 PCLK/2 PCLK/8 PCLK/32 PCLK/64 PCLK/1024 PCLK/8192 TMCI4	PCLK/1 PCLK/2 PCLK/8 PCLK/32 PCLK/64 PCLK/1024 PCLK/8192 TMCI5	PCLK/1 PCLK/2 PCLK/8 PCLK/32 PCLK/64 PCLK/1024 PCLK/8192 TMCI5	PCLK/1 PCLK/2 PCLK/8 PCLK/32 PCLK/64 PCLK/1024 PCLK/8192 TMCI6	PCLK/1 PCLK/2 PCLK/8 PCLK/32 PCLK/64 PCLK/1024 PCLK/8192 TMCI7	PCLK/1 PCLK/2 PCLK/8 PCLK/32 PCLK/64 PCLK/1024 PCLK/8192 TMCI7
Counter clear		TMR4.TCORA TMR4.TCORB TMRI4	TMR5.TCORA TMR5.TCORB TMRI5	TMR4.TCORA + TMR5.TCORA TMR4.TCORB + TMR5.TCORB TMRI4	TMR6.TCORA TMR6.TCORB TMRI6	TMR7.TCORA TMR7.TCORB TMRI7	TMR6.TCORA + TMR7.TCORA TMR6.TCORB + TMR7.TCORB TMRI6
Compare match	Compare match A	○	○	○	○	○	○
	Compare match B	○	○	○	○	○	○
Timer output	Low output	○	○	○	○	○	○
	High output	○	○	○	○	○	○
	Toggle output	○	○	○	○	○	○
DTC activation	Compare match A	○	○	○	○	○	○
	Compare match B	○	○	○	○	○	○
	TCNT overflow	—	—	—	—	—	—
Interrupt	Compare match A	CMIA4	CMIA5	CMIA4	CMIA6	CMIA7	CMIA6
	Compare match B	CMIB4	CMIB5	CMIB4	CMIB6	CMIB7	CMIB6
	TCNT overflow	OVI4	OVI5	OVI4	OVI6	OVI7	OVI6
Cascaded connection		TMR5 overflow	TMR4 compare match A	—	TMR7 overflow	TMR6 compare match A	—
A/D conversion start trigger of the A/D converter*1		○	—	○	○	—	○
SCI baud rate clock generation*2		—	—	—	—	—	—
Module stop setting*3		MSTPCRA.MSTPA3 bit (unit 2), MSTPCRA.MSTPA2 bit (unit 3)					

○: Possible
—: Impossible
Note 1. For details, see section 31, 12-Bit A/D Converter (S12ADF).
Note 2. For details, see section 26, Serial Communications Interface (SCIg).
Note 3. For details, see section 11, Low Power Consumption.

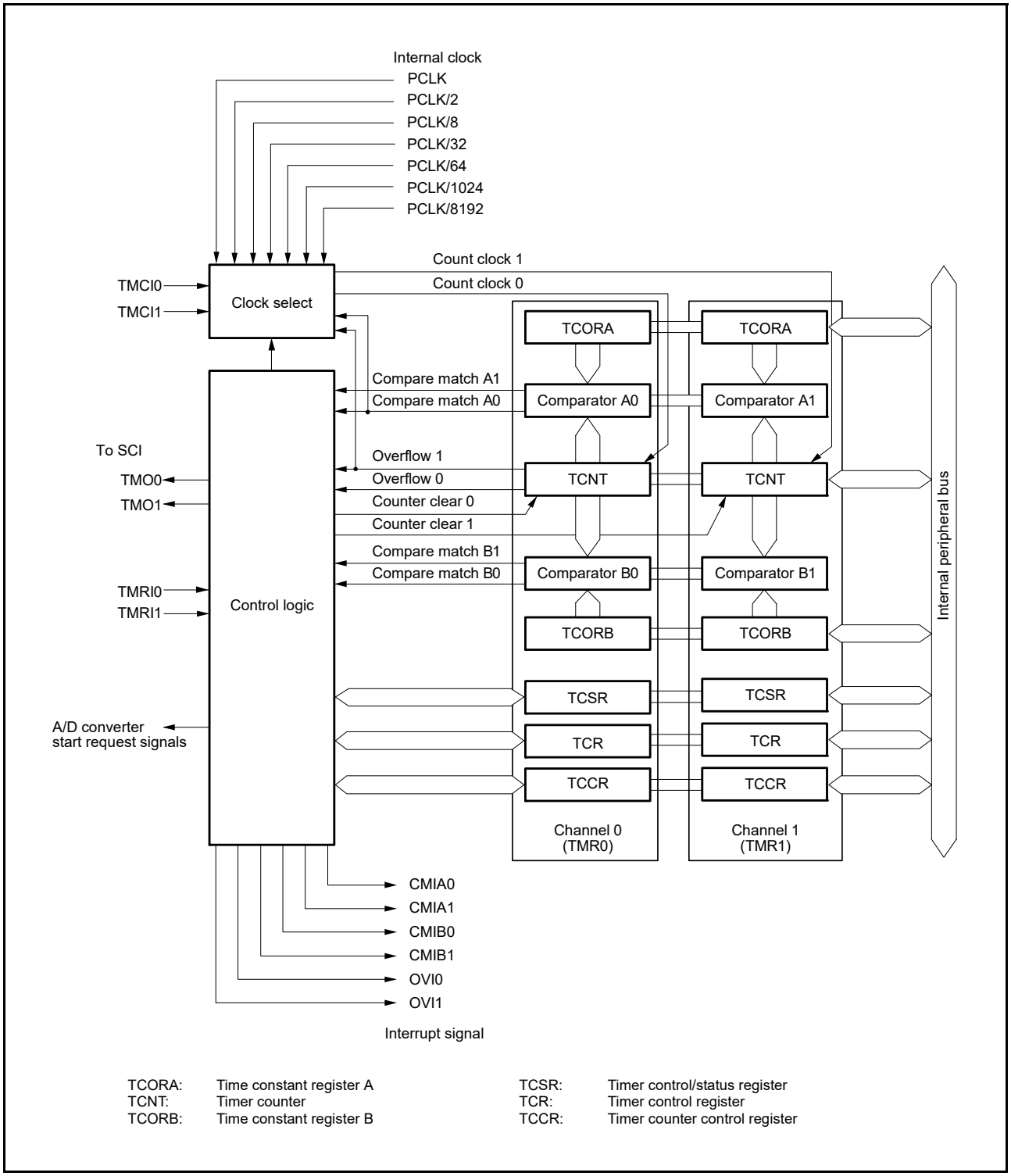


Figure 23.1 Block Diagram of TMR (Unit 0)

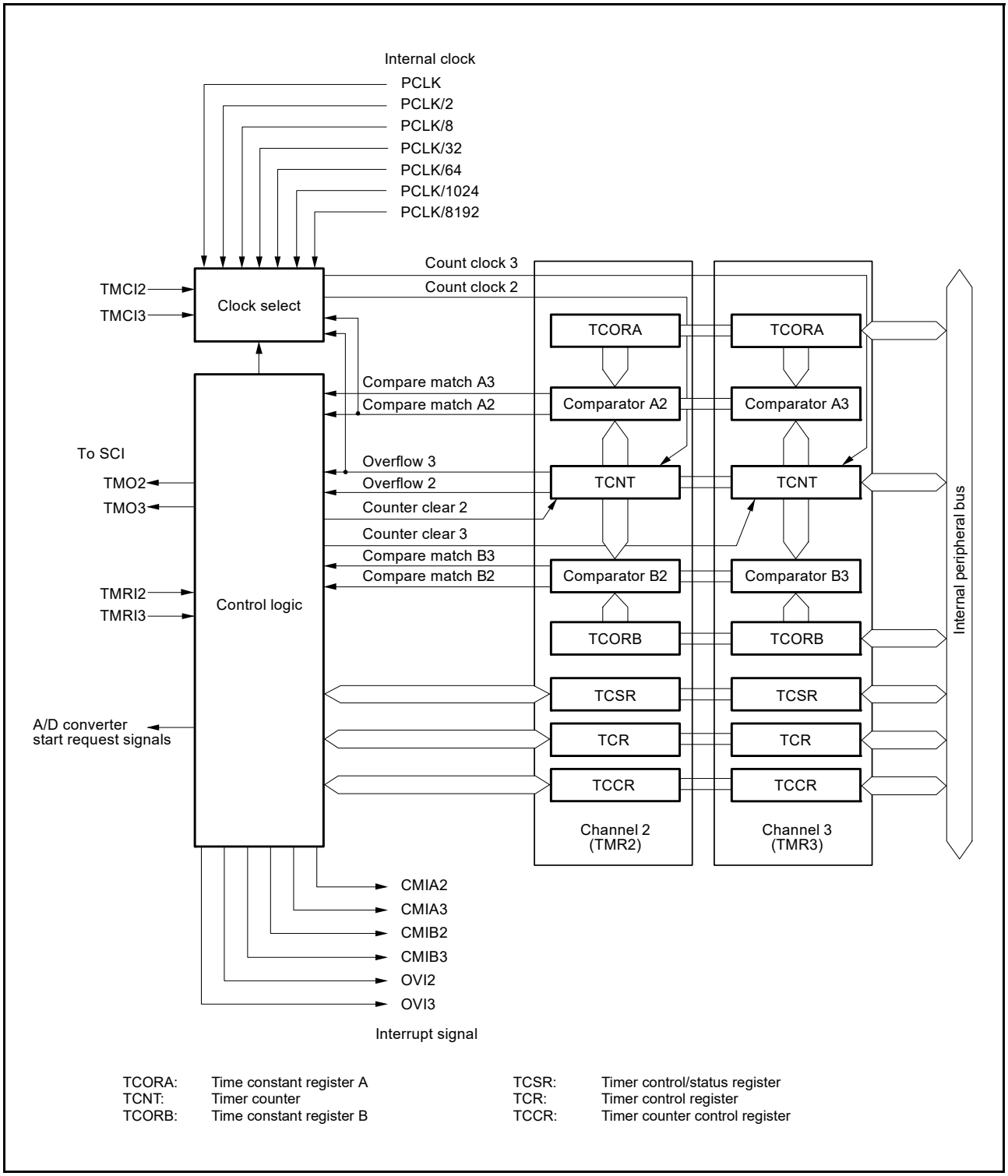


Figure 23.2 Block Diagram of TMR (Unit 1)

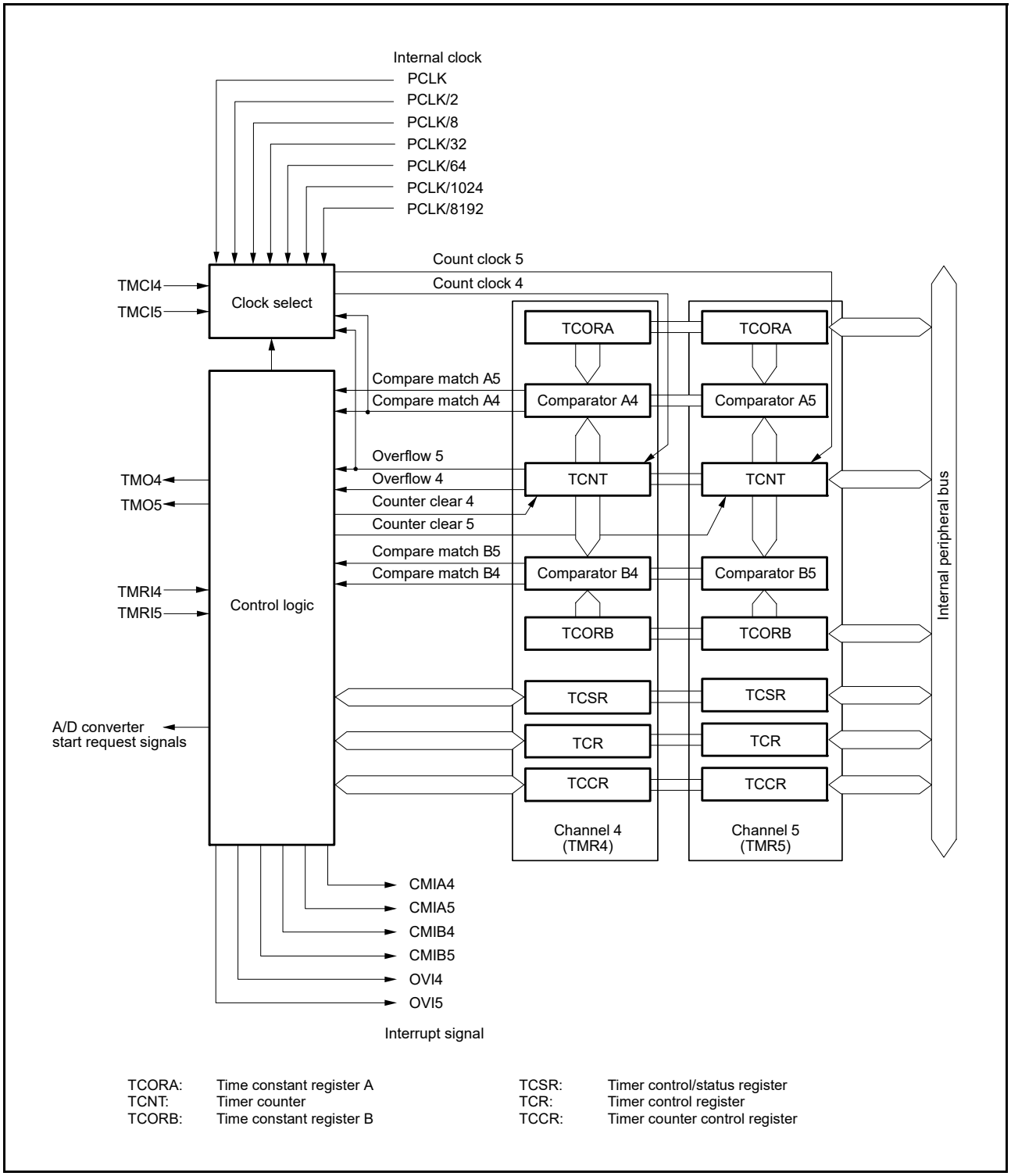


Figure 23.3 Block Diagram of TMR (Unit 2)

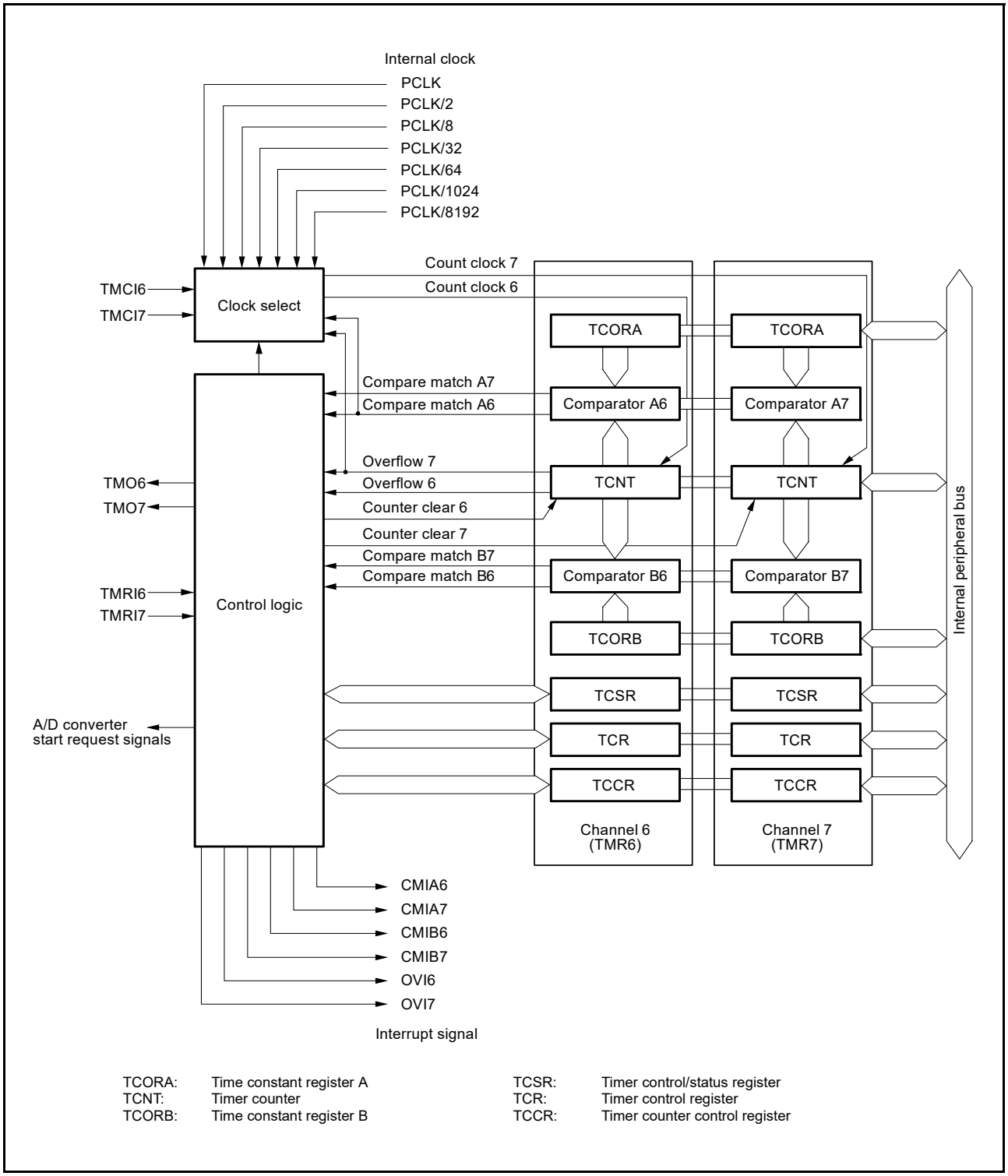


Figure 23.4 Block Diagram of TMR (Unit 3)

Table 23.4 lists the I/O pins of the TMR.

Table 23.4 Pin Configuration of TMR

Unit	Channel	Pin Name	I/O	Description
0	TMR0	TMO0	Output	Outputs compare match
		TMCI0	Input	Inputs external count clock
		TMRI0	Input	Inputs external counter reset
	TMR1	TMO1	Output	Outputs compare match
		TMCI1	Input	Inputs external count clock
		TMRI1	Input	Inputs external counter reset
1	TMR2	TMO2	Output	Outputs compare match
		TMCI2	Input	Inputs external count clock
		TMRI2	Input	Inputs external counter reset
	TMR3	TMO3	Output	Outputs compare match
		TMCI3	Input	Inputs external count clock
		TMRI3	Input	Inputs external counter reset
2	TMR4	TMO4	Output	Outputs compare match
		TMCI4	Input	Inputs external count clock
		TMRI4	Input	Inputs external counter reset
	TMR5	TMO5	Output	Outputs compare match
		TMCI5	Input	Inputs external count clock
		TMRI5	Input	Inputs external counter reset
3	TMR6	TMO6	Output	Outputs compare match
		TMCI6	Input	Inputs external count clock
		TMRI6	Input	Inputs external counter reset
	TMR7	TMO7	Output	Outputs compare match
		TMCI7	Input	Inputs external count clock
		TMRI7	Input	Inputs external counter reset

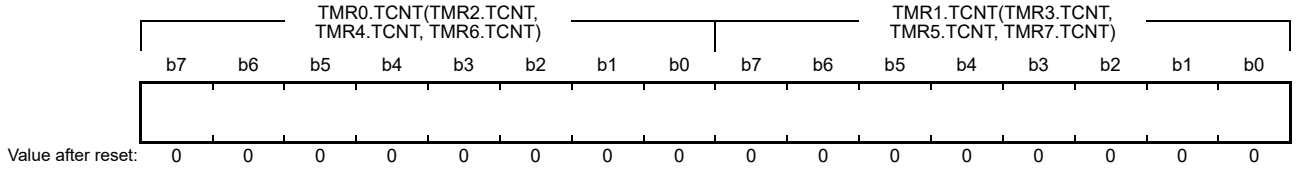
23.2 Register Descriptions

Table 23.5 Register Allocation for 16-Bit Access

Address	Upper 8 Bits	Lower 8 Bits
0008 8208h	TMR0.TCNT	TMR1.TCNT
0008 8204h	TMR0.TCORA	TMR1.TCORA
0008 8206h	TMR0.TCORB	TMR1.TCORB
0008 820Ah	TMR0.TCCR	TMR1.TCCR
0008 8218h	TMR2.TCNT	TMR3.TCNT
0008 8214h	TMR2.TCORA	TMR3.TCORA
0008 8216h	TMR2.TCORB	TMR3.TCORB
0008 821Ah	TMR2.TCCR	TMR3.TCCR
0008 8228h	TMR4.TCNT	TMR5.TCNT
0008 8224h	TMR4.TCORA	TMR5.TCORA
0008 8226h	TMR4.TCORB	TMR5.TCORB
0008 822Ah	TMR4.TCCR	TMR5.TCCR
0008 8238h	TMR6.TCNT	TMR7.TCNT
0008 8234h	TMR6.TCORA	TMR7.TCORA
0008 8236h	TMR6.TCORB	TMR7.TCORB
0008 823Ah	TMR6.TCCR	TMR7.TCCR

23.2.1 Timer Counter (TCNT)

Address(es): TMR0.TCNT 0008 8208h, TMR1.TCNT 0008 8209h, TMR2.TCNT 0008 8218h, TMR3.TCNT 0008 8219h, TMR4.TCNT 0008 8228h, TMR5.TCNT 0008 8229h, TMR6.TCNT 0008 8238h, TMR7.TCNT 0008 8239h



TCNT is an 8-bit readable/writable up-counter.

TMR0.TCNT and TMR1.TCNT (TMR2.TCNT and TMR3.TCNT, TMR4.TCNT and TMR5.TCNT, TMR6.TCNT and TMR7.TCNT) comprise a single 16-bit counter so they can be accessed together by a word transfer instruction.

The TCCR.CSS[1:0] and CKS[2:0] bits are used to select a count clock.

TCNT can be cleared by an external counter reset signal, compare match A, or compare match B. Which compare match to be used for clearing is selected by the TCR.CCLR[1:0] bits.

When TCNT overflows (its value changes from FFh to 00h), an overflow interrupt (low-level pulse) is output provided the interrupt request is enabled by the TCR.OVIE bit.

For details on the corresponding interrupt vector number, see section 14, Interrupt Controller (ICUb), and Table 23.7, TMR Interrupt Sources.

23.2.2 Time Constant Register A (TCORA)

Address(es): TMR0.TCORA 0008 8204h, TMR1.TCORA 0008 8205h, TMR2.TCORA 0008 8214h, TMR3.TCORA 0008 8215h, TMR4.TCORA 0008 8224h, TMR5.TCORA 0008 8225h, TMR6.TCORA 0008 8234h, TMR7.TCORA 0008 8235h

	TMR0.TCORA(TMR2.TCORA, TMR4.TCORA, TMR6.TCORA)								TMR1.TCORA(TMR3.TCORA, TMR5.TCORA, TMR7.TCORA)							
	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

TCORA is an 8-bit readable/writable register.
TMR0.TCORA and TMR1.TCORA (TMR2.TCORA and TMR3.TCORA, TMR4.TCORA and TMR5.TCORA, TMR6.TCORA and TMR7.TCORA) comprise a single 16-bit register so they can be accessed together by a word transfer instruction.
The value in TCORA is continually compared with the value in TCNT. When a match is detected, the corresponding compare match A is generated, and a compare match A interrupt (low-level pulse) is output provided the interrupt request is enabled by the TCR.CMIEA bit.
However, comparison is not performed during writing to TCORA. The timer output from the TMOn pin can be freely controlled by this compare match A and the settings of the TCSR.OSA[1:0] bits.

23.2.3 Time Constant Register B (TCORB)

Address(es): TMR0.TCORB 0008 8206h, TMR1.TCORB 0008 8207h, TMR2.TCORB 0008 8216h, TMR3.TCORB 0008 8217h, TMR4.TCORB 0008 8226h, TMR5.TCORB 0008 8227h, TMR6.TCORB 0008 8236h, TMR7.TCORB 0008 8237h

	TMR0.TCORB(TMR2.TCORB, TMR4.TCORB, TMR6.TCORB)								TMR1.TCORB(TMR3.TCORB, TMR5.TCORB, TMR7.TCORB)							
	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

TCORB is an 8-bit readable/writable register.
TMR0.TCORB and TMR1.TCORB (TMR2.TCORB and TMR3.TCORB, TMR4.TCORB and TMR5.TCORB, TMR6.TCORB and TMR7.TCORB) comprise a single 16-bit register so they can be accessed together by a word transfer instruction.
The value in TCORB is continually compared with the value in TCNT. When a match is detected, the corresponding compare match B is generated, and a compare match B interrupt (low-level pulse) is output provided the interrupt request is enabled by the TCR.CMIEB bit.
However, comparison is not performed during writing to TCORB. The timer output from the TMOn pin can be freely controlled by this compare match B and the settings of the TCSR.OSB[1:0] bits.

23.2.4 Timer Control Register (TCR)

Address(es): TMR0.TCR 0008 8200h, TMR1.TCR 0008 8201h, TMR2.TCR 0008 8210h, TMR3.TCR 0008 8211h, TMR4.TCR 0008 8220h, TMR5.TCR 0008 8221h, TMR6.TCR 0008 8230h, TMR7.TCR 0008 8231h

	b7	b6	b5	b4	b3	b2	b1	b0
	CMIEB	CMIEA	OVIE	CCLR[1:0]		—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4, b3	CCLR[1:0]	Counter Clear*1	b4 b3 0 0: Clearing is disabled 0 1: Cleared by compare match A 1 0: Cleared by compare match B 1 1: Cleared by the external counter reset signal (Select edge or level by the TMRIS bit in TCCR.)	R/W
b5	OVIE	Timer Overflow Interrupt Enable	0: Overflow interrupt requests (OVIn) are disabled 1: Overflow interrupt requests (OVIn) are enabled	R/W
b6	CMIEA	Compare Match Interrupt Enable A	0: Compare match A interrupt requests (CMIAn) are disabled 1: Compare match A interrupt requests (CMIAn) are enabled	R/W
b7	CMIEB	Compare Match Interrupt Enable B	0: Compare match B interrupt requests (CMIBn) are disabled 1: Compare match B interrupt requests (CMIBn) are enabled	R/W

Note 1. To use an external counter reset signal, set the corresponding pin function. For details, refer to section 18, I/O Ports and section 19, Multi-Function Pin Controller (MPC).

CCLR[1:0] Bits (Counter Clear)

Select the condition by which TCNT is cleared.

OVIE Bit (Timer Overflow Interrupt Enable)

Selects whether overflow interrupt requests (OVIn) issued by TCNT are enabled or disabled.

CMIEA Bit (Compare Match Interrupt Enable A)

Selects whether compare match A interrupt requests (CMIAn) that are issued when the value of TCORA corresponds to that of TCNT are enabled or disabled.

CMIEB Bit (Compare Match Interrupt Enable B)

Selects whether compare match B interrupt requests (CMIBn) that are issued when the value of TCORB corresponds to that of TCNT are enabled or disabled.

23.2.5 Timer Counter Control Register (TCCR)

Address(es): TMR0.TCCR 0008 820Ah, TMR1.TCCR 0008 820Bh, TMR2.TCCR 0008 821Ah, TMR3.TCCR 0008 821Bh, TMR4.TCCR 0008 822Ah, TMR5.TCCR 0008 822Bh, TMR6.TCCR 0008 823Ah, TMR7.TCCR 0008 823Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	TMRIS	—	—	CSS[1:0]		CKS[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	CKS[2:0]	Clock Select*1	See Table 23.6.	R/W
b4, b3	CSS[1:0]	Clock Source Select	See Table 23.6.	R/W
b6, b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	TMRIS	Timer Reset Detection Condition Select	0: Cleared at rising edge of the external counter reset signal 1: Cleared when the external counter reset signal is high	R/W

Note 1. To use an external count clock, set the corresponding pin function. For details, refer to section 18, I/O Ports and section 19, Multi-Function Pin Controller (MPC).

CKS[2:0] Bits (Clock Select)
CSS[1:0] Bits (Clock Source Select)

The CKS[2:0] and CSS[1:0] bits select a clock. For details, see Table 23.6.

TMRIS Bit (Timer Reset Detection Condition Select)

This bit is enabled when the TCR.CCLR[1:0] bits are 11b (cleared by external counter reset signal) and selects the condition for detecting counter reset (level or edge).

Table 23.6 Clock Input to TCNT and Count Condition

Channel	TCCR Register CSS[1:0] b4	b3	CKS[2:0] b2	b1	b0	Description
TMR0 (TMR2, TMR4, TMR6)	0	0	—	0	0	Clock input prohibited
					1	Uses external count clock. Counts at rising edge*1.
				1	0	Uses external count clock. Counts at falling edge*1.
					1	Uses external count clock. Counts at both rising and falling edges*1.
	0	1	0	0	0	Uses internal clock. Counts at PCLK.
					1	Uses internal clock. Counts at PCLK/2.
				1	0	Uses internal clock. Counts at PCLK/8.
					1	Uses internal clock. Counts at PCLK/32.
			1	0	0	Uses internal clock. Counts at PCLK/64.
					1	Uses internal clock. Counts at PCLK/1024.
				1	0	Uses internal clock. Counts at PCLK/8192.
					1	Clock input prohibited
	1	0	—	—	—	Setting prohibited
	1	1	—	—	—	Counts at TMR1.TCNT (TMR3.TCNT, TMR5.TCNT, TMR7.TCNT) overflow signal*2.
TMR1 (TMR3, TMR5, TMR7)	0	0	—	0	0	Clock input prohibited
					1	Uses external count clock. Counts at rising edge*1.
				1	0	Uses external count clock. Counts at falling edge*1.
					1	Uses external count clock. Counts at both rising and falling edges*1.
	0	1	0	0	0	Uses internal clock. Counts at PCLK.
					1	Uses internal clock. Counts at PCLK/2.
				1	0	Uses internal clock. Counts at PCLK/8.
					1	Uses internal clock. Counts at PCLK/32.
			1	0	0	Uses internal clock. Counts at PCLK/64.
					1	Uses internal clock. Counts at PCLK/1024.
				1	0	Uses internal clock. Counts at PCLK/8192.
					1	Clock input prohibited
	1	0	—	—	—	Setting prohibited
	1	1	—	—	—	Counts at TMR0.TCNT (TMR2.TCNT, TMR4.TCNT, TMR6.TCNT) compare match A*2.

Note 1. To use an external count clock, set the corresponding pin function. For details, see section 18, I/O Ports and section 19, Multi-Function Pin Controller (MPC).

Note 2. If the clock input of TMR0 (TMR2, TMR4, TMR6) is the overflow signal of the TMR1.TCNT (TMR3.TCNT, TMR5.TCNT, TMR7.TCNT) counter and that of TMR1 (TMR3, TMR5, TMR7) is the compare match signal of the TMR0.TCNT (TMR2.TCNT, TMR4.TCNT, TMR6.TCNT) counter, no TCNT count clock is generated. Do not use this setting.

23.2.6 Timer Control/Status Register (TCSR)

- TMR0.TCSR, TMR2.TCSR, TMR4.TCSR, TMR6.TCSR

Address(es): TMR0.TCSR 0008 8202h, TMR2.TCSR 0008 8212h, TMR4.TCSR 0008 8222h, TMR6.TCSR 0008 8232h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	ADTE	OSB[1:0]		OSA[1:0]	
Value after reset:	x	x	x	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b1, b0	OSA[1:0]	Output Select A*1	b1 b0 0 0: No change 0 1: Low is output 1 0: High is output 1 1: Output is inverted (toggle output)	R/W
b3, b2	OSB[1:0]	Output Select B *1	b3 b2 0 0: No change 0 1: Low is output 1 0: High is output 1 1: Output is inverted (toggle output)	R/W
b4	ADTE	A/D Trigger Enable	0: A/D conversion start request in response to compare match A is disabled. 1: A/D conversion start request in response to compare match A is enabled.	R/W
b7 to b5	—	Reserved	These bits are read as an undefined value. The write value should be 1.	R/W

Note 1. When the OSA[1:0] and OSB[1:0] bits are all 0, the output enable signal corresponding to the TMOn pin is negated and a request for high-impedance output is issued to the I/O port. Timer output pin is low until the first compare match occurs after a reset when either of the OSA[1:0] or OSB[1:0] bits are 1.

OSA[1:0] Bits (Output Select A)

These bits select a method of TMOn pin output when compare match A of TCORA and TCNT occurs.

OSB[1:0] Bits (Output Select B)

These bits select a method of TMOn pin output when compare match B of TCORB and TCNT occurs.

- TMR1.TCSR, TMR3.TCSR, TMR5.TCSR, TMR7.TCSR

Address(es): TMR1.TCSR 0008 8203h, TMR3.TCSR 0008 8213h, TMR5.TCSR 0008 8223h, TMR7.TCSR 0008 8233h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	OSB[1:0]		OSA[1:0]	
Value after reset:	x	x	x	1	0	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b1, b0	OSA[1:0]	Output Select A*1	b1 b0 0 0: No change 0 1: Low is output 1 0: High is output 1 1: Output is inverted (toggle output)	R/W
b3, b2	OSB[1:0]	Output Select B *1	b3 b2 0 0: No change 0 1: Low is output 1 0: High is output 1 1: Output is inverted (toggle output)	R/W
b4	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b7 to b5	—	Reserved	These bits are read as an undefined value. The write value should be 1.	R/W

Note 1. When the OSA[1:0] and OSB[1:0] bits are all 0, the output enable signal corresponding to the TMOn pin is negated and a request for high-impedance output is issued to the I/O port. Timer output pin is low until the first compare match occurs after a reset when either of the OSA[1:0] or OSB[1:0] bits are 1.

OSA[1:0] Bits (Output Select A)

These bits select a method of TMOn pin output when compare match A of TCORA and TCNT occurs.

OSB[1:0] Bits (Output Select B)

These bits select a method of TMOn pin output when compare match B of TCORB and TCNT occurs.

23.3 Operation

23.3.1 Pulse Output

Figure 23.5 shows an example of the 8-bit timer being used to generate a pulse output with a desired duty cycle.

1. Set the TCR.CCLR[1:0] bits to 01b (cleared by compare match A) so that TCNT is cleared at a compare match of TCORA.
2. Set the TCSR.OSA[1:0] bits to 10b (high output) and TCSR.OSB[1:0] bits to 01b (low output), causing the output to change to high at a compare match of TCORA and to low at a compare match of TCORB.

With these settings, the 8-bit timer provides pulses output at a cycle determined by TCORA with a pulse width determined by TCORB. No software intervention is required.
The timer output pin is low after the TCSR.OSA[1:0] or TCSR.OSB[1:0] bits are set until the first compare match occurs after a reset.

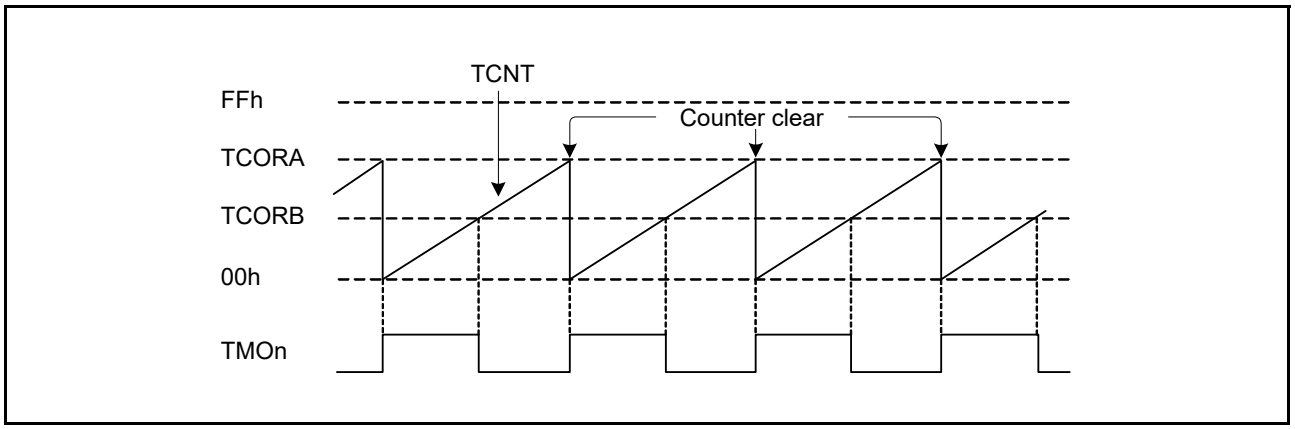


Figure 23.5 Example of Pulse Output (n = 0 to 7)

23.3.2 External Counter Reset Input

Figure 23.6 shows an example of the 8-bit timer being used to generate a pulse which is output after a desired delay time from a TMRIn input.

1. Set the TCR.CCLR[1:0] bits to 11b (cleared by external counter reset signal) and set the TMRIS bit in TCCR to 1 (cleared when the external counter reset signal is high) so that TCNT is cleared at the high level input of the TMRIn signal.
2. Set the TCSR.OSA[1:0] bits to 10b (high output) and the TCSR.OSB[1:0] bits to 01b (low output), causing the output to change to high at a compare match of TCORA and to low at a compare match of TCORB.

With these settings, the 8-bit timer provides pulses output at a desired delay time from a TMRIn input determined by TCORA and with a pulse width determined by TCORB and TCORA.

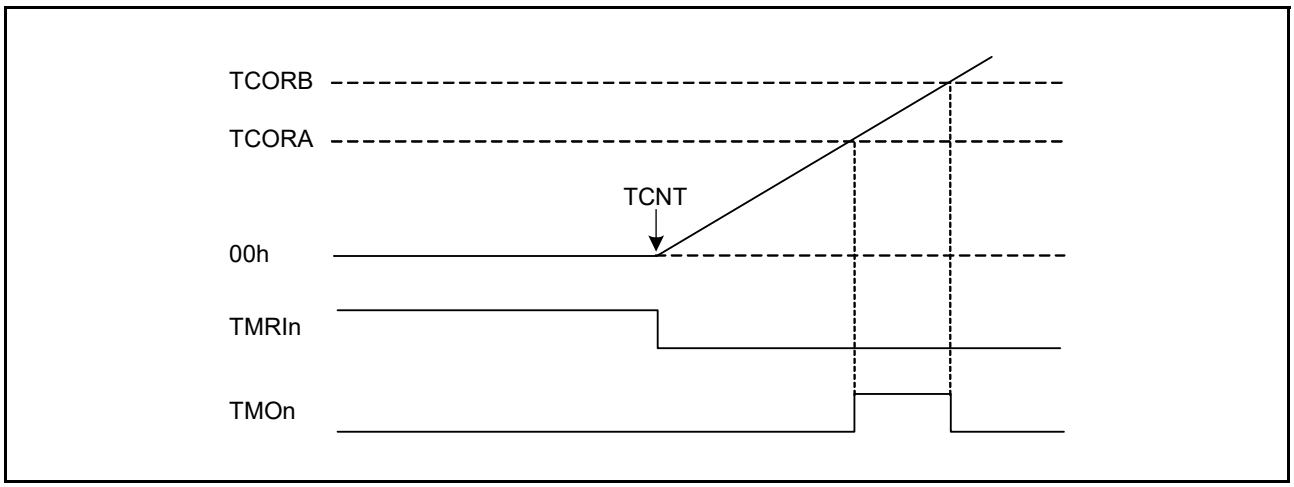


Figure 23.6 Example of External Counter Reset Signal Input (n = 0 to 7)

23.4 Operation Timing

23.4.1 TCNT Count Timing

Figure 23.7 shows the count timing of TCNT for internal clock. Figure 23.8 shows the count timing of TCNT for external clock.

Note that the external clock pulse width must be at least 1.5 PCLK cycles for increment at a single edge, and at least 2.5 PCLK cycles for increment at both edges. The counter will not increment correctly if the pulse width is less than these values.

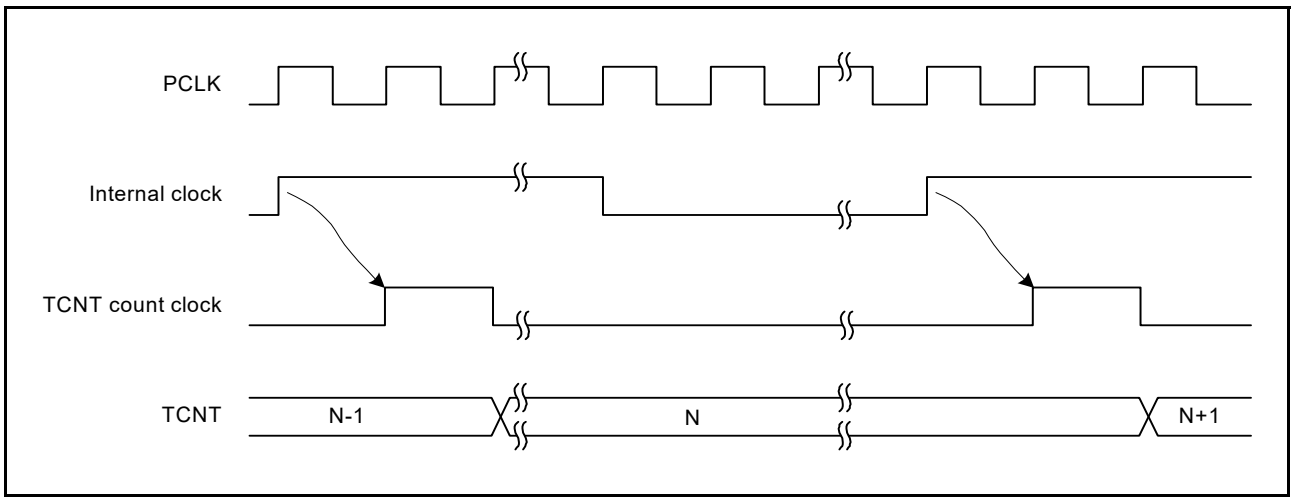


Figure 23.7 Count Timing for Internal Clock

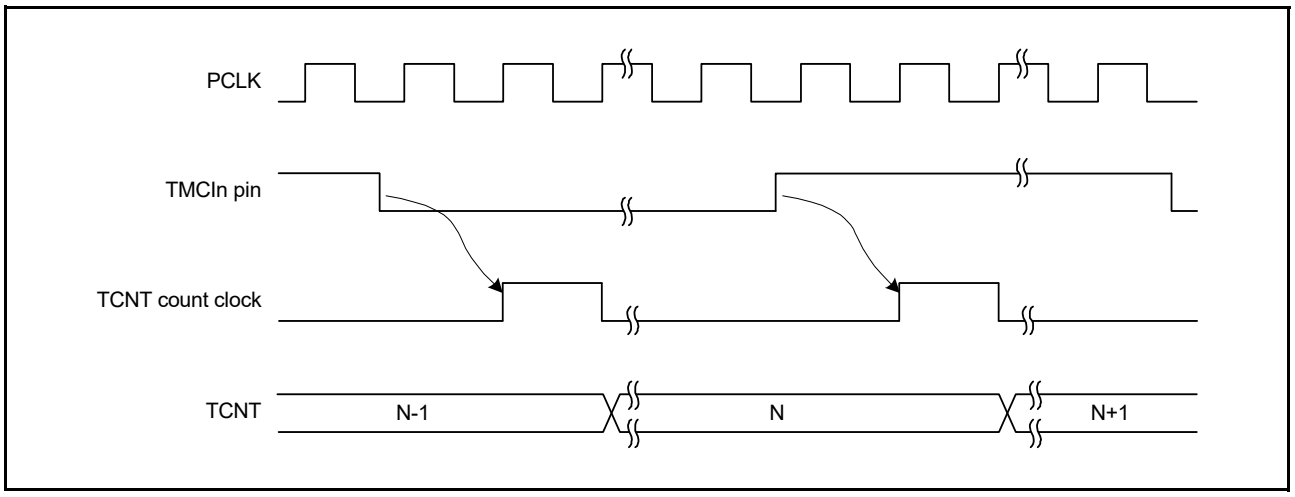


Figure 23.8 Count Timing for External Clock (at Both Edges)

23.4.2 Timing of Interrupt Signal Output on a Compare Match

A compare match refers to a match between the value of the TCORA or TCORB register and the TCNT, and a compare match interrupt signal is output at this time if the interrupt request is enabled. The compare match is generated in the last cycle in which the values match (at the time at which the value counted by TCNT to produce the match is updated). Accordingly, after a match between TCNT and the TCORA or TCORB register is detected, the compare match is not actually generated until the next cycle of the TCNT count clock. Figure 23.9 shows the timing of output of the interrupt signal.

For the corresponding interrupt vector number, see section 14, Interrupt Controller (ICUb) and Table 23.7.

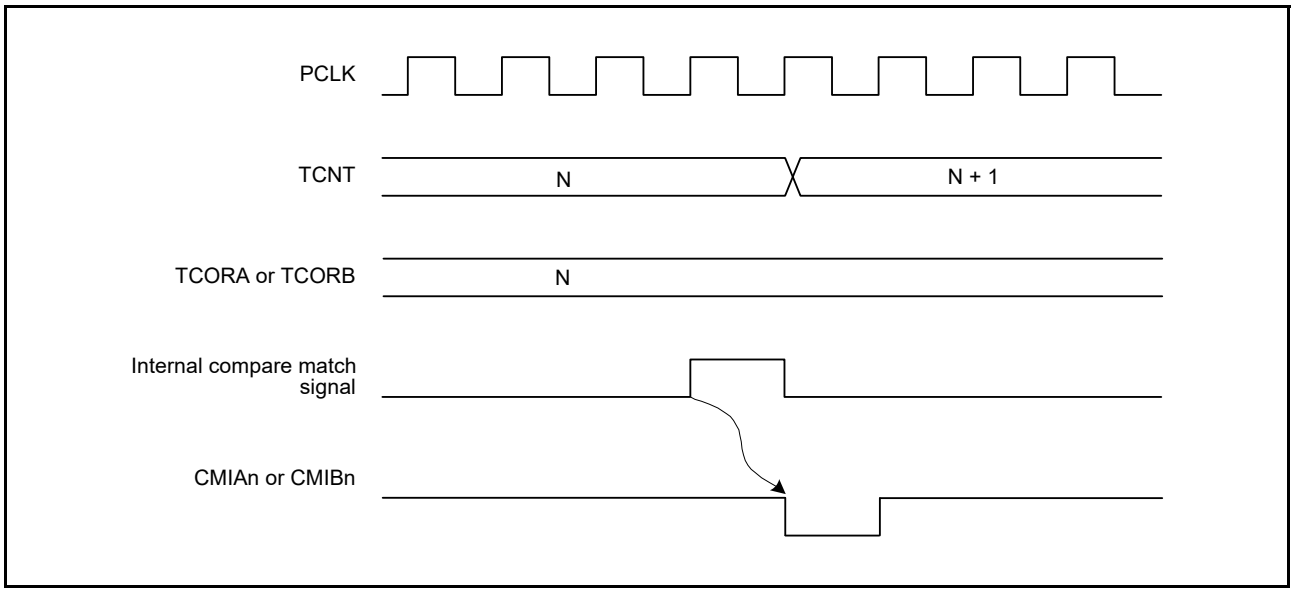


Figure 23.9 Timing of Interrupt Flag Setting to 1 at Compare Match (n = 0 to 7)

23.4.3 Timing of Timer Output Signal at Compare Match

When a compare match signal is generated, the output value specified by the TCSR.OSA[1:0] and OSB[1:0] bits is output on the timer output pin (TMOn).

Figure 23.10 shows the timing when the timer output is toggled by the compare match A signal.

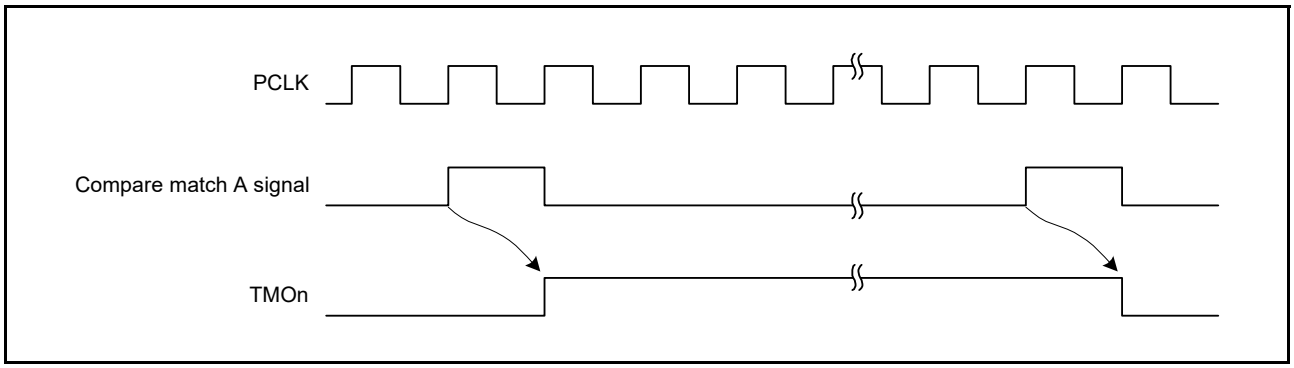


Figure 23.10 Timing of Timer Output Signal at Compare Match A Signal (n = 0 to 7)

23.4.4 Timing of Counter Clear by Compare Match

TCNT is cleared when compare match A or B occurs, depending on the settings of the TCR.CCLR[1:0] bits. Figure 23.11 shows the timing of this operation.

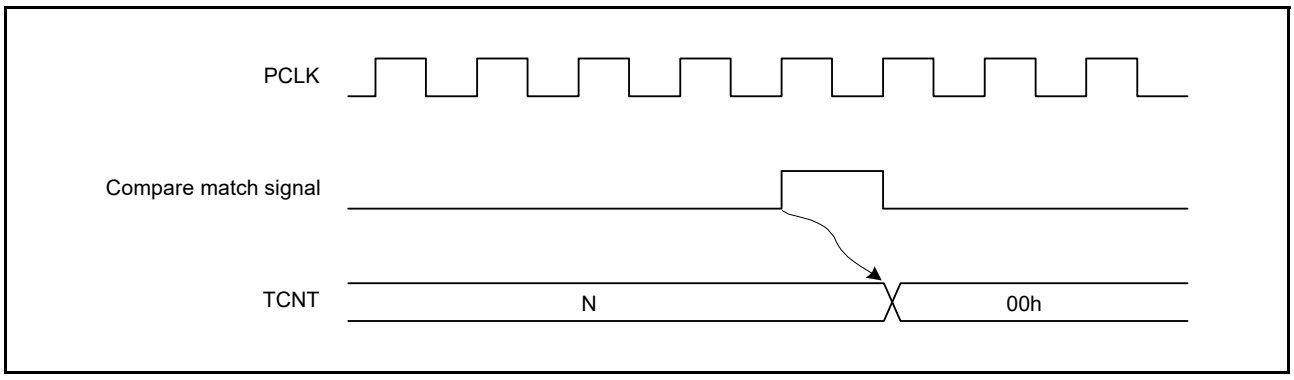


Figure 23.11 Timing of Counter Clear by Compare Match

23.4.5 Timing of the External Reset for TCNT

TCNT is cleared at the rising edge or high level of an external counter reset signal, depending on the settings of the TCR.CCLR[1:0] bits. At least 2 PCLK cycles are required from a reset input to clearing of TCNT. Figure 23.12 and Figure 23.13 show the timing of this operation.

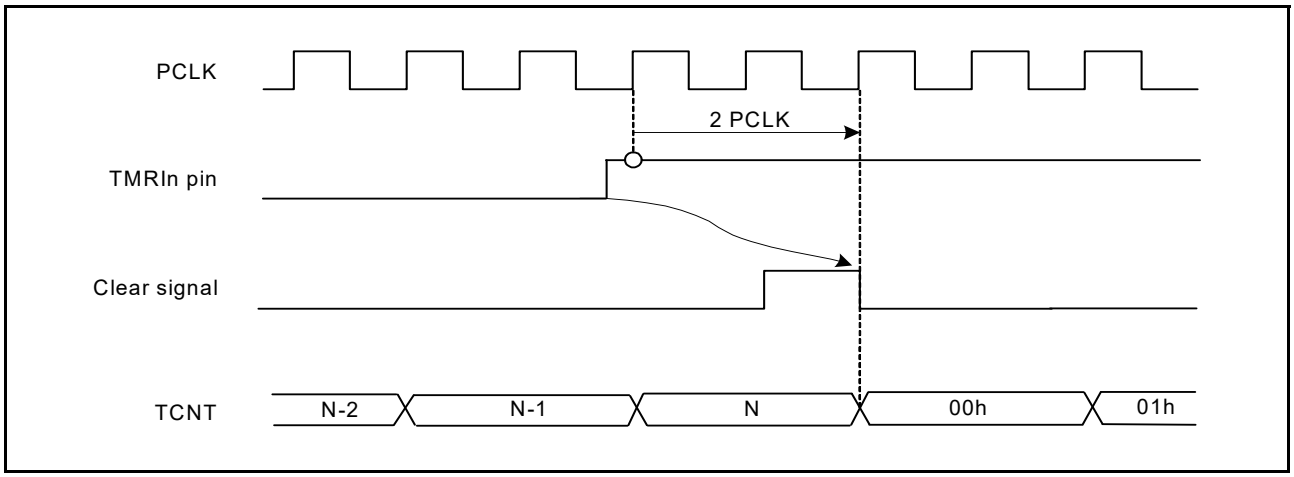


Figure 23.12 Clear Timing by External Counter Reset Signal (Rising Edge)

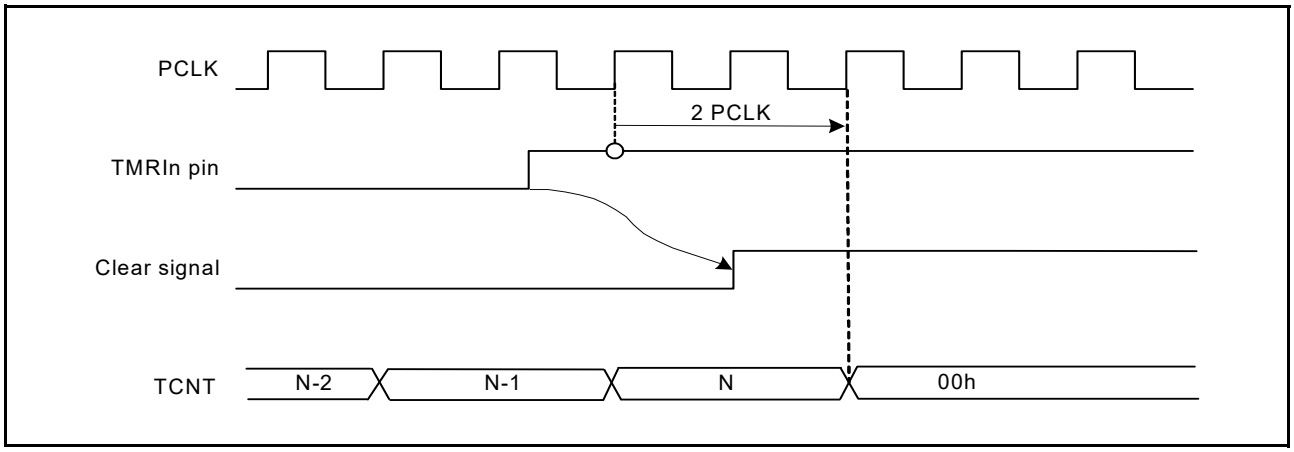


Figure 23.13 Clear Timing by External Counter Reset Signal (High Level)

23.4.6 Timing of Interrupt Signal Output on an Overflow

When TCNT overflows (changes from FFh to 00h), an overflow interrupt signal is output if this interrupt request is enabled.

Figure 23.14 shows the timing of output of the interrupt signal.

For the corresponding interrupt vector number, see section 14, Interrupt Controller (ICUb) and Table 23.7.

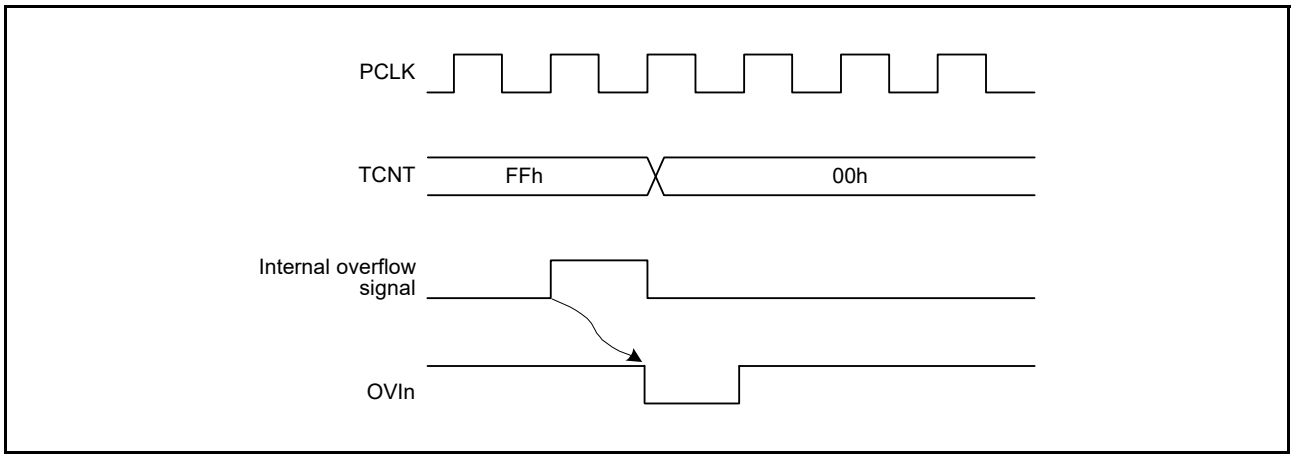


Figure 23.14 Timing of Overflow Interrupt Flag Setting to 1 (n = 0 to 7)

23.5 Operation with Cascaded Connection

If the CSS[1:0] bits in either TMR0.TCCR or TMR1.TCCR are set to 11b, the TMR of the two channels are cascaded. With this configuration, a single 16-bit timer could be used (16-bit counter mode) or compare matches of TMR0 could be counted by TMR1 (compare match count mode).

Supplementary information: This section describes unit 0. The operation of unit 1, unit 2, and unit 3 with cascaded connection is the same as unit 0.

23.5.1 16-Bit Count Mode

When the TMR0.TCCR.CSS[1:0] bits are set to 11b, the timer functions as a single 16-bit timer with TMR0 occupying the upper 8 bits and TMR1 occupying the lower 8 bits.

(1) Counter Clear Specification

- The settings of the TMR0.TCR.CCLR[1:0] bits become effective for the 16-bit counter. If the TMR0.TCR.CCLR[1:0] bits have been set for counter clear at compare match, the 16-bit counter (TMR0.TCNT and TMR1.TCNT together) is cleared when a 16-bit compare match event occurs. The 16-bit counter (TMR0.TCNT and TMR1.TCNT together) is cleared even if counter clear by the TMRI0 pin has been set.
- The settings of the TMR1.TCR.CCLR[1:0] bits are ignored.

(2) Pin Output

- Control of output from the TMO0 pin by the TMR0.TCSR.OSA[1:0] and OSB[1:0] bits is in accordance with the 16-bit compare match conditions.
- Control of output from the TMO1 pin by the TMR1.TCSR.OSA[1:0] and OSB[1:0] bits is in accordance with the lower 8-bit compare match conditions.

23.5.2 Compare Match Count Mode

When the TMR1.TCCR.CSS[1:0] bits are set to 11b, TMR1.TCNT counts the number of occurrences of compare match A for TMR0. TMR0 and TMR1 are controlled independently. Conditions such as generation of interrupts, output from the TMOn (n = 0, 1) pin, and counter clear are in accordance with the settings for each channel.

23.6 Interrupt Sources

23.6.1 Interrupt Sources and DTC Activation

There are three interrupt sources for TMRn: CMIAn, CMIBn, and OVIn. Their interrupt sources and priorities are listed in Table 23.7.
It is also possible to activate the DTC by means of CMIAn and CMIBn interrupts.

Table 23.7 TMR Interrupt Sources

Name	Interrupt Sources	DTC Activation	Priority
CMIA0	TMR0.TCORA compare match	Possible	High
CMIB0	TMR0.TCORB compare match	Possible	
OVI0	TMR0.TCNT overflow	Not possible	
CMIA1	TMR1.TCORA compare match	Possible	
CMIB1	TMR1.TCORB compare match	Possible	
OVI1	TMR1.TCNT overflow	Not possible	
CMIA2	TMR2.TCORA compare match	Possible	
CMIB2	TMR2.TCORB compare match	Possible	
OVI2	TMR2.TCNT overflow	Not possible	
CMIA3	TMR3.TCORA compare match	Possible	
CMIB3	TMR3.TCORB compare match	Possible	
OVI3	TMR3.TCNT overflow	Not possible	
CMIA4	TMR4.TCORA compare match	Possible	
CMIB4	TMR4.TCORB compare match	Possible	
OVI4	TMR4.TCNT overflow	Not possible	
CMIA5	TMR5.TCORA compare match	Possible	
CMIB5	TMR5.TCORB compare match	Possible	
OVI5	TMR5.TCNT overflow	Not possible	
CMIA6	TMR6.TCORA compare match	Possible	
CMIB6	TMR6.TCORB compare match	Possible	
OVI6	TMR6.TCNT overflow	Not possible	
CMIA7	TMR7.TCORA compare match	Possible	
CMIB7	TMR7.TCORB compare match	Possible	
OVI7	TMR7.TCNT overflow	Not possible	Low

23.6.2 Startup of the A/D Converter

The compare match A of TMR0, TMR2, TMR4, and TMR6 allows the A/D converter to be started.
An A/D conversion start request is issued to the A/D converter in response to a generation of compare match A when the TMRn.TCSR.ADTE bit is 1 (i.e., when an A/D conversion request in response to compare match A is enabled). In this case, the conversion trigger for the 8-bit timer should be selected in the A/D converter to start A/D conversion.

Table 23.8 Startup of A/D Converter

A/D Converter	TMR Unit No.	Target	A/D Conversion Start Request
S12AD, S12AD1, S12AD2 (12-bit A/D converter)	0	Compare match between TMR0.TCORA and TMR0.TCNT	TMTRG0AN_0
	1	Compare match between TMR2.TCORA and TMR2.TCNT	TMTRG0AN_1
	2	Compare match between TMR4.TCORA and TMR4.TCNT	TMTRG0AN_2
	3	Compare match between TMR6.TCORA and TMR6.TCNT	TMTRG0AN_3

23.7 Usage Notes

23.7.1 Module Stop State Setting

Operation of the TMR can be disabled or enabled by using the module stop control registers. The initial setting is for halting of TMR operation. Register access becomes possible after release from the module stop state. For details, see section 11, Low Power Consumption.

23.7.2 Notes on Setting Cycle

If the compare match is selected for counter clear, TCNT is cleared at the last PCLK in the cycle in which the value of TCNT matches with that of TCORA or TCORB. TCNT updates the counter value at this last state. Therefore, the counter frequency is obtained by the following formula (f: Counter frequency, PCLK: Operating frequency, N: TCORA and TCORB register setting value).

$$f = PCLK / (N + 1)$$

23.7.3 Conflict between TCNT Write and Counter Clear

If a counter clear signal is generated concurrently with CPU write to TCNT, the clear takes priority and the write is not performed as shown in Figure 23.15.

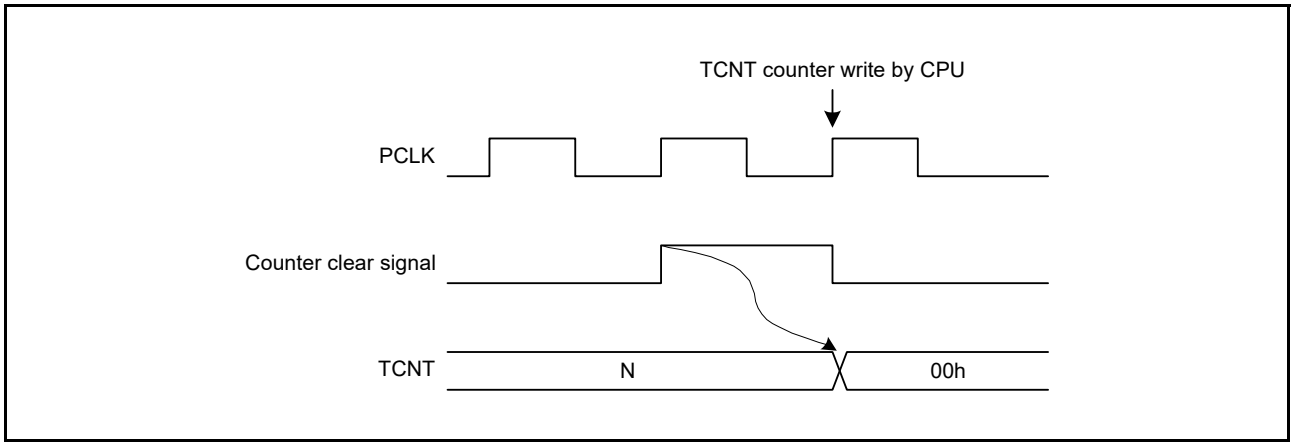


Figure 23.15 Conflict between TCNT Write and Counter Clear

23.7.4 Conflict between TCNT Write and Increment

Even if a counting-up signal is generated concurrently with CPU write to TCNT, the counting-up is not performed and the write takes priority as shown in Figure 23.16.

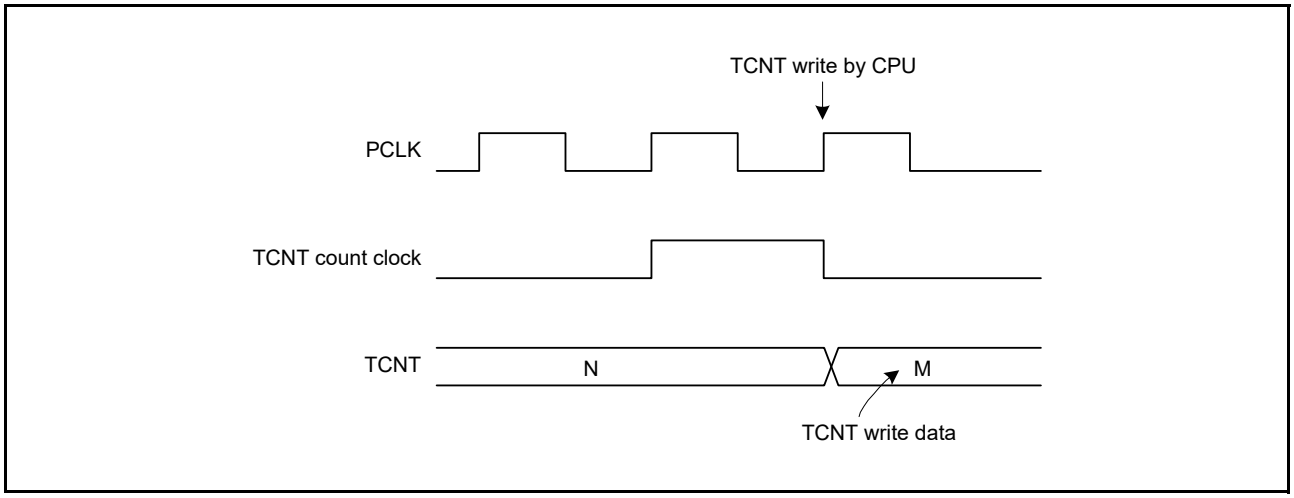


Figure 23.16 Conflict between TCNT Write and Increment

23.7.5 Conflict between TCORA or TCORB Write and Compare Match

Even if a compare match signal is generated simultaneously with CPU write to TCORA or TCORB as shown in Figure 23.17, the write takes priority and the compare match signal does not reach High level.

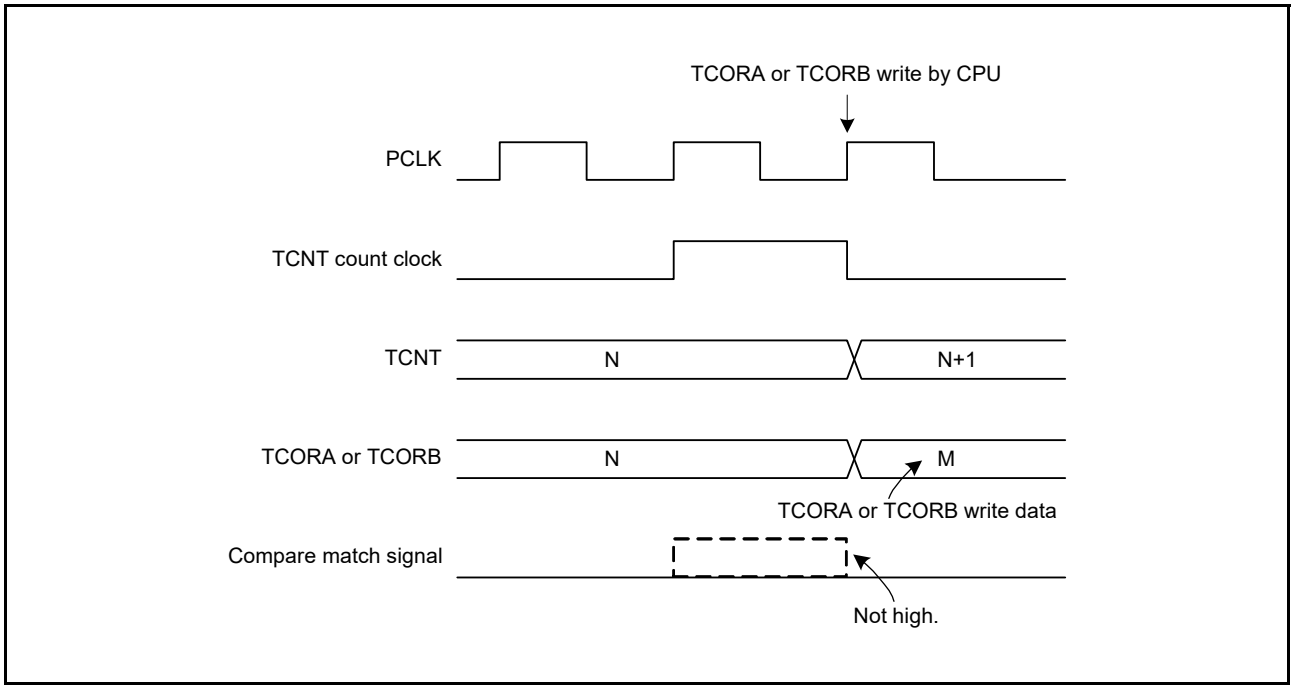


Figure 23.17 Conflict between TCORA or TCORB Write and Compare Match

23.7.6 Conflict between Compare Matches A and B

If compare match events A and B occur at the same time, the 8-bit timer operates in accordance with the priorities for the output methods high for compare match A and compare match B, as listed in Table 23.9.

Table 23.9 Timer Output Priorities

Output Setting	Priority
Toggle output	High
High output	↑
Low output	
No change	Low

23.7.7 Switching of Internal Clocks and TCNT Operation

TCNT may be incremented erroneously depending on when the internal clock is switched. Table 23.10 lists the relationship between the timing at which the internal clock is switched (by writing to the TCCR.CKS[2:0] bits) and the operation of TCNT.

When TCNT count clock is generated from an internal clock, the rising edge of the internal clock pulse are always monitored. If the signal levels of the clocks before and after switching change from low to high as shown in No. 2 in Table 23.10, the change is considered as an edge. Therefore, a TCNT count clock is generated and TCNT is incremented.

The erroneous increment of TCNT can also happen when switching between internal and internal clocks.

Table 23.10 Switching of Internal Clocks and TCNT Operation (1/2)

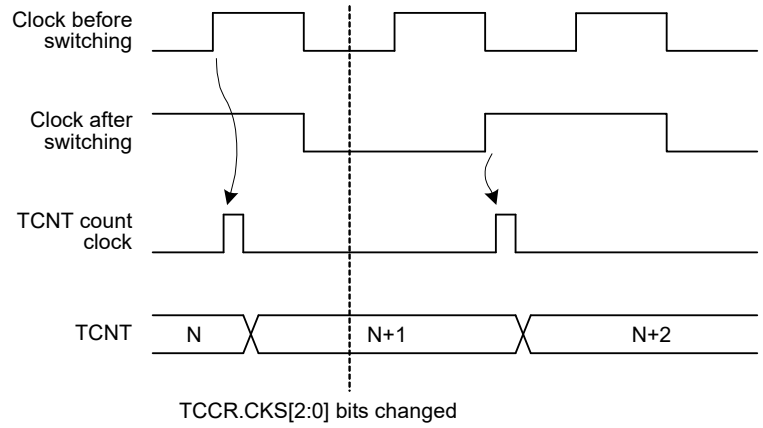
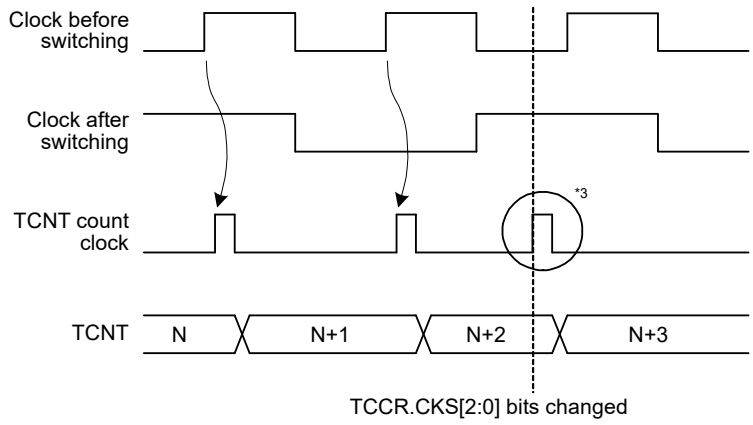
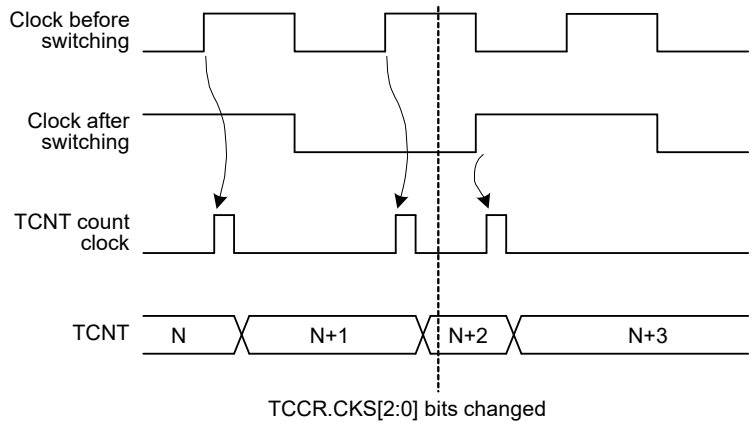
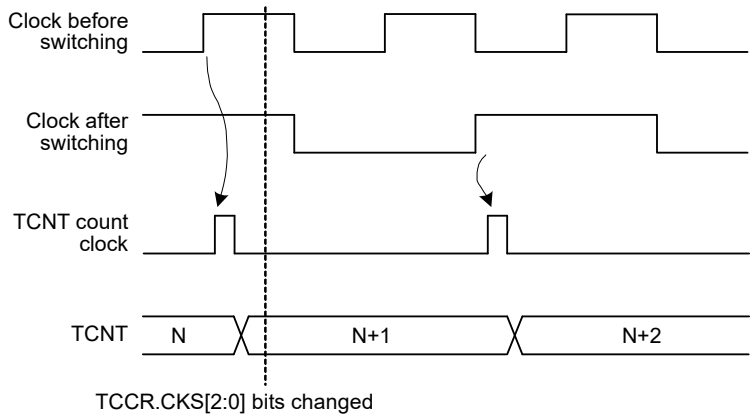
No.	Timing to Change the TCCR.CKS[2:0] Bits	TCNT Counter Operation
1	Switching from low to low*1	

Table 23.10 Switching of Internal Clocks and TCNT Operation (2/2)

No.	Timing to Change the TCCR.CKS[2:0] Bits	TCNT Counter Operation
2	Switching from low to high*2	
3	Switching from high to low*4	
4	Switching from high to high	

Note 1. Includes switching from low to stop, and from stop to low.
Note 2. Includes switching from stop to high.
Note 3. Generated because the change of the signal levels is considered as an edge; TCNT counter is incremented.
Note 4. Includes switching from high to stop.

23.7.8 Clock Source Setting with Cascaded Connection

If 16-bit counter mode and compare match count mode are specified at the same time, count clocks for TMR0.TCNT and TMR1.TCNT (TMR2.TCNT and TMR3.TCNT, TMR4.TCNT and TMR5.TCNT, TMR6.TCNT and TMR7.TCNT) are not generated, and the counter stops. Do not specify 16-bit counter mode and compare match count mode simultaneously.

23.7.9 Continuous Output of Compare Match Interrupt Signal

When TCORA or TCORB is set to 00h, PCLK/1 is set as the internal clock, and compare match is set as the counter clear source, the TCNT counter remains 00h and is not updated, and a compare match interrupt signal is output continuously to form a flat signal level.
At this time, the interrupt controller cannot detect the second and subsequent interrupts.
Figure 23.18 shows operation timing when the compare match interrupt signal is continuously output.

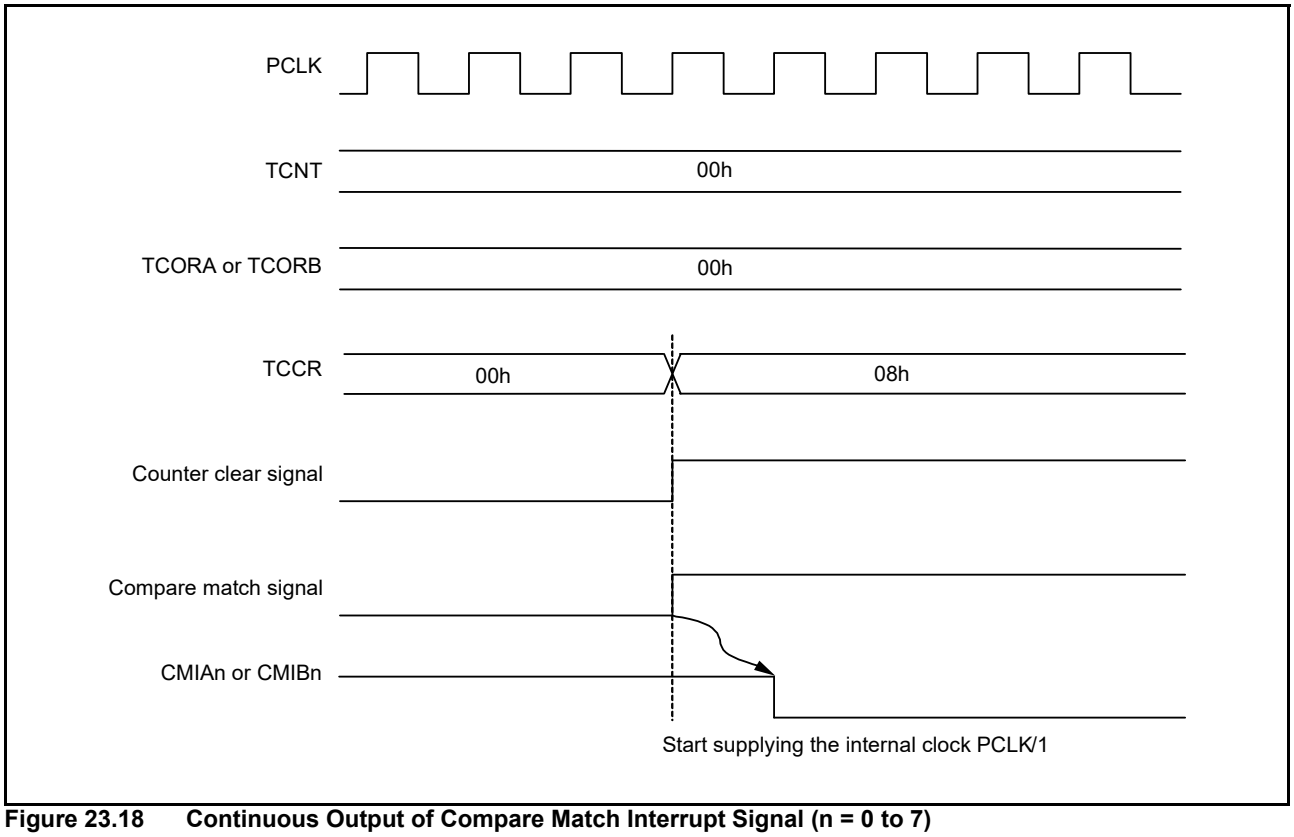


Figure 23.18 Continuous Output of Compare Match Interrupt Signal (n = 0 to 7)

24. Compare Match Timer (CMT)

This MCU has two on-chip compare match timer (CMT) units (unit 0 and unit 1), each consisting of a two-channel 16-bit timer (i.e., a total of four channels). The CMT has a 16-bit counter, and can generate interrupts at set intervals.
In this section, “PCLK” is used to refer to PCLKB.

24.1 Overview

Table 24.1 lists the specifications for the CMT.
Figure 24.1 shows a block diagram of the CMT (unit 0). A two-channel CMT constitutes a unit. Unit 0 and unit 1 are the same in terms of specifications. Compare match timer start register 0 (CMSTR0) and compare match interrupts (CMI0 and CMI1) of unit 0 correspond to compare match timer start register 1 (CMSTR1) and compare match interrupts (CMI2 and CMI3) of unit 1.

Table 24.1 CMT Specifications

Item	Description
Count clocks	• Four frequency dividing clocks One clock from PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected for each channel.
Interrupt	A compare match interrupt can be requested for each channel.
Low power consumption function	Each unit can be placed in a module stop state.

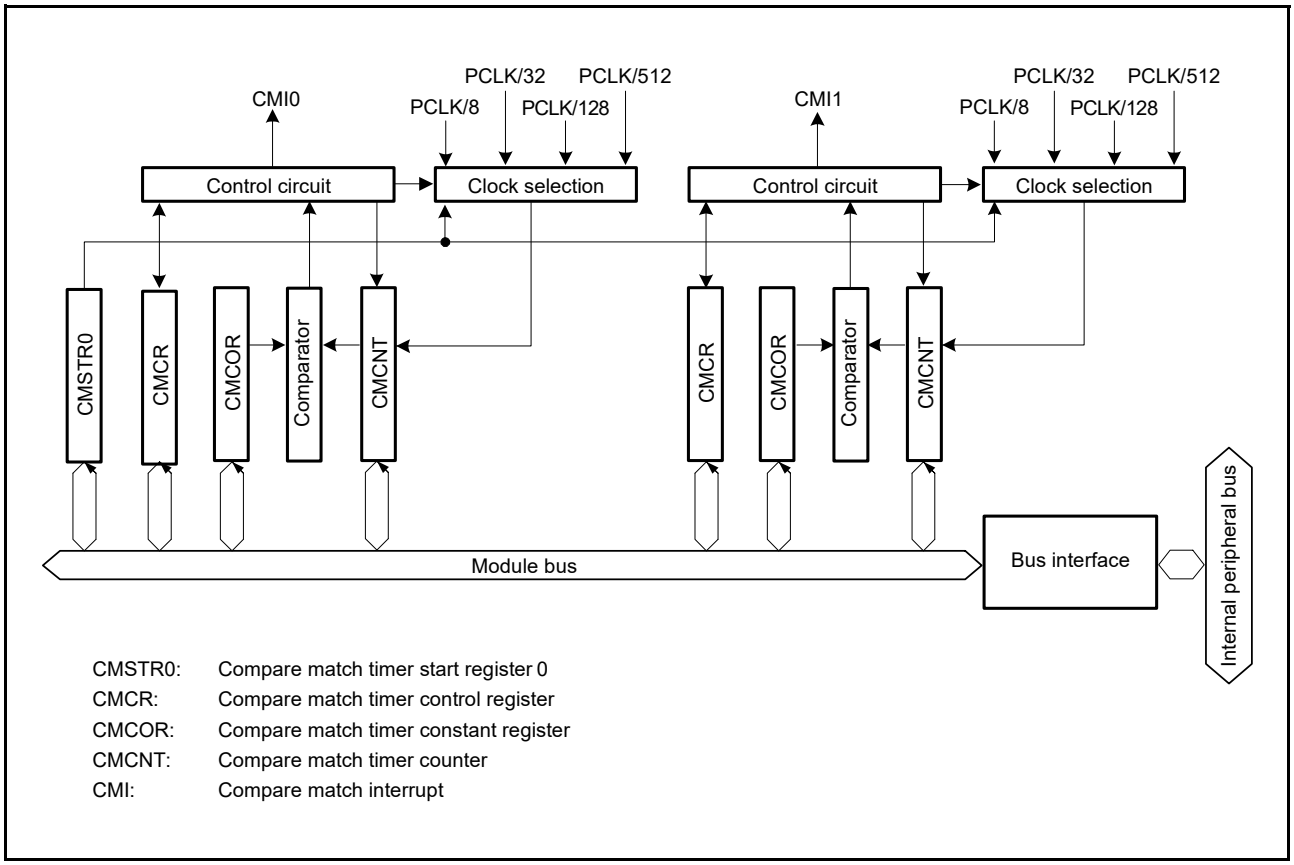


Figure 24.1 CMT (Unit 0) Block Diagram

24.2 Register Descriptions

24.2.1 Compare Match Timer Start Register 0 (CMSTR0)

Address(es): 0008 8000h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	STR1	STR0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	STR0	Count Start 0	0: CMT0.CMCNT count is stopped. 1: CMT0.CMCNT count is started.	R/W
b1	STR1	Count Start 1	0: CMT1.CMCNT count is stopped. 1: CMT1.CMCNT count is started.	R/W
b15 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

24.2.2 Compare Match Timer Start Register 1 (CMSTR1)

Address(es): 0008 8010h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	STR3	STR2
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	STR2	Count Start 2	0: CMT2.CMCNT count is stopped. 1: CMT2.CMCNT count is started.	R/W
b1	STR3	Count Start 3	0: CMT3.CMCNT count is stopped. 1: CMT3.CMCNT count is started.	R/W
b15 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

24.2.3 Compare Match Timer Control Register (CMCR)

Address(es): CMT0.CMCR 0008 8002h, CMT1.CMCR 0008 8008h, CMT2.CMCR 0008 8012h, CMT3.CMCR 0008 8018h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	CMIE	—	—	—	—	CKS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	x	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b1, b0	CKS[1:0]	Clock Select	b1 b0 0 0: PCLK/8 0 1: PCLK/32 1 0: PCLK/128 1 1: PCLK/512	R/W
b5 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	CMIE	Compare Match Interrupt Enable	0: Compare match interrupt (CMIn) disabled 1: Compare match interrupt (CMIn) enabled	R/W
b7	—	Reserved	This bit is read as undefined. The write value should be 1.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CKS[1:0] Bits (Clock Select)

These bits select the count source from four frequency dividing clocks obtained by dividing the peripheral module clock (PCLK).

When the CMSTRm.STRn (m = 0, 1; n = 0 to 3) bit is set to 1, the CMCNT counter starts counting up on the clock selected with the CKS[1:0] bits.

CMIE Bit (Compare Match Interrupt Enable)

The CMIE bit enables or disables compare match interrupt (CMIn) (n = 0 to 3) generation when the CMCNT counter and the CMCOR register values match.

24.2.4 Compare Match Counter (CMCNT)

Address(es): CMT0.CMCNT 0008 8004h, CMT1.CMCNT 0008 800Ah, CMT2.CMCNT 0008 8014h, CMT3.CMCNT 0008 801Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The CMCNT counter is a readable/writable up-counter.
When an frequency dividing clock is selected by the CMCR.CKS[1:0] bits and the CMSTRm.STRn (m = 0, 1; n = 0 to 3) bit is set to 1, the CMCNT counter starts counting up using the selected clock.
When the value in the CMCNT counter and the value in the CMCOR register match, the CMCNT counter is set to 0000h. At the same time, a compare match interrupt (CMIn) (n = 0 to 3) is generated.

24.2.5 Compare Match Constant Register (CMCOR)

Address(es): CMT0.CMCOR 0008 8006h, CMT1.CMCOR 0008 800Ch, CMT2.CMCOR 0008 8016h, CMT3.CMCOR 0008 801Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

The CMCOR register is a readable/writable register to set a value for compare match with the CMCNT counter.

24.3 Operation

24.3.1 Periodic Count Operation

When an frequency dividing clock is selected by the CMCR.CKS[1:0] bits and the CMSTRm.STRn (m = 0, 1; n = 0 to 3) bit is set to 1, the CMCNT counter starts counting up using the selected clock.
When the value in the counter and the value in the register match, a compare match interrupt (CMIn) (n = 0 to 3) is generated. The CMCNT counter then starts counting up again from 0000h. Figure 24.2 shows the operation of the CMCNT counter.

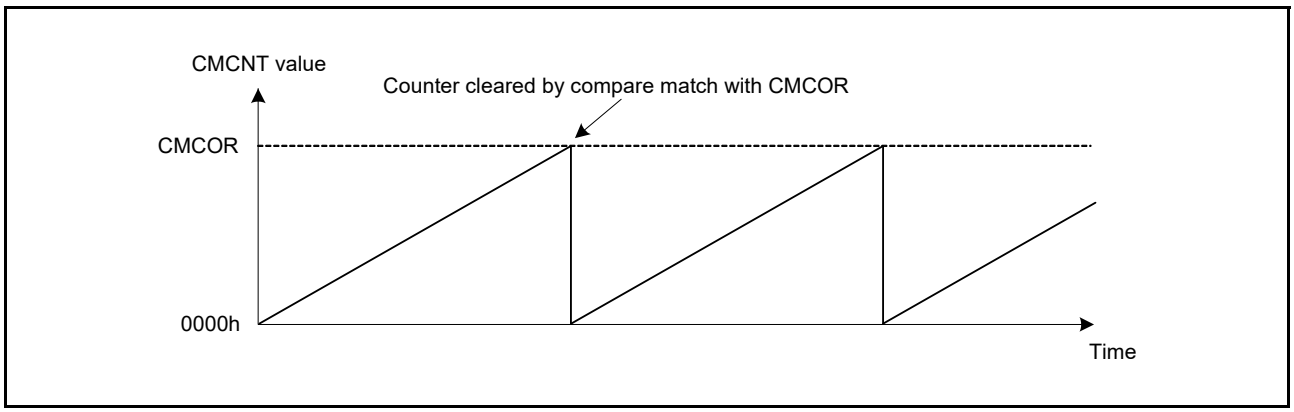


Figure 24.2 CMCNT Counter Operation

24.3.2 CMCNT Count Timing

As the count clock to be input to the CMCNT counter, one of four frequency dividing clocks (PCLK/8, PCLK/32, PCLK/128, and PCLK/512) obtained by dividing the peripheral module clock (PCLK) can be selected with the CMCR.CKS[1:0] bits. Figure 24.3 shows the timing of the CMCNT counter.

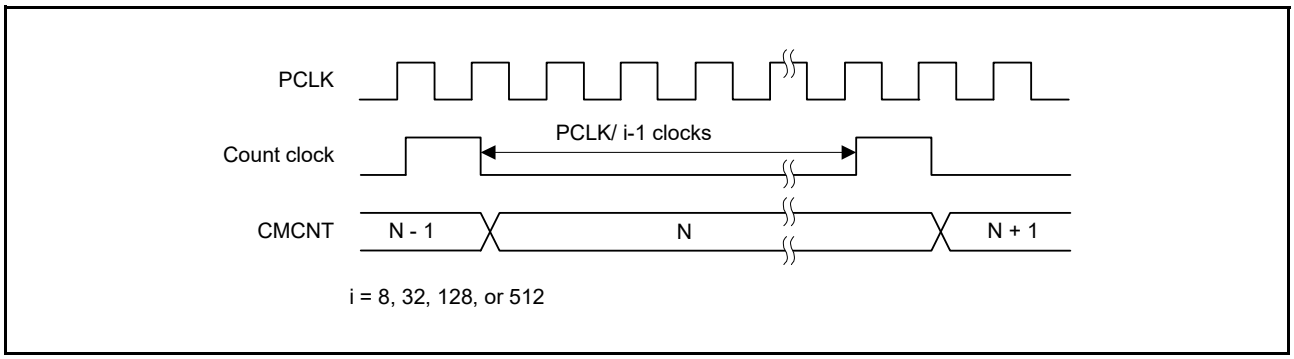


Figure 24.3 CMCNT Count Timing

24.4 Interrupts

24.4.1 Interrupt Sources

The CMT has channels and each of them to which a different vector address is allocated has a compare match interrupt (CMIn) (n = 0 to 3). When a compare match interrupt occurs, the corresponding interrupt request is output.
When the interrupt request is used to generate a CPU interrupt, the priority of channels can be changed by the interrupt controller settings. For details, see section 14, Interrupt Controller (ICUb).

Table 24.2 CMT Interrupt Sources

Name	Interrupt Sources	DTC Activation
CMI0	Compare match in CMT0	Possible
CMI1	Compare match in CMT1	Possible
CMI2	Compare match in CMT2	Possible
CMI3	Compare match in CMT3	Possible

24.4.2 Timing of Compare Match Interrupt Generation

When the CMCNT counter and the CMCOR register match, a compare match interrupt (CMIn) (n = 0 to 3) is generated. A compare match signal is generated at the last state in which the values match (the timing when the CMCNT counter updates the matched count value). That is, after a match between the CMCOR register and the CMCNT counter, the compare match signal is not generated until the next the CMCNT counter input clock.
Figure 24.4 shows the timing of a compare match interrupt.

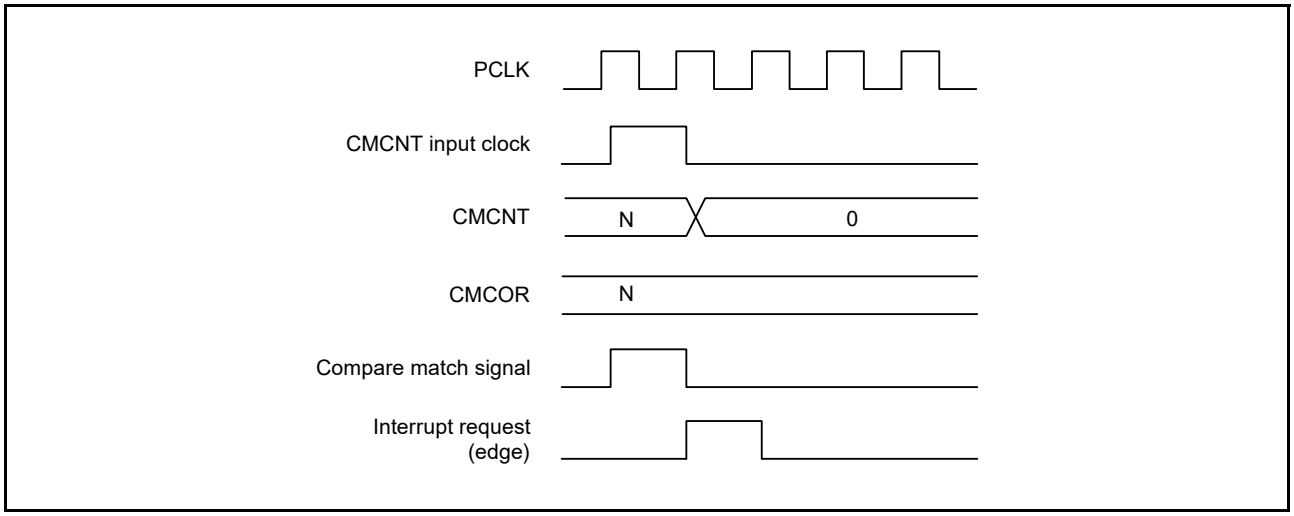


Figure 24.4 Timing of a Compare Match Interrupt

24.5 Usage Notes

24.5.1 Setting the Module Stop Function

The CMT can be enabled or disabled using the module stop control register. After a reset, the CMT is in the module stop state. The registers can be accessed by releasing the module stop state. For details, refer to section 11, Low Power Consumption.

24.5.2 Conflict between CMCNT Counter Writing and Compare Match

When the compare match signal is generated while writing to the CMCNT counter, clearing the CMCNT counter has priority over writing to it. In this case, the CMCNT counter is not written to. Figure 24.5 shows the timing to clear the CMCNT counter.

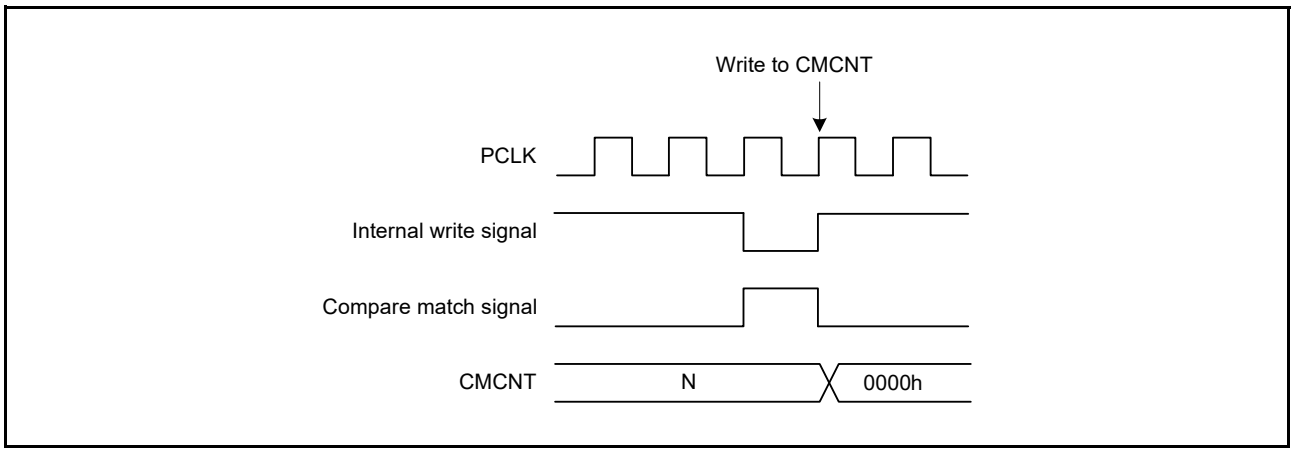


Figure 24.5 Conflict between CMCNT Counter Writing and Compare Match

24.5.3 Conflict between CMCNT Counter Writing and Incrementing

If writing to the counter and the incrementing conflict, the writing has priority over the incrementing. Figure 24.6 shows the timing to write the CMCNT counter.

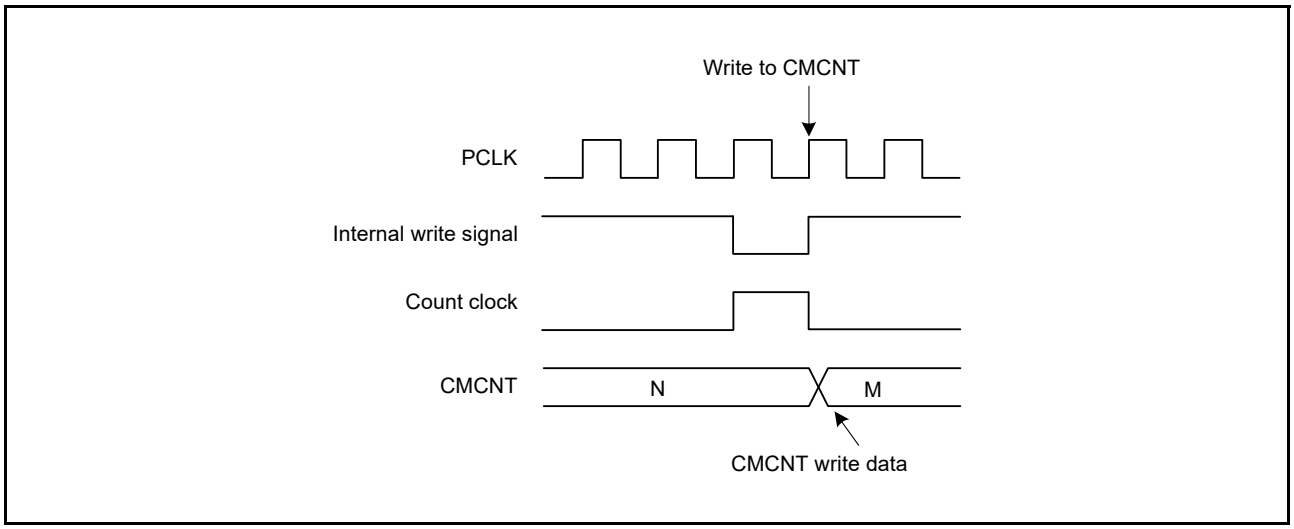


Figure 24.6 Conflict between CMCNT Counter Writing and Incrementing

25. Independent Watchdog Timer (IWDTa)

In this section, “PCLK” is used to refer to PCLKB.

25.1 Overview

The independent watchdog timer (IWDT) can be used to detect programs being out of control.
The user can detect when a program runs out of control if an underflow occurs, by creating a program that refreshes the IWDT counter before it underflows.
The functions of the IWDT are different from those of the WDT in the following respects.

- The divided IWDT-dedicated low-speed clock (IWDTCLK) is used as the count source (not affected by the PCLK).
- When making a transition to sleep mode, software standby mode, or deep sleep mode, the IWDTCSTPR.SLCSTP bit or the OFS0.IWDTSLCSTP bit can be used to select whether to stop the counter or not.

Table 25.1 lists the specifications of the IWDT and Figure 25.1 shows a block diagram of the IWDT.

Table 25.1 IWDT Specifications

Item	Description
Count source*1	IWDT-dedicated clock (IWDTCLK)
Clock divide ratio	Divide by 1, 16, 32, 64, 128, or 256
Counter operation	Counting down using a 14-bit down-counter
Conditions for starting the counter	• Counting automatically starts after a reset (auto-start mode) • Counting is started (register start mode) by refreshing the counter (writing 00h and then FFh to the IWDTRR register).
Conditions for stopping the counter	• Reset (the down-counter and other registers return to their initial values) • A counter underflows or a refresh error occurs Counting restarts (In auto-start mode, counting automatically restarts after a reset or after a non-maskable interrupt request is output. In register start mode, counting restarts after refreshing.)
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
Reset output sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Non-maskable interrupt sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Reading the counter value	The down-counter value can be read by the IWDTSR register.
Output signal (internal signal)	• Reset output • Interrupt request output • Sleep mode count stop control output
Auto-start mode (controlled by option function select register 0 (OFS0))	• Selecting the clock frequency divide ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selecting the reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, or deep sleep mode (OFS0.IWDTSLCSTP bit)
Register start mode (controlled by the IWDT registers)	• Selecting the clock frequency divide ratio after refreshing (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting the reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, or deep sleep mode (IWDTCSTPR.SLCSTP bit)

Note 1. Satisfy the frequency of the peripheral module clock (PCLK) ≥ 4 × (the frequency of the count source after divide).

To use the IWDT, the IWDT-dedicated clock (IWDTCLK) should be supplied so that the IWDT operates even if the peripheral module clock (PCLK) stops. The bus interface and registers operate with PCLK, and the 14-bit counter and control circuits operate with IWDTCLK.

Figure 25.1 is a block diagram of the IWDT.

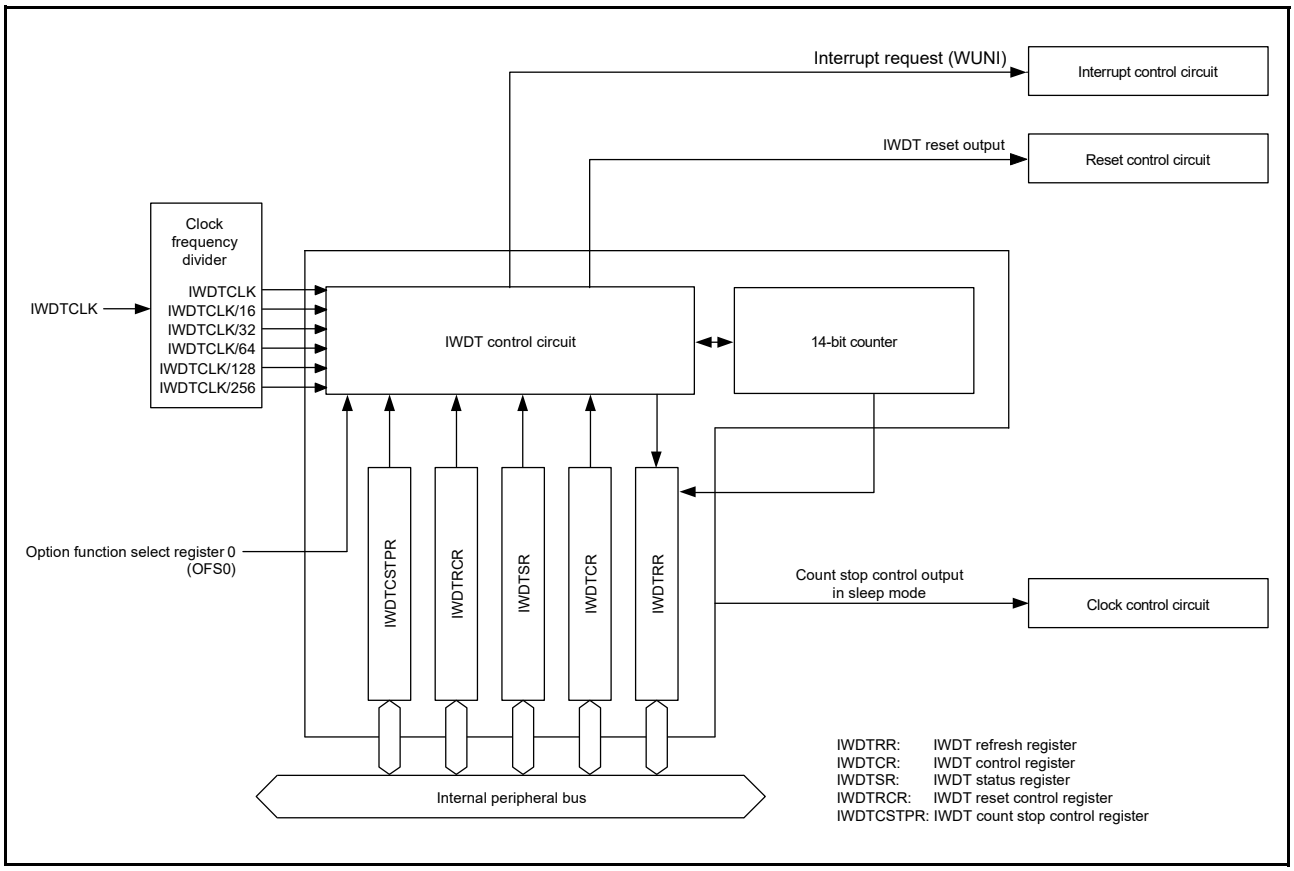
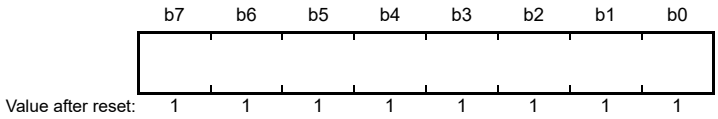


Figure 25.1 IWDT Block Diagram

25.2 Register Descriptions

25.2.1 IWDT Refresh Register (IWDTRR)

Address(es): IWDT.IWDTRR 0008 8030h



Bit	Description	R/W
b7 to b0	The counter is refreshed by writing 00h and then writing FFh to this register.	R/W

The IWDTRR register refreshes the counter of the IWDT.
The counter of the IWDT is refreshed by writing 00h and then writing FFh to the IWDTRR register (refresh operation) within the refresh-permitted period.
After the counter has been refreshed, it starts counting down from the value selected by the IWDT timeout period select bits (OFS0.IWDTTOPS[1:0]) in option function select register 0 (OFS0) in auto-start mode. In register start mode, counting down starts from the value selected by setting the timeout period select bits (TOPS[1:0]) in the IWDT control register (IWDTCR) in the first refresh operation after release from the reset state.
When 00h is written, the read value is 00h. When a value other than 00h is written, the read value is FFh.
For details of the refresh operation, refer to section 25.3.3, Refresh Operation.

25.2.2 IWDT Control Register (IWDTCR)

Address(es): IWDT.IWDTCR 0008 8032h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	RPSS[1:0]		—	—	RPES[1:0]		CKS[3:0]				—	—	TOPS[1:0]	
Value after reset:	0	0	1	1	0	0	1	1	1	1	1	1	0	0	1	1

Bit	Symbol	Bit Name	Description	R/W
b1, b0	TOPS[1:0]	Timeout Period Select	b1 b0 0 0: 128 cycles (007Fh) 0 1: 512 cycles (01FFh) 1 0: 1024 cycles (03FFh) 1 1: 2048 cycles (07FFh)	R/W
b3, b2	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R
b7 to b4	CKS[3:0]	Clock Divide Ratio Select	b7 b4 0 0 0 0: No division 0 0 1 0: Divide-by-16 0 0 1 1: Divide-by-32 0 1 0 0: Divide-by-64 1 1 1 1: Divide-by-128 0 1 0 1: Divide-by-256 Other settings are prohibited.	R/W
b9, b8	RPES[1:0]	Window End Position Select	b9 b8 0 0: 75% 0 1: 50% 1 0: 25% 1 1: 0% (window end position is not specified.)	R/W
b11, b10	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R
b13, b12	RPSS[1:0]	Window Start Position Select	b13 b12 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100% (window start position is not specified.)	R/W
b15, b14	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R

There are some restrictions on writing to the IWDTCR register. For details, refer to section 25.3.2, Control over Writing to the IWDTCR, IWDTRCR, and IWDTCSTPR Registers.

In auto-start mode, the settings in the IWDTCR register are disabled, and the settings in option function select register 0 (OFS0) are enabled. The bit setting made to the IWDTCR register can also be made in option function select register 0 (OFS0). For details, refer to section 25.3.8, Correspondence between Option Function Select Register 0 (OFS0) and IWDT Registers.

TOPS[1:0] Bits (Timeout Period Select)

These bits select the timeout period (period until the counter underflows) from among 128, 512, 1024, or 2048 cycles, taking the divided clock specified by the CKS[3:0] bits as one cycle.
After the counter is refreshed, the combination of the CKS[3:0] and TOPS[1:0] bits determines the time (number of IWDTCLK cycles) until the counter underflows.
Relations between the CKS[3:0] and TOPS[1:0] bit setting, the timeout period, and the number of IWDTCLK cycles are listed in Table 25.2.

Table 25.2 Settings and Timeout Periods

CKS[3:0] Bits				TOPS[1:0] Bits				
b7	b6	b5	b4	b1	b0	Clock Divide Ratio	Timeout Period (Number of Cycles)	Cycles of IWDTCLK
0	0	0	0	0	0	No division	128	128
				0	1		512	512
				1	0		1024	1024
				1	1		2048	2048
0	0	1	0	0	0	Divide-by-16	128	2048
				0	1		512	8192
				1	0		1024	16384
				1	1		2048	32768
0	0	1	1	0	0	Divide-by-32	128	4096
				0	1		512	16384
				1	0		1024	32768
				1	1		2048	65536
0	1	0	0	0	0	Divide-by-64	128	8192
				0	1		512	32768
				1	0		1024	65536
				1	1		2048	131072
1	1	1	1	0	0	Divide-by-128	128	16384
				0	1		512	65536
				1	0		1024	131072
				1	1		2048	262144
0	1	0	1	0	0	Divide-by-256	128	32768
				0	1		512	131072
				1	0		1024	262144
				1	1		2048	524288

CKS[3:0] Bits (Clock Divide Ratio Select)

These bits select the IWDTCLK clock divide ratio from among divide-by 1, 16, 32, 64, 128, and 256. Combination with the TOPS[1:0] bit setting, a count period between 128 and 524288 cycles of the IWDTCLK clock can be selected for the IWDT.

RPES[1:0] Bits (Window End Position Select)

These bits select 75%, 50%, 25% or 0% of the count period for the window end position of the counter. The window end position should be a value smaller than the window start position (window start position > window end position). If the window end position is greater than the window start position, only the window start position setting is enabled.
The counter values for the window start and end positions selected by setting the RPSS[1:0] and RPES[1:0] bits change depending on the TOPS[1:0] bit setting.
Table 25.3 lists the counter values for the window start and end positions corresponding to TOPS[1:0] bit values.

Table 25.3 Relationship between Timeout Period and Window Start and End Counter Values

TOPS[1:0] Bits		Timeout Period		Window Start and End Counter Value			
b1	b0	Cycles	Counter Value	100%	75%	50%	25%
0	0	128	007Fh	007Fh	005Fh	003Fh	001Fh
0	1	512	01FFh	01FFh	017Fh	00FFh	007Fh
1	0	1024	03FFh	03FFh	02FFh	01FFh	00FFh
1	1	2048	07FFh	07FFh	05FFh	03FFh	01FFh

RPSS[1:0] Bits (Window Start Position Select)

These bits select a counter window start position from 100%, 75%, 50%, or 25% of the count period (100% when the count starts and 0% when the counter underflows). The interval between the window start position and window end position is the refresh-permitted period and the other periods are refresh-prohibited periods.
Figure 25.2 shows the relationship between of the RPSS[1:0] and RPES[1:0] bit setting and the refresh-permitted and refresh-prohibited periods.

RPSS[1:0] Bits		RPES[1:0] Bits		Window	
b13	b12	b9	b8	Start (%)	End (%)
1	1	1	1	100	0
		1	0		25
		0	1		50
		0	0		75
1	0	1	1	75	0
		1	0		25
		0	1		50
		0	0		75
0	1	1	1	50	0
		1	0		25
		0	1		50
		0	0		75
0	0	1	1	25	0
		1	0		25
		0	1		50
		0	0		75

Note: If window end setting is greater than or equal to window start setting, the window end setting is set to 0%.

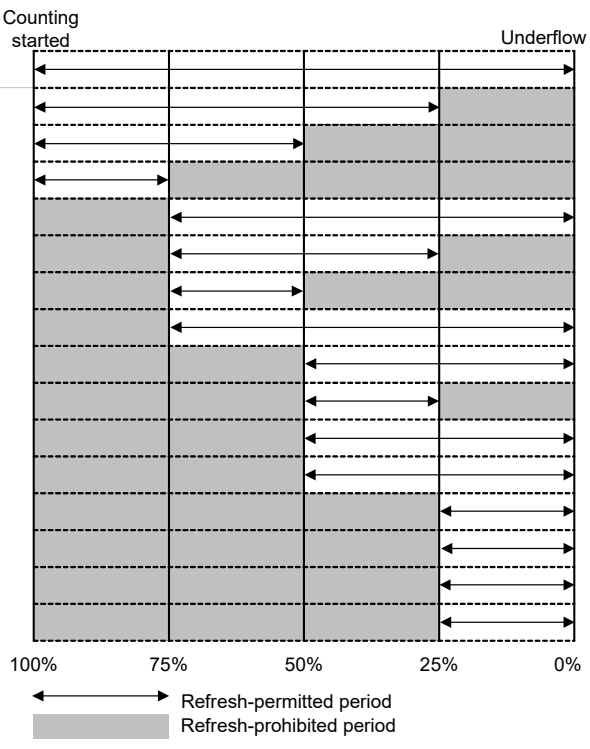


Figure 25.2 RPSS[1:0] and RPES[1:0] Bit Settings and the Refresh-Permitted Period

25.2.3 IWDT Status Register (IWDTSR)

Address(es): IWDT.IWDTSR 0008 8034h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	REFEF	UNDFF	CNTVAL[13:0]													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b13 to b0	CNTVAL[13:0]	Counter Value	Value counted by the counter	R
b14	UNDFF	Underflow Flag	0: No underflow occurred 1: Underflow occurred	R/(W) *1
b15	REFEF	Refresh Error Flag	0: No refresh error occurred 1: Refresh error occurred	R/(W) *1

Note 1. Only 0 can be written to clear the flag.

The IWDTSR register is initialized by the reset source of the IWDT. The IWDTSR register is not initialized by other reset sources.

CNTVAL[13:0] Bits (Counter Value)

These bits are used to confirm the counter value of the counter, but note that the read value may differ from the actual count by a value of one count.

UNDFF Flag (Underflow Flag)

This bit is used to confirm whether or not an underflow has occurred in the counter.
The value 1 indicates that the counter has underflowed. The value 0 indicates that the counter has not underflowed.
Write 0 to the UNDFF flag to set the value to 0. Writing 1 has no effect.

REFEF Flag (Refresh Error Flag)

This bit is used to confirm whether or not a refresh error (performing a refresh operation during a refresh-prohibited period).
The value 1 indicates that a refresh error has occurred. The value 0 indicates that no refresh error has occurred.
Write 0 to the REFEF flag to set the value to 0. Writing 1 has no effect.

25.2.4 IWDT Reset Control Register (IWDTRCR)

Address(es): IWDT.IWDTRCR 0008 8036h

	b7	b6	b5	b4	b3	b2	b1	b0
	RSTIRQS	—	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R
b7	RSTIRQS	Reset Interrupt Request Select	0: Non-maskable interrupt request output is enabled. 1: Reset output is enabled.	R/W

There are some restrictions on writing to the IWDTRCR register. For details, refer to section 25.3.2, Control over Writing to the IWDTCR, IWDTRCR, and IWDTCSTPR Registers.

In auto-start mode, the IWDTRCR register setting are disabled, and the settings in option function select register 0 (OFS0) are enabled. The bit setting mode to the IWDTRCR register can also be made in option function select register 0. For details, refer to section 25.3.8, Correspondence between Option Function Select Register 0 (OFS0) and IWDT Registers.

25.2.5 IWDT Count Stop Control Register (IWDTCSTPR)

Address(es): IWDT.IWDTCSTPR 0008 8038h

	b7	b6	b5	b4	b3	b2	b1	b0
	SLCSTP	—	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R
b7	SLCSTP	Sleep Mode Count Stop Control	0: Count stop is disabled. 1: Count is stopped at a transition to sleep mode, software standby mode, or deep sleep mode.	R/W

The IWDTCSTPR register controls whether to stop the IWDT counter in a low power consumption state. There are some restrictions on writing to the IWDTCSTPR register. For details, refer to section 25.3.2, Control over Writing to the IWDTCR, IWDTRCR, and IWDTCSTPR Registers.
In auto-start mode, the IWDTCSTPR register setting are disabled, and the settings in option function select register 0 (OFS0) are enabled. The bit setting mode to the IWDTCSTPR register can also be made in option function select register 0 (OFS0). For details, refer to section 25.3.8, Correspondence between Option Function Select Register 0 (OFS0) and IWDT Registers.

SLCSTP Bit (Sleep Mode Count Stop Control)

This bit selects whether to stop counting at a transition to sleep mode, software standby mode, or deep sleep mode.

25.2.6 Option Function Select Register 0 (OFS0)

For option function select register 0 (OFS0), refer to section 25.3.8, Correspondence between Option Function Select Register 0 (OFS0) and IWDT Registers.

25.3 Operation

25.3.1 Count Operation in Each Start Mode

Select the IWDT start mode by setting the IWDT start mode select bit (OFS0.IWDTSTRT) in option function select register 0.
When the OFS0.IWDTSTRT bit is 1 (register start mode), the IWDT control register (IWDTCR), IWDT reset control register (IWDTRCR), and IWDT count stop control register (IWDTCSTPR) are enabled, and counting is started by refreshing (writing) the IWDT refresh register (IWDTRR). When the OFS0.IWDTSTRT bit is 0 (auto-start mode), the setting of option function select register 0 (OFS0) is enabled, and counting automatically starts after reset.

25.3.1.1 Register Start Mode

When the IWDT start mode select bit (OFS0.IWDTSTRT) in option function select register 0 is 1, register start mode is selected, and the IWDT control register (IWDTCR), IWDT reset control register (IWDTRCR), and IWDT count stop control register (IWDTCSTPR) are enabled.
After the reset state is released, set the clock divide ratio, window start and end positions, and timeout period in the IWDTCR register, the reset output or interrupt request output in the IWDTRCR register, and the counter stop control at transitions to low power consumption states in the IWDTCSTPR register. Then refresh the counter to start counting down from the value selected by setting the timeout period select bits (IWDTCR.TOPS[1:0]).
Thereafter, as long as the program continues normal operation and the counter is refreshed in the refresh-permitted period, the value in the counter is re-set each time the counter is refreshed and counting down continues. The IWDT does not output the reset signal as long as this continues. However, if the counter underflows because the counter cannot be refreshed due to a program runaway, or if a refresh error occurs because the counter was refreshed outside the refresh-permitted period, the IWDT outputs a reset signal or a non-maskable interrupt request (WUNI). Set the IWDT reset interrupt request select bit (IWDTRCR.RSTIRQS) to select either reset output or interrupt request output.

Figure 25.3 shows an example of operation under the following conditions.

- The IWDT start mode select bit (OFS0.IWDTSTRT) is 1 (register start mode)
- The IWDT reset interrupt request select bit (IWDTRCR.RSTIRQS) is 1 (reset output is enabled)
- The IWDT window start position select bits (IWDTCR.RPSS[1:0]) are 10b (75%)
- The IWDT window end position select bits (IWDTCR.RPES[1:0]) are 10b (25%)

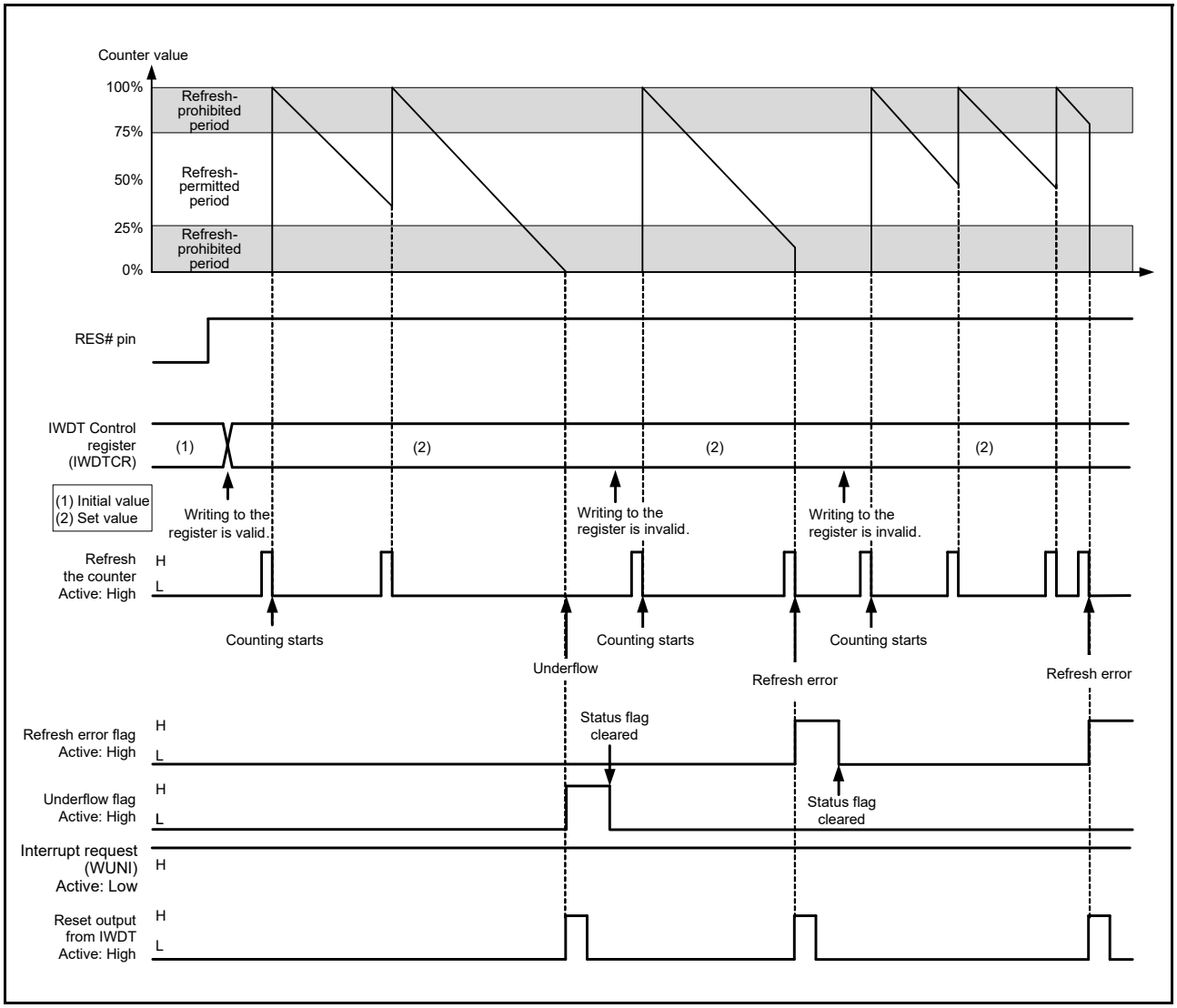


Figure 25.3 Operation Example in Register Start Mode

25.3.1.2 Auto-Start Mode

When the IWDT start mode select bit (OFS0.IWDTSTRT) in option function select register 0 is 0, auto-start mode is selected, and the IWDT control register (IWDTCR), IWDT reset control register (IWDTRCR), and IWDT count stop control register (IWDTCSTPR) are disabled.
Within the reset state, the clock divide ratio, window start and end positions, timeout period, reset output or interrupt request output, and counter stop control at transitions to low power consumption states are set using the values specified in option function select register 0 (OFS0). When the reset state is released, the counter automatically starts counting down from the value selected by the IWDT timeout period select bits (OFS0.IWDTTOPS[1:0]).
After that, as long as the program continues normal operation and the counter is refreshed in the refresh-permitted period, the value in the counter is re-set each time the counter is refreshed and counting down continues. The IWDT does not output the reset signal as long as this continues. However, if the counter underflows because refreshing of the counter is not possible due to the program having entered crashed execution or if a refresh error occurs due to refreshing outside the refresh-permitted period, the IWDT outputs the reset signal or non-maskable interrupt request (WUNI). After the reset signal or non-maskable interrupt request (WUNI) is generated, the counter reloads the timeout period after counting for one cycle, and restarts counting. Set the IWDT reset interrupt request select bit (OFS0.IWDTRSTIRQS) to select either reset output or interrupt request output.

Figure 25.4 shows an example of operation under the following conditions.

- The IWDT start mode select bit (OFS0.IWDTSTRT) is 0 (auto-start mode)
- The IWDT reset interrupt request select bit (OFS0.IWDTRSTIRQS) is 0 (non-maskable interrupt request output is enabled)
- The IWDT window start position select bits (OFS0.IWDTRPSS[1:0]) are 10b (75%)
- The IWDT window end position select bits (OFS0.IWDTRPES[1:0]) are 10b (25%)

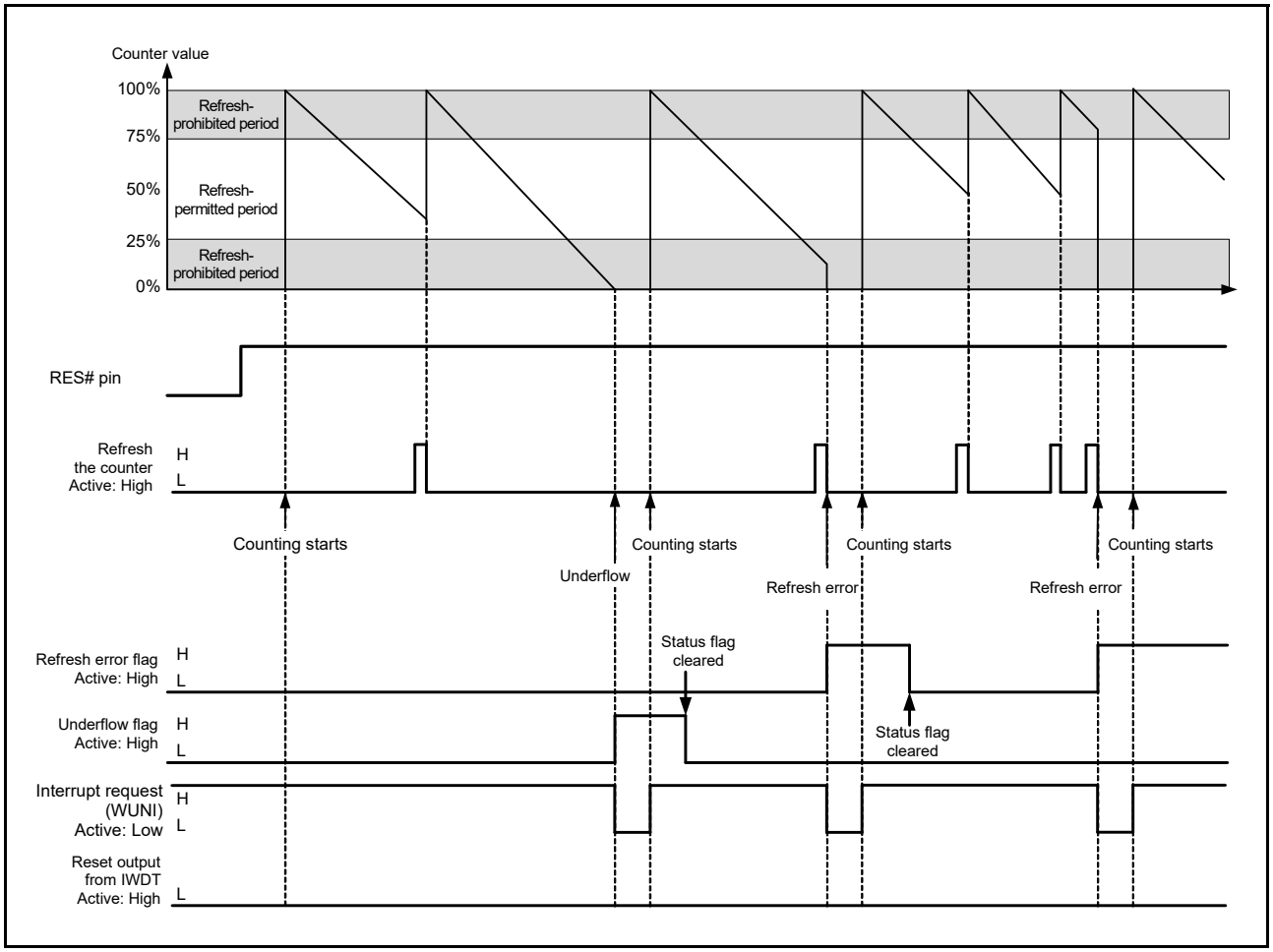


Figure 25.4 Operation Example in Auto-Start Mode

25.3.2 Control over Writing to the IWDTCR, IWDTRCR, and IWDTCSTPR Registers

Writing to the IWDT control register (IWDTCR), IWDT reset control register (IWDTRCR), or IWDT count stop control register (IWDTCSTPR) is only possible once between the release from the reset state and the first refresh operation. After a refresh operation (counting starts) or the IWDTCR, IWDTRCR, or IWDTCSTPR register is written to, the protection signal in the IWDT becomes 1 to protect registers IWDTCR, IWDTRCR, and IWDTCSTPR against subsequent attempts at writing.

This protection is released by the reset source of the IWDT. With other reset sources, the protection is not released.

Figure 25.5 shows control waveforms produced in response to writing to the IWDTCR register.

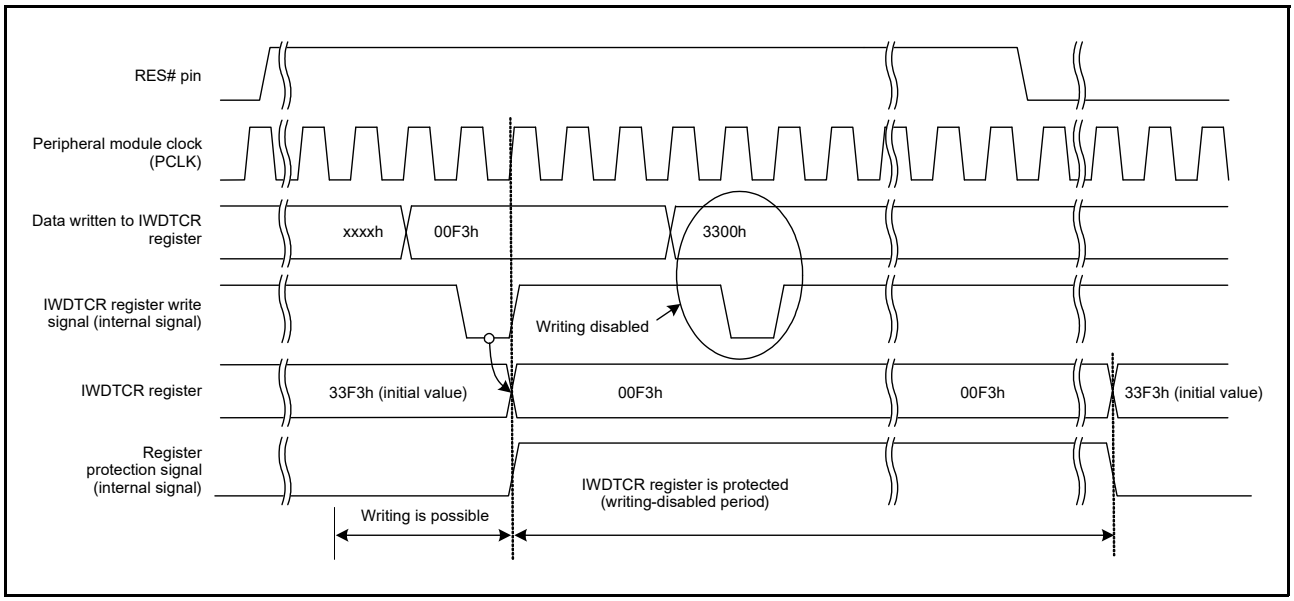


Figure 25.5 Control Waveforms Produced in Response to Writing to the IWDTCR Register

25.3.3 Refresh Operation

The counter is refreshed and starts operation (counting is started by refreshing) by writing the values 00h and then FFh to the IWDT refresh register (IWDTRR). If a value other than FFh is written after 00h, the counter is not refreshed. After such invalid writing, correct refreshing is performed by again writing 00h and then FFh to the IWDT refresh register (IWDTRR).
When writing is done in the order of 00h (first time) → 00h (second time), and if FFh is written after that, the writing order 00h → FFh is satisfied; writing 00h (n–1-th time) → 00h (nth time) → FFh is valid and correct refreshing will be done. Even when the first value written before 00h is not 00h, correct refreshing will be done if the operation contains the set of writing 00h → FFh. Moreover, even if a register other than the IWDTRR register is accessed or the IWDTRR register is read between writing 00h and writing FFh to the IWDTRR register, correct refreshing will be done.

[Sample sequences of writing that are valid for refreshing the counter]

- 00h → FFh
- 00h (n–1-th time) → 00h (nth time) → FFh
- 00h → access to another register or read from the IWDTRR register → FFh

[Sample sequences of writing that are not valid for refreshing the counter]

- 23h (a value other than 00h) → FFh
- 00h → 54h (a value other than FFh)
- 00h → AAh (00h and a value other than FFh) → FFh

Even when 00h is written to the IWDTRR register outside the refresh-permitted period, if FFh is written to the IWDTRR register in the refresh-permitted period, the writing sequence is valid and refreshing will be done.
After FFh is written to the IWDTRR register, refreshing the counter requires up to four cycles of the signal for counting (the clock divide ratio selection bits (IWDTCR.CKS[3:0]) determine how many cycles of the IWDT-dedicated clock (IWDTCLK) make up one cycle for counting). Therefore, writing FFh to the IWDTRR register should be completed four-count cycles before the end position of the refresh-permitted period or a counter underflow. The value of the counter can be checked by the counter bits (IWDTSR.CNTVAL[13:0]).

[Sample refreshing timings]

- When the window start position is set to 03FFh, even if 00h is written to the IWDTRR register before 03FFh is reached (0402h, for example), refreshing is done if FFh is written to the IWDTRR register after the value of the IWDTSR.CNTVAL[13:0] bits has reached 03FFh.
- When the window end position is set to 03FFh, refreshing is done if 0403h (four-count cycles before 03FFh) or a greater value is read from the IWDTSR.CNTVAL[13:0] bits immediately after writing 00h → FFh to the IWDTRR register.
- When the refresh-permitted period continues until count 0000h, refreshing can be done immediately before an underflow. In this case, if 0003h (four-count cycles before an underflow) or a greater value is read from the IWDTSR.CNTVAL[13:0] bits immediately after writing 00h → FFh to the IWDTRR register, no underflow occurs and refreshing is done.

Figure 25.6 shows the IWDT refresh-operation waveforms when PCLK > IWDTCLK and clock divide ratio = IWDTCLK.

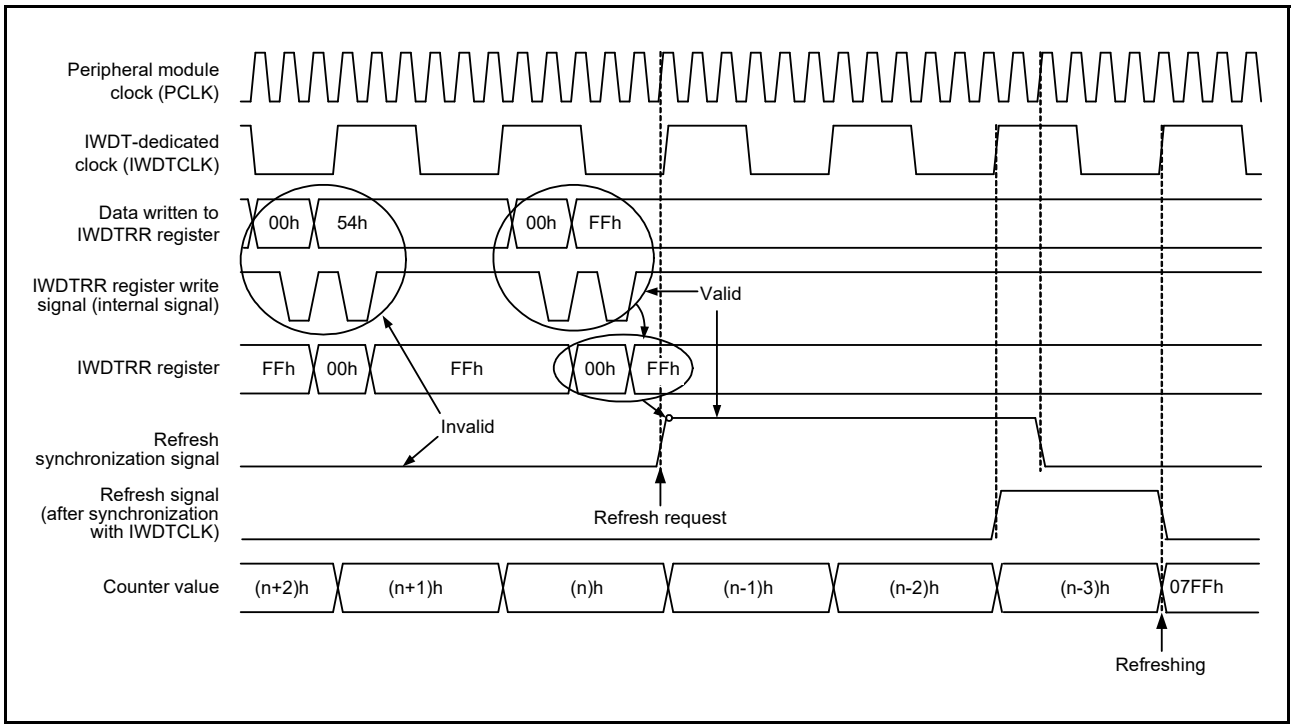


Figure 25.6 IWDT Refresh Operation Waveforms (IWDTCR.CKS[3:0] = 0000b, IWDTCR.TOPS[1:0] = 11b)

25.3.4 Status Flags

The refresh error (IWDTSR.REFEF) and underflow (IWDTSR.UNDFF) flags retain the source of the reset signal output from the IWDT or the source of the interrupt request from the IWDT.
Thus, after release from the reset state or interrupt request generation, read the IWDTSR.REFEF and IWDTSR.UNDFF flags to check for the reset or interrupt source.
For each flag, writing 0 clears the bit and writing 1 has no effect.
Leaving the status flags unchanged does not affect operation. If the flags are not cleared, at the time of the next reset or interrupt request from the IWDT, the earlier reset or interrupt source is cleared and the new reset or interrupt source is written.
After 0 is written to each flag, up to three IWDTCLK cycles and two PCLK cycles are required before the value is reflected.

25.3.5 Reset Output

When the reset interrupt selection bit (IWDTRCR.RSTIRQS) is set to 1 in register start mode or when the IWDT reset interrupt request select bit (OFS0.IWDTRSTIRQS) in option function select register 0 (OFS0) is set to 1 in auto-start mode, a reset signal is output when an underflow in the counter or a refresh error occurs.
In register start mode, the counter is initialized (all bits set to 0) and kept in that state after assertion of the reset signal. After the reset is released and the program is restarted, the counter is set up again and counting down is started by refreshing.
In auto-start mode, counting down automatically starts after the reset output.

25.3.6 Interrupt Sources

When the reset interrupt selection bit (IWDTRCR.RSTIRQS) is set to 0 in register start mode or when the IWDT reset interrupt request select bit (OFS0.IWDTRSTIRQS) in option function select register 0 (OFS0) is set to 0 in auto-start mode, an interrupt (WUNI) signal is output when an underflow in the counter or a refresh error occurs. This interrupt can be used as a non-maskable interrupt. For details, refer to section 14, Interrupt Controller (ICUb).

Table 25.4 IWDT Interrupt Source

Name	Interrupt Source	DTC Activation
WUNI	Counter underflow Refresh error	Not possible

25.3.7 Reading the Counter Value

As the counter in IWDT-dedicated clock (IWDTCLK), the counter value cannot be read directly. The IWDT synchronizes the counter value with the peripheral module clock (PCLK) and stores it in the counter value bits (IWDTSR.CNTVAL[13:0]) of the IWDT status register. Thus, the counter value can be checked indirectly through the IWDTSR.CNTVAL[13:0] bits.

Reading the counter value requires multiple PCLK clock cycles (up to four clock cycles), and the read counter value may differ from the actual counter value by a value of one count.

Figure 25.7 shows the processing for reading the IWDT counter value when PCLK > IWDTCLK and clock divide ratio = IWDTCLK.

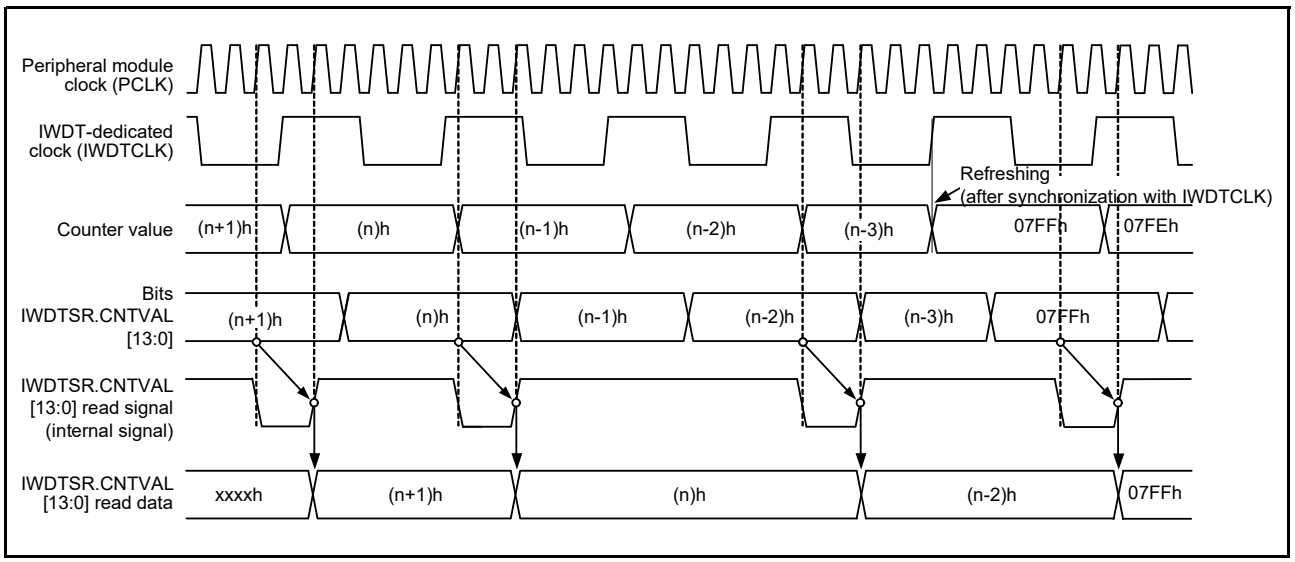


Figure 25.7 Processing for Reading IWDT Counter Value (IWDTCR.CKS[3:0] = 0000b, IWDTCR.TOPS[1:0] = 11b)

25.3.8 Correspondence between Option Function Select Register 0 (OFS0) and IWDT Registers

Table 25.5 lists the correspondence between option function select register 0 (OFS0) used in auto-start mode and the registers used in register start mode.
Do not change the OFS0 register setting during IWDT operation.
For details on option function select register 0 (OFS0), refer to section 7.2.1, Option Function Select Register 0 (OFS0).

Table 25.5 Correspondence between Option Function Select Register 0 (OFS0) and IWDT Registers

Target of Control	Function	OFS0 Register (Enabled in Auto-Start Mode) OFS0.IWDTSTRT = 0	IWDT Registers (Enabled in Register Start Mode) OFS0.IWDTSTRT = 1
Counter	Timeout period selection	OFS0.IWDTTOPS[1:0]	IWDTCR.TOPS[1:0]
	Clock frequency divide ratio selection	OFS0.IWDTCKS[3:0]	IWDTCR.CKS[3:0]
	Window start position selection	OFS0.IWDTRPSS[1:0]	IWDTCR.RPSS[1:0]
	Window end position selection	OFS0.IWDTRPES[1:0]	IWDTCR.RPES[1:0]
Reset output or interrupt request output	Reset output or interrupt request output selection	OFS0.IWDTRSTIRQS	IWDTRCR.RSTIRQS
Count stop	Sleep mode count stop control	OFS0.IWDTSLCSTP	IWDTCSTPR.SLCSTP

25.4 Usage Notes

25.4.1 Refresh Operations

When making the settings to control the timing of refreshing, consider variations in the range of errors due to the accuracy of the PCLK and IWDTCLK and set values which ensure that refreshing is possible.

25.4.2 Clock Divide Ratio Setting

Satisfy the frequency of the peripheral module clock (PCLK) ≥ 4 × (the frequency of the count source after divide).

26. Serial Communications Interface (SCIg)

This MCU has six independent serial communications interface (SCI) channels. The SCI consists of the SCIg module (SCI1, SCI5, SCI6, SCI8, SCI9, and SCI11).

The SCIg module (SCI1, SCI5, SCI6, SCI8, SCI9, and SCI11) can handle both asynchronous and clock synchronous serial communications.

Asynchronous serial data communications can be carried out with standard asynchronous communications chips such as a Universal Asynchronous Receiver/Transmitter (UART) or Asynchronous Communications Interface Adapter (ACIA). As an extended function in asynchronous communications mode, the SCI also supports smart card (IC card) interfaces conforming to ISO/IEC 7816-3 (standard for Identification Cards). The SCI is also supports simple SPI interfaces, and simple I^2C-bus interfaces when configured for single-master systems.

In this section, “PCLK” for SCI1, SCI5, SCI6, SCI8, and SCI9 is used to refer to PCLKB and “PCLK” for SCI11 is used to refer to PCLKA.

26.1 Overview

Table 26.1 lists the specifications of the SCIg module and Table 26.2 lists the specifications of the individual SCI channels.

Figure 26.1 and Figure 26.2 show the block diagrams of the SCIg module.

Table 26.1 SCIg Specifications (1/2)

Item		Description
Serial communication modes		• Asynchronous • Clock synchronous • Smart card interface • Simple I^2C-bus • Simple SPI bus
Transfer speed		Bit rate specifiable with the on-chip baud rate generator.
Full-duplex communications		Transmitter: Continuous transmission possible using double-buffer structure. Receiver: Continuous reception possible using double-buffer structure.
I/O pins		Refer to Table 26.3 to Table 26.5.
Data transfer		Selectable as LSB first or MSB first transfer*1
Interrupt sources		Transmit end, transmit data empty, receive data full, and receive error Completion of generation of a start condition, restart condition, or stop condition (for simple I^2C mode)
Low power consumption function		Module stop state can be set for each channel.
Asynchronous mode	Data length	7, 8, or 9 bits
	Transmission stop bit	1 or 2 bits
	Parity	Even parity, odd parity, or no parity
	Receive error detection	Parity, overrun, and framing errors
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/reception.
	Start-bit detection	Low level or falling edge is selectable.
	Break detection	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.
	Clock source	An internal or external clock can be selected. Transfer rate clock input from the TMR can be used. (SCI5, SCI6)
	Double-speed mode	Baud rate generator double-speed mode is selectable.
	Multi-processor communications function	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate digital noise filters.

Table 26.1 SCIg Specifications (2/2)

Item		Description
Clock synchronous mode	Data length	8 bits
	Receive error detection	Overrun error
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/reception.
Smart card interface mode	Error processing	An error signal can be automatically transmitted when detecting a parity error during reception
		Data can be automatically retransmitted when receiving an error signal during transmission
	Data type	Both direct convention and inverse convention are supported.
Simple I^2C mode	Transfer format	I^2C-bus format
	Operating mode	Master (single-master operation only)
	Transfer rate	Fast mode is supported (refer to section 26.2.11, Bit Rate Register (BRR) to set the transfer rate).
	Noise cancellation	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable.
Simple SPI bus	Data length	8 bits
	Detection of errors	Overrun error
	SS input pin function	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.
	Clock settings	Four kinds of settings for clock phase and clock polarity are selectable.
Bit rate modulation function		Correction of outputs from the on-chip baud rate generator can reduce errors.

Note 1. In simple I^2C mode, only MSB first is available.

Table 26.2 Functions of SCI Channels

Item	SCI1, SCI8, SCI9	SCI5, SCI6	SCI11
Asynchronous mode	Available	Available	Available
Clock synchronous mode	Available	Available	Available
Smart card interface mode	Available	Available	Available
Simple I^2C mode	Available	Available	Available
Simple SPI mode	Available	Available	Available
TMR clock input	Not available	Available	Not available
Peripheral module clock	PCLKB	PCLKB	PCLKA

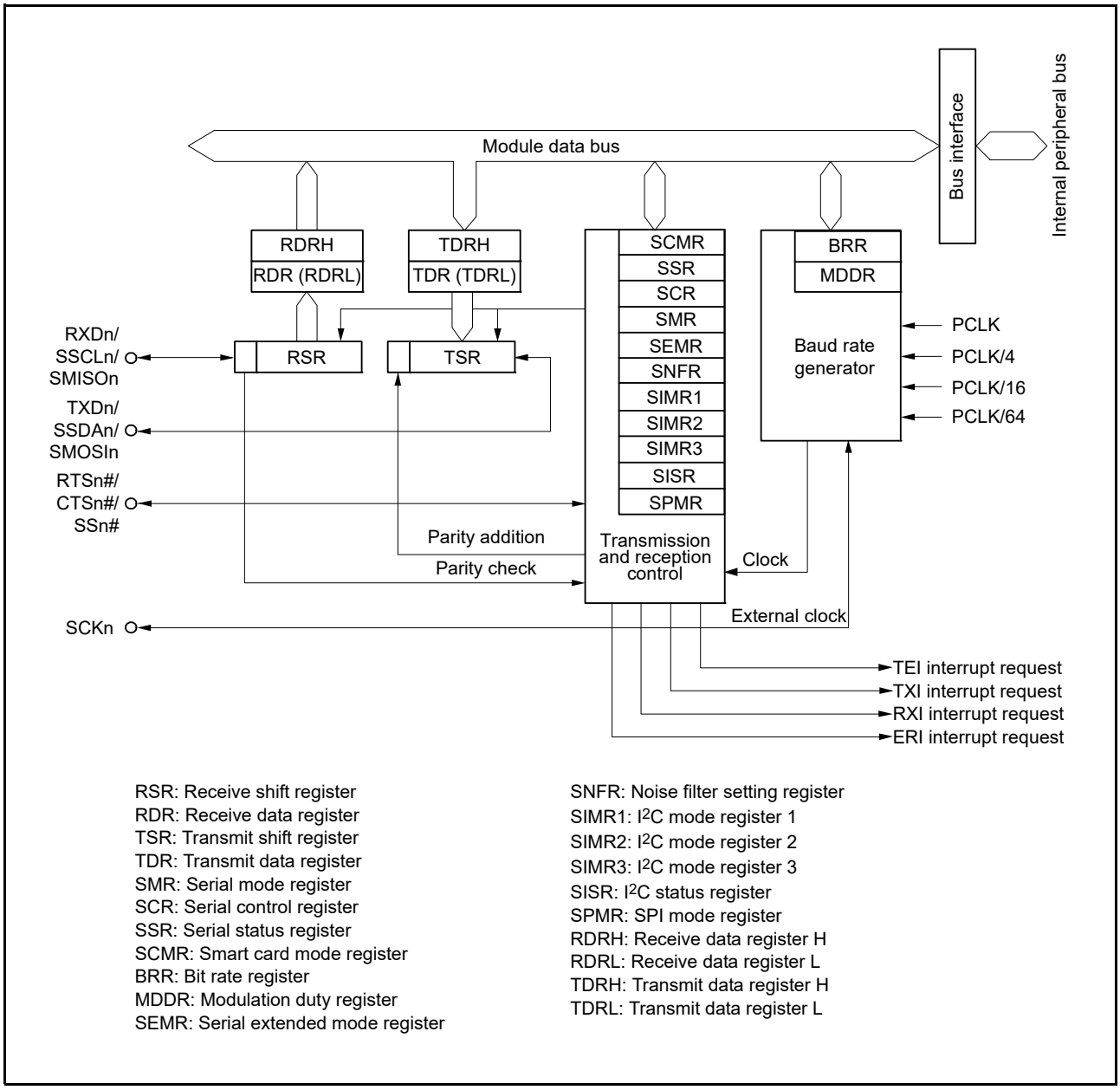


Figure 26.1 Block Diagram of SCIg (SCI1, SCI8 SCI9, and SCI11)

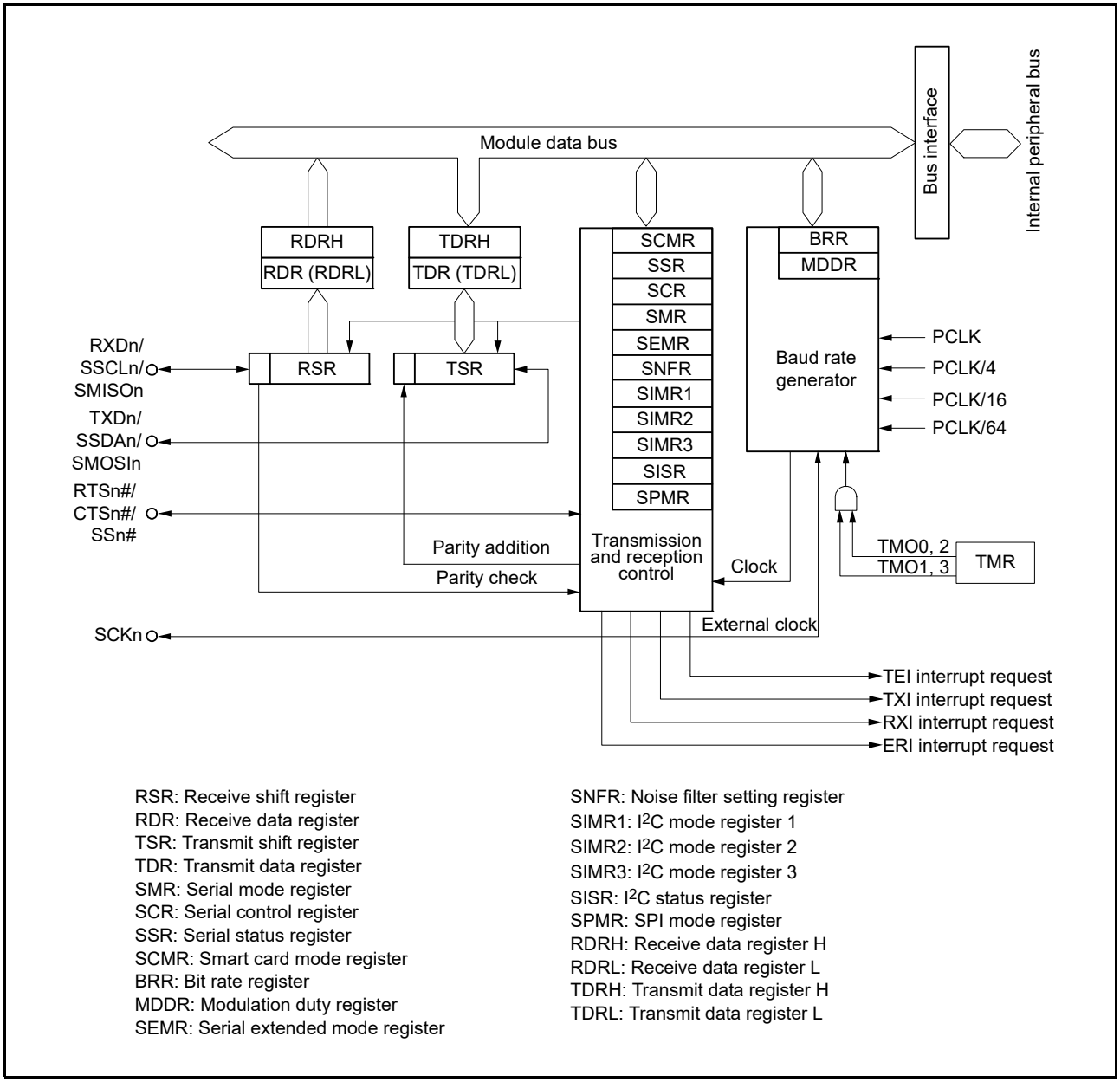


Figure 26.2 Block Diagram of SCIg (SCI5 and SCI6)

Table 26.3 to Table 26.5 list the pin configuration of the SCIs for the individual modes.

Table 26.3 SCI Pin Configuration in Asynchronous Mode and Clock Synchronous Mode

Channel	Pin Name	I/O	Function
SCI1	SCK1	I/O	SCI1 clock input/output
	RXD1	Input	SCI1 receive data input
	TXD1	Output	SCI1 transmit data output
	CTS1#/RTS1#	I/O	SCI1 transfer start control input/output
SCI5	SCK5	I/O	SCI5 clock input/output
	RXD5	Input	SCI5 receive data input
	TXD5	Output	SCI5 transmit data output
	CTS5#/RTS5#	I/O	SCI5 transfer start control input/output
SCI6	SCK6	I/O	SCI6 clock input/output
	RXD6	Input	SCI6 receive data input
	TXD6	Output	SCI6 transmit data output
	CTS6#/RTS6#	I/O	SCI6 transfer start control input/output
SCI8	SCK8	I/O	SCI8 clock input/output
	RXD8	Input	SCI8 receive data input
	TXD8	Output	SCI8 transmit data output
	CTS8#/RTS8#	I/O	SCI8 transfer start control input/output
SCI9	SCK9	I/O	SCI9 clock input/output
	RXD9	Input	SCI9 receive data input
	TXD9	Output	SCI9 transmit data output
	CTS9#/RTS9#	I/O	SCI9 transfer start control input/output
SCI11	SCK11	I/O	SCI11 clock input/output
	RXD11	Input	SCI11 receive data input
	TXD11	Output	SCI11 transmit data output
	CTS11#/RTS11#	I/O	SCI11 transfer start control input/output

Table 26.4 SCI Pin Configuration in Simple I^2C Mode

Channel	Pin Name	I/O	Function
SCI1	SSCL1	I/O	SCI1 I^2C clock input/output
	SSDA1	I/O	SCI1 I^2C data input/output
SCI5	SSCL5	I/O	SCI5 I^2C clock input/output
	SSDA5	I/O	SCI5 I^2C data input/output
SCI6	SSCL6	I/O	SCI6 I^2C clock input/output
	SSDA6	I/O	SCI6 I^2C data input/output
SCI8	SSCL8	I/O	SCI8 I^2C clock input/output
	SSDA8	I/O	SCI8 I^2C data input/output
SCI9	SSCL9	I/O	SCI9 I^2C clock input/output
	SSDA9	I/O	SCI9 I^2C data input/output
SCI11	SSCL11	I/O	SCI11 I^2C clock input/output
	SSDA11	I/O	SCI11 I^2C data input/output

Table 26.5 SCI Pin Configuration in Simple SPI Mode

Channel	Pin Name	I/O	Function
SCI1	SCK1	I/O	SCI1 clock input/output
	SMISO1	I/O	SCI1 slave transmit data input/output
	SMOSI1	I/O	SCI1 master transmit data input/output
	SS1#	Input	SCI1 chip select input
SCI5	SCK5	I/O	SCI5 clock input/output
	SMISO5	I/O	SCI5 slave transmit data input/output
	SMOSI5	I/O	SCI5 master transmit data input/output
	SS5#	Input	SCI5 chip select input
SCI6	SCK6	I/O	SCI6 clock input/output
	SMISO6	I/O	SCI6 slave transmit data input/output
	SMOSI6	I/O	SCI6 master transmit data input/output
	SS6#	Input	SCI6 chip select input
SCI8	SCK8	I/O	SCI8 clock input/output
	SMISO8	I/O	SCI8 slave transmit data input/output
	SMOSI8	I/O	SCI8 master transmit data input/output
	SS8#	Input	SCI8 chip select input
SCI9	SCK9	I/O	SCI9 clock input/output
	SMISO9	I/O	SCI9 slave transmit data input/output
	SMOSI9	I/O	SCI9 master transmit data input/output
	SS9#	Input	SCI9 chip select input
SCI11	SCK11	I/O	SCI11 clock input/output
	SMISO11	I/O	SCI11 slave transmit data input/output
	SMOSI11	I/O	SCI11 master transmit data input/output
	SS11#	Input	SCI11 chip select input

26.2 Register Descriptions

26.2.1 Receive Shift Register (RSR)

RSR is a shift register which is used to receive serial data input from the RXDn pin and converts it into parallel data.
When one frame of data has been received, it is automatically transferred to the RDR register.
The RSR register cannot be directly accessed by the CPU.

26.2.2 Receive Data Register (RDR)

Address(es): SCI1.RDR 0008 A025h, SCI5.RDR 0008 A0A5h, SCI6.RDR 0008 A0C5h, SCI8.RDR 0008 A105h, SCI9.RDR 0008 A125h, SCI11.RDR 000D 0005h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0

RDR is an 8-bit register that stores receive data.
When one frame of serial data has been received, the received serial data is transferred from RSR to RDR. Then the RSR register can receive the next data.
Since RSR and RDR function as a double buffer in this way, continuous receive operations can be performed.
Read RDR only once after a receive data full interrupt (RXI) has occurred. Note that if next one frame of data is received before reading receive data from RDR, an overrun error occurs.
RDR cannot be written to by the CPU.

26.2.3 Receive Data Register H, L, HL (RDRH, RDRL, RDRHL)

- Receive Data Register H (RDRH)

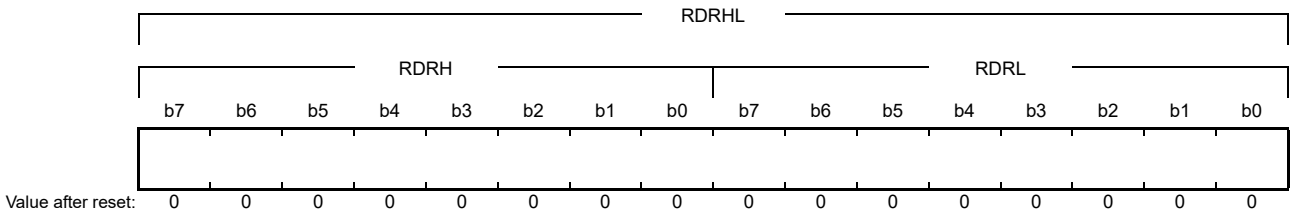
Address(es): SCI1.RDRH 0008 A030h, SCI5.RDRH 0008 A0B0h, SCI6.RDRH 0008 A0D0h, SCI8.RDRH 0008 A110h, SCI9.RDRH 0008 A130h, SCI11.RDRH 000D 0010h

- Receive Data Register L (RDRL)

Address(es): SCI1.RDRL 0008 A031h, SCI5.RDRL 0008 A0B1h, SCI6.RDRL 0008 A0D1h, SCI8.RDRL 0008 A111h, SCI9.RDRL 0008 A131h, SCI11.RDRL 000D 0011h

- Receive Data Register HL (RDRHL)

Address(es): SCI1.RDRHL 0008 A030h, SCI5.RDRHL 0008 A0B0h, SCI6.RDRHL 0008 A0D0h, SCI8.RDRHL 0008 A110h, SCI9.RDRHL 0008 A130h, SCI11.RDRHL 000D 0010h



RDRH and RDRL are 8-bit registers that store receive data. Use these registers when asynchronous mode and 9-bit data length are selected.

RDRL is the shadow register of RDR; i.e. access to RDRL is equivalent to access to RDR.

After one frame of data is received, the received data is transferred from the RSR register to these registers, thus allowing the RSR register to receive the next data.

The RSR, RDRH and RDRL registers have a double-buffered construction to enable continuous reception.

Read RDRH and RDRL should be performed only once in the order from RDRH to RDRL when a receive data full interrupt (RXI) request is issued. Note that an overrun error occurs when the next frame of data is received before the received data has been read from RDRL.

The CPU cannot write to the RDRH and RDRL registers. Bits 0 to 7 in RDRH are fixed to 0. These bits are read as 0.

The RDRHL register can be accessed in 16-bit units.

26.2.4 Transmit Data Register (TDR)

Address(es): SCI1.TDR 0008 A023h, SCI5.TDR 0008 A0A3h, SCI6.TDR 0008 A0C3h, SCI8.TDR 0008 A103h, SCI9.TDR 0008 A123h, SCI11.TDR 000D 0003h

TDR is an 8-bit register that stores transmit data.

When the SCI detects that the TSR register is empty, it transfers the transmit data written in the TDR register to the TSR register and starts transmission.

The double-buffered structures of the TDR register and the TSR register enable continuous serial transmission. If the next transmit data has already been written to the TDR register when one frame of data is transmitted, the SCI transfers the written data to the TSR register to continue transmission.

The CPU is able to read from or write to the TDR register at any time. Only write transmit data to the TDR register once after each instance of the transmit data empty interrupt (TXI).

26.2.5 Transmit Data Register H, L, HL (TDRH, TDRL, TDRHL)

- Transmit Data Register H (TDRH)

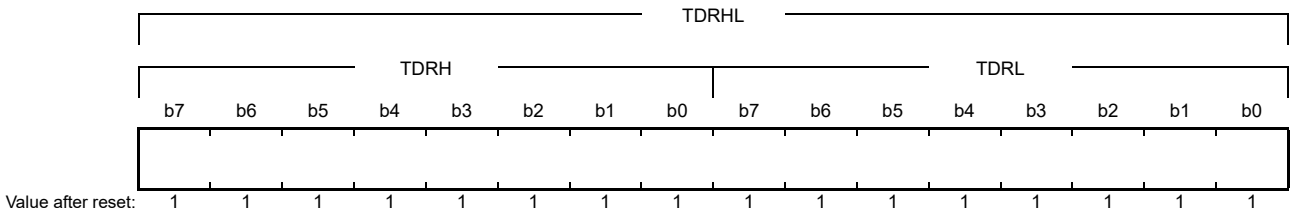
Address(es): SCI1.TDRH 0008 A02Eh, SCI5.TDRH 0008 A0AEh, SCI6.TDRH 0008 A0CEh, SCI8.TDRH 0008 A10Eh, SCI9.TDRH 0008 A12Eh, SCI11.TDRH 000D 000Eh

- Transmit Data Register L (TDRL)

Address(es): SCI1.TDRL 0008 A02Fh, SCI5.TDRL 0008 A0AFh, SCI6.TDRL 0008 A0CFh, SCI8.TDRL 0008 A10Fh, SCI9.TDRL 0008 A12Fh, SCI11.TDRL 000D 000Fh

- Transmit Data Register HL (TDRHL)

Address(es): SCI1.TDRHL 0008 A02Eh, SCI5.TDRHL 0008 A0AEh, SCI6.TDRHL 0008 A0CEh, SCI8.TDRHL 0008 A10Eh, SCI9.TDRHL 0008 A12Eh, SCI11.TDRHL 000D 000Eh



TDRH and TDRL are 8-bit registers that store transmit data. Use these registers when asynchronous mode and 9-bit data length are selected.
TDRL is the shadow register of TDR; i.e. access to TDRL is equivalent to access to TDR.
When empty space is detected in the TSR register, the transmit data stored in the TDRH and TDRL registers is transferred to TSR; i.e., transmitting is started.
The TSR, TDRH and TDRL registers have a double-buffered construction to realize continuous reception. When the next data to be transmitted is stored in the TDRL register after one frame of data has been transmitted, the transmitting operation is continued by transfer to the TSR register.
The CPU can read and write to the TDRH and TDRL registers. Bits 0 to 7 in RDRH are fixed to 1. These bits are read as 1. The write value should be 1.
Writing transmit data to the TDRH and TDRL registers should be performed only once in the order from TDRH to TDRL when a transmit data empty interrupt (TXI) request is issued.
The TDRHL register can be accessed in 16-bit units.

26.2.6 Transmit Shift Register (TSR)

TSR is a shift register that transmits serial data.
To perform serial data transmission, the SCI first automatically transfers transmit data from TDR to TSR, and then sends the data to the TXDn pin.
TSR cannot be directly accessed by the CPU.

26.2.7 Serial Mode Register (SMR)

Note: Some bits in SMR have different functions in smart card interface mode and non-smart card interface mode.

(1) Non-Smart Card Interface Mode (SCMR.SMIF = 0)

Address(es): SCI1.SMR 0008 A020h, SCI5.SMR 0008 A0A0h, SCI6.SMR 0008 A0C0h, SCI8.SMR 0008 A100h, SCI9.SMR 0008 A120h, SCI11.SMR 000D 0000h

	b7	b6	b5	b4	b3	b2	b1	b0
	CM	CHR	PE	PM	STOP	MP	CKS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	CKS[1:0]	Clock Select	b1 b0 0 0: PCLK (n = 0)*1 0 1: PCLK/4 (n = 1)*1 1 0: PCLK/16 (n = 2)*1 1 1: PCLK/64 (n = 3)*1	R/W*4
b2	MP	Multi-Processor Mode	(Valid only in asynchronous mode) 0: Multi-processor communications function is disabled 1: Multi-processor communications function is enabled	R/W*4
b3	STOP	Stop Bit Length	(Valid only in asynchronous mode) 0: 1 stop bit 1: 2 stop bits	R/W*4
b4	PM	Parity Mode	(Valid only when the PE bit is 1) 0: Selects even parity 1: Selects odd parity	R/W*4
b5	PE	Parity Enable	(Valid only in asynchronous mode) • When transmitting 0: Parity bit addition is not performed 1: The parity bit is added • When receiving 0: Parity bit checking is not performed 1: The parity bit is checked	R/W*4
b6	CHR	Character Length	(Valid only in asynchronous mode*2) Selects in combination with the SCMR.CHR1 bit. CHR1 CHR 0 0: Transmit/receive in 9-bit data length 0 1: Transmit/receive in 9-bit data length 1 0: Transmit/receive in 8-bit data length (initial value) 1 1: Transmit/receive in 7-bit data length*3	R/W*4
b7	CM	Communications Mode	0: Asynchronous mode or simple I2C mode 1: Clock synchronous mode or simple SPI mode	R/W*4

Note 1. n is the decimal notation of the value of n in the BRR register (refer to section 26.2.11, Bit Rate Register (BRR)).
Note 2. In other than asynchronous mode, this bit setting is invalid and a fixed data length of 8 bits is used.
Note 3. LSB first is fixed and the MSB (bit 7) in the TDR register is not transmitted in transmission.
Note 4. Writable only when TE in SCR = 0 and RE in SCR = 0 (both serial transmission and reception are disabled).

CKS[1:0] Bits (Clock Select)

These bits select the clock source for the on-chip baud rate generator.

For the relation between the settings of these bits and the baud rate, refer to section 26.2.11, Bit Rate Register (BRR).

MP Bit (Multi-Processor Mode)

Disables/enables the multi-processor communications function. The settings of the PE bit and PM bit are invalid in multi-processor mode.

STOP Bit (Stop Bit Length)

Selects the stop bit length in transmission.
In reception, only the first stop bit is checked regardless of this bit setting. If the second stop bit is 0, it is treated as the start bit of the next transmit frame.

PM Bit (Parity Mode)

Selects the parity mode (even or odd) for transmission and reception.
The setting of the PM bit is invalid in multi-processor mode.

PE Bit (Parity Enable)

When this bit is set to 1, the parity bit is added to transmit data, and the parity bit is checked in reception.
Irrespective of the setting of the PE bit, the parity bit is not added or checked in multi-processor format.

CHR Bit (Character Length)

Selects the data length for transmission and reception.
Selects in combination with the CHR1 bit in SCMR.
In other than asynchronous mode, a fixed data length of 8 bits is used.

(2) Smart Card Interface Mode (SCMR.SMIF = 1)

Address(es): SMCI1.SMR 0008 A020h, SMCI5.SMR 0008 A0A0h, SMCI6.SMR 0008 A0C0h, SMCI8.SMR 0008 A100h, SMCI9.SMR 0008 A120h, SMCI11.SMR 000D 0000h

	b7	b6	b5	b4	b3	b2	b1	b0
	GM	BLK	PE	PM	BCP[1:0]		CKS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	CKS[1:0]	Clock Select	b1 b0 0 0: PCLK (n = 0)*1 0 1: PCLK/4 (n = 1)*1 1 0: PCLK/16 (n = 2)*1 1 1: PCLK/64 (n = 3)*1	R/W*2
b3, b2	BCP[1:0]	Base Clock Pulse	Selects the number of base clock cycles in combination with the SCMR.BCP2 bit. Table 26.6 lists the combinations of the SCMR.BCP2 bit and SMR.BCP[1:0] bits.	R/W*2
b4	PM	Parity Mode	(Valid only when the PE bit is 1) 0: Selects even parity 1: Selects odd parity	R/W*2
b5	PE	Parity Enable	When this bit is set to 1, a parity bit is added to transmit data, and the parity of received data is checked. Set this bit to 1 in smart card interface mode.	R/W*2
b6	BLK	Block Transfer Mode	0: Normal mode operation 1: Block transfer mode operation	R/W*2
b7	GM	GSM Mode	0: Normal mode operation 1: GSM mode operation	R/W*2

Note 1. n is the decimal notation of the value of n in BRR (refer to section 26.2.11, Bit Rate Register (BRR)).
Note 2. Writable only when TE in SCR = 0 and RE in SCR = 0 (both serial transmission and reception are disabled).

CKS[1:0] Bits (Clock Select)

These bits select the clock source for the on-chip baud rate generator.

For the relationship between the settings of these bits and the baud rate, refer to section 26.2.11, Bit Rate Register (BRR).

BCP[1:0] Bits (Base Clock Pulse)

These bits select the number of base clock cycles in a 1-bit data transfer time in smart card interface mode.

Set these bits in combination with the SCMR.BCP2 bit.

For details, refer to section 26.6.4, Receive Data Sampling Timing and Reception Margin.

Table 26.6 Combinations of the SCMR.BCP2 Bit and SMR.BCP[1:0] Bits

SCMR.BCP2 Bit	SMR.BCP[1:0] Bits		Number of Base Clock Cycles for 1-Bit Transfer Period
0	0	0	93 clock cycles (S = 93)*1
0	0	1	128 clock cycles (S = 128)*1
0	1	0	186 clock cycles (S = 186)*1
0	1	1	512 clock cycles (S = 512)*1
1	0	0	32 clock cycles (S = 32)*1 (Initial Value)
1	0	1	64 clock cycles (S = 64)*1
1	1	0	372 clock cycles (S = 372)*1
1	1	1	256 clock cycles (S = 256)*1

Note 1. S is the value of S in BRR (refer to section 26.2.11, Bit Rate Register (BRR)).

PM Bit (Parity Mode)

Selects the parity mode for transmission and reception (even or odd).
For details on the usage of this bit in smart card interface mode, refer to section 26.6.2, Data Format (Except in Block Transfer Mode).

PE Bit (Parity Enable)

Set the PE bit to 1.
The parity bit is added to transmit data before transmission, and the parity bit is checked in reception.

BLK Bit (Block Transfer Mode)

Setting this bit to 1 allows block transfer mode operation.
For details, refer to section 26.6.3, Block Transfer Mode.

GM Bit (GSM Mode)

Setting this bit to 1 allows GSM mode operation.
In GSM mode, the SSR.TEND flag set timing is put forward to 11.0 etu (elementary time unit = 1-bit transfer time) from the start and the clock output control function is appended. For details, refer to section 26.6.6, Serial Data Transmission (Except in Block Transfer Mode) and section 26.6.8, Clock Output Control.

26.2.8 Serial Control Register (SCR)

Note: Some bits in the SCR register have different functions in smart card interface mode and non-smart card interface mode.

(1) Non-Smart Card Interface Mode (SCMR.SMIF = 0)

Address(es): SCI1.SCR 0008 A022h, SCI5.SCR 0008 A0A2h, SCI6.SCR 0008 A0C2h, SCI8.SCR 0008 A102h, SCI9.SCR 0008 A122h, SCI11.SCR 000D 0002h

	b7	b6	b5	b4	b3	b2	b1	b0
	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	CKE[1:0]	Clock Enable	• For SCI1, SCI8 SCI9, and SCI11 (Asynchronous mode) b1 b0 0 0: On-chip baud rate generator The SCKn pin functions as I/O port. 0 1: On-chip baud rate generator The clock with the same frequency as the bit rate is output from the SCKn pin. 1 x: External clock The clock with a frequency 16 times the bit rate should be input from the SCKn pin. Input a clock signal with a frequency eight times the bit rate when the SEMR.ABCS bit is 1. (Clock synchronous mode) b1 b0 0 x: Internal clock The SCKn pin functions as the clock output pin. 1 x: External clock The SCKn pin functions as the clock input pin.	R/W*1
b1, b0	CKE[1:0]	Clock Enable	• For SCI5 and SCI6 (Asynchronous mode) b1 b0 0 0: On-chip baud rate generator The SCKn pin is available for use as an I/O port according to the I/O port settings. 0 1: On-chip baud rate generator The clock with the same frequency as the bit rate is output from the SCKn pin. 1 x: External clock or TMR clock • The clock with a frequency 16 times the bit rate should be input from the SCKn pin. Input a clock signal with a frequency eight times the bit rate when the SEMR.ABCS bit is 1. • The TMR clock can be used. The SCKn pin is available for use as an I/O port according to the I/O port settings when the TMR clock is used. (Clock synchronous mode) b1 b0 0 x: Internal clock The SCKn pin functions as the clock output pin. 1 x: External clock The SCKn pin functions as the clock input pin.	R/W*1
b2	TEIE	Transmit End Interrupt Enable	0: A TEI interrupt request is disabled 1: A TEI interrupt request is enabled	R/W

Bit	Symbol	Bit Name	Description	R/W
b3	MPIE	Multi-Processor Interrupt Enable	(Valid in asynchronous mode when SMR.MP = 1) 0: Normal reception 1: When the data with the multi-processor bit set to 0 is received, the data is not read, and setting the status flags ORER and FER in SSR to 1 is disabled. When the data with the multi-processor bit set to 1 is received, the MPIE bit is automatically cleared to 0, and normal reception is resumed.	R/W
b4	RE	Receive Enable	0: Serial reception is disabled 1: Serial reception is enabled	R/W*2
b5	TE	Transmit Enable	0: Serial transmission is disabled 1: Serial transmission is enabled	R/W*2
b6	RIE	Receive Interrupt Enable	0: RXI and ERI interrupt requests are disabled 1: RXI and ERI interrupt requests are enabled	R/W
b7	TIE	Transmit Interrupt Enable	0: A TXI interrupt request is disabled 1: A TXI interrupt request is enabled	R/W

x: Don't care

Note 1. Writable only when TE = 0 and RE = 0.

Note 2. 1 can be written only when TE = 0 and RE = 0, while the SMR.CM bit is 1. After setting TE or RE to 1, only 0 can be written to TE and RE. While the SMR.CM bit is 0 and the SIMR1.IICM bit is 0, writing is enabled under any condition.

CKE[1:0] Bits (Clock Enable)

These bits select the clock source and SCKn pin function.

The combination of the settings of these bits and of the SEMR.ACS0 bit sets the internal TMR clock.

TEIE Bit (Transmit End Interrupt Enable)

Enables or disables a TEI interrupt request.

A TEI interrupt request is disabled by setting the TEIE bit to 0.

In simple I^2C mode, the TEI is allocated to the interrupt on completion of issuing a start, restart, or stop condition (STI). In this case, the TEIE bit can be used to enable or disable the STI.

MPIE Bit (Multi-Processor Interrupt Enable)

When this bit is set to 1 and the data with the multi-processor bit set to 0 is received, the data is not read and setting the status flags ORER and FER in the SSR register to 1 is disabled. When the data with the multi-processor bit set to 1 is received, the MPIE bit is automatically cleared to 0, and normal reception is resumed. For details, refer to section 26.4, Multi-Processor Communications Function.

When the data with the multi-processor bit set to 0 is received, the receive data is not transferred from the RSR to the RDR, a receive error is not detected, and setting the flags ORER and FER to 1 is disabled.

When the data with the multi-processor bit set to 1 is received, the MPB bit is set to 1, the MPIE bit is automatically cleared to 0, the RXI and ERI interrupt requests are enabled (if the SCR.RIE bit is set to 1), and setting the flags ORER and FER to 1 is enabled.

Set the MPIE bit to 0 if multi-processor communications function is not to be used.

RE Bit (Receive Enable)

Enables or disables serial reception.

When this bit is set to 1, serial reception is started by detecting the start bit in asynchronous mode or the synchronous clock input in clock synchronous mode. Note that the SMR register should be set prior to setting the RE bit to 1 in order to designate the reception format.

Even if reception is halted by setting the RE bit to 0, the ORER, FER, PER, and RDRF flags in the SSR register are not affected and the previous value is retained.

TE Bit (Transmit Enable)

Enables or disables serial transmission.

When this bit is set to 1, serial transmission is started by writing transmit data to TDR. Note that SMR should be set prior to setting the TE bit to 1 in order to designate the transmission format.

RIE Bit (Receive Interrupt Enable)

Enables or disables RXI and ERI interrupt requests.

An RXI interrupt request is disabled by setting the RIE bit to 0.

An ERI interrupt request can be canceled by reading 1 from the ORER, FER, or PER flag in the SSR register and then setting the flag to 0, or setting the RIE bit to 0.

TIE Bit (Transmit Interrupt Enable)

Enables or disables TXI interrupt request.

A TXI interrupt request is disabled by setting the TIE bit to 0.

(2) Smart Card Interface Mode (SCMR.SMIF = 1)

Address(es): SMCI1.SCR 0008 A022h, SMCI5.SCR 0008 A0A2h, SMCI6.SCR 0008 A0C2h, SMCI8.SCR 0008 A102h, SMCI9.SCR 0008 A122h, SMCI11.SCR 000D 0002h

	b7	b6	b5	b4	b3	b2	b1	b0
	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	CKE[1:0]	Clock Enable	• When SMR.GM = 0 b1 b0 0 0: Output disabled (The SCKn pin is available for use as an I/O port according to the I/O port settings.) 0 1: Clock output 1 x: (Setting prohibited) • When SMR.GM = 1 b1 b0 0 0: Output fixed low x 1: Clock output 1 0: Output fixed high	R/W*1
b2	TEIE	Transmit End Interrupt Enable	This bit should be 0 in smart card interface mode.	R/W
b3	MPIE	Multi-Processor Interrupt Enable	This bit should be 0 in smart card interface mode.	R/W
b4	RE	Receive Enable	0: Serial reception is disabled 1: Serial reception is enabled	R/W*2
b5	TE	Transmit Enable	0: Serial transmission is disabled 1: Serial transmission is enabled	R/W*2
b6	RIE	Receive Interrupt Enable	0: RXI and ERI interrupt requests are disabled 1: RXI and ERI interrupt requests are enabled	R/W
b7	TIE	Transmit Interrupt Enable	0: A TXI interrupt request is disabled 1: A TXI interrupt request is enabled	R/W

x: Don't care

Note 1. Writable only when TE = 0 and RE = 0.

Note 2. 1 can be written only when TE = 0 and RE = 0. After setting TE or RE to 1, only 0 can be written in TE and RE.

For details on interrupt requests, refer to section 26.11, Interrupt Sources.

CKE[1:0] Bits (Clock Enable)

These bits control the clock output from the SCKn pin.

In GSM mode, clock output can be dynamically switched. For details, refer to section 26.6.8, Clock Output Control.

TEIE Bit (Transmit End Interrupt Enable)

This bit should be 0 in smart card interface mode.

MPIE Bit (Multi-Processor Interrupt Enable)

This bit should be 0 in smart card interface mode.

RE Bit (Receive Enable)

Enables or disables serial reception.

When this bit is set to 1, serial reception is started by detecting the start bit. Note that the SMR register should be set prior to setting the RE bit to 1 in order to designate the reception format.

Even if reception is halted by setting the RE bit to 0, the ORER, FER, and PER flags in the SSR register are not affected and the previous value is retained.

TE Bit (Transmit Enable)

Enables or disables serial transmission.

When this bit is set to 1, serial transmission is started by writing transmit data to the TDR register. Note that the SMR register should be set prior to setting the TE bit to 1 in order to designate the transmission format.

RIE Bit (Receive Interrupt Enable)

Enables or disables RXI and ERI interrupt requests.

An RXI interrupt request is disabled by setting the RIE bit to 0.

An ERI interrupt request can be canceled by reading 1 from the ORER, FER, or PER flag in the SSR register and then setting the flag to 0, or setting the RIE bit to 0.

TIE Bit (Transmit Interrupt Enable)

Enables or disables TXI interrupt request.

A TXI interrupt request is disabled by setting the TIE bit to 0.

26.2.9 Serial Status Register (SSR)

Some bits in the SSR register have different functions in smart card interface mode and non-smart card interface mode.

(1) Non-Smart Card Interface Mode (SCMR.SMIF = 0)

Address(es): SCI1.SSR 0008 A024h, SCI5.SSR 0008 A0A4h, SCI6.SSR 0008 A0C4h, SCI8.SSR 0008 A104h, SCI9.SSR 0008 A124h, SCI11.SSR 000D 0004h

	b7	b6	b5	b4	b3	b2	b1	b0
	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT
Value after reset:	1	0	0	0	0	1	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	MPBT	Multi-Processor Bit Transfer	Sets the multi-processor bit for adding to the transmission frame 0: Data transmission cycles 1: ID transmission cycles	R/W
b1	MPB	Multi-Processor	Value of the multi-processor bit in the reception frame 0: Data transmission cycles 1: ID transmission cycles	R
b2	TEND	Transmit End Flag	0: A character is being transmitted. 1: Character transfer has been completed.	R
b3	PER	Parity Error Flag	0: No parity error occurred 1: A parity error has occurred	R/(W) *1
b4	FER	Framing Error Flag	0: No framing error occurred 1: A framing error has occurred	R/(W) *1
b5	ORER	Overrun Error Flag	0: No overrun error occurred 1: An overrun error has occurred	R/(W) *1
b6	RDRF	Receive Data Full Flag	0: No valid data is held in the RDR register 1: Received data is held in the RDR register	R/(W) *2
b7	TDRE	Transmit Data Empty Flag	0: Data to be transmitted is held in the TDR register 1: No data is held in the TDR register	R/(W) *2

Note 1. Only 0 can be written to this bit, to clear the flag. To clear this flag, confirm that the flag is 1 and then set it to 0.
Note 2. Write 1 when writing is necessary.

MPB Bit (Multi-Processor)

Holds the value of the multi-processor bit in the reception frame. This bit does not change when the SCR.RE bit is 0.

TEND Flag (Transmit End Flag)

Indicates completion of transmission.

[Setting conditions]

- When the SCR.TE bit is set to 0 (serial transmission is disabled)
  When the SCR.TE bit is changed from 0 to 1, the TEND flag is not affected and retains the value 1.
- When the TDR register is not updated at the time of transmission of the tail-end bit of a character being transmitted

[Clearing condition]

- When transmit data are written to the TDR register while the SCR.TE bit is 1
  When setting the TEND flag to 0 to complete the interrupt handling, refer to section 14.4.1.2, Operation of Status Flags for Level-Detected Interrupts.

PER Flag (Parity Error Flag)

Indicates that a parity error has occurred during reception in asynchronous mode and the reception ends abnormally.

[Setting condition]

- When a parity error is detected during reception
  Although receive data when the parity error occurs is transferred to RDR, no RXI interrupt request occurs. Note that when the PER flag is being set to 1, the subsequent receive data is not transferred to RDR.

[Clearing condition]

- When 0 is written to PER after reading PER = 1
  When setting the PER flag to 0 to complete the interrupt handling, refer to section 14.4.1.2, Operation of Status Flags for Level-Detected Interrupts.
  Even when the SCR.RE bit is set to 0 (serial reception is disabled), the PER flag is not affected and retains its previous value.

FER Flag (Framing Error Flag)

Indicates that a framing error has occurred during reception in asynchronous mode and the reception ends abnormally.

[Setting condition]

- When the stop bit is 0
  In 2-stop-bit mode, only the first stop bit is checked whether it is 1 but the second stop bit is not checked. Note that although receive data when the framing error occurs is transferred to RDR, no RXI interrupt request occurs. In addition, when the FER flag is being set to 1, the subsequent receive data is not transferred to RDR.

[Clearing condition]

- When 0 is written to FER after reading FER = 1
  When setting the FER flag to 0 to complete the interrupt handling, refer to section 14.4.1.2, Operation of Status Flags for Level-Detected Interrupts.
  Even when the SCR.RE bit is set to 0, the FER flag is not affected and retains its previous value.

ORER Flag (Overrun Error Flag)

Indicates that an overrun error has occurred during reception and the reception ends abnormally.

[Setting condition]

- When the next data is received before receive data is read from RDR
  In RDR, receive data prior to an overrun error occurrence is retained, but data received after the overrun error occurrence is lost. When the ORER flag is set to 1, subsequent serial reception cannot be performed. Note that, in clock synchronous mode, serial transmission also cannot continue.

[Clearing condition]

- When 0 is written to ORER after reading ORER = 1
  When setting the ORER flag to 0 to complete the interrupt handling, refer to section 14.4.1.2, Operation of Status Flags for Level-Detected Interrupts.
  Even when the SCR.RE bit is set to 0, the ORER flag is not affected and retains its previous value.

RDRF Flag (Receive Data Full Flag)

Indicates whether the RDR register has received data.

[Setting condition]

- When data has been received normally, and transferred from RSR to RDR

[Clearing condition]

- When data is read from RDR

TDRE Flag (Transmit Data Empty Flag)

Indicates whether the TDR register has data to be transmitted.

[Setting condition]

- When data is transferred from TDR to TSR

[Clearing condition]

- When data is written to TDR

(2) Smart Card Interface Mode (SCMR.SMIF = 1)

Address(es): SMCI1.SSR 0008 A024h, SMCI5.SSR 0008 A0A4h, SMCI6.SSR 0008 A0C4h, SMCI8.SSR 0008 A104h, SMCI9.SSR 0008 A124h, SMCI11.SSR 000D 0004h

	b7	b6	b5	b4	b3	b2	b1	b0
	TDRE	RDRF	ORER	ERS	PER	TEND	MPB	MPBT
Value after reset:	1	0	0	0	0	1	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	MPBT	Multi-Processor Bit Transfer	This bit should be set to 0 in smart card interface mode.	R/W
b1	MPB	Multi-Processor	This bit is not used in smart card interface mode. It should be set to 0.	R
b2	TEND	Transmit End Flag	0: A character is being transmitted. 1: Character transfer has been completed.	R
b3	PER	Parity Error Flag	0: No parity error occurred 1: A parity error has occurred	R/(W) *1
b4	ERS	Error Signal Status Flag	0: Low error signal not responded 1: Low error signal responded	R/(W) *1
b5	ORER	Overrun Error Flag	0: No overrun error occurred 1: An overrun error has occurred	R/(W) *1
b6	RDRF	Receive Data Full Flag	0: No valid data is held in the RDR register 1: Received data is held in the RDR register	R/(W) *2
b7	TDRE	Transmit Data Empty Flag	0: Data to be transmitted is held in the TDR register 1: No data is held in the TDR register	R/(W) *2

Note 1. Only 0 can be written to this bit, to clear the flag. To clear this flag, confirm that the flag is 1 and then set it to 0.
Note 2. Write 1 when writing is necessary.

TEND Flag (Transmit End Flag)

With no error signal from the receiving side, this bit is set to 1 when further data for transfer is ready to be transferred to the TDR register.

[Setting conditions]

- When the SCR.TE bit = 0 (serial transmission is disabled)
  When the SCR.TE bit is changed from 0 to 1, the TEND flag is not affected and retains the value 1.
- When a specified period has elapsed after the latest transmission of 1 byte, the ERS flag is 0, and the TDR register is not updated
  The set timing is determined by register settings as listed below.
  When SMR.GM = 0 and SMR.BLK = 0, 12.5 etu after the start of transmission
  When SMR.GM = 0 and SMR.BLK = 1, 11.5 etu after the start of transmission
  When SMR.GM = 1 and SMR.BLK = 0, 11.0 etu after the start of transmission
  When SMR.GM = 1 and SMR.BLK = 1, 11.0 etu after the start of transmission

[Clearing condition]

- When transmit data are written to the TDR register while the SCR.TE bit is 1
  When setting the TEND flag to 0 to complete the interrupt handling, refer to section 14.4.1.2, Operation of Status Flags for Level-Detected Interrupts.

PER Flag (Parity Error Flag)

Indicates that a parity error has occurred during reception in asynchronous mode and the reception ends abnormally.

[Setting condition]

- When a parity error is detected during reception
  Although receive data when the parity error occurs is transferred to RDR, no RXI interrupt request occurs. Note that when the PER flag is being set to 1, the subsequent receive data is not transferred to RDR.

[Clearing condition]

- When 0 is written to PER after reading PER = 1
  When setting the PER flag to 0 to complete the interrupt handling, refer to section 14.4.1.2, Operation of Status Flags for Level-Detected Interrupts.
  Even when the SCR.RE bit is set to 0 (serial reception is disabled), the PER flag is not affected and retains its previous value.

ERS Flag (Error Signal Status Flag)

[Setting condition]

- When a low error signal is sampled

[Clearing condition]

- When 0 is written to ERS after reading ERS = 1
  When setting the ERS flag to 0 to complete the interrupt handling, refer to section 14.4.1.2, Operation of Status Flags for Level-Detected Interrupts.
  Even when the SCR.RE bit is set to 0, the ERS flag is not affected and retains its previous value.

ORER Flag (Overrun Error Flag)

Indicates that an overrun error has occurred during reception and the reception ends abnormally.

[Setting condition]

- When the next data is received before receive data is read from RDR
  In RDR, the receive data prior to an overrun error occurrence is retained, but data received following the overrun error occurrence is lost. When the ORER flag is set to 1, subsequent serial reception cannot be performed.

[Clearing condition]

- When 0 is written to ORER after reading ORER = 1
  When setting the ORER flag to 0 to complete the interrupt handling, refer to section 14.4.1.2, Operation of Status Flags for Level-Detected Interrupts.
  Even when the SCR.RE bit is set to 0, the ORER flag is not affected and retains its previous value.

RDRF Flag (Receive Data Full Flag)

Indicates whether the RDR register has received data.

[Setting condition]

- When data has been received normally, and transferred from RSR to RDR

[Clearing condition]

- When data is read from RDR

TDRE Flag (Transmit Data Empty Flag)

Indicates whether the TDR register has data to be transmitted.

[Setting condition]

- When data is transferred from TDR to TSR

[Clearing condition]

- When data is written to TDR

26.2.10 Smart Card Mode Register (SCMR)

Address(es): SMCI1.SCMR 0008 A026h, SMCI5.SCMR 0008 A0A6h, SMCI6.SCMR 0008 A0C6h, SMCI8.SCMR 0008 A106h, SMCI9.SCMR 0008 A126h, SMCI11.SCMR 000D 0006h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCP2	—	—	CHR1	SDIR	SINV	—	SMIF
Value after reset:	1	1	1	1	0	0	1	0

Bit	Symbol	Bit Name	Description	R/W
b0	SMIF	Smart Card Interface Mode Select	0: Non-smart card interface mode (Asynchronous mode, clock synchronous mode, simple SPI mode, or simple I2C mode) 1: Smart card interface mode	R/W*1
b1	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b2	SINV	Transmitted/Received Data Invert	0: TDR contents are transmitted as they are. Receive data is stored as it is in RDR. 1: TDR contents are inverted before being transmitted. Receive data is stored in inverted form in RDR.	R/W*1
b3	SDIR	Transmitted/Received Data Transfer Direction	This bit can be used in the following modes. • Smart card interface mode • Asynchronous mode (multi-processor mode) • Clock synchronous mode • Simple SPI mode Set this bit to 1 if operation is to be in simple I2C mode. 0: Transfer with LSB first 1: Transfer with MSB first	R/W*1
b4	CHR1	Character Length 1	(Only valid in asynchronous mode)*2 Selects in combination with the SMR.CHR bit. CHR1 CHR 0 0: Transmit/receive in 9-bit data length 0 1: Transmit/receive in 9-bit data length 1 0: Transmit/receive in 8-bit data length (initial value) 1 1: Transmit/receive in 7-bit data length*3	R/W*1
b6, b5	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b7	BCP2	Base Clock Pulse 2	Selects the number of base clock cycles in combination with the SMR.BCP[1:0] bits. Table 26.7 lists the combinations of the SCMR.BCP2 bit and SMR.BCP[1:0] bits.	R/W*1

Note 1. Writable only when TE in SCR = 0 and RE in SCR = 0 (both serial transmission and reception are disabled).
Note 2. The setting is invalid and a fixed data length of 8 bits is used in modes other than asynchronous mode.
Note 3. LSB first should be selected and the value of MSB (b7) in the TDR register cannot be transmitted.

SMIF Bit (Smart Card Interface Mode Select)

When this bit is set to 1, smart card interface mode is selected.

When this bit is set to 0, non-smart card interface mode, i.e., asynchronous mode (including multi-processor mode), clock synchronous mode, simple SPI mode, or simple I2C mode is selected.

SINV Bit (Transmitted/Received Data Invert)

Inverts the transmit/receive data logic level. This bit does not affect the logic level of the parity bit. To invert the parity bit, invert the PM bit in the SMR register.

CHR1 bit (Character Length 1)

Selects the data length of transmit/receive data.

Selects in combination with the CHR bit in SMR.

A fixed data length of 8 bits is used in modes other than asynchronous mode.

BCP2 Bit (Base Clock Pulse 2)

Selects the number of base clock cycles in a 1-bit data transfer time in smart card interface mode. Set this bit in combination with the SMR.BCP[1:0] bits.

Table 26.7 Combinations of the SCMR.BCP2 Bit and SMR.BCP[1:0] Bits

SCMR.BCP2 Bit	SMR.BCP[1:0] Bits		Number of Base Clock Cycles for 1-Bit Transfer Period
0	0	0	93 clock cycles (S = 93)*1
0	0	1	128 clock cycles (S = 128)*1
0	1	0	186 clock cycles (S = 186)*1
0	1	1	512 clock cycles (S = 512)*1
1	0	0	32 clock cycles (S = 32)*1 (Initial Value)
1	0	1	64 clock cycles (S = 64)*1
1	1	0	372 clock cycles (S = 372)*1
1	1	1	256 clock cycles (S = 256)*1

Note 1. S is the value of S in BRR (refer to section 26.2.11, Bit Rate Register (BRR)).

26.2.11 Bit Rate Register (BRR)

Address(es): SCI1.BRR 0008 A021h, SCI5.BRR 0008 A0A1h, SCI6.BRR 0008 A0C1h, SCI8.BRR 0008 A101h, SCI9.BRR 0008 A121h, SCI11.BRR 000D 0001h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1

The BRR register is an 8-bit register that adjusts the bit rate.
As each SCI channel has independent baud rate generator control, different bit rates can be set for each. Table 26.8 shows the relationship between the setting (N) in the BRR register and the bit rate (B) for normal asynchronous mode, multi-processor transfer, clock synchronous mode, smart card interface mode, simple SPI mode, and simple I²C mode. The BRR register is writable only when the TE and RE bits in the SCR register are 0.

Table 26.8 Relationship between N Setting in BRR and Bit Rate B

Mode	SEMR Settings		BRR Setting	Error
	BGDM Bit	ABCS Bit		
Asynchronous, multi-processor transfer	0	0	$N = \frac{PCLK \times 10^6}{64 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \{\frac{PCLK \times 10^6}{B \times 64 \times 2^{2n-1} \times (N+1)} - 1\} \times 100$
	0	1	$N = \frac{PCLK \times 10^6}{32 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \{\frac{PCLK \times 10^6}{B \times 32 \times 2^{2n-1} \times (N+1)} - 1\} \times 100$
	1	0		
	1	1	$N = \frac{PCLK \times 10^6}{16 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \{\frac{PCLK \times 10^6}{B \times 16 \times 2^{2n-1} \times (N+1)} - 1\} \times 100$
Clock synchronous, simple SPI			$N = \frac{PCLK \times 10^6}{8 \times 2^{2n-1} \times B} - 1$	
Smart card interface			$N = \frac{PCLK \times 10^6}{S \times 2^{2n+1} \times B} - 1$	$Error\ (\%) = \{\frac{PCLK \times 10^6}{B \times S \times 2^{2n+1} \times (N+1)} - 1\} \times 100$
Simple I²C*1			$N = \frac{PCLK \times 10^6}{64 \times 2^{2n-1} \times B} - 1$	

B: Bit rate (bps)
N: BRR setting for on-chip baud rate generator ($0 \le N \le 255$)
PCLK: Operating frequency (MHz)
n and S: Determined by the settings of the SMR and SCMR registers as listed in the table below.
Note 1. Adjust the bit rate so that the widths at high and low level of the SCL output in simple I²C mode satisfy the I²C standard.

Table 26.9 Calculating Widths at High and Low Level for SCL

Mode	SCL	Formula (Result in Seconds)
I²C	Width at high level (minimum value)	$(N+1) \times 4 \times 2^{2n-1} \times 7 \times \frac{1}{PCLK \times 10^6}$
	Width at low level (minimum value)	$(N+1) \times 4 \times 2^{2n-1} \times 8 \times \frac{1}{PCLK \times 10^6}$

Table 26.10 Clock Source Settings

SMR.CKS[1:0] Bit Setting	Clock Source	n
0 0	PCLK	0
0 1	PCLK/4	1
1 0	PCLK/16	2
1 1	PCLK/64	3

Table 26.11 Base Clock Settings in Smart Card Interface Mode

SCMR.BCP2 Bit Setting	SMR.BCP[1:0] Bit Setting	Base Clock Cycles for 1-bit Period	S
0	0 0	93 clock cycles	93
0	0 1	128 clock cycles	128
0	1 0	186 clock cycles	186
0	1 1	512 clock cycles	512
1	0 0	32 clock cycles	32
1	0 1	64 clock cycles	64
1	1 0	372 clock cycles	372
1	1 1	256 clock cycles	256

Table 26.12 lists examples of N settings in BRR in normal asynchronous mode. Table 26.13 lists the maximum bit rate settable for each operating frequency. Examples of BRR (N) settings in clock synchronous mode and simple SPI mode are listed in Table 26.16. Examples of BRR (N) settings in smart card interface mode are listed in Table 26.18. Examples of BRR (N) settings in simple I^2C mode are listed in Table 26.20. In smart card interface mode, the number of base clock cycles S in a 1-bit data transfer time can be selected. For details, refer to section 26.6.4, Receive Data Sampling Timing and Reception Margin. Table 26.14 and Table 26.17 list the maximum bit rates with external clock input.

When either the asynchronous mode base clock select bit (ABCS) or the baud rate generator double-speed mode select bit (BGDM) in the serial extended mode register (SEMR) is set to 1 in asynchronous mode, the bit rate becomes twice that listed in Table 26.12. When both of those registers are set to 1, the bit rate becomes four times the listed value.

Table 26.12 Examples of BRR Settings for Various Bit Rates (Asynchronous Mode)

Bit Rate (bps)	Operating Frequency PCLK (MHz)														
	8			9.8304			10			12			12.288		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	141	0.03	2	174	–0.26	2	177	–0.25	2	212	0.03	2	217	0.08
150	2	103	0.16	2	127	0.00	2	129	0.16	2	155	0.16	2	159	0.00
300	1	207	0.16	1	255	0.00	2	64	0.16	2	77	0.16	2	79	0.00
600	1	103	0.16	1	127	0.00	1	129	0.16	1	155	0.16	1	159	0.00
1200	0	207	0.16	0	255	0.00	1	64	0.16	1	77	0.16	1	79	0.00
2400	0	103	0.16	0	127	0.00	0	129	0.16	0	155	0.16	0	159	0.00
4800	0	51	0.16	0	63	0.00	0	64	0.16	0	77	0.16	0	79	0.00
9600	0	25	0.16	0	31	0.00	0	32	–1.36	0	38	0.16	0	39	0.00
19200	0	12	0.16	0	15	0.00	0	15	1.73	0	19	–2.34	0	19	0.00
31250	0	7	0.00	0	9	–1.70	0	9	0.00	0	11	0.00	0	11	2.40
38400	—	—	—	0	7	0.00	0	7	1.73	0	9	–2.34	0	9	0.00

Bit Rate (bps)	Operating Frequency PCLK (MHz)														
	14			16			17.2032			18			19.6608		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	248	–0.17	3	70	0.03	3	75	0.48	3	79	–0.12	3	86	0.31
150	2	181	0.16	2	207	0.16	2	223	0.00	2	233	0.16	2	255	0.00
300	2	90	0.16	2	103	0.16	2	111	0.00	2	116	0.16	2	127	0.00
600	1	181	0.16	1	207	0.16	1	223	0.00	1	233	0.16	1	255	0.00
1200	1	90	0.16	1	103	0.16	1	111	0.00	1	116	0.16	1	127	0.00
2400	0	181	0.16	0	207	0.16	0	223	0.00	0	233	0.16	0	255	0.00
4800	0	90	0.16	0	103	0.16	0	111	0.00	0	116	0.16	0	127	0.00
9600	0	45	–0.93	0	51	0.16	0	55	0.00	0	58	–0.69	0	63	0.00
19200	0	22	–0.93	0	25	0.16	0	27	0.00	0	28	1.02	0	31	0.00
31250	0	13	0.00	0	15	0.00	0	16	1.20	0	17	0.00	0	19	–1.70
38400	—	—	—	0	12	0.16	0	13	0.00	0	14	–2.34	0	15	0.00

Bit Rate (bps)	Operating Frequency PCLK (MHz)														
	20			25			30			33			40		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	3	88	–0.25	3	110	–0.02	3	132	0.13	3	145	0.33	3	177	–0.25
150	3	64	0.16	3	80	0.47	3	97	–0.35	3	106	0.39	3	129	0.16
300	2	129	0.16	2	162	–0.15	2	194	0.16	2	214	–0.07	3	64	0.16
600	2	64	0.16	2	80	0.47	2	97	–0.35	2	106	0.39	2	129	0.16
1200	1	129	0.16	1	162	–0.15	1	194	0.16	1	214	–0.07	2	64	0.16
2400	1	64	0.16	1	80	0.47	1	97	–0.35	1	106	0.39	1	129	0.16
4800	0	129	0.16	0	162	–0.15	0	194	0.16	0	214	–0.07	1	64	0.16
9600	0	64	0.16	0	80	0.47	0	97	–0.35	0	106	0.39	0	129	0.16
19200	0	32	–1.36	0	40	–0.76	0	48	–0.35	0	53	–0.54	0	64	0.16
31250	0	19	0.00	0	24	0.00	0	29	0.00	0	32	0.00	0	39	0.00
38400	0	15	1.73	0	19	1.73	0	23	1.73	0	26	–0.54	0	32	–1.36

Bit Rate (bps)	Operating Frequency PCLK (MHz)					
	64*1			80*1		
	n	N	Error (%)	n	N	Error (%)
110						
150	3	207	0.16	3	255	1.73
300	3	103	0.16	3	129	0.16
600	3	51	0.16	3	64	0.16
1200	2	103	0.16	2	129	0.16
2400	2	51	0.16	2	64	0.16
4800	1	103	0.16	1	129	0.16
9600	1	51	0.16	1	64	0.16
19200	0	103	0.16	0	129	0.16
31250	0	63	0.00	0	79	0.00
38400	0	51	0.16	0	64	0.16

Note: This is an example when the ABCS and BGDM bits in SEMR are 0.
When either the ABCS bit or BGDM bit is set to 1, the bit rate doubles.
When both ABCS and BGDM bits in SEMR are set to 1, the bit rate increases four times.

Note 1. Supported by SCI11 only.

Table 26.13 Maximum Bit Rate for Each Operating Frequency (Asynchronous Mode)

	SEMR Settings						SEMR Settings				
PCLK (MHz)	BGDM Bit	ABCS Bit	n	N	Maximum Bit Rate (bps)	PCLK (MHz)	BGDM Bit	ABCS Bit	n	N	Maximum Bit Rate (bps)
8	0	0	0	0	250000	19.6608	0	0	0	0	614400
		1	0	0	500000			1	0	0	1228800
	1	0	0	0			1	0	0	0	
		1	0	0	1000000			1	0	0	2457600
9.8304	0	0	0	0	307200	20	0	0	0	0	625000
		1	0	0	614400			1	0	0	1250000
	1	0	0	0			1	0	0	0	
		1	0	0	1228800			1	0	0	2500000
10	0	0	0	0	312500	25	0	0	0	0	781250
		1	0	0	625000			1	0	0	1562500
	1	0	0	0			1	0	0	0	
		1	0	0	1250000			1	0	0	3125000
12	0	0	0	0	375000	30	0	0	0	0	937500
		1	0	0	750000			1	0	0	1875000
	1	0	0	0			1	0	0	0	
		1	0	0	1500000			1	0	0	3750000
12.288	0	0	0	0	384000	33	0	0	0	0	1031250
		1	0	0	768000			1	0	0	2062500
	1	0	0	0			1	0	0	0	
		1	0	0	1536000			1	0	0	4125000
14	0	0	0	0	437500	40	0	0	0	0	1250000
		1	0	0	875000			1	0	0	2500000
	1	0	0	0			1	0	0	0	
		1	0	0	1750000			1	0	0	5000000
16	0	0	0	0	500000	64*1	0	0	0	0	2000000
		1	0	0	1000000			1	0	0	4000000
	1	0	0	0			1	0	0	0	
		1	0	0	2000000			1	0	0	8000000
17.2032	0	0	0	0	537600	80*1	0	0	0	0	2500000
		1	0	0	1075200			1	0	0	5000000
	1	0	0	0			1	0	0	0	
		1	0	0	2150400			1	0	0	10000000
18	0	0	0	0	562500						
		1	0	0	1125000						
	1	0	0	0							
		1	0	0	2250000						

Note 1. Supported by SCI11 only.

Table 26.14 Maximum Bit Rate with External Clock Input (Asynchronous Mode)

		Maximum Bit Rate (bps)	
PCLK (MHz)	External Input Clock (MHz)	SEMR.ABCS Bit = 0	SEMR.ABCS Bit = 1
8	2.0000	125000	250000
9.8304	2.4576	153600	307200
10	2.5000	156250	312500
12	3.0000	187500	375000
12.288	3.0720	192000	384000
14	3.5000	218750	437500
16	4.0000	250000	500000
17.2032	4.3008	268800	537600
18	4.5000	281250	562500
19.6608	4.9152	307200	614400
20	5.0000	312500	625000
25	6.2500	390625	781250
30	7.5000	468750	937500
33	8.2500	515625	1031250
40	10.0000	625000	1250000
Over 40*1	10.0000	625000	1250000

Note 1. Supported by SCI11 only.

Table 26.15 Maximum Bit Rate with TMR Clock Input (Asynchronous Mode)

		Maximum Bit Rate (bps)	
PCLK (MHz)	TMR Clock (MHz)	SEMR.ABCS Bit = 0	SEMR.ABCS Bit = 1
8	4	250000	500000
9.8304	4.9152	307200	614400
10	5	312500	625000
12	6	375000	750000
12.288	6.144	384000	768000
14	7	437500	875000
16	8	500000	1000000
17.2032	8.6016	537600	1075200
18	9	562500	1125000
19.6608	9.8304	614400	1228800
20	10	625000	1250000
25	12.5	781250	1562500
30	15	937500	1875000
33	16.5	1031250	2062500
40	20	1250000	2500000

Table 26.16 BRR Settings for Various Bit Rates (Clock Synchronous Mode, Simple SPI Mode)

Bit Rate (bps)	Operating Frequency PCLK (MHz)																			
	8		10		16		20		25		30		33		40		64*1		80*1	
	n	N	n	N	n	N	n	N	n	N	n	N	n	N	n	N	n	N	n	N
110																				
250	3	124	—	—	3	249														
500	2	249	—	—	3	124	—	—			3	233								
1 k	2	124	—	—	2	249	—	—	3	97	3	116	3	128	3	155	3	249		
2.5 k	1	199	1	249	2	99	2	124	2	155	2	187	2	205	2	249	3	99	3	124
5 k	1	99	1	124	1	199	1	249	2	77	2	93	2	102	2	124	2	199	2	249
10 k	0	199	0	249	1	99	1	124	1	155	1	187	1	205	1	249	2	99	2	124
25 k	0	79	0	99	0	159	0	199	0	249	1	74	1	82	1	99	1	159	1	199
50 k	0	39	0	49	0	79	0	99	0	124	0	149	0	164	1	49	1	79	1	99
100 k	0	19	0	24	0	39	0	49	0	62	0	74	0	82	0	99	0	159	0	199
250 k	0	7	0	9	0	15	0	19	0	24	0	29	0	32	0	39	0	63	0	79
500 k	0	3	0	4	0	7	0	9	—	—	0	14	—	—	0	19	0	31	0	39
1 M	0	1			0	3	0	4	—	—	—	—	—	—	0	9	0	15	0	19
2.5 M			0	0*2			0	1	—	—	0	2	—	—	0	3			0	7
5 M							0	0*2							0	1			0	3
7.5 M											0	0*2								

Space: Setting prohibited.

—: Can be set, but an error will occur.

Note 1. Supported by SCI11 only.

Note 2. Continuous transmission or reception is not possible. After transmitting/receiving one frame of data, there is an interval of a 1-bit period before starting transmitting/receiving the next frame of data. The output of the synchronization clock is stopped for a 1-bit period. For this reason, it takes 9 bits worth of time to transfer one frame (8 bits) of data, and the average transfer rate is 8/9 times the bit rate.

Table 26.17 Maximum Bit Rate with External Clock Input (Clock Synchronous Mode, Simple SPI Mode)

PCLK (MHz)	External Input Clock (MHz)	Maximum Bit Rate (Mbps)
8	1.3333	1.3333
10	1.6667	1.6667
12	2.0000	2.0000
14	2.3333	2.3333
16	2.6667	2.6667
18	3.0000	3.0000
20	3.3333	3.3333
25	4.1667	4.1667
30	5.0000	5.0000
33	5.5000	5.5000
40	6.6667	6.6667
Over 40*1	6.6667	6.6667

Note 1. Supported by SCI11 only.

Table 26.18 BRR Settings for Various Bit Rates (Smart Card Interface Mode, n = 0, S = 372)

Bit Rate (bps)	PCLK (MHz)	n	N	Error (%)
9600	7.1424	0	0	0.00
	10.00	0	1	30
	10.7136	0	1	25
	13.00	0	1	8.99
	14.2848	0	1	0.00
	16.00	0	1	12.01
	18.00	0	2	15.99
	20.00	0	2	6.66
	25.00	0	3	12.49
	30.00	0	3	5.01
	33.00	0	4	7.59
	40.00	0	5	–6.66
	64.00*1	0	8	–0.44
	80.00*1	0	10	1.82

Note 1. Supported by SCI11 only.

Table 26.19 Maximum Bit Rate for Each Operating Frequency (Smart Card Interface Mode, S = 32)

PCLK (MHz)	Maximum Bit Rate (bps)	n	N
10.00	156250	0	0
10.7136	167400	0	0
13.00	203125	0	0
16.00	250000	0	0
18.00	281250	0	0
20.00	312500	0	0
25.00	390625	0	0
30.00	468750	0	0
33.00	515625	0	0
40.00	625000	0	0
64.00	1000000	0	0
80.00	1250000	0	0

Note 1. Supported by SCI11 only.

Table 26.20 BRR Settings for Various Bit Rates (Simple I²C Mode)

Bit Rate (bps)	Operating Frequency PCLK (MHz)														
	8			10			16			20			25		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
10 k	0	24	0.0	0	31	–2.3	1	12	–3.8	1	15	–2.3	1	19	–2.3
25 k	0	9	0.0	0	12	–3.8	1	4	0.0	1	6	–10.7	1	7	–2.3
50 k	0	4	0.0	0	6	–10.7	1	2	–16.7	1	3	–21.9	1	3	–2.3
100 k	0	2	–16.7	0	3	–21.9	0	4	0.0	0	6	–10.7	1	1	–2.3
250 k	0	0	0.0	0	1	–37.5	0	1	0.0	0	2	–16.7	0	3	–21.9
350 k										0	1	–10.7	0	2	–25.6

Bit Rate (bps)	Operating Frequency PCLK (MHz)														
	30			33			40			64*1			80*1		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
10 k	1	23	–2.3	1	25	–0.8	0	124	0.00	1	49	0.0	1	62	–0.8
25 k	1	9	–6.3	1	10	–6.3	0	40	0.00	0	79	0.0	1	24	0.0
50 k	1	4	–6.3	1	5	–14.1	0	24	0.00	0	39	0.0	0	49	0.0
100 k	1	2	–21.9	1	2	–14.1	0	12	–3.85	0	19	0.0	0	24	0.0
250 k	0	3	–6.3	0	4	–17.5	0	4	0.00	0	7	0.0	0	9	0.0
350 k	0	2	–10.7	0	2	–1.8	0	3	–10.71	0	5	–4.8	0	6	2.0

Note 1. Supported by SCI11 only.

Table 26.21 Minimum Widths at High and Low Level for SCL at Various Bit Rates (Simple I²C Mode)

Bit Rate (bps)	Operating Frequency PCLK (MHz)											
	8			10			16			20		
	n	N	Min. Widths at High/Low Level for SCL (µs)	n	N	Min. Widths at High/Low Level for SCL (µs)	n	N	Min. Widths at High/Low Level for SCL (µs)	n	N	Min. Widths at High/Low Level for SCL (µs)
10 k	0	24	43.75/50.00	0	31	44.80/51.20	1	12	45.50/52.00	1	15	44.80/51.20
25 k	0	9	17.50/20.00	0	12	18.20/20.80	1	4	17.50/20.00	1	6	19.60/22.40
50 k	0	4	8.75/10.00	0	6	9.80/11.20	1	2	10.50/12.00	1	3	11.20/12.80
100 k	0	2	5.25/6.00	0	3	5.60/6.40	0	4	4.37/5.00	0	6	4.90/5.60
250 k	0	0	1.75/2.00	0	1	2.80/3.20	0	1	1.75/2.00	0	2	2.10/2.40
350 k										0	1	1.40/1.60

Bit Rate (bps)	Operating Frequency PCLK (MHz)											
	25			30			33			40		
	n	N	Min. Widths at High/Low Level for SCL (µs)	n	N	Min. Widths at High/Low Level for SCL (µs)	n	N	Min. Widths at High/Low Level for SCL (µs)	n	N	Min. Widths at High/Low Level for SCL (µs)
10 k	1	19	44.80/51.20	1	23	44.80/51.20	1	25	44.12/50.42	1	32	46.20/52.80
25 k	1	7	17.92/20.48	1	9	18.66/21.33	1	10	18.66/21.33	1	12	18.20/20.80
50 k	1	3	8.96/10.24	1	4	9.33/10.66	1	5	10.18/11.63	1	6	9.80/11.20
100 k	1	1	4.48/5.12	1	2	5.60/6.40	1	2	5.09/5.81	0	13	4.90/5.60
250 k	0	3	2.24/2.56	0	3	1.86/2.13	0	4	2.12/2.42	0	4	1.75/2.00
350 k	0	2	1.68/1.92	0	2	1.40/1.60	0	2	1.27/1.45	0	3	1.40/1.60

Bit Rate (bps)	Operating Frequency PCLK (MHz)					
	64*1			80*1		
	n	N	Min. Widths at High/Low Level for SCL (µs)	n	N	Min. Widths at High/Low Level for SCL (µs)
10 k	1	49	43.75/50.00	1	62	44.10/50.40
25 k	0	79	17.50/20.00	1	24	17.50/20.00
50 k	0	39	8.75/10.00	0	49	8.75/10.00
100 k	0	19	4.38/5.00	0	24	4.38/5.00
250 k	0	7	1.75/2.00	0	9	1.75/2.00
350 k	0	5	1.31/1.50	0	6	1.23/1.40

Note 1. Supported by SCI11 only.

26.2.12 Modulation Duty Register (MDDR)

Address(es): SCI1.MDDR 0008 A032h, SCI5.MDDR 0008 A0B2h, SCI6.MDDR 0008 A0D2h, SCI8.MDDR 0008 A112h, SCI9.MDDR 0008 A132h, SCI11.MDDR 000D 0012h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1

The MDDR register corrects the bit rate adjusted by the BRR register.
When the SEMR.BRME bit is set to 1, the bit rate generated by the on-chip baud rate generator is evenly corrected according to the settings of the MDDR register (M/256). The relationship between the MDDR register setting (M) and the bit rate (B) is given in Table 26.22.
The range of the value that can be set in the MDDR register is from 80h to FFh. A value other than these cannot be set.
The MDDR register is writable only when the TE and RE bits in the SCR register are 0.

Table 26.22 Relationship between MDDR Setting (M) and Bit Rate (B) When Bit Rate Modulation Function is Used

Mode	SEMR Settings		BRR Setting	Error
	BGDM Bit	ABCS Bit		
Asynchronous multi-processor communication	0	0	$N = \frac{PCLK \times 10^6}{64 \times 2^{2n-1} \times (256/M) \times B} - 1$	$Error\ (\%) = \{\frac{PCLK \times 10^6}{B \times 64 \times 2^{2n-1} \times (256/M) \times (N+1)} - 1\} \times 100$
	0	1	$N = \frac{PCLK \times 10^6}{32 \times 2^{2n-1} \times (256/M) \times B} - 1$	$Error\ (\%) = \{\frac{PCLK \times 10^6}{B \times 32 \times 2^{2n-1} \times (256/M) \times (N+1)} - 1\} \times 100$
	1	0		
	1	1	$N = \frac{PCLK \times 10^6}{16 \times 2^{2n-1} \times (256/M) \times B} - 1$	$Error\ (\%) = \{\frac{PCLK \times 10^6}{B \times 16 \times 2^{2n-1} \times (256/M) \times (N+1)} - 1\} \times 100$
Clock synchronous mode, simple SPI mode*1			$N = \frac{PCLK \times 10^6}{8 \times 2^{2n-1} \times (256/M) \times B} - 1$	
Smart card interface mode			$N = \frac{PCLK \times 10^6}{S \times 2^{2n+1} \times (256/M) \times B} - 1$	$Error\ (\%) = \{\frac{PCLK \times 10^6}{B \times S \times 2^{2n+1} \times (256/M) \times (N+1)} - 1\} \times 100$
Simple I^2C*2			$N = \frac{PCLK \times 10^6}{64 \times 2^{2n-1} \times (256/M) \times B} - 1$	

B: Bit rate (bps)
M: MDDR setting (128 ≤ MDDR ≤ 256)
N: BRR setting for baud rate generator (0 ≤ N ≤ 255)
PCLK: Operating frequency (MHz)
n and S: Determined by the settings of the SMR and SCMR registers as listed in Table 26.10 and Table 26.11, section 26.2.11, Bit Rate Register (BRR).

Note 1. Do not use this function in clock synchronous mode and in the highest speed settings in simple SPI mode (SMR.CKS[1:0] = 00b, SCR.CKE[1] = 0, and BRR = 0).
Note 2. Adjust the bit rate so that the widths at high and low level of the SCL output in simple I^2C mode satisfy the I^2C standard.

26.2.13 Serial Extended Mode Register (SEMR)

Address(es): SCI1.SEMR 0008 A027h, SCI5.SEMR 0008 A0A7h, SCI6.SEMR 0008 A0C7h, SCI8.SEMR 0008 A107h, SCI9.SEMR 0008 A127h, SCI11.SEMR 000D 0007h

	b7	b6	b5	b4	b3	b2	b1	b0
	RXDESEL	BGDM	NFEN	ABCS	—	BRME	—	ACS0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ACS0	Asynchronous Mode Clock Source Select	(Valid only in asynchronous mode) 0: External clock input 1: Logical AND of two compare matches output from TMR (valid for SCI5 and SCI6 only) Available compare match output varies per SCI channel.	R/W*1
b1	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b2	BRME	Bit Rate Modulation Enable	0: Bit rate modulation function is disabled. 1: Bit rate modulation function is enabled.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	ABCS	Asynchronous Mode Base Clock Select	(Valid only in asynchronous mode) 0: Selects 16 base clock cycles for 1-bit period. 1: Selects 8 base clock cycles for 1-bit period.	R/W*1
b5	NFEN	Digital Noise Filter Function Enable	(In asynchronous mode) 0: Noise cancellation function for the RXDn input signal is disabled. 1: Noise cancellation function for the RXDn input signal is enabled. (in simple I^2C mode) 0: Noise cancellation function for the SSCLn and SSDAn input signals is disabled. 1: Noise cancellation function for the SSCLn and SSDAn input signals is enabled. The NFEN bit should be 0 in any mode other than above.	R/W*1
b6	BGDM	Baud Rate Generator Double-Speed Mode Select	(Only valid the CKE[1] bit in SCR is 0 in asynchronous mode). 0: Baud rate generator outputs the clock with normal frequency. 1: Baud rate generator outputs the clock with doubled frequency.	R/W
b7	RXDESEL	Asynchronous Start Bit Edge Detection Select	(Valid only in asynchronous mode) 0: The low level on the RXDn pin is detected as the start bit. 1: A falling edge on the RXDn pin is detected as the start bit.	R/W*1

Note 1. Writable only when TE in SCR = 0 and RE in SCR = 0 (both serial transmission and reception are disabled).

The SEMR register is used to select a clock source for 1-bit period in asynchronous mode or a detection method of the start bit.

ACS0 Bit (Asynchronous Mode Clock Source Select)

Selects the clock source in the asynchronous mode.

The ACS0 bit is valid in asynchronous mode (SMR.CM bit = 0) and when an external clock input is selected (SCR.CKE[1:0] bits = 10b or 11b). This bit is used to select an external clock input or the logical AND of compare matches output from the internal TMR.

Set the ACS0 bit to 0 in other than asynchronous mode.

For SCI5 and SCI6, the TMOn output (n = 0 to 3) of TMR units 0 and 1 can be set as the serial transfer base clock. Refer to Table 26.23 for details.

These bits for the other SCI channels than SCI5 and SCI6 are reserved. The write values to these bits for other than SCI5 and SCI6 should be 0.

Table 26.23 Correspondence between SCI Channels and Compare Match Outputs

SCI	TMR	Compare Match Output
SCI5	Unit 0	TMO0, TMO1
SCI6	Unit 1	TMO2, TMO3

Figure 26.3 shows a setting example of when TMO0 and TMO1 in the TMR unit 0 are selected for output.

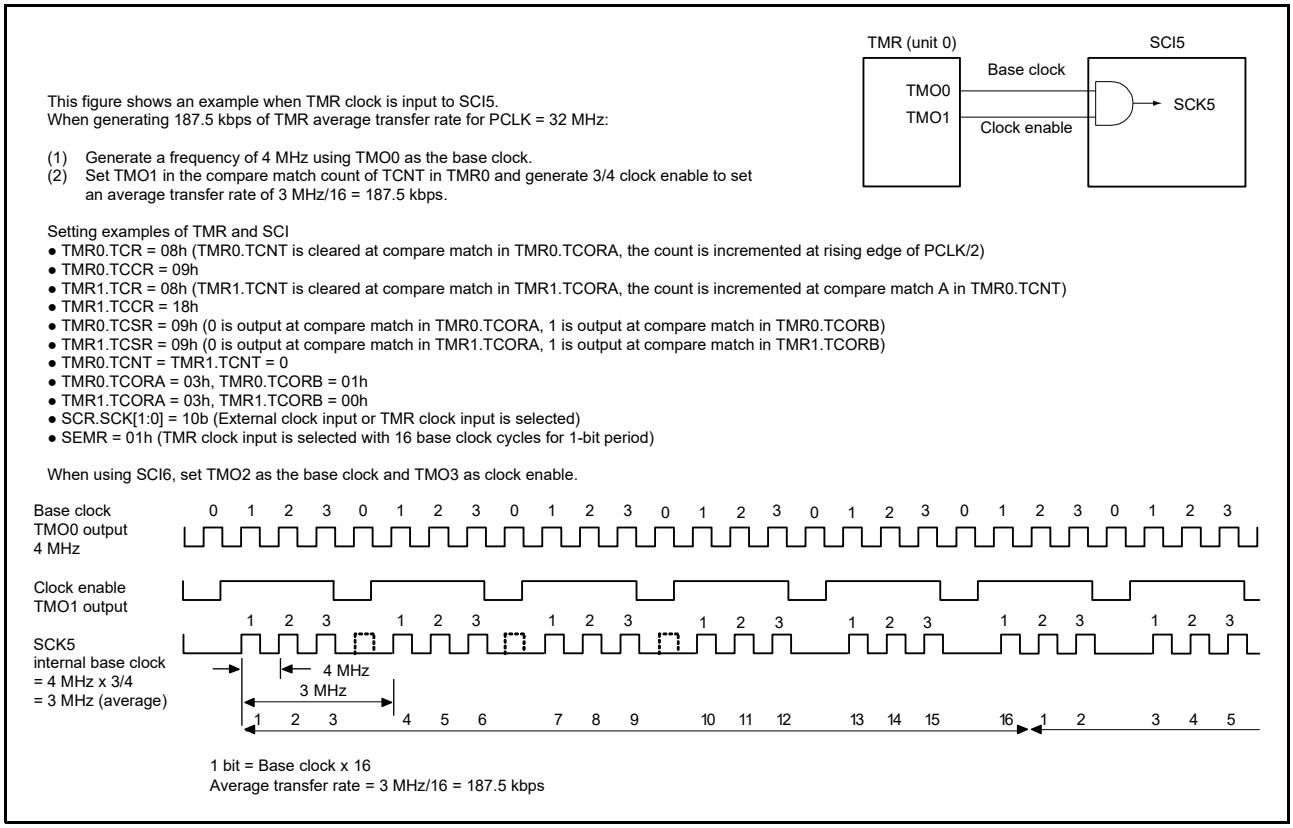


Figure 26.3 Example of Average Transfer Rate Setting When TMR Clock is Input

BRME bit (Bit Rate Modulation Enable)

Enables and disables the bit rate modulation function. The bit rate generated by on-chip baud rate generator is evenly corrected when this function is enabled.

NFEN Bit (Digital Noise Filter Function Enable)

This bit enables or disables the digital noise filter function.

When the function is enabled, noise cancellation is applied to the RXDn input signal in asynchronous mode, and noise cancellation is applied to the SSDAn and SSCLn input signals in simple I^2C mode.
In any mode other than above, set the NFEN bit to 0 to disable the digital noise filter function.
When the function is disabled, input signals are transferred as is, as internal signals.

BGDM bit (Baud Rate Generator Double-Speed Mode Select)

Selects the cycle of output clock for the baud rate generator.
This bit is valid when the on-chip baud rate generator is selected as the clock source (SCR.CKE[1] = 0) in asynchronous mode (SMR.CM = 0). For the clock output from the baud rate generator, either normal or doubled frequency can be selected. The base clock is generated by the clock output from the baud rate generator. When the BGDM bit is set to 1, the base clock cycle is halved and the bit rate is doubled.
Set this bit to 0 in modes other than asynchronous mode.

RXDESEL Bit (Asynchronous Start Bit Edge Detection Select)

Selects the detection method of the start bit for reception in asynchronous mode. When a break occurs, data receiving operation depends on the settings of this bit. Set this bit to 1 when reception should be stopped while a break occurs or when reception should be started without retaining the RXDn pin input at high level for the period of one data frame or longer after completion of the break.
Set this bit to 0 in modes other than asynchronous mode.

26.2.14 Noise Filter Setting Register (SNFR)

Address(es): SCI1.SNFR 0008 A028h, SCI5.SNFR 0008 A0A8h, SCI6.SNFR 0008 A0C8h, SCI8.SNFR 0008 A108h, SCI9.SNFR 0008 A128h, SCI11.SNFR 000D 0008h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	NFCS[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	NFCS[2:0]	Noise Filter Clock Select	In asynchronous mode, the standard setting for the base clock is as follows. b2 b0 0 0 0: The clock signal divided by 1 is used with the noise filter. In simple I2C mode, the standard settings for the clock source of the on-chip baud rate generator selected by the SMR.CKS[1:0] bits are given below. b2 b0 0 0 1: The clock signal divided by 1 is used with the noise filter. 0 1 0: The clock signal divided by 2 is used with the noise filter. 0 1 1: The clock signal divided by 4 is used with the noise filter. 1 0 0: The clock signal divided by 8 is used with the noise filter. Settings other than above are prohibited.	R/W*1
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Writing to these bits is only possible when the RE and TE bits in the SCR are 0 (serial reception and transmission disabled).

NFCS[2:0] Bits (Noise Filter Clock Select)

These bits select the sampling clock for the digital noise filter. To use the noise filter in asynchronous mode, set these bits to 000b. In simple I2C mode, set the bits to a value in the range from 001b to 100b.

26.2.15 I²C Mode Register 1 (SIMR1)

Address(es): SCI1.SIMR1 0008 A029h, SCI5.SIMR1 0008 A0A9h, SCI6.SIMR1 0008 A0C9h, SCI8.SIMR1 0008 A109h, SCI9.SIMR1 0008 A129h, SCI11.SIMR1 000D 0009h

	b7	b6	b5	b4	b3	b2	b1	b0
	IICDL[4:0]					—	—	IICM
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	IICM	Simple I²C Mode Select	SMIF IICM 0 0: Asynchronous mode, Multi-processor mode, Clock synchronous mode (in asynchronous mode, synchronous, or simple SPI mode) 0 1: Simple I²C mode 1 0: Smart card interface mode 1 1: Setting prohibited.	R/W*1
b2, b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7 to b3	IICDL[4:0]	SSDA Output Delay Select	(Cycles below are of the clock signal from the on-chip baud rate generator.) b7 b3 0 0 0 0 0: No output delay 0 0 0 0 1: 0 to 1 cycle 0 0 0 1 0: 1 to 2 cycles 0 0 0 1 1: 2 to 3 cycles 0 0 1 0 0: 3 to 4 cycles 0 0 1 0 1: 4 to 5 cycles : : 1 1 1 1 0: 29 to 30 cycles 1 1 1 1 1: 30 to 31 cycles	R/W*1

Note 1. Writing to these bits is only possible when the RE and TE bits in the SCR are 0 (both serial transmission and reception are disabled).

SIMR1 is used to select simple I²C mode and the number of delay stages for the SSDA output.

IICM Bit (Simple I²C Mode Select)

In conjunction with the SMIF bit in the SCMR register, this bit selects the operating mode.

IICDL[4:0] Bits (SSDA Output Delay Select)

These bits are used to set a delay for output on the SSDAn pin relative to the falling edge of the output on the SSCLn pin. The available delay settings range from no delay to 31 cycles, with the clock signal from the on-chip baud rate generator as the base. The signal obtained by frequency-dividing PCLK by the divisor set in the SMR.CKS[1:0] bits is supplied as the clock signal from the on-chip baud rate generator. Set these bits to 00000b unless operation is in simple I²C mode. In simple I²C mode, set the bits to a value in the range from 00001b to 11111b.

26.2.16 I²C Mode Register 2 (SIMR2)

Address(es): SCI1.SIMR2 0008 A02Ah, SCI5.SIMR2 0008 A0AAh, SCI6.SIMR2 0008 A0CAh, SCI8.SIMR2 0008 A10Ah, SCI9.SIMR2 0008 A12Ah, SCI11.SIMR2 000D 000Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	IICACKT	—	—	—	IICCSC	IICINTM
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	IICINTM	I²C Interrupt Mode Select	0: Use ACK/NACK interrupts. 1: Use reception and transmission interrupts.	R/W*1
b1	IICCSC	Clock Synchronization	0: No synchronization with the clock signal 1: Synchronization with the clock signal	R/W*1
b4 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5	IICACKT	ACK Transmission Data	0: ACK transmission 1: NACK transmission and reception of ACK/NACK	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Writing to these bits is only possible when the RE and TE bits in the SCR are 0 (serial reception and transmission disabled).

SIMR2 is used to select how reception and transmission are controlled in simple I²C mode.

IICINTM Bit (I²C Interrupt Mode Select)

This bit selects the sources of interrupt requests in simple I²C mode.

IICCSC Bit (Clock Synchronization)

Set the IICCSC bit to 1 if the internally generated SSCLn clock signal is to be synchronized when the SSCLn pin has been placed at the low level in the case of a wait inserted by the other device, etc.

The SSCLn clock signal is not synchronized if the IICCSC bit is 0. The SSCLn clock signal is generated in accord with the rate selected in the BRR regardless of the level being input on the SSCLn pin.

Set the IICCSC bit to 1 except during debugging.

IICACKT Bit (ACK Transmission Data)

Transmitted data contains ACK bits. Set this bit to 1 when ACK and NACK bits are received.

26.2.17 I²C Mode Register 3 (SIMR3)

Address(es): SCI1.SIMR3 0008 A02Bh, SCI5.SIMR3 0008 A0ABh, SCI6.SIMR3 0008 A0CBh, SCI8.SIMR3 0008 A10Bh, SCI9.SIMR3 0008 A12Bh, SCI11.SIMR3 000D 000Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	IICSCLS[1:0]		IICSDAS[1:0]		IICSTIF	IICSTP REQ	IICRST AREQ	IICSTA REQ
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	IICSTAREQ	Start Condition Generation	0: A start condition is not generated. 1: A start condition is generated.*1, *3, *4, *5	R/W
b1	IICRSTAREQ	Restart Condition Generation	0: A restart condition is not generated. 1: A restart condition is generated.*2, *3, *4, *5	R/W
b2	IICSTPREQ	Stop Condition Generation	0: A stop condition is not generated. 1: A stop condition is generated.*2, *3, *4, *5	R/W
b3	IICSTIF	Issuing of Start, Restart, or Stop Condition Completed Flag	0: There are no requests for generating conditions or a condition is being generated. 1: A start, restart, or stop condition is completely generated.	R/W
b5, b4	IICSDAS[1:0]	SSDA Output Select	b5 b4 0 0: Serial data output 0 1: Generate a start, restart, or stop condition. 1 0: Output the low level on the SSDAn pin. 1 1: Place the SSDAn pin in the high-impedance state.	R/W
b7, b6	IICSCLS[1:0]	SSCL Output Select	b7 b6 0 0: Serial clock output 0 1: Generate a start, restart, or stop condition. 1 0: Output the low level on the SSCLn pin. 1 1: Place the SSCLn pin in the high-impedance state.	R/W

Note 1. Generate a start condition only when the SSCLn and SSDAn pins are both high (the corresponding bits in the corresponding PIDR registers are 1).
Note 2. Generate a restart or stop condition only when the SSCLn pin is low (the corresponding bit in the PIDR register is 0).
Note 3. Do not set more than one from among the IICSTAREQ, IICRSTAREQ, and IICSTPREQ bits to 1 at a given time.
Note 4. Execute the generation of a condition after the value of the IICSTIF flag is 0.
Note 5. Do not write 0 to this bit while it is 1. Generation of a condition is suspended by writing 0 to this bit while it is 1.

SIMR3 is used to control the simple I²C mode start and stop conditions, and to hold the SSDAn and SSCLn pins at fixed levels.

IICSTAREQ Bit (Start Condition Generation)

When a start condition is to be generated, set both the IICSDAS[1:0] and IICSCLS[1:0] bits to 01b as well as setting the IICSTAREQ bit to 1.

[Setting condition]

- Writing 1 to the bit

[Clearing condition]

- Completion of generation of the start condition

IICRSTAREQ Bit (Restart Condition Generation)

When a restart condition is to be generated, set both the IICSDAS[1:0] and IICSCLS[1:0] bits to 01b as well as setting the IICRSTAREQ bit to 1.

[Setting condition]

- Writing 1 to the bit

[Clearing condition]

- Completion of generation of the restart condition

IICSTPREQ Bit (Stop Condition Generation)

When a stop condition is to be generated, set both the IICSDAS[1:0] and IICSCLS[1:0] bits to 01b as well as setting the IICSTPREQ bit to 1.

[Setting condition]

- Writing 1 to the bit

[Clearing condition]

- Completion of generation of the stop condition

IICSTIF Flag (Issuing of Start, Restart, or Stop Condition Completed Flag)

After generating a condition, this bit indicates that the generation is completed. When using the IICSTAREQ, IICRSTAREQ, or IICSTPREQ bit to cause generation of a condition, do so after setting the IICSTIF flag to 0.

When the IICSTIF flag is 1 while an interrupt request is enabled by setting the SCR.TEIE bit, an STI request is output.

[Setting condition]

- Completion of the generation of a start, restart, or stop condition (however, in cases where this conflicts with any of the conditions for the flag becoming 0 listed below, the other condition takes precedence)

[Clearing conditions]

- Writing 0 to the bit (confirm that the IICSTIF flag is 0 before doing so)
- Writing 0 to the SIMR1.IICM bit (when operation is not in simple I^2C mode)
- Writing 0 to the SCR.TE bit

IICSDAS[1:0] Bits (SSDA Output Select)

These bits control output from the SSDAn pin.

Set the IICSDAS[1:0] and IICSCLS[1:0] bits to the same value during normal operations.

IICSCLS[1:0] Bits (SSCL Output Select)

These bits control output from the SSCLn pin.

Set the IICSCLS[1:0] and IICSDAS[1:0] bits to the same value during normal operations.

26.2.18 I²C Status Register (SISR)

Address(es): SCI1.SISR 0008 A02Ch, SCI5.SISR 0008 A0ACh, SCI6.SISR 0008 A0CCh, SCI8.SISR 0008 A10Ch, SCI9.SISR 0008 A12Ch, SCI11.SISR 000D 000Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	IICACKR
Value after reset:	0	0	x	x	0	x	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b0	IICACKR	ACK Reception Data Flag	0: ACK received 1: NACK received	R/W*1
b1	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b2	—	Reserved	The read value is undefined.	R
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b5, b4	—	Reserved	The read value is undefined.	R
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only 0 can be written to this bit, to clear the flag.

SISR is used to monitor state in relation to simple I²C mode.

IICACKR Flag (ACK Reception Data Flag)

Received ACK and NACK bits can be read from this bit.

The IICACKR flag is updated at the rising of SSCLn clock for the ACK/NACK receiving bit.

26.2.19 SPI Mode Register (SPMR)

Address(es): SCI1.SPMR 0008 A02Dh, SCI5.SPMR 0008 A0ADh, SCI6.SPMR 0008 A0CDh, SCI8.SPMR 0008 A10Dh, SCI9.SPMR 0008 A12Dh, SCI11.SPMR 000D 000Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	CKPH	CKPOL	—	MFF	—	MSS	CTSE	SSE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SSE	SSn# Pin Function Enable	0: SSn# pin function is disabled. 1: SSn# pin function is enabled.	R/W*1
b1	CTSE	CTS Enable	0: CTS function is disabled (RTS output function is enabled). 1: CTS function is enabled.	R/W*1
b2	MSS	Master Slave Select	0: Transmission is through the TXDn pin and reception is through the RXDn pin (master mode). 1: Reception is through the TXDn pin and transmission is through the RXDn pin (slave mode).	R/W*1
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	MFF	Mode Fault Flag	0: No mode fault error 1: Mode fault error	R/W*2
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	CKPOL	Clock Polarity Select	0: Clock polarity is not inverted. 1: Clock polarity is inverted.	R/W*1
b7	CKPH	Clock Phase Select	0: Clock is not delayed. 1: Clock is delayed.	R/W*1

Note 1. Writing to these bits is only possible when the RE and TE bits in the SCR are 0 (both serial transmission and reception are disabled).
Note 2. Only 0 can be written to these bits, which clears the flag.

SPMR is used to select the extension settings in asynchronous and clock synchronous modes.

SSE Bit (SSn# Pin Function Enable)

Set this bit to 1 if the SSn# pin is to be used in control of transmission and reception (in simple SPI mode). Set this bit to 0 in any other mode. Furthermore, even for usage in simple SPI mode, the SSn# pin on the master side is not required to control reception and transmission when master mode (SCR.CKE[1:0] = 00b and MSS = 0) is selected and there is a single master, so the setting for the SSE bit is 0. Do not set both the SSE and CTSE bits to enabled (even if this setting is made, operation is the same as that when these bits are set to 0).

CTSE Bit (CTS Enable)

Set this bit to 1 if the SSn# pin is to be used for inputting of the CTS control signal to control of transmission and reception. The RTS signal is output when this bit is set to 0. Set this bit to 0 in smart card interface mode, simple SPI mode, and simple I^2C mode. Do not set both the CTSE and SSE bits to enabled (even if this setting is made, operation is the same as that when these bits are set to 0).

MSS Bit (Master Slave Select)

This bit selects between master and slave operation in simple SPI mode. The functions of the TXDn and RXDn pins are reversed when the MSS bit is set to 1, so that data is received through the TXDn pin and transmitted through the RXDn pin.
Set this bit to 0 in modes other than simple SPI mode.

MFF Flag (Mode Fault Flag)

This bit indicates mode fault errors.
In a multi-master configuration, determine the mode fault error occurrence by reading the MFF flag.
[Setting condition]

- Input on the SSn# pin being at the low level during master operation in simple SPI mode (SSE bit = 1 and MSS bit = 0)

[Clearing condition]

- Writing 0 to the bit after it was read as 1

CKPOL Bit (Clock Polarity Select)

This bit selects the polarity of the clock signal output through the SCKn pin. Refer to Figure 26.55 for details.
Set the bit to 0 in other than simple SPI mode and clock synchronous mode.

CKPH Bit (Clock Phase Select)

This bit selects the phase of the clock signal output through the SCKn pin. Refer to Figure 26.55 for details.
Set the bit to 0 in other than simple SPI mode and clock synchronous mode.

26.3 Operation in Asynchronous Mode

Figure 26.4 shows the general format for asynchronous serial communications.
One frame consists of a start bit (low level), transmit/receive data, a parity bit, and stop bits (high level).
In asynchronous serial communications, the communications line is usually held in the mark state (high level).
The SCI monitors the communications line. When the SCI detects a low, it regards that as a start bit and starts serial communication.
Inside the SCI, the transmitter and receiver are independent units, enabling full-duplex communications. Both the transmitter and the receiver also have a double-buffered structure, so that data can be read or written during transmission or reception, enabling continuous data transmission and reception.

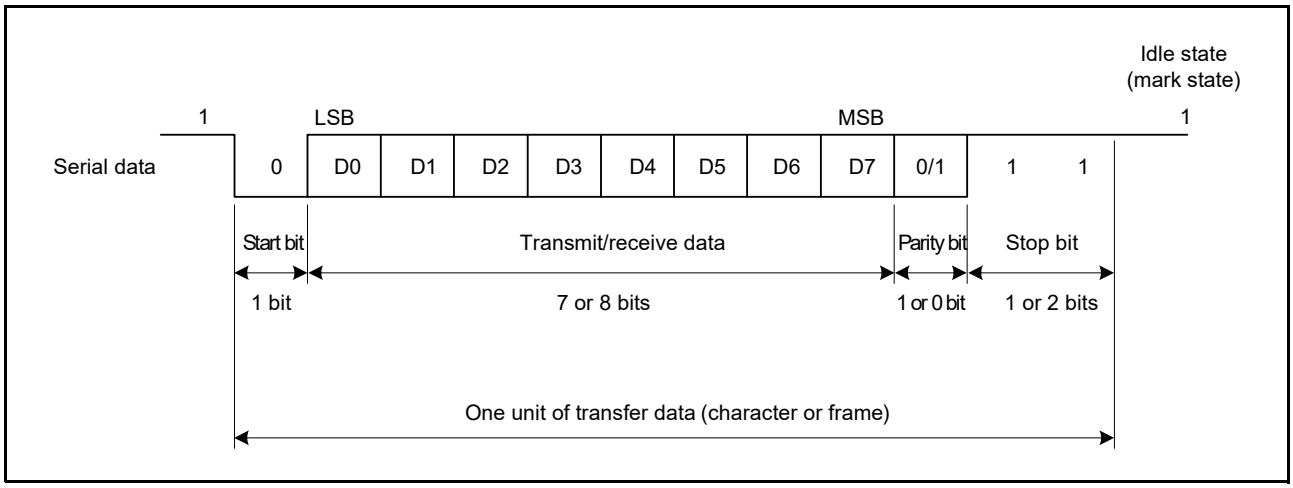


Figure 26.4 Data Format in Asynchronous Serial Communications (Example with 8-Bit Data, Parity, 2 Stop Bits)

26.3.1 Serial Data Transfer Format

Table 26.24 lists the serial data transfer formats that can be used in asynchronous mode.
Any of 18 transfer formats can be selected according to the SMR and SCMR setting. For details of multi-processor function, refer to section 26.4, Multi-Processor Communications Function.

Table 26.24 Serial Transfer Formats (Asynchronous Mode)

SCMR Setting	SMR Setting				Serial Transfer Format and Frame Length
CHR1	CHR	PE	MP	STOP	1 2 3 4 5 6 7 8 9 10 11 12 13
0	0	0	0	0	S 9-bit data STOP
0	0	0	0	1	S 9-bit data STOP STOP
0	0	1	0	0	S 9-bit data P STOP
0	0	1	0	1	S 9-bit data P STOP STOP
1	0	0	0	0	S 8-bit data STOP
1	0	0	0	1	S 8-bit data STOP STOP
1	0	1	0	0	S 8-bit data P STOP
1	0	1	0	1	S 8-bit data P STOP STOP
1	1	0	0	0	S 7-bit data STOP
1	1	0	0	1	S 7-bit data STOP STOP
1	1	1	0	0	S 7-bit data P STOP
1	1	1	0	1	S 7-bit data P STOP STOP
0	0	—	1	0	S 9-bit data MPB STOP
0	0	—	1	1	S 9-bit data MPB STOP STOP
1	0	—	1	0	S 8-bit data MPB STOP
1	0	—	1	1	S 8-bit data MPB STOP STOP
1	1	—	1	0	S 7-bit data MPB STOP
1	1	—	1	1	S 7-bit data MPB STOP STOP

S: Start bit
STOP: Stop bit
P: Parity bit
MPB: Multi-processor bit

26.3.2 Receive Data Sampling Timing and Reception Margin in Asynchronous Mode

In asynchronous mode, the SCI operates on a base clock with a frequency of 16 times*1 the bit rate.
In reception, the SCI samples the falling edge of the start bit using the base clock, and performs internal synchronization. Since receive data is sampled at the rising edge of the 8th pulse*1 of the base clock, data is latched at the middle of each bit, as shown in Figure 26.5. Thus the reception margin in asynchronous mode is determined by formula (1) below.

$$M = \left| (0.5 - \frac{1}{2N}) - (L - 0.5)\ F - \frac{D - 0.5}{N}\ (1 + F) \right| \times 100\ [\%] \cdots \text{Formula (1)}$$

M: Reception margin
N: Ratio of bit rate to clock (N = 16 when ABCS in SEMR = 0, N = 8 when ABCS in SEMR = 1)
D: Duty cycle of clock (D = 0.5 to 1.0)
L: Frame length (L = 9 to 13)
F: Absolute value of clock frequency deviation

Assuming values of F = 0 and D = 0.5 in formula (1), the reception margin is determined by the formula below.

M = {0.5 - 1/(2 × 16)} × 100 (%) = 46.875%

However, this is only the computed value, and a margin of 20% to 30% should be allowed in system design.

Note 1. This is an example when the ABCS bit in the SEMR register is 0. When the ABCS bit is 1, a frequency of 8 times the bit rate is used as a base clock and receive data is sampled at the rising edge of the 4th pulse of the base clock.

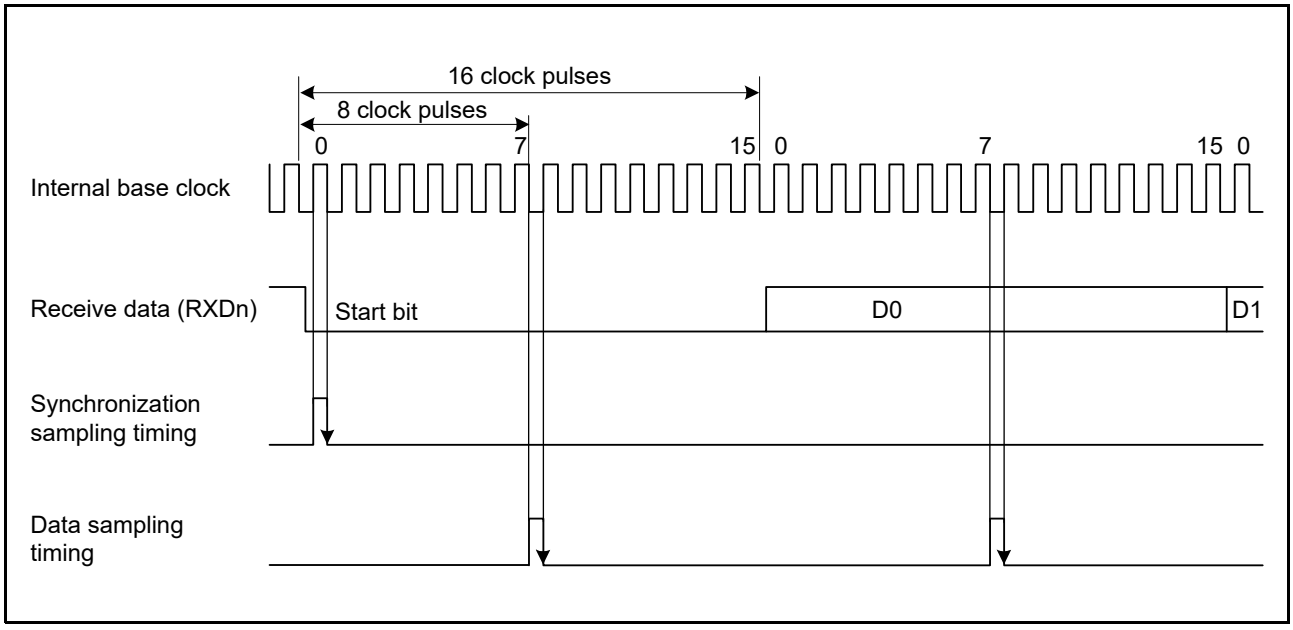


Figure 26.5 Receive Data Sampling Timing in Asynchronous Mode

26.3.3 Clock

Either an internal clock generated by the on-chip baud rate generator or an external clock input to the SCKn pin can be selected as the SCI's transfer clock, according to the setting of the CM bit in the SMR register and the CKE[1:0] bits in the SCR register.

When an external clock is input to the SCKn pin, the clock frequency should be 16 times the bit rate (when SEMR.ABCS bit = 0) and 8 times the bit rate (when SEMR.ABCS bit = 1). In addition, when an external clock is specified, the base clock of TMR0 and TMR1 can be selected by the SCIn.SEMR.ACS0 bit (n = 5, 6).

When the SCI is operated on an internal clock, the clock can be output from the SCKn pin. The frequency of the clock output in this case is equal to the bit rate, and the phase is such that the rising edge of the clock is in the middle of the transmit data, as shown in Figure 26.6.

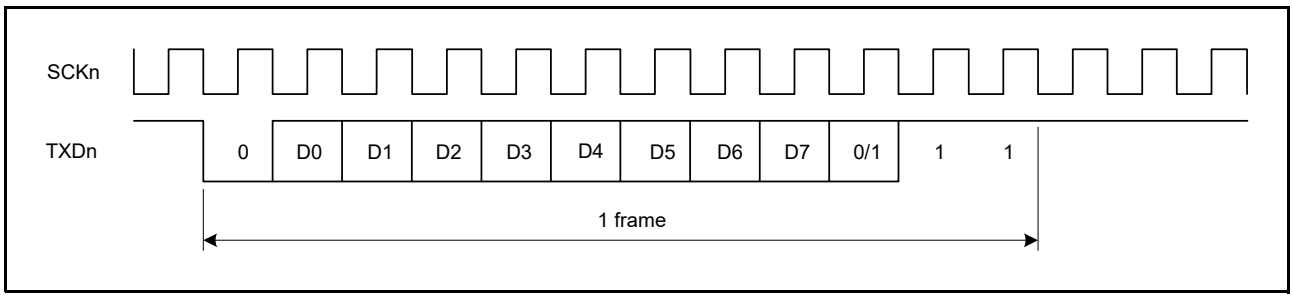


Figure 26.6 Phase Relationship between Output Clock and Transmit Data (Asynchronous Mode: SMR.CHR = 0, PE = 1, MP = 0, STOP = 1)

26.3.4 Double-Speed Mode

The output clock frequency of the on-chip baud rate generator is doubled by setting the SEMR.BGDM bit to 1, enabling high-speed communication at a doubled bit rate. If the SEMR.ABCS bit is set to 1 under the above condition, the number of base clock cycles changes from 16 to 8, so the bit rate becomes four times faster than the initial state.

As shown by Formula (1) in section 26.3.2, Receive Data Sampling Timing and Reception Margin in Asynchronous Mode, setting the SEMR.ABCS bit to 1 changes the number of cycles to 8, and the sampling interval becomes longer. This causes the reception margin to decrease. Therefore, setting the SEMR.BGDM bit to 1 and the SEMR.ABCS bit to 0 is recommended instead of setting the SEMR.BGDM bit to 0 and the SEMR.ABCS bit to 1 for high-speed operation at a doubled bit rate.

26.3.5 CTS and RTS Functions

The CTS function is the use of input on the CTSn# pin in transmission control. Setting the SPMR.CTSE bit to 1 enables the CTS function. When the CTS function is enabled, placing the low level on the CTSn# pin causes transmission to start.
Applying the high level to the CTS# pin while transmission is in progress does not affect transmission of the current frame, which continues.
In the RTS function, by using the function of output on the RTSn# pin, a low level is output when reception becomes possible. Conditions for output of the low and high level are shown below.

[Conditions for low-level output]
When the following conditions are all satisfied

- The SCR.RE bit is 1
- Reception is not in progress
- There are no received data yet to be read
- The ORER, FER, and PER flags in the SSR are all 0

[Condition for high-level output]
When the conditions for low-level output are not satisfied

Note that either one of CTS and RTS can be selected.

26.3.6 SCI Initialization (Asynchronous Mode)

Before transmitting and receiving data, start by writing the initial value 00h to the SCR register and then continue through the procedure for SCI given in Figure 26.7. Whenever the operating mode or transfer format is changed, the SCR register must be initialized before the change is made.

When the external clock is used in asynchronous mode, ensure that the clock signal is supplied even during initialization.

Note that setting the SCR.RE bit to 0 initializes neither the ORER, FER, PER, and RDRF flags in the SSR register nor registers RDR, RDRH, and RDRL.

Moreover, note that changing the value of the SCR.TE bit from 1 to 0 or 0 to 1 while the SCR.TIE bit is 1 leads to the generation of a transmit data empty interrupt (TXI) request.

In addition, note that setting bits TIE, TE, and TEIE in the SCR register to 1 simultaneously leads to the generation of a transmit end interrupt (TEI) request before the generation of a TXI interrupt request.

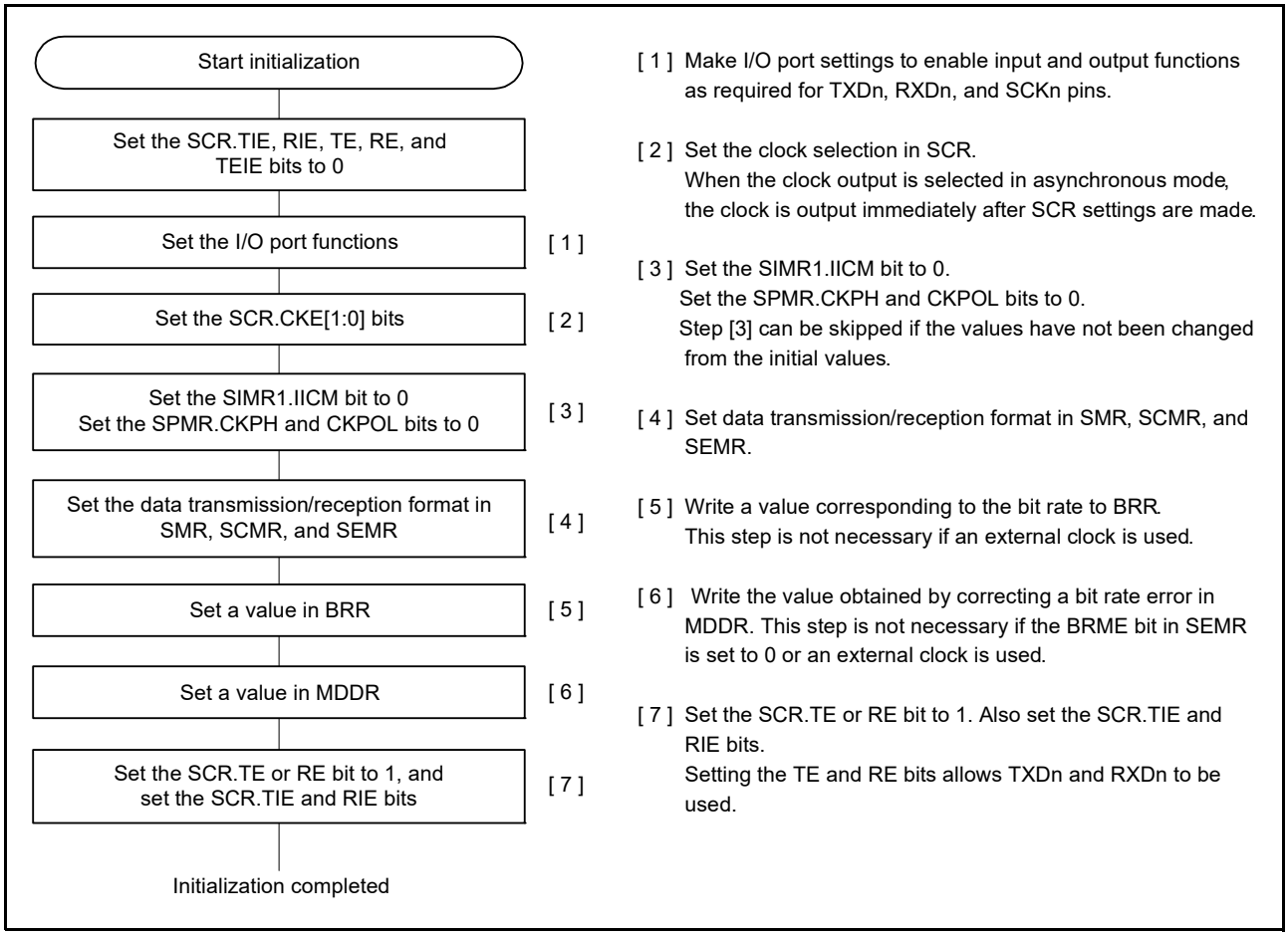


Figure 26.7 Sample SCI Initialization Flowchart (Asynchronous Mode)

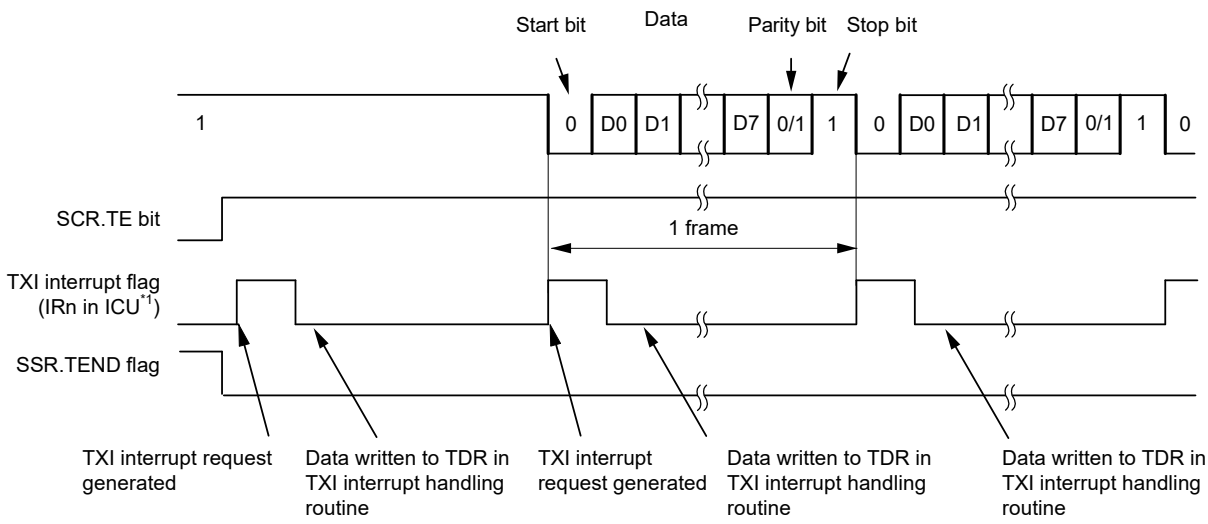
26.3.7 Serial Data Transmission (Asynchronous Mode)

Figure 26.8 to Figure 26.10 show an example of the operation for serial transmission in asynchronous mode.
In serial transmission, the SCI operates as described below.

1. The SCI transfers data from the TDR register*1 to the TSR register when data is written to the TDR register*1 in the TXI interrupt handling routine. The TXI interrupt request at the beginning of transmission is generated when the SCR.TE bit is set to 1 after the SCR.TIE bit is set to 1 or when these 2 bits are set to 1 simultaneously by a single instruction.
2. Transmission starts after the SPMR.CTSE bit is set to 0 (CTS function is disabled) and a low level on the CTSn# pin causes data transfer from the TDR register*1 to the TSR register. If the SCR.TIE bit is 1 at this time, a TXI interrupt request is generated. Continuous transmission is obtainable by writing the next transmit data to the TDR register*1 in the TXI interrupt handling routine before transmission of the current transmit data is completed. When TEI interrupt requests are in use, set the SCR.TIE bit to 0 (a TXI interrupt request is disabled) and the SCR.TEIE bit to 1 (a TEI interrupt request is enabled) after the last of the data to be transmitted are written to the TDR register*1, *2 from the handling routine for TXI requests.
3. Data is sent from the TXDn pin in the following order: start bit, transmit data, parity bit or multi-processor bit (may be omitted depending on the format), and stop bit.
4. The SCI checks for updating of (writing to) the TDR register*3 at the time of stop bit output.
5. When the TDR register*3 is updated, setting of the SPMR.CTSE bit to 0 (CTS function is disabled) or a low level input on the CTSn# pin cause the next transfer of the next transmit data from the TDR register*1 to the TSR register and sending of the stop bit, after which serial transmission of the next frame starts.
6. If the TDR register*3 is not updated, the SSR.TEND flag is set to 1, the stop bit is sent, and then the mark state is entered in which 1 is output. If the SCR.TEIE bit is 1 at this time, the SSR.TEND flag is set to 1 and a TEI interrupt request is generated.

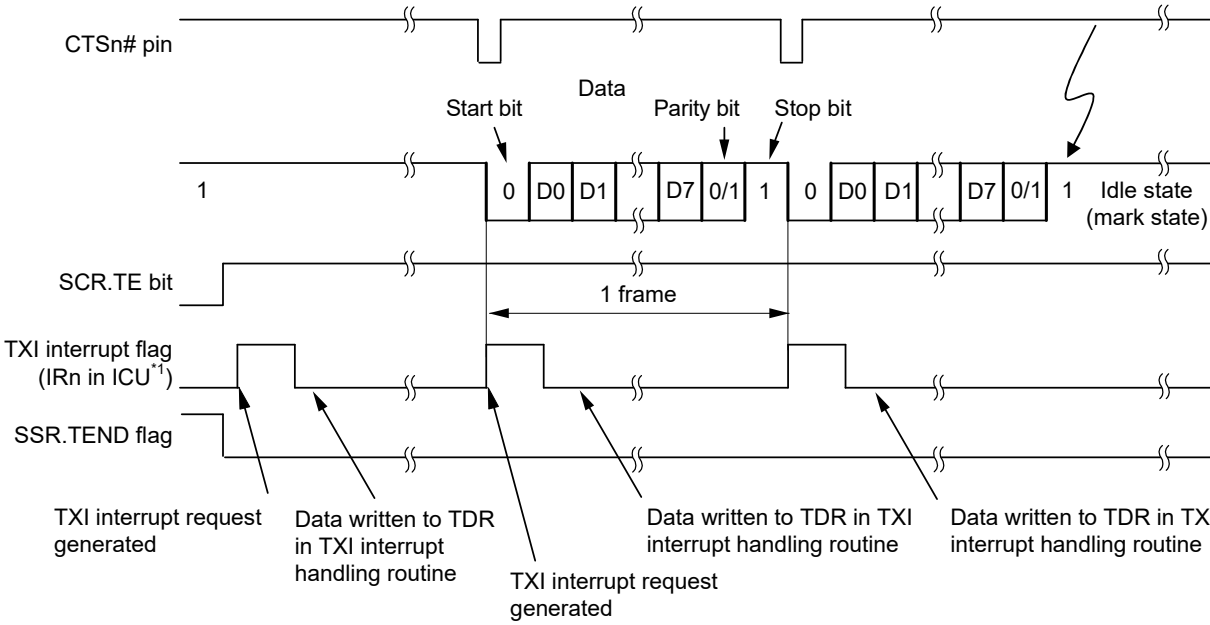
Note 1. Write data not to the TDR register but to the TDRH and TDRL registers when 9-bit data length is selected.
Note 2. Write data in the order from the TDRH register to the TDRL register when 9-bit data length is selected.
Note 3. The SCI checks for updating of the TDRL register only and does not check for updating of the TDRH register when 9-bit data length is selected.

Figure 26.11 shows a sample flowchart for serial transmission in asynchronous mode.



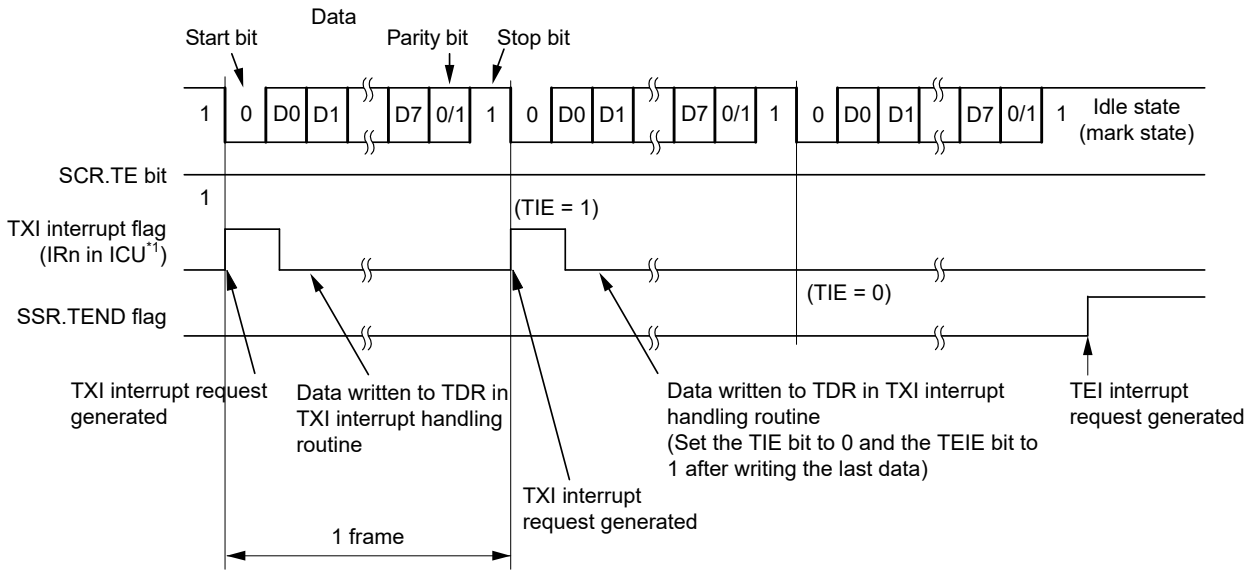
Note 1. Refer to the Interrupt Controller section for details on the corresponding interrupt vector number.

Figure 26.8 Example of Operation for Serial Transmission in Asynchronous Mode (1) (with 8-Bit Data, Parity, 1 Stop Bit, CTS Function Not Used, at the Beginning of Transmission)



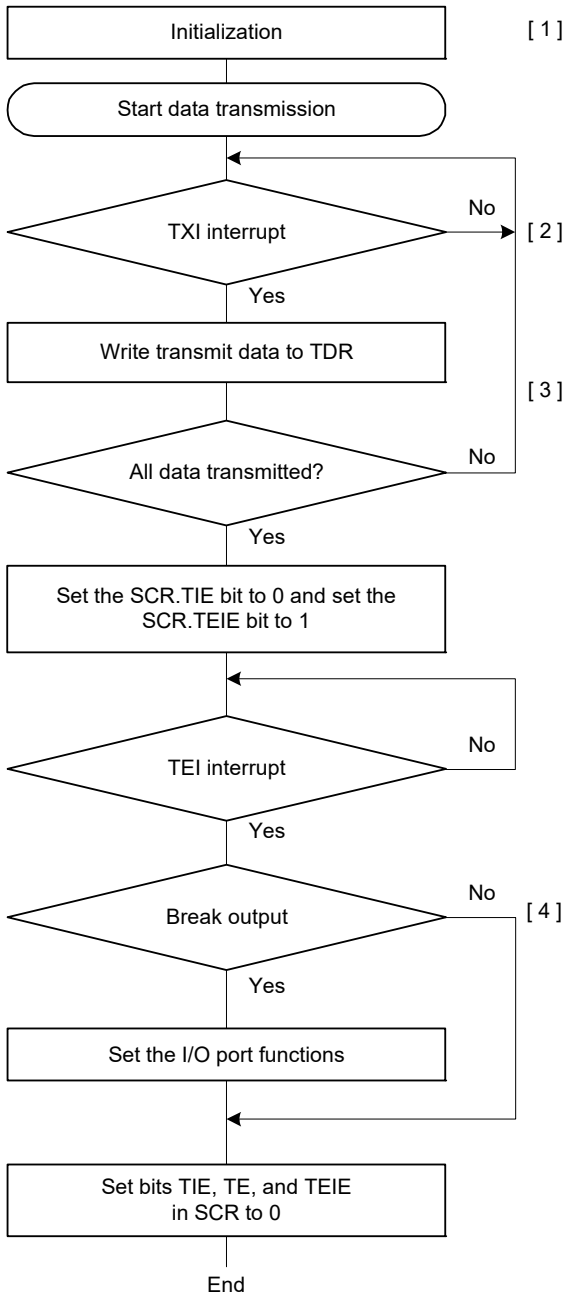
Note 1. Refer to the Interrupt Controller section for details on the corresponding interrupt vector number.

Figure 26.9 Example of Operation for Serial Transmission in Asynchronous Mode (2) (with 8-Bit Data, Parity, 1 Stop Bit, CTS Function Used, at the Beginning of Transmission)



Note 1. Refer to the Interrupt Controller section for details on the corresponding interrupt vector number.

Figure 26.10 Example of Operation for Serial Transmission in Asynchronous Mode (3) (with 8-Bit Data, Parity, 1 Stop Bit, CTS Function Not Used, from the Middle of Transmission until Transmission Completion)



[1] SCI initialization:
Set data transmission.
After the TE bit in SCR is set to 1, 1 is output for a frame, and transmission is enabled.

[2] Transmit data write to TDR by a TXI interrupt request:
When transmit data is transferred from TDR to TSR, a transmit data empty interrupt (TXI) request is generated.
Write transmit data to TDR once in the TXI interrupt handling routine.

[3] Serial transmission continuation procedure:
To continue serial transmission, write transmit data to TDR once using a TXI interrupt request.
Transmit data can also be written to TDR by activating the DTC.
When TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted are written to the TDR

[4] Break output at the end of serial transmission:
To output a break in serial transmission, set the I/O port function corresponding to the TXDn pin (corresponding to output of the low level), and after switching the TXDn pin to the general I/O port function, set the TE bit in the SCR to 0.

Note: The TDR register becomes the TDRH and TDRL registers when 9-bit data length is selected. Write data in the order from TDRH to TDRL.

Figure 26.11 Example of Serial Transmission Flowchart in Asynchronous Mode

26.3.8 Serial Data Reception (Asynchronous Mode)

Figure 26.12 and Figure 26.13 show an example of the operation for serial data reception in asynchronous mode. In serial data reception, the SCI operates as described below.

1. When the value of the SCR.RE bit becomes 1, the output signal on the RTSn# pin goes to the low level.
2. When the SCI monitors the communications line and detects a start bit, it performs internal synchronization, stores receive data in the RSR register, and checks the parity bit and stop bit.
3. If an overrun error occurs, the SSR.ORER flag is set to 1. If the SCR.RIE bit is 1 at this time, an ERI interrupt request is generated. Receive data is not transferred to the RDR register*1.
4. If a parity error is detected, the SSR.PER flag is set to 1 and receive data is transferred to the RDR register*1. If the SCR.RIE bit is 1 at this time, an ERI interrupt request is generated.
5. If a framing error (when the stop bit is 0) is detected, the SSR.FER flag is set to 1 and receive data is transferred to the RDR register*1. If the SCR.RIE bit is 1 at this time, an ERI interrupt request is generated.
6. When reception finishes successfully, receive data is transferred to the RDR register*1. If the SCR.RIE bit is 1 at this time, an RXI interrupt request is generated. Continuous reception is enabled by reading the receive data transferred to the RDR register*1 in this RXI interrupt handling routine before reception of the next receive data is completed. Reading the received data that have been transferred to the RDR register*1 causes the RTSn# pin to output the low level.

Note 1. Read data not in the RDR register but in the RDRH and RDRL registers when 9-bit data length is selected.
Note 2. The SCI checks for reading of the RDRL register only and does not check for reading of the RDRH register when 9-bit data length is selected.

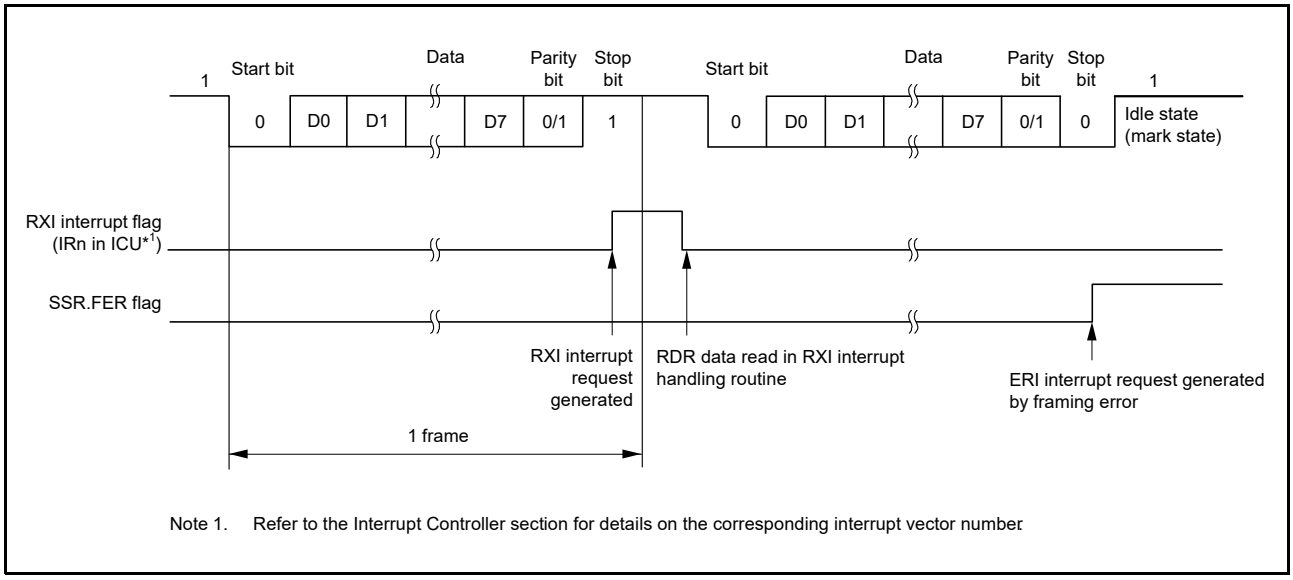
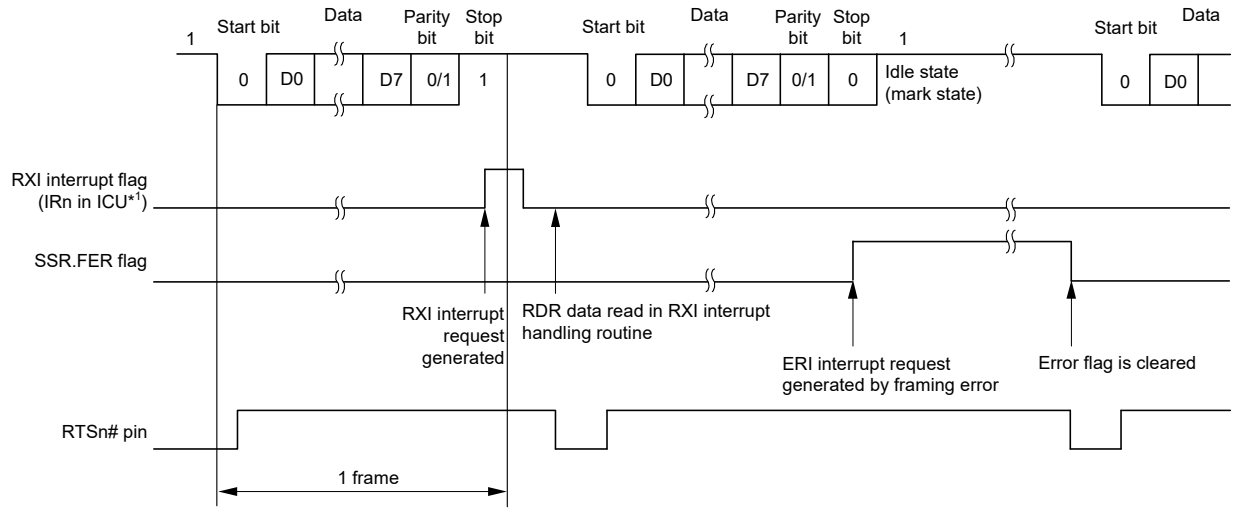


Figure 26.12 Example of SCI Operation for Serial Reception in Asynchronous Mode (1) (When RTS Function is Not Used) (Example with 8-Bit Data, Parity, 1 Stop Bit)



Note 1. Refer to the Interrupt Controller section for details on the corresponding interrupt vector number.

Figure 26.13 Example of SCI Operation for Serial Reception in Asynchronous Mode (2) (When RTS Function is Used) (Example with 8-Bit Data, Parity, 1 Stop Bit)

Table 26.25 lists the states of the flags in the SSR status register and receive data handling when a receive error is detected.

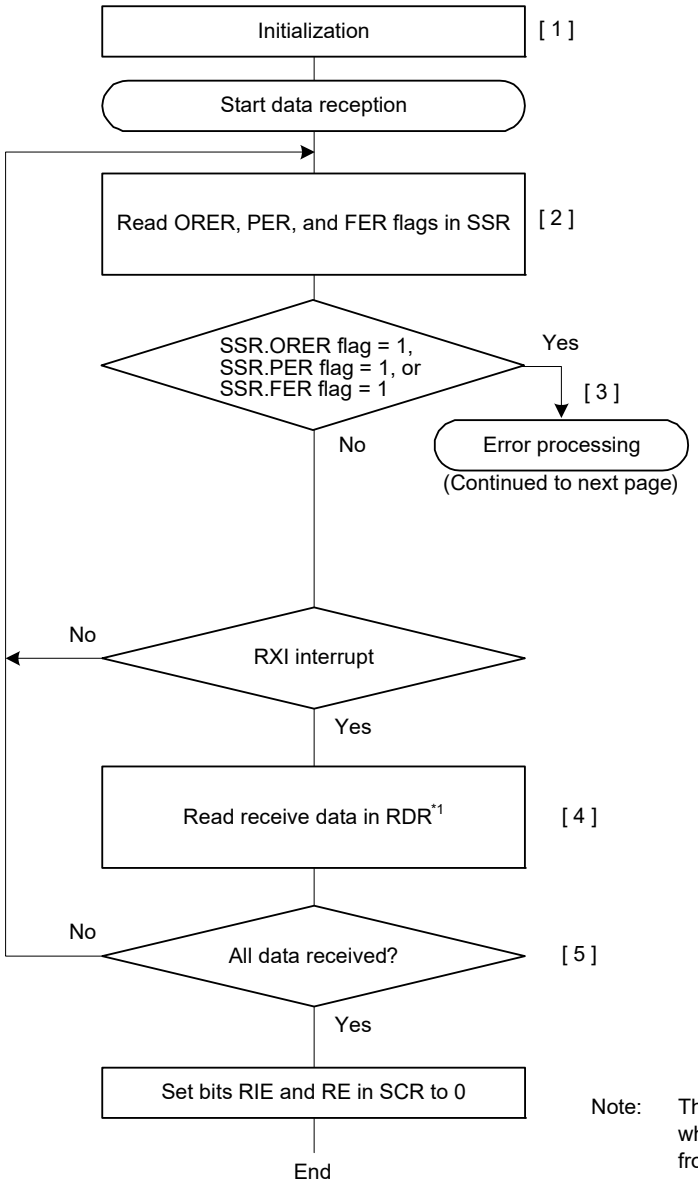
If a receive error is detected, an ERI interrupt request is generated but an RXI interrupt request is not generated. Data reception cannot be resumed while the receive error flag is 1. Accordingly, set the ORER, FER, and PER flags to 0 before resuming reception. Moreover, be sure to read the RDR (or the RDRL) during overrun error processing. When a reception is forcibly terminated by setting the SCR.RE bit to 0 during operation, read the RDR (or the RDRL) register because received data which has not yet been read may be left in RDR (or the RDRL).

Figure 26.14 and Figure 26.15 show samples of flowcharts for serial data reception.

Table 26.25 Flags in the SSR Status Register and Receive Data Handling

Flags in the SSR Status Register				
ORER	**FER**	**PER**	**Receive Data**	**Receive Error Type**
1	0	0	Lost	Overrun error
0	1	0	Transferred to RDR*1	Framing error
0	0	1	Transferred to RDR*1	Parity error
1	1	0	Lost	Overrun error + framing error
1	0	1	Lost	Overrun error + parity error
0	1	1	Transferred to RDR*1	Framing error + parity error
1	1	1	Lost	Overrun error + framing error + parity error

Note 1. Read data not in RDR but in the RDRH and RDRL registers when 9-bit data length is selected.



[1] SCI initialization:
Set data reception.

[2] [3] Receive error processing and break detection:
If a receive error occurs, an ERI interrupt is generated. An error is identified by reading the ORER, PER, and FER flags in SSR. After performing the appropriate error processing, be sure to set the ORER, PER, and FER flags to 0. Reception cannot be resumed if any of these flags is set to 1. In the case of a framing error, a break can be detected by reading the value of the input port corresponding to the RXDn pin.

[4] Read the receive data in RDR once in the RXI interrupt handling routine.

[5] Serial reception continuation procedure:
To continue serial reception, before the stop bit of the current frame is received, read data from RDR in the RXI interrupt handling routine.
The RDR data can also be read by activating the DTC.

Note: The RDR register becomes the RDRH and RDRL registers when 9-bit data length is selected. Read data in the order from RDRH to RDRL.

Figure 26.14 Example Flowchart of Serial Reception in Asynchronous Mode (1)

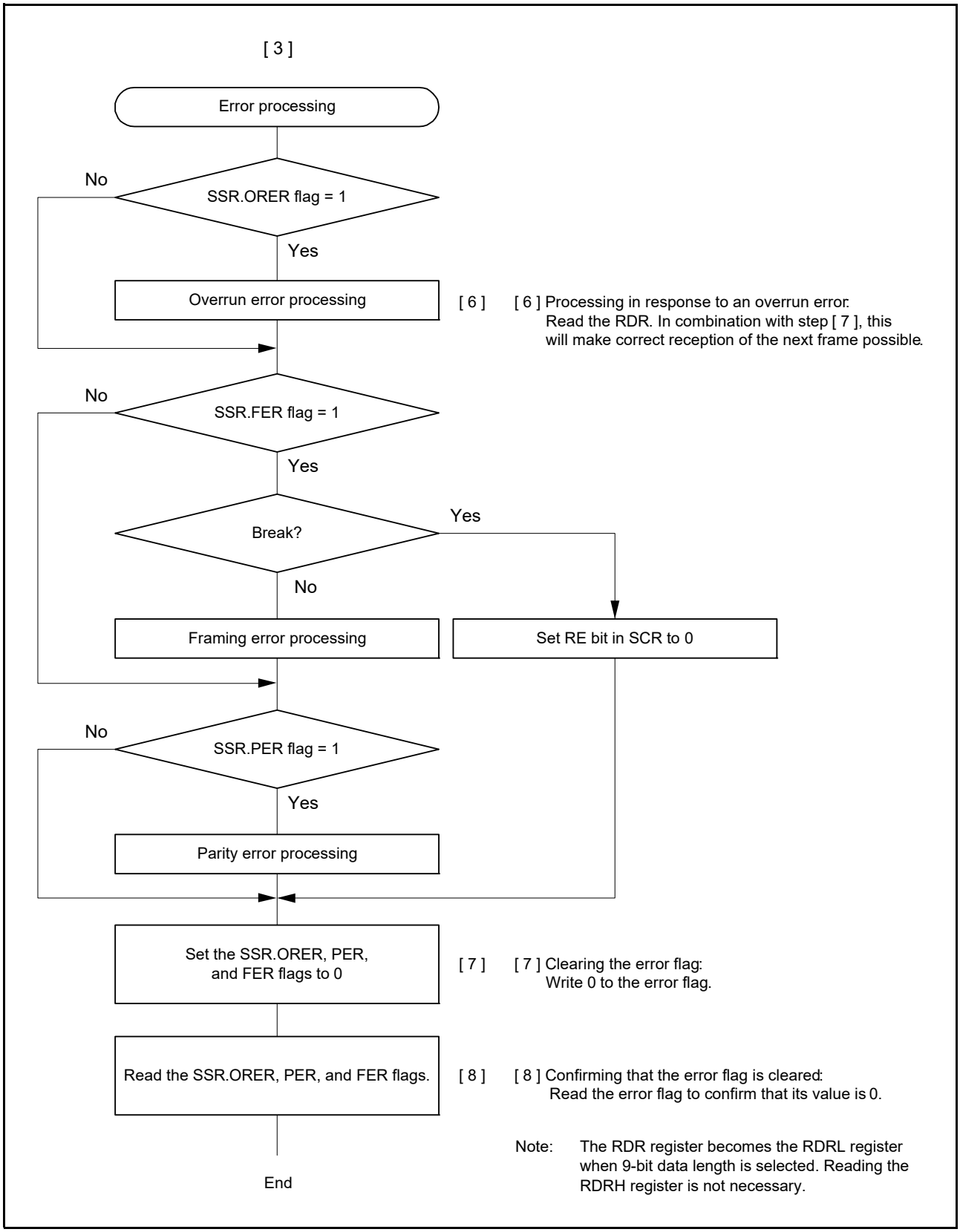


Figure 26.15 Example Flowchart of Serial Reception in Asynchronous Mode (2)

26.4 Multi-Processor Communications Function

Using the multi-processor communication functions enables to transmit and receive data by sharing a communication line between multiple processors by using asynchronous serial communication in which the multi-processor bit is added. In multi-processor communication, a unique ID code is allocated to each receiving station. Serial communication cycles consist of an ID transmission cycle to specify the receiving station and a data transmission cycle to transmit data to the specified receiving station. The multi-processor bit is used to distinguish between the ID transmission cycle and the data transmission cycle. When the multi-processor bit is set to 1, it indicates the ID transmission cycle and when the multi-processor bit is set to 0, it indicates the data transmission cycle. Figure 26.16 shows an example of communication between processors by using a multi-processor format. First, a transmitting station transmits communication data in which the multi-processor bit set to 1 is added to the ID code of the receiving station. Next, the transmitting station transmits the communication data in which the multi-processor bit set to 0 is added to the transmit data. Upon receiving the communication data in which the multi-processor bit is set to 1, the receiving station compares the received ID with the ID of the receiving station itself and if the two match, receives the communication data that is subsequently transmitted. If the received ID does not match with the ID of the receiving station, the receiving station skips the communication data until again receiving the communication data in which the multi-processor bit is set to 1.

For supporting this function, the SCI provides the SCR.MPIE bit. When the MPIE bit is set to 1, transfer of receive data from the RSR register to the RDR register (the RDRH and RDRL registers when 9-bit data length is selected), detection of a receive error, and setting the respective status flags RDRF, ORER and FER in the SSR register are disabled until reception of data in which the multi-processor bit is set to 1. Upon receiving a reception character in which the multi-processor bit is set to 1, the SSR.MPB bit is set to 1 and the SCR.MPIE bit is automatically cleared, thus returning to a normal reception operation. During this time, an RXI interrupt is generated if the SCR.RIE bit is 1.

When the multi-processor format is specified, specification of the parity bit is disabled. Apart from this, there is no difference from the operation in the normal asynchronous mode. A clock which is used for the multi-processor communication is also the same as the clock used in the normal asynchronous mode.

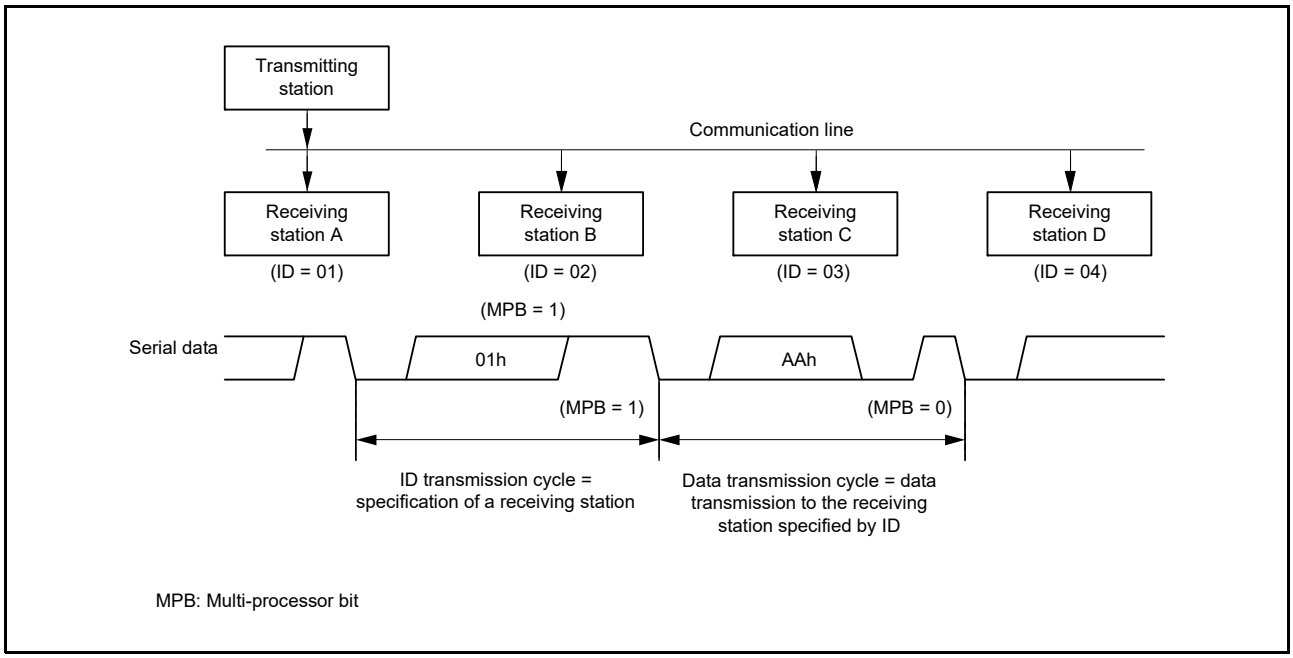


Figure 26.16 An Example of Communication using the Multi-Processor Format (Example of Transmission of Data AAh to Receiving Station A)

26.4.1 Multi-Processor Serial Data Transmission

Figure 26.17 is a sample flowchart of multi-processor data transmission. In the ID transmission cycle, the ID should be transmitted with the SSR.MPBT bit set to 1. In the data transmission cycle, the data should be transmitted with the MPBT bit set to 0. The other operations are the same as the operations in asynchronous mode.

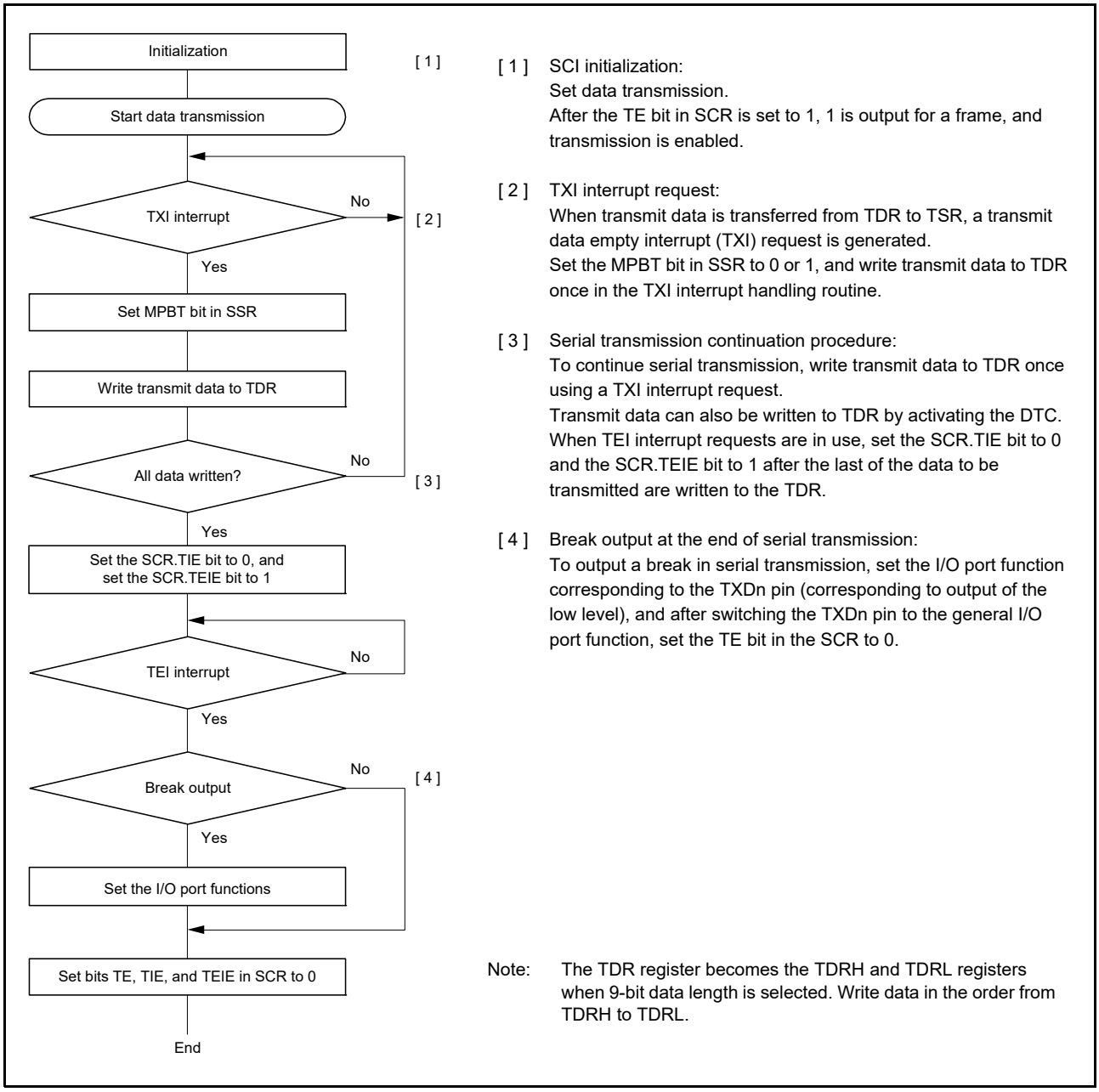


Figure 26.17 Example of Multi-Processor Serial Transmission Flowchart

26.4.2 Multi-Processor Serial Data Reception

Figure 26.19 and Figure 26.20 are sample flowcharts of multi-processor data reception. When the SCR.MPIE bit is set to 1, reading the communication data is skipped until reception of the communication data in which the multi-processor bit is set to 1. When the communication data in which the multi-processor bit is set to 1 is received, the received data is transferred to RDR (the RDRH and RDRL registers when 9-bit data length is selected). During this time, the RXI interrupt request is generated. The other operations are the same as the operations in asynchronous mode.
Figure 26.18 is the example of operation for reception.

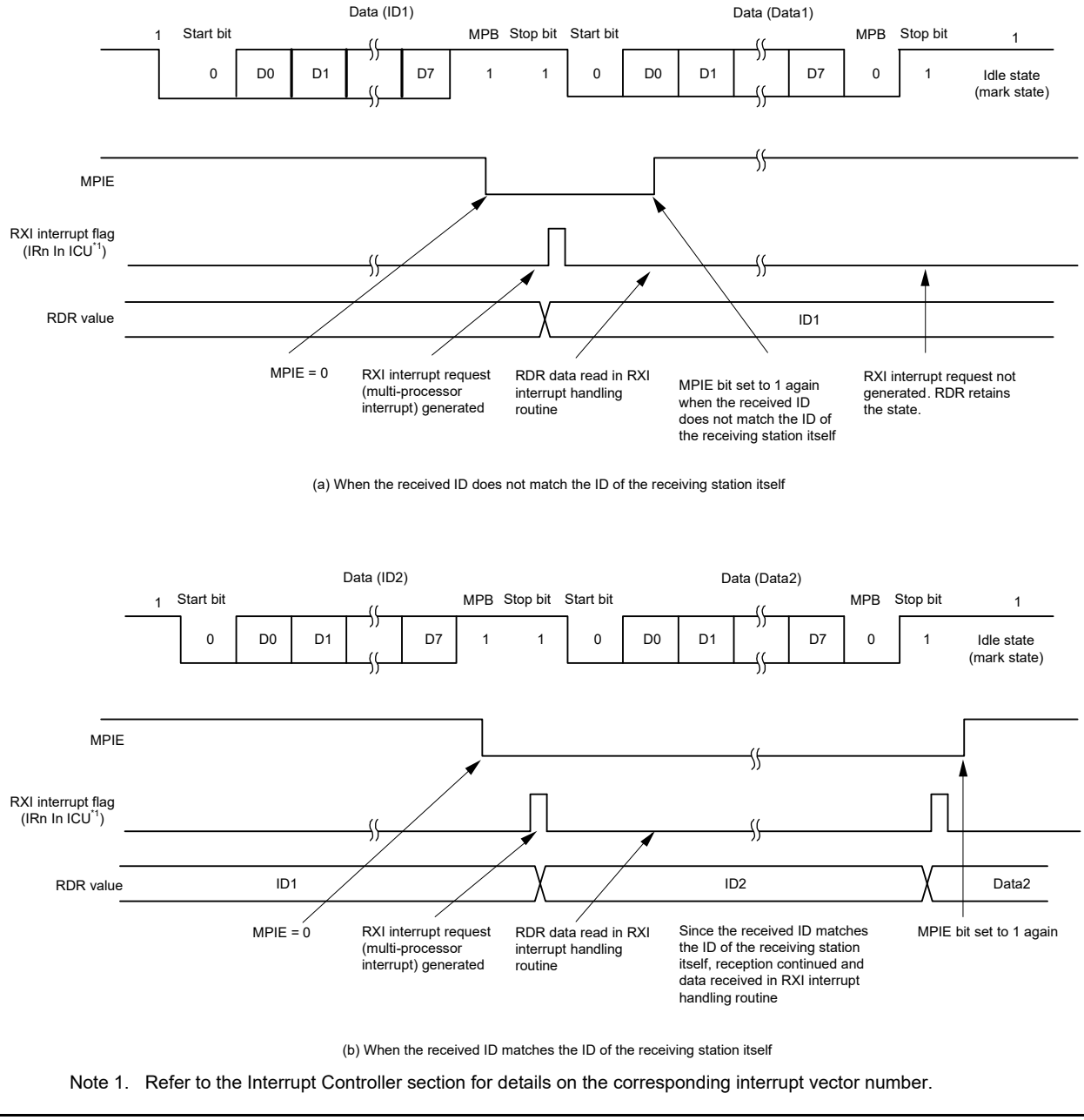
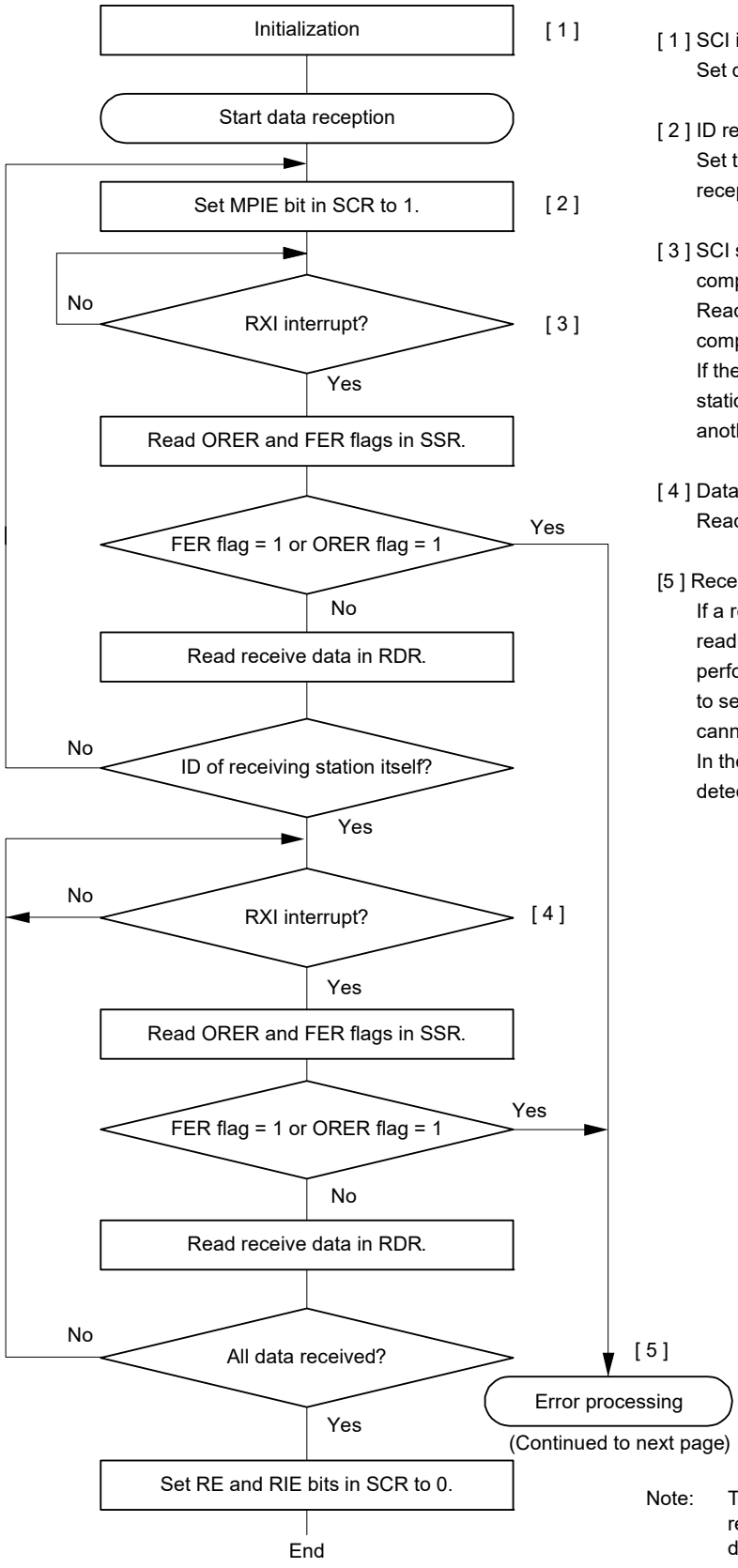


Figure 26.18 Example of SCI Reception (8-Bit Data/Multi-Processor Bit/1 Stop Bit)



[1] SCI initialization:
Set data reception.

[2] ID reception cycle:
Set the MPIE bit in SCR to 1 and wait for ID reception.

[3] SCI status confirmation and reception and comparison of ID:
Read data in RDR at the first RXI interrupt, and compare it with the ID of the receiving station itself. If the ID does not match the ID of the receiving station itself, set the MPIE bit to 1 again, and wait for another RXI interrupt RXI interrupt request.

[4] Data reception at an RXI interrupt:
Read data in RDR once in the RXI interrupt routine.

[5] Receive error processing and break detection:
If a receive error occurs, an error is identified by reading the ORER and FER flags in SSR. After performing the appropriate error processing, be sure to set the ORER and FER flags to 0. Reception cannot be resumed if any of these flags is set to 1. In the case of a framing error, a break can be detected by reading the value of the RXDn pin.

Note: The RDR register becomes the RDRH and RDRL registers when 9-bit data length is selected. Read data in the order from RDRH to RDRL.

Figure 26.19 Example of Multi-Processor Serial Reception Flowchart (1)

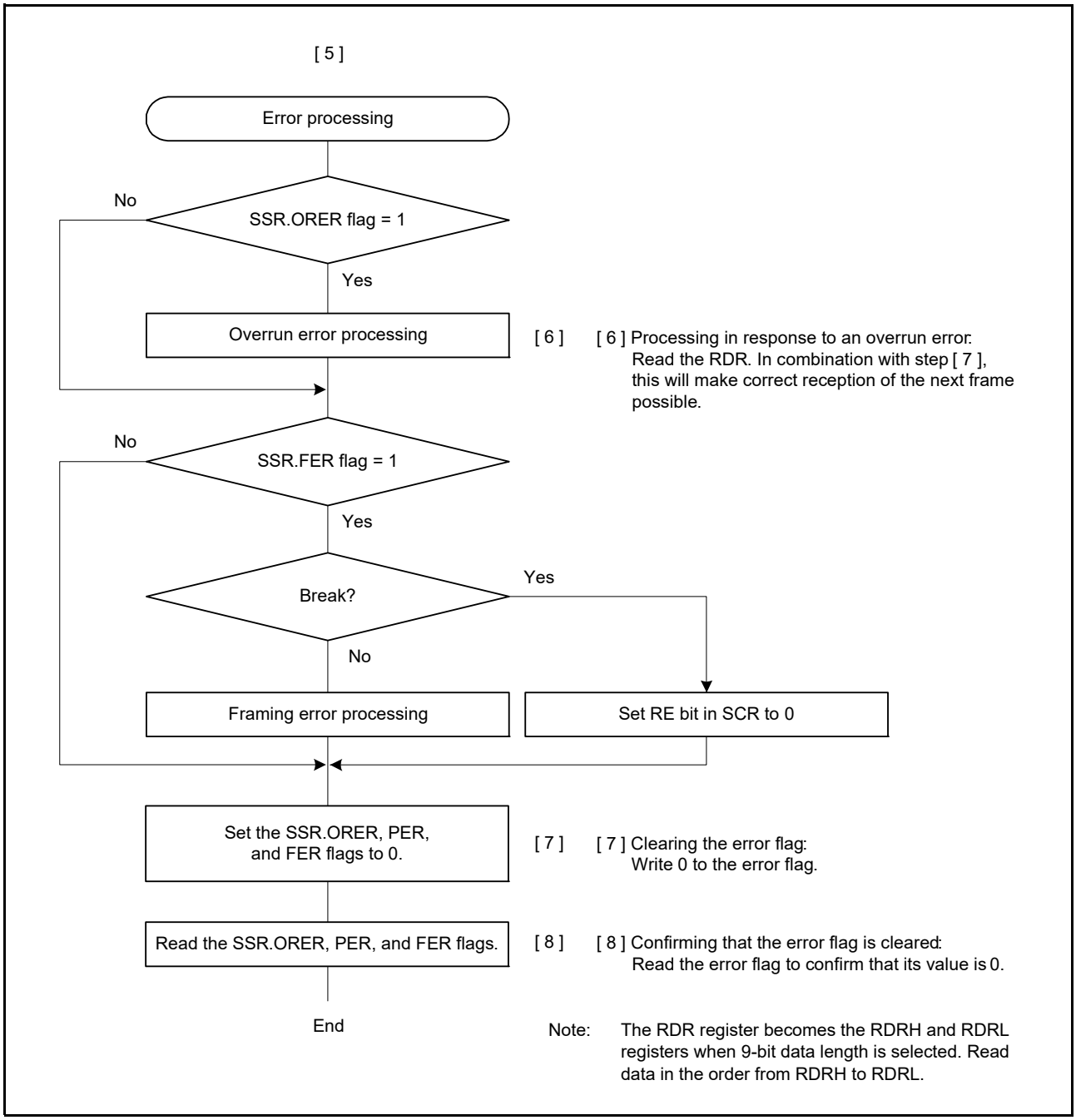


Figure 26.20 Example of Multi-Processor Serial Reception Flowchart (2)

26.5 Operation in Clock Synchronous Mode

Figure 26.21 shows the data format for clock synchronous serial data communications.
In clock synchronous mode, data is transmitted or received in synchronization with clock pulses. One character in transfer data consists of 8-bit data. In clock synchronous mode, no parity bit can be added.
In data transmission, the SCI outputs data from one falling edge of the synchronization clock to the next. In data reception, the SCI receives data in synchronization with the rising edge of the synchronization clock. After 8-bit data is output, the communication line holds the last bit output state.
Inside the SCI, the transmitter and receiver are independent units, enabling full-duplex communications by use of a common clock. Both the transmitter and the receiver also have a double-buffered structure, so that the next transmit data can be written during transmission or the previous receive data can be read during reception, enabling continuous data transfer.

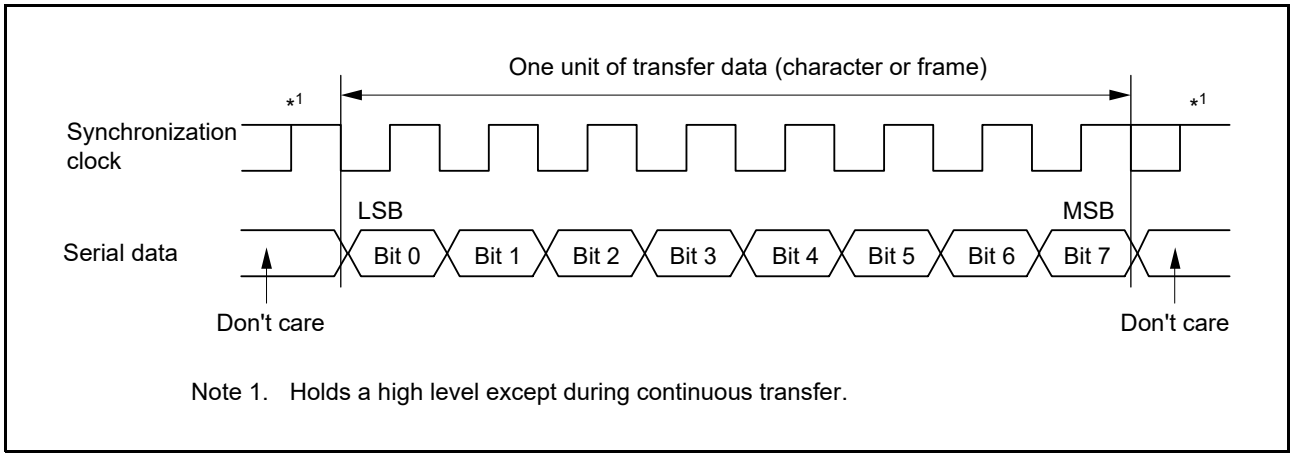


Figure 26.21 Data Format in Clock Synchronous Serial Communications (LSB First)

26.5.1 Clock

Either an internal clock generated by the on-chip baud rate generator or an external synchronization clock input at the SCKn pin can be selected, according to the setting of the SCR.CKE[1:0] bits.
When the SCI is operated on an internal clock, the synchronization clock is output from the SCKn pin. Eight synchronization clock pulses are output in the transfer of one character, and when no transfer is performed the clock is held high. However, when only data reception is performed while the CTS function is disabled, the synchronization clock output is started at the same time when the SCR.RE bit set to 1. The synchronization clock is stopped at the high level when an overrun error occurs or the SCR.RE bit is set to 0.
When only data reception is performed and the CTS function is enabled, the clock output is not started even when the SCR.RE bit set to 1 if the CTSn# pin input is high when the SCR.RE bit is 0. The synchronization clock output is started when the SCR.RE bit is set to 1 and the CTSn# pin input is low. After that, if the CTSn# pin input is high on completion of the frame reception, the synchronization clock output is stopped at the high level. If the CTSn# pin input continues to be low, the synchronization clock is stopped at the high level when an overrun error occurs or the SCR.RE bit is set to 0.

26.5.2 CTS and RTS Functions

In the CTS function, CTSn# pin input is used to control reception/transmission start when the clock source is the internal clock. Setting the SPMR.CTSE bit to 1 enables the CTS function.
When the CTS function is enabled, placing the low level on the CTSn# pin causes reception/transmission to start. Applying the high level to the CTS# pin while reception/transmission are in progress does not affect reception/transmission of the current frame, which continues.
In the RTS function, RTSn# pin output is used to request reception/transmission start when the clock source is an external synchronizing clock. A low level is output when serial communications become possible. Conditions for output of the low and high level are shown below.

[Conditions for low-level output]
When the following conditions are all satisfied

- The SCR.RE or SCR.TE bit is 1
- Transmission or reception of data is not in progress
- There are no received data yet to be read (when the SCR.RE bit is 1)
- Transmit data has been written (when the SCR.TE bit is 1)
- The SSR.ORER flag is 0

[Condition for high-level output]
The conditions for low-level output have not been satisfied.

26.5.3 SCI Initialization (Clock Synchronous Mode)

Before transmitting and receiving data, start by writing the initial value 00h to the SCR register and then continue through the procedure for SCI given in Figure 26.22. Whenever the operating mode or transfer format is changed, the SCR register must be initialized before the change is made.

Note that setting the SCR.RE bit to 0 initializes neither the ORER, FER, and PER flags in the SSR register nor the RDR register.

Moreover, note that switching the value of the SCR.TE bit from 1 to 0 or 0 to 1 while the SCR.TIE bit is 1 leads to the generation of a TXI interrupt request.

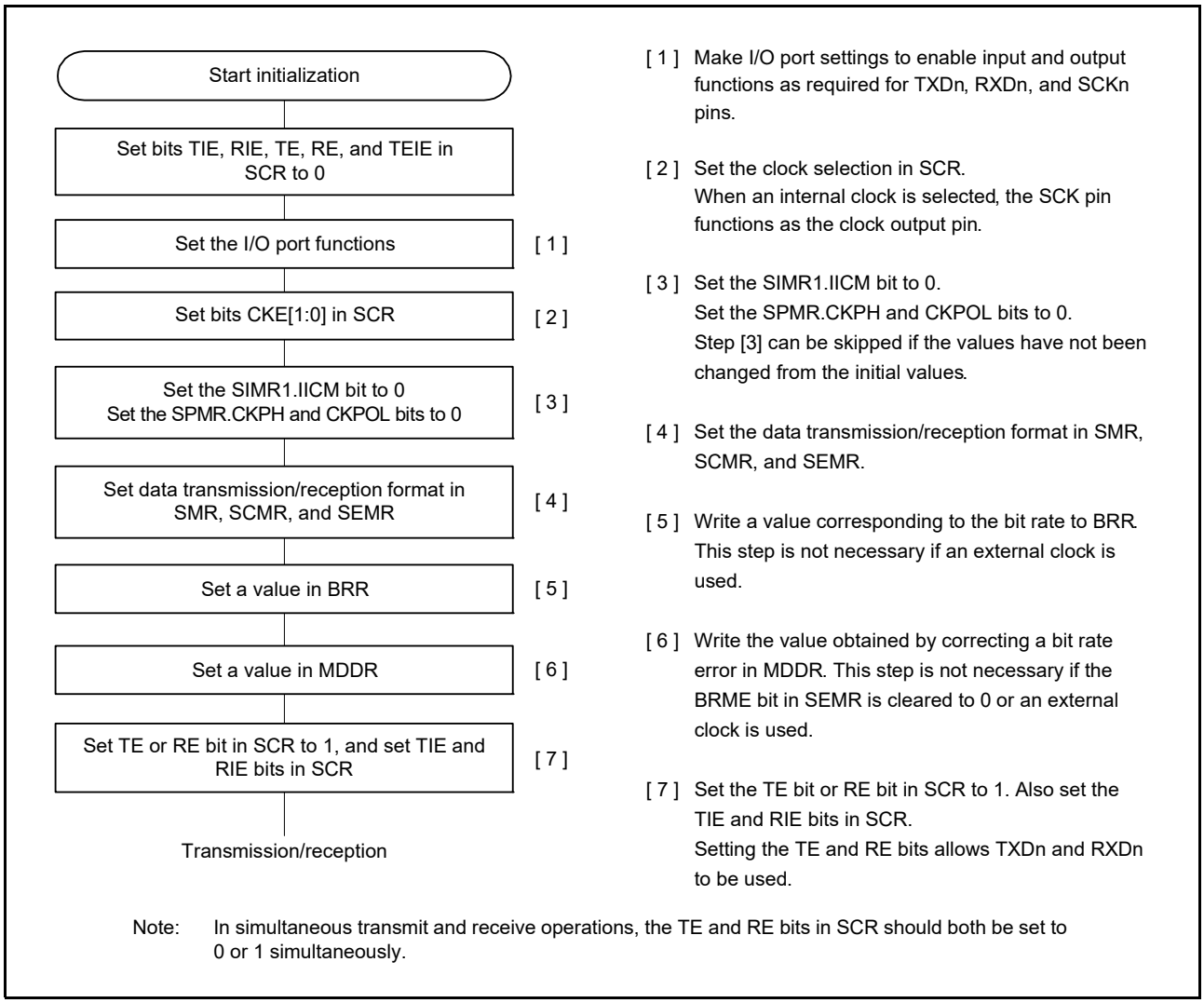


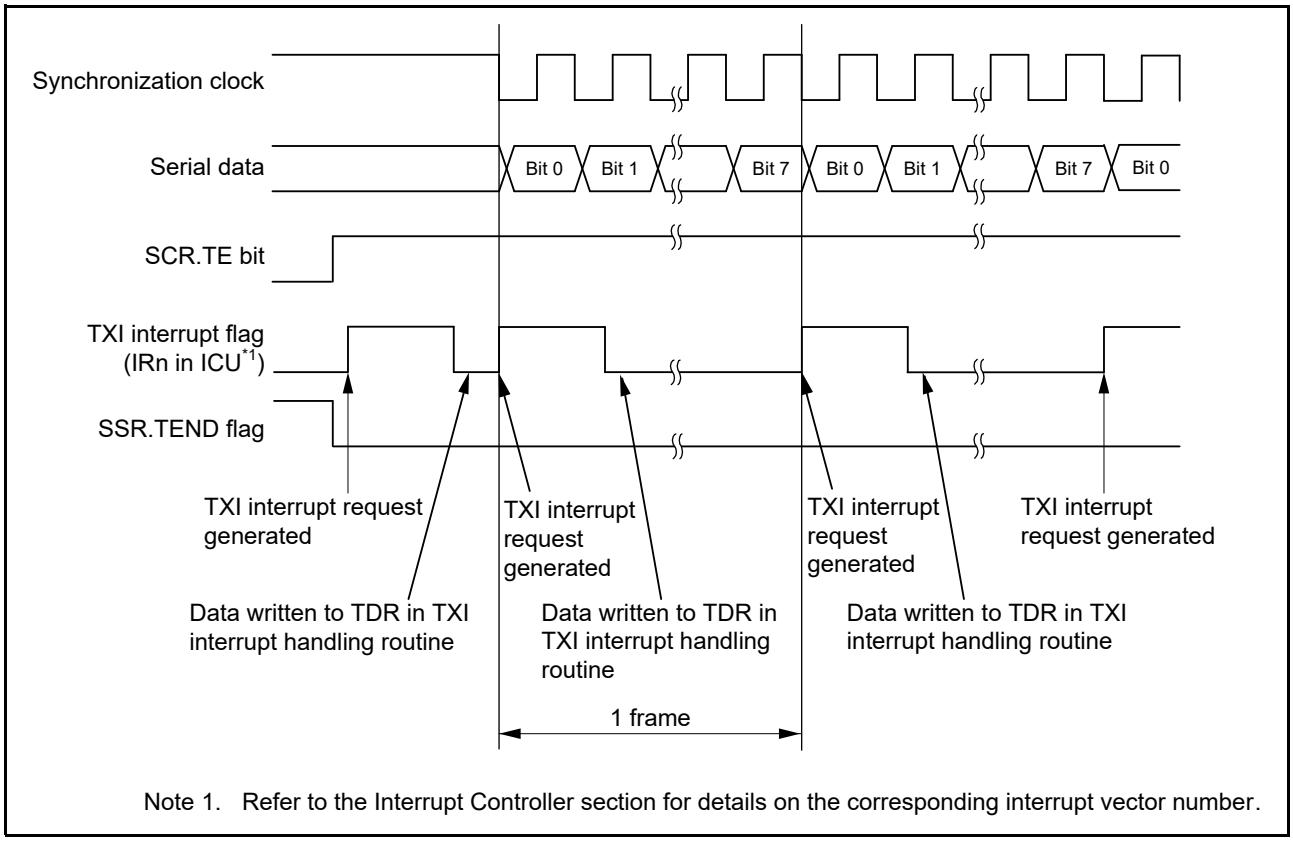
Figure 26.22 Example of SCI Initialization Flowchart (Clock Synchronous Mode)

26.5.4 Serial Data Transmission (Clock Synchronous Mode)

Figure 26.22, Figure 26.23, and Figure 26.24 show an example of the operation for serial transmission in clock synchronous mode.
In serial data transmission, the SCI operates as described below.

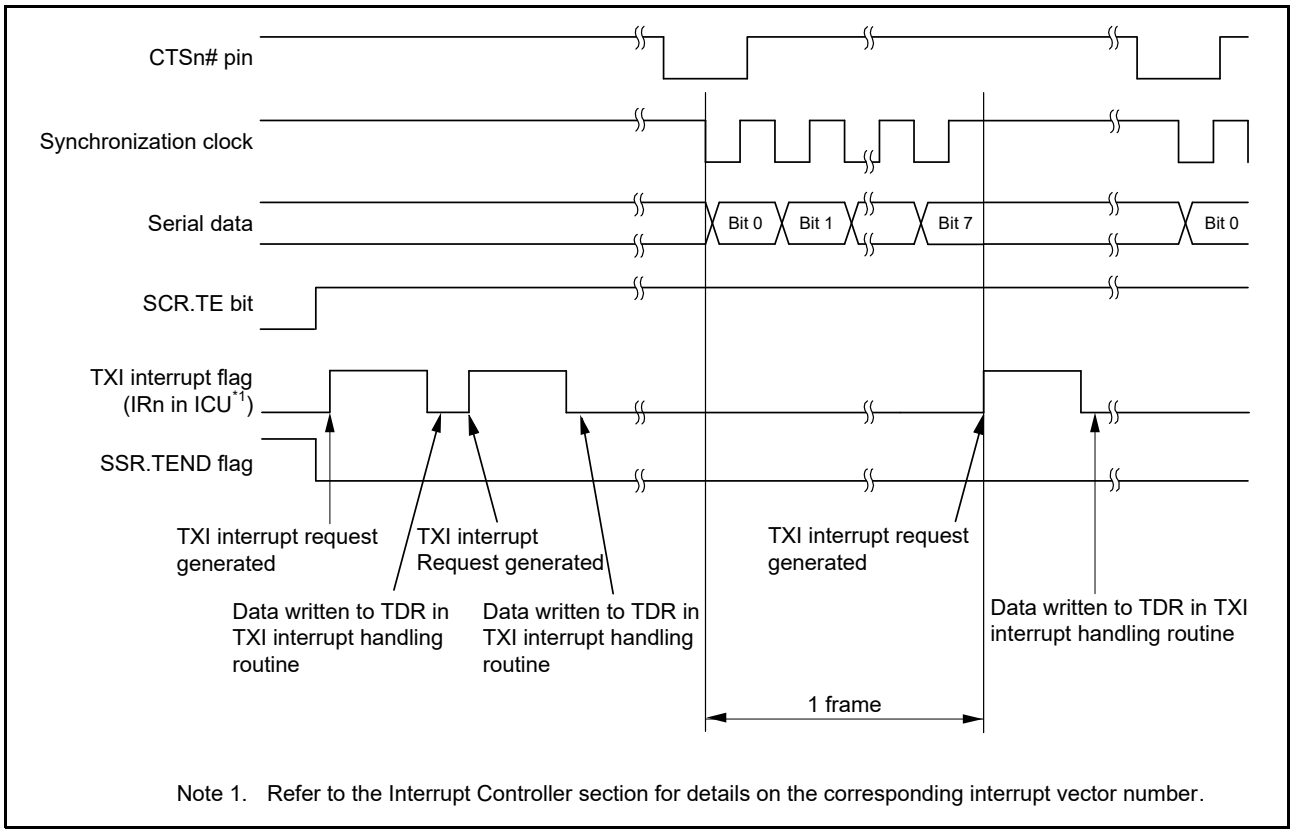
1. The SCI transfers data from TDR to TSR when data is written to TDR in the TXI interrupt handling routine. The TXI interrupt request at the beginning of transmission is generated when the TE bit in the SCR register is set to 1 after the TIE bit in the SCR register is set to 1 or when these 2 bits are set to 1 simultaneously by a single instruction.
2. After transferring data from the TDR register to the TSR register, the SCI starts transmission. When the SCR.TIE bit is set to 1 at this time, a TXI interrupt request is generated. Continuous transmission is enabled by writing the next transmit data to the TDR register in this TXI interrupt handling routine before transmission of the current transmit data has finished. When TEI interrupt requests are in use, set the SCR.TIE bit to 0 (a TXI interrupt request is disabled) and the SCR.TEIE bit to 1 (a TEI interrupt request is enabled) after the last of the data to be transmitted are written to the TDR register from the handling routine for TXI requests.
3. 8-bit data is sent from the TXDn pin in synchronization with the output clock when clock output mode has been specified and in synchronization with the input clock when use of an external clock has been specified. Output of the clock signal is suspended until the input CTS signal is at the low level while the CTSE bit in the SPMR register is 1 (CTS function is enabled).
4. The SCI checks for updating of (writing to) the TDR register at the time of the last bit output.
5. When TDR is updated, the next transmit data is transferred from the TDR register to the TSR register, and serial transmission of the next frame is started.
6. If the TDR register is not updated, set the SSR.TEND flag to 1 and the TXDn pin retains the output state of the last bit. If the TEIE bit in the SCR register is 1 at this time, a TEI interrupt request is generated. The SCKn pin is held high.

Figure 26.26 shows a sample flowchart of serial data transmission.
Transmission will not start while a receive error flag (ORER, FER, or PER in the SSR register) is set to 1. Be sure to set the receive error flags to 0 before starting transmission. Note that setting the RE bit in the SCR register to 0 does not clear the receive error flags.



Note 1. Refer to the Interrupt Controller section for details on the corresponding interrupt vector number.

Figure 26.23 Example of Serial Data Transmission in Clock Synchronous Mode When the CTS Function is Not Used at the Beginning of Transmission



Note 1. Refer to the Interrupt Controller section for details on the corresponding interrupt vector number.

Figure 26.24 Example of Serial Data Transmission in Clock Synchronous Mode When the CTS Function is Used at the Beginning of Transmission

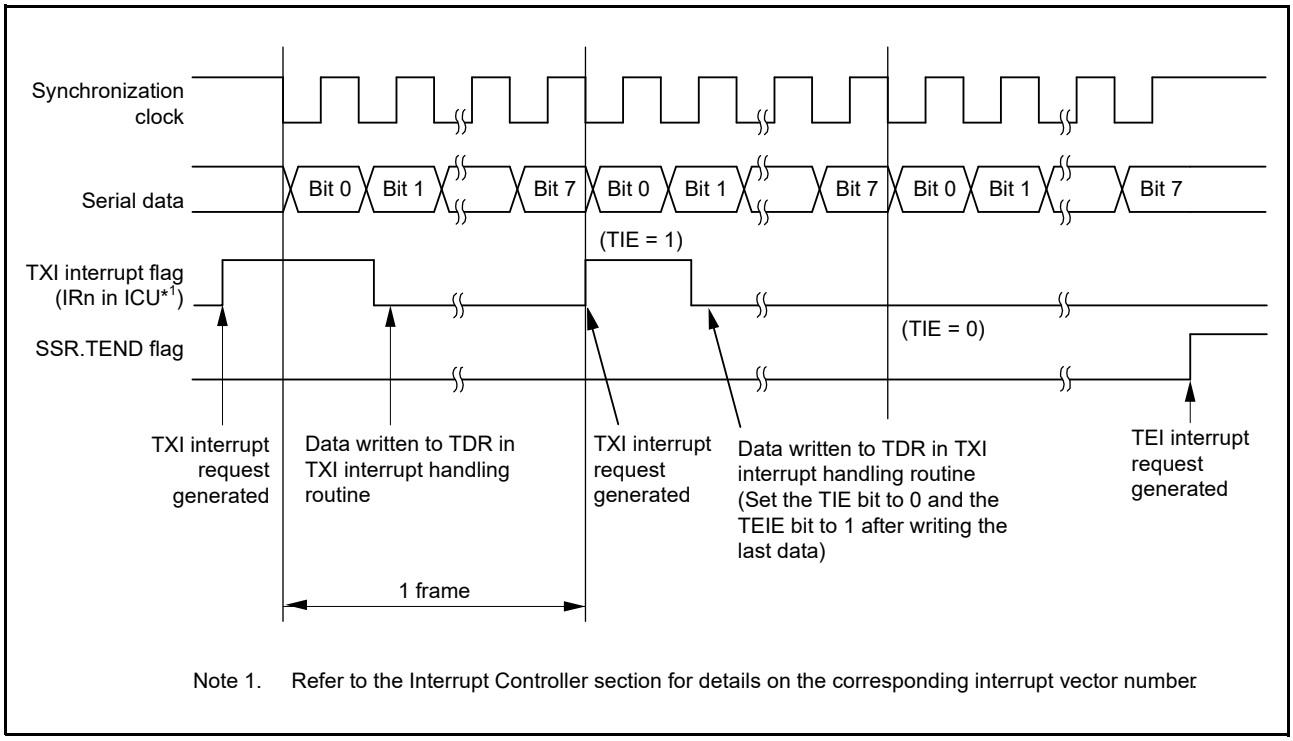
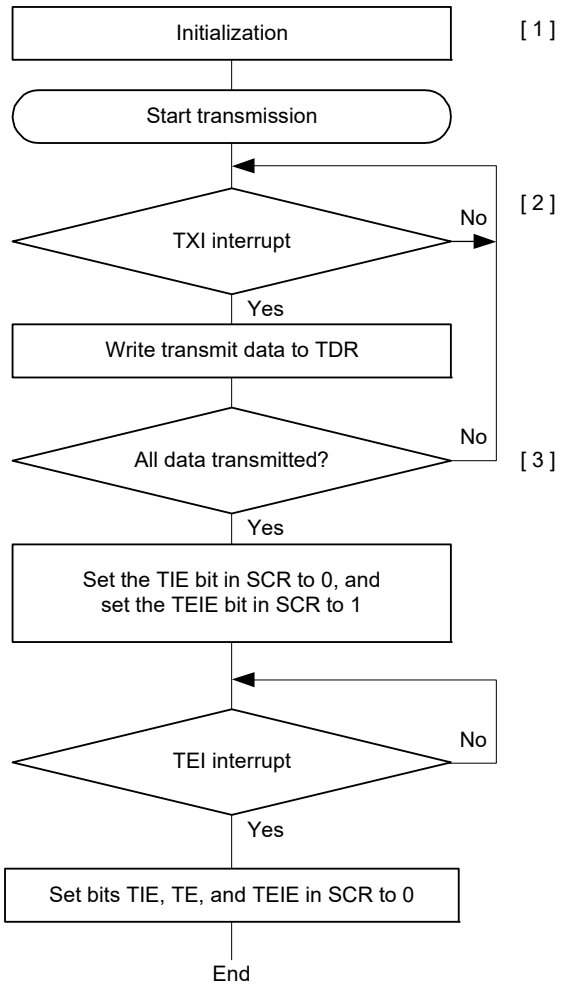


Figure 26.25 Example of Serial Data Transmission in Clock Synchronous Mode from the Middle of Transmission until Transmission Completion



[1] SCI initialization:
Set data transmission.

[2] Writing transmit data write to TDR by a TXI interrupt request:
When transmit data is transferred from TDR to TSR, a transmit data empty interrupt (TXI) request is generated.
Transmit data is written to TDR once from the handling routine for TXI requests.

[3] Serial transmission continuation procedure:
To continue serial transmission, write transmit data to TDR upon accepting a transmit data empty interrupt (TXI) request. Transmit data can also be written to TDR by activating the DTC by the TXI interrupt request.
When TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted are written to the TDR.

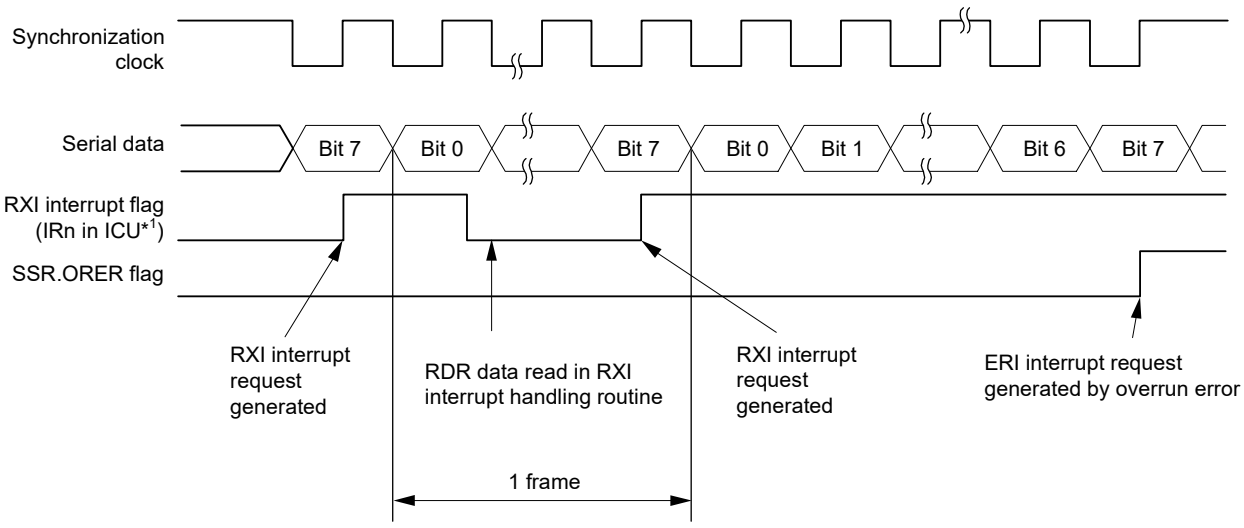
Note: When the external clock is in use (the value of the SCR.CKE[1:0] bits is 10b or 11b), the rising edge on the SCK pin for the last bit sets the SSR.TEND flag to 1. Setting the SCR.TE bit to 0 immediately after this may lead to insufficient received-data hold time on the receiver side.

Figure 26.26 Example Flowchart of Serial Transmission in Clock Synchronous Mode

26.5.5 Serial Data Reception (Clock Synchronous Mode)

Figure 26.27 and Figure 26.28 show an example of SCI operation for serial reception in clock synchronous mode. In serial data reception, the SCI operates as described below.

1. The value of the RE bit in the SCR register becoming 1 places the signal output on the RTSn# pin at the low level (when the RTS function is in use).
2. The SCI performs internal initialization and starts receiving data in synchronization with a synchronization clock input or output, and stores the receive data in the RSR register.
3. If an overrun error occurs, the ORER flag in the SSR register is set to 1. If the RIE bit in the SCR register is 1 at this time, an ERI interrupt request is generated. Receive data is not transferred to the RDR register.
4. When reception finishes successfully, receive data is transferred to the RDR register. If the RIE bit in the SCR register is 1 at this time, an RXI interrupt request is generated. Continuous reception is enabled by reading the receive data transferred to the RDR register in this RXI interrupt handling routine before reception of the next receive data is completed. Reading out the received data that have been transferred to the RDR register causes the RTSn# pin to output the low level (when the RTS function is in use).



Note 1. Refer to the Interrupt Controller section for the corresponding interrupt vector number.

Figure 26.27 Example of Operation for Serial Reception in Clock Synchronous Mode (1) (When RTS Function is Not Used)

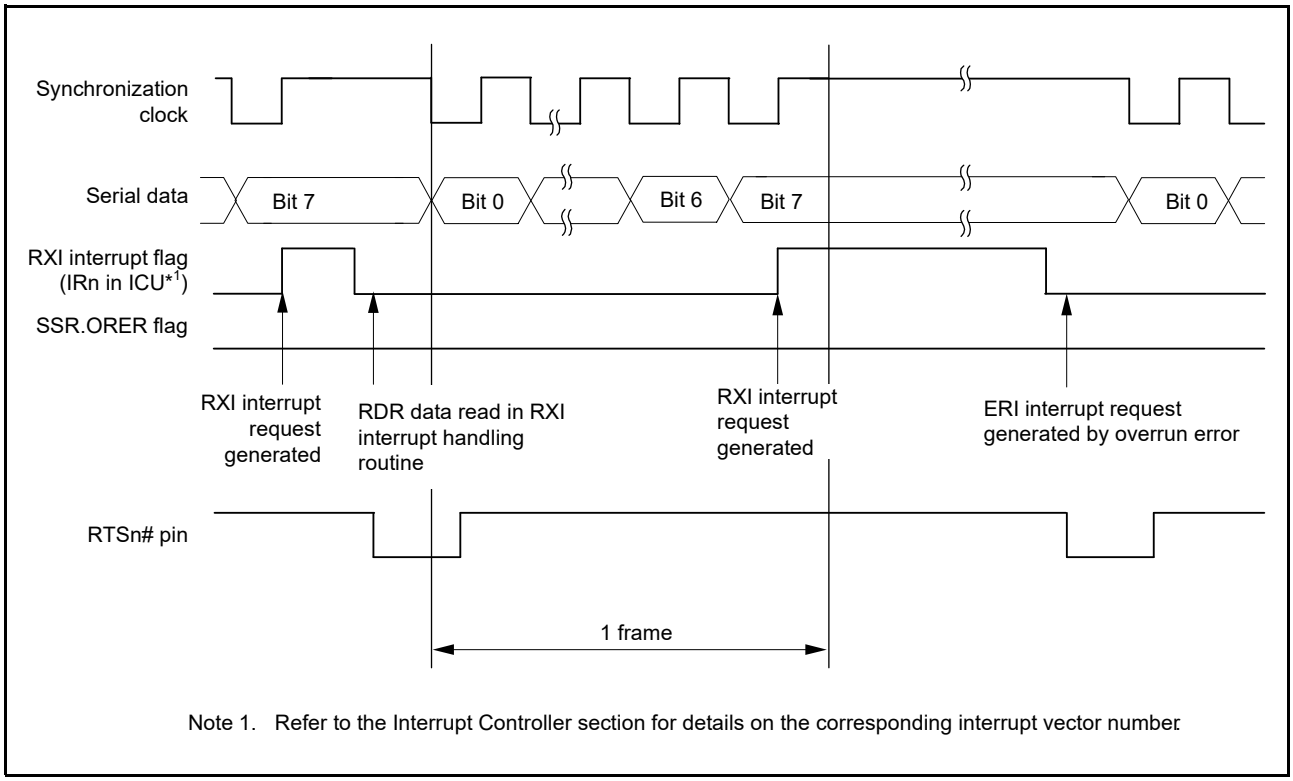
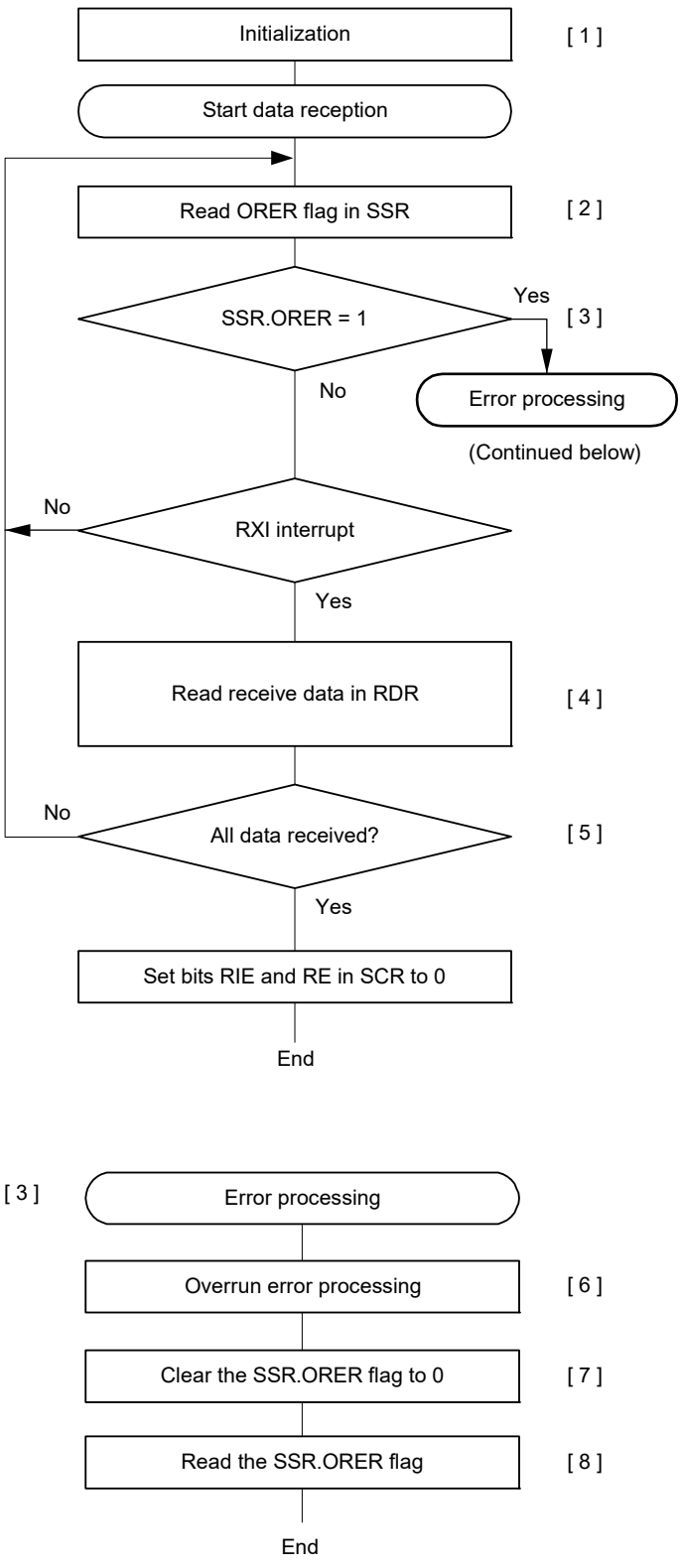


Figure 26.28 Example of Operation for Serial Reception in Clock Synchronous Mode (2) (When RTS Function is Used)

Data transfer cannot be resumed while a receive error flag is 1. Accordingly, clear the ORER, FER, and PER flags in the SSR register to 0 before resuming reception. Moreover, be sure to read the RDR register during overrun error processing. When a reception is forcibly terminated by setting the SCR.RE bit to 0 during operation, read the RDR register because received data which has not yet been read may be left in the RDR register.

Figure 26.29 shows a sample flowchart for serial data reception.



[1] SCI initialization:
Make input port-pin settings for pins to be used as RXDn pins.

[2] [3] Receive error processing:
If a receive error occurs, read the ORER flag in the SSR register, perform the relevant error processing, and then set the ORER flag to 0. Data reception cannot be resumed while the ORER flag is 1.

[4] Read the receive data in the RDR register once in the receive data full interrupt (RXI) request handling routine.

[5] Serial reception continuation procedure:
To continue serial reception, before the MSB (bit 7) of the current frame is received, finish reading the receive data in the RDR register. The RDR data can also be read by activating the DTC by an RXI interrupt request.

[6] Processing in response to an overrun error:
Read the RDR register. In combination with step [7], this will make correct reception of the next frame possible.

[7] Clearing the error flag:
Write 0 to the error flag.

[8] Confirming that the error flag is cleared:
Read the error flag to confirm that its value is 0.

Figure 26.29 Example Flowchart of Serial Reception in Clock Synchronous Mode

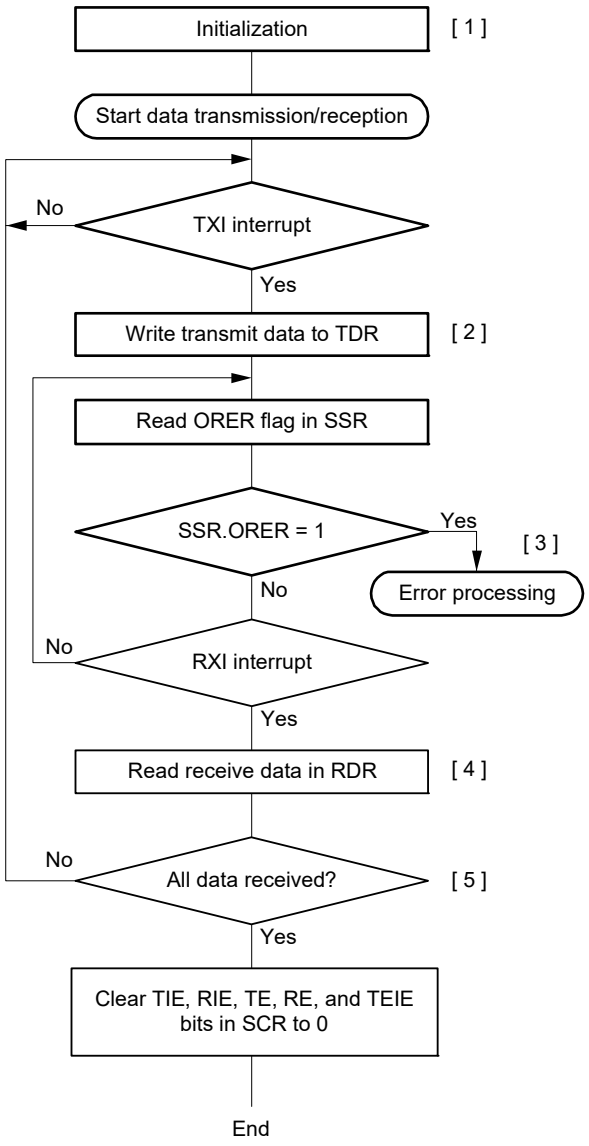
26.5.6 Simultaneous Serial Data Transmission and Reception (Clock Synchronous Mode)

Figure 26.30 shows a sample flowchart for simultaneous serial transmit and receive operations in clock synchronous mode.

After initializing the SCI, the following procedure should be used for simultaneous serial data transmit and receive operations.

To switch from transmit mode to simultaneous transmit and receive mode, check that the SCI has finished transmission by reading that the TEND flag in the SSR register is 1, and then initialize the SCR register. Then set the TIE, RIE, TE, and RE bits in the SCR register to 1 simultaneously by a single instruction.

To switch from receive mode to simultaneous transmit and receive mode, check that the SCI has finished reception, and then set the RIE and RE bits to 0. Then check that the receive error flags (ORER, FER, and PER in the SSR register) are 0, and then set the TIE, RIE, TE, and RE bits in the SCR register to 1 simultaneously by a single instruction.



[1] SCI initialization:
The TXDn pin can act as the output pin for transmitted data and the RXDn pin can act as the input pin for received data at the same time.

[2] Transmit data write:
Write transmit data to TDR once in the TXI interrupt handling routine.

[3] Receive error processing:
If a receive error occurs, read the ORER flag in the SSR register, perform the relevant error processing, and then set the ORER flag to 0. Data reception cannot be resumed while the ORER flag is 1.

[4] Reading receive data:
Read the receive data in the RDR register once in the RXI interrupt request handling routine.

[5] Serial transmission/reception continuation procedure:
To continue serial transmission and reception, before the MSB (bit 7) of the current frame is received, finish reading the receive data in the RDR register by the RXI interrupt. Also, before the MSB (bit 7) of the current frame is transmitted, write data to the TDR register by the TXI interrupt. Transmit data can also be written to the TDR register by activating the DTC by a transmit data empty interrupt (TXI) request. Similarly, the RDR data can also be read by activating the DTC by a receive data full interrupt (RXI) request.

Note: When switching from transmit or receive operation to simultaneous transmit and receive operations first set the TIE, RIE, TE, RE, and TEIE bits in SCR to 0, and then set TIE, RIE, TE, and RE bits to 1 simultaneously.

Figure 26.30 Example Flowchart of Simultaneous Serial Transmission and Reception in Clock Synchronous Mode

26.6 Operation in Smart Card Interface Mode

The SCI supports smart card (IC card) interfaces conforming to ISO/IEC 7816-3 (standard for Identification Cards), as an extended function of the SCI.
Smart card interface mode can be selected using the appropriate register.

26.6.1 Sample Connection

Figure 26.31 shows a sample connection between a smart card (IC card) and this MCU.
As in the figure, since this MCU communicates with an IC card using a single transmission line, interconnect the TXDn and RXDn pins and pull up the data transmission line to VCC using a resistor.
Setting the TE and RE bits in the SCR register to 1 with an IC card disconnected enables closed transmission/reception allowing self-diagnosis.
To supply an IC card with the clock pulses generated by the SCI, input the SCKn pin output to the CLK pin of an IC card.
The output port of the this MCU can be used to output a reset signal.

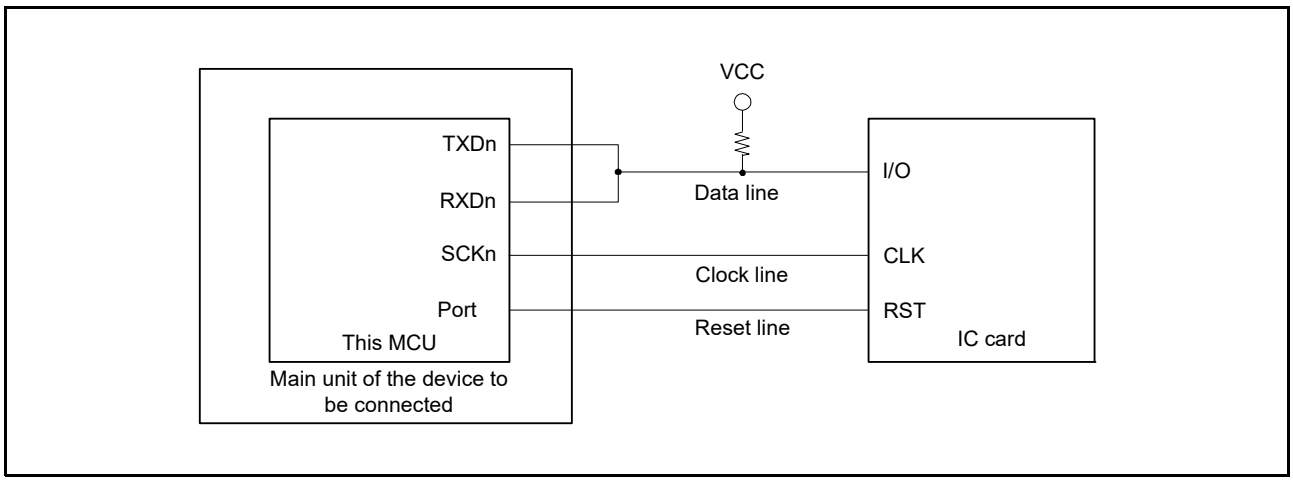


Figure 26.31 Sample Connection with a Smart Card (IC Card)

26.6.2 Data Format (Except in Block Transfer Mode)

Figure 26.32 shows the data transfer formats in smart card interface mode.

- One frame consists of 8-bit data and a parity bit in asynchronous mode.
- During transmission, at least 2 etu (elementary time unit: time required for transferring 1 bit) is secured as a guard time from the end of the parity bit until the start of the next frame.
- If a parity error is detected during reception, a low-level error signal is output for 1 etu after 10.5 etu has passed from the start bit.
- If an error signal is sampled during transmission, the same data is automatically retransmitted after at least 2 etu.

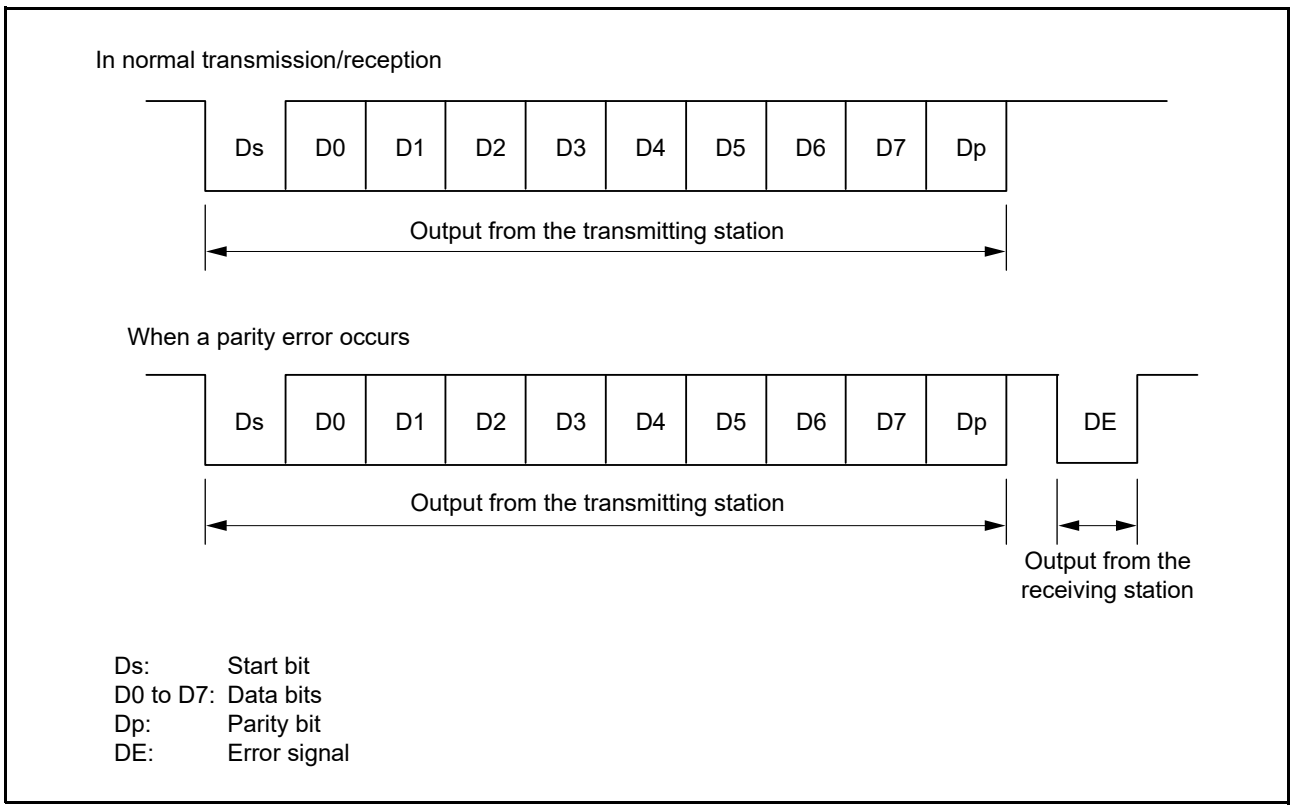


Figure 26.32 Data Formats in Smart Card Interface Mode

For communications with IC cards of the direct convention type and inverse convention type, follow the procedure below.

(1) Direct Convention Type

For the direct convention type, logic levels 1 and 0 correspond to states Z and A, respectively, and data is transferred with LSB first as the start character, as shown in Figure 26.33. Therefore, data in the start character in the figure is 3Bh. When using the direct convention type, write 0 to both the SDIR and SINV bits in the SCMR register. Write 0 to the PM bit in the SMR register in order to use even parity, which is prescribed by the smart card standard.

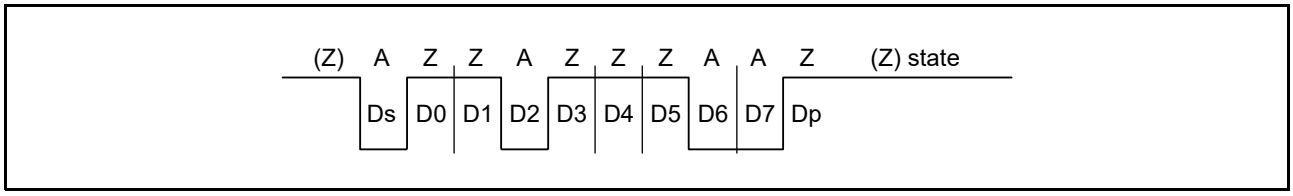


Figure 26.33 Direct Convention (SDIR in SCMR = 0, SINV in SCMR = 0, PM in SMR = 0)

(2) Inverse Convention Type

For the inverse convention type, logic levels 1 and 0 correspond to states A and Z, respectively and data is transferred with MSB first as the start character, as shown in Figure 26.34. Therefore, data in the start character in the figure is 3Fh. When using the inverse convention type, write 1 to both the SDIR and SINV bits in the SCMR register. The parity bit is logic level 0 to produce even parity, which is prescribed by the smart card standard, and corresponds to state Z. Since the SINV bit of the this MCU only inverts data bits D7 to D0, write 1 to the PM bit in the SMR register to invert the parity bit for both transmission and reception.

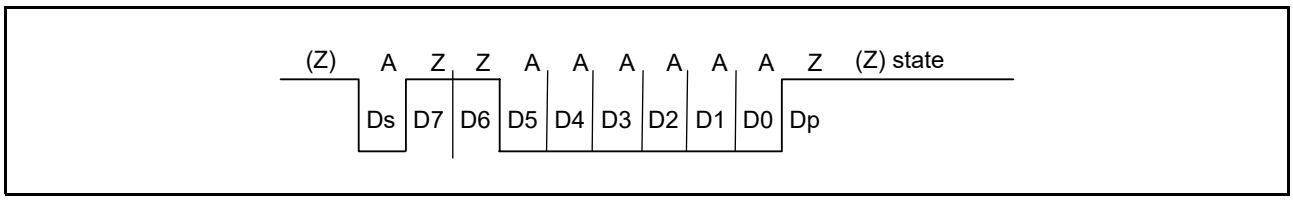


Figure 26.34 Inverse Convention (SDIR in SCMR = 1, SINV in SCMR = 1, PM in SMR = 1)

26.6.3 Block Transfer Mode

Block transfer mode is different from normal smart card interface mode in the following respects.

- Even if a parity error is detected during reception, no error signal is output. Since the PER bit in the SSR register is set by error detection, clear the PER bit before receiving the parity bit of the next frame.
- During transmission, at least 1 etu is secured as a guard time from the end of the parity bit until the start of the next frame.
- Since the same data is not retransmitted during transmission, the TEND flag in the SSR register is set 11.5 etu after transmission start.
- In block transfer mode, the ERS flag in the SSR register indicates the error signal status as in normal smart card interface mode, but the flag is read as 0 because no error signal is transferred.

26.6.4 Receive Data Sampling Timing and Reception Margin

Only the internal clock generated by the on-chip baud rate generator can be used as a transfer clock in smart card interface mode.

In this mode, the SCI can operate on a base clock with a frequency of 32, 64, 372, 256, 93, 128, 186, or 512 times the bit rate according to the settings of the BCP2 bit in the SCMR register and the BCP[1:0] bits in the SMR register (the frequency is always 16 times the bit rate in normal asynchronous mode).

For data reception, the falling edge of the start bit is sampled with the base clock to perform internal synchronization. Receive data is sampled on the 16th, 32nd, 186th, 128th, 46th, 64th, 93rd, and 256th rising edges of the base clock so that it can be latched at the middle of each bit as shown in Figure 26.35. The reception margin here is determined by the following formula.

$$M = \left| (0.5 - \frac{1}{2N}) - (L - 0.5)\ F - \frac{\left| D - 0.5 \right|}{N} (1 + F) \right| \times 100\ [\%]$$

M: Reception margin (%)
N: Ratio of bit rate to clock (N = 32, 64, 372, 256)
D: Duty cycle of clock (D = 0 to 1.0)
L: Frame length (L = 10)
F: Absolute value of clock frequency deviation

Assuming values of F = 0, D = 0.5, and N = 372 in the above formula, the reception margin is determined by the formula below.

$$M = \{0.5 - 1/(2 \times 372)\} \times 100\ [\%] = 49.866\%$$

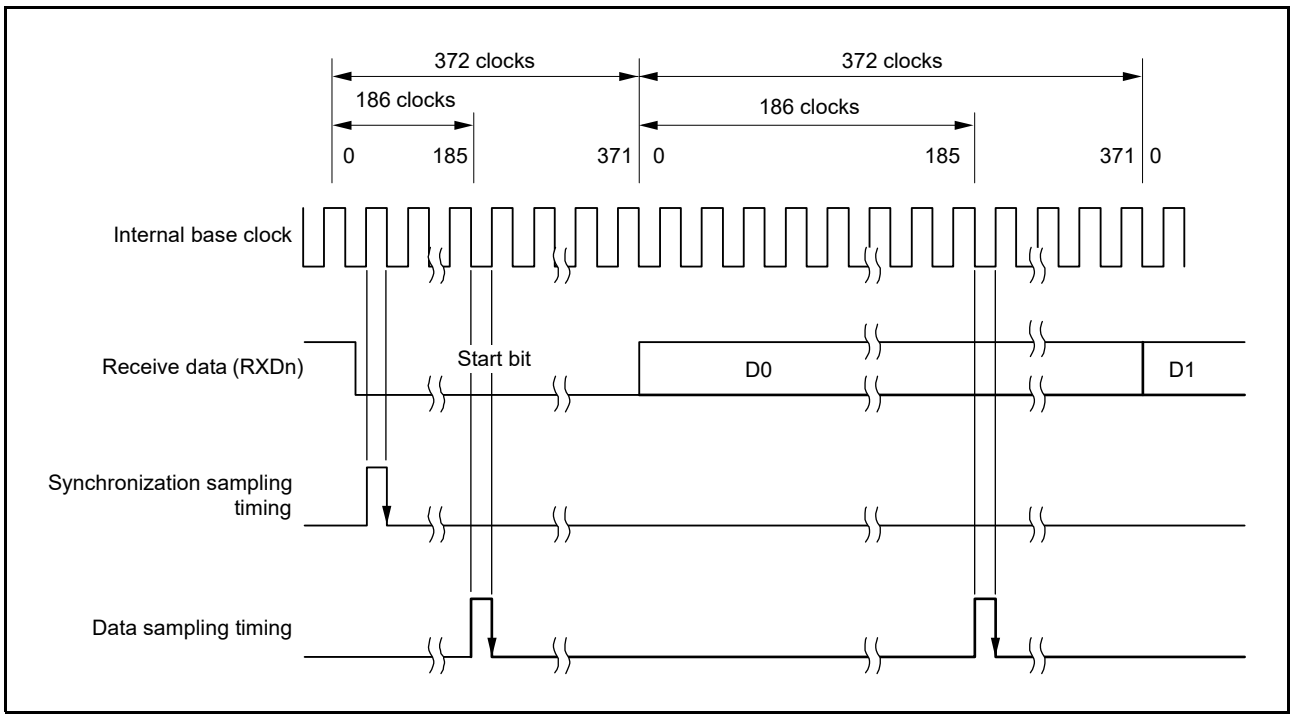


Figure 26.35 Receive Data Sampling Timing in Smart Card Interface Mode (When Clock Frequency is 372 Times the Bit Rate)

26.6.5 SCI Initialization (Smart Card Interface Mode)

Initialize the SCI following the example of flowchart shown in Figure 26.36.
Be sure to initialize the SCI before switching from transmission mode to reception mode and vice versa. Even if the RE bit is set to 0, the RDR register is not initialized.

To change reception mode to transmission mode, first check that reception has completed, and then initialize the SCI. At the end of initialization, set TE = 1 and RE = 0. Reception completion can be verified by reading the RXI request, ORER, or PER flag in the SSR register.
To change transmission mode to reception mode, first check that transmission has completed, and then initialize the SCI. At the end of initialization, set TE = 0 and RE = 1. Transmission completion can be verified by reading the TEND flag in the SSR register.

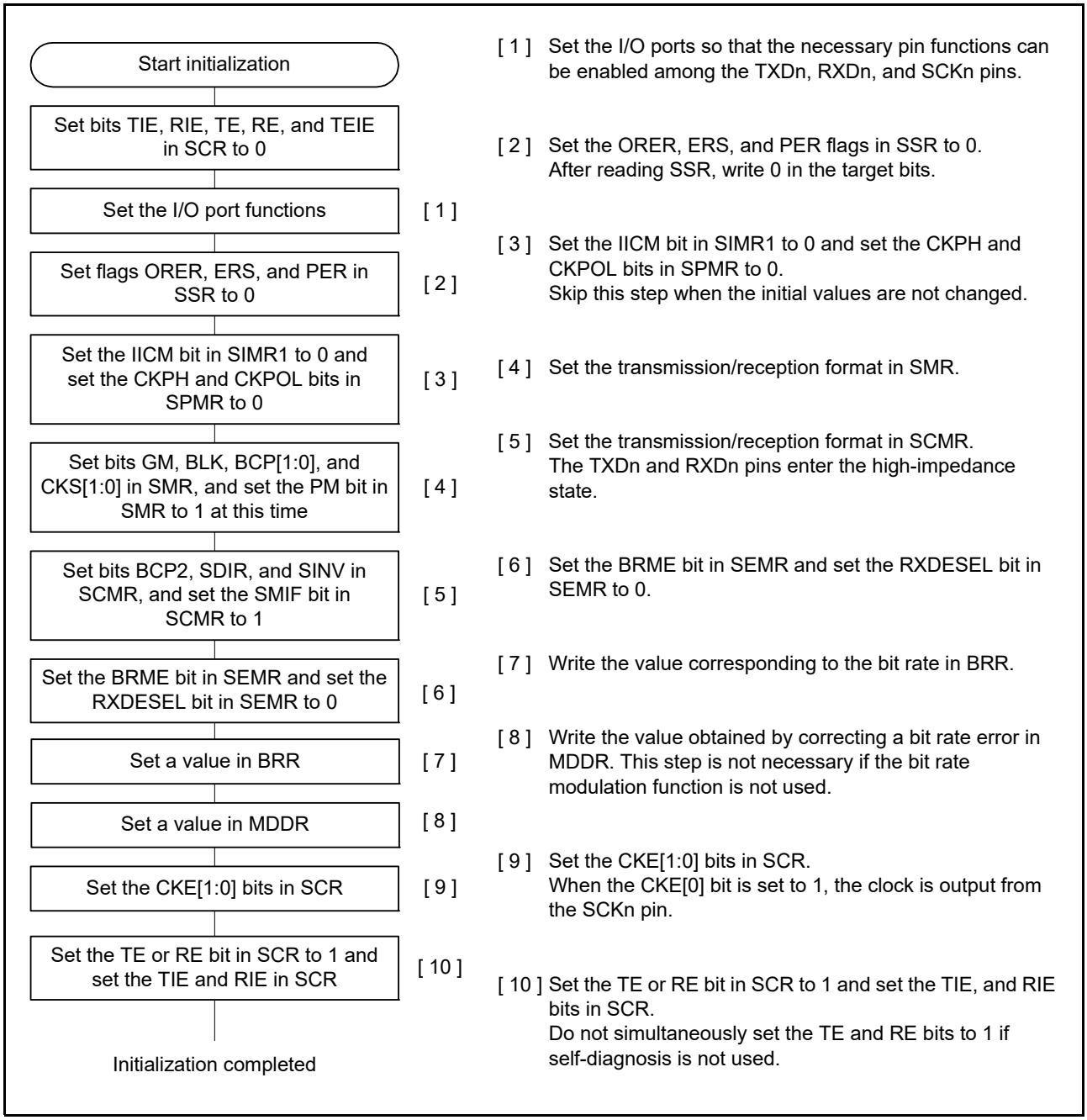


Figure 26.36 Example of SCI Initialization Flowchart (Smart Card Interface Mode)

26.6.6 Serial Data Transmission (Except in Block Transfer Mode)

Serial data transmission in smart card interface mode (except in block transfer mode), in that an error signal is sampled and data can be retransmitted, is different from that in non-smart card interface mode. Figure 26.37 shows the data retransfer operation during transmission.

1. When an error signal from the receiver end is sampled after one-frame data has been transmitted, the ERS flag in the SSR register is set to 1. If the RIE bit in the SCR register is 1 at this time, an ERI interrupt request is generated. Clear the ERS flag to 0 before the next parity bit is sampled.
2. For a frame in which an error signal is received, the TEND flag in the SSR register is not set. Data is retransferred from the TDR register to the TSR register allowing automatic data retransmission.
3. If no error signal is returned from the receiver, the ERS flag is not set to 1.
4. In this case, the SCI judges that transmission of one-frame data (including retransfer) has been completed, and the TEND flag is set. If the TIE bit in the SCR register is 1 at this time, a TXI interrupt request is generated. Writing transmit data to the TDR register starts transmission of the next data.

Figure 26.39 shows a sample flowchart of serial transmission. All the processing steps are automatically performed using a TXI interrupt request to activate the DTC.

When the TEND flag in the SSR register is set to 1 in transmission, if the TIE bit in the SCR register is 1, a TXI interrupt request is generated. The DTC is activated by a TXI interrupt request if the TXI interrupt request is specified as a source of DTC activation beforehand, allowing transfer of transmit data. The TEND flag is automatically set to 0 when the DTC transfers the data.

If an error occurs, the SCI automatically retransmits the same data. During this retransmission, the TEND flag is kept to 0 and the DTC is not activated. Therefore, the SCI and DTC automatically transmit the specified number of bytes, including retransmission in the case of error occurrence. However, since the ERS flag is not automatically cleared, set the RIE bit to 1 beforehand to enable an ERI interrupt request to be generated at error occurrence, and clear the ERS flag to 0.

When transmitting/receiving data using the DTC, be sure to make settings to enable the DTC before making SCI settings. For DTC settings, refer to section 17, Data Transfer Controller (DTCa).

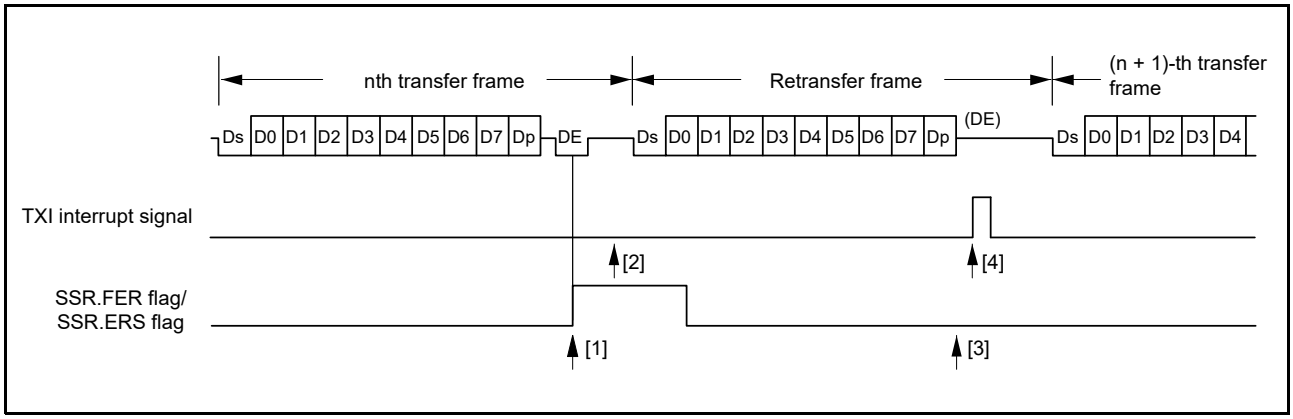


Figure 26.37 Data Retransfer Operation in SCI Transmission Mode

Note that the SSR.TEND flag is set in different timings depending on the GM bit setting in the SMR register. Figure 26.38 shows the TEND flag generation timing.

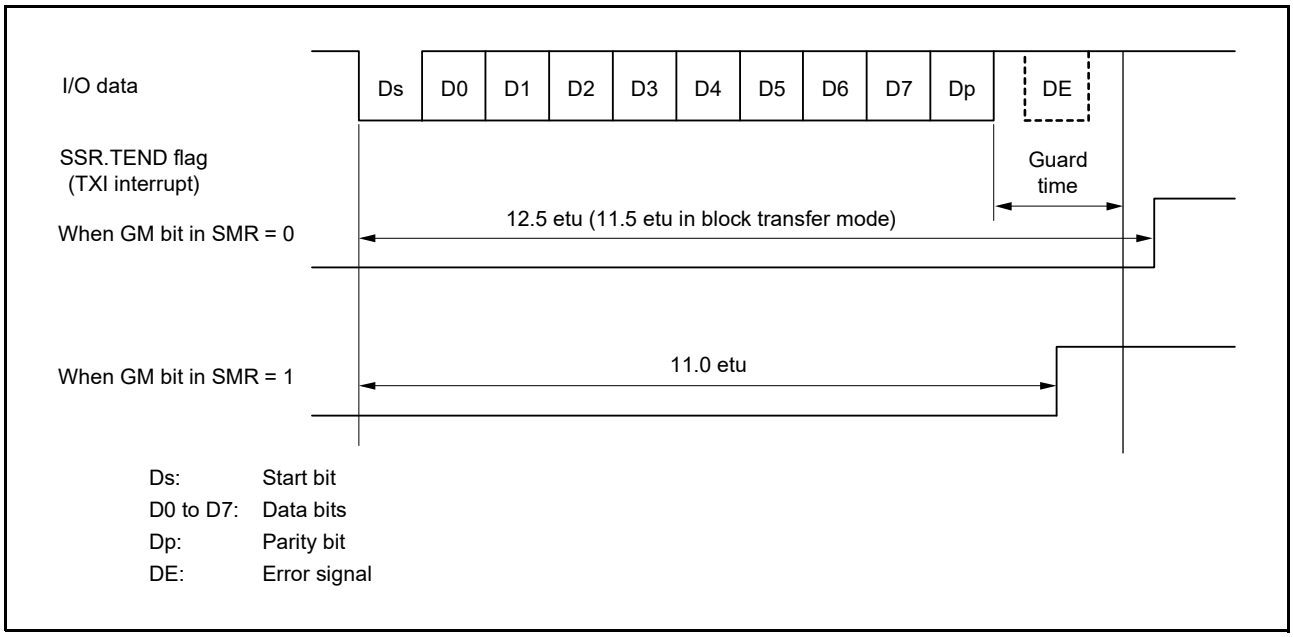


Figure 26.38 SSR.TEND Flag Generation Timing during Transmission

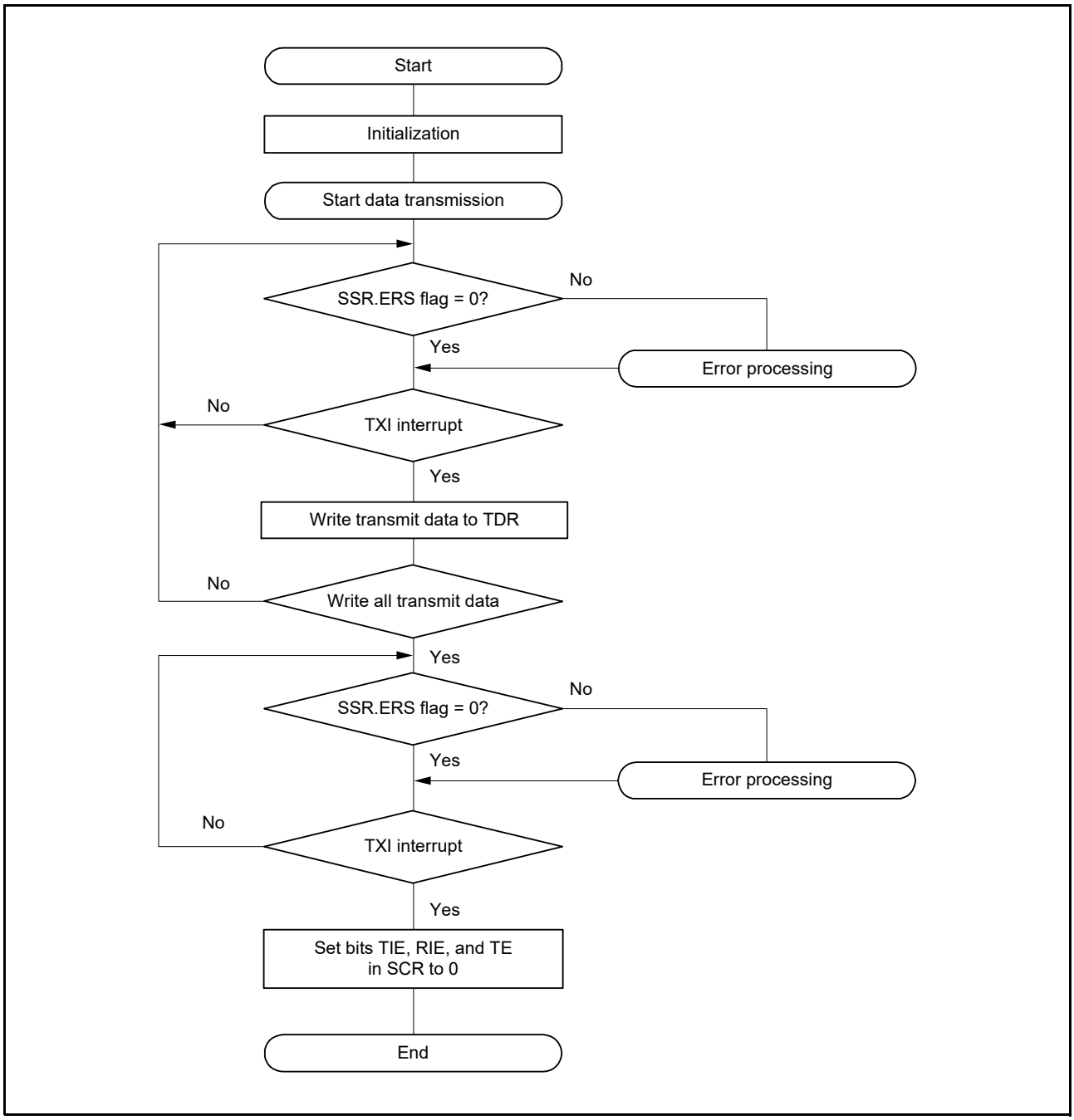


Figure 26.39 Sample Smart Card Interface Transmission Flowchart

26.6.7 Serial Data Reception (Except in Block Transfer Mode)

Serial data reception in smart card interface mode is similar to that in non-smart card interface mode. Figure 26.40 shows the data retransfer operation in reception mode.

1. If a parity error is detected in receive data, the PER flag in the SSR register is set to 1. When the RIE bit in the SCR register is 1 at this time, an ERI interrupt request is generated. Clear the PER flag to 0 before the next parity bit is sampled.
2. For a frame in which a parity error is detected, no RXI interrupt is generated.
3. When no parity error is detected, the PER flag in the SSR register is not set to 1.
4. In this case, data is determined to have been received successfully. When the RIE bit in the SCR register is 1, an RXI interrupt request is generated.

Figure 26.41 shows a sample flowchart for serial data reception. All the processing steps are automatically performed using an RXI interrupt request to activate the DTC.
In reception, setting the RIE bit to 1 allows an RXI interrupt request to be generated. The DTC is activated by an RXI interrupt request if the RXI interrupt request is specified as a source of DTC activation beforehand, allowing transfer of receive data.
If an error occurs during reception and either the ORER or PER flag in the SSR register is set to 1, a receive error interrupt (ERI) request is generated. Clear the error flag after the error occurrence. If an error occurs, the DTC is not activated and receive data is skipped. Therefore, the number of bytes of receive data specified in the DTC is transferred.
Even if a parity error occurs and the PER flag is set to 1 during reception, receive data is transferred to RDR, thus allowing the data to be read.
When a reception is forcibly terminated by setting the SCR.RE bit to 0 during operation, read the RDR register because the received data which has not yet been read may be left in RDR.

Note 1. For operations in block transfer mode, refer to section 26.3, Operation in Asynchronous Mode.

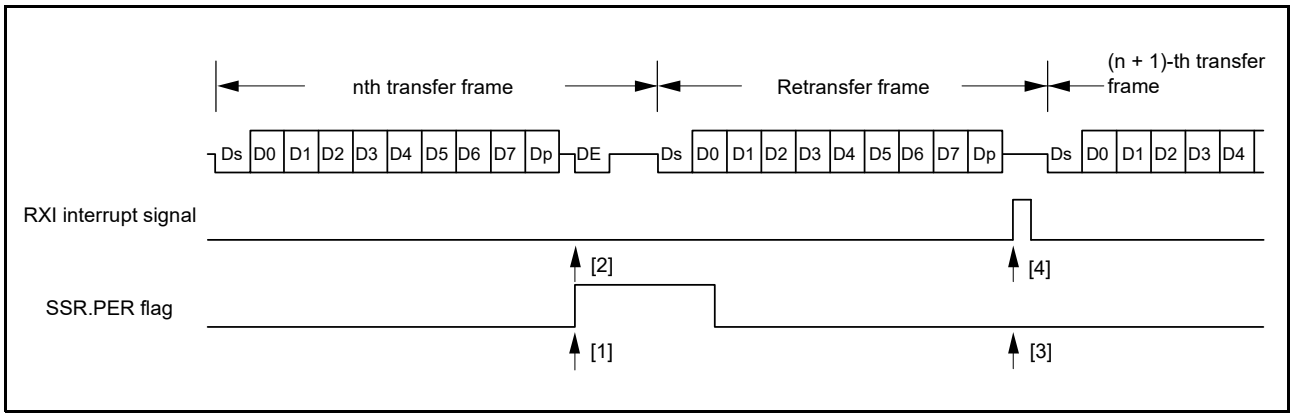


Figure 26.40 Data Retransfer Operation in SCI Reception Mode (Data Retransfer Operation during Reception)

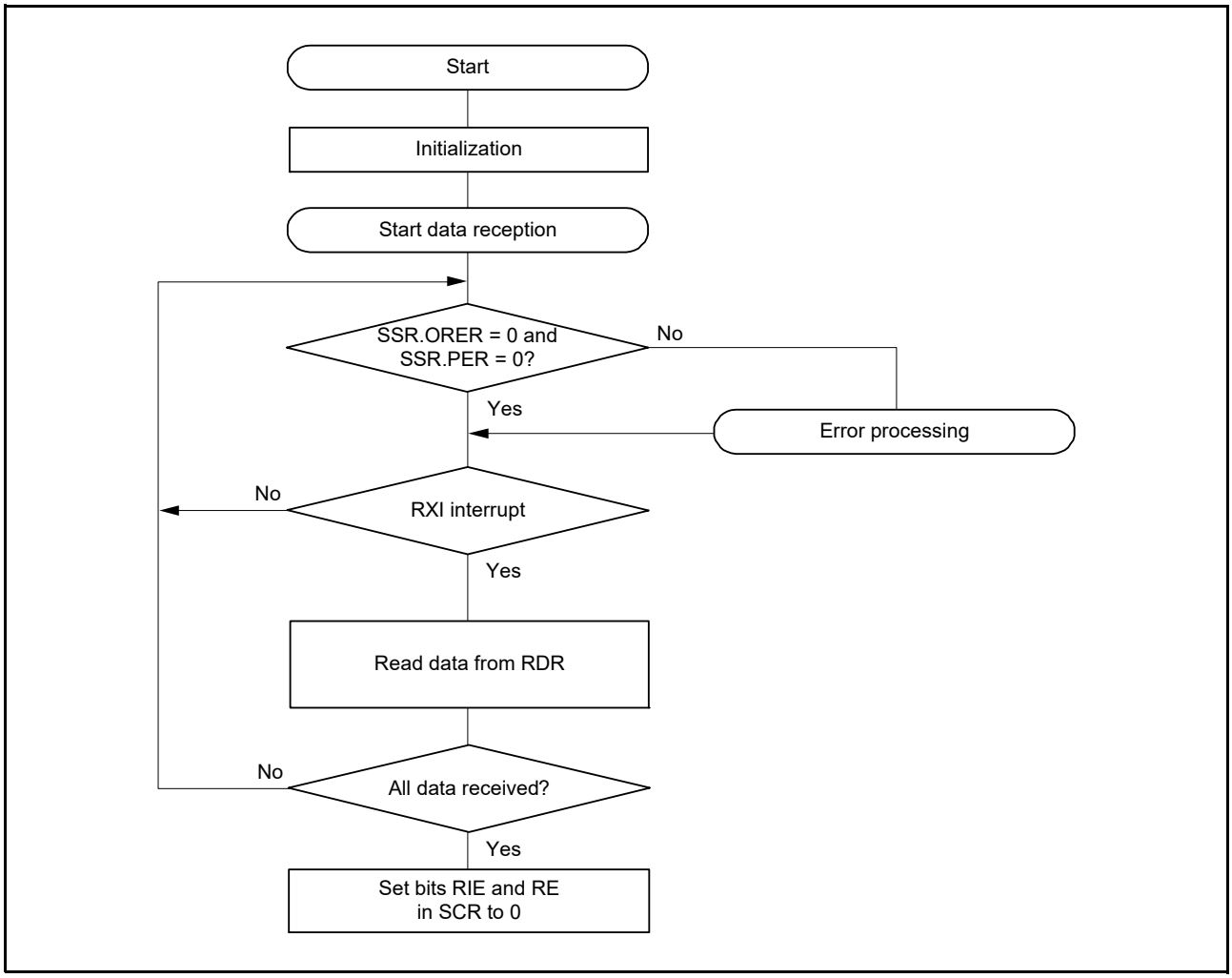


Figure 26.41 Sample Smart Card Interface Reception Flowchart

26.6.8 Clock Output Control

Clock output can be fixed using the CKE[1:0] bits in the SCR register when the GM bit in the SMR register is 1. Specifically, the minimum width of a clock pulse can be specified.

Figure 26.42 shows an example of clock output fixing timing when the CKE[0] bit is controlled with GM = 1 and CKE[1] = 0.

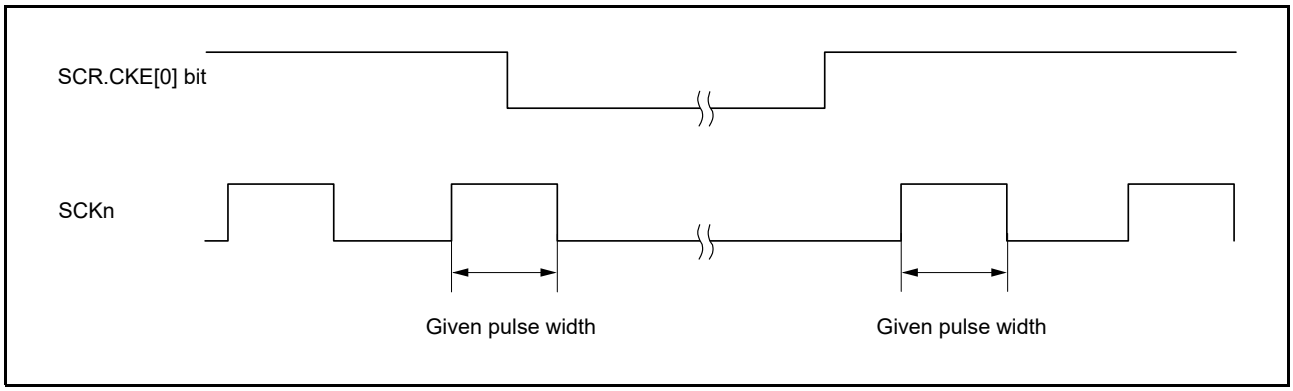


Figure 26.42 Clock Output Fixing Timing

To secure the appropriate clock duty cycle simultaneously with power-on, use the following procedure.

1. Initially, port input is enabled in the high-impedance state. To fix the potential level, use a pull-up or pull-down resistor.
2. Fix the SCKn pin to the specified output by setting the SCR.CKE[1] bit and I/O port functions.
3. Set SMR and SCMR to enable smart card interface mode.
4. Set the SCR.CKE[0] bit to 1 to start clock output.

26.7 Operation in Simple I2C Mode

Simple I2C-bus format is composed of 8 data bits and an acknowledge bit. By continuing into a slave-address frame after a start condition or restart condition, a master device is able to specify a slave device as the partner for communications. The currently specified slave device remains valid until a new slave device is specified or a stop condition is satisfied.
The 8 data bits in all frames are transmitted in order from the MSB.
The I2C format and timing of the I2C-bus are shown in Figure 26.43 and Figure 26.44.

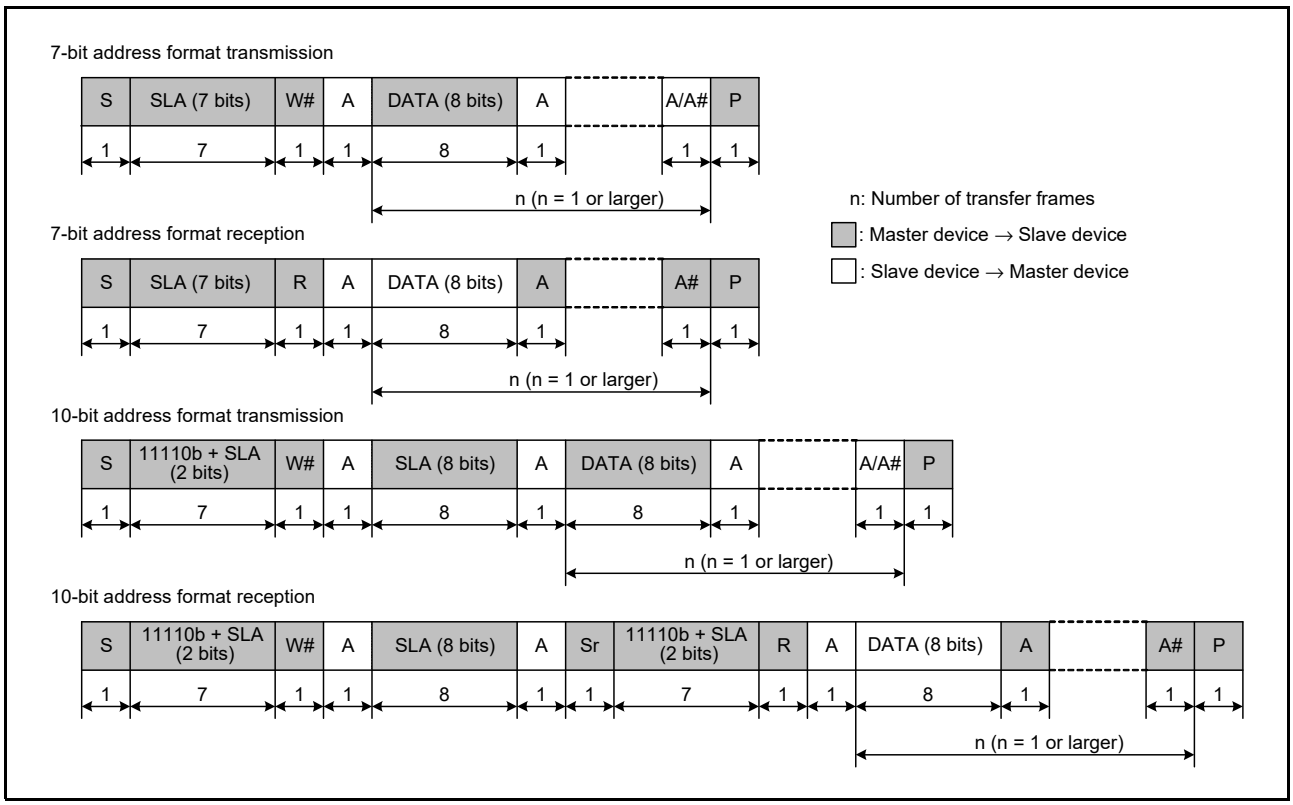


Figure 26.43 I2C-bus Format

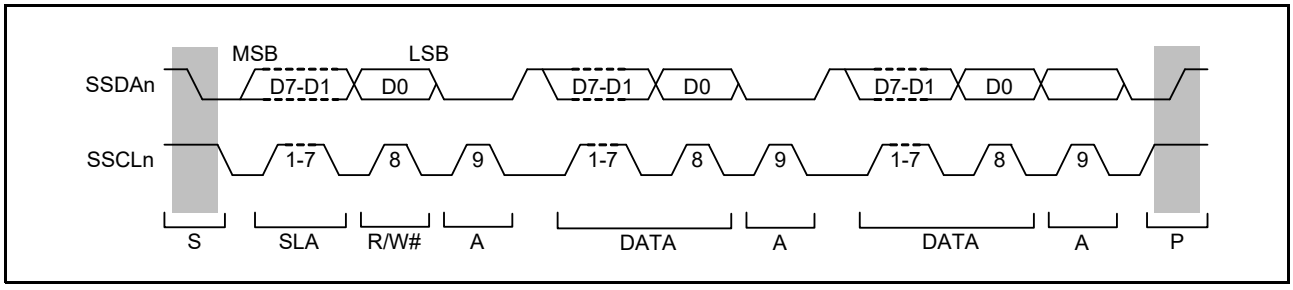


Figure 26.44 I2C-bus Timing (When SLA is 7 Bits)

S: Indicates a start condition, i.e. the master device changing the level on the SSDAn line from the high to the low level while the SSCLn line is at the high level.
SLA: Indicates a slave address, by which the master device selects a slave device.
R/W#: Indicates the direction of transfer (reception or transmission). The value 1 corresponds to transfer from the slave device to the master device and 0 corresponds to transfer from the master device to the slave device.
A/A#: Indicates an acknowledge bit. This is returned by the slave device for master transmission and by the master device for master reception. Return of the low level indicates ACK and return of the high level indicates NACK.
Sr: Indicates a restart condition, i.e. the master device changing the level on the SSDAn line from the high to the low level while the SSCLn line is at the high level and after the setup time has elapsed.
DATA: Indicates the data being received or transmitted.
P: Indicates a stop condition, i.e. the master device changing the level on the SSDAn line from the low to the high level while the SSCLn line is at the high level.

26.7.1 Generation of Start, Restart, and Stop Conditions

Writing 1 to the IICSTAREQ bit in the SIMR3 register causes the generation of a start condition. The generation of a start condition proceeds through the following operations.

- The level on the SSDAn line falls (from the high level to the low level) and the SSCLn line is kept in the released state.
- The hold time for the start condition is secured as half of a bit period at the bit rate determined by the setting of the BRR.
- The level on the SSCLn line falls (from the high level to the low level), the IICSTAREQ bit in the SIMR3 register is set (to 0), and a start-condition generated interrupt is output.

Writing 1 to the IICRSTAREQ bit in the SIMR3 register causes the generation of a start condition. The generation of a start condition proceeds through the following operations.

- The SSDAn line is released and the SSCLn line is kept at the low level.
- The period at low level for the SSCLn line is secured as half of a bit period at the bit rate determined by the setting of the BRR.
- The SSCLn line is released (transition from the low to the high level).
- Once the high level on the SSCLn line is detected, the setup time for the restart condition is secured as half of a bit period at the bit rate determined by the setting of the BRR.
- The level on the SSDAn line falls (from the high level to the low level).
- The hold time for the restart condition is secured as half of a bit period at the bit rate determined by the setting of the BRR.
- The level on the SSCLn line falls (from the high level to the low level), the IICRSTAREQ bit in the SIMR3 register is set (to 0), and a restart-condition generated interrupt is output.

Writing 1 to the IICSTPREQ bit in the SIMR3 register causes the generation of a stop condition. The generation of a stop condition proceeds through the following operations.

- The level on the SSDAn line falls (from the high level to the low level) and the SSCLn line is kept at the low level.
- The period at low level for the SSCLn line is secured as half of a bit period at the bit rate determined by the setting of the BRR.
- The SSCLn line is released (transition from the low to the high level).
- Once the high level on the SSCLn line is detected, the setup time for the stop condition is secured as half of a bit period at the bit rate determined by the setting of the BRR.
- The SSDAn is released (transition from the low to the high level), the IICSTPREQ bit in the SIMR3 register is set (to 0), and a stop-condition generated interrupt is output.

Figure 26.45 shows the timing of operations in the generation of start, restart, and stop conditions.

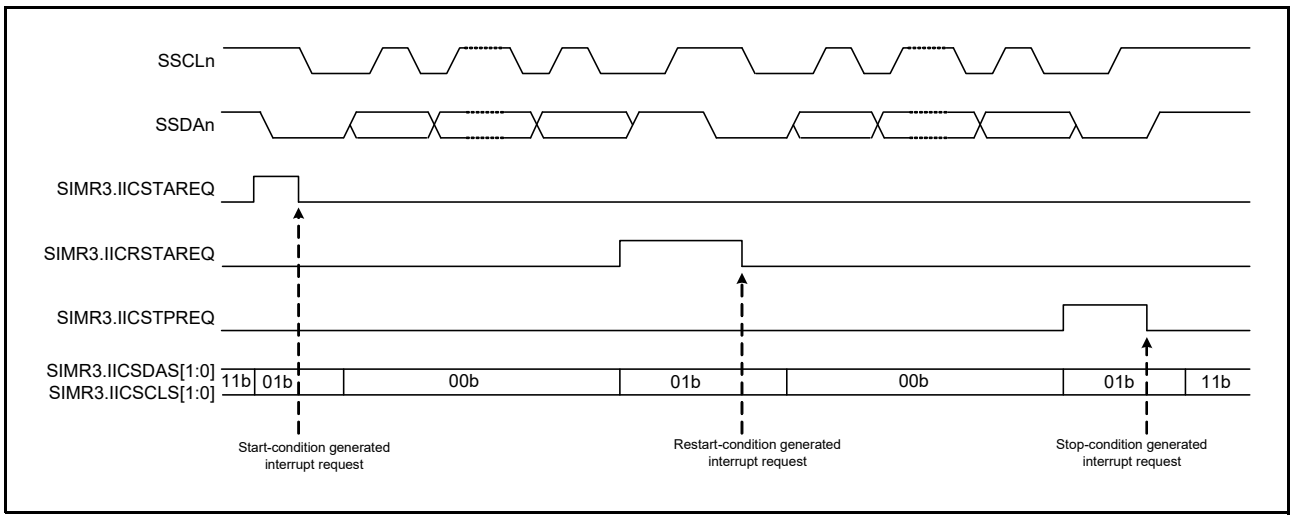


Figure 26.45 Timing of Operations in the Generation of Start, Restart, and Stop Conditions

26.7.2 Clock Synchronization

The SSCLn line may be placed at the low level in the case of a wait inserted by a slave device as the other side of transfer. Setting the IICCSC bit in the SIMR2 register to 1 applies control to obtain synchronization when the levels of the internal SSCLn clock signal and the level being input on the SSCLn pin differ.

When the IICCSC bit in the SIMR2 register is set to 1, the level of the internal SSCLn clock signal changes from low to high, counting to determine the period at high level is stopped while the low level is being input on the SSCLn pin, and counting to determine the period at high level starts after the transition of the input on the SSCLn pin to the high level. The interval from this time until counting to determine the period at high level starts on the transition of the SSCLn pin to the high level is the total of the delay of SSCLn output, delay for noise filtering of the input on the SSCLn pin (2 or 3 cycles of sampling clock for the noise filter), and delay for internal processing (1 or 2 cycles of PCLK). The period at high level of the internal SSCLn clock is extended even if other devices are not placing the low level on the SSCLn line.

If the IICCSC bit in the SIMR2 register is 1, synchronization is obtained for the transmission and reception of data by taking the logical AND of the input on the SSCLn pin and the internal SSCLn clock. If the IICCSC bit in the SIMR2 register is 0, synchronization with the internal SSCLn clock is obtained for the transmission and reception of data.

If a slave device inserts a period of waiting into the interval until the transition of the internal SSCLn clock signal from the low to the high level after a request for the generation of a start, restart, or stop condition is issued, the time until generation is prolonged by that period.

If a slave device inserts a period of waiting after the transition of the internal SSCLn clock signal from the low to the high level, although the generation-completed interrupt is issued without stopping the period of waiting, generation of the condition itself is not guaranteed. Figure 26.46 shows an example of operations to synchronize the clocks.

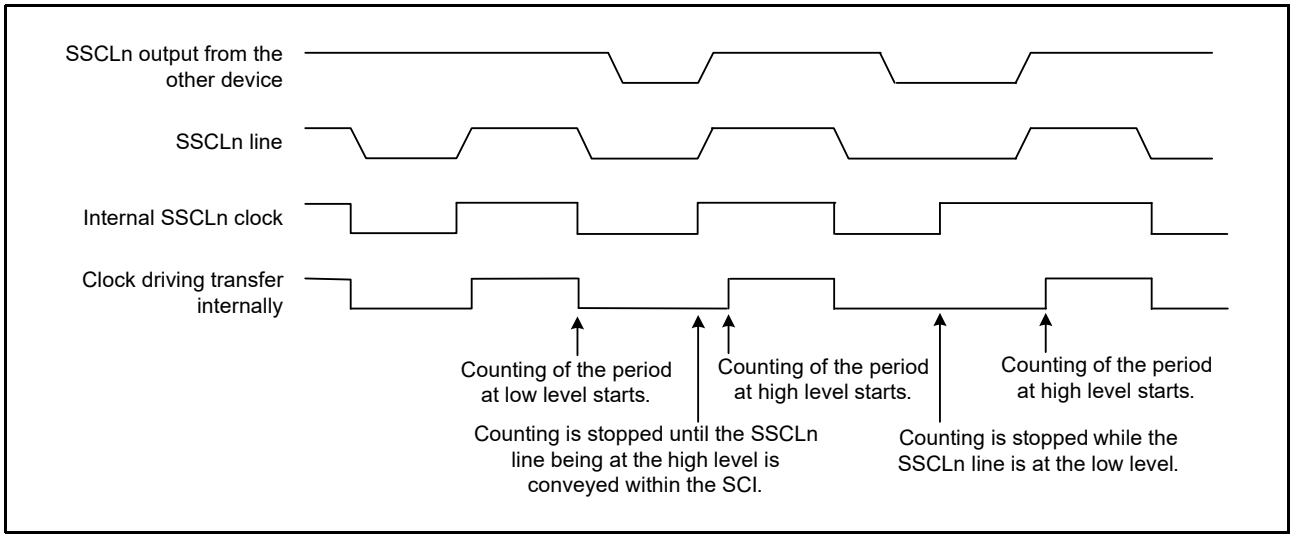


Figure 26.46 Example of Operations for Clock Synchronization

26.7.3 SSDA Output Delay

The IICDL[4:0] bits in the SIMR1 register can be used to set a delay for output on the SSDAn pin relative to falling edges of output on the SSCLn pin. Delay-time settings from 0 to 31 are selectable, representing periods of the corresponding numbers of cycles of the clock signal from the on-chip baud rate generator (derived by frequency-dividing the base clock, PCLK, by the divisor selected by the CKS[1:0] bits in the SMR register). A delay for output on the SSDAn pin is for the start condition/restart condition/stop condition signal, 8-bit transmit data, and an acknowledge bit. If the SSDA output delay is shorter than the time for the level on the SSCLn pin to fall, the change of the output on the SSDAn pin will start while the output level on the SSCLn pin is falling, creating a possibility of erroneous operation for slave devices. Ensure that settings for the delay of output on the SSDAn pin are for times greater than the time output on the SSCLn pin takes to fall (300 ns for I^2C in normal mode and fast mode).

Figure 26.47 shows the timing of delays in SSDA output.

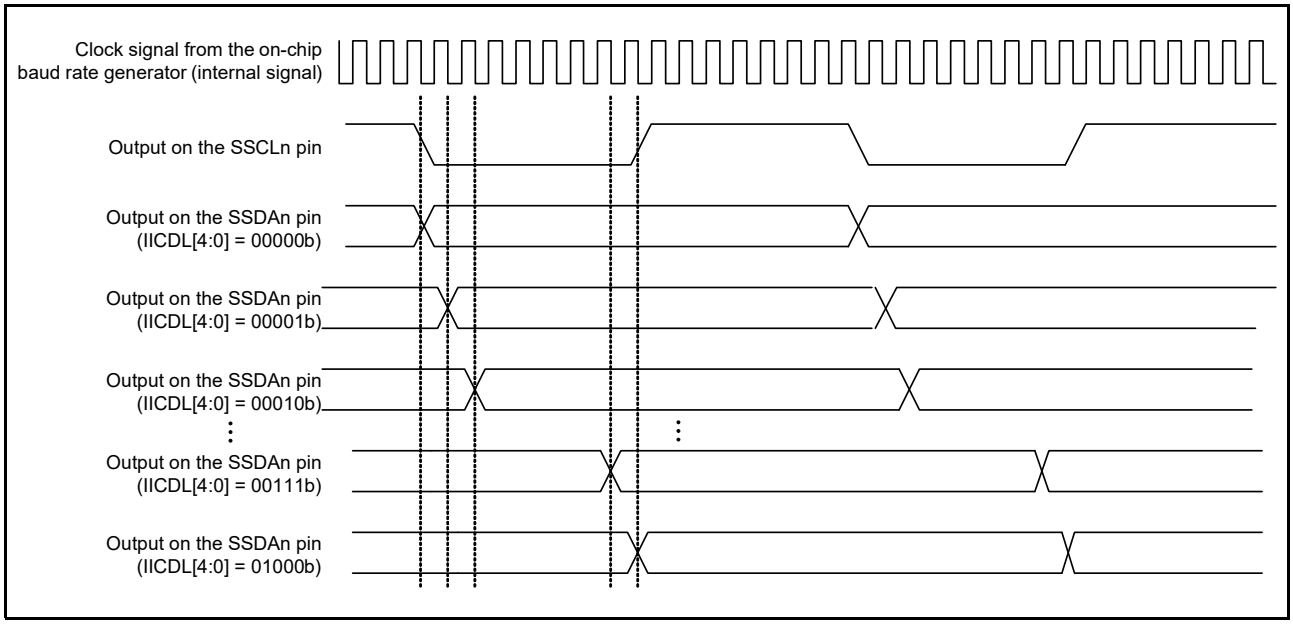


Figure 26.47 Timing of Delays in SSDA Output

26.7.4 SCI Initialization (Simple I2C Mode)

Before transferring data, write the initial value (00h) to SCR and initialize the interface following the example shown in Figure 26.48.

When changing the operating mode, transfer format, and so on, be sure to set SCR to its initial value before proceeding with the changes.

In simple I2C mode, the open-drain setting for the communication ports should be made on the port side.

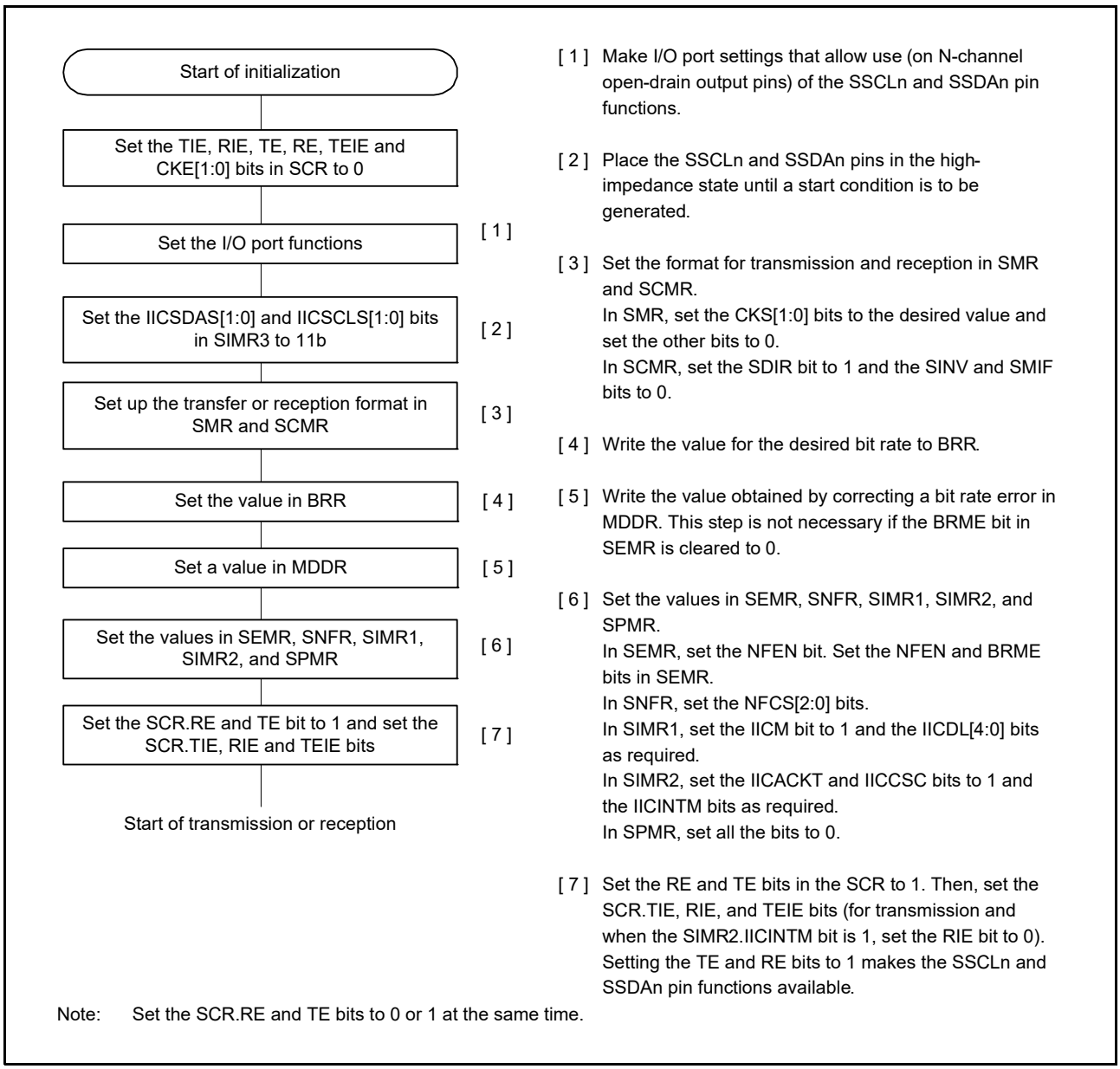


Figure 26.48 Example of the Flowchart of SCI Initialization (for Simple I2C Mode)

26.7.5 Operation in Master Transmission (Simple I2C Mode)

Figure 26.49 and Figure 26.50 show examples of operations in master transmission and Figure 26.51 is a flowchart showing the procedure for data transmission. Refer to Table 26.29 for more information on the STI interrupt.
When 10-bit slave addresses are in use, steps [3] and [4] in Figure 26.51 are repeated twice.
In simple I2C mode, the transmit data empty interrupt (TXI) is generated when communication of one frame is completed, unlike the TXI interrupt request generation timing during clock synchronous transmission.

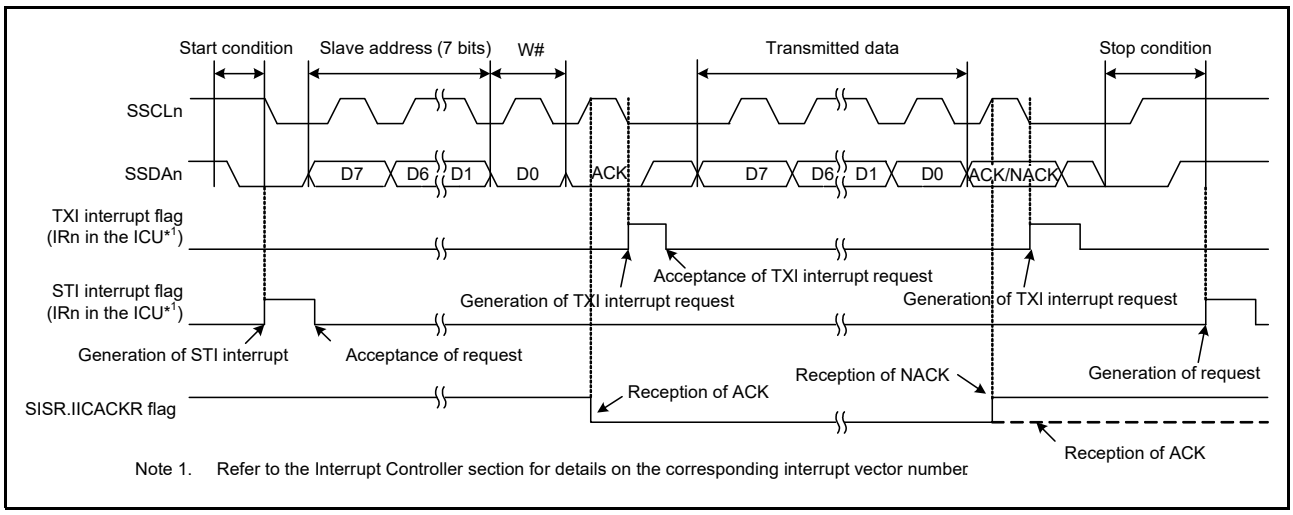


Figure 26.49 Example 1 of Operations for Master Transmission in Simple I2C-bus Mode (with 7-Bit Slave Addresses, Transmission Interrupts, and Reception Interrupts in Use)

When the SIMR2.IICINTM bit is set to 0 (use ACK/NACK interrupts) during master transmission, the DTC is activated by the ACK interrupt as the trigger and necessary number of data bytes are transmitted. When the NACK is received, error processing, such as transmission stop and retransmission, is performed by the NACK interrupt as the trigger.

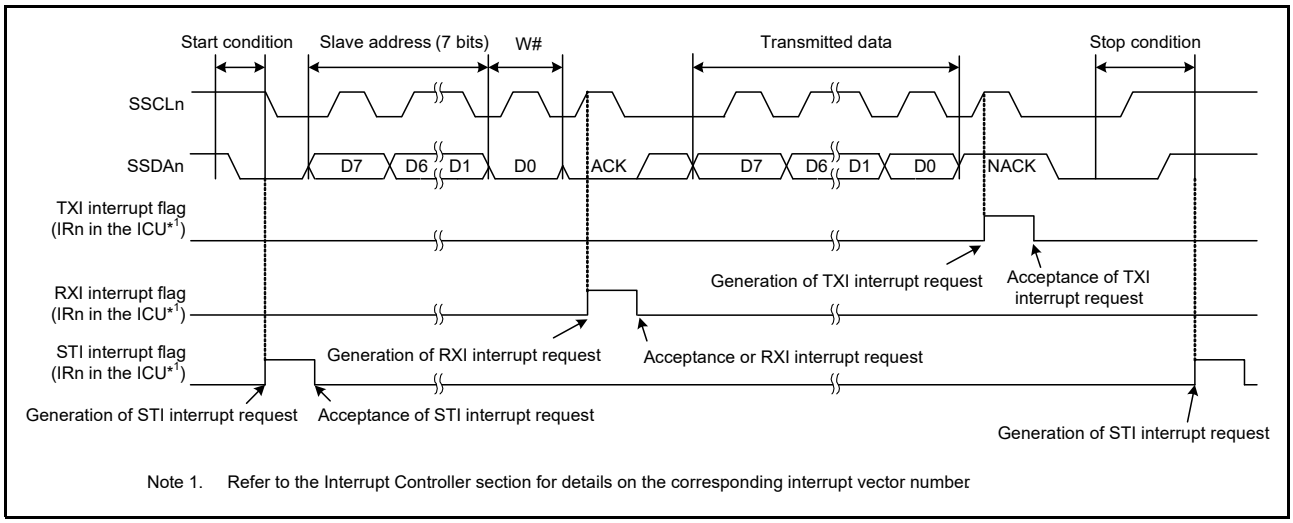
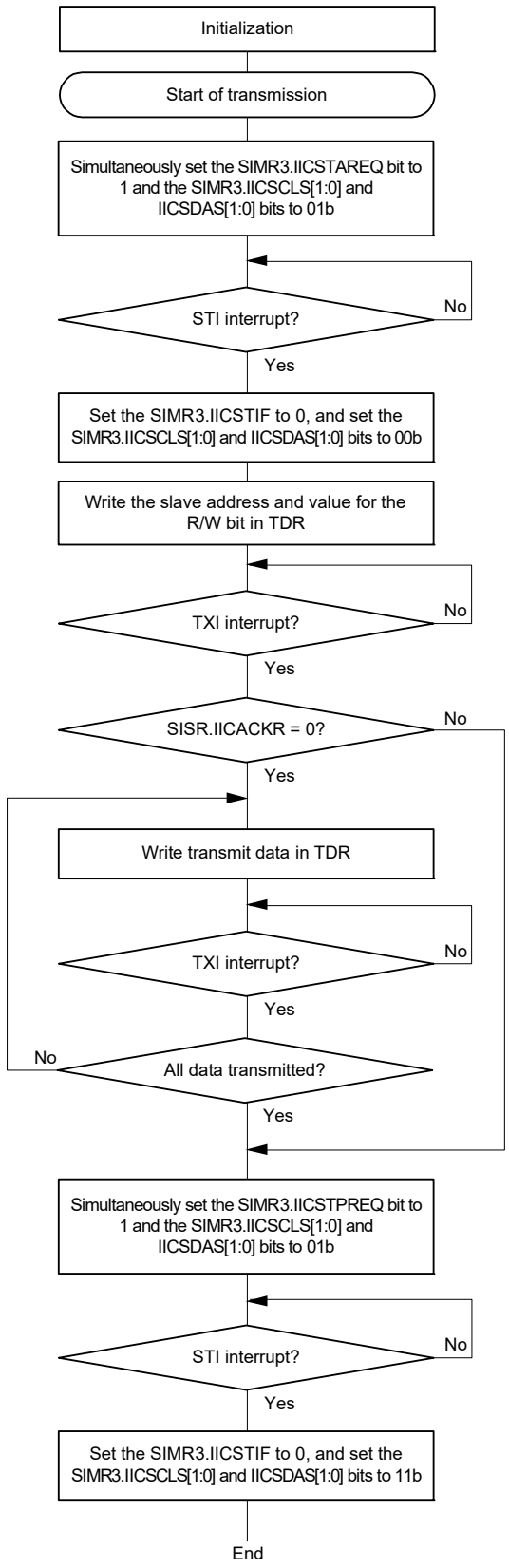


Figure 26.50 Example 2 of Operations for Master Transmission in Simple I2C-bus Mode (with 7-Bit Slave Addresses, ACK Interrupts, and NACK Interrupts in Use)



[1] Initialization for simple I²C mode
For transmission, set the SCR.RIE bit to 0 (RXI and ERI interrupts requests are disabled)

[2] Generate a start condition.

[3] Writing to TDR:
Writing the slave address and value for the R/W bit to TDR.

[4] Confirming ACK response from the slave address:
Check the SISR.IICACKR bit. If its value is 0, it is indicated that the slave device responded with ACK and operations proceed. If its value is 1, it is indicated that there was no response from a slave device so the next transition is to generation of the stop condition.

[5] Steps for continuing with serial transmission:
When transmission is to continue, write further transmit data to TDR. Except for the first data to be transmitted, a TXI request can activate the DTC to handle writing of data to TDR.

[6] Generation of a stop condition.

[3] and [4]: If 10-bit slave addresses are in use, processing of [3] and [4] is repeated twice.

Note: In simple I²C mode, the TXI interrupt request is generated when communication is completed, unlike the timing during clock synchronous transmission.

Figure 26.51 Example of the Procedure for Master Transmission Operations in Simple I²C Mode (with Transmission Interrupts and Reception Interrupts in Use)

26.7.6 Master Reception (Simple I2C Mode)

Figure 26.52 shows an example of operations in simple I2C mode master reception and Figure 26.53 is a flowchart showing the procedure for master reception.
The value of the SIMR2.IICINTM bit is assumed to be 1 (use reception and transmission interrupts).
In simple I2C mode, the transmit data empty interrupt (TXI) is generated when communication of one frame is completed, unlike the TXI interrupt request generation timing during clock synchronous transmission.

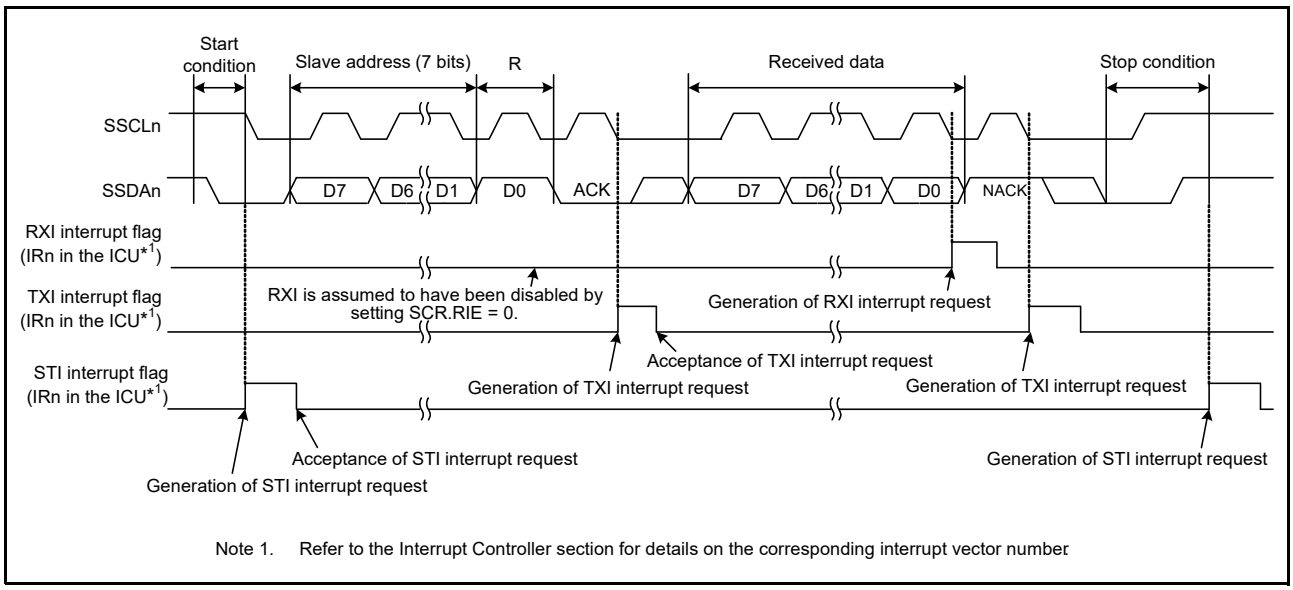
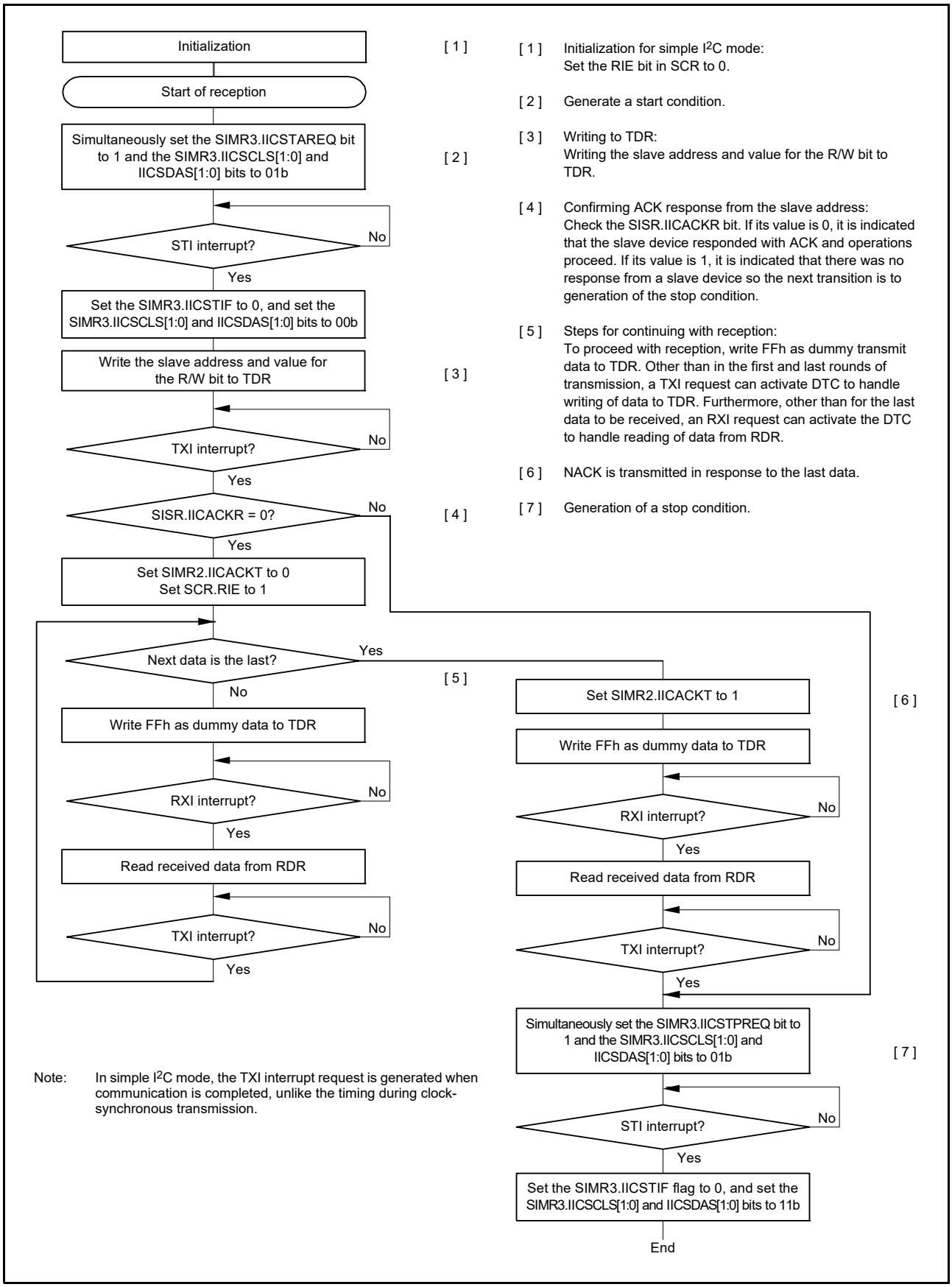


Figure 26.52 Example of Operations for Master Reception in Simple I2C-bus Mode (with 7-Bit Slave Addresses, Transmission Interrupts, and Reception Interrupts in Use)



[1] Initialization for simple I²C mode:
Set the RIE bit in SCR to 0.

[2] Generate a start condition.

[3] Writing to TDR:
Writing the slave address and value for the R/W bit to TDR.

[4] Confirming ACK response from the slave address:
Check the SISR.IICACKR bit. If its value is 0, it is indicated that the slave device responded with ACK and operations proceed. If its value is 1, it is indicated that there was no response from a slave device so the next transition is to generation of the stop condition.

[5] Steps for continuing with reception:
To proceed with reception, write FFh as dummy transmit data to TDR. Other than in the first and last rounds of transmission, a TXI request can activate DTC to handle writing of data to TDR. Furthermore, other than for the last data to be received, an RXI request can activate the DTC to handle reading of data from RDR.

[6] NACK is transmitted in response to the last data.

[7] Generation of a stop condition.

Note: In simple I²C mode, the TXI interrupt request is generated when communication is completed, unlike the timing during clock-synchronous transmission.

Figure 26.53 Example of the Procedure for Master Reception Operations in Simple I²C Mode (with Transmission Interrupts and Reception Interrupts in Use)

26.8 Operation in Simple SPI Mode

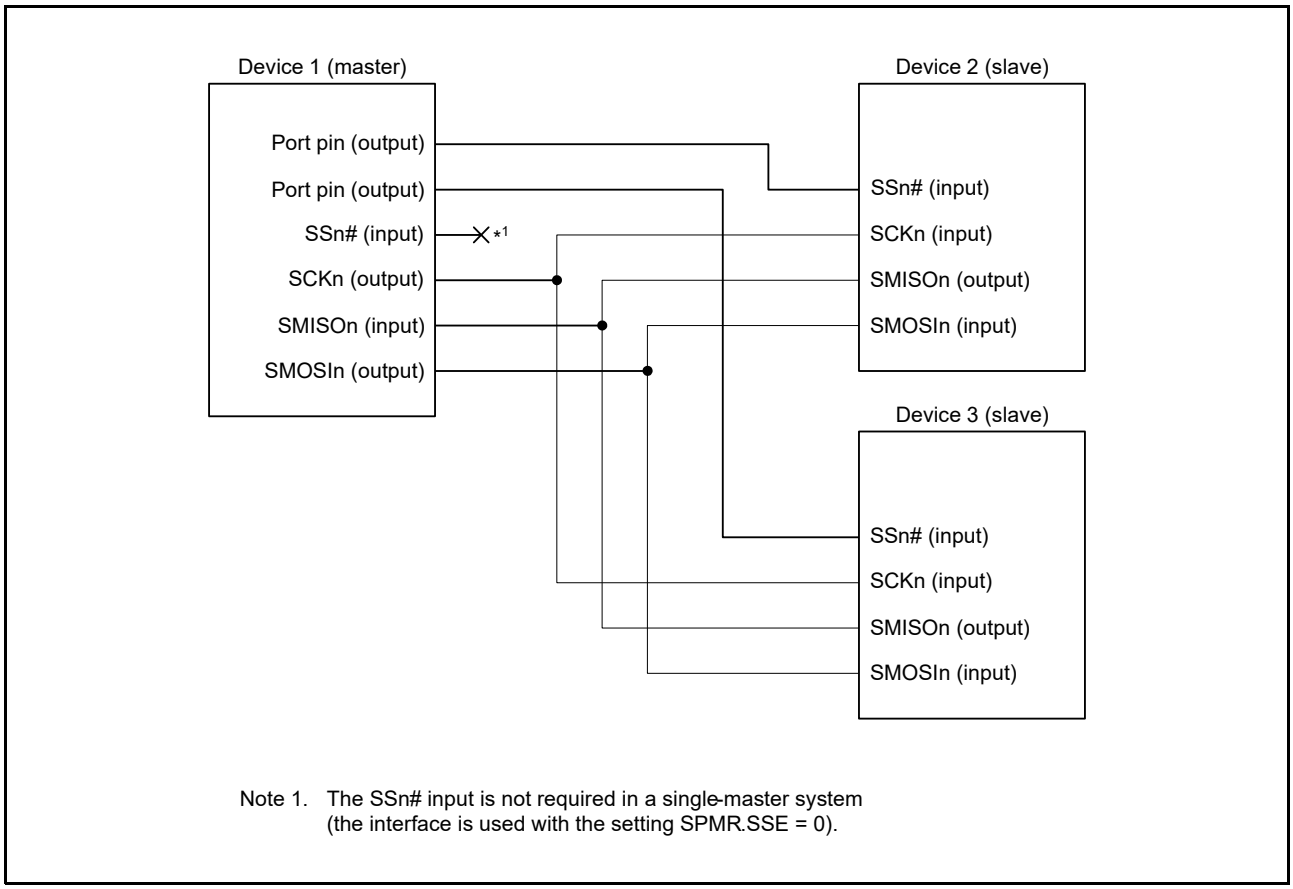
As an extended function, the SCI supports a simple SPI mode that handles transfer among one or multiple master devices and multiple slave devices.

Making the settings for clock synchronous mode (SCMR.SMIF = 0, SIMR1.IICM = 0, SMR.CM = 1) plus setting the SSE bit in the SPMR to 1 places the SCI in simple SPI mode. However, the SS pin function on the master side is unnecessary for connection of the device used as the master in simple SPI mode when the configuration only has a single master, so set the SSE bit in the SPMR to 0 in such cases.

Figure 26.54 shows an example of connections for simple SPI mode. Control a general port pin to produce the SS output signal from the master.

In simple SPI mode, data are transferred in synchronization with clock pulses in the same way as in clock synchronous mode. One character of data for transfer consists of 8 bits of data, and parity bits cannot be appended to this. The data can be inverted by setting the SCMR.SINV bit to 1.

Since the receiver and transmitter are independent of each other within the SCI module, full-duplex communications are possible, with a common clock signal. Furthermore, since both the transmitter and receiver have a double-buffered structure, writing of further transmit data while transmission is in progress and reading of previously received data while reception is in progress are both possible. Continuous transfer is thus possible.



Note 1. The SSn# input is not required in a single-master system (the interface is used with the setting SPMR.SSE = 0).

Figure 26.54 Example of Connections via a Simple SPI Mode (In Single Master Mode, SPMR.SSE Bit = 0)

26.8.1 States of Pins in Master and Slave Modes

The direction (input or output) of pins for the simple SPI mode interface differs according to whether the device is a master (SCR.CKE[1:0] = 00b or 01b and SPMR.MSS = 0) or slave (SCR.CKE[1:0] = 10b or 11b and SPMR.MSS = 1). Table 26.26 lists the states of pins according to the mode and the level on the SSn# pin.

Table 26.26 States of Pins by Mode and Input Level on the SSn# Pin

Mode	Input on SSn# Pin	State of SMOSIn Pin	State of SMISOn Pin	State of SCKn Pin
Master mode*1	High level (transfer can proceed)	Output for data transmission*2	Input for received data	Clock output*3
	Low level (transfer cannot proceed)	High-impedance	Input for received data (but disabled)	High-impedance
Slave mode	High level (transfer can proceed)	Input for received data (but disabled)	High-impedance	Clock input (but disabled)
	Low level (transfer cannot proceed)	Input for received data	Output for data transmission	Clock input

Note 1. When there is only a single master (SPMR.SSE = 0), transfer is possible regardless of the input level on the SSn# pin (this is equivalent to input of a high level on the SSn# pin). Since the SSn# pin function is not required, the pin is available for other purposes.
Note 2. The SMOSIn pin output is in the high-impedance state when serial transmission is disabled (SCR.TE bit = 0).
Note 3. The SCKn pin output is in the high-impedance state when serial transmission is disabled (SCR.TE and RE bits = 00b) in a multi-master configuration (SPMR.SSE = 1).

26.8.2 SS Function in Master Mode

Setting the CKE[1:0] bits in the SCR to 00b and the MSS bit in the SPMR to 0 selects master operation. The SSn# pin is not used in single-master configurations (SPMR.SSE = 0), so transmission or reception can proceed regardless of the value of the SSn# pin.

When the level on the SSn# pin is high in a multi-master configuration (SPMR.SSE = 1), a master device outputs clock signals from the SCKn pin before starting transmission or reception to indicate that there are no other masters or another master is performing reception or transmission. When the level on the SSn# pin is low in a multi-master configuration (SPMR.SSE = 1), there are other masters, and this indicates that transmission or reception is in progress. At this time the SMOSIn output and SCKn pins will be placed in the high-impedance state and starting transmission or reception will not be possible. Furthermore, the value of the SPMR.MFF bit will be 1, indicating a mode fault error. In a multi-master configuration, start error processing by reading SPMR.MFF flag. Also, even if a mode fault error occurs while transmission or reception is in progress, transmission or reception will not be stopped, but the SMOSIn and SCKn pin output will be placed in the high-impedance state after the completion of the transfer.

Control a general port pin to produce the SS output signal from the master.

26.8.3 SS Function in Slave Mode

Setting the CKE[1:0] bits in the SCR to 10b and the MSS bit in the SPMR to 1 selects slave operation. When the level on the SSn# pin is high, the SMISOn output pin will be in the high-impedance state and clock input through the SCKn pin will be ignored. When the level on the SSn# pin is low, clock input through the SCKn pin will be effective and transmission or reception can proceed.

If the input on the SSn# pin changes from low to high level during transmission or reception, the SMISOn output pin will be placed in the high-impedance state. Meanwhile, the internal processing for transmission or reception will continue at the rate of the clock input through the SCKn pin until processing for the character currently being transmitted or received is completed, after which it stops. At that time, an interrupt (the appropriate one from among TXI, RXI, and TEI) will be generated.

26.8.4 Relationship between Clock and Transmit/Receive Data

The CKPOL and CKPH bits in the SPMR can be used to set up the clock for use in transmission and reception in four different ways. The relation between the clock signal and the transmission and reception of data is shown in Figure 26.55. The relation is the same for both master and slave operation.

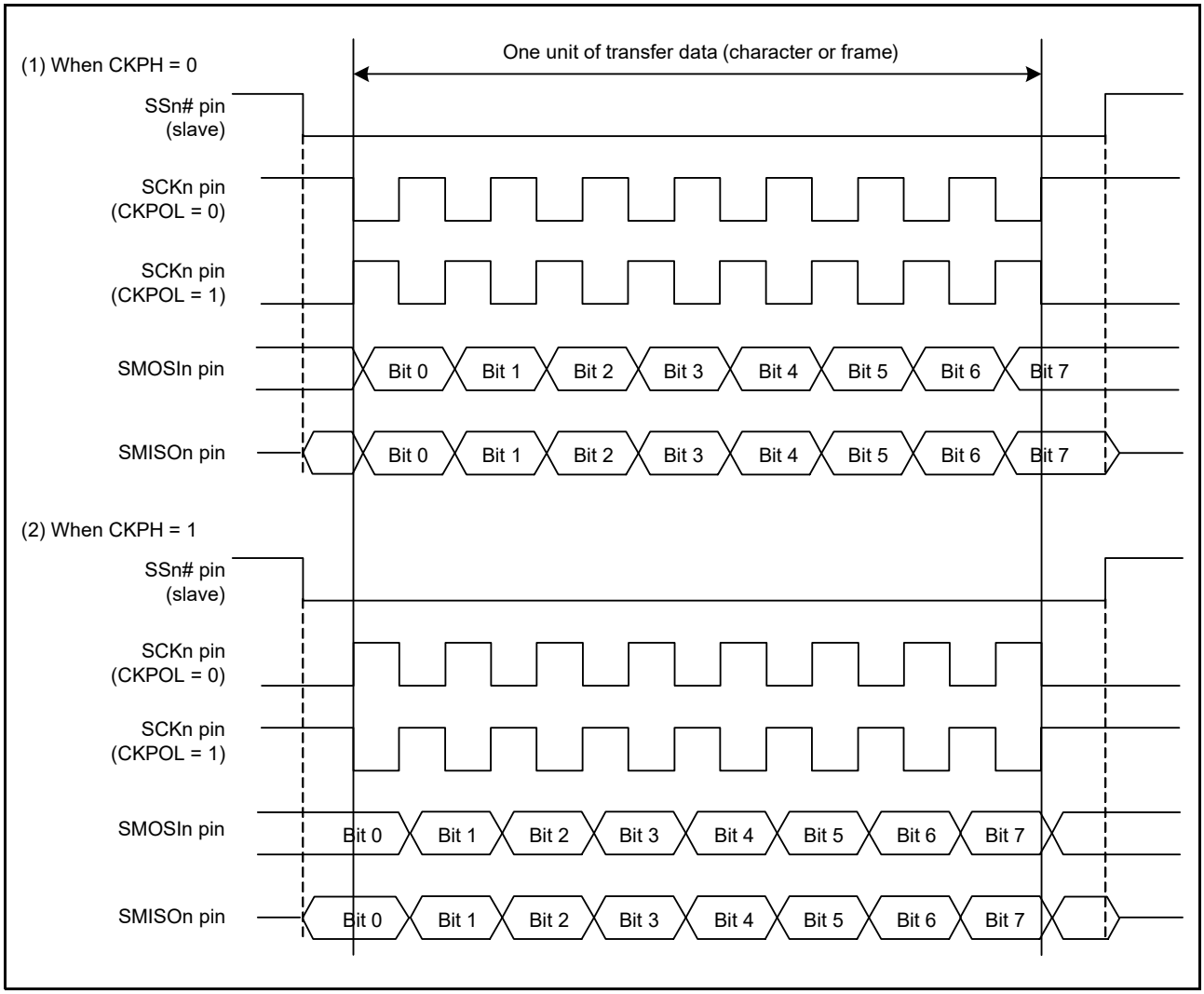


Figure 26.55 Relation between Clock Signal and Transmit/Receive Data in Simple SPI Mode

26.8.5 SCI Initialization (Simple SPI Mode)

The procedure is the same as for initialization in clock synchronous mode Figure 26.22, Sample SCI Initialization Flowchart. The CKPOL and CKPH bits in the SPMR must be set to ensure that the kind of clock signal they select is suitable for both master and slave devices.
For initialization, changes to the operating mode, changes to the transfer format, and so on, initialize the SCR register before proceeding with changes.
As well as setting the RE bit to 0, note that the SSR.ORER, FER, and PER flags, as well as the RDR, are not initialized. Note that changing the value of the TE bit from 1 to 0 or from 0 to 1 will lead to the generation of a transmit data empty interrupt (TXI) if the value of the TIE bit in the SCR is 1 at the time.

26.8.6 Transmission and Reception of Serial Data (Simple SPI Mode)

In master operation, ensure that the SSn# pin of the slave device on the other side of the transfer is at the low level before starting the transfer and at the high level on completion of the transfer. Otherwise, the procedures are the same as in clock synchronous mode.

26.9 Bit Rate Modulation Function

The bit rate modulation function corrects the bit rate by thinning out the specified amount of clocks from those input to the baud rate generator.
When the SEMR.BRME bit is 1, the baud rate generator validates and counts the average interval of the number of clocks set in the MDDR register out of the total 256 clocks input.
Figure 26.56 assumes the SCI is in asynchronous mode, bits SMR.CKS[1:0] are 00b, the BRR register is 00h, and the MDDR register is 160. In this example, the cycle of the base clock is evenly corrected to 256/160, and the bit rate is corrected to 160/256. Note that there is an imbalance in thinning out the internal clock, and expansion and contraction occur in the pulse width of the internal base clock.

Note: Do not use this function in clock synchronous mode and in the highest speed settings in simple SPI mode (SMR.CKS[1:0] = 00b, SCR.CKE[1] = 0, and BRR = 0).

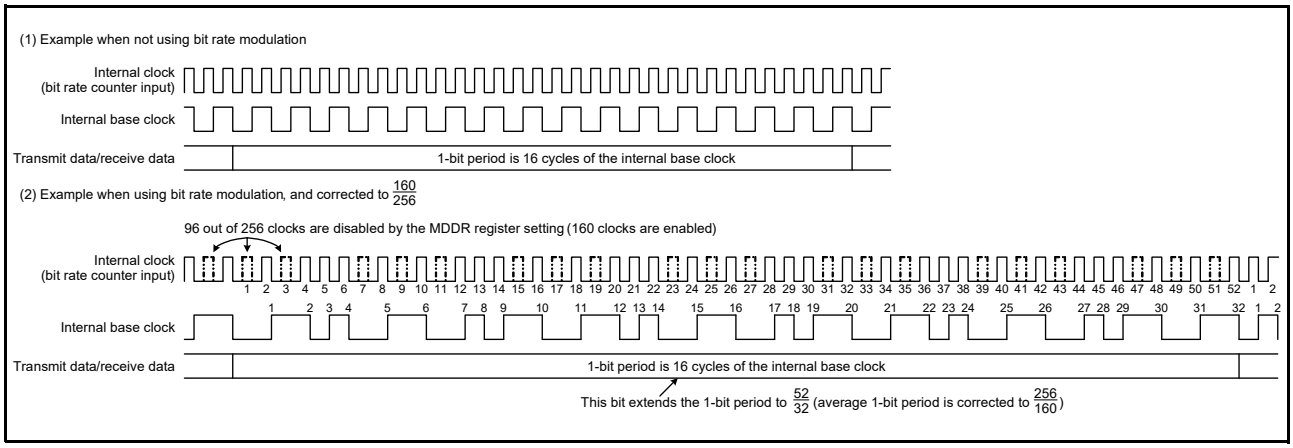


Figure 26.56 Example of the Base Clock When the Bit Rate Modulation Function is Used

26.10 Noise Cancellation Function

Figure 26.57 shows the configuration of the noise filter used for noise cancellation. The noise filter consists of two stages of flip-flop circuits and a match-detection circuit. When the level on the pin matches in three consecutive samples taken at the set sampling interval, the matching level continues to be conveyed internally until the level on the pin again matches in three consecutive samples.

In asynchronous mode, the noise cancellation function can be applied on the RXDn input signal. The period of the base clock (1/16th of a bit-period when SEMR.ABCS = 0 and 1/8th of a bit-period when SEMR.ABCS = 1) is the sampling interval.

In simple I^2C mode, the noise cancellation function can be applied on the SSDAn and SSCLn input signals. The sampling clock is the clock signal produced by frequency-dividing the signal from the clock source for the internal baud-rate generator by one, two, four, or eight as selected by the setting of the SNFR.NFCS[2:0] bits.

If the base clock is stopped with the noise filter enabled and then the clock input is started again, the noise filter operation resumes from where the clock was stopped. If SCR.TE and SCR.RE are set to 0 during base clock input, all of the noise filter flip-flop values are initialized to 1. Accordingly, if the input data is 1 when reception operation resumes, it is determined that a level match is detected and is conveyed to the internal signal. When the level being input corresponds to 0, the initial output of the noise filter is retained until the level matches in three consecutive samples.

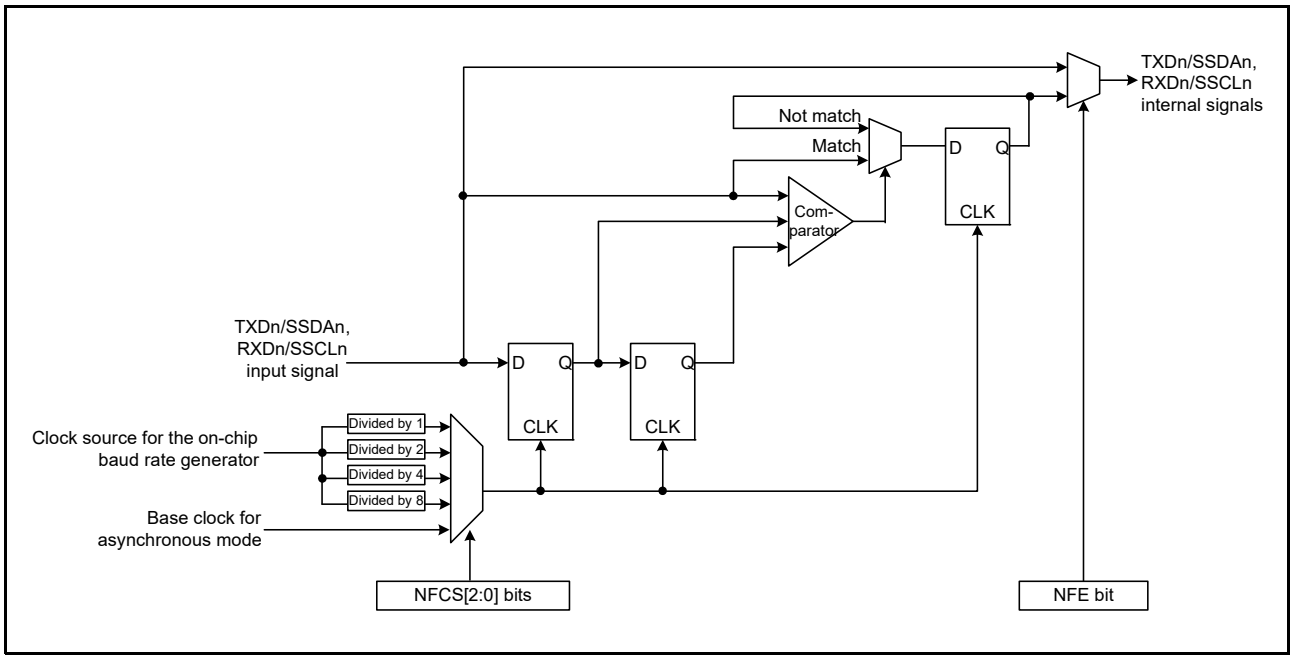


Figure 26.57 Block Diagram of Digital Noise Filter Circuit

26.11 Interrupt Sources

26.11.1 Buffer Operations for TXI and RXI Interrupts

If the conditions for a TXI and RXI interrupt are satisfied while the interrupt status flag in the interrupt controller is 1, the SCI does not output the interrupt request but retains it internally (with a capacity for retention of one request per source). When the value of the interrupt status flag in the interrupt controller becomes 0, the interrupt request retained within the SCI is output. The internally retained interrupt request is automatically discarded once the actual interrupt is output. Clearing of the corresponding interrupt enable bit (the TIE or RIE bit in the SCR) can also be used to discard an internally retained interrupt request.

26.11.2 Interrupts in Asynchronous Mode, Clock Synchronous Mode, and Simple SPI Mode

Table 26.27 lists interrupt sources in asynchronous mode, clock synchronous mode, and simple SPI mode. A different interrupt vector is assigned to each interrupt source, and individual interrupt sources can be enabled or disabled with the enable bits in the SCR register.

If the SCR.TIE bit is 1, a TXI interrupt request is generated when transmit data is transferred from the TDR or TDRL register*1 to the TSR. A TXI interrupt request can also be generated by setting the SCR.TE bit to 1 after setting the SCR.TIE bit to 1 or by using a single instruction to set the SCR.TE and SCR.TIE bit to 1 at the same time. A TXI interrupt request can activate the DTC to handle data transfer.

A TXI interrupt request is not generated by setting the SCR.TE bit to 1 while the setting of the SCR.TIE bit is 0 or by setting the SCR.TIE bit to 1 while the setting of the SCR.TE bit is 1.*2

When new data is not written by the time of transmission of the last bit of the current transmit data and the setting of the SCR.TEIE bit is 1, the SSR.TEND flag becomes 1 and a TEI interrupt request is generated. Furthermore, when the setting of the SCR.TE bit is 1, the SSR.TEND flag retains the value 1 until further transmit data are written to the TDR or TDRL register*1, and setting the SCR.TEIE bit to 1 leads to the generation of a TEI interrupt request.

Writing data to the TDR or TDRL register*1 leads to clearing of the SSR.TEND flag and, after a certain time, discarding of the TEI interrupt request.

If the SCR.RIE bit is 1, an RXI interrupt request is generated when received data is stored in the RDR. An RXI interrupt request can activate the DTC to handle data transfer.

Setting of any from among the ORER, FER, and PER flags in the SSR to 1 while the SCR.RIE bit is 1 leads to the generation of an ERI interrupt request. An RXI interrupt request is not generated at this time. Clearing all three flags (ORER, FER, and PER) leads to discarding of the ERI interrupt request.

Note 1. In the case where asynchronous mode and 9-bit data length are selected

Note 2. To temporarily disable TXI interrupts at the time of transmission of the last of the data and so on when you wish a new round of transmission to start after handling of the transmission-completed interrupt, control disabling and enabling of the interrupt by using the interrupt request enable bit in the interrupt controller rather than using the SCR.TIE bit. This can prevent the suppression of TXI interrupt requests in the transfer of new data.

Table 26.27 Interrupt Sources

Name	Interrupt Source	Interrupt Flag	DTC Activation	Priority
ERI	Receive error	ORER, FER, or PER	Not possible	High
RXI	Receive data full	RDRF	Possible	↑
TXI	Transmit data empty	TDRE	Possible	
TEI	Transmit end	TEND	Not possible	Low

26.11.3 Interrupts in Smart Card Interface Mode

Table 26.28 lists interrupt sources in smart card interface mode. A transmit end interrupt (TEI) request cannot be used in this mode.

Table 26.28 SCI Interrupt Sources

Name	Interrupt Source	Interrupt Flag	DTC Activation	Priority
ERI	Receive error or error signal detection	ORER, PER, or ERS	Not possible	High
RXI	Receive data full	—	Possible	↑
TXI	Transmit data empty	TEND	Possible	Low

Data transmission/reception using the DTC is also possible in smart card interface mode, similar to in the normal SCI mode. In transmission, when the TEND flag in the SSR register is set to 1, a TXI interrupt request is generated. This TXI interrupt request activates the DTC allowing transfer of transmit data if the TXI request is specified beforehand as a source of DTC activation. The TEND flag is automatically set to 0 when the DTC transfers the data.
If an error occurs, the SCI automatically retransmits the same data. During the retransmission, the TEND flag is kept to 0 and the DTC is not activated. Therefore, the SCI and DTC automatically transmit the specified number of bytes, including retransmission in the case of error occurrence. However, the ERS flag in the SSR register is not automatically cleared to 0 at error occurrence. Therefore, the ERS flag must be cleared by previously setting the RIE bit in the SCR register to 1 to enable an ERI interrupt request to be generated at error occurrence.
When transmitting/receiving data using the DTC, be sure to make settings to enable the DTC before making SCI settings. For DTC settings, refer to section 17, Data Transfer Controller (DTCa).
In reception, an RXI interrupt request is generated when receive data is set to RDR. This RXI interrupt request activates the DTC allowing transfer of receive data if the RXI request is specified beforehand as a source of DTC activation. If an error occurs, the error flag is set. Therefore, the DTC is not activated and an ERI interrupt request is issued to the CPU instead; the error flag must be cleared.

26.11.4 Interrupts in Simple I2C Mode

The interrupt sources in simple I2C mode are listed in Table 26.29. The STI interrupt is allocated to the transmit end interrupt (TEI) request. The receive error interrupt (ERI) request cannot be used.
The DTC can also be used to handle transfer in simple I2C mode.
When the value of the IICINTM bit in the SIMR2 register is 1, an RXI request will be generated on the falling edge of the SSCLn signal for the eighth bit. If the RXI has been set up as an activating request for the DTC beforehand, the RXI request will activate the DTC to handle transfer of the received data. Furthermore, a TXI request is generated on the falling edge of the SSCLn signal for the ninth bit (acknowledge bit). If the TXI has been set up as an activating request for the DTC beforehand, the TXI request will activate the DTC to handle transfer of the transmit data.
When the value of the IICINTM bit in the SIMR2 register is 0, an RXI request (ACK detection) if the input on the SSDAn pin is at the low level or a TXI request (NACK detection) if the input on the SSDAn pin is at the high level will be generated on the rising edge of the SSCLn signal for the ninth bit (acknowledge bit). If the RXI has been set up as an activating request for the DTC beforehand, the RXI request will activate the DTC to handle transfer of the received data. Also, if the DTC is used for data transfer in reception or transmission, be sure to set up and enable the DTC before setting up the SCI.
When the IICSTAREQ, IICRSTAREQ, and IICSTPREQ bits in the SIMR3 register are used to generate a start condition, restart condition, or stop condition, the STI request is issued when generation is complete.

Table 26.29 SCI Interrupt Sources

Name	Interrupt Source		Interrupt Flag	DTC Activation	Priority
	IICINTM bit = 0	IICINTM bit = 1			
RXI	ACK detection	Reception	—	Possible	High
TXI	NACK detection	Transmission	—	Possible*1	↑
STI	Completion of generation of a start, restart, or stop condition		IICSTIF	Not possible	Low

Note 1. Activation of the DTC is only possible when the SIMR2.IICINTM bit is 1 (use reception and transmission interrupts).

26.12 Usage Notes

26.12.1 Setting the Module Stop Function

Module stop control register B (MSTPCRB) and module stop control register C (MSTPCRC) are used to stop and start SCI operations. With the value after a reset, SCI operations are stopped. Register access is enabled by releasing the module stop state. For details, refer to section 11, Low Power Consumption.

26.12.2 Break Detection and Processing

When a framing error is detected, a break can be detected by reading the RXDn pin value directly. In a break, the input from the RXDn pin becomes all 0s, and so the FER flag in the SSR register is set to 1 (framing error has occurred), and the PER flag in the SSR register may also be set to 1 (parity error has occurred). When the SEMR.RXDESEL bit is 0, the SCI continues the receive operation even after a break is received. Therefore, note that even if the FER flag is set to 0 (no framing error occurred), it will be set to 1 again. When the SEMR.RXDESEL bit is 1, the SCI sets the SSR.FER flag to 1 and stops receiving operation until a start bit of the next data frame is detected. If the SSR.FER flag is set to 0 at this time, the SSR.FER flag retains 0 during the break. When the RXDn pin becomes high and the break ends, detecting the beginning of the start bit at the first falling edge of the RXDn pin allows the SCI to start the receiving operation.

26.12.3 Mark State and Generating Breaks

When the SCR.TE bit is 0 (serial transmission is disabled), setting the I/O port function makes selection of the level and direction (input or output) of the TXDn pin possible. If this is done, the TXDn pin can be placed in the mark state to send a break at the time of data transmission. Until the SCR.TE bit is set to 1 (serial transmission is enabled), the I/O port function is used to set the TXDn pin to output high and set the pin mode to a general I/O port pin, and thus place the communication line in the mark state (state of having the value 1). On the other hand, to output a break at the time of data transmission, set the TXDn pin to output low and make the pin mode settings for a general I/O port pin. When the SCR.TE bit is set to 0, the transmitter is initialized regardless of the current state of transmission.

26.12.4 Receive Error Flags and Transmit Operations (Clock Synchronous Mode and Simple SPI Mode)

Transmission cannot be started when a receive error flag (ORER) in the SSR register is set to 1, even if data is written to the TDR register. Be sure to set the receive error flags to 0 before starting transmission. Note also that the receive error flags cannot be set to 0 even if the RE bit in the SCR register is set to 0 (serial reception is disabled).

26.12.5 Writing Data to the TDR Register

Data can be written to registers TDR, TDRH, and TDRL. However, if new data is written to registers TDR, TDRH, and TDRL when transmit data is remaining in registers TDR, TDRH, and TDRL, the previous data in registers TDR, TDRH, and TDRL is lost because it has not been transferred to the TSR register yet. Be sure to write transmit data to registers TDR, TDRH, and TDRL in the TXI interrupt request handling routine.

26.12.6 Restrictions on Clock Synchronous Transmission (Clock Synchronous Mode and Simple SPI Mode)

When the external clock source is used as a synchronization clock, the following restrictions apply.

(1) Start of transmission

Update TDR by the CPU or DTC and wait for at least five PCLK cycles (at least 10 PCLK cycles for SCI11) before allowing the transmit clock to be input (refer to Figure 26.58).

(2) Continuous transmission

(a) Write the next transmit data to TDR or TDRL before the falling edge of the transmit clock (bit 7) (refer to Figure 26.58).

(b) When updating TDR after bit 7 has started to transmit, update TDR while the synchronization clock is in the low-level period, and set the high-level width of the transmit clock (bit 7) to four PCLK cycles (eight PCLK cycles for SCI11) or longer (refer to Figure 26.58).

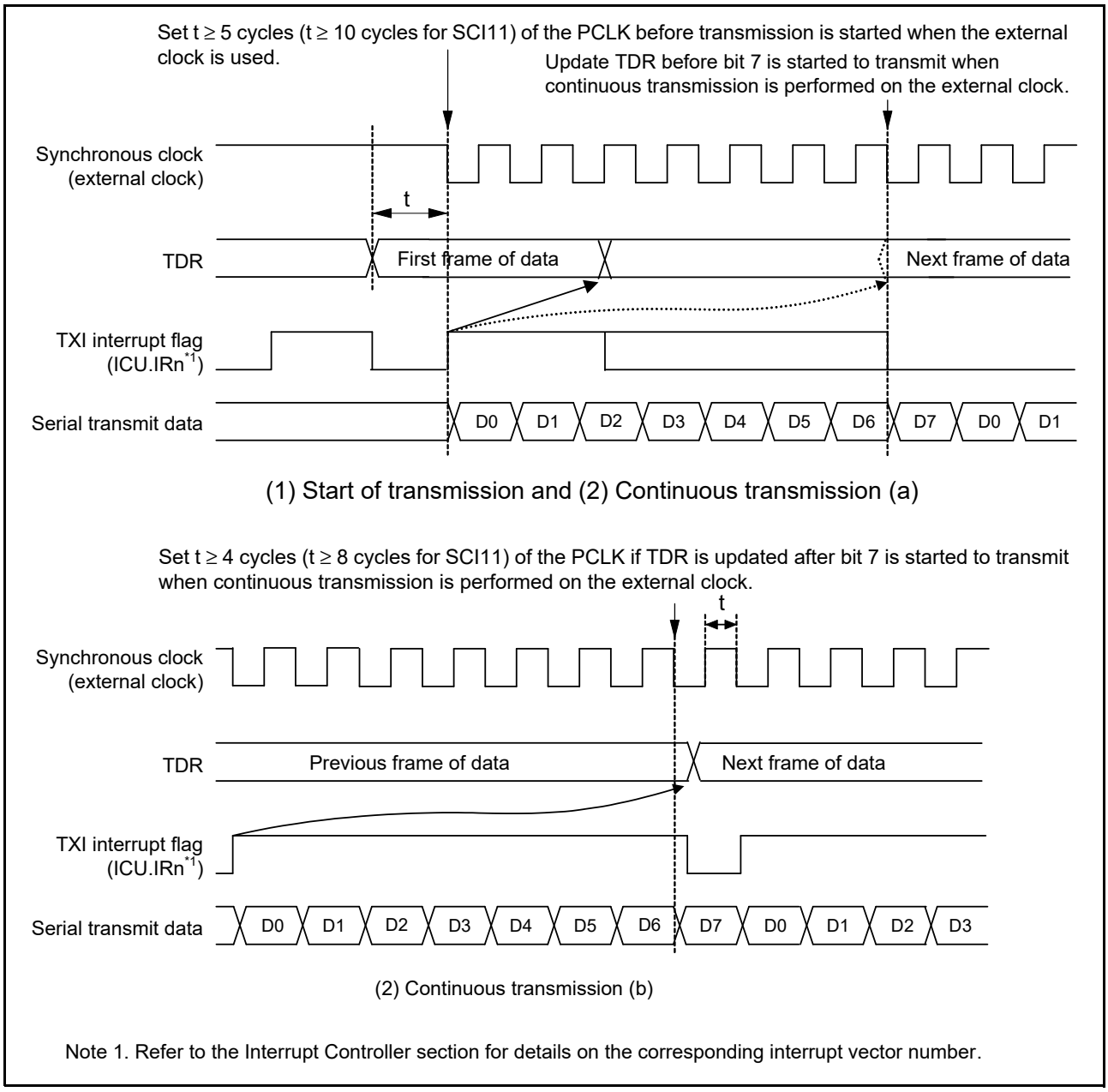


Figure 26.58 Restrictions on Use of External Clock in Clock Synchronous Transmission

26.12.7 Restrictions on Using DTC

When using the DTC to read RDR, RDRH, and RDRL, be sure to set the receive data full interrupt (RXI) as the activation source of the relevant SCI.

26.12.8 Notes on Starting Transfer

At the point where transfer starts when the interrupt status flag (IRn.IR bit) in the interrupt controller is 1, follow the procedure below to clear interrupt requests before permitting operations (by setting the SCR.TE or SCR.RE bit to 1). For details on the interrupt status flag, refer to section 14, Interrupt Controller (ICUb).

- Confirm that transfer has stopped (the setting of the SCR.TE or SCR.RE bits is 0).
- Set the corresponding interrupt enable bit (SCR.TIE or SCR.RIE) to 0.
- Read the corresponding interrupt enable bit (SCR.TIE or SCR.RIE bit) to check that it has become 0.
- Set the interrupt status flag (IRn.IR bit) in the interrupt controller to 0.

26.12.9 SCI Operations during Low Power Consumption State

(1) Transmission

When making settings for the module stopped state or in transitions to software standby, stop operations (by setting the TIE, TE, and TEIE bits in the SCR to 0) after switching the TXDn pin to the general I/O port pin function. Setting the TE bit to 0 resets the TSR register and the TEND bit in the SSR. Depending on the port settings, output pins may output the level before a transition to the low power consumption state is made after release from the module stopped state or software standby mode. When transitions to these states are made during transmission, the data being transmitted become indeterminate.

To transmit data in the same transmission mode after cancellation of the low power consumption state, set the TE bit to 1, read SSR, and write data to TDR sequentially to start data transmission. To transmit data with a different transmission mode, initialize the SCI first.

Figure 26.59 shows a sample flowchart for transition to software standby mode during transmission. Figure 26.60 and Figure 26.61 show the port pin states during transition to software standby mode.

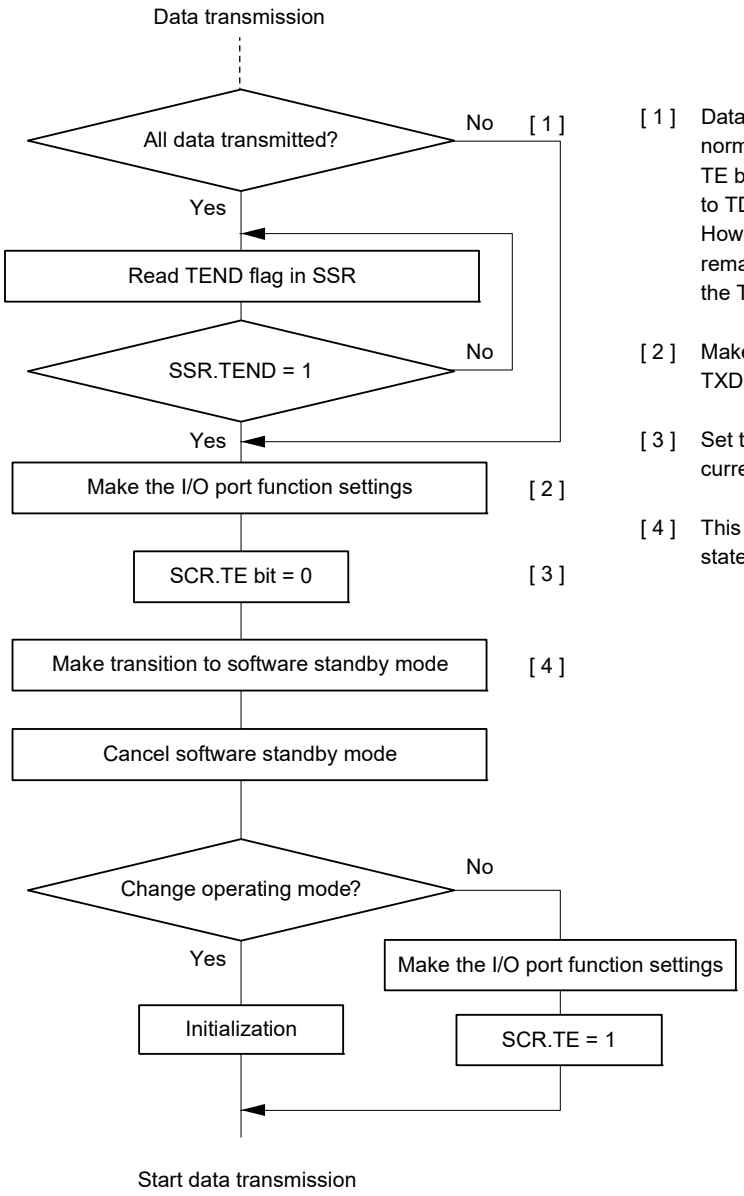
Before specifying the module stop state or making a transition to software standby mode from the transmission mode using DTC transfer, stop the transmit operations (TE = 0). To start transmission after cancellation using the DTC, set the TE and TIE bits to 1. The TXI interrupt flag is set to 1 and transmission starts using the DTC.

(2) Reception

Before specifying the module stop state or making a transition to software standby mode, stop the receive operations (RE = 0 in the SCR register). If transition is made during data reception, the data being received will be invalid.

To receive data in the same reception mode after cancellation of the low power consumption state, set the RE bit to 1, and then start reception. To receive data in a different reception mode, initialize the SCI first.

Figure 26.62 shows a sample flowchart for transition to software standby mode during reception.



[1] Data being transmitted is lost halfway. Data can be normally transmitted from the CPU by setting the TE bit in SCR to 1, reading SSR, and writing data to TDR after canceling software standby mode. However, if the DTC has been activated, the data remaining in the DTC will be transmitted when both the TE and TIE bits in SCR are set to 1.

[2] Make the I/O port function settings to switch the TXDn pin to operate as a general I/O port.

[3] Set the TIE and TEIE bits in the SCR if they are currently set to 1.

[4] This includes the setting for the module stopped state.

Figure 26.59 Example of Flowchart for Transition to Software Standby Mode during Transmission

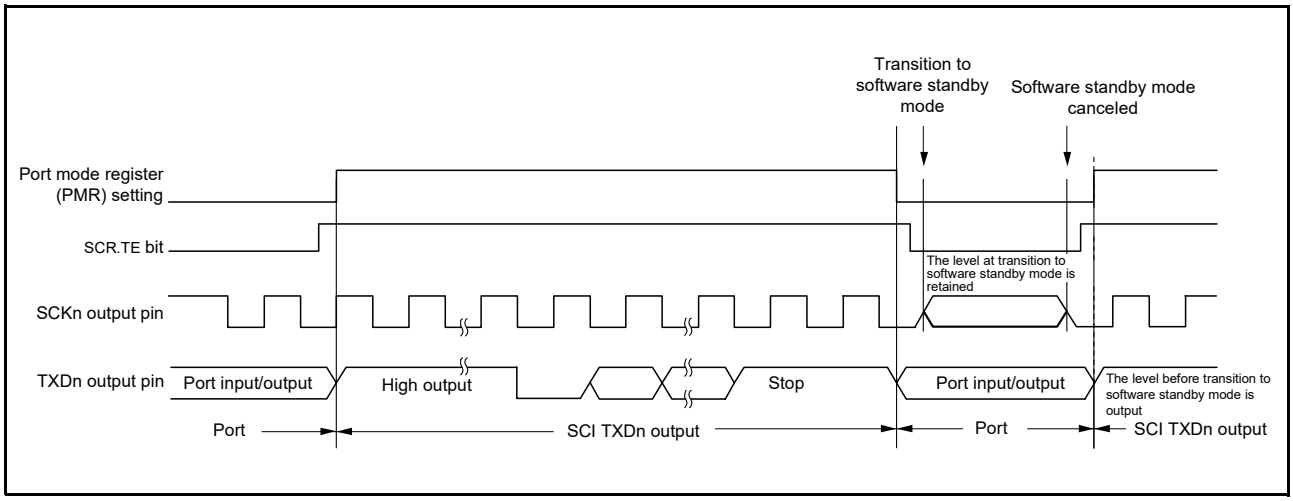


Figure 26.60 Port Pin States during Transition to Software Standby Mode (Internal Clock, Asynchronous Transmission)

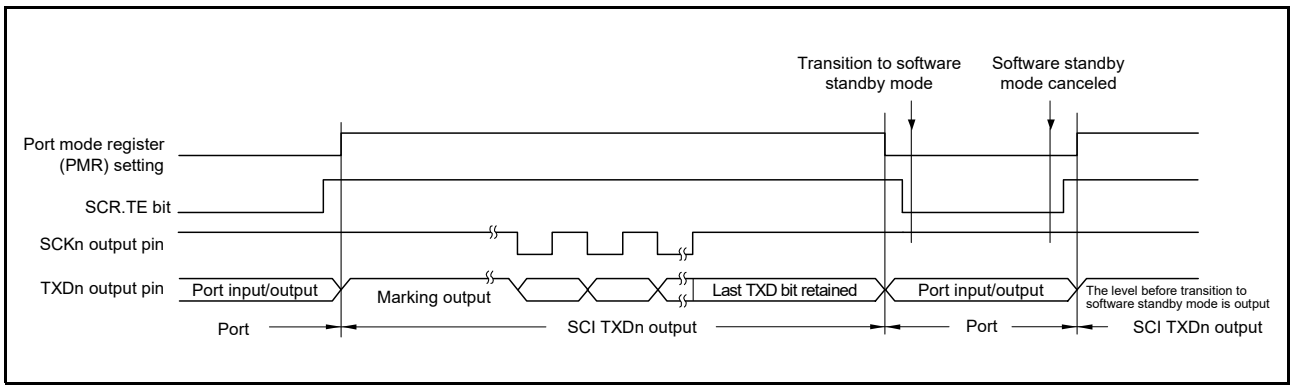


Figure 26.61 Port Pin States during Transition to Software Standby Mode (Internal Clock, Clock Synchronous Transmission)

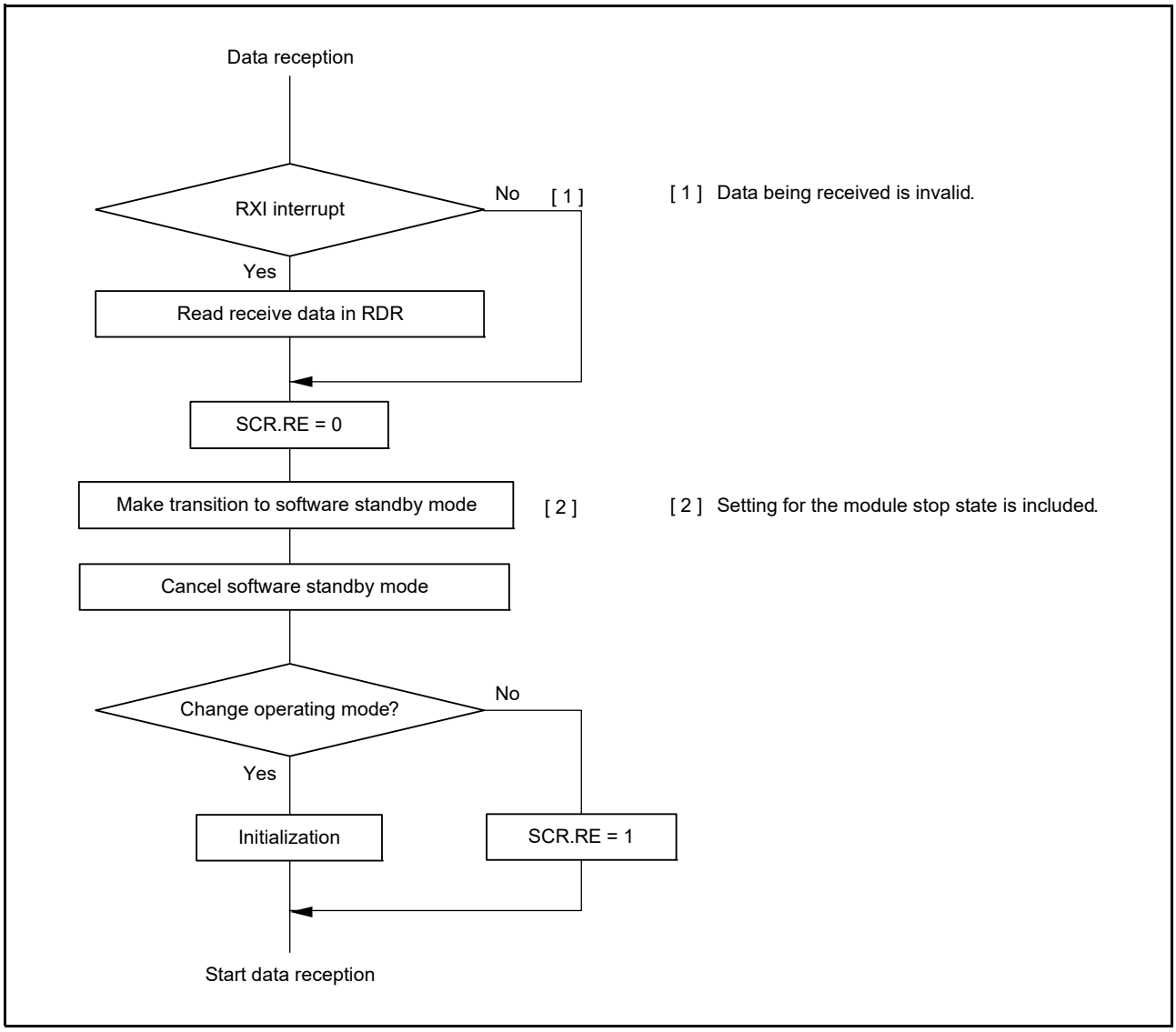


Figure 26.62 Example of Flowchart for Transition to Software Standby Mode during Reception

26.12.10 External Clock Input in Clock Synchronous Mode and Simple SPI Mode

In clock synchronous mode and simple SPI mode, the external clock SCKn must be input as follows:
High-pulse period, low-pulse period = 2 PCLK cycles or more, period = 6 PCLK cycles or more
Refer to the electric characteristics for the condition of the external clock input to SCI11.

26.12.11 Limitations on Simple SPI Mode

(1) Master Mode

- Use a resistor to pull up or pull down the clock line matching the initial settings for the transfer clock set by the SPMR.CKPH and CKPOL bits when the SPMR.SSE bit is 1.
  This prevents the clock line from being placed in the high-impedance state when the SCR.TE bit is set to 0 or unexpected edges from being generated on the clock line when the SCR.TE bit is changed from 0 to 1. When the SPMR.SSE bit is 0 in single master mode, pulling up or pulling down the clock line is not necessary because the clock line is not placed in the high-impedance state even when the SCR.TE bit is set to 0.
- In the case of the setting for clock delay (SPMR.CKPH bit is 1), the receive data full interrupt (RXI) is generated before the final clock edge on the SCKn pin as indicated in Figure 26.63. If the TE and RE bits in the SCR become 0 at this time before the final edge of the clock signal on the SCKn pin, the SCKn pin is placed in the high-impedance state, so the width of the last clock pulse of the transfer clock is shortened. Furthermore, an RXI interrupt may lead to the input signal on the SSn# pin of a connected slave going to the high level before the final edge of the clock signal on the SCKn pin, leading to incorrect operation of the slave.
- In a multi-master configuration, take care because the SCKn pin output becomes high-impedance while the input on the SSn# pin is at the low level if a mode fault error occurs as the current character is being transferred, stopping supply of the clock signal to the connected slave. Remake the settings for the connected slave to avoid misaligned bits when transfer is restarted.

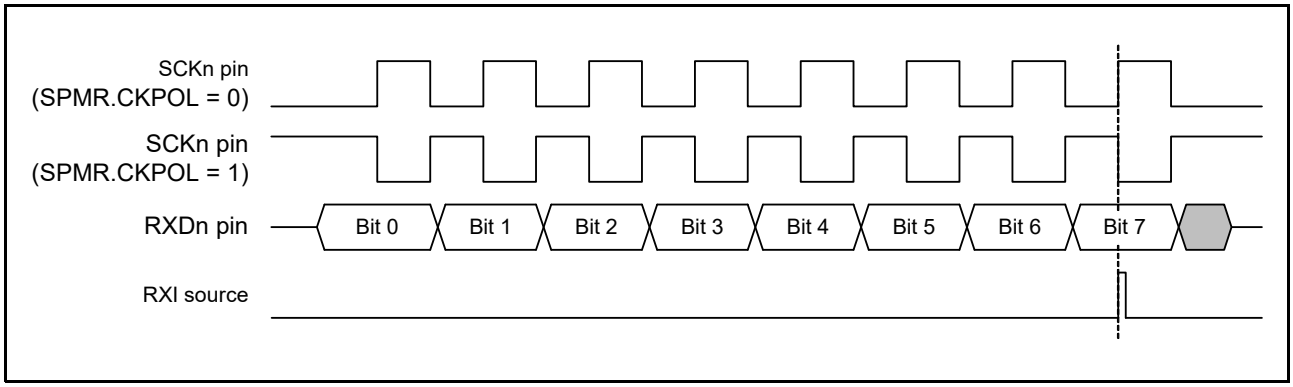


Figure 26.63 Timing of the RXI Interrupt in Simple SPI Mode (with Clock Delay)

(2) Slave Mode

- Secure at least five cycles (at least 10 cycles for SCI11) of the PCLK from writing transmit data in the TDR register to start of the external clock input. Also secure at least five cycles (at least 10 cycles for SCI11) of the PCLK from input of low level on the SSn# pin to start of the external clock input.
- Provide an external clock signal from the master the same as the transmit/receive data length.
- Control the input on the SSn# pin before the start and after the end of data transfer.
- When the level being input on the SSn# pin is to be changed from low to high while the current character is being transferred, set the TE and RE bits in the SCR to 0 and, after remaking the settings, restart transfer of the first byte.

26.12.12 Note on Transmit Enable Bit (TE Bit)

When setting the SCR.TE bit to 0 (serial transmission is disabled) while the pin function is “TXDn”, output of the pin becomes high impedance.

Prevent the TXDn line from becoming high impedance by any of the following ways:

(1) Connect a pull-up resistor to the TXDn line.

(2) Change the pin function to “general-purpose I/O port, output” before setting the SCR.TE bit to 0.
Set the SCR.TE bit to 1 before changing the pin function to “TXDn”.

26.12.13 Note on Stopping Reception When Using the RTS Function in Asynchronous Mode

One clock cycle of PCLK is required for the time from setting the SCR.RE bit to 0 to stopping the RTS signal generator in asynchronous mode.

When reading the RDR (or RDRL) register after setting the SCR.RE bit to 0, confirm that the RE bit has been set to 0 before reading the RDR (or RDRL) register to prevent these two processes from being performed consecutively.

27. I2C-bus Interface (RIICa)

This MCU has a single-channel I2C-bus interface (RIIC).
The RIIC module conforms with the NXP I2C-bus (Inter-IC bus) interface and provides a subset of its functions.
In this section, “PCLK” is used to refer to PCLKB.

27.1 Overview

Table 27.1 lists the specifications of the RIIC, Figure 27.1 shows a block diagram of the RIIC, and Figure 27.2 shows an example of I/O pin connections to external circuits (I2C-bus configuration example). Table 27.2 lists the I/O pins of the RIIC.

Table 27.1 RIIC Specifications (1/2)

Item	Description
Communications format	• I2C-bus format or SMBus format • Master mode or slave mode selectable • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate
Transfer rate	Fast-mode is supported (up to 400 kbps)
SCL clock	For master operation, the duty cycle of the SCL clock is selectable in the range from 4 to 96%.
Issuing and detecting conditions	Start, restart, and stop conditions are automatically generated. Start conditions (including restart conditions) and stop conditions are detectable.
Slave address	• Up to three different slave addresses can be set. • 7-bit and 10-bit address formats are supported (along with the use of both at once). • General call addresses, device ID addresses, and SMBus host addresses are detectable.
Acknowledgment	• For transmission, the acknowledge bit is automatically loaded. Transfer of the next data for transmission can be automatically suspended on detection of a not-acknowledge bit. • For reception, the acknowledge bit is automatically transmitted. If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible.
Wait function	• In reception, the following periods of waiting can be obtained by holding the SCL clock at the low level: Waiting between the eighth and ninth clock cycles Waiting between the ninth clock cycle and the first clock cycle of the next transfer
SDA output delay function	Timing of the output of transmitted data, including the acknowledge bit, can be delayed.
Arbitration	• For multi-master operation Operation to synchronize the SCL clock in cases of conflict with the SCL signal from another master is possible. When issuing the start condition would create conflict on the bus, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. In master operation, loss of arbitration is detected by testing for non-matching between the signal on the SDA line and the internal signal for the SDA line. • Loss of arbitration due to detection of the start condition while the bus is busy is detectable (to prevent the issuing of double start conditions). • Loss of arbitration in transfer of a not-acknowledge bit due to the internal signal for the SDA line and the level on the SDA line not matching is detectable. • Loss of arbitration due to non-matching of internal and line levels for data is detectable in slave transmission.
Timeout function	The internal timeout function is capable of detecting long-interval stop of the SCL clock.
Noise cancellation	The interface incorporates digital noise filters for both the SCL and SDA signals, and the width for noise cancellation by the filters is adjustable by software.
Interrupt sources	Four sources: • Error in transfer or occurrence of events Detection of arbitration, NACK, timeout, a start condition including a restart condition, or a stop condition • Receive data full (including matching with a slave address) • Transmit data empty (including matching with a slave address) • Transmit end

Table 27.1 RIIC Specifications (2/2)

Item	Description
Low power consumption function	Module stop state can be set.
RIIC operating modes	• Four Master transmit mode, master receive mode, slave transmit mode, and slave receive mode

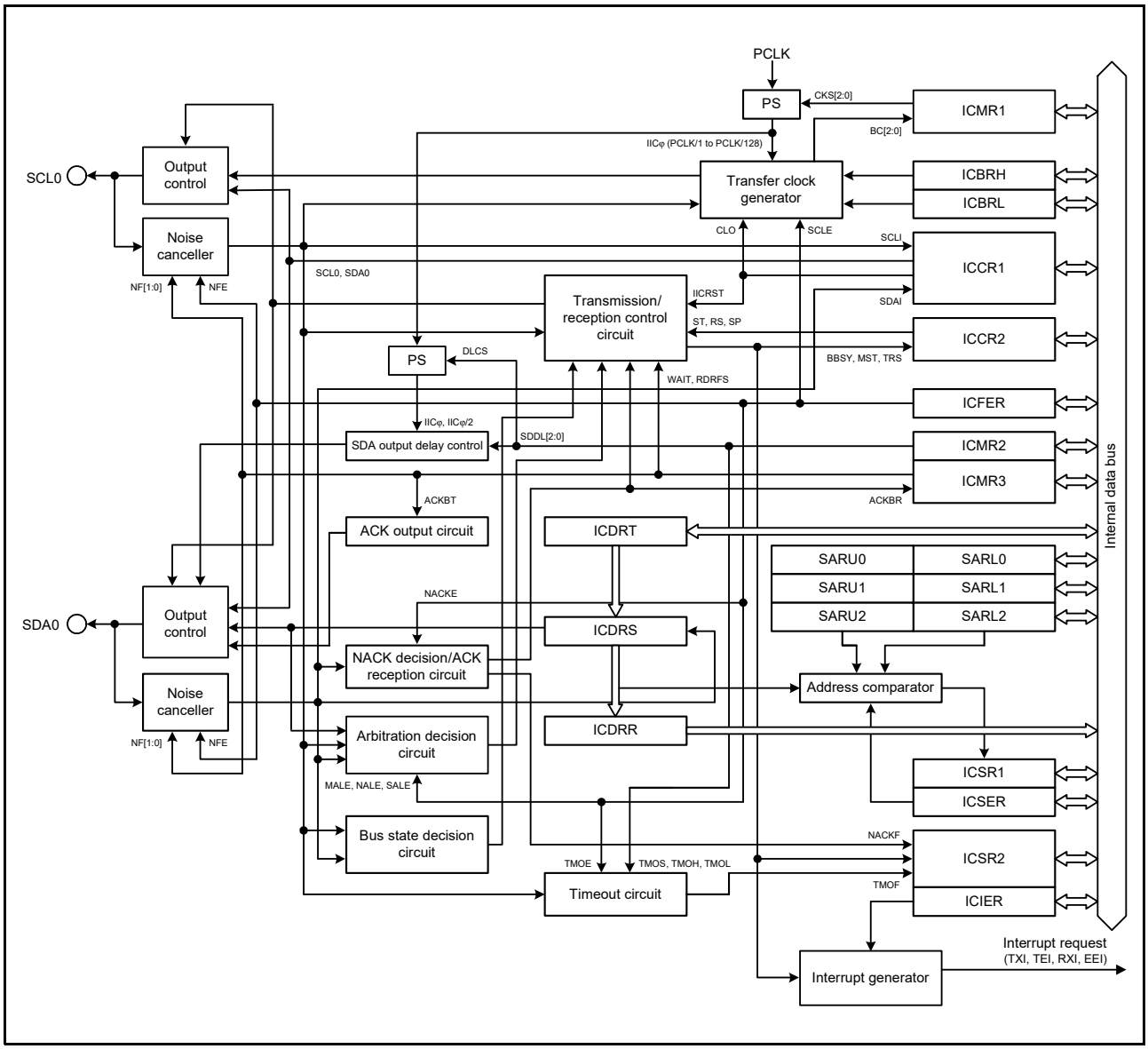


Figure 27.1 RIIC Block Diagram

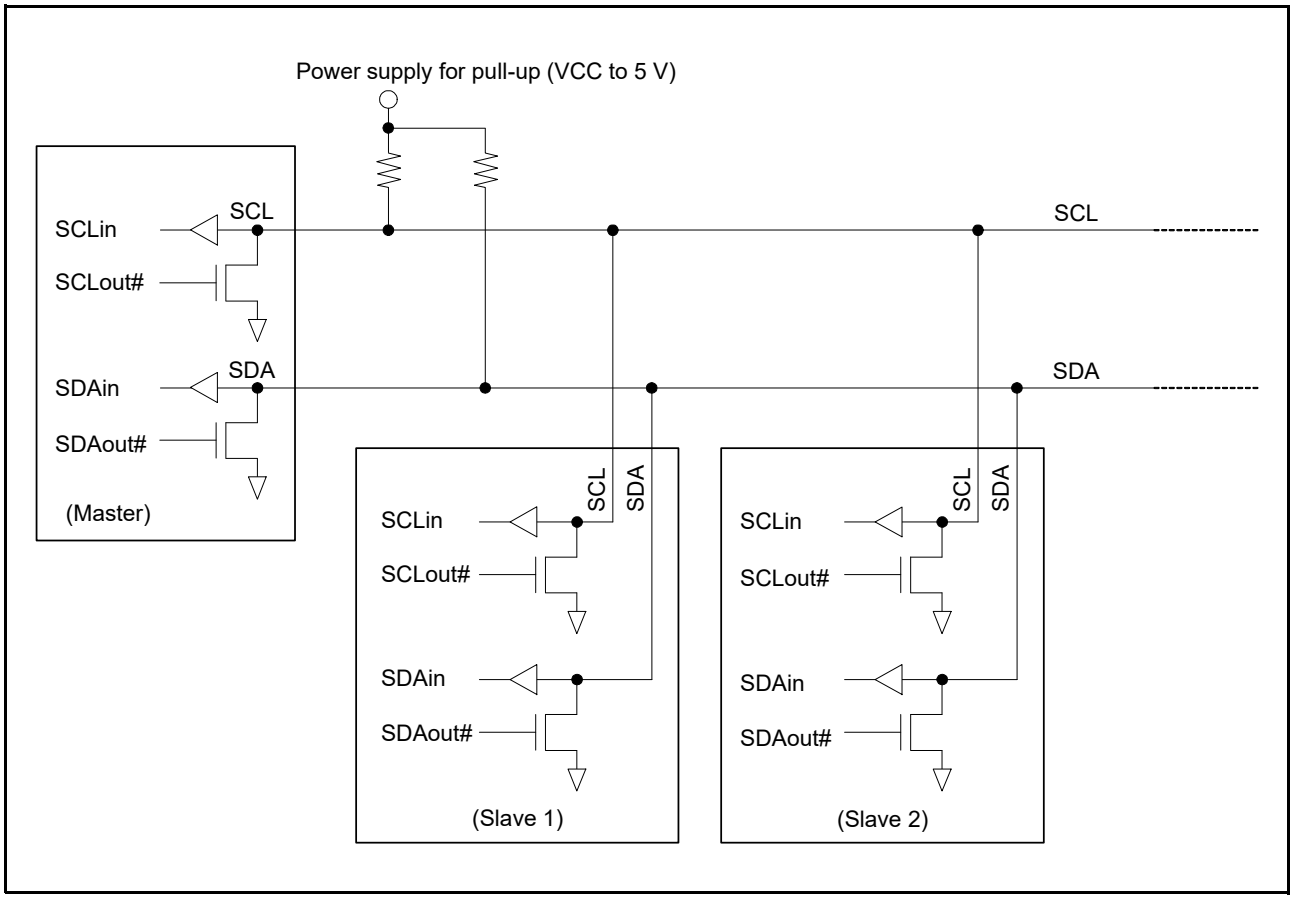


Figure 27.2 I/O Pin Connection to the External Circuit (I2C-bus Configuration Example)

The input level of the signals for RIIC is CMOS when I2C-bus is selected (ICMR3.SMBS bit is 0), or TTL when SMBus is selected (ICMR3.SMBS bit is 1).

Table 27.2 RIIC Pin Configuration

Channel	Pin Name	I/O	Function
RIIC0	SCL0	I/O	RIIC0 serial clock I/O pin
	SDA0	I/O	RIIC0 serial data I/O pin

27.2 Register Descriptions

27.2.1 I2C-bus Control Register 1 (ICCR1)

Address(es): RIIC0.ICCR1 0008 8300h

	b7	b6	b5	b4	b3	b2	b1	b0
	ICE	IICRST	CLO	SOWP	SCLO	SDAO	SCLI	SDAI
Value after reset:	0	0	0	1	1	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b0	SDAI	SDA Line Monitor	0: SDA0 line is low. 1: SDA0 line is high.	R
b1	SCLI	SCL Line Monitor	0: SCL0 line is low. 1: SCL0 line is high.	R
b2	SDAO	SDA Output Control/Monitor	• Read: 0: The RIIC has driven the SDA0 pin low. 1: The RIIC has released the SDA0 pin. • Write: 0: The RIIC drives the SDA0 pin low. 1: The RIIC releases the SDA0 pin.	R/W
b3	SCLO	SCL Output Control/Monitor	• Read: 0: The RIIC has driven the SCL0 pin low. 1: The RIIC has released the SCL0 pin. • Write: 0: The RIIC drives the SCL0 pin low. 1: The RIIC releases the SCL0 pin. (High level output is achieved through an external pull-up resistor.)	R/W
b4	SOWP	SCLO/SDAO Write Protect	0: SCLO and SDAO bits can be written. 1: SCLO and SDAO bits are protected. (This bit is read as 1.)	R/W
b5	CLO	Extra SCL Clock Cycle Output	0: Does not output an extra SCL clock cycle (default). 1: Outputs an extra SCL clock cycle. (The CLO bit is cleared automatically after one clock cycle is output.)	R/W
b6	IICRST	I2C-bus Interface Internal Reset	0: Releases the RIIC reset or internal reset. 1: Initiates the RIIC reset or internal reset. (Clears the bit counter and the SCL0/SDA0 output latch)	R/W
b7	ICE	I2C-bus Interface Enable	0: Disable (SCL0 and SDA0 pins in inactive state) 1: Enable (SCL0 and SDA0 pins in active state) (Combined with the IICRST bit to select either RIIC or internal reset.)	R/W

SDAO Bit (SDA Output Control/Monitor) and SCLO Bit (SCL Output Control/Monitor)

These bits are used to directly control the SDA0 and SCL0 signals output from the RIIC.

When writing to these bits, also write 0 to the SOWP bit.

The result of setting these bits is input to the RIIC via the input buffer. When slave mode is selected, a start condition may be detected and the bus may be released depending on the bit settings.

Do not rewrite these bits during a start condition, stop condition, restart condition, or during transmission or reception. Operation after rewriting under the above conditions is not guaranteed.

When reading these bits, the state of signals output from the RIIC can be read.

CLO Bit (Extra SCL Clock Cycle Output)

This bit is used to output an extra SCL clock cycle for debugging or error processing.
Normally, set the bit to 0. Setting the bit to 1 in a normal communication state causes a communication error.
For details on this function, refer to section 27.11.2, Extra SCL Clock Cycle Output Function.

IICRST Bit (I2C-bus Interface Internal Reset)

This bit is used to reset the internal states of the RIIC.
Setting this bit to 1 initiates an RIIC reset or internal reset.
Whether an RIIC reset or internal reset is initiated is determined according to the combination with the ICE bit. Table 27.3 lists the resets of the RIIC.
The RIIC reset initializes all registers and internal states of the RIIC, and the internal reset initializes the bit counter (ICMR1.BC[2:0] bits), the I2C-bus shift register (ICDRS), and the I2C-bus status registers (ICSR1 and ICSR2) as well as the internal states of the RIIC. For the reset conditions for each register, refer to section 27.14, Initialization of Registers and Functions When a Reset is Issued or a Condition is Detected.
An internal reset initiated with the IICRST bit set to 1 during operation (with the ICE bit set to 1) resets the internal states of the RIIC without initializing the port settings and the control and setting registers of the RIIC when the bus or RIIC hangs up due to a communication error.
If the RIIC hangs up in a low level output state, resetting the internal states cancels the low level output state and releases the bus with the SCL0 pin and SDA0 pin at a high impedance.

Note: If an internal reset is initiated using the IICRST bit for a bus hang-up occurred during communication with the master device in slave mode, the states may become different between the slave device and the master device (due to the difference in the bit counter information). For this reason, do not initiate an internal reset in slave mode, but initiate restoration processing from the master device. If an internal reset is necessary because the RIIC hangs up with the SCL0 line in a low level output state in slave mode, initiate an internal reset and then issue a restart condition from the master device or resume communication from the start condition issuance after issuing a stop condition. If communication is restarted by initiating a reset solely in the slave device without issuing a start condition or restart condition from the master device, synchronization will be lost because the master and slave devices operate asynchronously.

Table 27.3 RIIC Resets

IICRST	ICE	State	Specifications
1	0	RIIC reset	Resets all registers and internal states of the RIIC.
	1	Internal reset	Resets the ICMR1.BC[2:0] bits, registers ICSR1, ICSR2, and ICDRS, and the internal states of the RIIC.

ICE Bit (I2C-bus Interface Enable)

This bit selects the active or inactive state of the SCL0 and SDA0 pins. It can also be combined with the IICRST bit to initiate two types of resets. See Table 27.3, RIIC Resets, for the types of resets.
Set the ICE bit to 1 when using the RIIC. The SCL0 and SDA0 pins are placed in the active state when the ICE bit is set to 1.
Set the ICE bit to 0 when the RIIC is not to be used. The SCL0 and SDA0 pins are placed in the inactive state when the ICE bit is set to 0. Do not assign the SCL0 or SDA0 pin to the RIIC when setting up the multi-function pin controller (MPC). Note that the slave address comparison operation is carried out if the pins are assigned to the RIIC.

27.2.2 I2C-bus Control Register 2 (ICCR2)

Address(es): RIIC0.ICCR2 0008 8301h

	b7	b6	b5	b4	b3	b2	b1	b0
	BBSY	MST	TRS	—	SP	RS	ST	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b1	ST	Start Condition Issuance Request	0: Does not request to issue a start condition. 1: Requests to issue a start condition.	R/W
b2	RS	Restart Condition Issuance Request	0: Does not request to issue a restart condition. 1: Requests to issue a restart condition.	R/W
b3	SP	Stop Condition Issuance Request	0: Does not request to issue a stop condition. 1: Requests to issue a stop condition.	R/W
b4	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b5	TRS	Transmit/Receive Mode	0: Receive mode 1: Transmit mode	R/W*1
b6	MST	Master/Slave Mode	0: Slave mode 1: Master mode	R/W*1
b7	BBSY	Bus Busy Detection Flag	0: The I2C-bus is released (bus free state). 1: The I2C-bus is occupied (bus busy state).	R

Note 1. When the ICMR1.MTWP bit is set to 1, bits MST and TRS can be written to.

ST Bit (Start Condition Issuance Request)

This bit is used to request transition to master mode and issuance of a start condition.

When this bit is set to 1 to request to issue a start condition, a start condition is issued when the BBSY flag is set to 0 (bus free state).

For details on the start condition issuance, refer to section 27.10, Start Condition/Restart Condition/Stop Condition Issuing Function.

[Setting condition]

- When 1 is written to the ST bit

[Clearing conditions]

- When 0 is written to the ST bit
- When a start condition has been issued (a start condition is detected)
- When the ICSR2.AL (arbitration-lost) flag is set to 1
- When 1 is written to the ICCR1.IICRST bit to apply an RIIC reset or an internal reset

Note: Set the ST bit to 1 (start condition issuance request) when the BBSY flag is set to 0 (bus free state). Note that arbitration may be lost due to a start condition issuance error if the ST bit is set to 1 (start condition issuance request) when the BBSY flag is set to 1 (bus busy state).

RS Bit (Restart Condition Issuance Request)

This bit is used to request that a restart condition be issued in master mode.
When this bit is set to 1 to request to issue a restart condition, a restart condition is issued when the BBSY flag is set to 1 (bus busy state) and the MST bit is set to 1 (master mode).
For details on the restart condition issuance, refer to section 27.10, Start Condition/Restart Condition/Stop Condition Issuing Function.
[Setting condition]

- When 1 is written to the RS bit with the ICCR2.BBSY flag set to 1

[Clearing conditions]

- When 0 is written to the RS bit
- When a restart condition has been issued (a start condition is detected)
- When the ICSR2.AL (arbitration-lost) flag is set to 1
- When 1 is written to the ICCR1.IICRST bit to apply an RIIC reset or an internal reset

Note: Do not set the RS bit to 1 while issuing a stop condition.
Note: If 1 (requests to issue a restart condition) is written to the RS bit in slave mode, the restart condition is not issued but the RS bit remains set to 1. If the operating mode changes to master mode with the bit not being cleared, note that the restart condition may be issued.

SP Bit (Stop Condition Issuance Request)

This bit is used to request that a stop condition be issued in master mode.
When this bit is set to 1 to request to issue a stop condition, a stop condition is issued when the BBSY flag is set to 1 (bus busy state) and the MST bit is set to 1 (master mode).
For details on the stop condition issuance, refer to section 27.10, Start Condition/Restart Condition/Stop Condition Issuing Function.
[Setting condition]

- When 1 is written to the SP bit with both the BBSY flag and the ICCR2.MST bit set to 1

[Clearing conditions]

- When 0 is written to the SP bit
- When a stop condition has been issued (a stop condition is detected)
- When the ICSR2.AL (arbitration-lost) flag is set to 1
- When a start condition and a restart condition are detected
- When 1 is written to the ICCR1.IICRST bit to apply an RIIC reset or an internal reset

Note: Writing to the SP bit is not possible while the setting of the BBSY flag is 0 (bus free state).
Note: Do not set the SP bit to 1 while a restart condition is being issued.

TRS Bit (Transmit/Receive Mode)

This bit indicates transmit or receive mode.
The RIIC is in receive mode when the TRS bit is set to 0 and is in transmit mode when the bit is set to 1. Combination of this bit and the MST bit indicates the operating mode of the RIIC.
The value of TRS bit is automatically changed to 1 for transmit mode or 0 for receive mode by issuing or detection of a start condition and setting of the R/W# bit. Although writing to the TRS bit is possible when the ICMR1.MTWP bit is set to 1, writing to this bit is not necessary during normal usage.
[Setting conditions]

- When a start condition is issued normally according to the start condition issuance request (when a start condition is detected with the ST bit set to 1)
- When a restart condition is issued normally according to the restart condition issuance request (when a restart condition is detected with the RS bit set to 1)
- When the R/W# bit added to the slave address is set to 0 in master mode
- When the address received in slave mode matches the address enabled in the ICSER register, with the R/W# bit set to 1
- When 1 is written to the TRS bit with the ICMR1.MTWP bit set to 1

[Clearing conditions]

- When a stop condition is detected
- The ICSR2.AL (arbitration-lost) flag being set to 1
- In master mode, reception of a slave address to which an R/W# bit with the value 1 is appended
- In slave mode, a match between the received address and the address enabled in the ICSER register when the value of the received R/W# bit is 0 (including cases where the received address is the general call address)
- In slave mode, a restart condition is detected (a start condition is detected with ICCR2.BBSY flag is 1 and ICCR2.MST bit is 0)
- When 0 is written to the TRS bit with the ICMR1.MTWP bit set to 1
- When 1 is written to the ICCR1.IICRST bit to apply an RIIC reset or an internal reset

MST Bit (Master/Slave Mode)

This bit indicates master or slave mode.
The RIIC is in slave mode when the MST bit is set to 0 and is in master mode when the bit is set to 1. Combination of this bit and the TRS bit indicates the operating mode of the RIIC.
The value of the MST bit is automatically changed to 1 for master mode or 0 for slave mode by issuing of a start condition and issuing or detection of a stop condition, etc. Although writing to the MST bit is possible when the ICMR1.MTWP bit is set to 1, writing to this bit is not necessary during normal usage.
[Setting conditions]

- When a start condition is issued normally according to the start condition issuance request (when a start condition is detected with the ST bit set to 1)
- When 1 is written to the MST bit with the ICMR1.MTWP bit set to 1

[Clearing conditions]

- When a stop condition is detected
- When the ICSR2.AL (arbitration-lost) flag is set to 1
- When 0 is written to the MST bit with the ICMR1.MTWP bit set to 1
- When 1 is written to the ICCR1.IICRST bit to apply an RIIC reset or an internal reset

BBSY Flag (Bus Busy Detection Flag)

The BBSY flag indicates whether the I2C-bus is occupied (bus busy state) or released (bus free state).
This bit is set to 1 when the SDA0 line changes from high to low under the condition of SCL0 line = high, assuming that a start condition has been issued.
When the SDA0 line changes from low to high under the condition of SCL0 line = high, this bit is set to 0 after the bus free time (specified in the ICBRL register) start condition is not detected, assuming that a stop condition has been issued.
[Setting condition]

- When a start condition is detected

[Clearing conditions]

- When the bus free time (specified in the ICBRL register) start condition is not detected after detecting a stop condition
- When 1 is written to the ICCR1.IICRST bit with the ICCR1.ICE bit set to 0 (RIIC reset)

27.2.3 I2C-bus Mode Register 1 (ICMR1)

Address(es): RIIC0.ICMR1 0008 8302h

	b7	b6	b5	b4	b3	b2	b1	b0
	MTWP	CKS[2:0]			BCWP	BC[2:0]		
Value after reset:	0	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	BC[2:0]	Bit Counter	b2 b0 0 0 0: 9 bits 0 0 1: 2 bits 0 1 0: 3 bits 0 1 1: 4 bits 1 0 0: 5 bits 1 0 1: 6 bits 1 1 0: 7 bits 1 1 1: 8 bits	R/W*1
b3	BCWP	BC Write Protect	0: Enables a value to be written in the BC[2:0] bits. (This bit is read as 1.)	R/W*1
b6 to b4	CKS[2:0]	Internal Reference Clock Select	Select the internal reference clock (IICφ) source for the RIIC. b6 b4 0 0 0: PCLK/1 clock 0 0 1: PCLK/2 clock 0 1 0: PCLK/4 clock 0 1 1: PCLK/8 clock 1 0 0: PCLK/16 clock 1 0 1: PCLK/32 clock 1 1 0: PCLK/64 clock 1 1 1: PCLK/128 clock	R/W
b7	MTWP	MST/TRS Write Protect	0: Disables writing to the ICCR2.MST and TRS bits. 1: Enables writing to the ICCR2.MST and TRS bits.	R/W

Note 1. Rewrite the BC[2:0] bits and set the BCWP bit to 0 at the same time.

BC[2:0] Bits (Bit Counter)

These bits function as a counter that indicates the number of bits remaining to be transferred at the detection of a rising edge on the SCL0 line. Although these bits are writable and readable, it is not necessary to access these bits under normal conditions.

To write to these bits, specify the number of bits to be transferred plus one (data is transferred with an additional acknowledge bit) between transferred bytes when the SCL0 line is at a low level.

The values of the BC[2:0] bits return to 000b at the end of a data transfer including the acknowledge bit or when a start condition including a restart condition is detected.

27.2.4 I2C-bus Mode Register 2 (ICMR2)

Address(es): RIIC0.ICMR2 0008 8303h

	b7	b6	b5	b4	b3	b2	b1	b0
	DLCS	SDDL[2:0]			—	TMOH	TMOL	TMOS
Value after reset:	0	0	0	0	0	1	1	0

Bit	Symbol	Bit Name	Description	R/W
b0	TMOS	Timeout Detection Time Select	0: Long mode is selected. 1: Short mode is selected.	R/W
b1	TMOL	Timeout L Count Control	0: Count-up is disabled while the SCL0 line is at a low level. 1: Count-up is enabled while the SCL0 line is at a low level.	R/W
b2	TMOH	Timeout H Count Control	0: Count-up is disabled while the SCL0 line is at a high level. 1: Count-up is enabled while the SCL0 line is at a high level.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6 to b4	SDDL[2:0]	SDA Output Delay Counter	• When ICMR2.DLCS bit is 0 (IICφ) b6 b4 0 0 0: No output delay 0 0 1: 1 IICφ cycle 0 1 0: 2 IICφ cycles 0 1 1: 3 IICφ cycles 1 0 0: 4 IICφ cycles 1 0 1: 5 IICφ cycles 1 1 0: 6 IICφ cycles 1 1 1: 7 IICφ cycles • When ICMR2.DLCS bit is 1 (IICφ/2) b6 b4 0 0 0: No output delay 0 0 1: 1 or 2 IICφ cycles 0 1 0: 3 or 4 IICφ cycles 0 1 1: 5 or 6 IICφ cycles 1 0 0: 7 or 8 IICφ cycles 1 0 1: 9 or 10 IICφ cycles 1 1 0: 11 or 12 IICφ cycles 1 1 1: 13 or 14 IICφ cycles	R/W
b7	DLCS	SDA Output Delay Clock Source Select	0: The internal reference clock (IICφ) is selected as the clock source of the SDA output delay counter. 1: The internal reference clock divided by 2 (IICφ/2) is selected as the clock source of the SDA output delay counter.*1	R/W

Note 1. The DLCS bit setting of 1 (IICφ/2) only becomes valid when SCL pin is low. When SCL pin is high, the DLCS bit setting of 1 becomes invalid and the clock source becomes the internal reference clock (IICφ).

TMOS Bit (Timeout Detection Time Select)

This bit is used to select long mode or short mode for the timeout detection time when the timeout function is enabled (ICFER.TMOE bit is 1). When this bit is set to 0, long mode is selected. When this bit is set to 1, short mode is selected. In long mode, the timeout detection internal counter functions as a 16-bit counter. In short mode, the counter functions as a 14-bit counter. While the SCL0 line is in the state that enables this counter as specified by bits TMOH and TMOL, the counter counts up in synchronization with the internal reference clock (IICφ) as a count source.
For details on the timeout function, refer to section 27.11.1, Timeout Function.

TMOL Bit (Timeout L Count Control)

This bit is used to enable or disable the internal counter of the timeout function to count up while the SCL0 line is held low when the timeout function is enabled (ICFER.TMOE bit is 1).

TMOH Bit (Timeout H Count Control)

This bit is used to enable or disable the internal counter of the timeout function to count up while the SCL0 line is held high when the timeout function is enabled (ICFER.TMOE bit is 1).

SDDL[2:0] Bits (SDA Output Delay Counter)

The SDA output can be delayed by the SDDL[2:0] setting. This counter works with the clock source selected by the DLCS bit. The setting of this function can be used for all types of SDA output, including the transmission of the acknowledge bit.

Set the SDA output delay time to meet the I2C-bus specification (within the data enable time/acknowledge enable time*1) or the SMBus specification (within the data hold time: 300 ns or more, and SCL-clock low-level period - the data setup time: 250 ns). Note that, if a value outside the specification is set, communication with communication devices may malfunction or it may seemingly become a start condition or stop condition depending on the bus state.

For details on this function, refer to section 27.5, SDA Output Delay Function.

Note 1. Data enable time/acknowledge enable time
3,450 ns (up to 100 kbps: Standard-mode (Sm))
900 ns (up to 400 kbps: Fast-mode (Fm))

27.2.5 I2C-bus Mode Register 3 (ICMR3)

Address(es): RIIC0.ICMR3 0008 8304h

	b7	b6	b5	b4	b3	b2	b1	b0
	SMBS	WAIT	RDRFS	ACKWP	ACKBT	ACKBR	NF[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	NF[1:0]	Noise Filter Stage Select	b1 b0 0 0: Noise of up to one IICφ cycle is filtered out (single-stage filter). 0 1: Noise of up to two IICφ cycles is filtered out (2-stage filter). 1 0: Noise of up to three IICφ cycles is filtered out (3-stage filter). 1 1: Noise of up to four IICφ cycles is filtered out (4-stage filter).	R/W
b2	ACKBR	Receive Acknowledge	0: 0 is received as the acknowledge bit (ACK reception). 1: 1 is received as the acknowledge bit (NACK reception).	R
b3	ACKBT	Transmit Acknowledge	0: 0 is sent as the acknowledge bit (ACK transmission). 1: 1 is sent as the acknowledge bit (NACK transmission).	R/W*1
b4	ACKWP	ACKBT Write Protect	0: Modification of the ACKBT bit is disabled. 1: Modification of the ACKBT bit is enabled.	R/W*1
b5	RDRFS	RDRF Flag Set Timing Select	0: The RDRF flag is set at the rising edge of the ninth SCL clock cycle. (The SCL0 line is not held low at the falling edge of the eighth clock cycle.) 1: The RDRF flag is set at the rising edge of the eighth SCL clock cycle. (The SCL0 line is held low at the falling edge of the eighth clock cycle.) Low-hold is released by writing a value to the ACKBT bit.	R/W*2
b6	WAIT	WAIT	0: No WAIT (The period between ninth clock cycle and first clock cycle is not held low.) 1: WAIT (The period between ninth clock cycle and first clock cycle is held low.) Low-hold is released by reading the ICDRR register.	R/W*2
b7	SMBS	SMBus/I2C-bus Select	0: The I2C-bus is selected. 1: The SMBus is selected.	R/W

Note 1. Write to the ACKBT bit only while the ACKWP bit is already 1. If it is attempted to write 1 to both the ACKWP and ACKBT bits at the same time, the ACKBT bit will not be set to 1.

Note 2. The WAIT and RDRFS bits are valid only in receive mode (invalid in transmit mode).

NF[1:0] Bits (Noise Filter Stage Select)

These bits are used to select the number of stages in the digital noise filter.

For details on the digital noise filter function, refer to section 27.6, Digital Noise Filter Circuit.

Note: Set the noise range to be filtered out by the noise filter within a range less than the SCL0 line high-level period or low-level period. If the noise filter width is set to a value of [the shorter one of either SCL high width or SCL low width] – {1.5 × t_{IICcyc} (cycle time of internal reference clock (IICφ)) + 120 ns (pulse width suppressed by the analog noise filter, a reference value)} or a greater value, the SCL clock is regarded as noise by the noise filter function of the RIIC, which may prevent the RIIC from operating normally.

ACKBR Bit (Receive Acknowledge)

This bit is used to store the acknowledge bit information received from the receive device in transmit mode.
[Setting condition]

- When 1 is received as the acknowledge bit with the ICCR2.TRS bit set to 1

[Clearing conditions]

- When 0 is received as the acknowledge bit with the ICCR2.TRS bit set to 1
- When 1 is written to the ICCR1.IICRST bit while the ICCR1.ICE bit is 0 (RIIC reset)

ACKBT Bit (Transmit Acknowledge)

This bit is used to set the bit to be sent at the acknowledge timing in receive mode.
[Setting condition]

- When 1 is written to this bit with the ACKWP bit set to 1

[Clearing conditions]

- When 0 is written to this bit with the ACKWP bit set to 1
- When stop condition issuance is detected (when a stop condition is detected with the ICCR2.SP bit set to 1)
- When 1 is written to the ICCR1.IICRST bit while the ICCR1.ICE bit is 0 (RIIC reset)

ACKWP Bit (ACKBT Write Protect)

This bit is used to control the modification of the ACKBT bit.

RDRFS Bit (RDRF Flag Set Timing Select)

This bit is used to select the RDRF flag set timing in receive mode and also to select whether to hold the SCL0 line low at the falling edge of the eighth SCL clock cycle.
When the RDRFS bit is 0, the SCL0 line is not held low at the falling edge of the eighth SCL clock cycle, and the RDRF flag is set to 1 at the rising edge of the ninth SCL clock cycle.
When the RDRFS bit is 1, the RDRF flag is set to 1 at the rising edge of the eighth SCL clock cycle and the SCL0 line is held low at the falling edge of the eighth SCL clock cycle. The low-hold of the SCL0 line is released by writing a value to the ACKBT bit.
After data is received with this setting, the SCL0 line is automatically held low before the acknowledge bit is sent. This enables processing to send ACK (ACKBT bit is 0) or NACK (ACKBT bit is 1) according to receive data.

WAIT Bit (WAIT)

This bit is used to control whether to hold the period between the ninth SCL clock cycle and the first SCL clock cycle low until the I2C-bus receive data register (ICDRR) is completely read each time single-byte data is received in receive mode.
When the WAIT bit is 0, the receive operation is continued without holding the period between the ninth and the first SCL clock cycle low. When both the RDRFS and WAIT bits are 0, continuous receive operation is enabled with the double buffer.
When the WAIT bit is 1, the SCL0 line is held low from the falling edge of the ninth clock cycle until the ICDRR register value is read each time single-byte data is received. This enables receive operation in byte units.

Note: When the value of the WAIT bit is to be read, be sure to read the ICDRR register beforehand.

SMBS Bit (SMBus/I2C-bus Select)

Setting this bit to 1 selects the SMBus and enables the ICSER.HOAE bit.

27.2.6 I2C-bus Function Enable Register (ICFER)

Address(es): RIIC0.ICFER 0008 8305h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	SCLE	NFE	NACKE	SALE	NALE	MALE	TMOE
Value after reset:	0	1	1	1	0	0	1	0

Bit	Symbol	Bit Name	Description	R/W
b0	TMOE	Timeout Function Enable	0: The timeout function is disabled. 1: The timeout function is enabled.	R/W
b1	MALE	Master Arbitration-Lost Detection Enable	0: Master arbitration-lost detection is disabled. (Disables the arbitration-lost detection function and does not clear the ICCR2.MST and TRS bits automatically when arbitration is lost.) 1: Master arbitration-lost detection is enabled. (Enables the arbitration-lost detection function and clears the ICCR2.MST and TRS bits automatically when arbitration is lost.)	R/W
b2	NALE	NACK Transmission Arbitration-Lost Detection Enable	0: NACK transmission arbitration-lost detection is disabled. 1: NACK transmission arbitration-lost detection is enabled.	R/W
b3	SALE	Slave Arbitration-Lost Detection Enable	0: Slave arbitration-lost detection is disabled. 1: Slave arbitration-lost detection is enabled.	R/W
b4	NACKE	NACK Reception Transfer Suspension Enable	0: Transfer operation is not suspended during NACK reception (transfer suspension disabled). 1: Transfer operation is suspended during NACK reception (transfer suspension enabled).	R/W
b5	NFE	Digital Noise Filter Circuit Enable	0: No digital noise filter circuit is used. 1: A digital noise filter circuit is used.	R/W
b6	SCLE	SCL Synchronous Circuit Enable	0: No SCL synchronous circuit is used. 1: An SCL synchronous circuit is used.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

TMOE Bit (Timeout Function Enable)

This bit is used to enable or disable the timeout function.

For details on the timeout function, refer to section 27.11.1, Timeout Function.

MALE Bit (Master Arbitration-Lost Detection Enable)

This bit is used to specify whether to use the arbitration-lost detection function in master mode. Normally, set this bit to 1.

NALE Bit (NACK Transmission Arbitration-Lost Detection Enable)

This bit is used to specify whether to cause arbitration to be lost when ACK is detected during transmission of NACK in receive mode (such as when slaves with the same address exist on the bus or when two or more masters select the same slave device simultaneously with different number of receive bytes).

SALE Bit (Slave Arbitration-Lost Detection Enable)

This bit is used to specify whether to cause arbitration to be lost when a value different from the value being transmitted is detected on the bus in slave transmit mode (such as when slaves with the same address exist on the bus or when a mismatch with the transmit data occurs due to noise).

NACKE Bit (NACK Reception Transfer Suspension Enable)

This bit is used to specify whether to continue or discontinue the transfer operation when NACK is received from the slave device in transmit mode. Normally, set this bit to 1.
When NACK is received with the NACKE bit set to 1, the next transfer operation is suspended.
When the NACKE bit is 0, the next transfer operation is continued regardless of the received acknowledge content.
For details on the NACK reception transfer suspension function, refer to section 27.8.2, NACK Reception Transfer Suspension Function.

SCLE Bit (SCL Synchronous Circuit Enable)

This bit is used to specify whether to synchronize the SCL clock with the SCL input clock. Normally, set this bit to 1.
When the SCLE bit is set to 0 (no SCL synchronous circuit used), the RIIC does not synchronize the SCL clock with the SCL input clock. In this setting, the RIIC outputs the SCL clock with the transfer rate set in registers ICBRH and ICBRL regardless of the SCL0 line state. For this reason, if the bus load of the I2C-bus line is much larger than the specification value or if the SCL clock output overlaps in multiple masters, the short-cycle SCL clock that does not meet the specification may be output. When no SCL synchronous circuit is used, it also affects the issuance of a start condition, restart condition, and stop condition, and the continuous output of extra SCL clock cycles.
This bit must not be set to 0 except for checking the output of the set transfer rate.

27.2.7 I2C-bus Status Enable Register (ICSER)

Address(es): RIIC0.ICSER 0008 8306h

	b7	b6	b5	b4	b3	b2	b1	b0
	HOAE	—	DIDE	—	GCAE	SAR2E	SAR1E	SAR0E
Value after reset:	0	0	0	0	1	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	SAR0E	Slave Address Register 0 Enable	0: Slave address in registers SARL0 and SARU0 is disabled. 1: Slave address in registers SARL0 and SARU0 is enabled.	R/W
b1	SAR1E	Slave Address Register 1 Enable	0: Slave address in registers SARL1 and SARU1 is disabled. 1: Slave address in registers SARL1 and SARU1 is enabled.	R/W
b2	SAR2E	Slave Address Register 2 Enable	0: Slave address in registers SARL2 and SARU2 is disabled. 1: Slave address in registers SARL2 and SARU2 is enabled.	R/W
b3	GCAE	General Call Address Enable	0: General call address detection is disabled. 1: General call address detection is enabled.	R/W
b4	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b5	DIDE	Device-ID Address Detection Enable	0: Device-ID address detection is disabled. 1: Device-ID address detection is enabled.	R/W
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	HOAE	Host Address Enable	0: Host address detection is disabled. 1: Host address detection is enabled.	R/W

SARyE Bit (Slave Address Register y Enable) (y = 0 to 2)

This bit is used to enable or disable the slave address set in registers SARLy and SARUy.

When this bit is set to 1, the slave address set in registers SARLy and SARUy is enabled and is compared with the received slave address.

When this bit is set to 0, the slave address set in registers SARLy and SARUy is disabled and is ignored even if it matches the received slave address.

GCAE Bit (General Call Address Enable)

This bit is used to specify whether to ignore the general call address (0000 000b + 0 (write): All 0) when it is received.

When this bit is set to 1, if the received slave address matches the general call address, the RIIC recognizes the received slave address as the general call address independently of the slave addresses set in registers SARLy and SARUy (y = 0 to 2) and performs data receive operation.

When this bit is set to 0, the received slave address is ignored even if it matches the general call address.

DIDE Bit (Device-ID Address Detection Enable)

This bit is used to specify whether to recognize and execute the device-ID address when a device ID (1111 100b) is received in the first byte after a start condition or restart condition is detected.

When this bit is set to 1, if the received first byte matches the device ID, the RIIC recognizes that the device-ID address has been received. When the following R/W# bit is 0 (write), the RIIC recognizes the second and the following bytes as slave addresses and continues the receive operation.

When this bit is set to 0, the RIIC ignores the received first byte even if it matches the device ID address and recognizes the first byte as a normal slave address.

For details on the device-ID address detection, refer to section 27.7.3, Device-ID Address Detection.

HOAE Bit (Host Address Enable)

This bit is used to specify whether to ignore received host address (0001 000b) when the ICMR3.SMBS bit is 1.

When this bit is set to 1 while the ICMR3.SMBS bit is 1, if the received slave address matches the host address, the RIIC recognizes the received slave address as the host address independently of the slave addresses set in registers SARLy and SARUy (y = 0 to 2) and performs the receive operation.

When the ICMR3.SMBS bit or the HOAE bit is set to 0, the received slave address is ignored even if it matches the host address.

27.2.8 I2C-bus Interrupt Enable Register (ICIER)

Address(es): RIIC0.ICIER 0008 8307h

	b7	b6	b5	b4	b3	b2	b1	b0
	TIE	TEIE	RIE	NAKIE	SPIE	STIE	ALIE	TMOIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TMOIE	Timeout Interrupt Request Enable	0: Timeout interrupt (TMOI) request is disabled. 1: Timeout interrupt (TMOI) request is enabled.	R/W
b1	ALIE	Arbitration-Lost Interrupt Request Enable	0: Arbitration-lost interrupt (ALI) request is disabled. 1: Arbitration-lost interrupt (ALI) request is enabled.	R/W
b2	STIE	Start Condition Detection Interrupt Request Enable	0: Start condition detection interrupt (STI) request is disabled. 1: Start condition detection interrupt (STI) request is enabled.	R/W
b3	SPIE	Stop Condition Detection Interrupt Request Enable	0: Stop condition detection interrupt (SPI) request is disabled. 1: Stop condition detection interrupt (SPI) request is enabled.	R/W
b4	NAKIE	NACK Reception Interrupt Request Enable	0: NACK reception interrupt (NAKI) request is disabled. 1: NACK reception interrupt (NAKI) request is enabled.	R/W
b5	RIE	Receive Data Full Interrupt Request Enable	0: Receive data full interrupt (RXI) request is disabled. 1: Receive data full interrupt (RXI) request is enabled.	R/W
b6	TEIE	Transmit End Interrupt Request Enable	0: Transmit end interrupt (TEI) request is disabled. 1: Transmit end interrupt (TEI) request is enabled.	R/W
b7	TIE	Transmit Data Empty Interrupt Request Enable	0: Transmit data empty interrupt (TXI) request is disabled. 1: Transmit data empty interrupt (TXI) request is enabled.	R/W

TMOIE Bit (Timeout Interrupt Request Enable)

This bit is used to enable or disable timeout interrupt (TMOI) requests when the ICSR2.TMOF flag is set to 1. A TMOI interrupt request is canceled by setting the TMOF flag or the TMOIE bit to 0.

ALIE Bit (Arbitration-Lost Interrupt Request Enable)

This bit is used to enable or disable arbitration-lost interrupt (ALI) requests when the ICSR2.AL flag is set to 1. An ALI interrupt request is canceled by setting the AL flag or the ALIE bit to 0.

STIE Bit (Start Condition Detection Interrupt Request Enable)

This bit is used to enable or disable start condition detection interrupt (STI) requests when the ICSR2.START flag is set to 1. An STI interrupt request is canceled by setting the START flag or the STIE bit to 0.

SPIE Bit (Stop Condition Detection Interrupt Request Enable)

This bit is used to enable or disable stop condition detection interrupt (SPI) requests when the ICSR2.STOP flag is set to 1. An SPI interrupt request is canceled by setting the STOP flag or the SPIE bit to 0.

NAKIE Bit (NACK Reception Interrupt Request Enable)

This bit is used to enable or disable NACK reception interrupt (NAKI) requests when the ICSR2.NACKF flag is set to 1. An NAKI interrupt request is canceled by setting the NACKF flag or the NAKIE bit to 0.

RIE Bit (Receive Data Full Interrupt Request Enable)

This bit is used to enable or disable receive data full interrupt (RXI) requests when the ICSR2.RDRF flag is set to 1.

TEIE Bit (Transmit End Interrupt Request Enable)

This bit is used to enable or disable transmit end interrupt (TEI) requests when the ICSR2.TEND flag is set to 1. An TEI interrupt request is canceled by setting the TEND flag or the TEIE bit to 0.

TIE Bit (Transmit Data Empty Interrupt Request Enable)

This bit is used to enable or disable transmit data empty interrupt (TXI) requests when the ICSR2.TDRE flag is set to 1.

27.2.9 I2C-bus Status Register 1 (ICSR1)

Address(es): RIIC0.ICSR1 0008 8308h

	b7	b6	b5	b4	b3	b2	b1	b0
	HOA	—	DID	—	GCA	AAS2	AAS1	AAS0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	AAS0	Slave Address 0 Detection Flag	0: Slave address 0 is not detected. 1: Slave address 0 is detected.	R/(W) *1
b1	AAS1	Slave Address 1 Detection Flag	0: Slave address 1 is not detected. 1: Slave address 1 is detected.	R/(W) *1
b2	AAS2	Slave Address 2 Detection Flag	0: Slave address 2 is not detected. 1: Slave address 2 is detected.	R/(W) *1
b3	GCA	General Call Address Detection Flag	0: General call address is not detected. 1: General call address is detected.	R/(W) *1
b4	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b5	DID	Device-ID Address Detection Flag	0: Device-ID command is not detected. 1: Device-ID command is detected. • This bit is set to 1 when the first byte received immediately after a start condition is detected matches a value of (device ID (1111 100b) + 0 (write)).	R/(W) *1
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	HOA	Host Address Detection Flag	0: Host address is not detected. 1: Host address is detected. • This bit is set to 1 when the received slave address matches the host address (0001 000b).	R/(W) *1

Note 1. Only 0 can be written to clear the flag.

AASy Flag (Slave Address y Detection Flag) (y = 0 to 2)

[Setting conditions]

For 7-bit address format: SARUy.FS bit = 0

- When the received slave address matches the SARLy.SVA[6:0] bits value with the ICSER.SARyE bit set to 1 (slave address y detection enabled)
  This flag is set to 1 at the rising edge of the ninth SCL clock cycle in the first byte.

For 10-bit address format: SARUy.FS bit = 1

- When the received slave address matches a value of (11110b + SARUy.SVA[1:0] bits) and the following address matches the SARLy value with the ICSER.SARyE bit set to 1 (slave address y detection enabled)
  This flag is set to 1 at the rising edge of the ninth SCL clock cycle in the second byte.

[Clearing conditions]

- When 0 is written to the AASy flag after reading the AASy flag to be 1
- When a stop condition is detected
- When 1 is written to the ICCR1.IICRST bit to apply an RIIC reset or an internal reset

For 7-bit address format: SARUy.FS bit = 0

- When the received slave address does not match the SARLy.SVA[6:0] bits value with the ICSER.SARyE bit set to 1 (slave address y detection enabled)
  This flag is set to 0 at the rising edge of the ninth SCL clock cycle in the first byte.

For 10-bit address format: SARUy.FS bit = 1

- When the received slave address does not match a value of (11110b + SARUy.SVA[1:0] bits) with the ICSER.SARyE bit set to 1 (slave address y detection enabled)
  This flag is set to 0 at the rising edge of the ninth SCL clock cycle in the first byte.
- When the received slave address matches a value of (11110b + SARUy.SVA[1:0] bits) and the following address does not match the SARLy value with the ICSER.SARyE bit set to 1 (slave address y detection enabled)
  This flag is set to 0 at the rising edge of the ninth SCL clock cycle in the second byte.

GCA Flag (General Call Address Detection Flag)

[Setting condition]

- When the received slave address matches the general call address (0000 000b + 0 (write)) with the ICSER.GCAE bit set to 1 (general call address detection is enabled)
  This flag is set to 1 at the rising edge of the ninth SCL clock cycle in the first byte.

[Clearing conditions]

- When 0 is written to the GCA flag after reading GCA flag to be 1
- When a stop condition is detected
- When the received slave address does not match the general call address (0000 000b + 0 (write)) with the ICSER.GCAE bit set to 1 (general call address detection is enabled)
  This flag is set to 0 at the rising edge of the ninth SCL clock cycle in the first byte.
- When 1 is written to the ICCR1.IICRST bit to apply an RIIC reset or an internal reset

DID Flag (Device-ID Address Detection Flag)

[Setting condition]

- When the first byte received immediately after a start condition or restart condition is detected matches a value of (device ID (1111 100b) + 0 (write)) with the ICSER.DIDE bit set to 1 (device-ID address detection is enabled)
  This flag is set to 1 at the rising edge of the ninth SCL clock cycle in the first byte.

[Clearing conditions]

- When 0 is written to the DID flag after reading DID flag to be 1
- When a stop condition is detected
- When the first byte received immediately after a start condition or restart condition is detected does not match a value of (device ID (1111 100b)) with the ICSER.DIDE bit set to 1 (device-ID address detection is enabled)
  This flag is set to 0 at the rising edge of the ninth SCL clock cycle in the first byte.
- When the first byte received immediately after a start condition or restart condition is detected matches a value of (device ID (1111 100b) + 0 (write)) and the second byte does not match any of slave addresses 0 to 2 with the ICSER.DIDE bit set to 1 (device-ID address detection is enabled)
  This flag is set to 0 at the rising edge of the ninth SCL clock cycle in the second byte.
- When 1 is written to the ICCR1.IICRST bit to apply an RIIC reset or an internal reset

HOA Flag (Host Address Detection Flag)

[Setting condition]

- When the received slave address matches the host address (0001 000b) with the ICSER.HOAE bit set to 1 (host address detection is enabled)
  This flag is set to 1 at the rising edge of the ninth SCL clock cycle in the first byte.

[Clearing conditions]

- When 0 is written to the HOA flag after reading HOA flag to be 1
- When a stop condition is detected
- When the received slave address does not match the host address (0001 000b) with the ICSER.HOAE bit set to 1

(host address detection is enabled)
This flag is set to 0 at the rising edge of the ninth SCL clock cycle in the first byte.

- When 1 is written to the ICCR1.IICRST bit to apply an RIIC reset or an internal reset

27.2.10 I2C-bus Status Register 2 (ICSR2)

Address(es): RIIC0.ICSR2 0008 8309h

	b7	b6	b5	b4	b3	b2	b1	b0
	TDRE	TEND	RDRF	NACKF	STOP	START	AL	TMOF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TMOF	Timeout Detection Flag	0: Timeout is not detected. 1: Timeout is detected.	R/(W) *1
b1	AL	Arbitration-Lost Flag	0: Arbitration is not lost. 1: Arbitration is lost.	R/(W) *1
b2	START	Start Condition Detection Flag	0: Start condition is not detected. 1: Start condition is detected.	R/(W) *1
b3	STOP	Stop Condition Detection Flag	0: Stop condition is not detected. 1: Stop condition is detected.	R/(W) *1
b4	NACKF	NACK Detection Flag	0: NACK is not detected. 1: NACK is detected.	R/(W) *1
b5	RDRF	Receive Data Full Flag	0: The ICDRR register contains no receive data. 1: The ICDRR register contains receive data.	R/(W) *1
b6	TEND	Transmit End Flag	0: Data is being transmitted. 1: Data has been transmitted.	R/(W) *1
b7	TDRE	Transmit Data Empty Flag	0: The ICDRT register contains transmit data. 1: The ICDRT register contains no transmit data.	R

Note 1. Only 0 can be written to clear the flag.

TMOF Flag (Timeout Detection Flag)

This flag is set to 1 when the RIIC recognizes timeout after the SCL0 line state remains unchanged for a certain period.
[Setting condition]

- When the SCL0 line state remains unchanged for the period specified by bits ICMR2.TMOH, TMOL, and TMOS while the ICFER.TMOE bit is 1 (the timeout function is enabled) in master mode or in slave mode and the received slave address matches.

[Clearing conditions]

- When 0 is written to the TMOF bit after reading TMOF = 1
- When 1 is written to the ICCR1.IICRST bit to apply an RIIC reset or an internal reset

AL Flag (Arbitration-Lost Flag)

This flag shows that bus mastership has been lost (loss in arbitration) due to a bus conflict or some other reason when a start condition is issued or an address and data are transmitted. The RIIC monitors the level on the SDA0 line during transmission and, if the level on the line does not match the value of the bit being output, sets the value of the AL flag to 1 to indicate that the bus is occupied by another device.
The RIIC can also set the flag to indicate the detection of loss of arbitration during NACK transmission in master mode or during data transmission in slave mode.

[Setting conditions]

When master arbitration-lost detection is enabled: ICFER.MALE = 1

- When the internal SDA output state does not match the SDA0 line level at the rising edge of SCL clock except for the ACK period during data (including slave address) transmission in master transmit mode (when the SDA0 line is driven low while the internal SDA output is at a high level (the SDA0 pin is in the high-impedance state))
- When a start condition is detected while the ICCR2.ST bit is 1 (start condition issuance request) or the internal SDA output state does not match the SDA0 line level
- When the ICCR2.ST bit is set to 1 (start condition issuance request) with the ICCR2.BBSY flag set to 1.

When NACK arbitration-lost detection is enabled: ICFER.NALE = 1

- When the internal SDA output state does not match the SDA0 line level at the rising edge of SCL clock in the ACK period during NACK transmission in receive mode

When slave arbitration-lost detection is enabled: ICFER.SALE = 1

- When the internal SDA output state does not match the SDA0 line level at the rising edge of SCL clock except for the ACK period during data transmission in slave transmit mode

[Clearing conditions]

- When 0 is written to the AL flag after reading AL = 1
- When 1 is written to the ICCR1.IICRST bit to apply an RIIC reset or an internal reset

Table 27.4 Relationship between Arbitration-Lost Generation Sources and Arbitration-Lost Enable Functions

ICFER			ICSR2		
MALE	NALE	SALE	AL	Error	Arbitration-Lost Generation Source
1	×	×	1	Start condition issuance error	When internal SDA output state does not match SDA0 line level when a start condition is detected while the ICCR2.ST bit is 1
					When ICCR2.ST bit is set to 1 with ICCR2.BBSY flag set to 1
			1	Transmit data mismatch	When transmit data (including slave address) does not match the bus state in master transmit mode
×	1	×	1	NACK transmission mismatch	When ACK is detected during transmission of NACK in master receive mode or slave receive mode
×	×	1	1	Transmit data mismatch	When transmit data does not match the bus state in slave transmit mode

×: Don't care

START Flag (Start Condition Detection Flag)

[Setting condition]

- When a start condition (or a restart condition) is detected

[Clearing conditions]

- When 0 is written to the START bit after reading START = 1
- When a stop condition is detected
- When 1 is written to the ICCR1.IICRST bit to apply an RIIC reset or an internal reset

STOP Flag (Stop Condition Detection Flag)

[Setting condition]

- When a stop condition is detected

[Clearing conditions]

- When 0 is written to the STOP bit after reading STOP = 1
- When 1 is written to the ICCR1.IICRST bit to apply an RIIC reset or an internal reset

NACKF Flag (NACK Detection Flag)

[Setting condition]

- When acknowledge is not received (NACK is received) from the receive device in transmit mode with the ICFER.NACKE bit set to 1 (transfer suspension enabled)

[Clearing conditions]

- When 0 is written to the NACKF bit after reading NACKF = 1
- When 1 is written to the ICCR1.IICRST bit to apply an RIIC reset or an internal reset

Note: When the NACKF flag is set to 1, the RIIC suspends data transmission/reception. Writing to the ICDRT register in transmit mode or reading from the ICDRR register in receive mode with the NACKF flag set to 1 does not enable data transmit/receive operation. To restart data transmission/reception, set the NACKF flag to 0.

RDRF Flag (Receive Data Full Flag)

[Setting conditions]

- When receive data has been transferred from the ICDRS register to the ICDRR register
  This flag is set to 1 at the rising edge of the eighth or ninth SCL clock cycle (selected by the ICMR3.RDRFS bit)
- When the received slave address matches after a start condition (or a restart condition) is detected with the ICCR2.TRS bit set to 0

[Clearing conditions]

- When 0 is written to the RDRF bit after reading RDRF = 1
- When data is read from the ICDRR register
- When 1 is written to the ICCR1.IICRST bit to apply an RIIC reset or an internal reset

TEND Flag (Transmit End Flag)

[Setting condition]

- At the rising edge of the ninth SCL clock cycle while the TDRE flag is 1

[Clearing conditions]

- When 0 is written to the TEND bit after reading TEND = 1
- When data is written to the ICDRT register
- When a stop condition is detected
- When 1 is written to the ICCR1.IICRST bit to apply an RIIC reset or an internal reset

TDRE Flag (Transmit Data Empty Flag)

[Setting conditions]

- When data has been transferred from the ICDRT register to the ICDRS register and the ICDRT register becomes empty
- When the ICCR2.TRS bit is set to 1
- When the received slave address matches while the TRS bit is 1

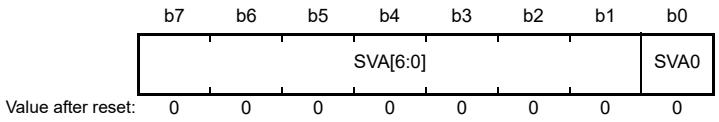
[Clearing conditions]

- When data is written to the ICDRT register
- When the ICCR2.TRS bit is set to 0
- When 1 is written to the ICCR1.IICRST bit to apply an RIIC reset or an internal reset

Note: When the NACKF flag is set to 1 while the ICFER.NACKE bit is 1, the RIIC suspends data transmission/reception. Here, if the TDRE flag is 0 (next transmit data has been written), data is transferred to the ICDRS register and the ICDRT register becomes empty at the rising edge of the ninth clock cycle, but the TDRE flag is not set to 1.

27.2.11 Slave Address Register Ly (SARLy) (y = 0 to 2)

Address(es): RIIC0.SARL0 0008 830Ah, RIIC0.SARL1 0008 830Ch, RIIC0.SARL2 0008 830Eh



Bit	Symbol	Bit Name	Description	R/W
b0	SVA0	10-Bit Address LSB	A slave address is set.	R/W
b7 to b1	SVA[6:0]	7-Bit Address/10-Bit Address Lower Bits	A slave address is set.	R/W

SVA0 Bit (10-Bit Address LSB)

When the 10-bit address format is selected (SARUy.FS bit is 1), this bit functions as the LSB of a 10-bit address and forms the lower 8 bits of a 10-bit address in combination with the SVA[6:0] bits.
When the ICSER.SARyE bit is set to 1 (SARLy and SARUy enabled) and the SARUy.FS bit is 1, this bit is valid. While the SARUy.FS bit or SARyE bit is 0, the setting of this bit is ignored.

SVA[6:0] Bits (7-Bit Address/10-Bit Address Lower Bits)

When the 7-bit address format is selected (SARUy.FS bit is 0), these bits function as a 7-bit address. When the 10-bit address format is selected (SARUy.FS bit is 1), these bits function as the lower 8 bits of a 10-bit address in combination with the SVA0 bit.
While the ICSER.SARyE bit is 0, the setting of these bits is ignored.

27.2.12 Slave Address Register Uy (SARUy) (y = 0 to 2)

Address(es): RIIC0.SARU0 0008 830Bh, RIIC0.SARU1 0008 830Dh, RIIC0.SARU2 0008 830Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SVA[1:0]		FS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	FS	7-Bit/10-Bit Address Format Select	0: The 7-bit address format is selected. 1: The 10-bit address format is selected.	R/W
b2, b1	SVA[1:0]	10-Bit Address Upper Bits	A slave address is set.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

FS Bit (7-Bit/10-Bit Address Format Select)

This bit is used to select 7-bit address or 10-bit address for slave address y (in registers SARLy and SARUy).

When the ICSER.SARyE bit is set to 1 (registers SARLy and SARUy enabled) and the SARUy.FS bit is 0, the 7-bit address format is selected for slave address y, the SARLy.SVA[6:0] bits setting is valid, and the settings of the SVA[1:0] bits and the SARLy.SVA0 bit are ignored.

When the ICSER.SARyE bit is set to 1 (registers SARLy and SARUy enabled) and the SARUy.FS bit is 1, the 10-bit address format is selected for slave address y and the settings of the SVA[1:0] bits and SARLy are valid.

While the ICSER.SARyE bit is 0 (registers SARLy and SARUy disabled), the setting of the SARUy.FS bit is invalid.

SVA[1:0] Bits (10-Bit Address Upper Bits)

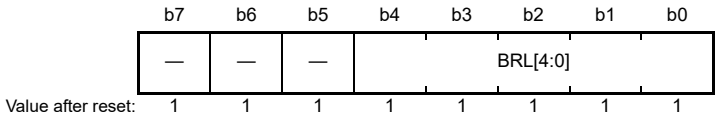
When the 10-bit address format is selected (FS = 1), these bits function as the upper 2 bits of a 10-bit address.

When the ICSER.SARyE bit is set to 1 (SARLy and SARUy enabled) and the SARUy.FS bit is 1, these bits are valid.

While the SARUy.FS bit or SARyE bit is 0, the setting of these bits is ignored.

27.2.13 I2C-bus Bit Rate Low-Level Register (ICBRL)

Address(es): RIIC0.ICBRL 0008 8310h



Bit	Symbol	Bit Name	Description	R/W
b4 to b0	BRL[4:0]	Bit Rate Low-Level Period	Low-level period of SCL clock	R/W
b7 to b5	—	Reserved	These bits are read as 1. The write value should be 1.	R/W

ICBRL is a 5-bit register to set the low-level period of SCL clock.
It also works to generate the data setup time for automatic SCL low-hold operation (refer to section 27.8, Automatic Low-Hold Function for SCL); when the RIIC is used only in slave mode, this register needs to be set to a value longer than the data setup time*1.
ICBRL counts the low-level period with the internal reference clock (IICφ) specified by the ICMR1.CKS[2:0] bits.
If the digital noise filter is enabled (the ICFER.NFE bit is 1), set the ICBRL register to a value at least one greater than the number of stages in the noise filter. Regarding the number of stages in the noise filter, see the description of the ICMR3.NF[1:0] bits.

Note 1. Data setup time (tSU: DAT)
250 ns (up to 100 kbps: Standard-mode (Sm))
100 ns (up to 400 kbps: Fast-mode (Fm))

27.2.14 I2C-bus Bit Rate High-Level Register (ICBRH)

Address(es): RIIC0.ICBRH 0008 8311h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	BRH[4:0]				
Value after reset:	1	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	BRH[4:0]	Bit Rate High-Level Period	High-level period of SCL clock	R/W
b7 to b5	—	Reserved	These bits are read as 1. The write value should be 1.	R/W

ICBRH is a 5-bit register to set the high-level period of SCL clock. ICBRH is valid in master mode. If the RIIC is used only in slave mode, this register need not to set the high-level period.
ICBRH counts the high-level period with the internal reference clock (IICφ) specified by the ICMR1.CKS[2:0] bits.
If the digital noise filter is enabled (the ICFER.NFE bit is 1), set the ICBRH register to a value at least one greater than the number of stages in the noise filter. Regarding the number of stages in the noise filter, see the description of the ICMR3.NF[1:0] bits.

The I2C transfer rate and the SCL clock duty are calculated using the following expression.
Transfer rate = 1 / {[(ICBRH + 1) + (ICBRL + 1)] / IICφ*1 + SCL0 line rising time [tr] + SCL0 line falling time [tf]}
Duty cycle = {SCL0 line rising time [tr]*2 + (ICBRH + 1) / IICφ} / {SCL0 line falling time [tf]*2 + (ICBRL + 1) / IICφ}

Note 1. IICφ = PCLK × Division ratio
Note 2. The SCL0 line rising time [tr] and SCL0 line falling time [tf] depend on the total bus line capacitance [Cb] and the pull-up resistor [Rp]. For details, see the I2C-bus specification from NXP Semiconductors.

Table 27.5 lists examples of ICBRH/ICBRL settings.

Table 27.5 Examples of ICBRH/ICBRL Settings for Transfer Rate

Transfer Rate (kbps)	Operating Frequency PCLK (MHz)								
	8			10			12.5		
	CKS[2:0]	ICBRH	ICBRL	CKS[2:0]	ICBRH	ICBRL	CKS[2:0]	ICBRH	ICBRL
10	100b	22 (F6h)	25 (F9h)	101b	13 (EDh)	15 (EFh)	101b	16 (F0h)	20 (F4h)
50	010b	16 (F0h)	19 (F3h)	010b	21 (F5h)	24 (F8h)	011b	12 (ECh)	15 (EFh)
100	001b	15 (EFh)	18 (F2h)	001b	19 (F3h)	23 (F7h)	001b	24 (F8h)	29 (FDh)
400	000b	4 (E4h)	10 (EAh)	000b	5 (E5h)	12 (ECh)	000b	7 (E7h)	16 (F0h)

Transfer Rate (kbps)	Operating Frequency PCLK (MHz)								
	16			20			25		
	CKS[2:0]	ICBRH	ICBRL	CKS[2:0]	ICBRH	ICBRL	CKS[2:0]	ICBRH	ICBRL
10	101b	22 (F6h)	25 (F9h)	110b	13 (EDh)	15 (EFh)	110b	16 (F0h)	20 (F4h)
50	011b	16 (F0h)	19 (F3h)	011b	21 (F5h)	24 (F8h)	100b	12 (ECh)	15 (EFh)
100	010b	15 (EFh)	18 (F2h)	010b	19 (F3h)	23 (F7h)	010b	24 (F8h)	29 (FDh)
400	000b	9 (E9h)	20 (F4h)	000b	11 (EBh)	25 (F9h)	001b	7 (E7h)	16 (F0h)

Transfer Rate (kbps)	Operating Frequency PCLK (MHz)								
	30			32			33		
	CKS[2:0]	ICBRH	ICBRL	CKS[2:0]	ICBRH	ICBRL	CKS[2:0]	ICBRH	ICBRL
10	110b	20 (F4h)	24 (F8h)	110b	22 (F6h)	25 (F9h)	110b	22 (F6h)	26 (FAh)
50	100b	15 (EFh)	18 (F2h)	100b	16 (F0h)	19 (F3h)	100b	17 (F1h)	20 (F4h)
100	010b	2 (E2h)	3 (E3h)	011b	15 (EFh)	18 (F2h)	011b	16 (F0h)	19 (F3h)
400	001b	8 (E8h)	19 (F3h)	001b	9 (E9h)	20 (F4h)	001b	9 (E9h)	21 (F5h)

Transfer Rate (kbps)	Operating Frequency PCLK (MHz)		
	40		
	CKS[2:0]	ICBRH	ICBRL
10	111b	13 (7Dh)	15 (7Fh)
50	100b	21 (F5h)	24 (F8h)
100	011b	19 (F3h)	23 (F7h)
400	001b	11 (7Bh)	25 (F9h)

Note: ICBRH/ICBRL settings in these tables are calculated using the following values:
SCL0 line rising time (tr): 100 kbps or less (Sm): 1000 ns, 400 kbps or less (Fm): 300 ns
SCL0 line falling time (tf): 400 kbps or less (Sm/Fm): 300 ns
For the specified values of SCL0 line rising time (tr) and SCL0 line falling time (tf), see the I2C-bus specification from NXP Semiconductors.

27.2.15 I2C-bus Transmit Data Register (ICDRT)

Address(es): RIIC0.ICDRT 0008 8312h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1

When the ICDRT register detects a space in the I2C-bus shift register (ICDRS), it transfers the transmit data that has been written to the ICDRT register to the ICDRS register and starts transmitting data in transmit mode.
The double-buffer structure of the ICDRT register and the ICDRS register allows continuous transmit operation if the next transmit data has been written to the ICDRT register while the ICDRS register data is being transmitted.
The ICDRT register can always be read and written. Write transmit data to the ICDRT register once when a transmit data empty interrupt (TXI) request is generated.

27.2.16 I2C-bus Receive Data Register (ICDRR)

Address(es): RIIC0.ICDRR 0008 8313h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0

When 1 byte of data has been received, the received data is transferred from the I2C-bus shift register (ICDRS) to the ICDRR register to enable the next data to be received.
The double-buffer structure of the ICDRS register and the ICDRR register allows continuous receive operation if the received data has been read from the ICDRR register while the ICDRS register is receiving data.
The ICDRR register cannot be written. Read data from the ICDRR register once when a receive data full interrupt (RXI) request is generated.
If the ICDRR register receives the next receive data before the current data is read from the ICDRR register (while the ICSR2.RDRF flag is 1), the RIIC automatically holds the SCL clock low one cycle before the RDRF flag is set to 1 next.

27.2.17 I2C-bus Shift Register (ICDRS)

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	—	—	—	—	—	—	—	—

The ICDRS register is an 8-bit shift register to transmit and receive data.
During transmission, transmit data is transferred from the ICDRT register to the ICDRS register and is sent from the SDA0 pin. During reception, data is transferred from the ICDRS register to the ICDRR register after 1 byte of data has been received.
The ICDRS register cannot be accessed directly.

27.3 Operation

27.3.1 Communication Data Format

The I2C-bus format consists of 8-bit data and 1-bit acknowledge. The first byte following a start condition or restart condition is an address byte used to specify a slave device with which the master device communicates. The specified slave is valid until a new slave is specified or a stop condition is issued.
Figure 27.3 shows the I2C-bus format, and Figure 27.4 shows the I2C-bus timing.

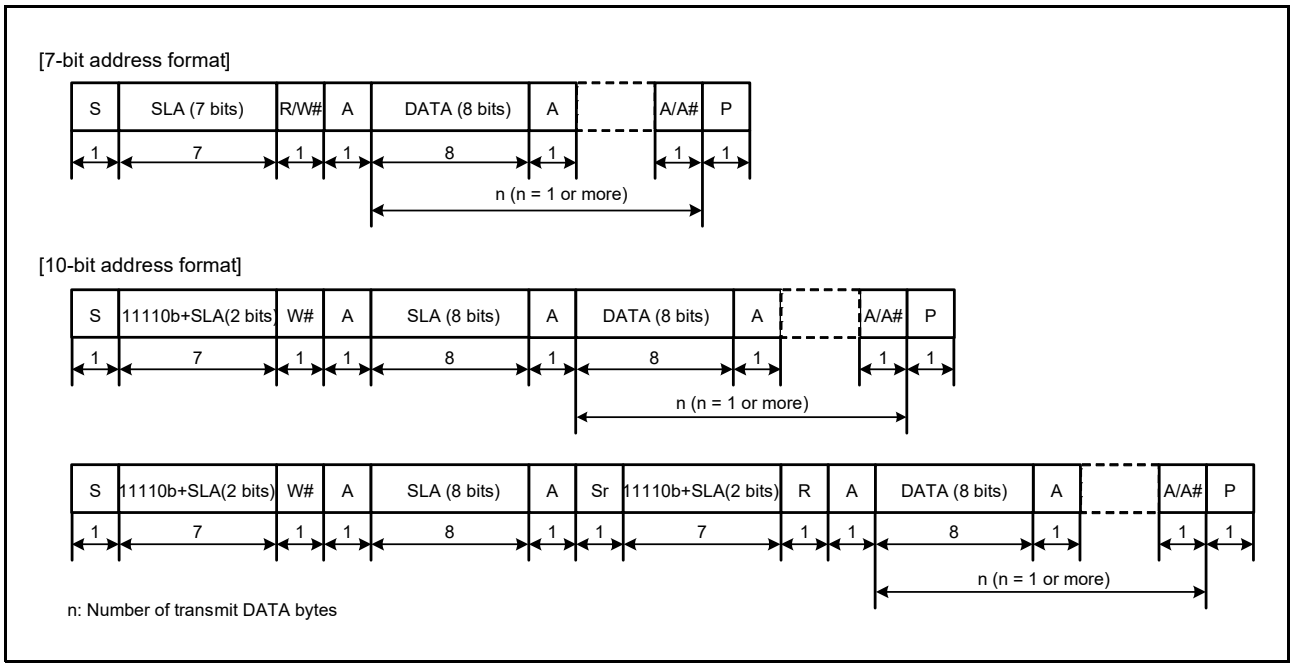


Figure 27.3 I2C-bus Format

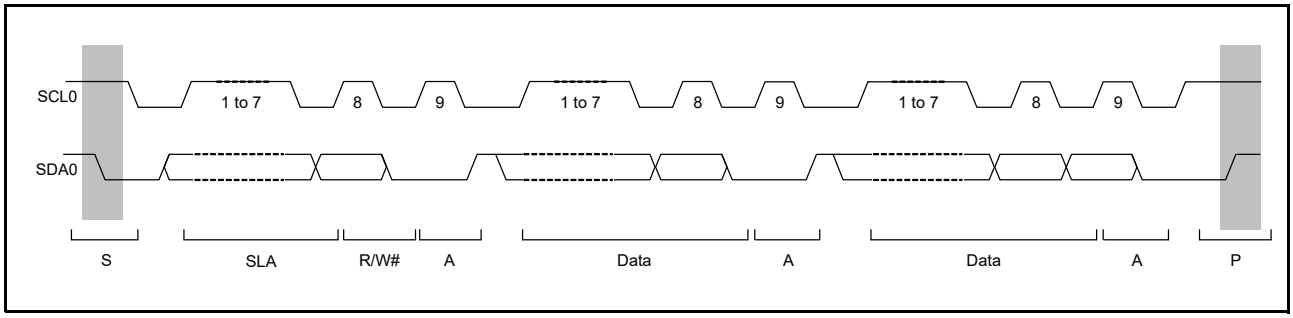


Figure 27.4 I2C-bus Timing (SLA = 7 Bits)

S: Start condition. The master device drives the SDA0 line low from high level while the SCL0 line is at a high level.

SLA: Slave address, by which the master device selects a slave device.

R/W#: Indicates the direction of data transfer: from the slave device to the master device when R/W is 1, or from the master device to the slave device when R/W is 0.

A: Acknowledge. The receive device drives the SDA0 line low. (In master transmit mode, the slave device returns acknowledge. In master receive mode, the master device returns acknowledge.)

A#: Not Acknowledge. The receive device drives the SDA0 line high.

Sr: Restart condition. The master device drives the SDA0 line low from the high level after the setup time has elapsed with the SCL0 line at the high level.

DATA: Transmitted or received data

P: Stop condition. The master device drives the SDA0 line high from low level while the SCL0 line is at a high level.

27.3.2 Initial Settings

Before starting data transmission and reception, initialize the RIIC according to the procedure in Figure 27.5.
Set the ICCR1.ICE bit to 1 (internal reset) after setting the ICCR1.IICRST bit to 1 (RIIC reset) with the ICCR1.ICE bit set to 0 (SCL0 and SDA0 pins in inactive state). This initializes the various flags and internal state of the ICSR1 register. After that, set registers SARLy, SARUy, ICSER, ICMR1, ICBRH, and ICBRL (y = 0 to 2), and set the other registers as necessary (for initial settings of the RIIC, see Figure 27.5). When the necessary register settings have been completed, set the ICCR1.IICRST bit to 0 (releases the RIIC reset). This step is not necessary if initialization of the RIIC has already been completed.

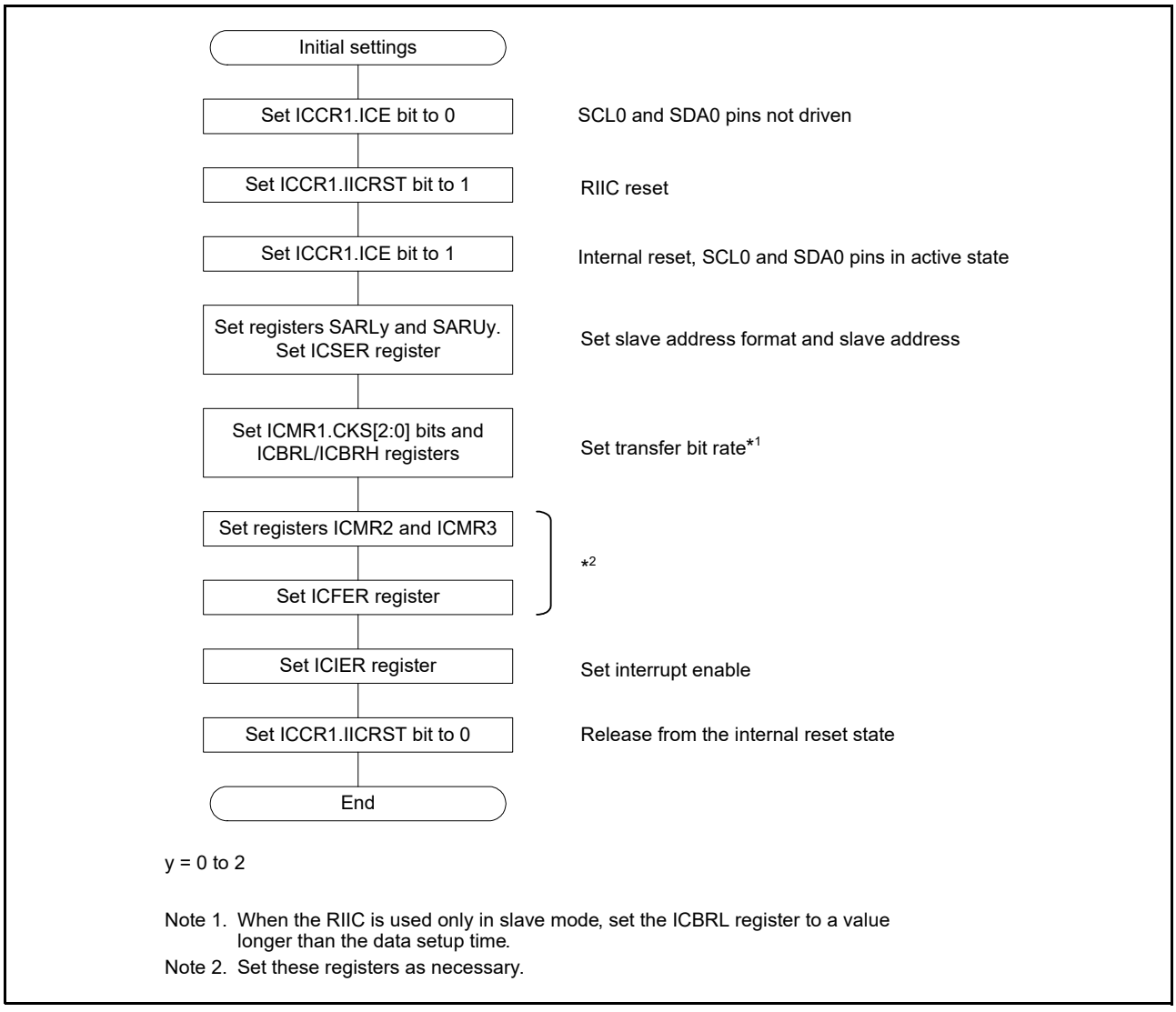


Figure 27.5 Example of RIIC Initialization Flowchart

27.3.3 Master Transmit Operation

In master transmit operation, the RIIC outputs the SCL clock and transmitted data signals as the master device, and the slave device returns acknowledgments. Figure 27.6 shows an example of usage of master transmission and Figure 27.7 to Figure 27.9 show the timing of operations in master transmission.
The following describes the procedure and operations for master transmission.

(1) Initial settings. For details, refer to section 27.3.2, Initial Settings.
(2) Read the ICCR2.BBSY flag to check that the bus is open, and then set the ICCR2.ST bit to 1 (start condition issuance request). Upon receiving the request, the RIIC issues a start condition. At the same time, the BBSY flag and the ICSR2.START flag are automatically set to 1 and the ST bit is automatically set to 0. At this time, if the start condition is detected and the internal levels for the SDA output state and the levels on the SDA0 line have matched while the ST bit is 1, the RIIC recognizes that issuing of the start condition as requested by the ST bit has been successfully completed, and bits MST and TRS in the ICCR2 register are automatically set to 1, placing the RIIC in master transmit mode. The ICSR2.TDRE flag is also automatically set to 1 in response to setting of the TRS bit to 1.
(3) Check that the ICSR2.TDRE flag is 1, and then write the value for transmission (the slave address and the R/W# bit) to the ICDRT register. Once the data for transmission are written to the ICDRT register, the TDRE flag is automatically set to 0, the data are transferred from the ICDRT register to the ICDRS register, and the TDRE flag is again set to 1. After the byte containing the slave address and R/W# bit has been transmitted, the value of the TRS bit is automatically updated to select master transmit or master receive mode in accord with the value of the transmitted R/W# bit. If the value of the R/W# bit was 0, the RIIC continues in master transmit mode.
Because the ICSR2.NACKF flag being 1 at this time indicates that no slave device recognized the address or there was an error in communications, write 1 to the ICCR2.SP bit to issue a stop condition.
For data transmission with an address in the 10-bit format, start by writing 1111 0b, the 2 higher-order bits of the slave address, and W to the ICDRT register as the first address transmission. Then, as the second address transmission, write the 8 lower-order bits of the slave address to the ICDRT register.
(4) After confirming that the ICSR2.TDRE flag is 1, write the data for transmission to the ICDRT register. The RIIC automatically holds the SCL0 line low until the data for transmission are ready or a stop condition is issued.
(5) After all bytes of data for transmission have been written to the ICDRT register, wait until the value of the ICSR2.TEND flag returns to 1, and then set the ICCR2.SP bit to 1 (stop condition issuance request). Upon receiving a stop condition issuance request, the RIIC issues the stop condition.
(6) Upon detecting the stop condition, the RIIC automatically sets bits MST and TRS in the ICCR2 register to 00b and enters slave receive mode. Furthermore, it automatically sets the TDRE and TEND flags to 0, and sets the ICSR2.STOP flag to 1.
(7) After checking that the ICSR2.STOP flag is 1, set the ICSR2.NACKF and STOP flags to 0 for the next transfer operation.

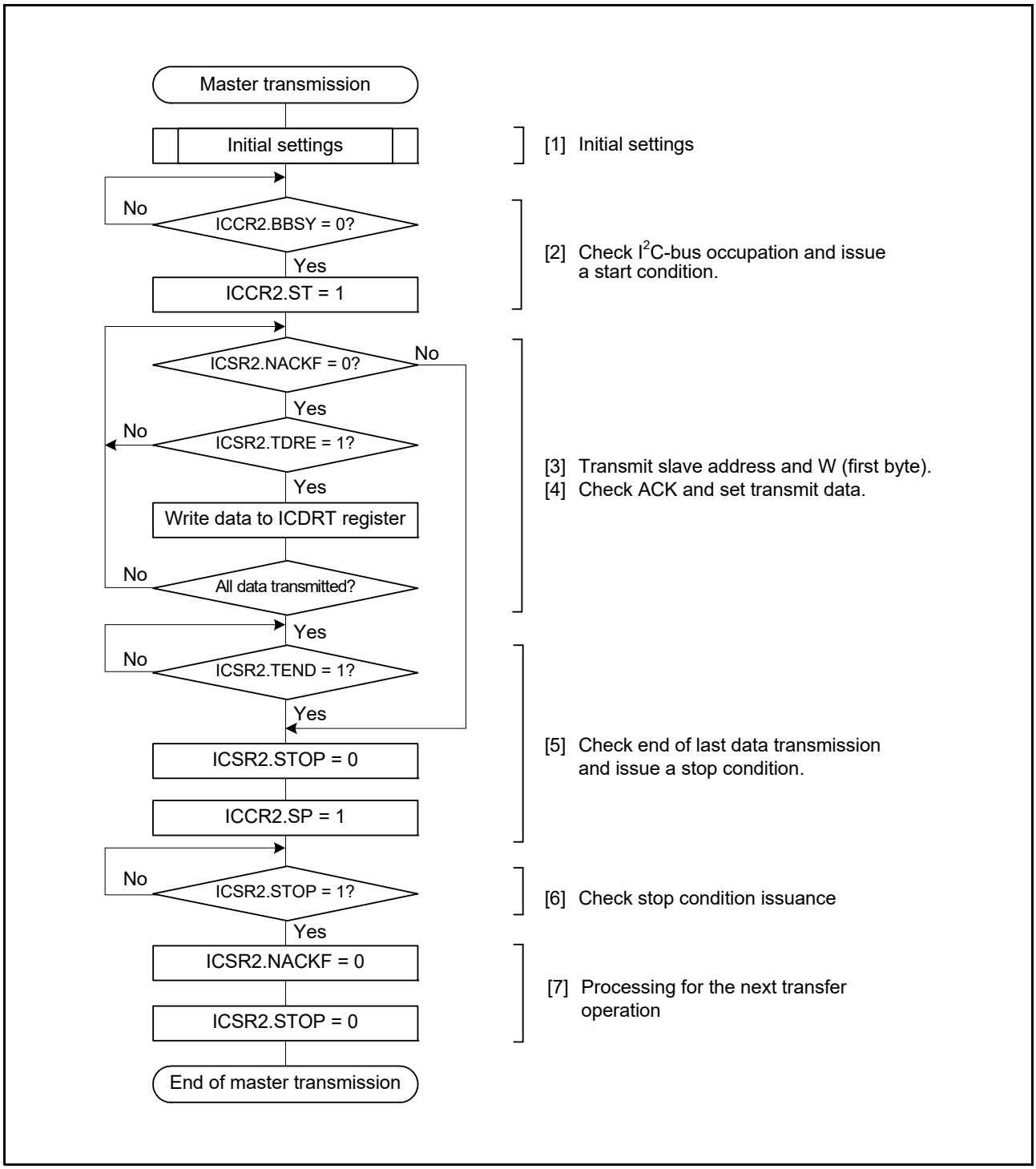


Figure 27.6 Example of Master Transmission Flowchart

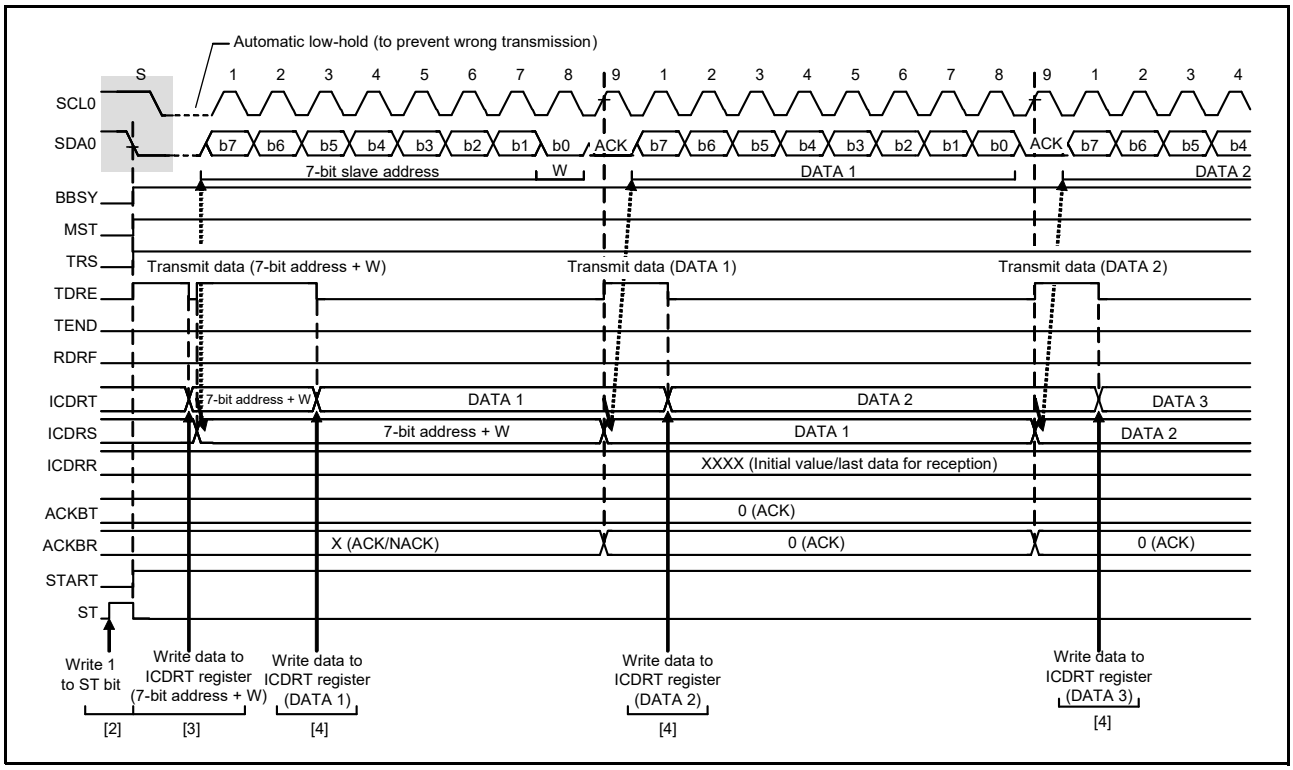


Figure 27.7 Master Transmit Operation Timing (1) (7-Bit Address Format)

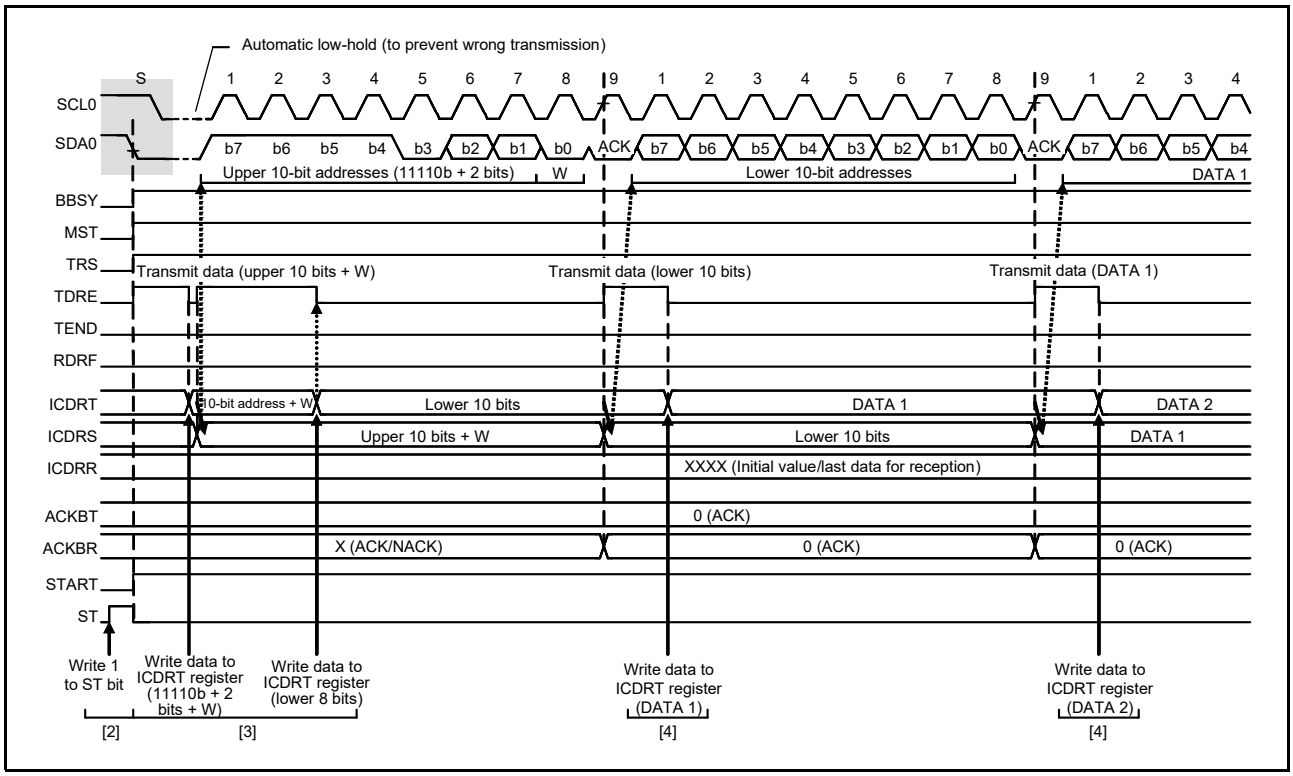


Figure 27.8 Master Transmit Operation Timing (2) (10-Bit Address Format)

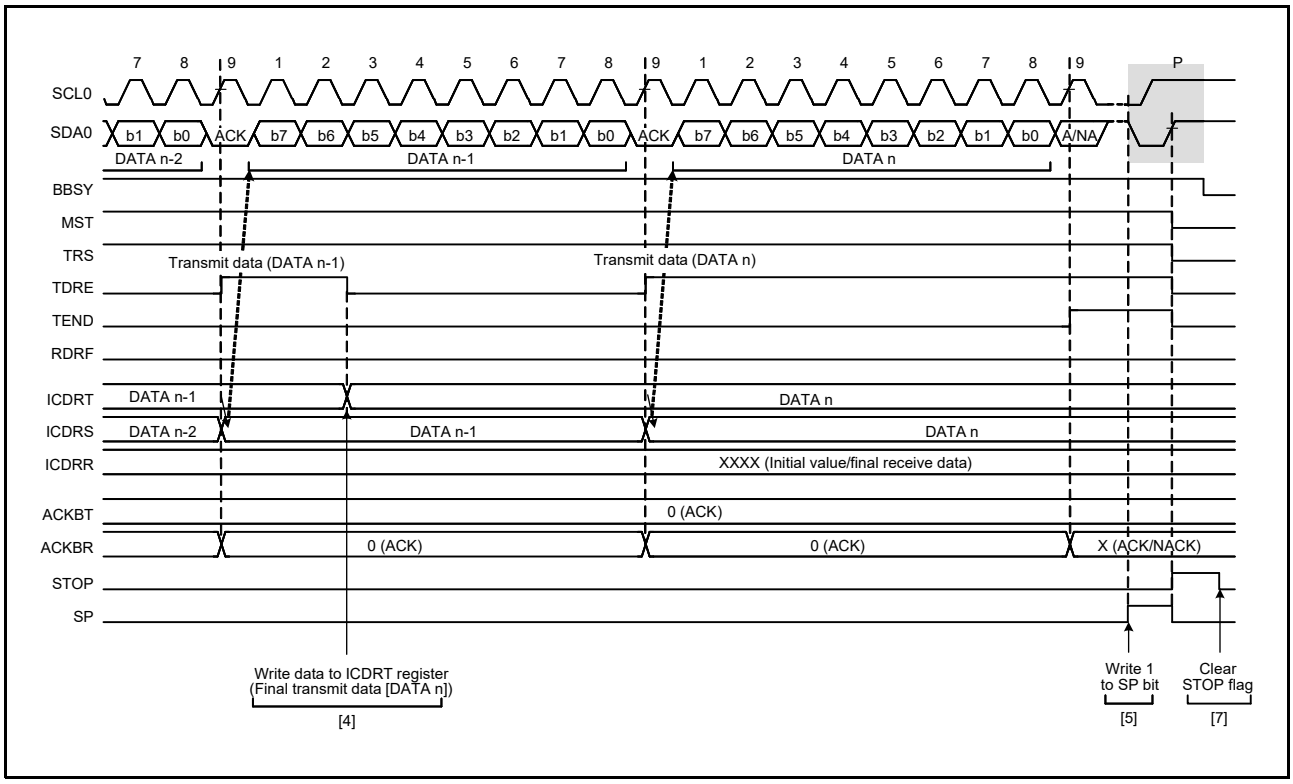


Figure 27.9 Master Transmit Operation Timing (3)

27.3.4 Master Receive Operation

In master receive operation, the RIIC as a master device outputs the SCL clock, receives data from the slave device, and returns acknowledgments. Because the RIIC must start by sending a slave address to the corresponding slave device, this part of the procedure is performed in master transmit mode, but the subsequent steps are in master receive mode.
Figure 27.10 and Figure 27.11 show examples of usage of master reception (7-bit address format) and Figure 27.12 to Figure 27.14 show the timing of operations in master reception.
The following describes the procedure and operations for master reception.

(1) Initial settings. For details, refer to section 27.3.2, Initial Settings.

(2) Read the ICCR2.BBSY flag to check that the bus is open, and then set the ICCR2.ST bit to 1 (start condition issuance request). Upon receiving the request, the RIIC issues a start condition. When the RIIC detects the start condition, the BBSY flag and the ICSR2.START flag are automatically set to 1 and the ST bit is automatically set to 0. At this time, if the start condition is detected and the levels for the SDA output and the levels on the SDA0 line have matched while the ST bit is 1, the RIIC recognizes that issuing of the start condition as requested by the ST bit has been successfully completed, and bits MST and TRS in the ICCR2 register are automatically set to 1, placing the RIIC in master transmit mode. The ICSR2.TDRE flag is also automatically set to 1 in response to setting of the TRS bit to 1.

(3) Check that the ICSR2.TDRE flag is 1, and then write the value for transmission (the first byte indicates the slave address and value of the R/W# bit) to the ICDRT register. Once the data for transmission are written to the ICDRT register, the TDRE flag is automatically set to 0, the data are transferred from the ICDRT register to the ICDRS register, and the TDRE flag is again set to 1. Once the byte containing the slave address and R/W# bit has been transmitted, the value of the ICCR2.TRS bit is automatically updated to select transmit or receive mode in accord with the value of the transmitted R/W# bit. If the value of the R/W# bit was 1, the TRS bit is set to 0 on the rising edge of the ninth cycle of SCL clock, placing the RIIC in master receive mode. At this time, the TDRE flag is set to 0 and the ICSR2.RDRF flag is automatically set to 1.

Because the ICSR2.NACKF flag being 1 at this time indicates that no slave device recognized the address or there was an error in communications, write 1 to the ICCR2.SP bit to issue a stop condition.
For master reception from a device with a 10-bit address, start by using master transmission to issue the 10-bit address, and then issue a restart condition. After that, transmitting 1111 0b, the two higher-order bits of the slave address, and the R bit places the RIIC in master receive mode.

(4) Dummy read the ICDRR register after confirming that the ICSR2.RDRF flag is 1; this makes the RIIC start output of the SCL clock and start data reception.

(5) After 1 byte of data has been received, the ICSR2.RDRF flag is set to 1 on the rising edge of the eighth or ninth cycle of SCL clock (the clock signal) as selected by the ICMR3.RDRFS bit. Reading the ICDRR register at this time will produce the received data, and the RDRF flag is automatically set to 0 at the same time. Furthermore, the value of the acknowledgment field received during the ninth cycle of SCL clock is returned as the value set in the ICMR3.ACKBT bit. Furthermore, if the next byte to be received is the next to last byte, set the ICMR3.WAIT bit to 1 (for wait insertion) before reading the ICDRR register (containing the second byte from last). As well as enabling NACK output even in the case of delays in processing to set the ICMR3.ACKBT bit to 1 (NACK) in step (6), due to other interrupts, etc., this fixes the SCL0 line to the low level on the falling edge of the ninth clock cycle in reception of the last byte, so the state is such that issuing a stop condition is possible.

(6) When the ICMR3.RDRFS bit is 0 and the slave device must be notified that it is to end transfer for data reception after transfer of the next (final) byte, set the ICMR3.ACKBT bit to 1 (NACK).

(7) After reading the byte before last from the ICDRR register, if the value of the ICSR2.RDRF flag is confirmed to be 1, write 1 to the ICCR2.SP bit (stop condition issuance request) and then read the last byte from the ICDRR register. When the ICDRR register is read, the RIIC is released from the wait state and issues the stop condition after low-level output in the ninth clock cycle is completed or the SCL0 line is released from the low-hold state.

(8) Upon detecting the stop condition, the RIIC automatically sets bits MST and TRS in the ICCR2 register to 00b and enters slave receive mode. Furthermore, detection of the stop condition leads to setting of the ICSR2.STOP flag to 1.

(9) After checking that the ICSR2.STOP flag is 1, set the ICSR2.NACKF and STOP flags to 0 for the next transfer operation.

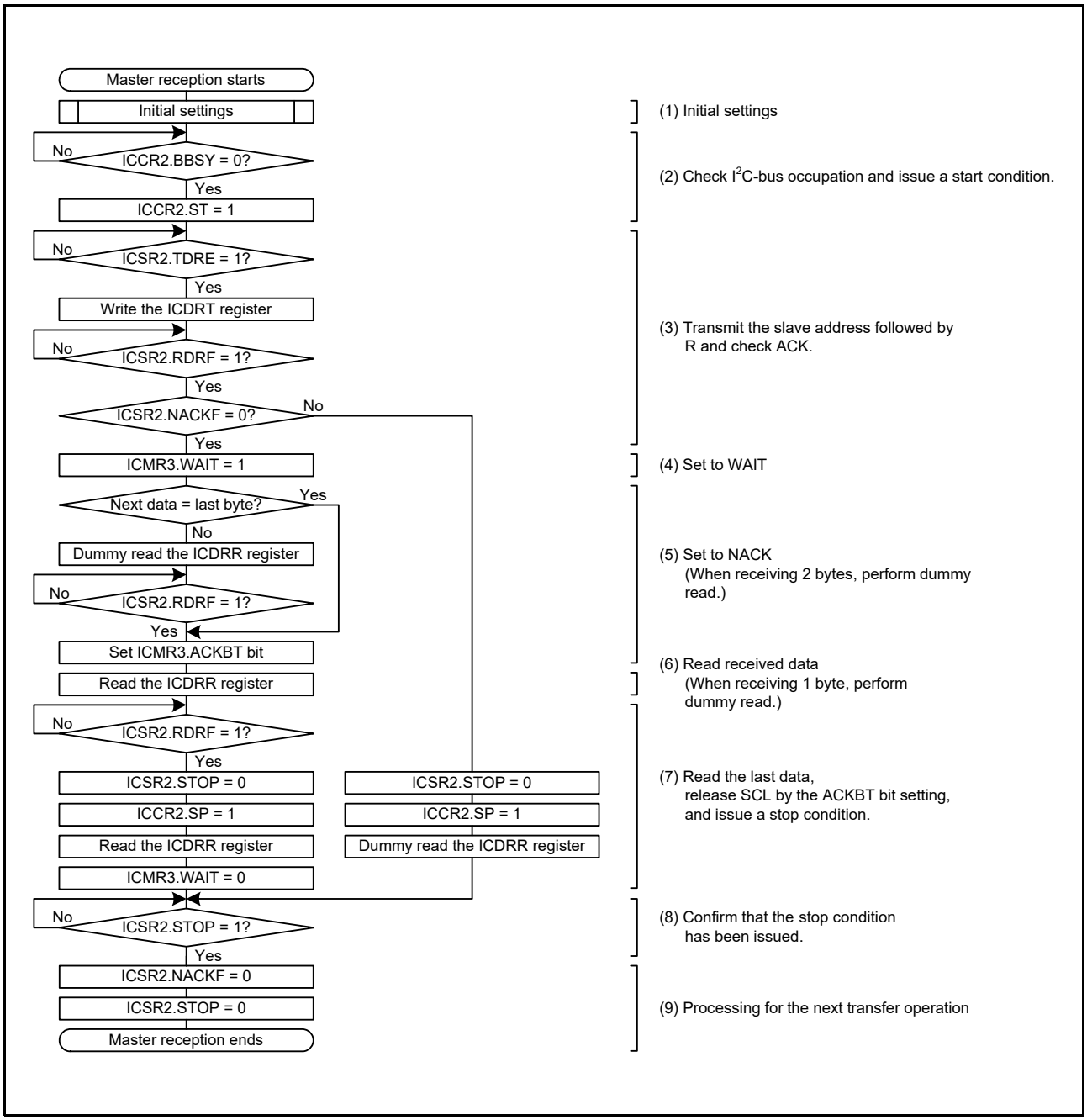


Figure 27.10 Example of Master Reception (7-Bit Address Format, 1 or 2 bytes)

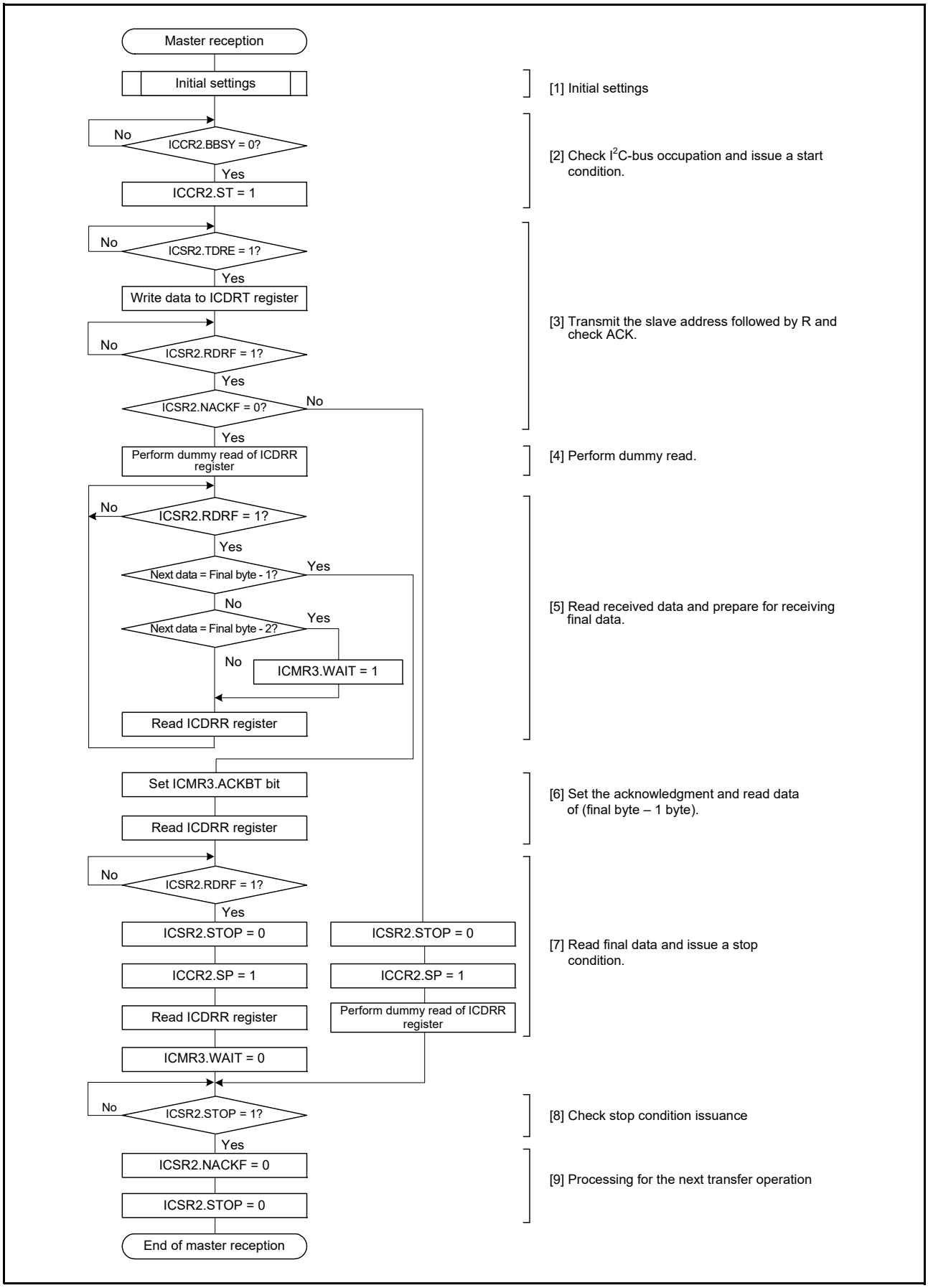


Figure 27.11 Example of Master Reception (7-Bit Address Format, 3 Bytes or More)

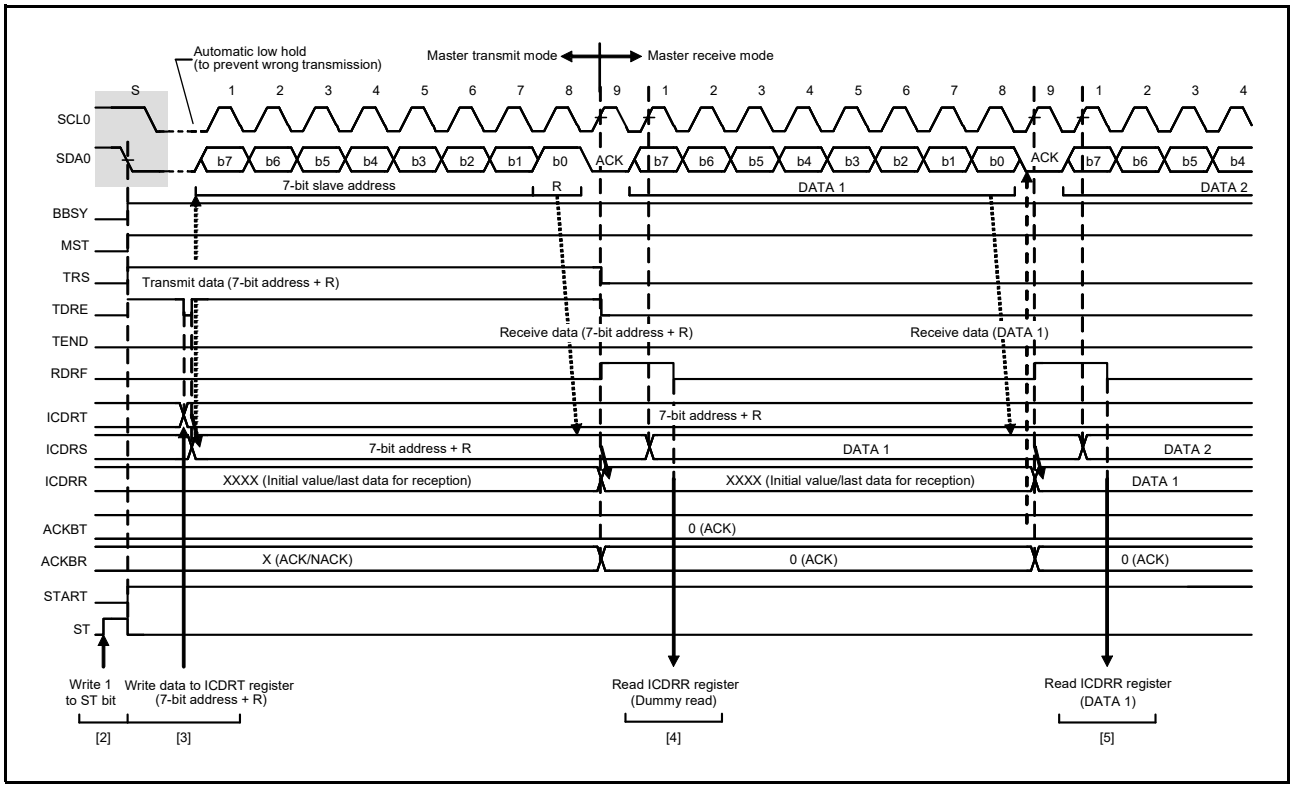


Figure 27.12 Master Receive Operation Timing (1) (7-Bit Address Format, When RDRFS bit is 0)

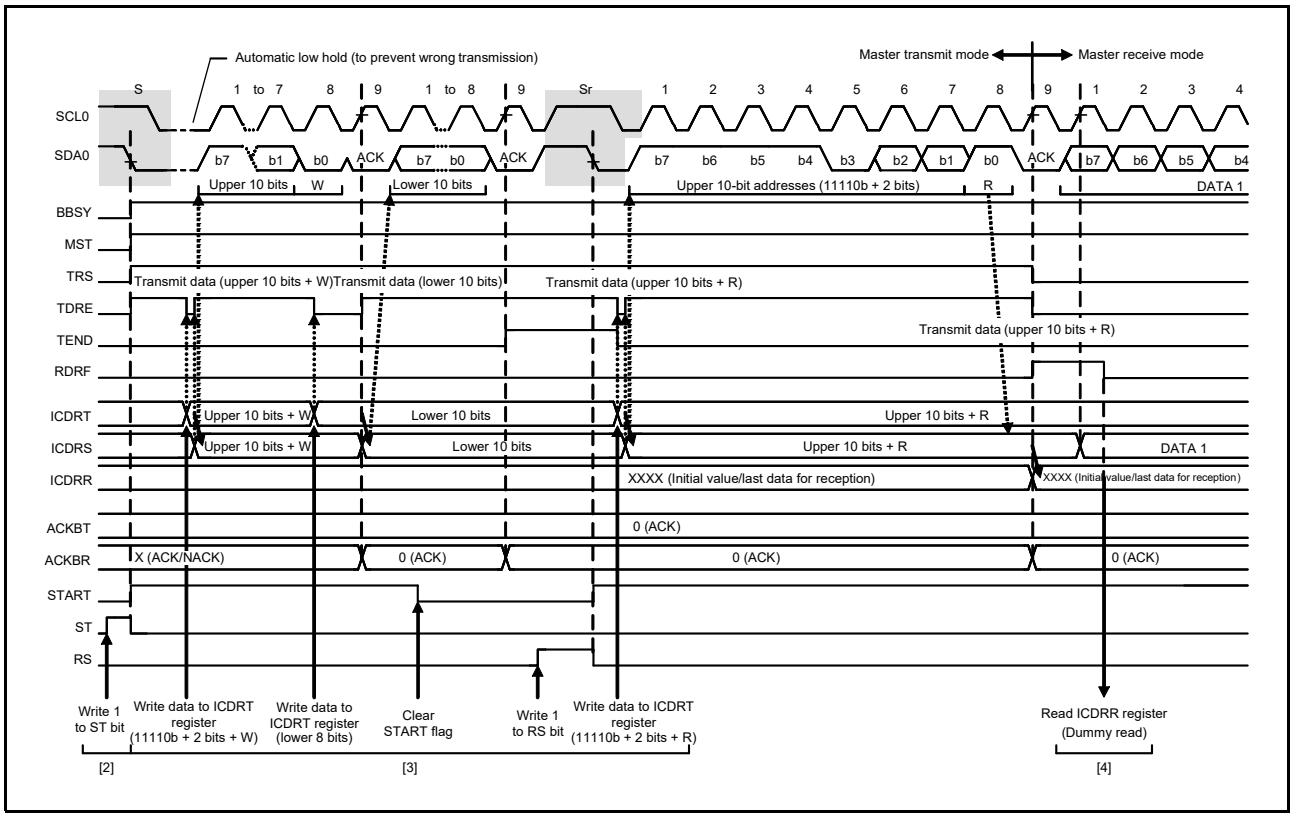


Figure 27.13 Master Receive Operation Timing (2) (10-Bit Address Format, When RDRFS bit is 0)

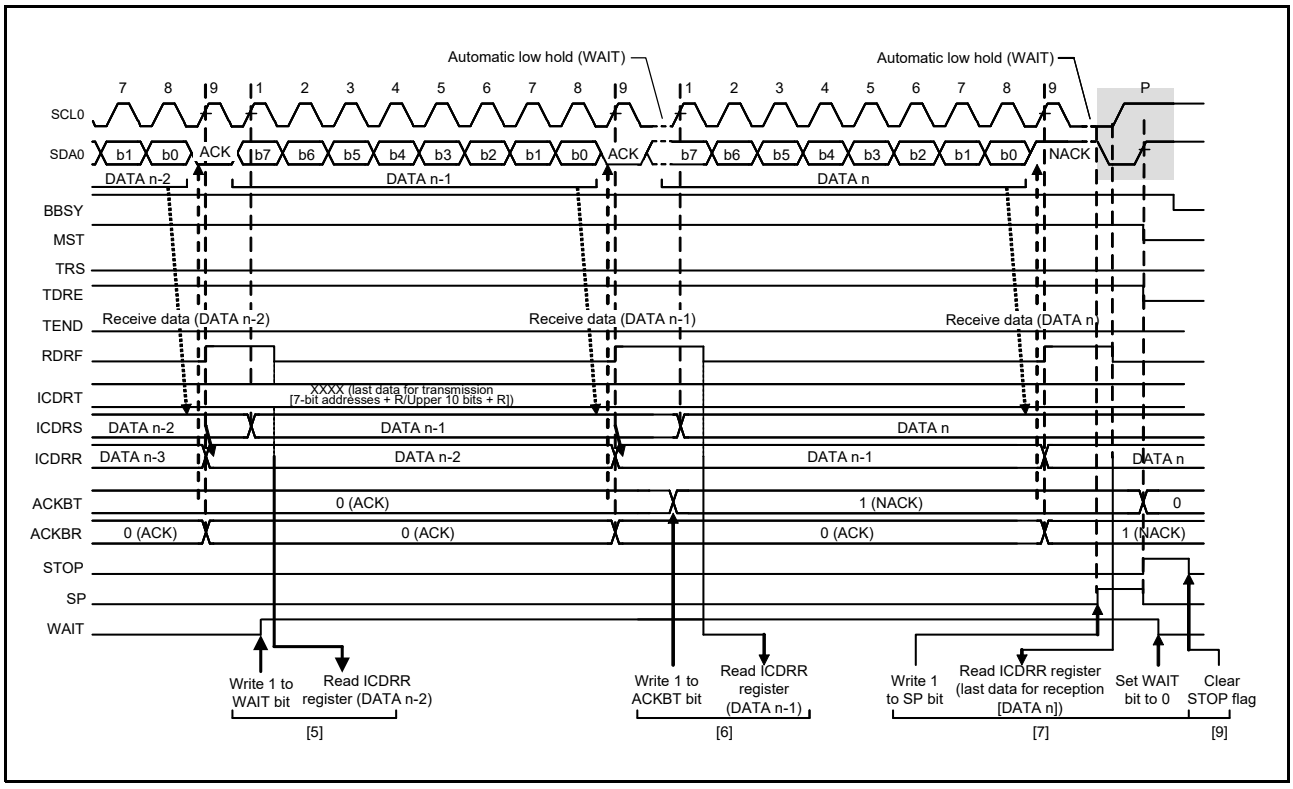


Figure 27.14 Master Receive Operation Timing (3) (When RDRFS bit is 0)

27.3.5 Slave Transmit Operation

In slave transmit operation, the master device outputs the SCL clock, the RIIC transmits data as a slave device, and the master device returns acknowledgments.

Figure 27.15 shows an example of usage of slave transmission and Figure 27.16 and Figure 27.17 show the timing of operations in slave transmission.

The following describes the procedure and operations for slave transmission.

(1) Initial settings. For details, refer to section 27.3.2, Initial Settings.
After initial settings, the RIIC will stay in the standby state until it receives a slave address that it matches.

(2) After receiving a matching slave address, the RIIC sets one of the corresponding bits ICSR1.HOA, GCA, and AASy (y = 0 to 2) to 1 on the rising edge of the ninth cycle of SCL clock (the clock signal) and outputs the value set in the ICMR3.ACKBT bit to the acknowledge bit on the ninth cycle of SCL clock. If the value of the R/W# bit that was also received at this time is 1, the RIIC automatically places itself in slave transmit mode by setting both the ICCR2.TRS bit and the ICSR2.TDRE flag to 1.

(3) After the ICSR2.TDRE flag is confirmed to be 1, write the data for transmission to the ICDRT register. At this time, if the RIIC does not receive acknowledge from the master device (receives an NACK signal) while the ICFER.NACKE bit is 1, the RIIC suspends transfer of the next data.

(4) Wait until the ICSR2.TEND flag is set to 1 while the ICSR2.TDRE flag is 1, after the ICSR2.NACKF flag is set to 1 or the last byte for transmission is written to the ICDRT register. When the ICSR2.NACKF flag or the TEND flag is 1, the RIIC drives the SCL0 line low on the ninth falling edge of SCL clock.

(5) When the ICSR2.NACKF flag or the ICSR2.TEND flag is 1, dummy read the ICDRR register to complete the processing. This releases the SCL0 line.

(6) Upon detecting the stop condition, the RIIC automatically sets bits ICSR1.HOA, GCA, and AASy (y = 0 to 2), flags ICSR2.TDRE and TEND, and the ICCR2.TRS bit to 0, and enters slave receive mode.

(7) After checking that the ICSR2.STOP flag is 1, set the ICSR2.NACKF and STOP flags to 0 for the next transfer operation.

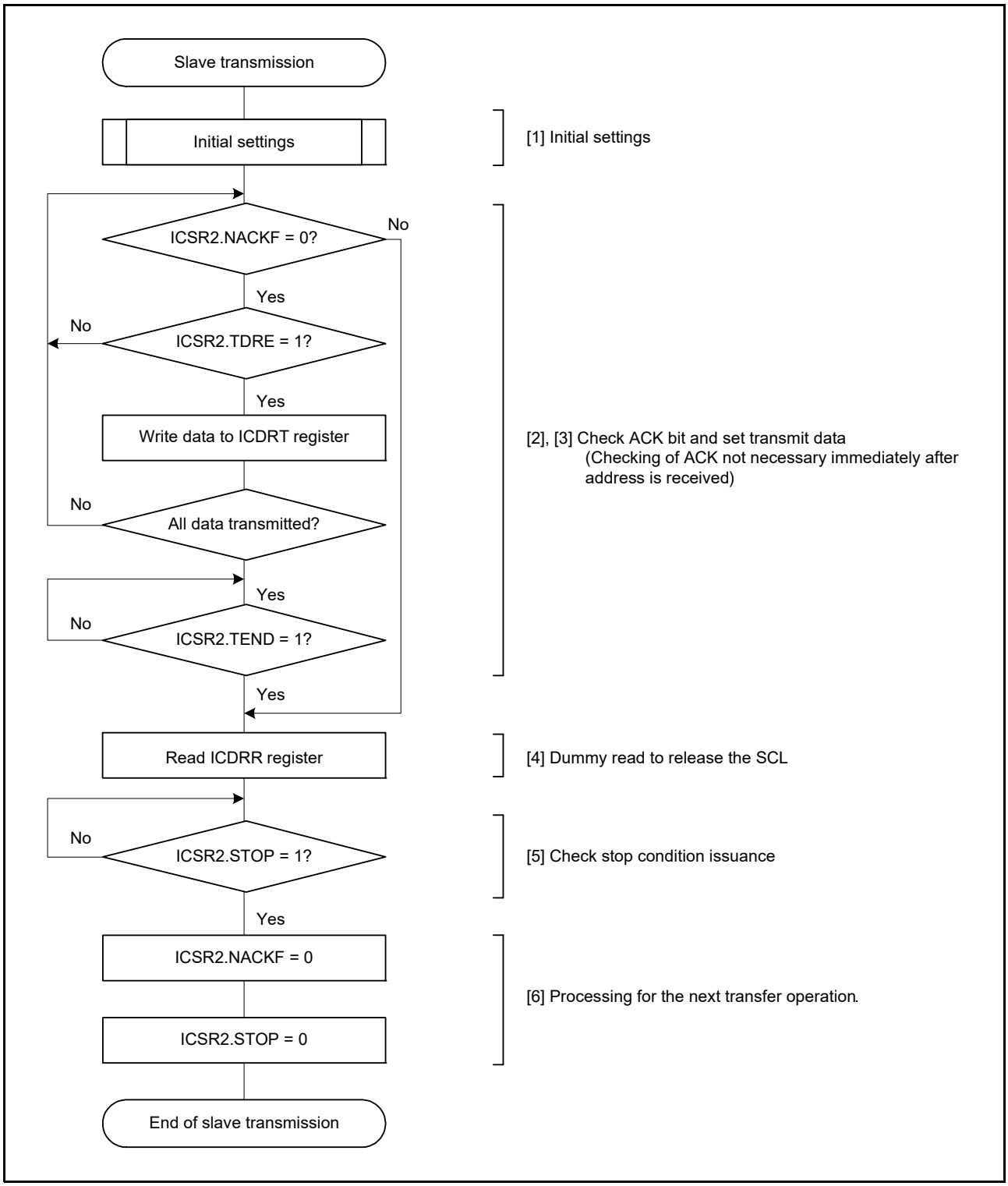


Figure 27.15 Example of Slave Transmission Flowchart

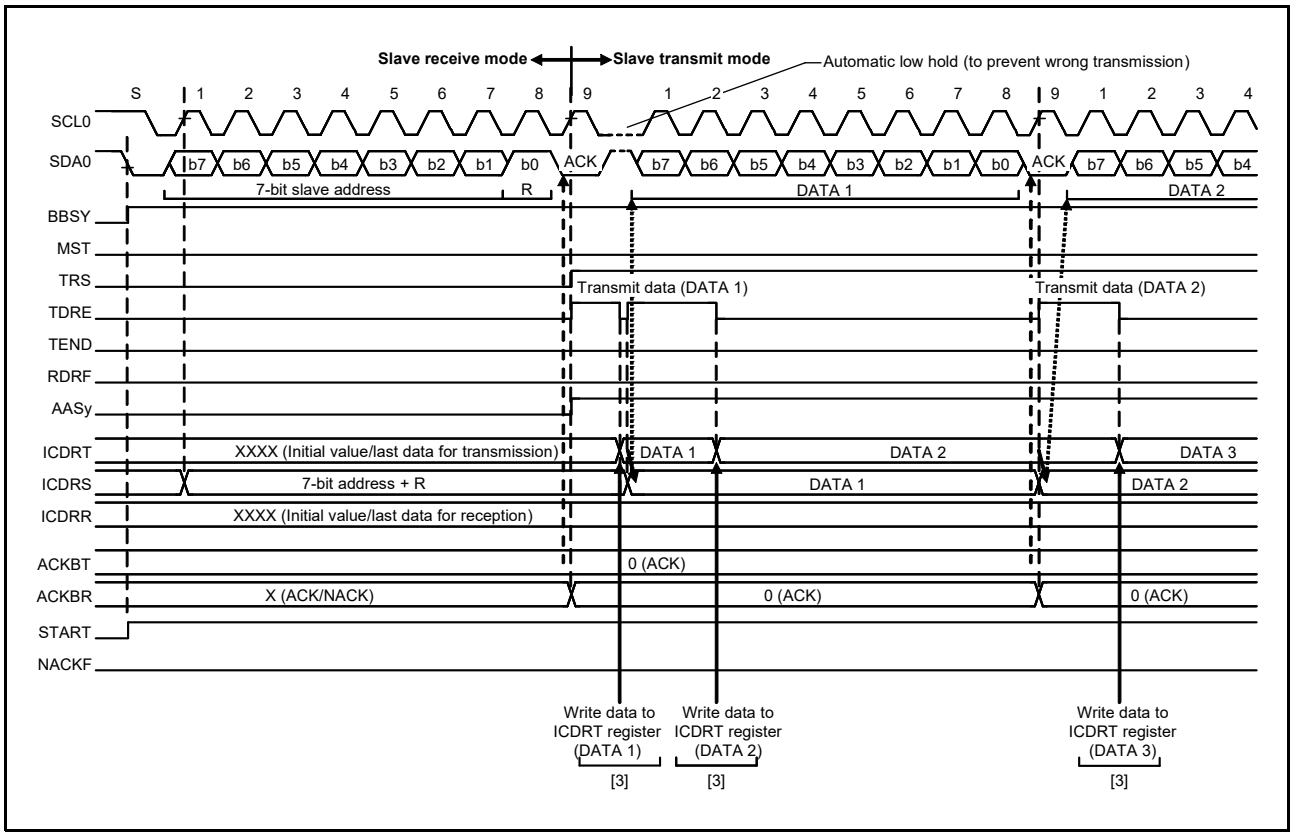


Figure 27.16 Slave Transmit Operation Timing (1) (7-Bit Address Format)

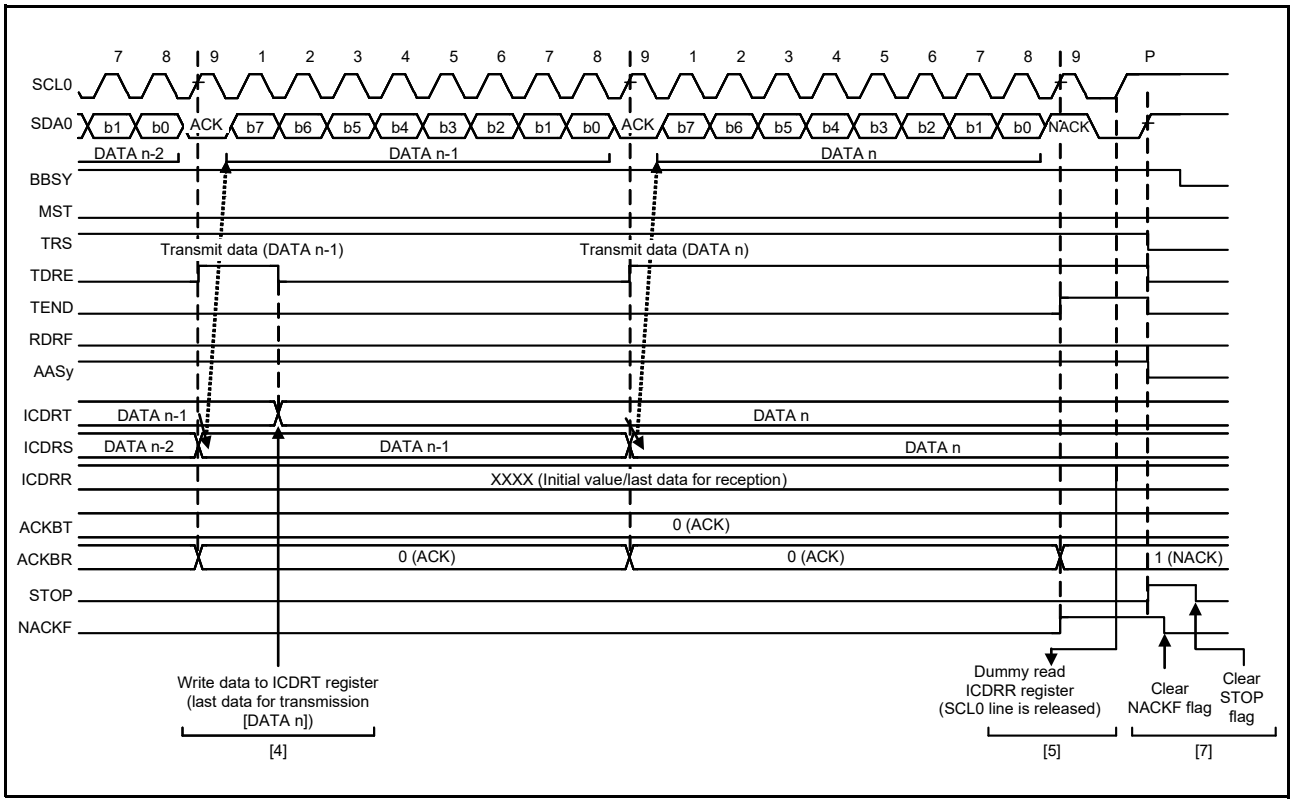


Figure 27.17 Slave Transmit Operation Timing (2)

27.3.6 Slave Receive Operation

In slave receive operation, the master device outputs the SCL clock and transmit data, and the RIIC returns acknowledgments as a slave device.

Figure 27.18 shows an example of usage of slave reception and Figure 27.19 and Figure 27.20 show the timing of operations in slave reception.

The following describes the procedure and operations for slave reception.

(1) Initial settings. For details, refer to section 27.3.2, Initial Settings.
After initial settings, the RIIC will stay in the standby state until it receives a slave address that it matches.

(2) After receiving a matching slave address, the RIIC sets one of the corresponding bits ICSR1.HOA, GCA, and AASy (y = 0 to 2) to 1 on the rising edge of the ninth cycle of SCL clock (the clock signal) and outputs the value set in the ICMR3.ACKBT bit to the acknowledge bit on the ninth cycle of SCL clock. If the value of the R/W# bit that was also received at this time is 0, the RIIC continues to place itself in slave receive mode and sets the ICSR2.RDRF flag to 1.

(3) After the ICSR2.STOP flag is confirmed to be 0 and the ICSR2.RDRF flag to be 1, dummy read the ICDRR register (the dummy value consists of the slave address and R/W# bit when the 7-bit address format is selected, or the lower 8 bits when the 10-bit address format is selected).

(4) When the ICDRR register is read, the RIIC automatically sets the ICSR2.RDRF flag to 0. If reading of the ICDRR register is delayed and a next byte is received while the RDRF flag is still set to 1, the RIIC holds the SCL0 line low from one SCL cycle before the timing with which RDRF should be set. In this case, reading the ICDRR register releases the SCL0 line from being held at the low level.
When the ICSR2.STOP flag is 1 and the ICSR2.RDRF flag is also 1, read the ICDRR register until all the data is completely received.

(5) Upon detecting the stop condition, the RIIC automatically clears bits ICSR1.HOA, GCA, and AASy (y = 0 to 2) to 0.

(6) After checking that the ICSR2.STOP flag is 1, set the ICSR2.STOP flag to 0 for the next transfer operation.

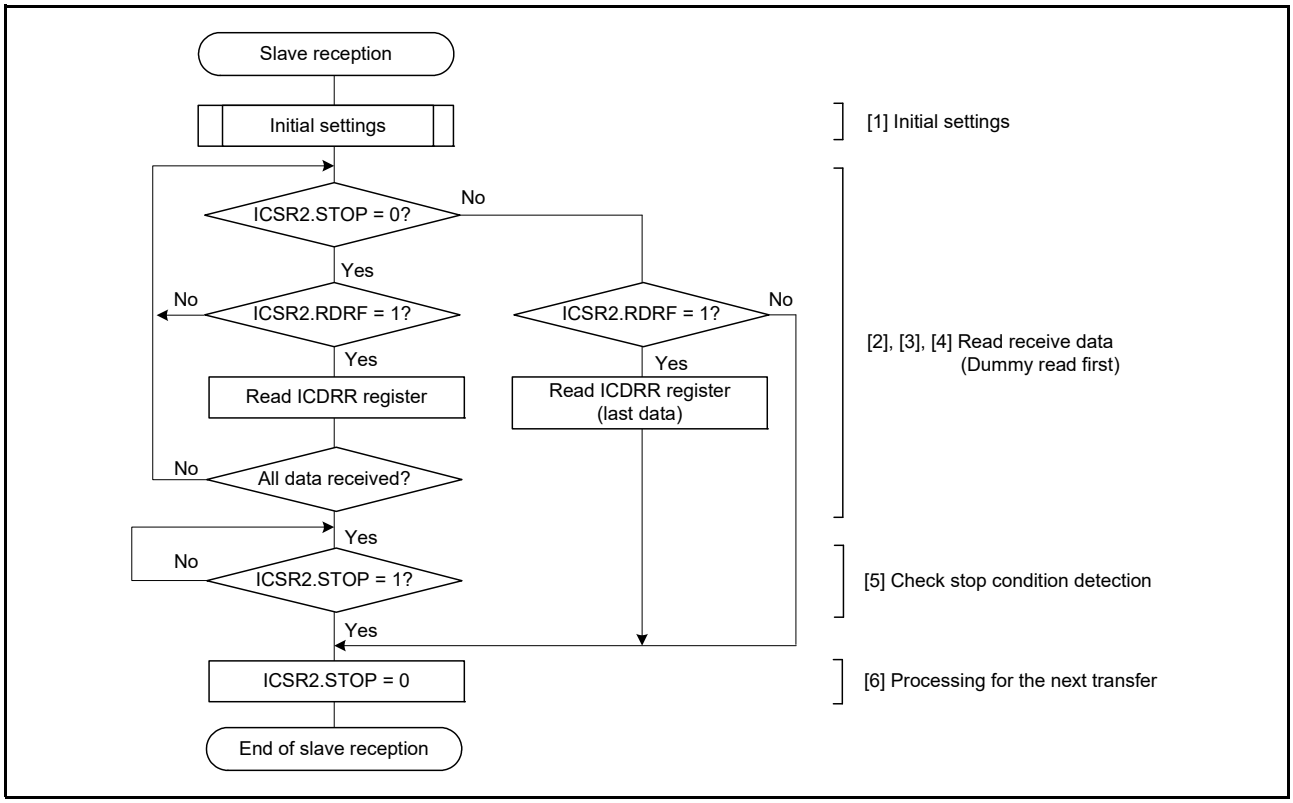


Figure 27.18 Example of Slave Reception Flowchart

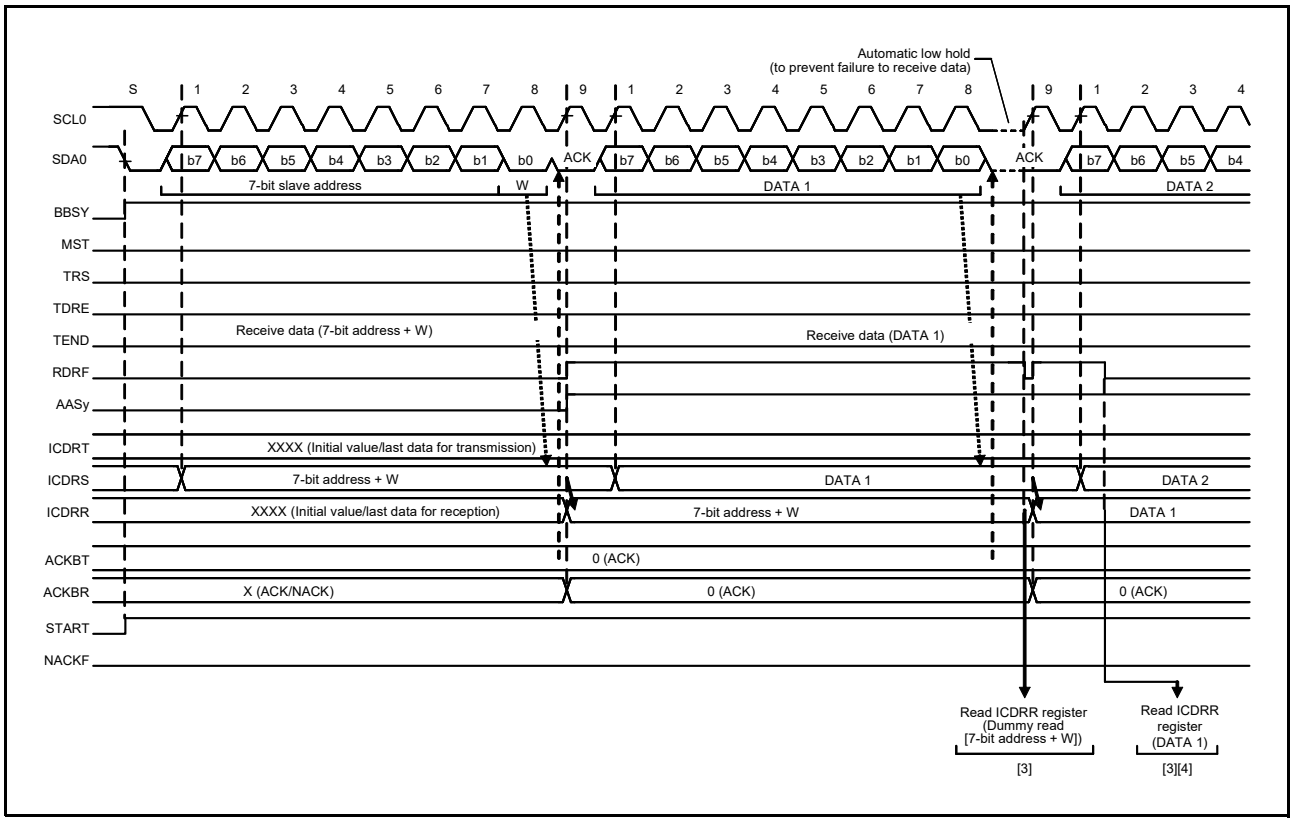


Figure 27.19 Slave Receive Operation Timing (1) (7-Bit Address Format, when RDRFS bit is 0)

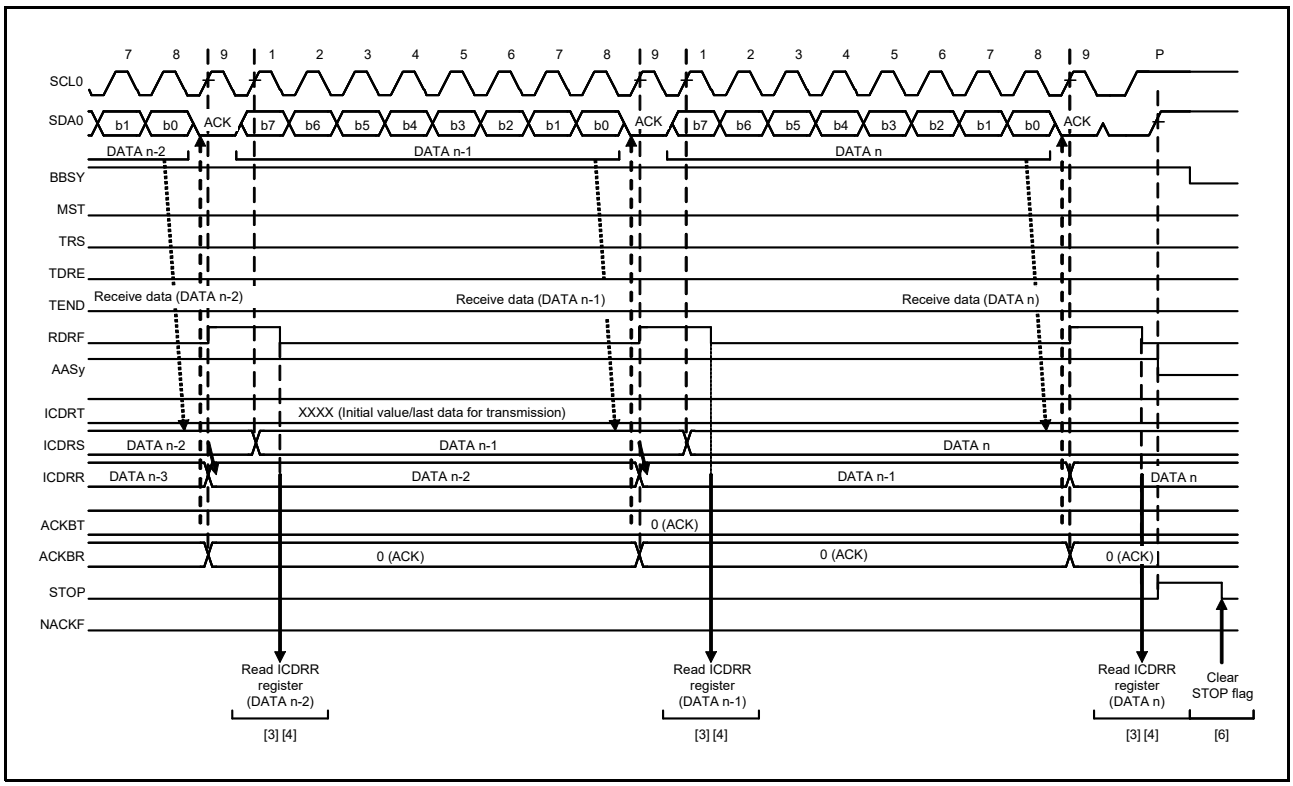


Figure 27.20 Slave Receive Operation Timing (2) (when RDRFS bit is 0)

27.4 SCL Synchronization Circuit

In generation of the SCL clock, the RIIC starts counting out the value for width at high level specified in the ICBRH register when it detects a rising edge on the SCL0 line and drives the SCL0 line low once counting of the width at high level is complete. When the RIIC detects the falling edge of the SCL0 line, it starts counting out the width at low level period specified in the ICBRL register, and then stops driving the SCL0 line (releases the line) once counting of the width at low level is complete. The SCL clock is thus generated.

If multiple master devices are connected to the I2C-bus, a collision of SCL signals may arise due to contention with another master device. In such cases, the master devices have to synchronize their SCL signals. Because this synchronization of SCL signals must be bit by bit, the RIIC is equipped with a facility (the SCL synchronization circuit) to obtain bit-by-bit synchronization of the SCL clock signals by monitoring the SCL0 line while in master mode.

When the RIIC has detected a rising edge on the SCL0 line and thus started counting out the width at high level specified in the ICBRH register, and the level on the SCL0 line falls because an SCL signal is being generated by another master device, the RIIC stops counting when it detects the falling edge, drives the level on the SCL0 line low, and starts counting out the width at low level specified in the ICBRL register. When the RIIC finishes counting out the width at low level, it stops driving the SCL0 line to the low level (i.e. releases the line). At this time, if the width at low level of the SCL clock signal from the other master device is longer than the width at low level set in the RIIC, the width at low level of the SCL signal will be extended. Once the width at low level for the other master device has ended, the SCL signal rises because the SCL0 line has been released. When the RIIC finishes outputting the low-level period of the SCL clock, the SCL0 line is released and the SCL clock rises. That is, in cases of contention of SCL signals from more than one master, the width at high level of the SCL signal is synchronized with that of the clock having the narrower width, and the width at low level of the SCL signal is synchronized with that of the clock having the broader width. However, such synchronization of the SCL signal is only enabled when the ICFER.SCLE bit is set to 1.

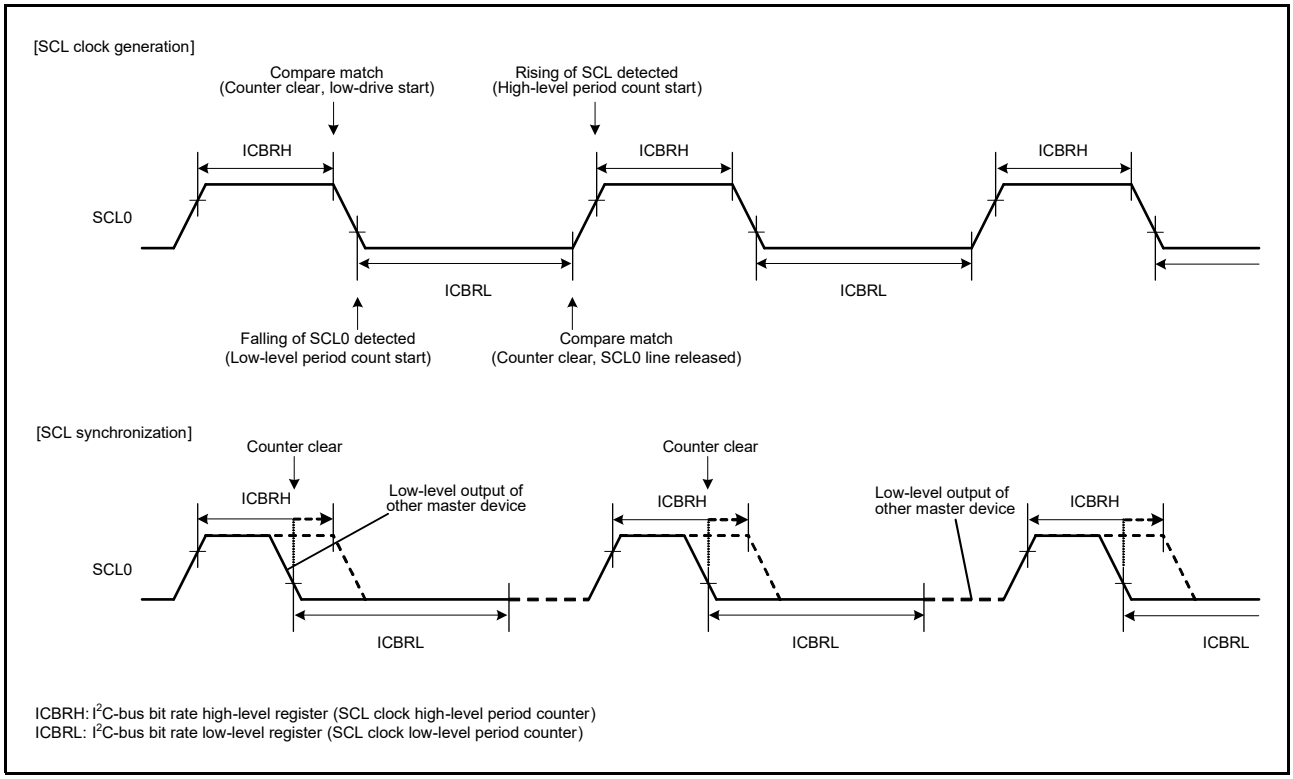


Figure 27.21 Generation and Synchronization of the SCL Signal from the RIIC

27.5 SDA Output Delay Function

The RIIC module incorporates a function for delaying output on the SDA line. The delay can be applied to all output (issuing of the start, restart, and stop conditions, data, and the ACK and NACK signals) on the SDA line.

With the SDA output delay function, SDA output is delayed from detection of a falling edge of the SCL signal to ensure that the SDA signal is output within the interval over which the SCL clock is at the low level. Doing this leads to usage with the aim of preventing erroneous operation of communications devices, with the aim of satisfying the 300-ns (min.) data-hold time requirement of the SMBus specification.

The output delay function is enabled by setting the ICMR2.SDDL[2:0] bits to any value other than 000b, and disabled by setting the same bits to 000b.

While the SDA output delay function is enabled (i.e. while the ICMR2.SDDL[2:0] bits are set to any value other than 000b), the ICMR2.DLCS bit selects the clock source for counting by the SDA output delay counter as the internal base clock (IICφ) for the RIIC module or as a clock signal derived by dividing the frequency of the internal base clock by two (IICφ/2). The counter counts the number of cycles set in the ICMR2.SDDL[2:0] bits. After counting of the set number of cycles of delay is completed, the RIIC module places the required output (start, restart, or stop condition, data, or an ACK or NACK signal) on the SDA line.

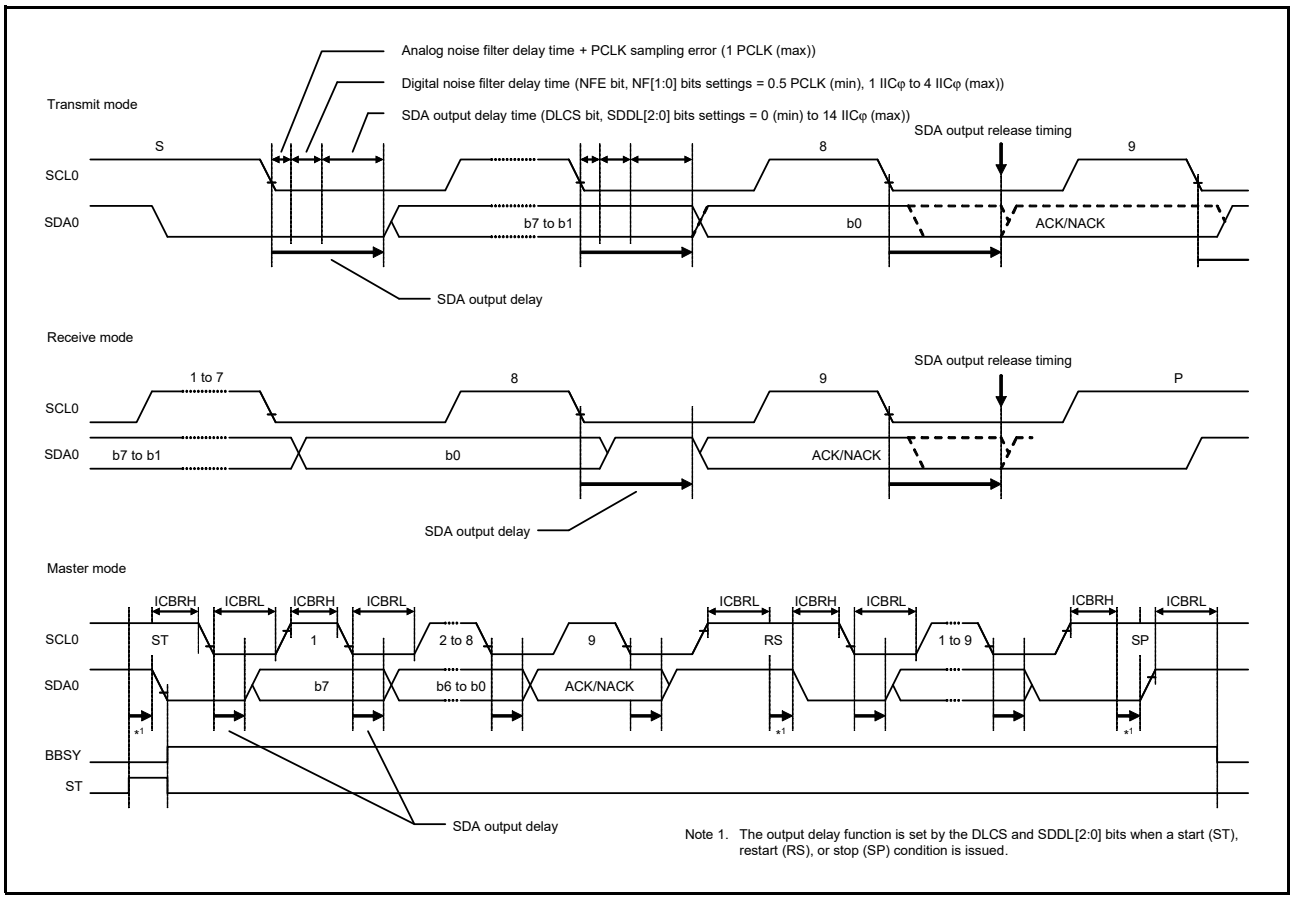


Figure 27.22 SDA Output Delay Function

27.6 Digital Noise Filter Circuit

The states of the SCL0 and SDA0 pins are conveyed to the internal circuitry through analog noise-filter and digital noise-filter circuits. Figure 27.23 is a block diagram of the digital noise-filter circuit.

The on-chip digital noise-filter circuit of the RIIC consists of four flip-flop circuit stages connected in series and a match-detection circuit.

The number of effective stages in the digital noise filter is selected by the ICMR3.NF[1:0] bits. The selected number of effective stages determines the noise-filtering capability as a period from one to four IICφ cycles.

The input signal to the SCL0 pin (or SDA0 pin) is sampled on falling edges of the IICφ signal. When the input signal level matches the output level of the number of effective flip-flop circuit stages as selected by the ICMR3.NF[1:0] bits, the signal level is conveyed to the subsequent stage. If the signal levels do not match, the previous value is retained.

If the ratio between the frequency of the internal operating clock (PCLK) and the transfer rate is small (e.g. data transfer at 400 kbps with PCLK = 4 MHz), the characteristics of the digital noise filter may lead to the elimination of needed signals as noise. In such cases, it is possible to disable the digital noise-filter circuit (by setting the ICFER.NFE bit to 0) and use only the analog noise filter circuit.

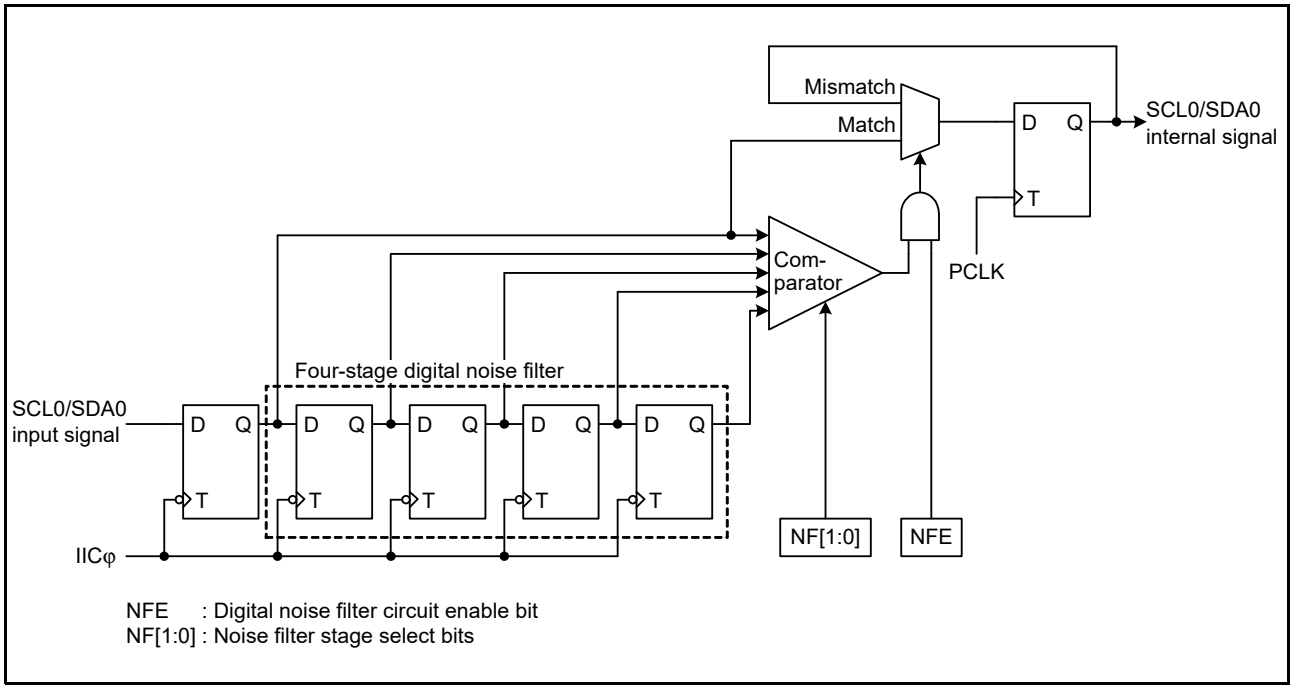


Figure 27.23 Block Diagram of Digital Noise Filter Circuit

27.7 Address Match Detection

The RIIC can set three unique slave addresses in addition to the general call address and host address, and also can set 7-bit or 10-bit slave addresses.

27.7.1 Slave-Address Match Detection

The RIIC can set three unique slave addresses, and has a slave address detection function for each unique slave address. When the ICSER.SARyE bit (y = 0 to 2) is set to 1, the slave addresses set in registers SARUy and SARLy (y = 0 to 2) can be detected.

When the RIIC detects a match of the set slave address, the corresponding ICSR1.AASy flag (y = 0 to 2) is set to 1 at the rising edge of the ninth SCL clock cycle, and the ICSR2.RDRF flag or the ICSR2.TDRE flag is set to 1 by the following R/W# bit. This causes a receive data full interrupt (RXI) or transmit data empty interrupt (TXI) to be generated. The AASy flag is used to identify which slave address has been specified.

Figure 27.24 to Figure 27.26 show the AASy flag set timing in three cases.

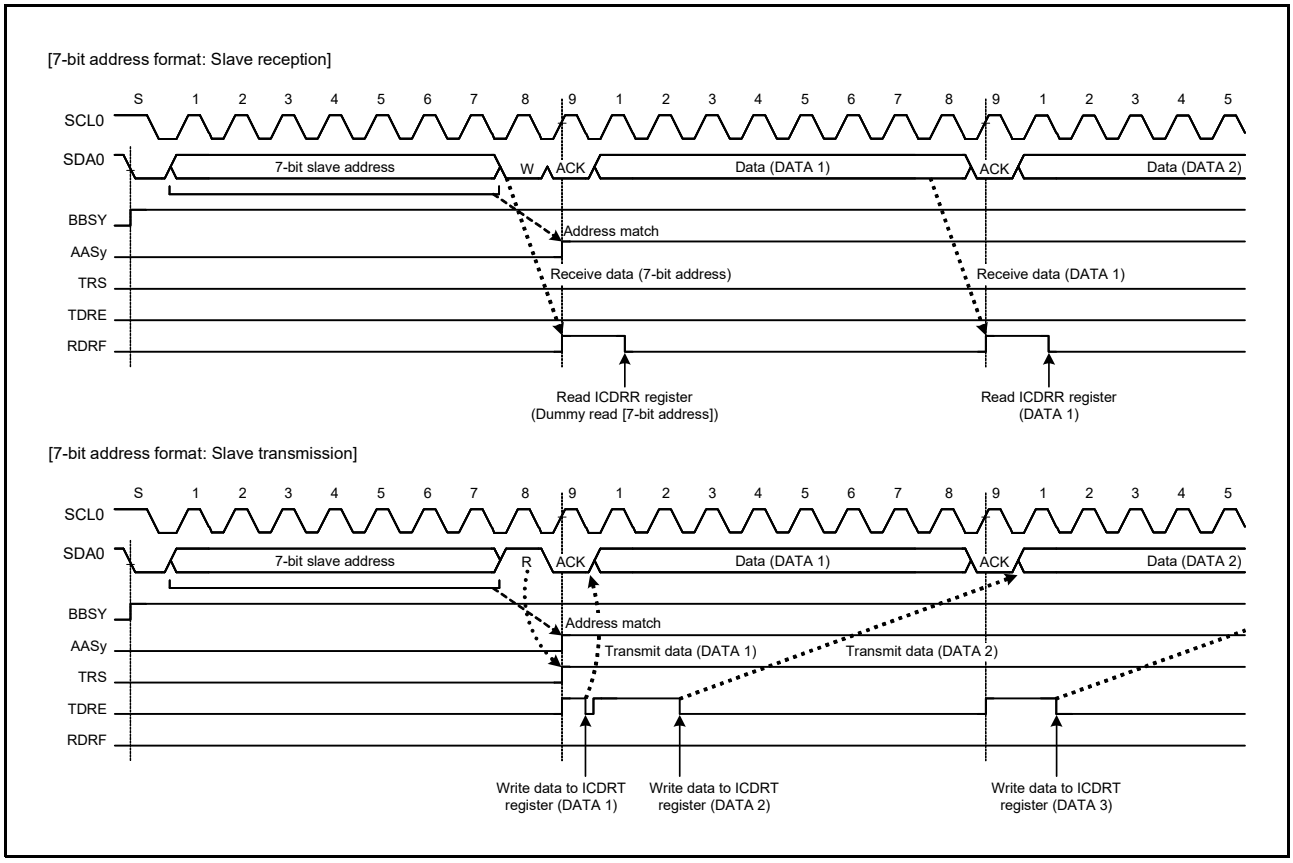


Figure 27.24 AASy Flag Set Timing with 7-Bit Address Format Selected

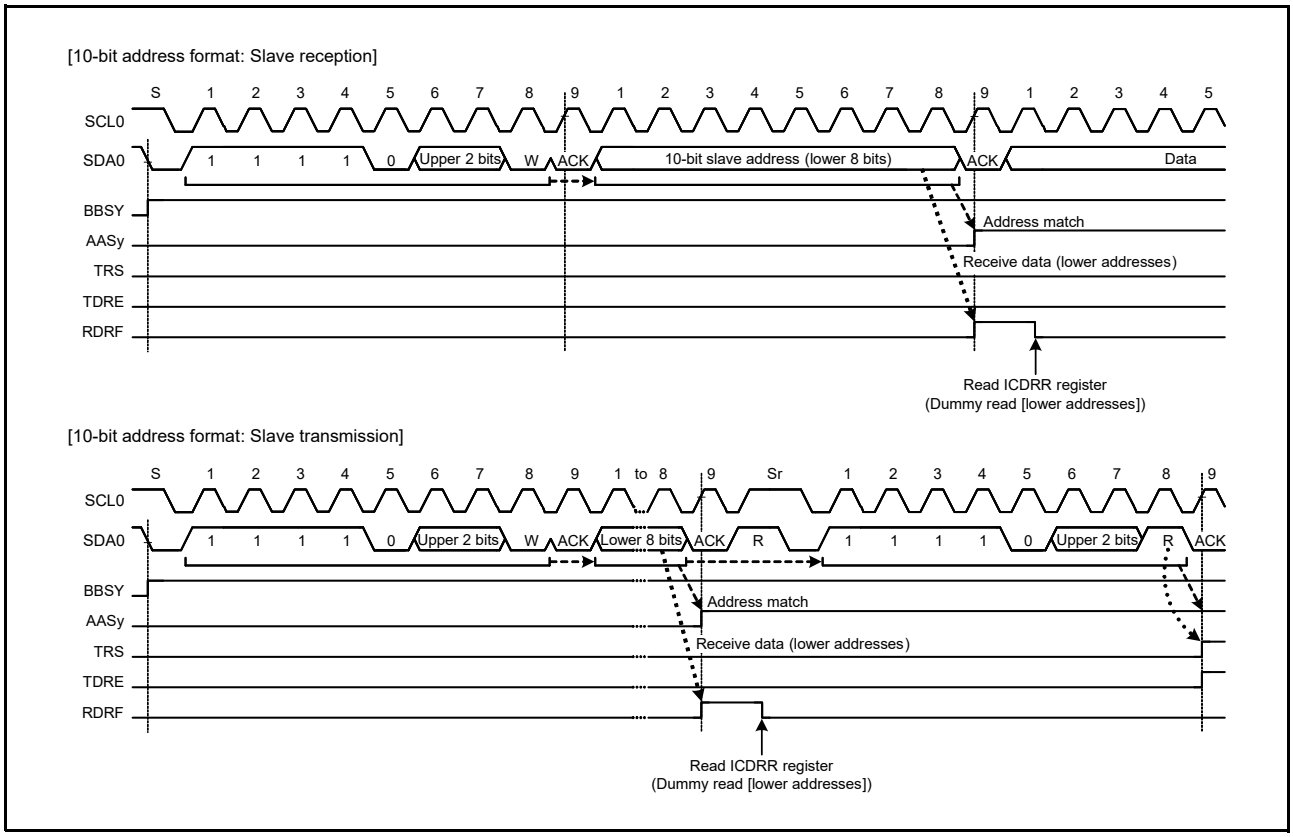


Figure 27.25 AASy Flag Set Timing with 10-Bit Address Format Selected

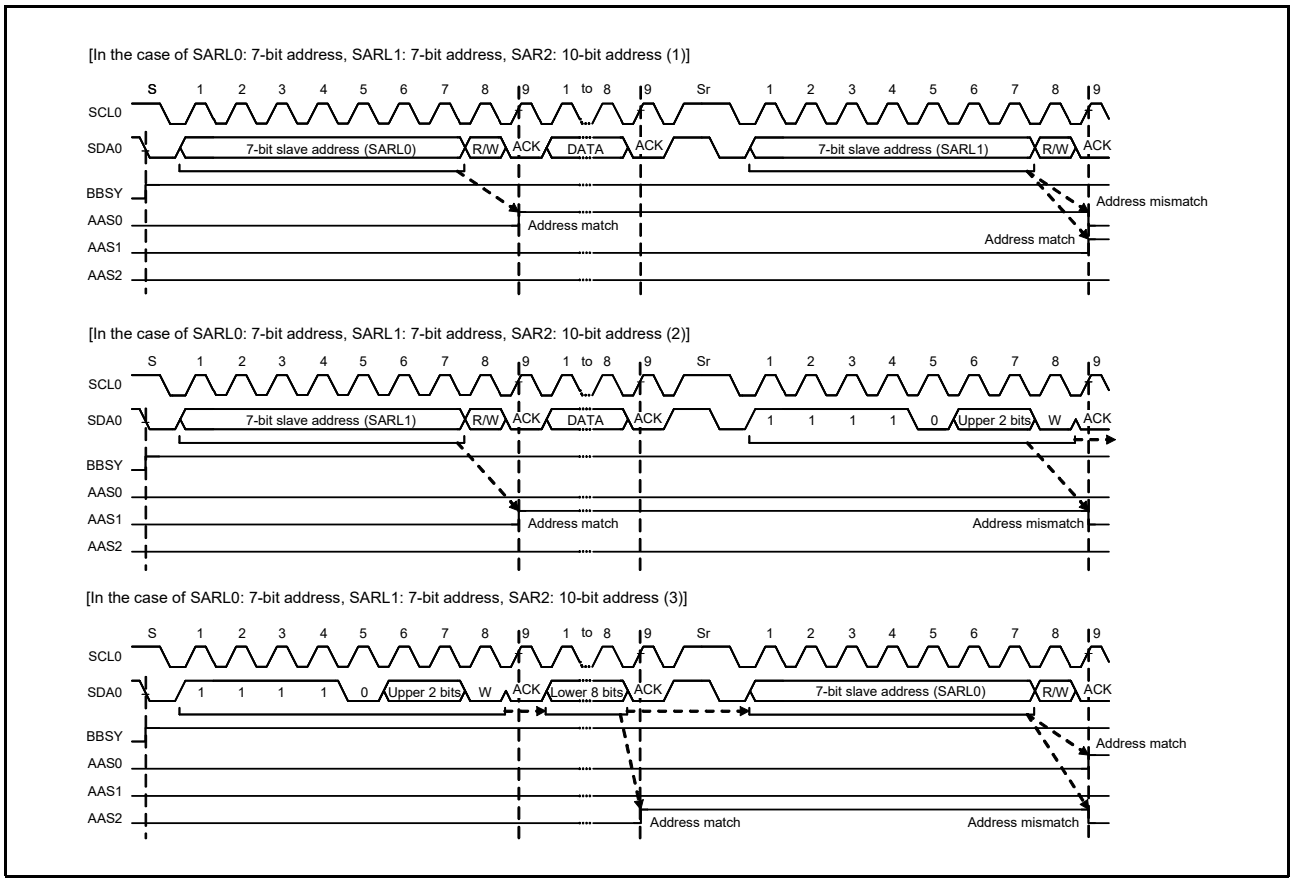


Figure 27.26 AASy Flag Set/Clear Timing with 7-Bit/10-Bit Address Formats Mixed

27.7.2 Detection of the General Call Address

The RIIC has a facility for detecting the general call address (0000 000b + 0 (write)). This is enabled by setting the ICSER.GCAE bit to 1.

If the address received after a start or restart condition is issued is 0000 000b + 1 (read) (start byte), the RIIC recognizes this as the address of a slave device with an “all-zero” address but not as the general call address.

When the RIIC detects the general call address, both the ICSR1.GCA flag and the ICSR2.RDRF flag are set to 1 on the rising edge of the ninth cycle of SCL clock. This leads to the generation of a receive data full interrupt (RXI). The value of the GCA flag can be confirmed to recognize that the general call address has been transmitted.

Operation after detection of the general call address is the same as normal slave receive operation.

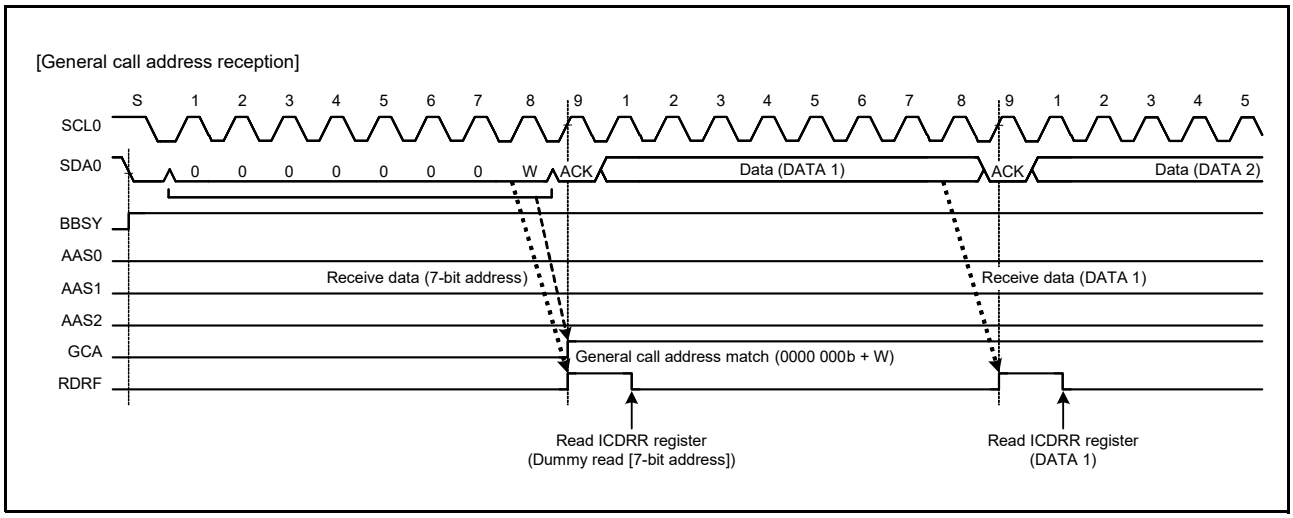


Figure 27.27 Timing of GCA Flag Setting during Reception of General Call Address

27.7.3 Device-ID Address Detection

The RIIC module has a facility for detecting device-ID addresses conformant with the I2C-bus specification (Rev. 03). When the RIIC receives 1111 100b as the first byte after a start condition or restart condition was issued with the ICSER.DIDE bit set to 1, the RIIC recognizes the address as a device ID, sets the ICSR1.DID flag to 1 on the rising edge of the eighth SCL clock cycle when the following R/W# bit is 0, and then compares the second and subsequent bytes with its own slave address. If the address matches the value in the slave address register, the RIIC sets the corresponding ICSR1.AASy flag (y = 0 to 2) to 1.

After that, when the first byte received after a start or restart condition is issued matches the device ID address (1111 100b) again and the following R/W# bit is 1, the RIIC does not compare the second and subsequent bytes and sets the ICSR2.TDRE flag to 1.

In the device-ID address detection function, the RIIC sets the DID flag to 0 if a match with the RIIC's own slave address is not obtained or a match with the device ID address is not obtained after a match with the RIIC's own slave address and the detection of a restart condition. If the first byte after detection of a start or restart condition matches the device ID address (1111 100b) and the R/W# bit is 0, the RIIC sets the DID flag to 1 and compares the second and subsequent bytes with the RIIC's slave address. If the R/W# bit is 1, the DID flag holds the previous value and the RIIC does not compare the second and subsequent bytes. Therefore, the reception of a device-ID address can be checked by reading the DID flag after confirming that TDRE flag is 1.

Furthermore, prepare the device-ID fields (3 bytes: 12 bits indicating the manufacturer + 9 bits identifying the part + 3 bits indicating the revision) that must be sent to the host after reception of a continuous device-ID field as normal data for transmission. For details of the information that must be included in device-ID fields, contact NXP Semiconductors.

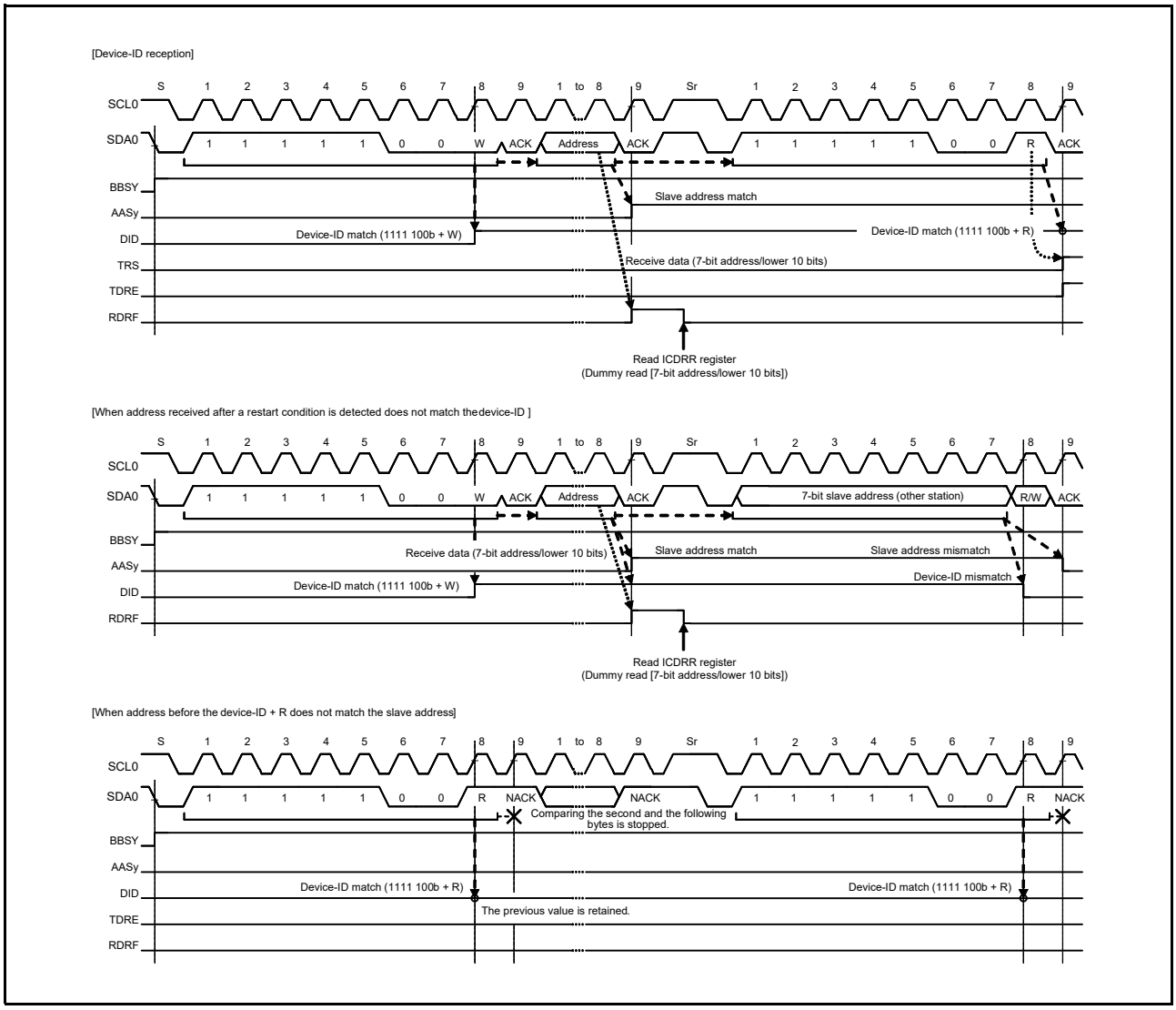


Figure 27.28 AASy/DID Flag Set/Clear Timing during Reception of Device-ID

27.7.4 Host Address Detection

The RIIC has a function to detect the host address while the SMBus is operating. When the ICSER.HOAE bit is set to 1 while the ICMR3.SMBS bit is 1, the RIIC can detect the host address (0001 000b) in slave receive mode (bits MST and TRS in the ICCR2 register are 00b).

When the RIIC detects the host address, the ICSR1.HOA flag is set to 1 at the rising edge of the ninth SCL clock cycle, and at the same time, the ICSR2.RDRF flag is set to 1 when the R/W# bit is 0 (Wr bit). This causes a receive data full interrupt (RXI) to be generated. The HOA flag is used to recognize that the host address was sent from the smart battery or other devices.

If the bit following the host address (0001 000b) is an Rd bit (R/W# bit is 1), the RIIC can also detect the host address. After the host address is detected, the RIIC operates in the same manner as normal slave operation.

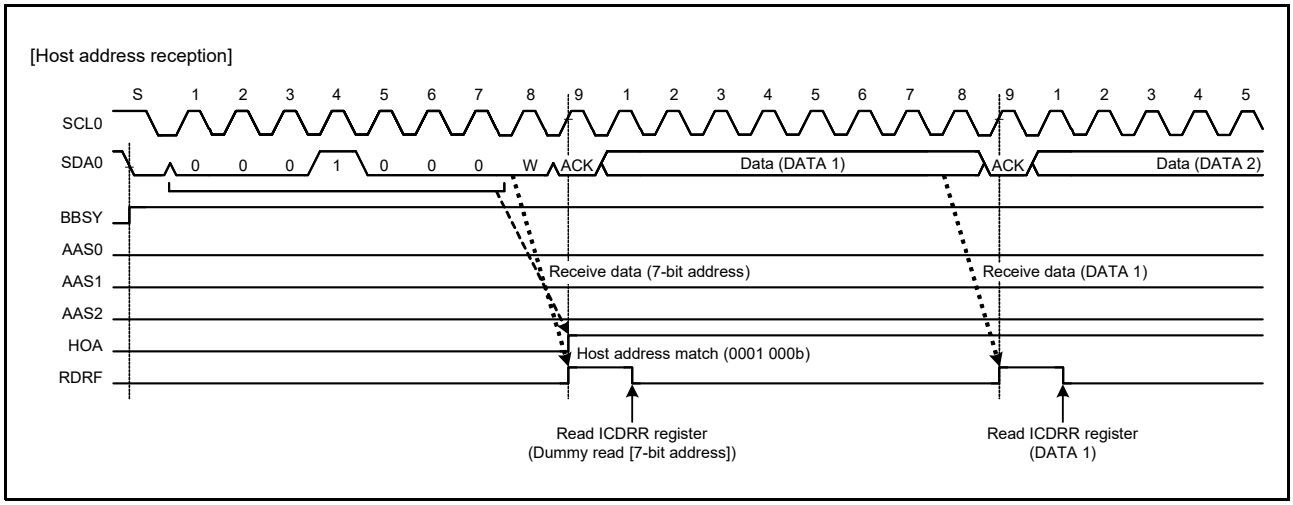


Figure 27.29 HOA Flag Set Timing during Reception of Host Address

27.8 Automatic Low-Hold Function for SCL

27.8.1 Function to Prevent Wrong Transmission of Transmit Data

If the shift register (ICDRS) is empty when data have not been written to the I2C-bus transmit data register (ICDRT) with the RIIC in transmission mode (ICCR2.TRS bit is 1), the SCL0 line is automatically held at the low level over the intervals shown below. This low-hold period is extended until data for transmission have been written, which prevents the unintended transmission of erroneous data.

Master transmit mode

- Low-level interval after a start condition or restart condition is issued
- Low-level interval between the ninth clock cycle of one transfer and the first clock cycle of the next

Slave transmit mode

- Low-level interval between the ninth clock cycle of one transfer and the first clock cycle of the next

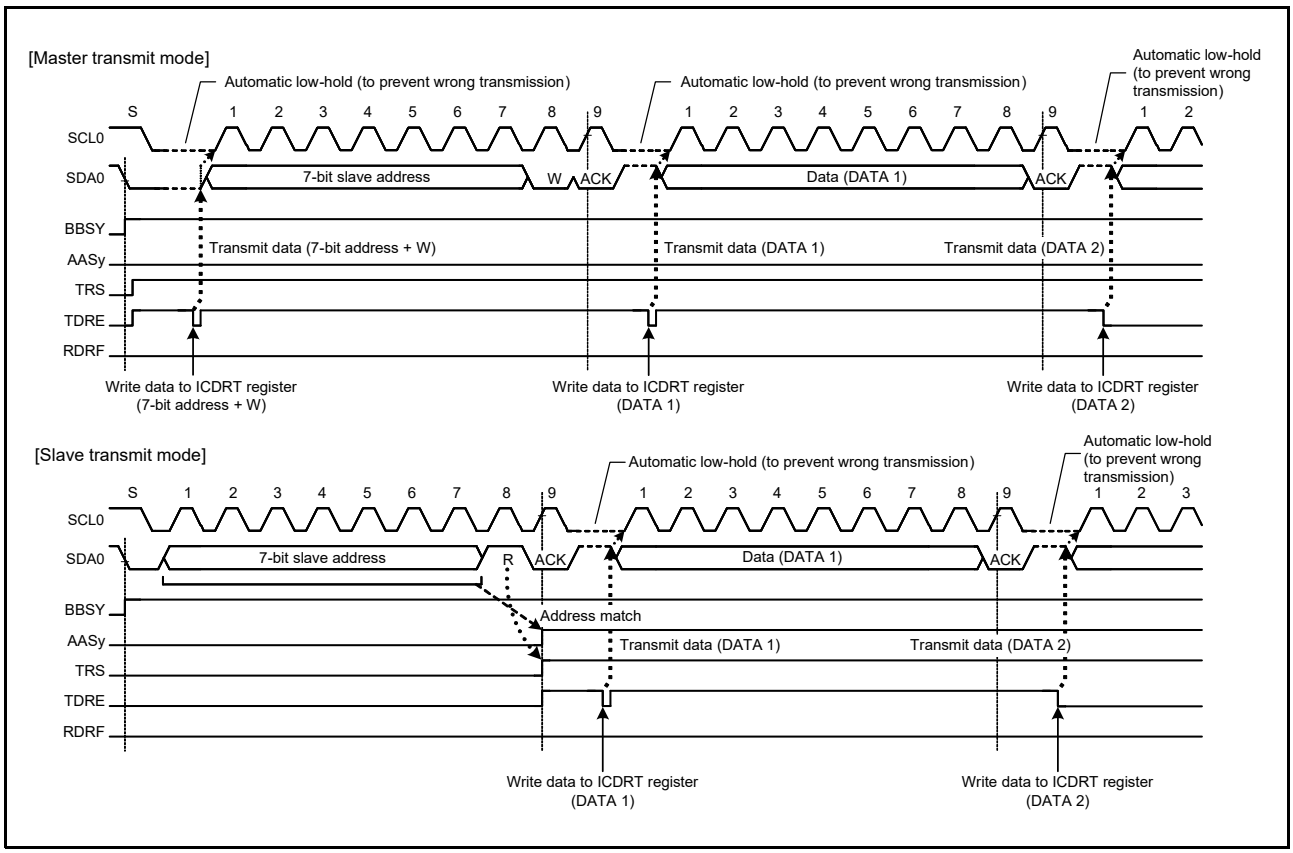


Figure 27.30 Automatic Low-Hold Operation in Transmit Mode

27.8.2 NACK Reception Transfer Suspension Function

The RIIC has a function to suspend transfer operation when NACK is received in transmit mode (ICCR2.TRS bit is 1). This function is enabled when the ICFER.NACKE bit is set to 1 (transfer suspension enabled). If the next transmit data has already been written (ICSR2.TDRE flag is 0) when NACK is received, next data transmission at the falling edge of the ninth SCL clock cycle is automatically suspended. This prevents the SDA0 line output level from being held low when the MSB of the next transmit data is 0.

If the transfer operation is suspended by this function (ICSR2.NACKF flag is 1), transmit operation and receive operation are discontinued. To restore transmit/receive operation, be sure to set the NACKF flag to 0. In master transmit mode, after setting the NACKF flag to 0, issue a restart condition, or issue a stop condition and then issue a start condition again.

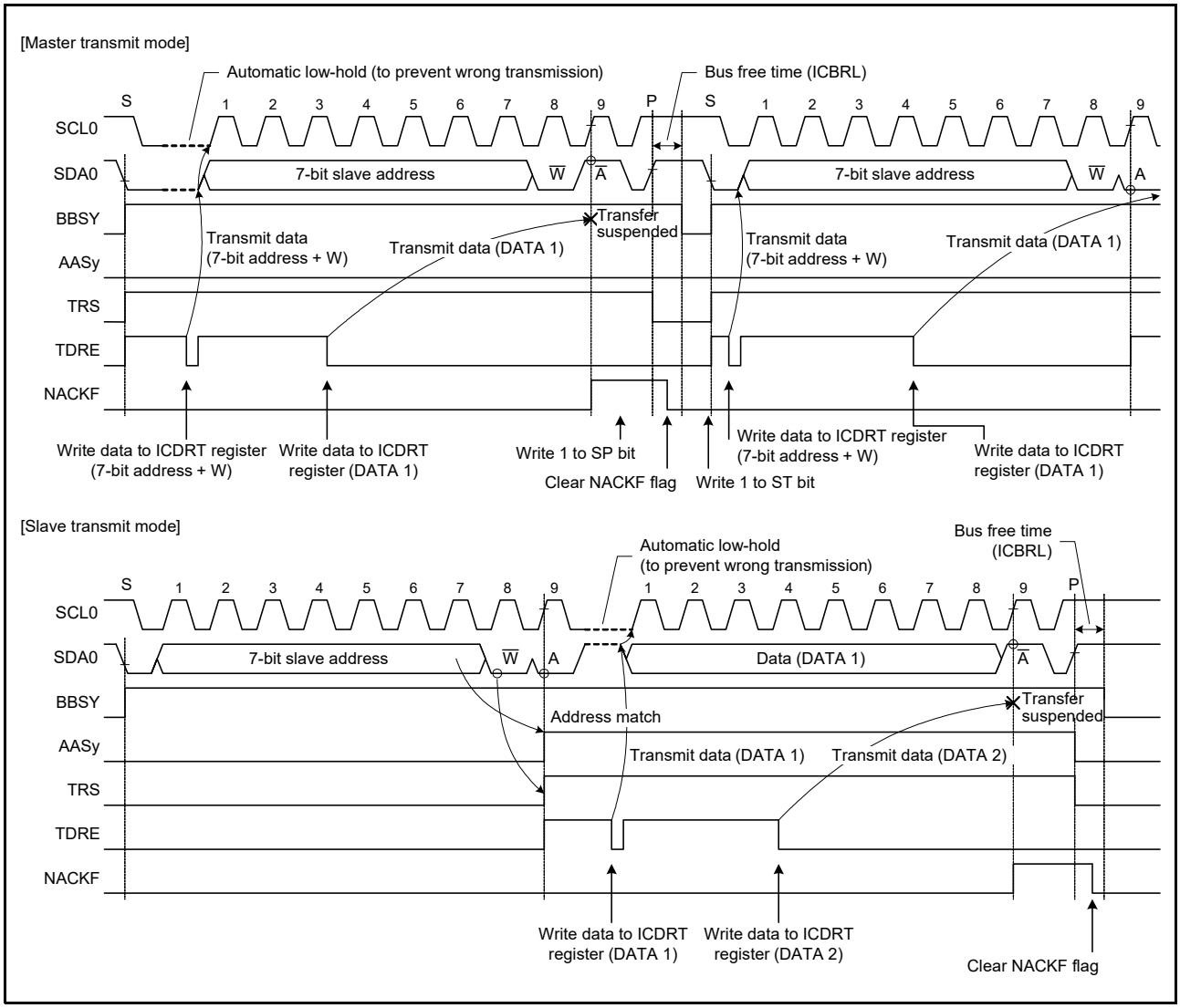


Figure 27.31 Suspension of Data Transfer When NACK is Received (NACKE = 1)

27.8.3 Function to Prevent Failure to Receive Data

If response processing is delayed when receive data (ICDRR) read is delayed for a period of one transfer byte or more with receive data full (ICSR2.RDRF flag is 1) in receive mode (ICCR2.TRS bit is 0), the RIIC holds the SCL0 line low automatically immediately before the next data is received to prevent failure to receive data.
This function to prevent failure to receive data using the automatic low-hold function is also enabled even if the read processing of the final receive data is delayed and, in the meantime, the RIIC's own slave address is designated after a stop condition is issued. This function does not disturb other communication because the RIIC does not hold the SCL0 line low when a mismatch with its own slave address occurs after a stop condition is issued.
Sections in which the SCL0 line is held low can be selected with a combination of the WAIT and RDRFS bits in the ICMR3 register.

(1) 1-Byte Receive Operation and Automatic Low-Hold Function Using the WAIT Bit

When the ICMR3.WAIT bit is set to 1, the RIIC performs 1-byte receive operation using the WAIT bit function. Furthermore, when the ICMR3.RDRFS bit is 0, the RIIC automatically sends the ICMR3.ACKBT bit value for the acknowledge bit in the period from the falling edge of the eighth SCL clock cycle to the falling edge of the ninth SCL clock cycle, and automatically holds the SCL0 line low at the falling edge of the ninth SCL clock cycle using the WAIT bit function. This low-hold is released by reading data from the ICDRR register, which enables bytewise receive operation.
The WAIT bit function is enabled for receive bytes after a match with the RIIC's own slave address (including the general call address and host address) is obtained in master receive mode or slave receive mode.

(2) 1-Byte Receive Operation (ACK/NACK Transmission Control) and Automatic Low-Hold Function Using the RDRFS Bit

When the ICMR3.RDRFS bit is set to 1, the RIIC performs 1-byte receive operation using the RDRFS bit function. When the RDRFS bit is set to 1, the ICSR2.RDRF flag (receive data full) is set to 1 at the rising edge of the eighth SCL clock cycle, and the SCL0 line is automatically held low at the falling edge of the eighth SCL clock cycle. This low-hold is released by writing a value to the ICMR3.ACKBT bit, but cannot be released by reading data from the ICDRR register, which enables receive operation by the ACK/NACK transmission control according to the data received in byte units.
The RDRFS bit function is enabled for receive bytes after a match with the RIIC's own slave address (including the general call address and host address) is obtained in master receive mode or slave receive mode.

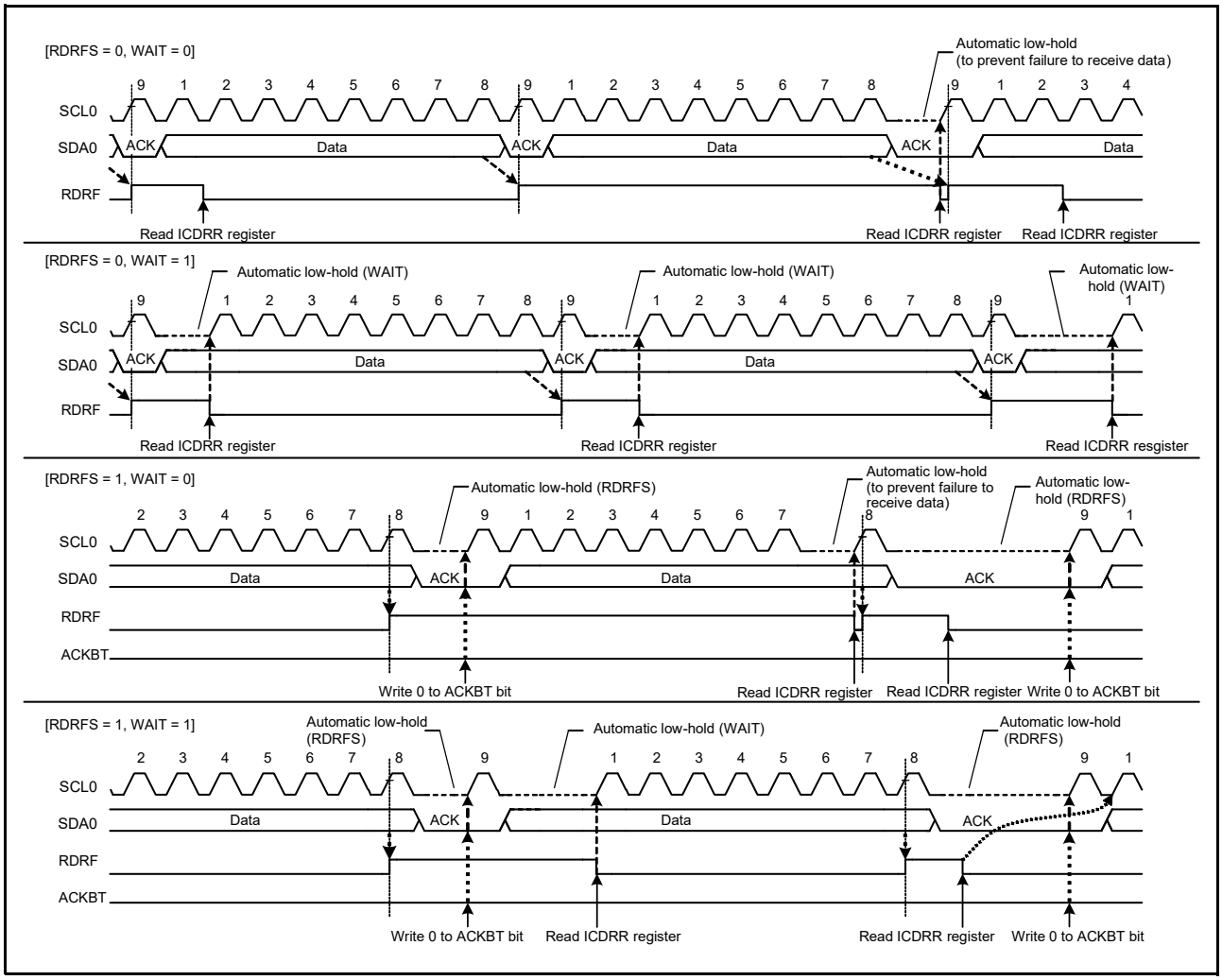


Figure 27.32 Automatic Low-Hold Operation in Receive Mode (Using RDRFS and WAIT Bits)

27.9 Arbitration-Lost Detection Functions

In addition to the normal arbitration-lost detection function defined by the I2C-bus specification, the RIIC has functions to prevent double-issue of a start condition, to detect arbitration-lost during transmission of NACK, and to detect arbitration-lost in slave transmit mode.

27.9.1 Master Arbitration-Lost Detection (MALE Bit)

The RIIC drives the SDA0 line low to issue a start condition. However, if the SDA0 line has already been driven low by another master device issuing a start condition, the RIIC causes arbitration to be lost, so priority is given to transfer by the other master device. Similarly, if the ICCR2.ST bit is set to 1 while the ICCR2.BBSY flag is 1 (bus busy state), arbitration is lost, so priority is given to transfer by the other master device. No start condition is issued in this case.
When a start condition is issued successfully, if the data for transmission including the address bits (i.e. the internal SDA output level) and the level on the SDA0 line do not match (the high output as the internal SDA output; i.e. the SDA0 pin is in the high-impedance state) and the low level is detected on the SDA0 line, the RIIC loses in arbitration.
After a loss in arbitration of mastership, the RIIC immediately enters slave receive mode. If a slave address (including the general call address) matches its own address at this time, the RIIC continues in slave operation.
A loss in arbitration of mastership is detected when the following conditions are met while the ICFER.MALE bit is 1 (master arbitration-lost detection enabled).

Conditions for master arbitration-lost

- Non-matching of the internal level for output on SDA and the level on the SDA0 line after a start condition was issued by setting the ICCR2.ST bit to 1 while the ICCR2.BBSY flag was set to 0 (erroneous issuing of a start condition)
- Setting of the ICCR2.ST bit to 1 (start condition double-issue error) while the BBSY flag is set to 1
- When the transmit data excluding acknowledge (internal SDA output level) does not match the level on the SDA0 line in master transmit mode (bits MST and TRS in the ICCR2 register = 11b)

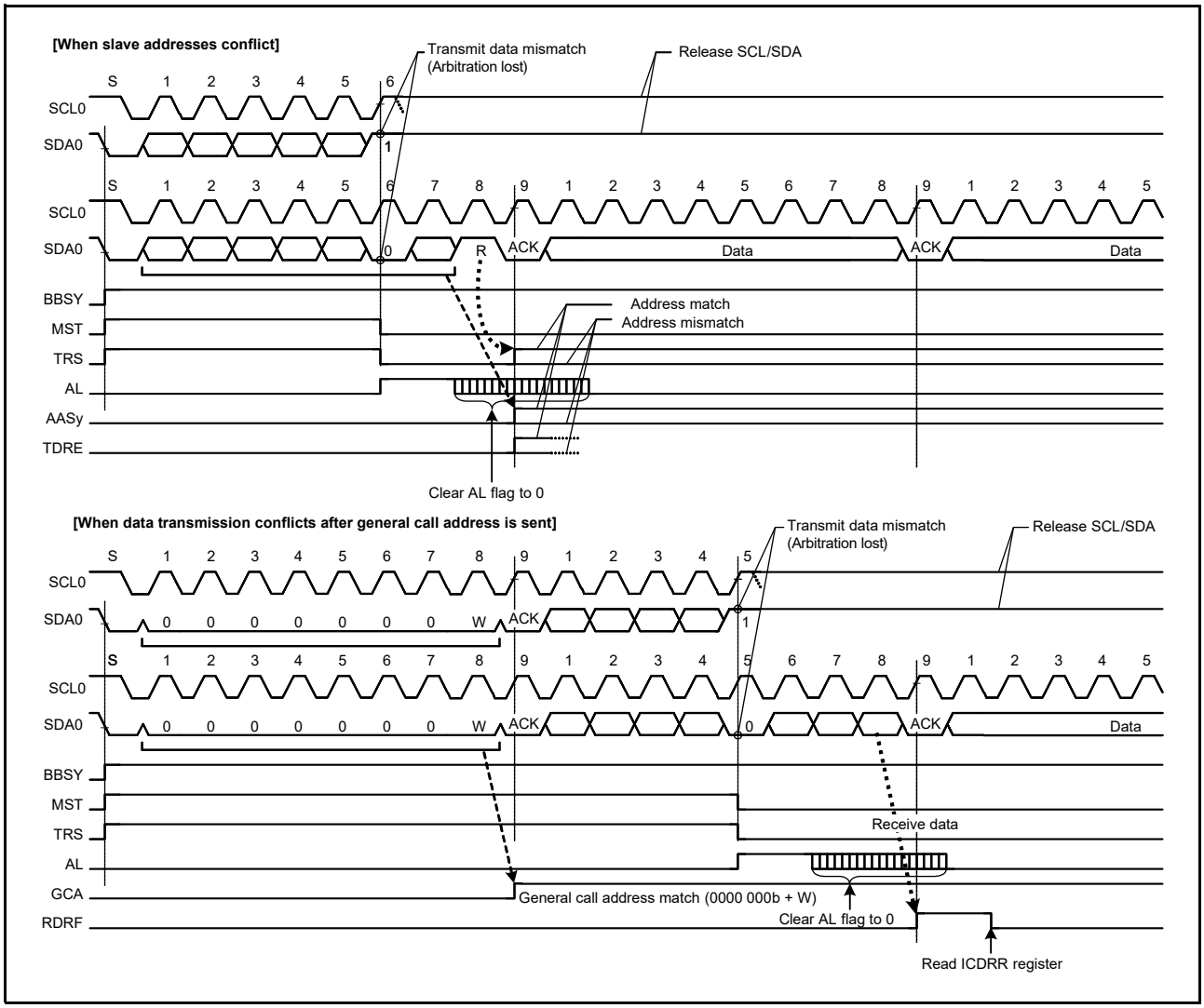


Figure 27.33 Examples of Master Arbitration-Lost Detection (MALE = 1)

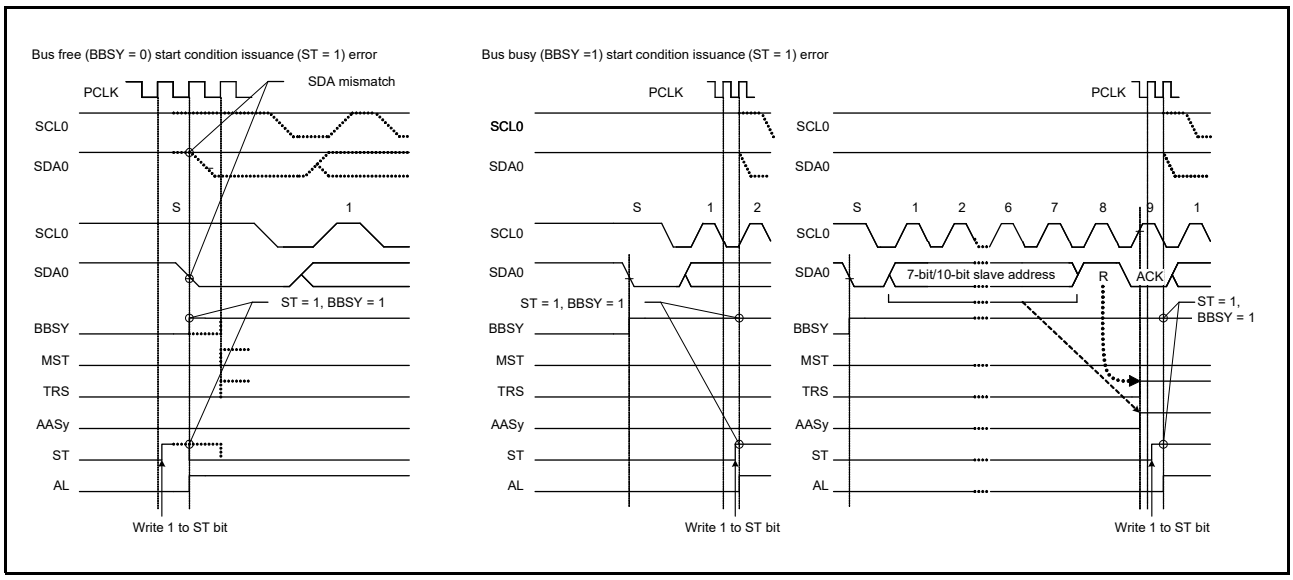


Figure 27.34 Arbitration-Lost When a Start Condition is Issued (MALE = 1)

27.9.2 Function to Detect Loss of Arbitration during NACK Transmission (NALE Bit)

The RIIC has a function to cause arbitration to be lost if the internal SDA output level does not match the level on the SDA0 line (the high output as the internal SDA output; i.e. the SDA0 pin is in the high-impedance state) and the low level is detected on the SDA0 line during transmission of NACK in receive mode. Arbitration is lost due to a conflict of NACK transmission and ACK transmission when two or more master devices receive data from the same slave device simultaneously in a multi-master system. Such conflict occurs when multiple master devices send/receive the same information through a single slave device. Figure 27.35 shows an example of arbitration-lost detection during transmission of NACK.

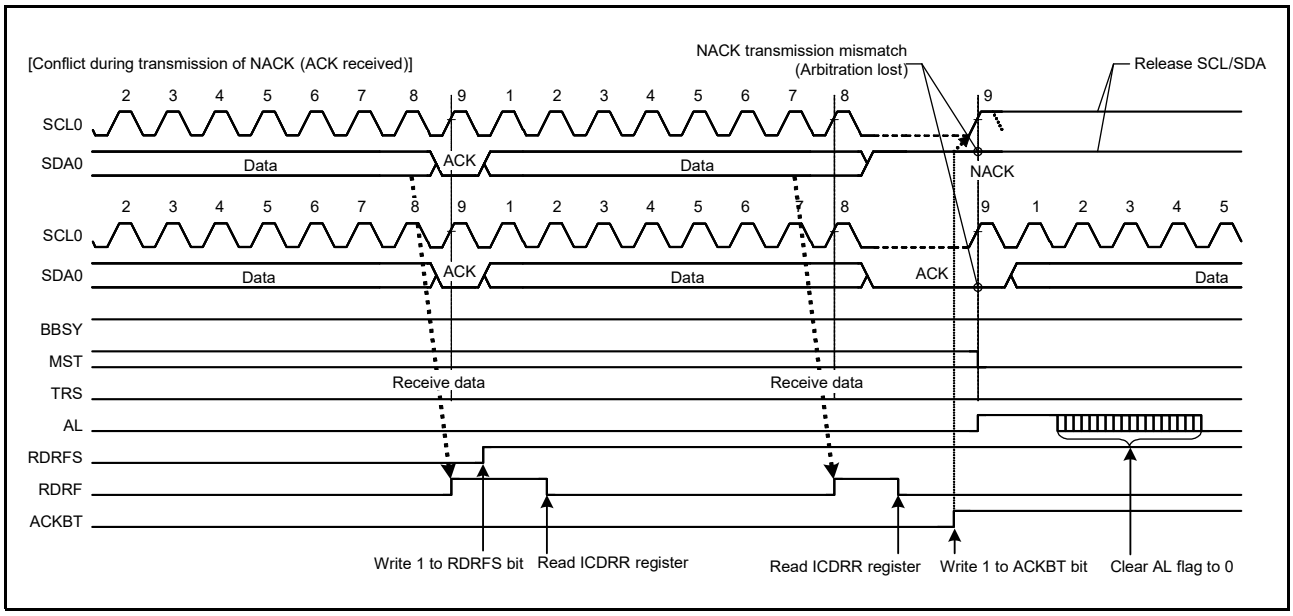


Figure 27.35 Example of Arbitration-Lost Detection during Transmission of NACK (NALE = 1)

The following explains arbitration-lost detection using an example where two master devices (master A and master B) and a single slave device are connected through the bus. In this example, master A receives 2 bytes of data from the slave device, and master B receives 4 bytes of data from the slave device.

If master A and master B access the slave device simultaneously, because the slave address is identical, arbitration is not lost in both master A and master B during access to the slave device. Therefore, both master A and master B recognize that they have obtained the bus mastership and operate as such. Here, master A sends NACK when it has received 2 final bytes of data from the slave device. Meanwhile, master B sends ACK because it has not received necessary 4 bytes of data. At this time, the NACK transmission from master A and the ACK transmission from master B conflict. In general, if a conflict like this occurs, master A cannot detect ACK transmitted by master B and issues a stop condition. Therefore, the issuance of the stop condition conflicts with the SCL clock output of master B, which disturbs communication.

When the RIIC receives ACK during transmission of NACK, it detects a defeat in conflict with other master devices and causes arbitration to be lost.

If arbitration is lost during transmission of NACK, the RIIC immediately cancels the slave match condition and enters slave receive mode. This prevents a stop condition from being issued, preventing a communication failure on the bus.

Similarly, in the ARP command processing of SMBus, the function to detect loss of arbitration during transmission of NACK is also available for eliminating the extra clock cycle processing (such as FFh transmission processing) necessary if the UDID (Unique Device Identifier) of assign address does not match in the Get UDID (general) processing after the Assign address command.

The RIIC detects arbitration-lost during transmission of NACK when the following condition is met with the ICFER.NALE bit set to 1 (arbitration-lost detection during NACK transmission enabled).

Condition for arbitration-lost during NACK transmission

- When the internal SDA output level does not match the SDA0 line (ACK is received) during transmission of NACK (ICMR3.ACKBT bit = 1)

27.9.3 Slave Arbitration-Lost Detection (SALE Bit)

The RIIC has a function to cause arbitration to be lost if the data for transmission (i.e. the internal SDA output level) and the level on the SDA0 line do not match (the high output as the internal SDA output; i.e. the SDA0 pin is in the high-impedance state and the low level is detected on the SDA0 line in slave transmit mode). This arbitration-lost detection function is mainly used when transmitting a UDID (Unique Device Identifier) over an SMBus.
When it loses slave arbitration, the RIIC is immediately released from the slave-matched state and enters slave receive mode. This function can detect conflicts of data during transmission of UDIDs over an SMBus and eliminate subsequent redundant processing (processing for the transmission of FFh).
The RIIC detects slave arbitration-lost when the following condition is met with the ICFER.SALE bit set to 1 (slave arbitration-lost detection enabled).

Condition for slave arbitration-lost

- When transmit data excluding acknowledge (internal SDA output level) does not match the SDA0 line in slave transmit mode (bits MST and TRS in the ICCR2 register are 01b)

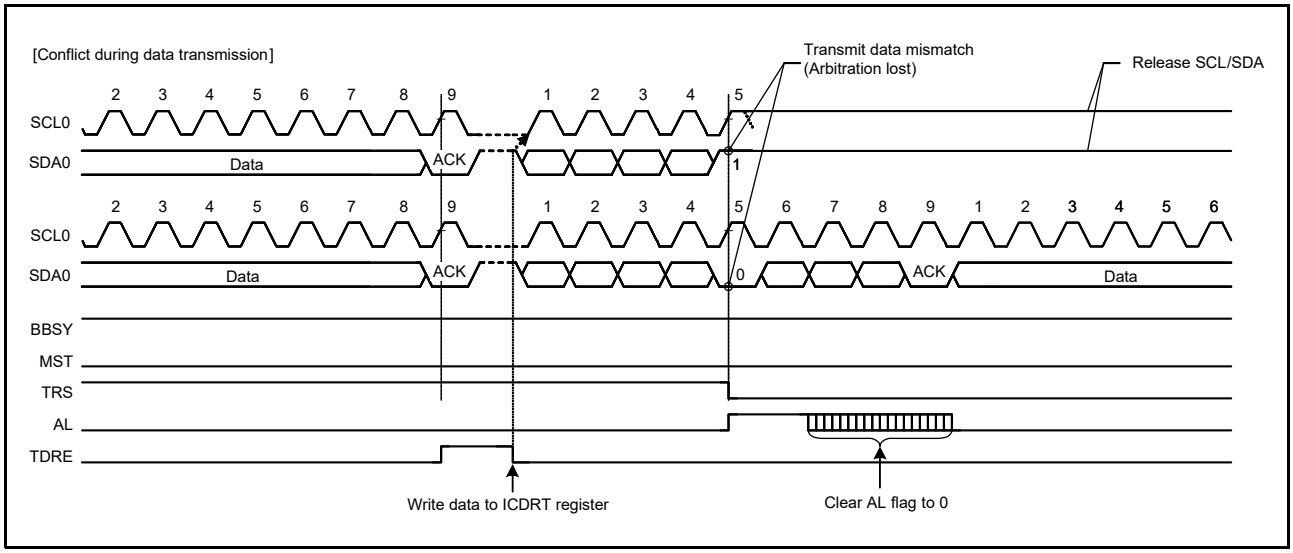


Figure 27.36 Example of Slave Arbitration-Lost Detection (SALE = 1)

27.10 Start Condition/Restart Condition/Stop Condition Issuing Function

27.10.1 Issuing a Start Condition

The RIIC issues a start condition when the ICCR2.ST bit is set to 1.
When the ST bit is set to 1, a start condition issuance request is made and the RIIC issues a start condition when the ICCR2.BBSY flag is 0 (bus free state). When a start condition is issued normally, the RIIC automatically shifts to the master transmit mode.
A start condition is issued in the following sequence.

Start condition issuance

(1) Drive the SDA0 line low (high level to low level).
(2) Ensure the time set in the ICBRH register and the start condition hold time.
(3) Drive the SCL0 line low (high level to low level).
(4) Detect low level of the SCL0 line and ensure the low-level period of SCL0 line set in the ICBRL register.

27.10.2 Issuing a Restart Condition

The RIIC issues a restart condition when the ICCR2.RS bit is set to 1.
When the RS bit is set to 1, a restart condition issuance request is made and the RIIC issues a restart condition when the ICCR2.BBSY flag is 1 (bus busy state) and the ICCR2.MST bit is 1 (master mode).
A restart condition is issued in the following sequence.

Restart condition issuance

(1) Release the SDA0 line.
(2) Ensure the low-level period of SCL0 line set in the ICBRL register.
(3) Release the SCL0 line (low level to high level).
(4) Detect a high level of the SCL0 line and ensure the time set in the ICBRL register and the restart condition setup time.
(5) Drive the SDA0 line low (high level to low level).
(6) Ensure the time set in the ICBRH register and the restart condition hold time.
(7) Drive the SCL0 line low (high level to low level).
(8) Detect a low level of the SCL0 line and ensure the low-level period of SCL0 line set in the ICBRL register.

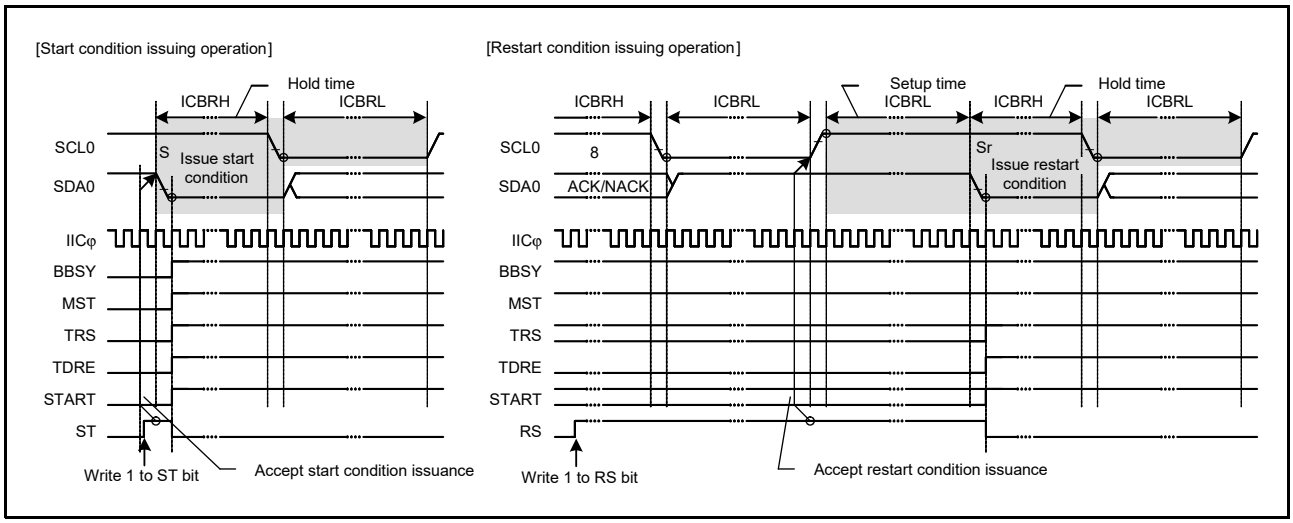


Figure 27.37 Start Condition/Restart Condition Issue Timing (ST and RS Bits)

27.10.3 Issuing a Stop Condition

The RIIC issues a stop condition when the ICCR2.SP bit is set to 1.
When the SP bit is set to 1, a stop condition issuance request is made and the RIIC issues a stop condition when the ICCR2.BBSY flag is 1 (bus busy state) and the ICCR2.MST bit is 1 (master mode).
A stop condition is issued in the following sequence.

Stop condition issuance

(1) Drive the SDA0 line low (high level to low level).
(2) Ensure the low-level period of SCL0 line set in the ICBRL register.
(3) Release the SCL0 line (low level to high level).
(4) Detect a high level of the SCL0 line and ensure the time set in the ICBRH register and the stop condition setup time.
(5) Release the SDA0 line (low level to high level).
(6) Ensure the time set in the ICBRL register and the bus free time.
(7) Set the BBSY flag to 0 (to release the bus mastership).

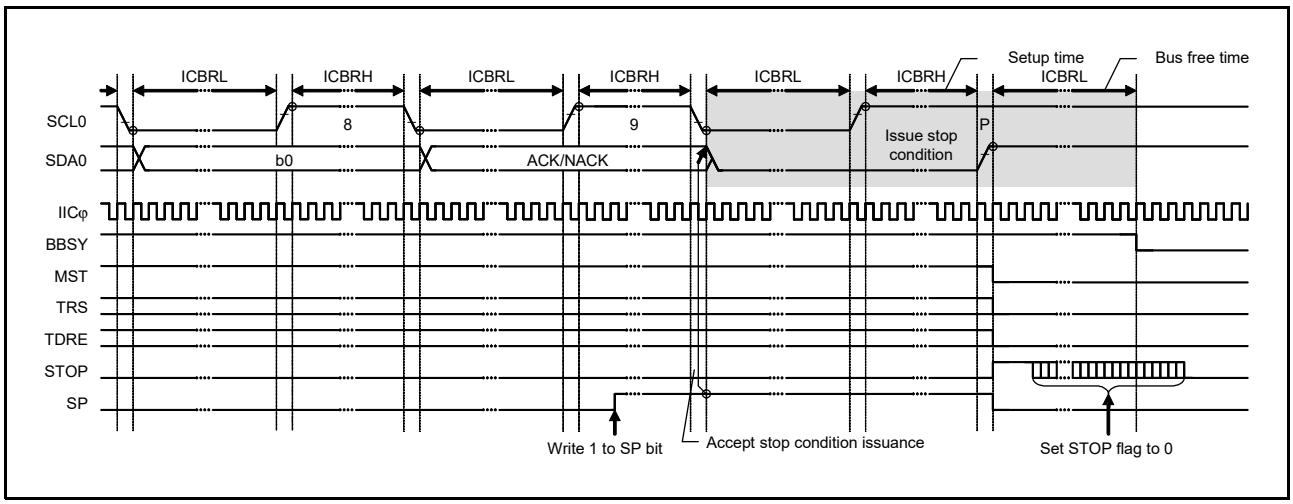


Figure 27.38 Stop Condition Issue Timing (SP Bit)

27.11 Bus Hanging

If the clock signals from the master and slave devices go out of synchronization due to noise or other factors, the I2C-bus might hang with a fixed level on the SCL0 line and/or SDA0 line.
As measures against the bus hanging, the RIIC has a timeout function to detect hanging by monitoring the SCL0 line, a function for the output of an extra SCL clock cycle to release the bus from a hung state due to clock signals being out of synchronization, the RIIC reset function, and internal reset function.
By checking bits SCLO, SDAO, SCLI, and SDAI in the ICCR1 register, it is possible to see whether the RIIC or its partner in communications is placing the low level on the SCL0 or SDA0 lines.

27.11.1 Timeout Function

The RIIC includes a timeout function for detecting when the SCL0 line has been stuck longer than the predetermined time. The RIIC can detect an abnormal bus state by monitoring that the SCL0 line is stuck low or high for a predetermined time.
The timeout function monitors the SCL0 line state and counts the low-level period or high-level period using the internal counter. The timeout function resets the internal counter each time the SCL0 line changes (rising or falling), but continues to count unless the SCL0 line changes. If the internal counter overflows due to no SCL0 line change, the RIIC can detect the timeout and report the bus hung state.
This timeout function is enabled when the ICFER.TMOE bit is 1. It detects a hung state that the SCL0 line is stuck low or high during the following conditions:

- The bus is busy (ICCR2.BBSY flag is 1) in master mode (ICCR2.MST bit is 1).
- The RIIC's own slave address is detected (ICSR1 register is not 00h) and the bus is busy (ICCR2.BBSY flag is 1) in slave mode (ICCR2.MST bit is 0).
- The bus is free (ICCR2.BBSY flag is 0) while generation of a start condition is requested (ICCR2.ST bit is 1).

The internal counter of the timeout function works using the internal reference clock (IICφ) set by the ICMR1.CKS[2:0] bits as a count source. It functions as a 16-bit counter when long mode is selected (ICMR2.TMOS bit is 0) or a 14-bit counter when short mode is selected (TMOS bit is 1).
The SCL0 line level (low/high or both levels) during which this counter is activated can be selected by the setting of bits TMOH and TMOL in the ICMR2 register. If both bits TMOL and TMOH are set to 0, the internal counter does not work.

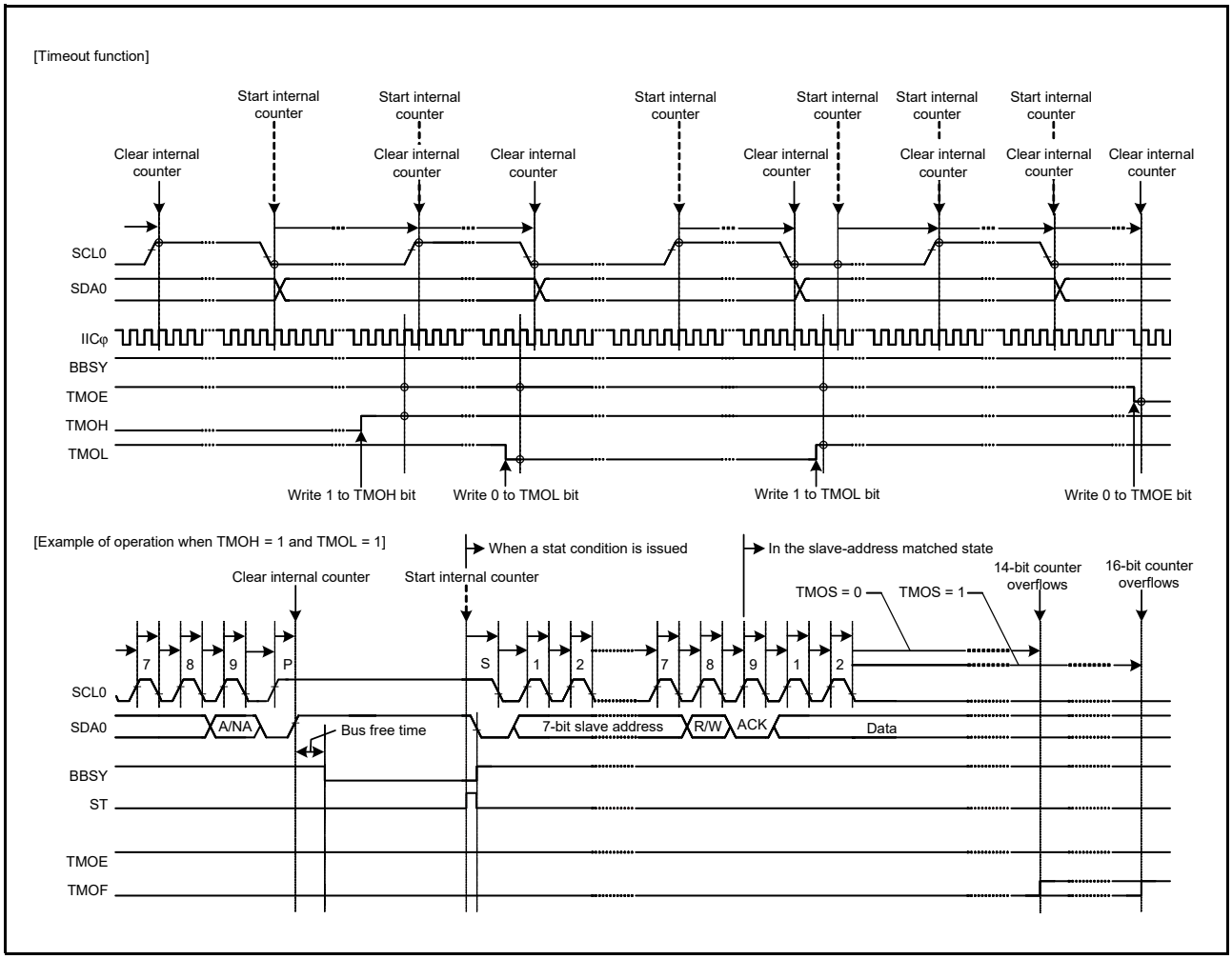


Figure 27.39 Timeout Function

27.11.2 Extra SCL Clock Cycle Output Function

In master mode, the RIIC module has a facility for the output of extra SCL clock cycles to release the SDA0 line of the slave device from being held at the low level due to the master being out of synchronization with the slave device.
This function is mainly used in master mode to release the SDA0 line of the slave device from the state of being fixed to the low level by including extra cycles of SCL output from the RIIC with single cycles of the SCL clock as the unit if the RIIC cannot issue a stop condition because the slave device is holding the SDA0 line at the low level. Do not use this facility in normal situations. Using it when communications are proceeding correctly will lead to malfunctions.
When the ICCR1.CLO bit is set to 1 in master mode, a single cycle of the SCL clock at the frequency corresponding to the transfer rate settings (settings of the ICMR1.CKS[2:0] bits, and of registers ICBRH and ICBRL) is output as an extra clock cycle. After output of this single cycle of the SCL clock, the CLO bit is automatically set to 0. Therefore, further extra clock cycles can be output consecutively by writing 1 to the CLO bit after confirming the CLO bit to be 0.
When the RIIC module is in master mode and the slave device is holding the SDA0 line at the low level because synchronization with the slave device has been lost due to the effects of noise, etc., the output of a stop condition is not possible. The facility for output of an extra cycle of the SCL clock can be used to output extra cycles of SCL one by one to make the slave device release the SDA0 line from being held at the low level, thus recovering the bus from an unusable state. Release of the SDA0 line by the slave device can be monitored by reading the ICCR1.SDAI bit. After confirming release of the SDA0 line by the slave device, complete communications by reissuing the stop condition.
Use this facility with the ICFER.MALE bit (master arbitration-lost detection disabled) set to 0. If the MALE bit is set to 1 (master arbitration-lost detection enabled), arbitration is lost when the value of the ICCR1.SDAO bit does not match the state of the SDA0 line, so take care on this point.

Output conditions for using the ICCR1.CLO bit

- When the bus is free (ICCR2.BBSY flag is 0) or in master mode (ICCR2.MST bit is 1 and ICCR2.BBSY flag is 1)
- When the communication device does not hold the SCL0 line low

Figure 27.40 shows the operation timing of the extra SCL clock cycle output function (CLO bit).

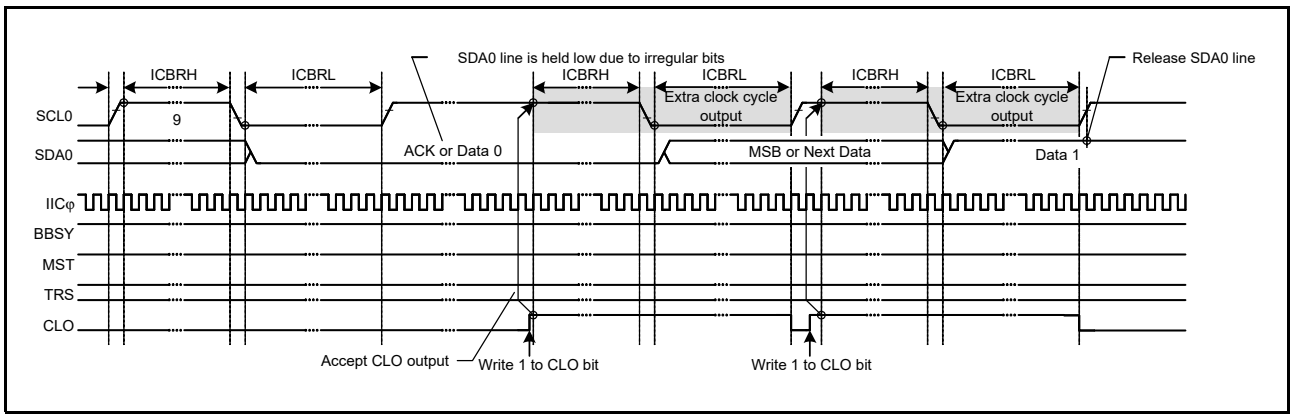


Figure 27.40 Extra SCL Clock Cycle Output Function (CLO Bit)

27.11.3 RIIC Reset and Internal Reset

The RIIC module incorporates a function for resetting itself. There are two types of reset. One is referred to as an RIIC reset; this initializes all registers including the ICCR2.BBSY flag. The other is referred to as an internal reset; this releases the RIIC from the slave-address matched state and initializes the internal counter while retaining other settings. After issuing a reset, be sure to set the ICCR1.IICRST bit to 0.

Both types of reset are effective for release from bus-hung states because both restore the output state of the SCL0 and SDA0 pins to the high-impedance state.

Issuing a reset during slave operation may lead to a loss of synchronization between the master device clock and the slave device clock, so avoided this where possible. Note that monitoring of the bus state, such as for the presence of a start condition, is not possible during an RIIC reset (bits ICE and IICRST in the ICCR1 register are 01b).

For a detailed description of the RIIC and internal resets, refer to section 27.14, Initialization of Registers and Functions When a Reset is Issued or a Condition is Detected.

27.12 SMBus Operation

The RIIC is available for data communication conforming to the SMBus (Version 2.0). To perform SMBus communication, set the ICMR3.SMBS bit to 1. To use the transfer rate within a range of 10 kbps to 100 kbps of the SMBus specification, set the ICMR1.CKS[2:0] bits, the ICBRH register, and the ICBRL register. In addition, determine the values of the ICMR2.DLCS bit and the ICMR2.SDDL[2:0] bits to meet the data hold time specification of 300 ns or more. If the RIIC is used only as a slave device, the transfer rate setting is not necessary, whereas the ICBRL register needs to be set to a value longer than the data setup time (250 ns).
For the SMBus device default address (1100 001b), use one of the slave address registers L0 to L2 (registers SARL0, SARL1, and SARL2), and set the corresponding SARUy.FS bit (7-bit/10-bit address format select) (y = 0 to 2) to 0 (7-bit address format).
When transmitting the UDID (Unique Device Identifier), set the ICFER.SALE bit to 1 to enable the slave arbitration-lost detection function.

27.12.1 SMBus Timeout Measurement

(1) Measuring timeout of slave device

The following period (timeout interval: $T_{LOW:SEXT}$) must be measured for slave devices in SMBus communication.

- From start condition to stop condition

To measure timeout for slave devices, measure the period from start condition detection to stop condition detection with the MTU or TMR timer using a start condition detection interrupt (STI) and stop condition detection interrupt (SPI) of the RIIC. The measured timeout period must be within the total clock low-level period [slave device] $T_{LOW:SEXT}$: 25 ms (max.) of the SMBus specification.
If the time measured with the MTU or TMR exceeds the clock low-level detection timeout $T_{TIMEOUT}$: 25 ms (min.) of the SMBus specification, the slave device must release the bus by writing 1 to the ICCR1.IICRST bit to issue an internal reset of the RIIC. When an internal reset is issued, the RIIC stops driving the bus for the SCL0 pin and SDA0 pin and make the SCL0/SDA0 pin outputs high-impedance, which releases the bus.

(2) Measuring timeout of master device

The following periods (timeout interval: $T_{LOW:MEXT}$) must be measured for master devices in SMBus communication.

- From start condition to acknowledge bit
- Between acknowledge bits
- From acknowledge bit to stop condition

To measure timeout for master devices, measure these periods with the MTU or TMR timer using a start condition detection interrupt (STI), stop condition detection interrupt (SPI), and transmit end interrupt (TEI) or receive data full interrupt (RXI) of the RIIC. The measured timeout period must be within the total clock low-level extended period (master device) $T_{LOW:MEXT}$: 10 ms (max.) of the SMBus specification, and the total of all $T_{LOW:MEXT}$ from start condition to stop condition must be within $T_{LOW:SEXT}$: 25 ms (max.).
For the ACK receive timing (rising edge of the ninth SCL clock cycle), monitor the ICSR2.TEND flag in master transmit mode (master transmitter) and the ICSR2.RDRF flag in master receive mode (master receiver). For this reason, perform bytewise transmit operation in master transmit mode, and hold the ICMR3.RDRFS bit 0 until the byte just before reception of the final byte in master receive mode. While the RDRFS bit is 0, the RDRF flag is set to 1 at the rising edge of the ninth SCL clock cycle.
If the period measured with the MTU or TMR exceeds the total clock low-level extended period (master device) $T_{LOW:MEXT}$: 10 ms (max.) of the SMBus specification or the total of measured periods exceeds the clock low-level detection timeout $T_{TIMEOUT}$: 25 ms (min.) of the SMBus specification, the master device must stop the transaction by issuing a stop condition. In master transmit mode, immediately stop the transmit operation (writing data to the ICDRT register).

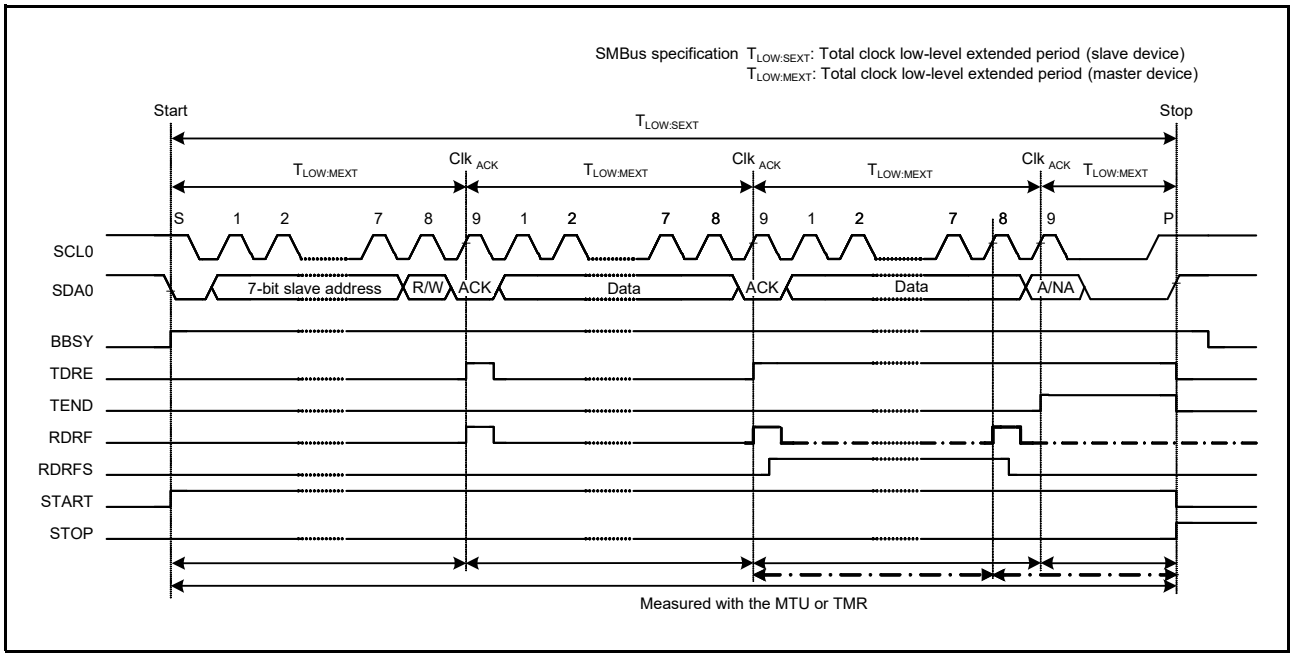


Figure 27.41 SMBus Timeout Measurement

27.12.2 Packet Error Code (PEC)

This MCU incorporates a CRC calculator. The CRC calculator enables transmission of a packet error code (PEC) or checking the received data of the SMBus in data communication of the RIIC. For the CRC generating polynomials of the CRC calculator, refer to section 30, CRC Calculator (CRC).

The PEC data in master transmit mode can be generated by writing all transmit data to the CRC data input register (CRCDIR) in the CRC calculator.

The PEC data in master receive mode can be checked by writing all receive data to CRCDIR in the CRC calculator and comparing the obtained value in the CRC data output register (CRCDOR) with the received PEC data.

To send ACK or NACK according to the match or mismatch result when the final byte is received as a result of the PEC code check, set the ICMR3.RDRFS bit to 1 before the rising edge of the eighth SCL clock cycle during reception of the final byte, and hold the SCL0 line low at the falling edge of the eighth clock cycle.

27.12.3 SMBus Host Notification Protocol (Notify ARP Master Command)

In communications over an SMBus, a slave device can temporarily act as a master device to notify the SMBus host (or ARP master) of its own slave address or to request its own slave address from the SMBus host.

For a product of this MCU to operate as an SMBus host (or ARP master), the host address (0001 000b) sent from the slave device must be detected as a slave address, so the RIIC has a function for detecting the host address. To detect the host address as a slave address, set the ICMR3.SMBS bit and the ICSER.HOAE bit to 1. Operation after the host address has been detected is the same as normal slave operation.

27.13 Interrupt Sources

The RIIC issues four types of interrupt request: transfer error or event generation (arbitration-lost, NACK detection, timeout detection, start condition detection, and stop condition detection), receive data full, transmit data empty, and transmit end.

Table 27.6 lists details of the several interrupt requests. The receive data full and transmit data empty are both capable of activating data transfer by the DTC.

Table 27.6 Interrupt Sources

Symbol	Interrupt Source	Interrupt Flag	DTC Activation	Priority	Interrupt Condition
EEI	Transfer error/ event generation	AL	Not possible	High	AL = 1 and ALIE = 1
		NACKF			NACKF = 1 and NAKIE = 1
		TMOF			TMOF = 1 and TMOIE = 1
		START			START = 1 and STIE = 1
		STOP			STOP = 1 and SPIE = 1
RXI*2	Receive data full	RDRF	Possible		RDRF = 1 and RIE = 1
TXI*1	Transmit data empty	TDRE	Possible		TDRE = 1 and TIE = 1
TEI*3	Transmit end	TEND	Not possible	Low	TEND = 1 and TEIE = 1

Note: There is a delay time between the execution of a write instruction for a peripheral module by the CPU and actual writing to the module. Thus, when an interrupt flag has been cleared or an interrupt request has been masked, read the relevant flag again to check whether clearing or masking has been completed, and then return from interrupt handling. Returning from interrupt handling without checking that writing to the module has been completed creates a possibility of repeated processing of the same interrupt.

Note 1. Because TXI is an edge-detected interrupted, it does not require clearing. Furthermore, the ICSR2.TDRE flag (a condition for TXI) is automatically set to 0 when data for transmission are written to the ICDRT register or a stop condition is detected (ICSR2.STOP flag is 1).

Note 2. Because RXI is an edge-detected interrupted, it does not require clearing. Furthermore, the ICSR2.RDRF flag (a condition for RXI) is automatically set to 0 when data are read from the ICDRR register.

Note 3. When using the TEI interrupt, clear the ICSR2.TEND flag in the TEI interrupt handling.
Note that the ICSR2.TEND flag is automatically set to 0 when data for transmission are written to the ICDRT register or a stop condition is detected (ICSR2.STOP flag is 1).

Clear the each flag or mask the interrupt request during interrupt handling.

27.13.1 Buffer Operation for TXI and RXI Interrupts

If the conditions for generating a TXI and RXI interrupt are satisfied while the corresponding IR flag is 1, the interrupt request is not output for the ICU but retained internally (the capacity for internal retention is one request per source). An interrupt request that was being retained internally is output to the ICU when the value of the ICU.IRn.IR flag becomes 0. Internally retained interrupt requests are automatically cleared under normal conditions of usage.

Internally retained interrupt requests can also be cleared by writing 0 to the corresponding interrupt enable bit in the ICIER register.

27.14 Initialization of Registers and Functions When a Reset is Issued or a Condition is Detected

The RIIC can be reset by MCU reset, RIIC reset, and internal reset functions. Table 27.7 lists the reset states of registers and functions when a reset is issued or a condition is detected.

Table 27.7 Reset States of Registers and Functions When a Reset is Issued or a Condition is Detected

		MCU Reset	RIIC Reset (ICE = 0, IICRST = 1)	Internal Reset (ICE = 1, IICRST = 1)	Start Condition/ Restart Condition Detection	Stop Condition Detection
ICCR1	ICE, IICRST	To be reset	Retained	Retained	Retained	Retained
	SCLO, SDAO		To be reset	To be reset		
	Others			Retained		
ICCR2	BBSY	To be reset	To be reset	Retained	Retained	Retained
	ST, RS			To be reset	To be reset	
	TRS, MST				Retained	To be reset
	SP				To be reset	
ICMR1	BC[2:0]	To be reset	To be reset	To be reset	To be reset	Retained
	Others			Retained	Retained	
ICMR2		To be reset	To be reset	Retained	Retained	Retained
ICMR3	ACKBT	To be reset	To be reset	Retained	Retained	To be reset
	Others					Retained
ICFER		To be reset	To be reset	Retained	Retained	Retained
ICSER		To be reset	To be reset	Retained	Retained	Retained
ICIER		To be reset	To be reset	Retained	Retained	Retained
ICSR1		To be reset	To be reset	To be reset	Retained	To be reset
ICSR2	TDRE, TEND	To be reset	To be reset	To be reset	Retained	To be reset
	START					
	Others					Retained
SARL0, SARL1, SARL2, SARU0, SARU1, SARU2		To be reset	To be reset	Retained	Retained	Retained
ICBRH, ICBRL		To be reset	To be reset	Retained	Retained	Retained
ICDRT		To be reset	To be reset	Retained	Retained	Retained
ICDRR		To be reset	To be reset	Retained	Retained	Retained
ICDRS		To be reset	To be reset	To be reset	Retained	Retained
Timeout function		To be reset	To be reset	To be reset	Operation	Operation
Bus free time measurement		To be reset	To be reset	Operation	Operation	Operation

To be reset: Registers and functions are initialized.
Retained: Registers and functions are not initialized, but retained or updated according to the state.

27.15 Usage Notes

27.15.1 Setting Module Stop Function

Module stop state can be entered or released using module stop control register B (MSTPCRB). The initial setting is for operation of the RIIC to be stopped. RIIC register access is enabled by releasing the module stop state.
For details on module stop control register B, refer to section 11, Low Power Consumption.

27.15.2 Notes on Starting Transfer

If the IR flag corresponding to the RIIC interrupt is 1 when transfer is started (ICCR1.ICE bit is 1), follow the procedure below to clear interrupts before enabling operations. Starting transfer with the IR flag set to 1 while the ICCR1.ICE bit is 1 leads to an interrupt request being internally retained after transfer starts, and this can lead to unanticipated behavior of the IR flag.

1. Confirm that the ICCR1.ICE bit is 0.
2. Set the relevant interrupt enable bits (ICIER.TIE, etc.) on the peripheral function side to 0.
3. Read the relevant interrupt enable bits (ICIER.TIE, etc.) on the peripheral function side and confirm that its value is 0.
4. Set the IR flag to 0.

28. CAN Module (RSCAN)

28.1 Overview

This MCU incorporates the Controller Area Network (CAN) module with one channel of CAN protocol controller conforming to the ISO 11898-1 standard. Table 28.1 shows the CAN module specifications. Figure 28.1 shows the CAN module block diagram. Table 28.2 lists the I/O pins of the CAN module.
In this section, the following variables indicate the number of registers.

- j (j = 0 to 15): Receive rule entry register number
  (GAFLIDLj, GAFLIDHj, GAFLMLj, GAFLMHj, GAFLPLj, GAFLPHj)
- m (m = 0, 1): Receive FIFO buffer number
- n (n = 0 to 15): Receive buffer number
- p (p = 0 to 3): Transmit buffer number
- r (r = 0 to 127): RAM test register (RPGACCr) number

Table 28.1 CAN Module Specifications (1/2)

Item	Specification
Number of channels	1
Protocol	ISO 11898-1 compliant
Communication speed	• Maximum 1 Mbps $\text{Communication speed (CAN bit time clock)} = \frac{1}{\text{CAN bit time}}$ CAN bit time = CANTq × Tq count per bit $\text{CANTq} = \frac{\text{CFGL.BRP[9:0] bits} + 1}{\text{fCAN}}$ Tq: Time quantum fCAN: Frequency of CAN clock source (selected by the GCFGL.DCS bit)
Buffer	20 buffers in total • Individual buffers: 4 buffers (4 buffers for one channel) Transmit buffer: 4 buffers per a channel • Shared buffers: 16 buffers Receive buffer: 0 to 16 buffers Receive FIFO buffer: 2 FIFO buffers (up to 16 buffers allocatable to each) Transmit/receive FIFO buffer: A FIFO buffer per a channel (up to 16 buffers allocatable to each)
Reception function	• Receives data frames and remote frames. • Selects ID format (standard ID, extended ID, or both IDs) to be received. • Sets interrupt enable/disable for each FIFO. • Mirror function (to receive messages transmitted from the own CAN node) • Timestamp function (to record message reception time as a 16-bit timer value)
Reception filter function	• Selects receive messages according to 16 receive rules. • Sets the number of receive rules (0 to 16) for each channel. • Acceptance filter processing: Sets ID and mask for each receive rule. • DLC filter processing: Sets DLC check value for each receive rule.
Receive message transfer function	• Routing function to transfer receive messages to arbitrary destinations (can be transferred to up to 2 buffers). Transfer destination: Receive buffer, receive FIFO buffer, and transmit/receive FIFO buffer • Label addition function Stores label information together when storing a message in a receive buffer and FIFO buffer.
Transmission function	• Transmits data frames and remote frames. • Selects ID format (standard ID, extended ID, or both IDs) to be transmitted. • Sets interrupt enable/disable for each transmit buffer and transmit/receive FIFO buffer. • Selects ID priority transmission or transmit buffer number priority transmission. • Transmit abort function (completion of the abort can be confirmed with the flag) • One-shot transmission function
Interval transmission function	Sets message transmission interval time (transmit mode of transmit/receive FIFO buffers)

Table 28.1 CAN Module Specifications (2/2)

Item	Specification
Transmit history function	Stores the history information of transmitted messages.
Bus off recovery mode selection	Selects a method of returning from bus off state. • ISO 11898-1 compliant • Automatic transition to channel halt mode at bus-off entry • Automatic transition to channel halt mode at bus-off end • Transition to channel halt mode by a program • Transition to the error-active state by a program (forcible return from the bus off state)
Error status monitoring	• Monitors CAN protocol errors (stuff error, form error, ACK error, CRC error, bit error, ACK delimiter error, and bus dominant lock). • Detects error status transitions (error warning, error passive, bus off entry, and bus off recovery) • Reads the error counter. • Monitors DLC errors.
Interrupt source	5 sources • Global (2 sources) Global receive FIFO interrupt Global error interrupt • Channel (3 sources/channel) Channel transmit interrupt – Transmit complete interrupt – Transmit abort interrupt – Transmit/receive FIFO transmit complete interrupt – Transmit history interrupt Transmit/receive FIFO receive interrupt Channel error interrupt
CAN clock source	Peripheral module clock (PCLK), CANMCLK
Test function	Test function for user evaluation • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback) • RAM test (read/write test)
Low power consumption	Module stop state can be set.

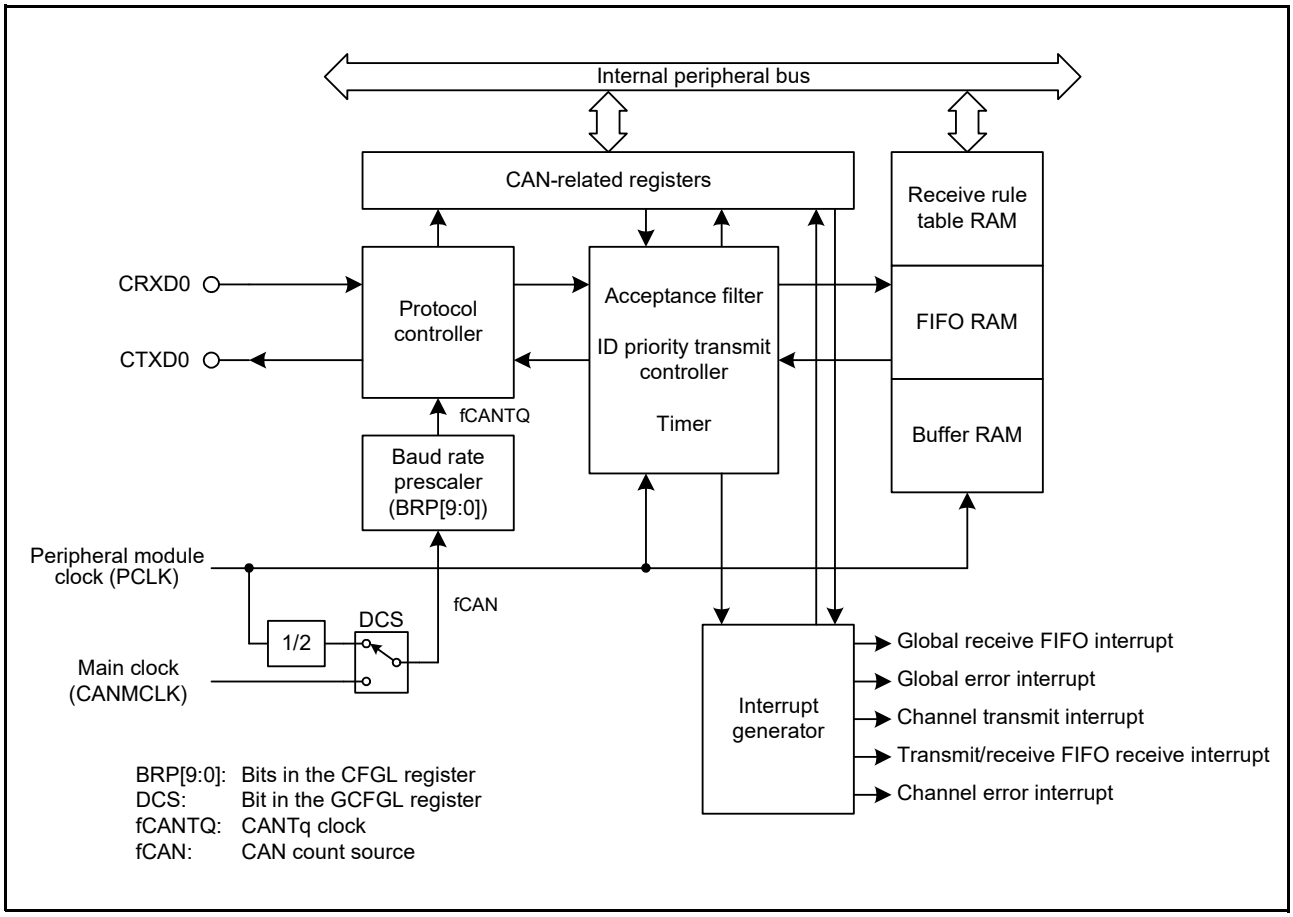


Figure 28.1 CAN Module Block Diagram

- CRXD0/CTXD0: CAN input/output pins
- Protocol controller: Handles CAN protocol processing such as bus arbitration, bit timing at transmission and reception, stuffing, and error handling, etc.
- Receive rule table RAM: Stores the rules for filtering received messages. Each receive rule specifies an ID/ frame format/data length code of the message to be received, a label to be attached to the message that has passed through the filter, and the location of such message to be stored.
- FIFO RAM: Includes three 16-stage FIFO buffers. There are two FIFOs for reception only and one FIFO for transmission or reception.
- Buffer RAM: Used as a transmit and receive buffer. There are 4 buffers for transmission and 16 buffers for reception.
- Acceptance filter: Performs filtering of received messages.
- Timer: There are a timer for timestamp function during reception and a timer which determines the message transmission intervals while using the transmit FIFO buffer.

Table 28.2 I/O Pins of the CAN Module

Pin Name	I/O	Description
CRXD0	Input	Receive data input pins of the RSCAN0
CTXD0	Output	Transmit data output pins of the RSCAN0

28.2 Register Descriptions

28.2.1 Bit Configuration Register L (CFGL)

Address(es): RSCAN0.CFGL 000A 8300h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	BRP[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b9 to b0	BRP[9:0]	Prescaler Division Ratio Set	When these bits are set to P (0 to 1023), the baud rate prescaler divides fCAN by P + 1.	R/W
b15 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Modify the CFGL register only in channel reset mode or channel halt mode. Set this register in channel reset mode before making a transition to channel communication mode or channel halt mode. For setting bit timing, see section 28.9, Initial Settings.

BRP[9:0] Bits (Prescaler Division Ratio Set)

The CAN Tq clock (fCANTQ) is obtained by the CAN clock source (fCAN) and setting the clock division ratio with the BRP[9:0] bits and one clock cycle of the CAN Tq clock is 1 Time Quantum (Tq).

28.2.2 Bit Configuration Register H (CFGH)

Address(es): RSCAN0.CFGH 000A 8302h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	SJW[1:0]		—	TSEG2[2:0]			TSEG1[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	TSEG1[3:0]	Time Segment 1 Control	b3 b0 0 0 0 0: Setting prohibited 0 0 0 1: Setting prohibited 0 0 1 0: Setting prohibited 0 0 1 1: 4 Tq 0 1 0 0: 5 Tq 0 1 0 1: 6 Tq 0 1 1 0: 7 Tq 0 1 1 1: 8 Tq 1 0 0 0: 9 Tq 1 0 0 1: 10 Tq 1 0 1 0: 11 Tq 1 0 1 1: 12 Tq 1 1 0 0: 13 Tq 1 1 0 1: 14 Tq 1 1 1 0: 15 Tq 1 1 1 1: 16 Tq	R/W
b6 to b4	TSEG2[2:0]	Time Segment 2 Control	b6 b4 0 0 0: Setting prohibited 0 0 1: 2 Tq 0 1 0: 3 Tq 0 1 1: 4 Tq 1 0 0: 5 Tq 1 0 1: 6 Tq 1 1 0: 7 Tq 1 1 1: 8 Tq	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b9, b8	SJW[1:0]	Resynchronization Jump Width Control	b9 b8 0 0: 1 Tq 0 1: 2 Tq 1 0: 3 Tq 1 1: 4 Tq	R/W
b15 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Modify the CFGH register only in channel reset mode or channel halt mode. Set this register in channel reset mode before making a transition to channel communication mode or channel halt mode. For setting bit timing, see section 28.9, Initial Settings.

TSEG1[3:0] Bits (Time Segment 1 Control)

These bits are used to specify a Tq value for the total length of the propagation time segment (PROP_SEG) and phase buffer segment 1 (PHASE_SEG1). A value of 4 Tq to 16 Tq can be set.

TSEG2[2:0] Bits (Time Segment 2 Control)

These bits are used to specify a Tq value for the length of phase buffer segment 2 (PHASE_SEG2).
A value of 2 Tq to 8 Tq can be set. Set a value smaller than the value of the TSEG1[3:0] bits.

SJW[1:0] Bits (Resynchronization Jump Width Control)

These bits are used to specify a Tq value for the resynchronization jump width. A value of 1 Tq to 4 Tq can be set. Set a value equal to or smaller than the value of the TSEG2[3:0] bits.

28.2.3 Control Register L (CTRL)

Address(es): RSCAN0.CTRL 000A 8304h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ALIE	BLIE	OLIE	BORIE	BOEIE	EPIE	EWIE	BEIE	—	—	—	—	RTBO	CSLPR	CHMDC[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bit	Symbol	Bit Name	Description	R/W
b1, b0	CHMDC[1:0]	Mode Select	b1 b0 0 0: Channel communication mode. 0 1: Channel reset mode. 1 0: Channel halt mode. 1 1: Setting prohibited.	R/W
b2	CSLPR	Channel Stop Mode	0: Other than channel stop mode. 1: Channel stop mode.	R/W
b3	RTBO	Forcible Return from Bus-off	When this bit is set to 1, forcible return from the bus off state is made. This bit is read as 0.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	BEIE	Protocol Error Interrupt Enable	0: Protocol error interrupt is disabled. 1: Protocol error interrupt is enabled.	R/W
b9	EWIE	Error Warning Interrupt Enable	0: Error warning interrupt is disabled. 1: Error warning interrupt is enabled.	R/W
b10	EPIE	Error Passive Interrupt Enable	0: Error passive interrupt is disabled. 1: Error passive interrupt is enabled.	R/W
b11	BOEIE	Bus Off Entry Interrupt Enable	0: Bus off entry interrupt is disabled. 1: Bus off entry interrupt is enabled.	R/W
b12	BORIE	Bus Off Recovery Interrupt Enable	0: Bus off recovery interrupt is disabled. 1: Bus off recovery interrupt is enabled.	R/W
b13	OLIE	Overload Frame Transmit Interrupt Enable	0: Overload frame transmit interrupt is disabled. 1: Overload frame transmit interrupt is enabled.	R/W
b14	BLIE	Bus Lock Interrupt Enable	0: Bus lock interrupt is disabled. 1: Bus lock interrupt is enabled.	R/W
b15	ALIE	Arbitration Lost Interrupt Enable	0: Arbitration lost interrupt is disabled. 1: Arbitration lost interrupt is enabled.	R/W

CHMDC[1:0] Bits (Mode Select)

These bits are used to select a channel mode (channel communication mode, channel reset mode, or channel halt mode). For details, see section 28.3.2, Channel Modes. Setting the CSLPR bit to 1 in channel reset mode allows transition to channel stop mode. Do not set the CHMDC[1:0] bits to 11b. When the CAN module has transitioned to channel halt mode depending on the setting of the CTRH.BOM[1:0] bits, the CHMDC[1:0] bits automatically become 10b.

CSLPR Bit (Channel Stop Mode)

Setting this bit to 1 places the channel in channel stop mode.
Setting this bit to 0 makes the channel leave from channel stop mode.
Do not modify this bit in channel communication mode or channel halt mode.

RTBO Bit (Forcible Return from Bus-off)

Setting this bit to 1 (forcible return from the bus off state) in the bus off state forcibly returns the state from the bus off state to the error active state. This bit is automatically set to 0. Setting this bit to 1 sets the STSH.TEC[7:0] and STSH.REC[7:0] flags to 00h and also sets the STSL.BOSTS flag to 0 (not in bus off state).The other registers remain unchanged. No bus off recovery interrupt request due to return from the bus off state is generated. Use this bit only when the CTRH.BOM[1:0] bits are 00b (ISO 11898-1 compliant).

A delay of up to 1 CAN bit time occurs after the RTBO bit is set to 1 until the CAN module transitions to the error active state. Set this bit to 1 in channel communication mode.

BEIE Bit (Protocol Error Interrupt Enable)

When the ERFLL.BEF flag is set to 1 while the BEIE bit is 1, an error interrupt request is generated. Modify this bit only in channel reset mode.

EWIE Bit (Error Warning Interrupt Enable)

When the ERFLL.EWF flag is set to 1 while the EWIE bit is 1, an error interrupt request is generated. Modify this bit only in channel reset mode.

EPIE Bit (Error Passive Interrupt Enable)

When the ERFLL.EPF flag is set to 1 while the EPIE bit is 1, an error interrupt request is generated. Modify this bit only in channel reset mode.

BOEIE Bit (Bus Off Entry Interrupt Enable)

When the ERFLL.BOEF flag is set to 1 while the BOEIE bit is 1, an error interrupt request is generated. Modify this bit only in channel reset mode.

BORIE Bit (Bus Off Recovery Interrupt Enable)

When the ERFLL.BORF flag is set to 1 while the BORIE bit is 1, an error interrupt request is generated. Modify this bit only in channel reset mode.

OLIE Bit (Overload Frame Transmit Interrupt Enable)

When the ERFLL.OVLF flag is set to 1 while the OLIE bit is 1, an error interrupt request is generated. Modify this bit only in channel reset mode.

BLIE Bit (Bus Lock Interrupt Enable)

When the ERFLL.BLF flag is set to 1 while the BLIE bit is 1, an error interrupt request is generated. Modify this bit only in channel reset mode.

ALIE Bit (Arbitration Lost Interrupt Enable)

When the ERFLL.ALF flag is set to 1 while the ALIE bit is 1, an error interrupt request is generated. Modify this bit only in channel reset mode.

28.2.4 Control Register H (CTRH)

Address(es): RSCAN0.CTRH 000A 8306h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	CTMS[1:0]		CTME	ERRD	BOM[1:0]		—	—	—	—	TAIE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TAIE	Transmit Abort Interrupt Enable	0: Transmit abort interrupt is disabled. 1: Transmit abort interrupt is enabled.	R/W
b4 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6, b5	BOM[1:0]	Bus Off Recovery Mode Select	b6 b5 0 0: ISO 11898-1 compliant 0 1: Transition to channel halt mode at bus-off entry 1 0: Transition to channel halt mode at bus-off end 1 1: Transition to channel halt mode in the bus off state by a program request	R/W
b7	ERRD	Error Display Mode Select	0: Only the first error is indicated after bits 14 to 8 in the ERFLL register have all been cleared. 1: The error flags of all errors are indicated.	R/W
b8	CTME	Communication Test Mode Enable	0: Communication test mode is disabled. 1: Communication test mode is enabled.	R/W
b10, b9	CTMS[1:0]	Communication Test Mode Select	b10 b9 0 0: Standard test mode 0 1: Listen-only mode 1 0: Self-test mode 0 (external loopback mode) 1 1: Self-test mode 1 (internal loopback mode)	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TAIE Bit (Transmit Abort Interrupt Enable)

When transmit abort of the transmit buffer is completed with the TAIE bit set to 1, an interrupt request is generated. Modify this bit only in channel reset mode.

BOM[1:0] Bits (Bus Off Recovery Mode Select)

These bits are used to select a bus off recovery mode of the CAN module.

When the BOM[1:0] bits are set to 00b, return to the error active state from the bus off state is compliant with the ISO 11898-1 standard. That is, the CAN module reenters the CAN communication (error active state) after 11 consecutive recessive bits are detected 128 times. A bus off recovery interrupt request is generated at the time of return from the bus off state. Even if the CTRL.CHMDC[1:0] bits are set to 10b (channel halt mode) before recessive bits are detected 128 times, the CAN module does not transition to channel halt mode until recessive bits are detected 128 times.

When the CAN module reaches the bus off state while the BOM[1:0] bits are set to 01b, the CTRL.CHMDC[1:0] bits are set to 10b and the CAN module transitions to channel halt mode. No bus off recovery interrupt request is generated at the time of return from the bus off state and the STSH.TEC[7:0] and STSH.REC[7:0] flags are set to 00h.

When the CAN module reaches the bus off state when the BOM[1:0] bits are set to 10b, the CTRL.CHMDC[1:0] bits are set to 10b and the CAN module transitions to channel halt mode after return from the bus off state (11 consecutive recessive bits are detected 128 times). A bus off recovery interrupt request is generated at the time of return from the bus off state and the STSH.TEC[7:0] and STSH.REC[7:0] flags are set to 00h.

When the BOM[1:0] bits are set to 11b and the CTRL.CHMDC[1:0] bits are set to 10b while the CAN module is in the bus off state, the CAN module transitions to channel halt mode. No bus off recovery interrupt request is generated at the time of return from the bus off state and the STSH.TEC[7:0] and STSH.REC[7:0] flags are set to 00h. However, if 11 consecutive recessive bits are detected 128 times and the CAN module has recovered to the error active state from the

bus off state before the CTRL.CHMDC[1:0] bits are set to 10b, a bus off recovery interrupt request is generated.
If the CPU requests transition to channel reset mode at the same time when the CAN module transitions to channel halt mode (at bus off entry when the BOM[1:0] bits are 01b or at bus off end when the BOM[1:0] bits are 10b), the CPU's request takes precedence. Modify these bits only in channel reset mode.

ERRD Bit (Error Display Mode Select)

This bit is used to control display mode of bits 14 to 8 in the ERFLL register.
When this bit is 0, only the flags of the first error are set to 1. If two or more errors occur first, all the flags of detected errors are set to 1.
When this bit is 1, all the flags of errors that have occurred are set to 1 regardless of the error occurrence order. Modify this bit only in channel reset mode or channel halt mode.

CTME Bit (Communication Test Mode Enable)

Setting this bit to 1 enables communication test mode. Modify this bit only in channel halt mode. This bit is set to 0 in channel reset mode.

CTMS[1:0] Bits (Communication Test Mode Select)

These bits are used to select a communication test mode. Modify these bits only in channel halt mode. These bits are set to 0 in channel reset mode.

28.2.5 Status Register L (STSL)

Address(es): RSCAN0.STSL 000A 8308h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	COMSTS	RECSTS	TRMSTS	BOSTS	EPSTS	CSLPSTS	CHLTSTS	CRSTSTS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	CRSTSTS	Channel Reset Status Flag	0: Not in channel reset mode 1: In channel reset mode	R
b1	CHLTSTS	Channel Halt Status Flag	0: Not in channel halt mode 1: In channel halt mode	R
b2	CSLPSTS	Channel Stop Status Flag	0: Not in channel stop mode 1: In channel stop mode	R
b3	EPSTS	Error Passive Status Flag	0: Not in error passive state 1: In error passive state	R
b4	BOSTS	Bus Off Status Flag	0: Not in bus off state 1: In bus off state	R
b5	TRMSTS	Transmit Status Flag	0: Bus idle or in reception 1: In transmission or bus off state	R
b6	RECSTS	Receive Status Flag	0: Bus idle, in transmission or bus off state 1: In reception	R
b7	COMSTS	Communication Status Flag	0: Communication is not ready. 1: Communication is ready.	R
b15 to b8	—	Reserved	These bits are read as 0.	R

CRSTSTS Flag (Channel Reset Status Flag)

This flag is set to 1 when the CAN module has transitioned to channel reset mode, and is set to 0 when the CAN module has transitioned to channel communication mode or channel halt mode. This flag remains 1 even if the CAN module transitions from channel reset mode to channel stop mode.

CHLTSTS Flag (Channel Halt Status Flag)

This flag is set to 1 when the CAN module has transitioned to channel halt mode, and is set to 0 when the CAN module has exited channel halt mode.

CSLPSTS Flag (Channel Stop Status Flag)

This flag is set to 1 when the CAN module has transitioned to channel stop mode, and is set to 0 when the CAN module has returned from channel stop mode.

EPSTS Flag (Error Passive Status Flag)

This flag is set to 1 when the CAN module has entered the error passive state (128 ≤ STSH.TEC[7:0] value ≤ 255 or 128 ≤ STSH.REC[7:0] value), and is set to 0 when the CAN module has exited the error passive state or has entered channel reset mode.

BOSTS Flag (Bus Off Status Flag)

This flag is set to 1 when the CAN module has entered the bus off state (STSH.TEC[7:0] value > 255), and is set to 0 when the CAN module has exited the bus off state.

TRMSTS Flag (Transmit Status Flag)

This flag is set to 1 when transmission has started, and is set to 0 when the bus has become idle or reception has started. This flag remains 1 in the bus off state.

RECSTS Flag (Receive Status Flag)

This flag is set to 1 when reception has started, and is set to 0 when the bus has become idle or transmission has started.

COMSTS Flag (Communication Status Flag)

This flag indicates that communication is ready.
This flag becomes 1 when the CAN module has detected 11 consecutive recessive bits after it has transitioned from channel reset mode or channel halt mode to channel communication mode. This flag becomes 0 in channel reset mode or channel halt mode.

28.2.6 Status Register H (STSH)

Address(es): RSCAN0.STSH 000A 830Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TEC[7:0]								REC[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description	R/W
b7 to b0	REC[7:0]	The receive error counter (REC) can be read.	R
b15 to b8	TEC[7:0]	The transmit error counter (TEC) can be read.	R

REC[7:0] Flags

These flags indicate the receive error counter value. For receive error counter increment/decrement conditions, see the CAN standard (ISO 11898-1).
These flags become 00h in channel reset mode.

TEC[7:0] Flags

These flags indicate the transmit error counter value. For transmit error counter increment/decrement conditions, see the CAN standard (ISO 11898-1).
These flags become 00h in channel reset mode.

28.2.7 Error Flag Register L (ERFLL)

Address(es): RSCAN0.ERFLL 000A 830Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	ADERR	B0ERR	B1ERR	CERR	AERR	FERR	SERR	ALF	BLF	OVLF	BORF	BOEF	EPF	EWF	BEF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	BEF	Bus Error Flag	0: No channel bus error is detected. 1: Channel bus error is detected.	R/(W) *1
b1	EWF	Error Warning Flag	0: No error warning is detected. 1: Error warning is detected.	R/(W) *1
b2	EPF	Error Passive Flag	0: No error passive is detected. 1: Error passive is detected.	R/(W) *1
b3	BOEF	Bus Off Entry Flag	0: No bus off entry is detected. 1: Bus off entry is detected.	R/(W) *1
b4	BORF	Bus Off Recovery Flag	0: No bus off recovery is detected. 1: Bus off recovery is detected.	R/(W) *1
b5	OVLF	Overload Flag	0: No overload is detected. 1: Overload is detected.	R/(W) *1
b6	BLF	Bus Lock Flag	0: No channel bus lock is detected. 1: Channel bus lock is detected.	R/(W) *1
b7	ALF	Arbitration Lost Flag	0: No arbitration lost is detected. 1: Arbitration lost is detected.	R/(W) *1
b8	SERR	Stuff Error Flag	0: No stuff error is detected. 1: Stuff error is detected.	R/(W) *1
b9	FERR	Form Error Flag	0: No form error is detected. 1: Form error is detected.	R/(W) *1
b10	AERR	ACK Error Flag	0: No ACK error is detected. 1: ACK error is detected.	R/(W) *1
b11	CERR	CRC Error Flag	0: No CRC error is detected. 1: CRC error is detected.	R/(W) *1
b12	B1ERR	Recessive Bit Error Flag	0: No recessive bit error is detected. 1: Recessive bit error is detected.	R/(W) *1
b13	B0ERR	Dominant Bit Error Flag	0: No dominant bit error is detected. 1: Dominant bit error is detected.	R/(W) *1
b14	ADERR	ACK Delimiter Error Flag	0: No ACK delimiter error is detected. 1: ACK delimiter error is detected.	R/(W) *1
b15	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note 1. The only effective value for writing to this flag is 0, which clears the flag. Otherwise writing to the flag results in retention of its state.

See the CAN standard (ISO 11898-1) if you want to check error occurrence conditions. To clear each flag of this register, write 0 by the program. These flags cannot be set to 1 by the program. If any of these flags is set to 1 at the timing when the program writes 0 to the flag, the flag becomes 1. Each flag becomes 0 in channel reset mode.
With respect to bits 14 to 8 in the ERFLL register, if an error is detected with all flags of bits 14 to 8 set to 0 when the CTRH.ERRD bit is set to 0 (only the first error information is displayed), the corresponding flag becomes 1.

BEF Flag (Bus Error Flag)

This flag is set to 1 when any one of the ADERR, B0ERR, B1ERR, CERR, AERR, FERR, and SERR flags is set to 1.

EWF Flag (Error Warning Flag)

This flag becomes 1 only when the STSH.REC[7:0] or STSH.TEC[7:0] value exceeds 95 for the first time. Therefore, if the program writes 0 to this flag with the STSH.REC[7:0] or STSH.TEC [7:0] value remaining over 95, this bit is not set to 1 until both STSH.REC[7:0] and STSH.TEC[7:0] values become 95 or less and then the STSH.REC[7:0] or STSH.TEC[7:0] value exceeds 95 again.

EPF Flag (Error Passive Flag)

This flag becomes 1 when the CAN module becomes error passive state (STSH.REC[7:0] or STSH.TEC[7:0] value > 127). This flag becomes 1 only when the STSH.REC[7:0] or STSH.TEC[7:0] value exceeds 127 for the first time. Therefore, if the program writes 0 to this flag with the STSH.REC[7:0] or STSH.TEC[7:0] value remaining over 127, this bit is not set to 1 until both STSH.REC[7:0] and STSH.TEC[7:0] values become 127 or less and then the STSH.REC[7:0] or STSH.TEC[7:0] value exceeds 127 again.

BOEF Flag (Bus Off Entry Flag)

This flag is set to 1 when the state becomes bus off state (STSH.TEC[7:0] value > 255). This flag is also set to 1 when the state becomes bus off state with the CTRH.BOM[1:0] bits set to 01b (transition to channel halt mode at bus off entry).

BORF Flag (Bus Off Recovery Flag)

This flag is set to 1 when 11 consecutive recessive bits have been detected 128 times and the CAN module returns from the bus off state. However, this flag is not set to 1 if the CAN module returns from the bus off state in any of the following ways before 11 consecutive recessive bits are detected 128 times.

- The CTRL.CHMDC[1:0] bits are set to 01b (channel reset mode).
- The CTRL.RTBO bit is set to 1 (forcible return from the bus off state is made).
- The CTRH.BOM[1:0] bits are set to 01b (transition to channel halt mode at bus off entry).
- The CTRL.CHMDC[1:0] bits are set to 10b (channel halt mode) before 11 consecutive recessive bits are detected 128 times with the CTRH.BOM[1:0] bits set to 11b (transition to channel halt mode upon a request from the program during bus off).

OVLF Flag (Overload Flag)

This flag is set to 1 when the overload frame transmit condition has been detected when performing reception or transmission.

BLF Flag (Bus Lock Flag)

This flag is set to 1 when 32 consecutive dominant bits have been detected on the CAN bus in channel communication mode. After that, detection of the bus lock becomes possible again if either of the following conditions is met.

- A recessive bit is detected after the BLF flag has been modified from 1 to 0.
- The CAN module transitions to channel reset mode and returns to channel communication mode after the BLF flag has been modified from 1 to 0.

ALF Flag (Arbitration Lost Flag)

This flag is set to 1 when an arbitration lost has been detected.

SERR Flag (Stuff Error Flag)

This flag is set to 1 when a stuff error has been detected.

FERR Flag (Form Error Flag)

This flag is set to 1 when a form error has been detected.

AERR Flag (ACK Error Flag)

This flag is set to 1 when an ACK error has been detected.

CERR Flag (CRC Error Flag)

This flag is set to 1 when a CRC error has been detected.

B1ERR Flag (Recessive Bit Error Flag)

This flag is set to 1 when a dominant bit has been detected though a recessive bit was transmitted.

B0ERR Flag (Dominant Bit Error Flag)

This flag is set to 1 when a recessive bit has been detected though a dominant bit was transmitted.

ADERR Flag (ACK Delimiter Error Flag)

This flag is set to 1 when a form error has been detected in the ACK delimiter during transmission.

28.2.8 Error Flag Register H (ERFLH)

Address(es): RSCAN0.ERFLH 000A 830Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	CRCREG[14:0]														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b14 to b0	CRCREG[14:0]	CRC Calculation Data	A CRC value calculated based on the transmit message or receive message is indicated.	R
b15	—	Reserved	This bit is read as 0.	R

CRCREG[14:0] Flags (CRC Calculation Data)

When the CTRH.CTME bit is set to 1 (communication test mode is enabled), the CRC value calculated based on the transmit or receive message can be read. When the CTRH.CTME bit is set to 0 (communication test mode is disabled), these bits are read as 0.

28.2.9 Global Configuration Register L (GCFGL)

Address(es): RSCAN.GCFGL 000A 8322h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	TSSS	TSP[3:0]				—	—	—	DCS	MME	DRE	DCE	TPRI
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TPRI	Transmit Priority Select	0: ID priority 1: Transmit buffer number priority	R/W
b1	DCE	DLC Check Enable	0: DLC check is disabled. 1: DLC check is enabled.	R/W
b2	DRE	DLC Replacement Enable	0: DLC replacement is disabled. 1: DLC replacement is enabled.	R/W
b3	MME	Mirror Function Enable	0: Mirror function is disabled. 1: Mirror function is enabled.	R/W
b4	DCS	CAN Clock Source Select	0: PCLK 1: CANMCLK (obtained from the main clock)	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b11 to b8	TSP[3:0]	Timestamp Clock Source Division	b11 b8 0 0 0 0: Not divided 0 0 0 1: Divided by 2 0 0 1 0: Divided by 4 0 0 1 1: Divided by 8 0 1 0 0: Divided by 16 0 1 0 1: Divided by 32 0 1 1 0: Divided by 64 0 1 1 1: Divided by 128 1 0 0 0: Divided by 256 1 0 0 1: Divided by 512 1 0 1 0: Divided by 1024 1 0 1 1: Divided by 2048 1 1 0 0: Divided by 4096 1 1 0 1: Divided by 8192 1 1 1 0: Divided by 16384 1 1 1 1: Divided by 32768	R/W
b12	TSSS	Timestamp Clock Source Select	0: PCLK 1: CAN bit time clock	R/W
b15 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Modify the GCFGL register only in global reset mode.

TPRI Bit (Transmit Priority Select)

This bit is used to set the transmit priority.

When this bit is set to 0, ID priority is selected and the transmit priority complies with the CAN bus arbitration rule (ISO 11898-1 standard). When this bit is set to 1, transmit buffer number priority is selected and the minimum number of transmit buffer specified for transmission takes precedence.

DCE Bit (DLC Check Enable)

Setting this bit to 1 makes the DLC check function available. Set the GAFLPHj.GAFLDLC[3:0] bits to 0000b before setting the DCE bit to 0.

DRE Bit (DLC Replacement Enable)

When the DRE bit is set to 1, the DLC value of the receive rule is stored in the buffer instead of the DLC value of the received message after the DLC value has passed through the DLC filter. In this case, a value of 00h is stored in the data byte that exceeds the DLC value of the receive rule.
When the DCE bit is set to 1 (DLC check is enabled), the DLC replacement function is available.

MME Bit (Mirror Function Enable)

Setting this bit to 1 makes the mirror function available.

DCS Bit (CAN Clock Source Select)

When this bit is set to 0, the peripheral clock (PCLK) divided by 2 is used as the CAN clock source (fCAN).
When this bit is set to 1, CANMCLK obtained from the EXTAL pin is used as the CAN clock source (fCAN).

TSP[3:0] Bits (Timestamp Clock Source Division)

The clock obtained by dividing the clock source selected by the TSSS bit by the TSP[3:0] value is the count source of the timestamp counter.

TSSS Bit (Timestamp Clock Source Select)

This bit is used to select a clock source of the timestamp counter.

28.2.10 Global Configuration Register H (GCFGH)

Address(es): RSCAN.GCFGH 000A 8324h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ITRCP[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	ITRCP[15:0]	Interval Timer Prescaler Set	If the set value is M, PCLK is frequency-divided by M. Setting 0000h is prohibited when the interval timer is in use.	R/W

Modify the GCFGH register only in global reset mode.

ITRCP[15:0] Bits (Interval Timer Prescaler Set)

These bits are used to set a clock source division value of the interval timer for FIFO buffers. For details, see section 28.5.3 (1) Interval Transmission Function.

28.2.11 Global Control Register L (GCTRL)

Address(es): RSCAN.GCTRL 000A 8326h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	THLEIE	MEIE	DEIE	—	—	—	—	—	GSLPR	GMDC[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bit	Symbol	Bit Name	Description	R/W
b1, b0	GMDC[1:0]	Global Mode Select	b1 b0 0 0: Global operating mode 0 1: Global reset mode 1 0: Global test mode 1 1: Setting prohibited	R/W
b2	GSLPR	Global Stop Mode	0: Other than global stop mode 1: Global stop mode	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	DEIE	DLC Error Interrupt Enable	0: DLC error interrupt is disabled. 1: DLC error interrupt is enabled.	R/W
b9	MEIE	FIFO Message Lost Interrupt Enable	0: FIFO message lost interrupt is disabled. 1: FIFO message lost interrupt is enabled.	R/W
b10	THLEIE	Transmit History Buffer Overflow Interrupt Enable	0: Transmit history buffer overflow interrupt is disabled. 1: Transmit history buffer overflow interrupt is enabled.	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

GMDC[1:0] Bits (Global Mode Select)

These bits are used to select the mode of entire CAN module (global operating mode, global reset mode, or global test mode). For details, see section 28.3.1, Global Modes. Setting the GSLPR bit to 1 in global reset mode places the CAN module in global stop mode.

GSLPR Bit (Global Stop Mode)

Setting this bit to 1 places the CAN module in global stop mode.
Setting this bit to 0 makes the CAN module leave from global stop mode.
Do not modify this bit in global operating mode or in global test mode.

DEIE Bit (DLC Error Interrupt Enable)

When the DEIE bit is set to 1 and the GERFLL.DEF flag is set to 1, an interrupt request is generated. Modify this bit only in global reset mode.

MEIE Bit (FIFO Message Lost Interrupt Enable)

When the MEIE bit is set to 1 and the GERFLL.MES flag is set to 1, an interrupt request is generated. Modify this bit only in global reset mode.

THLEIE Bit (Transmit History Buffer Overflow Interrupt Enable)

When the THLEIE bit is set to 1 and the GERFLL.THLES flag is set to 1, an interrupt request is generated. Modify this bit only in global reset mode.

28.2.12 Global Control Register H (GCTRH)

Address(es): RSCAN.GCTRH 000A 8328h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TSRST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TSRST	Timestamp Counter Reset	Setting the TSRST bit to 1 resets the timestamp counter. This bit is read as 0.	R/W
b15 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TSRST Bit (Timestamp Counter Reset)

This bit is used to reset the timestamp counter. When this bit is set to 1, the GTSC register is set to 0000h.

28.2.13 Global Status Register (GSTS)

Address(es): RSCAN.GSTS 000A 832Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	GRAMINIT	GSLPSTS	GHLTSTS	GRSTSTS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	GRSTSTS	Global Reset Status Flag	0: Not in global reset mode 1: In global reset mode	R
b1	GHLTSTS	Global Test Status Flag	0: Not in global test mode 1: In global test mode	R
b2	GSLPSTS	Global Stop Status Flag	0: Not in global stop mode 1: In global stop mode	R
b3	GRAMINIT	CAN RAM Initialization Status Flag	0: CAN RAM initialization is completed. 1: CAN RAM initialization is ongoing.	R
b15 to b4	—	Reserved	These bits are read as 0.	R

GRSTSTS Flag (Global Reset Status Flag)

This flag is set to 1 when the CAN module has transitioned to global reset mode, and is set to 0 when the CAN module has exited global reset mode. This flag remains 1 even when the CAN module has transitioned from global reset mode to global stop mode.

GHLTSTS Flag (Global Test Status Flag)

This flag is set to 1 when the CAN module has transitioned to global test mode, and is set to 0 when the CAN module has exited global test mode.

GSLPSTS Flag (Global Stop Status Flag)

This flag is set to 1 when the CAN module has transitioned to global stop mode, and is set to 0 when the CAN module has returned from global stop mode.

GRAMINIT Flag (CAN RAM Initialization Status Flag)

This flag indicates the initialization status of the CAN RAM.
This flag is set to 1 after the CAN module is enabled, and is set to 0 when CAN RAM initialization is completed.

28.2.14 Global Error Flag Register (GERFLL)

Address(es): RSCAN.GERFLL 000A 832Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	THLES	MES	DEF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DEF	DLC Error Flag	0: No DLC error is present. 1: A DLC error is present.	R/(W) *1
b1	MES	FIFO Message Lost Status Flag	0: No FIFO message lost error is present. 1: A FIFO message lost error is present.	R
b2	THLES	Transmit History Buffer Overflow Status Flag	0: No transmit history buffer overflow is present. 1: A transmit history buffer overflow is present.	R
b7 to b3	—	Reserved	The read value is undefined. The write value should be 0.	R/W

Note 1. The only effective value for writing to this flag is 0, which clears the flag. Otherwise writing to the flag results in retention of its state.

All flags in the GERFLL register are set to 0 in global reset mode.

DEF Flag (DLC Error Flag)

The DEF flag is set to 1 when an error has been detected during the DLC check. This flag can be set to 0 by writing 0 by the program.

MES Flag (FIFO Message Lost Status Flag)

The MES flag is set to 1 when any one of the RFSTSm.RFMLT flags or the CFSTS0.CFMLT flag is set to 1.
This flag is set to 0 when all RFSTSm.RFMLT flags and the CFSTS0.CFMLT flag are set to 0.

THLES Flag (Transmit History Buffer Overflow Status Flag)

The THLES flag is set to 1 when the THLSTS0.THLELT flag is set to 1.
This flag is set to 0 when the THLSTS0.THLELT flag is set to 0.

28.2.15 Global Transmit Interrupt Status Register (GTINTSTS)

Address(es): RSCAN.GTINTSTS 000A 8388h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	THIF0	CFTIF0	TAIF0	TSIF0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TSIF0	RSCAN0 Transmit Buffer Interrupt Status Flag	0: No transmit buffer transmit complete interrupt request is present. 1: A transmit buffer transmit complete interrupt request is present.	R
b1	TAIF0	RSCAN0 Transmit Buffer Abort Interrupt Status Flag	0: No transmit buffer abort interrupt request is present. 1: A transmit buffer abort interrupt request is present.	R
b2	CFTIF0	RSCAN0 Transmit/Receive FIFO Interrupt Status Flag	0: No transmit/receive FIFO transmit interrupt request is present. 1: A transmit/receive FIFO transmit interrupt request is present.	R
b3	THIF0	RSCAN0 Transmit History Interrupt Status Flag	0: No transmit history interrupt request is present. 1: A transmit history interrupt request is present.	R
b15 to b4	—	Reserved	These bits are read as 0.	R

All flags in the GTINTSTS register are set to 0 in global reset or channel reset mode.

TSIF0 Flag (RSCAN0 Transmit Buffer Interrupt Status Flag)

The TSIF0 flag is set to 1 when the TMIEC.TMIEp bit is set to 1 (enabling interrupts) and the corresponding TMSTSp.TMTRF[1:0] flags are set to 10b (transmission has been completed without transmit abort request) or 11b (transmission has been completed with transmit abort request).
This flag is set to 0 when all TMSTSp.TMTRF[1:0] flags that satisfy a condition for setting the TSIF0 flag to 1 are set to 00b. This flag is also set to 0 when the TMIEC.TMIEp bit is set to 0.

TAIF0 Flag (RSCAN0 Transmit Buffer Abort Interrupt Status Flag)

The TAIF0 flag is set to 1 when the CTRH.TAIE bit is set to 1 (enabling interrupts) and the TMSTSp.TMTRF[1:0] flags are set to 01b (transmit abort has been completed).
This flag is set to 0 when the TMSTSp.TMTRF[1:0] flags, which indicate that the abort of transmission has been completed, are set to 00b.

CFTIF0 Flag (RSCAN0 Transmit/Receive FIFO Interrupt Status Flag)

The CFTIF0 flag is set to 1 when the CFCCL0.CFTXIE bit is set to 1 (enabling interrupts) and the CFSTS0.CFTXIF flag is set to 1 (interrupt request present).
This flag is set to 0 when the CFSTS0.CFTXIF flag is set to 0. This flag is also set to 0 when the CFCCL0.CFTXIE bit is set to 0.

THIF0 Flag (RSCAN0 Transmit History Interrupt Status Flag)

The THIF0 flag is set to 1 when the THLCC0.THLIE bit is set to 1 (enabling interrupts) and the THLSTS0.THLIF flag is set to 1 (interrupt request present).
This flag is set to 0 when the THLSTS0.THLIF flag is set to 0. This flag is also set to 0 when the THLCC0.THLIE bit is set to 0.

28.2.16 Timestamp Register (GTSC)

Address(es): RSCAN.GTSC 000A 832Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TS[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description	Counter Value	R/W
b15 to b0	TS[15:0]	The timestamp counter value can be read.	0000h to FFFFh	R

When the TS[15:0] bits are read, the read value shows the timestamp counter (16-bit free-running counter) value at that time. The TS[15:0] value is captured when the SOF is detected and then stored in the receive buffer or the FIFO buffer.
The timestamp counter is initialized in global reset mode.
The timestamp counter start timing and stop timing depend on the count source.

- When the GCFGL.TSSS value is 0 (PCLK is selected):
  The timestamp counter starts counting when the CAN module has transitioned to global operating mode.
  This counter stops counting when the CAN module has transitioned to global stop mode or global test mode.
- When the GCFGL.TSSS value is 1 (CAN bit time clock is selected):
  The timestamp counter starts counting when the corresponding channel has transitioned to channel communication mode.
  This counter stops counting when the corresponding channel has transitioned to channel reset mode or channel halt mode.

28.2.17 Receive Rule Number Configuration Register (GAFLCFG)

Address(es): RSCAN.GAFLCFG 000A 8330h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	RNC0[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	RNC0[4:0]	RSCAN0 Receive Rule Number Set	Set the number of receive rules of channel 0. Set these bits to a value within a range of 00h to 10h.	R/W
b15 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Modify the GAFLCFG register only in global reset mode.
Up to 16 rules can be registered in the receive rule table.

RNC0[4:0] Bits (RSCAN0 Receive Rule Number Set)

These bits are used to set the number of rules to be registered in the channel 0 receive rule table.
Set these bits to a value within a range of 00h to 10h.

28.2.18 Receive Rule Entry Register jAL (GAFLIDLj) (j = 0 to 15)

Address(es): RSCAN.GAFLIDL0 000A 83A0h, RSCAN.GAFLIDL1 000A 83ACh, RSCAN.GAFLIDL2 000A 83B8h, RSCAN.GAFLIDL3 000A 83C4h, RSCAN.GAFLIDL4 000A 83D0h, RSCAN.GAFLIDL5 000A 83DCh, RSCAN.GAFLIDL6 000A 83E8h, RSCAN.GAFLIDL7 000A 83F4h, RSCAN.GAFLIDL8 000A 8400h, RSCAN.GAFLIDL9 000A 840Ch, RSCAN.GAFLIDL10 000A 8418h, RSCAN.GAFLIDL11 000A 8424h, RSCAN.GAFLIDL12 000A 8430h, RSCAN.GAFLIDL13 000A 843Ch, RSCAN.GAFLIDL14 000A 8448h, RSCAN.GAFLIDL15 000A 8454h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	GAFLID[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	GAFLID[15:0]	ID Set L	Set the ID of the receive rule. For the standard ID, set the ID in bits 10 to 0 and set bits 15 to 11 to 0.	R/W

Modify the GAFLIDLj register only when the GRWCR.RPAGE bit is set to 0 in global reset mode.

GAFLID[15:0] Bits (ID Set L)

These bits are used to set the ID field of the receive rule. The ID value set by these bits is compared with the ID in the received message during the acceptance filter processing.

28.2.19 Receive Rule Entry Register jAH (GAFLIDHj) (j = 0 to 15)

Address(es): RSCAN.GAFLIDH0 000A 83A2h, RSCAN.GAFLIDH1 000A 83AEh, RSCAN.GAFLIDH2 000A 83BAh, RSCAN.GAFLIDH3 000A 83C6h, RSCAN.GAFLIDH4 000A 83D2h, RSCAN.GAFLIDH5 000A 83DEh, RSCAN.GAFLIDH6 000A 83EAh, RSCAN.GAFLIDH7 000A 83F6h, RSCAN.GAFLIDH8 000A 8402h, RSCAN.GAFLIDH9 000A 840Eh, RSCAN.GAFLIDH10 000A 841Ah, RSCAN.GAFLIDH11 000A 8426h, RSCAN.GAFLIDH12 000A 8432h, RSCAN.GAFLIDH13 000A 843Eh, RSCAN.GAFLIDH14 000A 844Ah, RSCAN.GAFLIDH15 000A 8456h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	GAFLIDE	GAFLRTR	GAFLLB	GAFLID[28:16]												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b12 to b0	GAFLID[28:16]	ID Set H	Set the ID of the receive rule. For the standard ID, set these bits to 0.	R/W
b13	GAFLLB	Receive Rule Target Message Select	0: When a message transmitted from another CAN node is received 1: When a message transmitted from own node is received	R/W
b14	GAFLRTR	RTR Select	0: Data frame 1: Remote frame	R/W
b15	GAFLIDE	IDE Select	0: Standard ID 1: Extended ID	R/W

Modify the GAFLIDHj register only when the GRWCR.RPAGE bit is set to 0 in global reset mode.

GAFLID[28:16] Bits (ID Set H)

These bits are used to set the ID field of the receive rule. The ID value set by these bits is compared with the ID in the received message during the acceptance filter processing.

GAFLLB Bit (Receive Rule Target Message Select)

When this bit is set to 0, data processing using the receive rule is performed when receiving messages transmitted from another CAN node.

When this bit is set to 1 when the mirror function is used, data processing using the receive rule is performed when receiving messages transmitted from the own CAN node.

GAFLRTR Bit (RTR Select)

This bit is used to select the frame format (data frame or remote frame) of the receive rule. This bit is compared with the RTR bit in the received message during the acceptance filter processing.

GAFLIDE Bit (IDE Select)

This bit is used to select the ID format (standard ID or extended ID) of the receive rule. This bit is compared with the IDE bit in the received message during the acceptance filter processing.

28.2.20 Receive Rule Entry Register jBL (GAFLMLj) (j = 0 to 15)

Address(es): RSCAN.GAFLML0 000A 83A4h, RSCAN.GAFLML1 000A 83B0h, RSCAN.GAFLML2 000A 83BCh, RSCAN.GAFLML3 000A 83C8h, RSCAN.GAFLML4 000A 83D4h, RSCAN.GAFLML5 000A 83E0h, RSCAN.GAFLML6 000A 83ECh, RSCAN.GAFLML7 000A 83F8h, RSCAN.GAFLML8 000A 8404h, RSCAN.GAFLML9 000A 8410h, RSCAN.GAFLML10 000A 841Ch, RSCAN.GAFLML11 000A 8428h, RSCAN.GAFLML12 000A 8434h, RSCAN.GAFLML13 000A 8440h, RSCAN.GAFLML14 000A 844Ch, RSCAN.GAFLML15 000A 8458h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	GAFLIDM[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	GAFLIDM[15:0]	ID Mask L	0: The corresponding ID bit is not compared. 1: The corresponding ID bit is compared.	R/W

Modify the GAFLMLj register only when the GRWCR.RPAGE bit is set to 0 in global reset mode.

GAFLIDM[15:0] Bits (ID Mask L)

These bits are used to mask the corresponding ID bit of the receive rule.

28.2.21 Receive Rule Entry Register jBH (GAFLMHj) (j = 0 to 15)

Address(es): RSCAN.GAFLMH0 000A 83A6h, RSCAN.GAFLMH1 000A 83B2h, RSCAN.GAFLMH2 000A 83BEh, RSCAN.GAFLMH3 000A 83CAh, RSCAN.GAFLMH4 000A 83D6h, RSCAN.GAFLMH5 000A 83E2h, RSCAN.GAFLMH6 000A 83EEh, RSCAN.GAFLMH7 000A 83FAh, RSCAN.GAFLMH8 000A 8406h, RSCAN.GAFLMH9 000A 8412h, RSCAN.GAFLMH10 000A 841Eh, RSCAN.GAFLMH11 000A 842Ah, RSCAN.GAFLMH12 000A 8436h, RSCAN.GAFLMH13 000A 8442h, RSCAN.GAFLMH14 000A 844Eh, RSCAN.GAFLMH15 000A 845Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	GAFLIDEM	GAFLRTRM	—	GAFLIDM[28:16]												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b12 to b0	GAFLIDM[28:16]	ID Mask H	0: The corresponding ID bit is not compared. 1: The corresponding ID bit is compared.	R/W
b13	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b14	GAFLRTRM	RTR Mask	0: The RTR bit is not compared. 1: The RTR bit is compared	R/W
b15	GAFLIDEM	IDE Mask	0: The IDE bit is not compared. 1: The IDE bit is compared.	R/W

Modify the GAFLMHj register only when the GRWCR.RPAGE bit is set to 0 in global reset mode.

GAFLIDM[28:16] Bits (ID Mask H)

These bits are used to mask the corresponding ID bit of the receive rule.

GAFLRTRM Bit (RTR Mask)

This bit is used to mask the RTR bit of the receive rule.

GAFLIDEM Bit (IDE Mask)

When this bit is set to 1, filter processing is performed only for messages of the ID format specified by the GAFLIDHj.GAFLIDE bit.

When this bit is set to 0, it is regarded that all received messages have matched the specified ID format. To set the GAFLIDEM bit to 0, set the GAFLMHj.GAFLIDM[28:16] bits and the GAFLMLj.GAFLIDM[15:0] bits to all 0s.

28.2.22 Receive Rule Entry Register jCL (GAFLPLj) (j = 0 to 15)

Address(es): RSCAN.GAFLPL0 000A 83A8h, RSCAN.GAFLPL1 000A 83B4h, RSCAN.GAFLPL2 000A 83C0h, RSCAN.GAFLPL3 000A 83CCh, RSCAN.GAFLPL4 000A 83D8h, RSCAN.GAFLPL5 000A 83E4h, RSCAN.GAFLPL6 000A 83F0h, RSCAN.GAFLPL7 000A 83FCh, RSCAN.GAFLPL8 000A 8408h, RSCAN.GAFLPL9 000A 8414h, RSCAN.GAFLPL10 000A 8420h, RSCAN.GAFLPL11 000A 842Ch, RSCAN.GAFLPL12 000A 8438h, RSCAN.GAFLPL13 000A 8444h, RSCAN.GAFLPL14 000A 8450h, RSCAN.GAFLPL15 000A 845Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	GAFLRMV	GAFLRMDP[6:0]							—	—	—	GAFLFDP4	—	—	GAFLFDP1	GAFLFDP0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	GAFLFDP0	Receive FIFO Buffer Select 0	0: Not select a receive FIFO buffer 0 1: Select a receive FIFO buffer 0	R/W
b1	GAFLFDP1	Receive FIFO Buffer Select 1	0: Not select a receive FIFO buffer 1 1: Select a receive FIFO buffer 1	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	GAFLFDP4	RSCAN0 Transmit/Receive FIFO Buffer Select 0	0: Not select an RSCAN0 transmit/receive FIFO buffer 0 1: Select an RSCAN0 transmit/receive FIFO buffer 0	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b14 to b8	GAFLRMDP[6:0]	Receive Buffer Number Select	Set the receive buffer number to store receive messages.	R/W
b15	GAFLRMV	Receive Buffer Enable	0: No receive buffer is used. 1: A receive buffer is used.	R/W

Modify the GAFLPLj register only when the GRWCR.RPAGE bit is set to 0 in global reset mode.

GAFLFDP0 Bit (Receive FIFO Buffer Select 0),
GAFLFDP1 Bit (Receive FIFO Buffer Select 1),
GAFLFDP4 Bit (RSCAN0 Transmit/Receive FIFO Buffer Select 0)

These bits are used to specify FIFO buffers that store receive messages that have passed through the filter. Up to two FIFO buffers are selectable. However, when the GAFLPLj.GAFLRMV bit is set to 1 (a receive buffer is used), up to one FIFO buffer is selectable. Only receive FIFO buffers and the transmit/receive FIFO buffer for which the CFCCH0.CFM[1:0] bits are set to 00b (receive mode) are selectable.

GAFLRMDP[6:0] Bits (Receive Buffer Number Select)

These bits are used to select the number of the receive buffer that stores receive messages that have passed through the filter when the GAFLRMV bit is set to 1. Set these bits to a value smaller than the value set by the RMNB.NRXMB[4:0] bits.

GAFLRMV Bit (Receive Buffer Enable)

When this bit is set to 1, receive messages that have passed through the filter are stored in the receive buffer selected by the GAFLRMDP[6:0] bits.

28.2.23 Receive Rule Entry Register jCH (GAFLPHj) (j = 0 to 15)

Address(es): RSCAN.GAFLPH0 000A 83AAh, RSCAN.GAFLPH1 000A 83B6h, RSCAN.GAFLPH2 000A 83C2h, RSCAN.GAFLPH3 000A 83CEh, RSCAN.GAFLPH4 000A 83DAh, RSCAN.GAFLPH5 000A 83E6h, RSCAN.GAFLPH6 000A 83F2h, RSCAN.GAFLPH7 000A 83FEh, RSCAN.GAFLPH8 000A 840Ah, RSCAN.GAFLPH9 000A 8416h, RSCAN.GAFLPH10 000A 8422h, RSCAN.GAFLPH11 000A 842Eh, RSCAN.GAFLPH12 000A 843Ah, RSCAN.GAFLPH13 000A 8446h, RSCAN.GAFLPH14 000A 8452h, RSCAN.GAFLPH15 000A 845Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	GAFLDLC[3:0]				GAFLPTR[11:0]											
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b11 to b0	GAFLPTR[11:0]	Receive Rule Label	Set the 12-bit label information.	R/W
b15 to b12	GAFLDLC[3:0]	Receive Rule DLC	b15 b12 0 0 0 0: 0 or more data bytes (DLC check is disabled) 0 0 0 1: 1 or more data bytes 0 0 1 0: 2 or more data bytes 0 0 1 1: 3 or more data bytes 0 1 0 0: 4 or more data bytes 0 1 0 1: 5 or more data bytes 0 1 1 0: 6 or more data bytes 0 1 1 1: 7 or more data bytes 1 x x x: 8 or more data bytes	R/W

x: Don’t care

Modify the GAFLPHj register only when the GRWCR.RPAGE bit is set to 0 in global reset mode.

GAFLPTR[11:0] Bits (Receive Rule Label)

These bits are used to set a 12-bit label to be attached to messages that have passed through the filter. A label is attached when a message is stored in the receive buffer or the FIFO buffer.

GAFLDLC[3:0] Bits (Receive Rule DLC)

These bits are used to set the minimum data length necessary for receiving messages. If the data length of a message that is being filtered is equal to or larger than the value set by the GAFLDLC[3:0] bits, the message passes the DLC check. Setting these bits to 0000b disables the DLC check function allowing messages with any data length to pass the DLC check.

28.2.24 Receive Buffer Number Configuration Register (RMNB)

Address(es): RSCAN.RMNB 000A 8332h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	NRXMB[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	NRXMB[4:0]	Receive Buffer Number Configuration	Set the number of receive buffers. Set a value of 0 to 16.	R/W
b15 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Modify the RMNB register only in global reset mode.

NRXMB[4:0] Bits (Receive Buffer Number Configuration)

These bits are used to set the total number of receive buffers of the CAN module. The maximum value is 16.
Setting these bits to all 0s makes receive buffers unavailable.

28.2.25 Receive Buffer Receive Complete Flag Register (RMND0)

Address(es): RSCAN.RMND0 000A 8334h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RMNS[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	RMNS[15:0]	Receive Buffer Receive Complete Flag n	0: Receive buffer n contains no new message (n = 0 to 15). 1: Receive buffer n contains a new message.	R/W

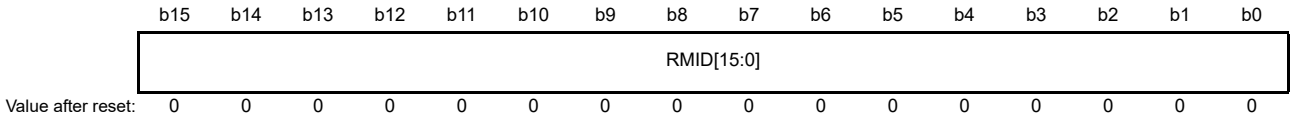
Write 0 to the RMND0 register in global operating mode or global test mode.

RMNS[15:0] Flags (Receive Buffer Receive Complete Flag n)

Each of the RMNS[15:0] flags is set to 1 when the processing for storing a message in the corresponding receive buffer starts.
To set these flags to 0, write 0 to the corresponding flag by the program. In this case, write this register in 16-bit unit to ensure that only the specified bit is set to 0 and the other bits are set to 1. These bits cannot be set to 0 while a message is being stored. It takes time of 10 clock cycles of PCLK for storing a message.
These flags are set to 0 in global reset mode.

28.2.26 Receive Buffer Register nAL (RMIDLn) (n = 0 to 15)

Address(es): RSCAN.RMIDL0 000A 83A0h, RSCAN.RMIDL1 000A 83B0h, RSCAN.RMIDL2 000A 83C0h, RSCAN.RMIDL3 000A 83D0h, RSCAN.RMIDL4 000A 83E0h, RSCAN.RMIDL5 000A 83F0h, RSCAN.RMIDL6 000A 8400h, RSCAN.RMIDL7 000A 8410h, RSCAN.RMIDL8 000A 8420h, RSCAN.RMIDL9 000A 8430h, RSCAN.RMIDL10 000A 8440h, RSCAN.RMIDL11 000A 8450h, RSCAN.RMIDL12 000A 8460h, RSCAN.RMIDL13 000A 8470h, RSCAN.RMIDL14 000A 8480h, RSCAN.RMIDL15 000A 8490h



Bit	Symbol	Bit Name	Description	R/W
b15 to b0	RMID[15:0]	Receive Buffer ID Data L	The standard ID or extended ID of received message can be read. Read bits 10 to 0 for standard ID. Bits 15 to 11 are read as 0.	R

This register can be read when the GRWCR.RPAGE bit is 1.

RMID[15:0] Bits (Receive Buffer ID Data L)

These bits indicate the ID of the message stored in the receive buffer.

28.2.27 Receive Buffer Register nAH (RMIDHn) (n = 0 to 15)

Address(es): RSCAN.RMIDH0 000A 83A2h, RSCAN.RMIDH1 000A 83B2h, RSCAN.RMIDH2 000A 83C2h, RSCAN.RMIDH3 000A 83D2h, RSCAN.RMIDH4 000A 83E2h, RSCAN.RMIDH5 000A 83F2h, RSCAN.RMIDH6 000A 8402h, RSCAN.RMIDH7 000A 8412h, RSCAN.RMIDH8 000A 8422h, RSCAN.RMIDH9 000A 8432h, RSCAN.RMIDH10 000A 8442h, RSCAN.RMIDH11 000A 8452h, RSCAN.RMIDH12 000A 8462h, RSCAN.RMIDH13 000A 8472h, RSCAN.RMIDH14 000A 8482h, RSCAN.RMIDH15 000A 8492h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RMIDE	RMRTR	—	RMID[28:16]												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b12 to b0	RMID[28:16]	Receive Buffer ID Data H	The standard ID or extended ID of received message can be read. For standard ID, these bits are read as 0.	R
b13	—	Reserved	This bit is read as 0.	R
b14	RMRTR	Receive Buffer RTR	0: Data frame 1: Remote frame	R
b15	RMIDE	Receive Buffer IDE	0: Standard ID 1: Extended ID	R

This register can be read when the GRWCR.RPAGE bit is 1.

RMID[28:16] Bits (Receive Buffer ID Data H)

These bits indicate the ID of the message stored in the receive buffer.

RMRTR Bit (Receive Buffer RTR)

This bit indicates the frame format (data frame or remote frame) of the message stored in the receive buffer.

RMIDE Bit (Receive Buffer IDE)

This bit indicates the ID format (standard ID or extended ID) of the message stored in the receive buffer.

28.2.28 Receive Buffer Register nBL (RMTSn) (n = 0 to 15)

Address(es): RSCAN.RMTS0 000A 83A4h, RSCAN.RMTS1 000A 83B4h, RSCAN.RMTS2 000A 83C4h, RSCAN.RMTS3 000A 83D4h, RSCAN.RMTS4 000A 83E4h, RSCAN.RMTS5 000A 83F4h, RSCAN.RMTS6 000A 8404h, RSCAN.RMTS7 000A 8414h, RSCAN.RMTS8 000A 8424h, RSCAN.RMTS9 000A 8434h, RSCAN.RMTS10 000A 8444h, RSCAN.RMTS11 000A 8454h, RSCAN.RMTS12 000A 8464h, RSCAN.RMTS13 000A 8474h, RSCAN.RMTS14 000A 8484h, RSCAN.RMTS15 000A 8494h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RMTS[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	RMTS[15:0]	Receive Buffer Timestamp Data	Timestamp value of the received message can be read.	R

This register can be read when the GRWCR.RPAGE bit is 1.

RMTS[15:0] Bits (Receive Buffer Timestamp Data)

These bits indicate the timestamp value of the message stored in the receive buffer.

28.2.29 Receive Buffer Register nBH (RMPTRn) (n = 0 to 15)

Address(es): RSCAN.RMPTR0 000A 83A6h, RSCAN.RMPTR1 000A 83B6h, RSCAN.RMPTR2 000A 83C6h, RSCAN.RMPTR3 000A 83D6h, RSCAN.RMPTR4 000A 83E6h, RSCAN.RMPTR5 000A 83F6h, RSCAN.RMPTR6 000A 8406h, RSCAN.RMPTR7 000A 8416h, RSCAN.RMPTR8 000A 8426h, RSCAN.RMPTR9 000A 8436h, RSCAN.RMPTR10 000A 8446h, RSCAN.RMPTR11 000A 8456h, RSCAN.RMPTR12 000A 8466h, RSCAN.RMPTR13 000A 8476h, RSCAN.RMPTR14 000A 8486h, RSCAN.RMPTR15 000A 8496h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RMDLC[3:0]				RMPTR[11:0]											
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b11 to b0	RMPTR[11:0]	Receive Buffer Label Data	Label information of the received message can be read.	R
b15 to b12	RMDLC[3:0]	Receive Buffer DLC Data	b15 b12 0 0 0 0: 0 data bytes 0 0 0 1: 1 data byte 0 0 1 0: 2 data bytes 0 0 1 1: 3 data bytes 0 1 0 0: 4 data bytes 0 1 0 1: 5 data bytes 0 1 1 0: 6 data bytes 0 1 1 1: 7 data bytes 1 x x x: 8 data bytes	R

x: Don’t care

This register can be read when the GRWCR.RPAGE bit is 1.

RMPTR[11:0] Bits (Receive Buffer Label Data)

These bits indicate the label information of the message stored in the receive buffer.

RMDLC[3:0] Bits (Receive Buffer DLC Data)

These bits indicate the data length of the message stored in the receive buffer.

28.2.30 Receive Buffer Register nCL (RMDF0n) (n = 0 to 15)

Address(es): RSCAN.RMDF00 000A 83A8h, RSCAN.RMDF01 000A 83B8h, RSCAN.RMDF02 000A 83C8h, RSCAN.RMDF03 000A 83D8h, RSCAN.RMDF04 000A 83E8h, RSCAN.RMDF05 000A 83F8h, RSCAN.RMDF06 000A 8408h, RSCAN.RMDF07 000A 8418h, RSCAN.RMDF08 000A 8428h, RSCAN.RMDF09 000A 8438h, RSCAN.RMDF010 000A 8448h, RSCAN.RMDF011 000A 8458h, RSCAN.RMDF012 000A 8468h, RSCAN.RMDF013 000A 8478h, RSCAN.RMDF014 000A 8488h, RSCAN.RMDF015 000A 8498h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RMDB1[7:0]								RMDB0[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	RMDB0[7:0]	Receive Buffer Data Byte 0	Data in the message stored in the receive buffer can be read.	R
b15 to b8	RMDB1[7:0]	Receive Buffer Data Byte 1		R

When the RMPTRn.RMDLC[3:0] value is smaller than 1000b, data bytes for which no data is set are read as 00h.
This register can be read when the GRWCR.RPAGE bit is 1.

28.2.31 Receive Buffer Register nCH (RMDF1n) (n = 0 to 15)

Address(es): RSCAN.RMDF10 000A 83AAh, RSCAN.RMDF11 000A 83BAh, RSCAN.RMDF12 000A 83CAh, RSCAN.RMDF13 000A 83DAh, RSCAN.RMDF14 000A 83EAh, RSCAN.RMDF15 000A 83FAh, RSCAN.RMDF16 000A 840Ah, RSCAN.RMDF17 000A 841Ah, RSCAN.RMDF18 000A 842Ah, RSCAN.RMDF19 000A 843Ah, RSCAN.RMDF110 000A 844Ah, RSCAN.RMDF111 000A 845Ah, RSCAN.RMDF112 000A 846Ah, RSCAN.RMDF113 000A 847Ah, RSCAN.RMDF114 000A 848Ah, RSCAN.RMDF115 000A 849Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RMDB3[7:0]								RMDB2[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	RMDB2[7:0]	Receive Buffer Data Byte 2	Data in the message stored in the receive buffer can be read.	R
b15 to b8	RMDB3[7:0]	Receive Buffer Data Byte 3		R

When the RMPTRn.RMDLC[3:0] value is smaller than 1000b, data bytes for which no data is set are read as 00h.
This register can be read when the GRWCR.RPAGE bit is 1.

28.2.32 Receive Buffer Register nDL (RMDF2n) (n = 0 to 15)

Address(es): RSCAN.RMDF20 000A 83ACh, RSCAN.RMDF21 000A 83BCh, RSCAN.RMDF22 000A 83CCh, RSCAN.RMDF23 000A 83DCh, RSCAN.RMDF24 000A 83ECh, RSCAN.RMDF25 000A 83FCh, RSCAN.RMDF26 000A 840Ch, RSCAN.RMDF27 000A 841Ch, RSCAN.RMDF28 000A 842Ch, RSCAN.RMDF29 000A 843Ch, RSCAN.RMDF210 000A 844Ch, RSCAN.RMDF211 000A 845Ch, RSCAN.RMDF212 000A 846Ch, RSCAN.RMDF213 000A 847Ch, RSCAN.RMDF214 000A 848Ch, RSCAN.RMDF215 000A 849Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RMDB5[7:0]								RMDB4[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	RMDB4[7:0]	Receive Buffer Data Byte 4	Data in the message stored in the receive buffer can be read.	R
b15 to b8	RMDB5[7:0]	Receive Buffer Data Byte 5		R

When the RMPTRn.RMDLC[3:0] value is smaller than 1000b, data bytes for which no data is set are read as 00h.
This register can be read when the GRWCR.RPAGE bit is 1.

28.2.33 Receive Buffer Register nDH (RMDF3n) (n = 0 to 15)

Address(es): RSCAN.RMDF30 000A 83AEh, RSCAN.RMDF31 000A 83BEh, RSCAN.RMDF32 000A 83CEh, RSCAN.RMDF33 000A 83DEh, RSCAN.RMDF34 000A 83EEh, RSCAN.RMDF35 000A 83FEh, RSCAN.RMDF36 000A 840Eh, RSCAN.RMDF37 000A 841Eh, RSCAN.RMDF38 000A 842Eh, RSCAN.RMDF39 000A 843Eh, RSCAN.RMDF310 000A 844Eh, RSCAN.RMDF311 000A 845Eh, RSCAN.RMDF312 000A 846Eh, RSCAN.RMDF313 000A 847Eh, RSCAN.RMDF314 000A 848Eh, RSCAN.RMDF315 000A 849Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RMDB7[7:0]								RMDB6[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	RMDB6[7:0]	Receive Buffer Data Byte 6	Data in the message stored in the receive buffer can be read.	R
b15 to b8	RMDB7[7:0]	Receive Buffer Data Byte 7		R

When the RMPTRn.RMDLC[3:0] value is smaller than 1000b, data bytes for which no data is set are read as 00h.
This register can be read when the GRWCR.RPAGE bit is 1.

28.2.34 Receive FIFO Control Register m (RFCCm) (m = 0, 1)

Address(es): RSCAN.RFCC0 000A 8338h, RSCAN.RFCC1 000A 833Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RFIGCV[2:0]			RFIM	—	RFDC[2:0]			—	—	—	—	—	—	RFIE	RFE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	RFE	Receive FIFO Buffer Enable	0: No receive FIFO buffer is used. 1: Receive FIFO buffers are used.	R/W
b1	RFIE	Receive FIFO Interrupt Enable	0: Receive FIFO interrupt is disabled. 1: Receive FIFO interrupt is enabled.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b10 to b8	RFDC[2:0]	Receive FIFO Buffer Depth Configuration	b10 b8 0 0 0: 0 messages 0 0 1: 4 messages 0 1 0: 8 messages 0 1 1: 16 messages 1 0 0: Setting prohibited 1 0 1: Setting prohibited 1 1 0: Setting prohibited 1 1 1: Setting prohibited	R/W
b11	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b12	RFIM	Receive FIFO Interrupt Source Select	0: An interrupt occurs when the condition set by the RFIGCV[2:0] bits is met. 1: An interrupt occurs each time a message has been received.	R/W
b15 to b13	RFIGCV[2:0]	Receive FIFO Interrupt Request Timing Select	b15 b13 0 0 0: When FIFO is 1/8 full. 0 0 1: When FIFO is 2/8 full. 0 1 0: When FIFO is 3/8 full. 0 1 1: When FIFO is 4/8 full. 1 0 0: When FIFO is 5/8 full. 1 0 1: When FIFO is 6/8 full. 1 1 0: When FIFO is 7/8 full. 1 1 1: When FIFO is full.	R/W

RFE Bit (Receive FIFO Buffer Enable)

Setting the RFE bit to 1 makes receive FIFO buffers available. Setting this bit to 0 sets the RFSTSm.RFEMP flag to 1 (the receive FIFO buffer contains no unread message (buffer empty)). Modify this bit only in global operating mode or global test mode.

RFIE Bit (Receive FIFO Interrupt Enable)

Setting the RFIE bit to 1 enables receive FIFO interrupts. Modify this bit when the RFE bit is set to 0 (no receive FIFO buffer is used).

RFDC[2:0] Bits (Receive FIFO Buffer Depth Configuration)

These bits are used to select the number of messages that can be stored in a single receive FIFO buffer. If these bits are set to 000b, do not use any receive FIFO buffer. Modify these bits only in global reset mode.

RFIM Bit (Receive FIFO Interrupt Source Select)

This bit is used to select a FIFO interrupt source. Modify this bit only in global reset mode.

RFIGCV[2:0] Bits (Receive FIFO Interrupt Request Timing Select)

These bits are used to specify the fraction of the transmit/receive FIFO buffer (the number of messages is selected by the setting of the RFDC[2:0] bits) that must be filled for the FIFO buffer to generate a receive interrupt request when the RFIM bit is set to 0.

When the RFDC[2:0] bits are set to 001b (4 messages), set the RFIGCV[2:0] bits to 001b, 011b, 101b, or 111b. Modify these bits only in global reset mode.

28.2.35 Receive FIFO Status Register m (RFSTSm) (m = 0, 1)

Address(es): RSCAN.RFSTS0 000A 8340h, RSCAN.RFSTS1 000A 8342h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	RFMC[5:0]						—	—	—	—	RFIF	RFMLT	RFFLL	RFEMP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	RFEMP	Receive FIFO Buffer Empty Status Flag	0: The receive FIFO buffer contains unread messages. 1: The receive FIFO buffer contains no unread message (buffer empty).	R
b1	RFFLL	Receive FIFO Buffer Full Status Flag	0: The receive FIFO buffer is not full. 1: The receive FIFO buffer is full.	R
b2	RFMLT	Receive FIFO Message Lost Flag	0: No receive FIFO message is lost. 1: A receive FIFO message is lost.	R/(W) *1
b3	RFIF	Receive FIFO Interrupt Request Flag	0: No receive FIFO interrupt request is present. 1: A receive FIFO interrupt request is present.	R/(W) *1
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13 to b8	RFMC[5:0]	Receive FIFO Unread Message Counter	The number of unread messages stored in the receive FIFO buffer is displayed.	R
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The only effective value for writing to this flag is 0, which clears the flag. Otherwise writing to the flag results in retention of its state.

RFEMP Flag (Receive FIFO Buffer Empty Status Flag)

This flag is set to 1 when all messages in the receive FIFO buffer have been read. This flag is also set to 1 when the RFCCm.RFE bit is 0 or in global reset mode.

This flag is set to 0 when even a single received message has been stored in the receive FIFO buffer.

RFFLL Flag (Receive FIFO Buffer Full Status Flag)

This flag is set to 1 when the number of messages stored in the receive FIFO buffer matches the FIFO buffer depth set by the RFCCm.RFDC[2:0] bits.

If the number of messages stored in the receive FIFO buffer becomes smaller than the FIFO buffer depth set by the RFCCm.RFDC[2:0] bits, this flag is set to 0. This flag is also set to 0 when the RFCCm.RFE bit is set to 0 (no receive FIFO buffer is used) or in global reset mode.

RFMLT Flag (Receive FIFO Message Lost Flag)

This flag is set to 1 when it is attempted to store a new message while the receive FIFO buffer is full. In this case, the new message is discarded.

This flag is set to 0 in global reset mode or by writing 0 to this flag.

Modify this bit only in global operating mode or global test mode.

RFIF Flag (Receive FIFO Interrupt Request Flag)

This flag is set to 1 when the receive FIFO interrupt request generation conditions set by the RFCCm.RFIGCV[2:0] bits (m = 0, 1) and the RFCCm.RFIM bit are met. This flag is set to 0 in global reset mode or by writing 0 to this flag. Modify this bit only in global operating mode or global test mode.

RFMC[5:0] Flags (Receive FIFO Unread Message Counter)

These flags indicate the number of unread messages in the receive FIFO buffer. This flag becomes 00h when the RFCCm.RFE bit is set to 0.

28.2.36 Receive FIFO Pointer Control Register m (RFPCTRm) (m = 0, 1)

Address(es): RSCAN.RFPCTR0 000A 8348h, RSCAN.RFPCTR1 000A 834Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	RFPC[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	RFPC[7:0]	Receive FIFO Pointer	When these bits are set to FFh, the read pointer moves to the next unread message in the receive FIFO buffer. The setting for these bits must be FFh.	W
b15 to b8	—	Reserved	The write value should be 0.	W

RFPC[7:0] Bits (Receive FIFO Pointer)

When the RFPC[7:0] bits are set to FFh, the read pointer moves to the next unread message in the receive FIFO buffer. At this time, the RFSTSm.RFMC[5:0] (receive FIFO unread message counter) value is decremented. Read the RFIDLm, RFIDHm, RFTSm, RFPTRm, and RFDF0m to RFDF3m registers to read messages in the receive FIFO buffer, and then write FFh to the RFPC[7:0] bits.

Write FFh to these bits when the RFCCm.RFE bit is set to 1 (receive FIFO buffers are used) and the RFSTSm.RFEMP flag is 0 (the receive FIFO buffer contains unread messages).

28.2.37 Receive FIFO Access Register mAL (RFIDLm) (m = 0, 1)

Address(es): RSCAN.RFIDL0 000A 85A0h, RSCAN.RFIDL1 000A 85B0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RFID[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	RFID[15:0]	Receive FIFO Buffer ID Data L	The standard ID or extended ID of received message can be read. Read bits 10 to 0 for standard ID. Bits 15 to 11 are read as 0.	R

This register can be read when the GRWCR.RPAGE bit is 1.

RFID[15:0] Bits (Receive FIFO Buffer ID Data L)

These bits indicate the ID of the message stored in the receive FIFO buffer.

28.2.38 Receive FIFO Access Register mAH (RFIDHm) (m = 0, 1)

Address(es): RSCAN.RFIDH0 000A 85A2h, RSCAN.RFIDH1 000A 85B2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RFIDE	RFRTR	—	RFID[28:16]												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b12 to b0	RFID[28:16]	Receive FIFO Buffer ID Data H	The standard ID or extended ID of received message can be read. For standard ID, these bits are read as 0.	R
b13	—	Reserved	This bit is read as 0.	R
b14	RFRTR	Receive FIFO Buffer RTR	0: Data frame 1: Remote frame	R
b15	RFIDE	Receive FIFO Buffer IDE	0: Standard ID 1: Extended ID	R

This register can be read when the GRWCR.RPAGE bit is 1.

RFID[28:16] Bits (Receive FIFO Buffer ID Data H)

These bits indicate the ID of the message stored in the receive FIFO buffer.

RFRTR Bit (Receive FIFO Buffer RTR)

This bit indicates the frame format (data frame or remote frame) of the message stored in the receive FIFO buffer.

RFIDE Bit (Receive FIFO Buffer IDE)

This bit indicates the ID format (standard ID or extended ID) of the message stored in the receive FIFO buffer.

28.2.39 Receive FIFO Access Register mBL (RFTSm) (m = 0, 1)

Address(es): RSCAN.RFTS0 000A 85A4h, RSCAN.RFTS1 000A 85B4h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RFTS[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	RFTS[15:0]	Receive FIFO Buffer Timestamp Data	Timestamp value of the received message can be read.	R

This register can be read when the GRWCR.RPAGE bit is 1.

RFTS[15:0] Bits (Receive FIFO Buffer Timestamp Data)

These bits indicate the timestamp value of the message stored in the receive FIFO buffer.

28.2.40 Receive FIFO Access Register mBH (RFPTRm) (m = 0, 1)

Address(es): RSCAN.RFPTR0 000A 85A6h, RSCAN.RFPTR1 000A 85B6h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RFDLC[3:0]				RFPTR[11:0]											
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b11 to b0	RFPTR[11:0]	Receive FIFO Buffer Label Data	Label information of the received message can be read.	R
b15 to b12	RFDLC[3:0]	Receive FIFO Buffer DLC Data	b15 b12 0 0 0 0: 0 data bytes 0 0 0 1: 1 data byte 0 0 1 0: 2 data bytes 0 0 1 1: 3 data bytes 0 1 0 0: 4 data bytes 0 1 0 1: 5 data bytes 0 1 1 0: 6 data bytes 0 1 1 1: 7 data bytes 1 x x x: 8 data bytes	R

x: Don't care

This register can be read when the GRWCR.RPAGE bit is 1.

RFPTR[11:0] Bits (Receive FIFO Buffer Label Data)

These bits indicate the label information of the message stored in the receive FIFO buffer.

RFDLC[3:0] Bits (Receive FIFO Buffer DLC Data)

These bits indicate the data length of the message stored in the receive FIFO buffer.

28.2.41 Receive FIFO Access Register mCL (RFDF0m) (m = 0, 1)

Address(es): RSCAN.RFDF00 000A 85A8h, RSCAN.RFDF01 000A 85B8h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RFDB1[7:0]								RFDB0[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	RFDB0[7:0]	Receive FIFO Buffer Data Byte 0	Data in the message stored in the receive FIFO buffer can be read.	R
b15 to b8	RFDB1[7:0]	Receive FIFO Buffer Data Byte 1		R

When the RFPTRm.RFDLC[3:0] value is smaller than 1000b, data bytes for which no data is set are read as 00h.
This register can be read when the GRWCR.RPAGE bit is 1.

28.2.42 Receive FIFO Access Register mCH (RFDF1m) (m = 0, 1)

Address(es): RSCAN.RFDF10 000A 85AAh, RSCAN.RFDF11 000A 85BAh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RFDB3[7:0]								RFDB2[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	RFDB2[7:0]	Receive FIFO Buffer Data Byte 2	Data in the message stored in the receive FIFO buffer can be read.	R
b15 to b8	RFDB3[7:0]	Receive FIFO Buffer Data Byte 3		R

When the RFPTRm.RFDLC[3:0] value is smaller than 1000b, data bytes for which no data is set are read as 00h.
This register can be read when the GRWCR.RPAGE bit is 1.

28.2.43 Receive FIFO Access Register mDL (RFDF2m) (m = 0, 1)

Address(es): RSCAN.RFDF20 000A 85ACh, RSCAN.RFDF21 000A 85BCh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RFDB5[7:0]								RFDB4[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	RFDB4[7:0]	Receive FIFO Buffer Data Byte 4	Data in the message stored in the receive FIFO buffer can be read.	R
b15 to b8	RFDB5[7:0]	Receive FIFO Buffer Data Byte 5		R

When the RFPTRm.RFDLC[3:0] value is smaller than 1000b, data bytes for which no data is set are read as 00h.
This register can be read when the GRWCR.RPAGE bit is 1.

28.2.44 Receive FIFO Access Register mDH (RFDF3m) (m = 0, 1)

Address(es): RSCAN.RFDF30 000A 85AEh, RSCAN.RFDF31 000A 85BEh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RFDB7[7:0]								RFDB6[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	RFDB6[7:0]	Receive FIFO Buffer Data Byte 6	Data in the message stored in the receive FIFO buffer can be read.	R
b15 to b8	RFDB7[7:0]	Receive FIFO Buffer Data Byte 7		R

When the RFPTRm.RFDLC[3:0] value is smaller than 1000b, data bytes for which no data is set are read as 00h.
This register can be read when the GRWCR.RPAGE bit is 1.

28.2.45 Transmit/Receive FIFO Control Register 0L (CFCCL0)

Address(es): RSCAN0.CFCCL0 000A 8350h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CFIGCV[2:0]			CFIM	—	CFDC[2:0]			—	—	—	—	—	CFTXIE	CFRXIE	CFE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CFE	Transmit/Receive FIFO Buffer Enable	0: No transmit/receive FIFO buffer is used. 1: Transmit/receive FIFO buffers are used.	R/W
b1	CFRXIE	Transmit/Receive FIFO Receive Interrupt Enable	0: Transmit/receive FIFO receive interrupt is disabled. 1: Transmit/receive FIFO receive interrupt is enabled.	R/W
b2	CFTXIE	Transmit/Receive FIFO Transmit Interrupt Enable	0: Transmit/receive FIFO transmit interrupt is disabled. 1: Transmit/receive FIFO transmit interrupt is enabled.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b10 to b8	CFDC[2:0]	Transmit/Receive FIFO Buffer Depth Configuration	b10 b8 0 0 0: 0 messages 0 0 1: 4 messages 0 1 0: 8 messages 0 1 1: 16 messages 1 0 0: Setting prohibited 1 0 1: Setting prohibited 1 1 0: Setting prohibited 1 1 1: Setting prohibited	R/W
b11	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b12	CFIM	Transmit/Receive FIFO Interrupt Source Select	0: • Receive mode When the number of received messages has met the condition set by the CFIGCV[2:0] bits, a FIFO receive interrupt request is generated. • Transmit mode When the buffer becomes empty upon completion of message transmission, a FIFO transmit interrupt request is generated. 1: • Receive mode A FIFO receive interrupt request is generated each time a message has been received. • Transmit mode A FIFO transmit interrupt request is generated each time a message has been transmitted.	R/W
b15 to b13	CFIGCV[2:0]	Transmit/Receive FIFO Receive Interrupt Request Timing Select	b15 b13 0 0 0: When FIFO is 1/8 full. 0 0 1: When FIFO is 2/8 full. 0 1 0: When FIFO is 3/8 full. 0 1 1: When FIFO is 4/8 full. 1 0 0: When FIFO is 5/8 full. 1 0 1: When FIFO is 6/8 full. 1 1 0: When FIFO is 7/8 full. 1 1 1: When FIFO is full.	R/W

CFE Bit (Transmit/Receive FIFO Buffer Enable)

Setting this bit to 1 makes transmit/receive FIFO buffers available.

When this bit is set to 0 in transmit mode, if a message in the transmit/receive FIFO buffer is being transmitted or to be transmitted next, the transmit/receive FIFO buffer becomes empty after completion of transmission, CAN bus error detection, or arbitration lost. In other cases or in receive mode, the transmit/receive FIFO buffer becomes empty immediately.

This bit is set to 0 when the following conditions are met.

- Receive mode: Global reset mode
- Transmit mode: Channel reset mode

Modify this bit only in the following mode.

- Receive mode: Global operating mode or global test mode
- Transmit mode: Channel communication mode or channel halt mode

CFRXIE Bit (Transmit/Receive FIFO Receive Interrupt Enable)

When this bit is set to 1 and the CFSTS0.CFRXIF flag is set to 1, a transmit/receive FIFO receive interrupt request is generated.
Modify this bit with the CFE bit set to 0.

CFTXIE Bit (Transmit/Receive FIFO Transmit Interrupt Enable)

When this bit is set to 1 and the CFSTS0.CFTXIF flag is set to 1, a transmit/receive FIFO transmit interrupt request is generated.
Modify this bit with the CFE bit set to 0 (no transmit/receive FIFO buffer is used).

CFDC[2:0] Bits (Transmit/Receive FIFO Buffer Depth Configuration)

These bits are used to set the number of messages that can be stored in a single transmit/receive FIFO buffer.
If these bits are set to 000b, do not use any receive FIFO buffer. Modify these bits only in global reset mode.

CFIM Bit (Transmit/Receive FIFO Interrupt Source Select)

This bit is used to select a transmit/receive FIFO interrupt source. Modify this bit only in global reset mode.

CFIGCV[2:0] Bits (Transmit/Receive FIFO Receive Interrupt Request Timing Select)

These bits are used to specify the fraction of the transmit/receive FIFO buffer (the number of messages is selected by the setting of the CFDC[2:0] bits) that must be filled for the FIFO buffer to generate a receive interrupt request when the CFCCH0.CFM[1:0] bits are set to 00b (receive mode) and the CFIM bit is set to 0.
When the CFDC[2:0] bits are set to 001b (4 messages), set the CFIGCV[2:0] bits to 001b, 011b, 101b, or 111b.
Modify these bits only in global reset mode.

28.2.46 Transmit/Receive FIFO Control Register 0H (CFCCH0)

Address(es): RSCAN0.CFCCH0 000A 8352h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CFITT[7:0]								—	—	CFTML[1:0]		CFITR	CFITSS	CFM[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	CFM[1:0]	Transmit/Receive FIFO Mode Select	b1 b0 0 0: Receive mode 0 1: Transmit mode 1 0: Setting prohibited 1 1: Setting prohibited	R/W
b2	CFITSS	Interval Timer Clock Source Select	0: Clock selected by the CFITR bit 1: CAN bit time clock	R/W
b3	CFITR	Transmit/Receive FIFO Interval Timer Resolution	0: Clock obtained by frequency-dividing PCLK by the ITRCP[15:0] value 1: Clock obtained by frequency-dividing PCLK by the ITRCP[15:0] value × 10	R/W
b5, b4	CFTML[1:0]	Transmit Buffer Link Configuration	Set the transmit buffer number to be linked to the transmit/receive FIFO buffer.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	CFITT[7:0]	Message Transmission Interval Configuration	Set a message transmission interval. Set these bits to a value within a range of 00h to FFh.	R/W

CFM[1:0] Bits (Transmit/Receive FIFO Mode Select)

These bits are used to select transmit/receive FIFO mode. Modify these bits only in global reset mode.

CFITSS Bit (Interval Timer Clock Source Select)

Setting this bit to 0 selects the clock selected by the CFITR bit as the clock source for counting by the interval timer.
Setting this bit to 1 selects the CAN bit time clock as the clock source for counting by the interval timer. Set the CFCCL0.CFE bit to 0 (no transmit/receive FIFO buffer is used) before modifying the CFITSS bit.

CFITR Bit (Transmit/Receive FIFO Interval Timer Resolution)

This bit is valid when the setting of the CFITSS bit is 1.
Setting this bit to 0 selects the clock obtained by frequency-dividing PCLK by the GCFGH.ITRCP[15:0] value.
Setting this bit to 1 selects the clock obtained by frequency-dividing PCLK by the GCFGH.ITRCP[15:0] value × 10.
Modifying this bit with the CFCCL0.CFE bit set to 0 (no transmit/receive FIFO buffer is used).

CFTML[1:0] Bits (Transmit Buffer Link Configuration)

These bits are used to set the number of transmit buffer to be linked to the transmit/receive FIFO buffer when the CFM[1:0] bits are set to 01b (transmit mode).
Setting the CFCCL0.CFDC[2:0] bits to 001b or more enables the setting of the CFTML[1:0] bits.
Modify these bits only in global reset mode.

CFITT[7:0] Bits (Message Transmission Interval Configuration)

These bits are used to set a message transmission interval when transmitting messages continuously from a transmit/receive FIFO buffer whose CFM[1:0] bits are set to 01b (transmit mode).
Set the CFCCL0.CFE bit to 0 (no transmit/receive FIFO buffer is used) and then modify the CFITT[7:0] bits.

28.2.47 Transmit/Receive FIFO Status Register 0 (CFSTS0)

Address(es): RSCAN0.CFSTS0 000A 8358h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CFMC[5:0]						—	—	—	CFTXIF	CFRXIF	CFMLT	CFFLL	CFEMP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	CFEMP	Transmit/Receive FIFO Buffer Empty Status Flag	0: The transmit/receive FIFO buffer contains messages. 1: The transmit/receive FIFO buffer contains no message (buffer empty).	R
b1	CFFLL	Transmit/Receive FIFO Buffer Full Status Flag	0: The transmit/receive FIFO buffer is not full. 1: The transmit/receive FIFO buffer is full.	R
b2	CFMLT	Transmit/Receive FIFO Message Lost Flag	0: No transmit/receive FIFO message is lost. 1: A transmit/receive FIFO message is lost.	R/(W) *1
b3	CFRXIF	Transmit/Receive FIFO Receive Interrupt Request Flag	0: No transmit/receive FIFO receive interrupt request is present. 1: A transmit/receive FIFO receive interrupt request is present.	R/(W) *1
b4	CFTXIF	Transmit/Receive FIFO Transmit Interrupt Request Flag	0: No transmit/receive FIFO transmit interrupt request is present. 1: A transmit/receive FIFO transmit interrupt request is present.	R/(W) *1
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13 to b8	CFMC[5:0]	Transmit/Receive FIFO Message Counter	The number of messages stored in the transmit/receive FIFO buffer is indicated.	R
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The only effective value for writing to this flag is 0, which clears the flag. Otherwise writing to the flag results in retention of its state.

CFEMP Flag (Transmit/Receive FIFO Buffer Empty Status Flag)

[Setting conditions]

- When the CFCCH0.CFM[1:0] value is 00b: All messages have been read, or global reset mode.
- When the CFCCH0.CFM[1:0] value is 01b: All messages have been transmitted, or channel reset mode.
- When the CFCCL0.CFE value is 0 (no transmit/receive FIFO buffer is used).
  Note that this flag is set to 1 after transmission completion, CAN bus error detection, or arbitration lost when the message in the transmit/receive FIFO buffer is being transmitted or to be transmitted next.

[Clearing conditions]

- When the CFCCH0.CFM[1:0] value is 00b: Any one of received messages has been stored in the transmit/receive FIFO buffer.
- When the CFCCH0.CFM[1:0] value is 01b: A value FFh has been written to the CFPCTR0 register after data was written to the CFIDL0, CFIDH0, CFPTR0, and CFDF00 to CFDF30 registers.

CFFLL Flag (Transmit/Receive FIFO Buffer Full Status Flag)

[Setting condition]

- When the number of messages stored in the transmit/receive FIFO buffer matches the FIFO buffer depth set by the CFCCL0.CFDC[2:0] bits.

[Clearing conditions]

- When the number of messages stored in the transmit/receive FIFO buffer becomes smaller than the FIFO buffer

depth set by the CFCCL0.CFDC[2:0] bits.

- When the CFCCL0.CFE value is 0 (no transmit/receive FIFO buffer is used).
  Note that this flag is set to 0 after transmission completion, CAN bus error detection, or arbitration lost when the message in the transmit/receive FIFO buffer is being transmitted or to be transmitted next.
- When CFCCH0.CFM[1:0] value is 00b: In global reset mode
- When CFCCH0.CFM[1:0] value is 01b: In channel reset mode

CFMLT Flag (Transmit/Receive FIFO Message Lost Flag)

[Setting condition]

- When it is attempted to store a new message while the transmit/receive FIFO buffer is full. In this case, the new message is discarded.

[Clearing conditions]

- Write 0 to the CFMLT flag
- When CFCCH0.CFM[1:0] value is 00b: In global reset mode
- When CFCCH0.CFM[1:0] value is 01b: In channel reset mode

Set this flag to 0 in global operating mode or global test mode.

CFRXIF Flag (Transmit/Receive FIFO Receive Interrupt Request Flag)

[Setting condition]

- When CFCCH0.CFM[1:0] value is 00b and interrupt source setting the CFCCL0.CFIM bit is generated.

[Clearing conditions]

- Write 0 to the CFRXIF flag
- When CFCCH0.CFM[1:0] value is 00b: In global reset mode
- When CFCCH0.CFM[1:0] value is 01b: In channel reset mode

Set this flag to 0 in global operating mode or global test mode.

CFTXIF Flag (Transmit/Receive FIFO Transmit Interrupt Request Flag)

[Setting condition]

- When CFCCH0.CFM[1:0] value is 01b and interrupt source setting the CFCCL0.CFIM bit is generated.

[Clearing conditions]

- Write 0 to the CFTXIF flag
- When CFCCH0.CFM[1:0] value is 00b: In global reset mode
- When CFCCH0.CFM[1:0] value is 01b: In channel reset mode

Set this flag to 0 in global operating mode or global test mode.

CFMC[5:0] Flags (Transmit/Receive FIFO Message Counter)

The CFMC[5:0] flags indicate the following values that depend on the setting of the CFCCH0.CFM[1:0] bits.

- When CFM[1:0] value is 01b (transmit mode): Number of untransmitted messages in the buffer
- When CFM[1:0] value is 00b (receive mode): Number of unread received messages in the buffer

These bits are set to 0 when any of the following conditions is met.

- When CFCCH0.CFM[1:0] value is 00b: In global reset mode
- When CFCCH0.CFM[1:0] value is 01b: In channel reset mode

28.2.48 Transmit/Receive FIFO Pointer Control Register 0 (CFPCTR0)

Address(es): RSCAN0.CEPCTR0 000A 835Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	CFPC[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	CFPC[7:0]	RSCAN0 Transmit/Receive FIFO Pointer	Receive mode: Writing FFh to these bits moves the read pointer to the next unread message in the transmit/receive FIFO buffer. Transmit mode: Writing FFh to these bits moves the write pointer to the next stage of the transmit/receive FIFO buffer.	W
b15 to b8	—	Reserved	The write value should be 0.	W

CFPC[7:0] Bits (RSCAN0 Transmit/Receive FIFO Pointer)

Receive mode (CFCCH0.CFM[1:0] value is 00b):
Writing FFh to the CFPC[7:0] bits moves the read pointer to the next unread message in the transmit/receive FIFO buffer. At this time, the CFSTS0.CFMC[5:0] value (transmit/receive FIFO message counter) is decremented. Read the CFIDL0, CFIDH0, CFTS0, CFPTR0, and CFDF00 to CFDF30 registers to read messages in the transmit/receive FIFO buffer, and then write FFh to the CFPC[7:0] bits.
Write FFh to these bits when the CFCCL0.CFE bit is set to 1 (transmit/receive FIFO buffers are used) and the CFSTS0.CFEMP flag is set to 0 (the transmit/receive FIFO buffer contains messages).

Transmit mode (CFCCH0.CFM[1:0] value is 01b):
Writing FFh to the CFPC[7:0] bits stores the data written to the CFIDL0, CFIDH0, CFPTR0, and CFDF00 to CFDF30 registers in the transmit/receive FIFO buffer and moves the write pointer to the next stage of the transmit/receive FIFO buffer. At this time, the CFSTS0.CFMC[5:0] value is incremented. Write transmit messages to the CFIDL0, CFIDH0, CFPTR0, and CFDF00 to CFDF30 registers and then write FFh to the CFPC[7:0] bits.
Write FFh to these bits when the CFCCL0.CFE bit is set to 1 and the CFSTS0.CFFLL flag is set to 0 (the transmit/receive FIFO buffer is not full).

28.2.49 Transmit/Receive FIFO Access Register 0AL (CFIDL0)

Address(es): RSCAN0.CFIDL0 000A 85E0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CFID[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	CFID[15:0]	Transmit/Receive FIFO Buffer ID Data L	When CFCCH0.CFM[1:0] value is 01b (transmit mode): Set standard ID or extended ID. For standard ID, write an ID to bits 10 to 0 and write 0 to bits 15 to 11. When CFCCH0.CFM[1:0] value is 00b (receive mode): Standard ID or extended ID in the received message can be read. For standard ID, read bits 10 to 0. Bits 15 to 11 are read as 0.	R/W

Modify this register only when the CFCCH0.CFM[1:0] value is 01b (transmit mode). This register is readable only when the CFCCH0.CFM[1:0] value is 00b (receive mode).
This register can be read/written when the GRWCR.RPAGE bit is 1.

CFID[15:0] Bits (Transmit/Receive FIFO Buffer ID Data L)

These bits indicate the ID of the received message stored in the transmit/receive FIFO buffer when the CFCCH0.CFM[1:0] value is 00b.
When the CFCCH0.CFM[1:0] value is 01b, set the ID of the message to be transmitted from the transmit/receive FIFO buffer.

28.2.50 Transmit/Receive FIFO Access Register 0AH (CFIDH0)

Address(es): RSCAN0.CFIDH0 000A 85E2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CFIDE	CFRTR	THLEN	CFID[28:16]												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b12 to b0	CFID[28:16]	Transmit/Receive FIFO Buffer ID Data H	When CFCCH0.CFM[1:0] value is 01b (transmit mode): Set standard ID or extended ID. For standard ID, write 0 to these bits. When CFCCH0.CFM[1:0] value is 00b (receive mode): Standard ID or extended ID in the received message can be read. For standard ID, these bits are read as 0.	R/W
b13	THLEN	Transmit History Data Store Enable	This bit is valid only when the CFCCH0.CFM[1:0] value is 01b (transmit mode). 0: Transmit history data is not stored in the buffer. 1: Transmit history data is stored in the buffer.	R/W
b14	CFRTR	Transmit/Receive FIFO Buffer RTR	0: Data frame 1: Remote frame	R/W
b15	CFIDE	Transmit/Receive FIFO Buffer IDE	0: Standard ID 1: Extended ID	R/W

Modify this register only when the CFCCH0.CFM[1:0] value is 01b (transmit mode).
This register is readable only when the CFCCH0.CFM[1:0] value is 00b (receive mode).
This register can be read/written when the GRWCR.RPAGE bit is 1.

CFID[28:16] Bits (Transmit/Receive FIFO Buffer ID Data H)

These bits indicate the ID of the received message stored in the transmit/receive FIFO buffer when the CFCCH0.CFM[1:0] value is 00b.
When the CFCCH0.CFM[1:0] value is 01b, set the ID of the message to be transmitted from the transmit/receive FIFO buffer.

THLEN Bit (Transmit History Data Store Enable)

When this bit is set to 1, the transmit history data (label information, buffer number, and buffer type) of transmit messages is stored in the transmit history buffer after transmission is completed.
This bit is enabled when the CFCCH0.CFM[1:0] value is 01b (transmit mode).

CFRTR Bit (Transmit/Receive FIFO Buffer RTR)

This bit indicates the data format (data frame or remote frame) of the received message stored in the transmit/receive FIFO buffer when the CFCCH0.CFM[1:0] value is 00b. When the CFCCH0.CFM[1:0] value is 01b, set the data format of the message to be transmitted from the transmit/receive FIFO buffer.

CFIDE Bit (Transmit/Receive FIFO Buffer IDE)

This bit indicates the ID format (standard ID or extended ID) of the received message stored in the transmit/receive FIFO buffer when the CFCCH0.CFM[1:0] value is 00b. When the CFCCH0.CFM[1:0] value is 01b, set the ID format of the message to be transmitted from the transmit/receive FIFO buffer.

28.2.51 Transmit/Receive FIFO Access Register 0BL (CFTS0)

Address(es): RSCAN0.CFTS0 000A 85E4h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CFTS[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	CFTS[15:0]	Transmit/Receive FIFO Buffer Timestamp Data	These bits are valid only when the CFCCH0.CFM[1:0] value is 00b (receive mode). The timestamp value of the received message can be read.	R

This register can be read when the GRWCR.RPAGE bit is 1.

CFTS[15:0] Bits (Transmit/Receive FIFO Buffer Timestamp Data)

These bits indicate the timestamp value of the message stored in the transmit/receive FIFO buffer.
These bits are valid when the CFCCH0.CFM[1:0] value is 00b.

28.2.52 Transmit/Receive FIFO Access Register 0BH (CFPTR0)

Address(es): RSCAN0.CFPTR0 000A 85E6h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CFDLC[3:0]				CFPTR[11:0]											
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b11 to b0	CFPTR[11:0]	Transmit/Receive FIFO Buffer Label Data	When CFCCH0.CFM[1:0] value is 01b (transmit mode): Set the label information to be stored in the transmit history buffer. Only CFPTR[7:0] bits are valid. When CFCCH0.CFM[1:0] value is 00b (receive mode): The label information of the received message can be read.	R/W
b15 to b12	CFDLC[3:0]	Transmit/Receive FIFO Buffer DLC Data	b15 b12 0 0 0 0: 0 data bytes 0 0 0 1: 1 data byte 0 0 1 0: 2 data bytes 0 0 1 1: 3 data bytes 0 1 0 0: 4 data bytes 0 1 0 1: 5 data bytes 0 1 1 0: 6 data bytes 0 1 1 1: 7 data bytes 1 x x x: 8 data bytes	R/W

x: Don’t care

Modify this register only when the CFCCH0.CFM[1:0] value is 01b (transmit mode).
This register is readable only when the CFCCH0.CFM[1:0] value is 00b (receive mode).
This register can be read/written when the GRWCR.RPAGE bit is 1.

CFPTR[11:0] Bits (Transmit/Receive FIFO Buffer Label Data)

These bits indicate the label information attached to the received message stored in the transmit/receive FIFO buffer when the CFCCH0.CFM[1:0] value is 00b. When the CFCCH0.CFM[1:0] value is 01b, the CFPTR[7:0] value is stored in the transmit history buffer when message transmission has been completed.

CFDLC[3:0] Bits (Transmit/Receive FIFO Buffer DLC Data)

These bits indicate the data length of the received message stored in the transmit/receive FIFO buffer when the CFCCH0.CFM[1:0] value is 00b. When the CFCCH0.CFM[1:0] value is 01b, set the data length of the message to be transmitted from the transmit/receive FIFO buffer.
If 9-byte or more data length is set, 8 bytes of data is actually transmitted.

28.2.53 Transmit/Receive FIFO Access Register 0CL (CFDF00)

Address(es): RSCAN0.CFDF00 000A 85E8h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CFDB1[7:0]								CFDB0[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	CFDB0[7:0]	Transmit/Receive FIFO Buffer Data Byte 0	When CFCCH0.CFM[1:0] value is 01b (transmit mode): Set the transmit/receive FIFO buffer data. When CFCCH0.CFM[1:0] value is 00b (receive mode): The message data stored in the transmit/receive FIFO buffer can be read.	R/W
b15 to b8	CFDB1[7:0]	Transmit/Receive FIFO Buffer Data Byte 1		R/W

Modify this register only when the CFCCH0.CFM[1:0] value is 01b.
This register is readable only when the CFCCH0.CFM[1:0] value is 00b. When the CFPTR0.CFDLC[3:0] value is smaller than 1000b, data bytes for which no data is set are read as 00h.
This register can be read/written when the GRWCR.RPAGE bit is 1.

28.2.54 Transmit/Receive FIFO Access Register 0CH (CFDF10)

Address(es): RSCAN0.CFDF10 000A 85EAh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CFDB3[7:0]								CFDB2[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	CFDB2[7:0]	Transmit/Receive FIFO Buffer Data Byte 2	When CFCCH0.CFM[1:0] value is 01b (transmit mode): Set the transmit/receive FIFO buffer data. When CFCCH0.CFM[1:0] value is 00b (receive mode): The message data stored in the transmit/receive FIFO buffer can be read.	R/W
b15 to b8	CFDB3[7:0]	Transmit/Receive FIFO Buffer Data Byte 3		R/W

Modify this register only when the CFCCH0.CFM[1:0] value is 01b.
This register is readable only when the CFCCH0.CFM[1:0] value is 00b. When the CFPTR0.CFDLC[3:0] value is smaller than 1000b, data bytes for which no data is set are read as 00h.
This register can be read/written when the GRWCR.RPAGE bit is 1.

28.2.55 Transmit/Receive FIFO Access Register 0DL (CFDF20)

Address(es): RSCAN0.CFDF20 000A 85ECh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CFDB5[7:0]								CFDB4[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	CFDB4[7:0]	Transmit/Receive FIFO Buffer Data Byte 4	When CFCCH0.CFM[1:0] value is 01b (transmit mode): Set the transmit/receive FIFO buffer data. When CFCCH0.CFM[1:0] value is 00b (receive mode): The message data stored in the transmit/receive FIFO buffer can be read.	R/W
b15 to b8	CFDB5[7:0]	Transmit/Receive FIFO Buffer Data Byte 5		R/W

Modify this register only when the CFCCH0.CFM[1:0] value is 01b.
This register is readable only when the CFCCH0.CFM[1:0] value is 00b. When the CFPTR0.CFDLC[3:0] value is smaller than 1000b, data bytes for which no data is set are read as 00h.
This register can be read/written when the GRWCR.RPAGE bit is 1.

28.2.56 Transmit/Receive FIFO Access Register 0DH (CFDF30)

Address(es): RSCAN0.CFDF30 000A 85EEh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CFDB7[7:0]								CFDB6[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	CFDB6[7:0]	Transmit/Receive FIFO Buffer Data Byte 6	When CFCCH0.CFM[1:0] value is 01b (transmit mode): Set the transmit/receive FIFO buffer data. When CFCCH0.CFM[1:0] value is 00b (receive mode): The message data stored in the transmit/receive FIFO buffer can be read.	R/W
b15 to b8	CFDB7[7:0]	Transmit/Receive FIFO Buffer Data Byte 7		R/W

Modify this register only when the CFCCH0.CFM[1:0] value is 01b.
This register is readable only when the CFCCH0.CFM[1:0] value is 00b. When the CFPTR0.CFDLC[3:0] value is smaller than 1000b, data bytes for which no data is set are read as 00h.
This register can be read/written when the GRWCR.RPAGE bit is 1.

28.2.57 Receive FIFO Message Lost Status Register (RFMSTS)

Address(es): RSCAN.RFMSTS 000A 8360h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	RF1MLT	RF0MLT
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	RF0MLT	Receive FIFO Buffer 0 Message Lost Status Flag	0: No receive FIFO buffer m message is lost (m = 0, 1). 1: A receive FIFO buffer m message is lost.	R
b1	RF1MLT	Receive FIFO Buffer 1 Message Lost Status Flag		R
b7 to b2	—	Reserved	These bits are read as 0.	R

The RFMSTS register is set to 00h in global reset mode.

RFmMLT Flag (Receive FIFO Buffer m Message Lost Status Flag)

The RFmMLT flag is set to 1 when the RFSTSm.RFMLT flag is set to 1 (a receive FIFO message is lost). When the RFSTSm.RFMLT flag is set to 0, the RFmMLT flag is set to 0.

28.2.58 Transmit/Receive FIFO Message Lost Status Register (CFMSTS)

Address(es): RSCAN0.CFMSTS 000A 8361h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CF0MLT
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CF0MLT	RSCAN0 Transmit/Receive FIFO Buffer 0 Message Lost Status Flag	0: No RSCAN0 transmit/receive FIFO buffer 0 message is lost. 1: An RSCAN0 transmit/receive FIFO buffer 0 message is lost.	R
b7 to b1	—	Reserved	These bits are read as 0.	R

The CFMSTS register is set to 00h in global reset mode.

CF0MLT Flag (RSCAN0 Transmit/Receive FIFO Buffer 0 Message Lost Status Flag)

The CF0MLT flag is set to 1 when the CFSTS0.CFMLT flag is set to 1 (a transmit/receive FIFO message is lost). When the CFSTS0.CFMLT flag is set to 0, the CF0MLT flag is set to 0.

28.2.59 Receive FIFO Interrupt Status Register (RFISTS)

Address(es): RSCAN.RFISTS 000A 8362h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	RF1IF	RF0IF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	RF0IF	Receive FIFO Buffer 0 Interrupt Request Status Flag	0: No receive FIFO buffer m interrupt request is present (m = 0, 1). 1: A receive FIFO buffer m interrupt request is present.	R
b1	RF1IF	Receive FIFO Buffer 1 Interrupt Request Status Flag		R
b7 to b2	—	Reserved	These bits are read as 0.	R

The RFISTS register is set to 00h in global reset mode.

RFmIF Flag (Receive FIFO Buffer m Interrupt Request Status Flag)

The RFmIF flag is set to 1 when the RFSTSm.RFIF flag is set to 1 (a receive FIFO interrupt request is present). When the RFSTSm.RFIF flag is set to 0, the RFmIF flag is set to 0.

28.2.60 Transmit/Receive FIFO Receive Interrupt Status Register (CFISTS)

Address(es): RSCAN.CFISTS 000A 8363h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CF0IF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CF0IF	RSCAN0 Transmit/Receive FIFO Buffer 0 Receive Interrupt Request Status Flag	0: No RSCAN0 transmit/receive FIFO buffer 0 receive interrupt request is present. 1: An RSCAN0 transmit/receive FIFO buffer 0 receive interrupt request is present.	R
b7 to b1	—	Reserved	These bits are read as 0.	R

The CFISTS register is set to 00h in global reset mode.

CF0IF Flag (RSCAN0 Transmit/Receive FIFO Buffer 0 Receive Interrupt Request Status Flag)

The CF0IF flag is set to 1 when the CFSTS0.CFRXIF flag is set to 1 (a transmit/receive FIFO receive interrupt request is present). When the CFSTS0.CFRXIF flag is set to 0, the CF0IF flag is set to 0.

28.2.61 Transmit Buffer Control Register p (TMCp) (p = 0 to 3)

Address(es): RSCAN0.TMC0 000A 8364h, RSCAN0.TMC1 000A 8365h, RSCAN0.TMC2 000A 8366h, RSCAN0.TMC3 000A 8367h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	TMOM	TMTAR	TMTR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TMTR	Transmit Request	0: Transmission is not requested. 1: Transmission is requested.	R/(W) *1
b1	TMTAR	Transmit Abort Request	0: Transmit abort is not requested. 1: Transmit abort is requested.	R/(W) *1
b2	TMOM	One-Shot Transmission Enable	0: One-shot transmission is disabled. 1: One-shot transmission is enabled.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. the only effective value for writing to this bit is 1, which sets the bit. Otherwise writing to the bit results in retention of its state.

When the TMCp register meets the following condition, set it to 00h.

- The TMCp register corresponds to the transmit buffer number selected by the CFCCH0.CFTML[1:0] bits.

Bits in the TMCp register become all 0s in channel reset mode. Modify the TMCp register (p = 0 to 3) only in channel communication mode or channel halt mode.

TMTR Bit (Transmit Request)

Setting this bit to 1 transmits the message stored in the transmit buffer.
The TMTR bit is set to 0 when any of the following conditions is met, but is not set to 0 by writing 0 by the program.

- Transmission has been completed.
- Transmit abort has been completed by setting the TMTAR bit to 1.
- An error or arbitration lost has been detected with the TMOM bit set to 1.

Set the TMTR bit to 1 when the TMSTSp.TMTRF[1:0] value is 00b.

TMTAR Bit (Transmit Abort Request)

Setting this bit to 1 generates a transmit abort request for the message stored in the transmit buffer. However, a message that is being transmitted or to be transmitted next cannot be aborted.
When the TMTR bit is set to 1, the TMTAR bit can be set to 1.
The TMTAR bit is set to 0 when any of the following conditions is met, but is not set to 0 by writing 0 by the program.

- Transmission has been completed.
- Transmit abort has been completed.
- An error or arbitration lost has been detected.

If this bit becomes 0 at the timing when the program writes 1 to this bit, this bit becomes 0.

TMOM Bit (One-Shot Transmission Enable)

Setting this bit to 1 enables one-shot transmission. When transmission fails, retransmission defined in the CAN protocol is not performed.
Modify the TMOM bit when the TMSTSp.TMTRM flag is set to 0. To set the TMOM bit to 1, also set the TMTR bit together.

28.2.62 Transmit Buffer Status Register p (TMSTSp) (p = 0 to 3)

Address(es): RSCAN0.TMSTS0 000A 836Ch, RSCAN0.TMSTS1 000A 836Dh, RSCAN0.TMSTS2 000A 836Eh, RSCAN0.TMSTS3 000A 836Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	TMTARM	TMTRM	TMTRF[1:0]		TMTSTS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TMTSTS	Transmit Buffer Transmit Status Flag	0: Transmission is not in progress. 1: Transmission is in progress.	R
b2, b1	TMTRF[1:0]	Transmit Buffer Transmit Result Flag	b2 b1 0 0: Transmission is in progress or no transmit request is present. 0 1: Transmit abort has been completed. 1 0: Transmission has been completed (without transmit abort request). 1 1: Transmission has been completed (with transmit abort request).	R/W
b3	TMTRM	Transmit Buffer Transmit Request Status Flag	0: No transmit request is present. 1: A transmit request is present.	R
b4	TMTARM	Transmit Buffer Transmit Abort Request Status Flag	0: No transmit abort request is present. 1: A transmit abort request is present.	R
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R

The TMSTSp register becomes all 0s in channel reset mode.

TMTSTS Flag (Transmit Buffer Transmit Status Flag)

This flag is set to 1 when transmission from the transmit buffer starts, and is set to 0 when transmission from the transmit buffer has been completed or terminated due to a bus error or arbitration lost.

TMTRF[1:0] Flags (Transmit Buffer Transmit Result Flag)

These flags indicate the result of transmission from the transmit buffer.
00b: Transmission is in progress or no transmit request is present.
01b: Transmission from the transmit buffer was aborted.
10b: Transmission has been completed with the TMCp.TMTAR bit set to 0 (transmit abort is not requested).
11b: Transmission has been completed with the TMCp.TMTAR bit set to 1 (transmit abort is requested).
Write 00b to the TMTRF[1:0] flags in channel communication mode or channel halt mode. Do not write any value other than 00b to these flags.

TMTRM Flag (Transmit Buffer Transmit Request Status Flag)

The TMTRM flag is set to 1 when the TMCp.TMTR bit is set to 1, and is set to 0 when the TMCp.TMTR bit is set to 0.

TMTARM Flag (Transmit Buffer Transmit Abort Request Status Flag)

The TMTARM flag is set to 1 when the TMCp.TMTAR bit is set to 1, and is set to 0 when the TMCp.TMTAR bit is set to 0.

28.2.63 Transmit Buffer Transmit Request Status Register (TMTRSTS)

Address(es): RSCAN0.TMTRSTS 000A 8374h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	TMTRSTS3	TMTRSTS2	TMTRSTS1	TMTRSTS0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TMTRSTS0	RSCAN0 Transmit Buffer 0 Transmit Request Status Flag	0: No transmit request is present. 1: A transmit request is present.	R
b1	TMTRSTS1	RSCAN0 Transmit Buffer 1 Transmit Request Status Flag		R
b2	TMTRSTS2	RSCAN0 Transmit Buffer 2 Transmit Request Status Flag		R
b3	TMTRSTS3	RSCAN0 Transmit Buffer 3 Transmit Request Status Flag		R
b15 to b4	—	Reserved	These bits are read as 0.	R

TMTRSTSp Flag (RSCAN0 Transmit Buffer p Transmit Request Status Flag) (p = 0 to 3)

This flag indicates the status of the TMCp.TMTR bit.

When the TMTR bit is set to 1 (transmission is requested), the corresponding TMTRSTSp flag is set to 1.

The corresponding TMTRSTSp flag is set to 0 when the TMTR bit is set to 0 (transmission is not requested) or in channel reset mode.

28.2.64 Transmit Buffer Transmit Complete Status Register (TMTCSTS)

Address(es): RSCAN0.TMTCSTS 000A 8376h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	TMTCSTS3	TMTCSTS2	TMTCSTS1	TMTCSTS0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TMTCSTS0	RSCAN0 Transmit Buffer 0 Transmit Complete Status Flag	0: Transmission has not been completed. 1: Transmission has been completed.	R
b1	TMTCSTS1	RSCAN0 Transmit Buffer 1 Transmit Complete Status Flag		R
b2	TMTCSTS2	RSCAN0 Transmit Buffer 2 Transmit Complete Status Flag		R
b3	TMTCSTS3	RSCAN0 Transmit Buffer 3 Transmit Complete Status Flag		R
b15 to b4	—	Reserved	These bits are read as 0.	R

TMTCSTSp Flag (RSCAN0 Transmit Buffer p Transmit Complete Status Flag) (p = 0 to 3)

When the TMSTSp.TMTRF[1:0] flags are set to 10b (transmission has been completed (without transmit abort request)) or 11b (transmission has been completed (with transmit abort request)), the corresponding TMTCSTSp flag is set to 1. This flag is set to 0 when the corresponding TMSTSp.TMTRF[1:0] flags are set to 00b or in channel reset mode.

28.2.65 Transmit Buffer Transmit Abort Status Register (TMTASTS)

Address(es): RSCAN0.TMTASTS 000A 8378h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	TMTASTS3	TMTASTS2	TMTASTS1	TMTASTS0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TMTASTS0	RSCAN0 Transmit Buffer 0 Transmit Abort Status Flag	0: Transmission is not aborted. 1: Transmission is aborted.	R
b1	TMTASTS1	RSCAN0 Transmit Buffer 1 Transmit Abort Status Flag		R
b2	TMTASTS2	RSCAN0 Transmit Buffer 2 Transmit Abort Status Flag		R
b3	TMTASTS3	RSCAN0 Transmit Buffer 3 Transmit Abort Status Flag		R
b15 to b4	—	Reserved	These bits are read as 0.	R

TMTASTSp Flag (RSCAN0 Transmit Buffer p Transmit Abort Status Flag) (p = 0 to 3)

When the TMSTSp.TMTRF[1:0] flags are set to 01b (transmit abort has been completed), the corresponding TMTASTSp flag is set to 1.

This flag is set to 0 when the corresponding TMSTSp.TMTRF[1:0] flags are set to 00b or in channel reset mode.

28.2.66 Transmit Buffer Interrupt Enable Register (TMIEC)

Address(es): RSCAN0.TMIEC 000A 837Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	TMIE3	TMIE2	TMIE1	TMIE0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TMIE0	RSCAN0 Transmit Buffer 0 Interrupt Enable	0: Transmit buffer interrupt is disabled. 1: Transmit buffer interrupt is enabled.	R/W
b1	TMIE1	RSCAN0 Transmit Buffer 1 Interrupt Enable		R/W
b2	TMIE2	RSCAN0 Transmit Buffer 2 Interrupt Enable		R/W
b3	TMIE3	RSCAN0 Transmit Buffer 3 Interrupt Enable		R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TMIEp Bit (RSCAN0 Transmit Buffer p Interrupt Enable) (p = 0 to 3)

When TMIEp bit is set to 1 and the corresponding transmission has been completed, a transmit buffer interrupt request is generated.

Modify this bit when the corresponding TMSTSp.TMTRM flag is 0 (no transmit request is present).

Write 0 to bits corresponding to transmit buffers linked to transmit/receive FIFO buffers.

28.2.67 Transmit Buffer Register pAL (TMIDLp) (p = 0 to 3)

Address(es): RSCAN0.TMIDL0 000A 8600h, RSCAN0.TMIDL1 000A 8610h, RSCAN0.TMIDL2 000A 8620h, RSCAN0.TMIDL3 000A 8630h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TMID[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	TMID[15:0]	Transmit Buffer ID Data L	Set standard ID or extended ID. For standard ID, write an ID to bits b10 to b0 and write 0 to bits b15 to b11.	R/W

Modify this register when the corresponding TMSTSp.TMTRM flag is set to 0 (no transmit request is present). If this register is linked to any transmit/receive FIFO buffer, do not write data to this register.

This register can be read/written when the GRWCR.RPAGE bit is 1.

TMID[15:0] Bits (Transmit Buffer ID Data L)

These bits are used to set the ID of the message to be transmitted from the transmit buffer.

28.2.68 Transmit Buffer Register pAH (TMIDHp) (p = 0 to 3)

Address(es): RSCAN0.TMIDH0 000A 8602h, RSCAN0.TMIDH1 000A 8612h, RSCAN0.TMIDH2 000A 8622h, RSCAN0.TMIDH3 000A 8632h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TMIDE	TMRTR	THLEN	TMID[28:16]												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b12 to b0	TMID[28:16]	Transmit Buffer ID Data H	Set standard ID or extended ID. For standard ID, write 0 to these bits.	R/W
b13	THLEN	Transmit History Data Store Enable	0: Transmit history data is not stored in the buffer. 1: Transmit history data is stored in the buffer.	R/W
b14	TMRTR	Transmit Buffer RTR	0: Data frame 1: Remote frame	R/W
b15	TMIDE	Transmit Buffer IDE	0: Standard ID 1: Extended ID	R/W

Modify this register when the corresponding TMSTSp.TMTRM flag is set to 0 (no transmit request is present). If this register is linked to any transmit/receive FIFO buffer, do not write data to this register.
This register can be read/written when the GRWCR.RPAGE bit is 1.

TMID[28:16] Bits (Transmit Buffer ID Data H)

These bits are used to set the ID of the message to be transmitted from the transmit buffer.

THLEN Bit (Transmit History Data Store Enable)

When this bit is set to 1, the transmit history data (label information, buffer number, and buffer type) of transmit messages is stored in the transmit history buffer after transmission is completed.

TMRTR Bit (Transmit Buffer RTR)

This bit is used to set the data format of the message to be transmitted from the transmit buffer.

TMIDE Bit (Transmit Buffer IDE)

This bit is used to set the ID format of the message to be transmitted from the transmit buffer.

28.2.69 Transmit Buffer Register pBH (TMPTRp) (p = 0 to 3)

Address(es): RSCAN0.TMPTR0 000A 8606h, RSCAN0.TMPTR1 000A 8616h, RSCAN0.TMPTR2 000A 8626h, RSCAN0.TMPTR3 000A 8636h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TMDLC[3:0]				—	—	—	—	TMPTR[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	TMPTR[7:0]	Transmit Buffer Label Data	Set the label information to be stored in the transmit history buffer.	R/W
b11 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b12	TMDLC[3:0]	Transmit Buffer DLC Data	b15 b12 0 0 0 0: 0 data bytes 0 0 0 1: 1 data byte 0 0 1 0: 2 data bytes 0 0 1 1: 3 data bytes 0 1 0 0: 4 data bytes 0 1 0 1: 5 data bytes 0 1 1 0: 6 data bytes 0 1 1 1: 7 data bytes 1 x x x: 8 data bytes	R/W

x: Don’t care

Modify this register when the corresponding TMSTSp.TMTRM flag is set to 0 (no transmit request is present). If this register is linked to any transmit/receive FIFO buffer, do not write data to this register.
This register can be read/written when the GRWCR.RPAGE bit is 1.

TMPTR[7:0] Bits (Transmit Buffer Label Data)

When message transmission has been completed, the TMPTR[7:0] value is stored in the transmit history buffer.

TMDLC[3:0] Bits (Transmit Buffer DLC Data)

These bits are used to set the data length of the message to be transmitted from the transmit buffer when the TMIDHp.TMRTR bit is set to 0 (data frame). If a 9-byte (or more) data length is set, 8 bytes of data is actually transmitted.
When the TMIDHp.TMRTR bit is set to 1 (remote frame), set the data length of messages to be requested.

28.2.70 Transmit Buffer Register pCL (TMDF0p) (p = 0 to 3)

Address(es): RSCAN0.TMDF00 000A 8608h, RSCAN0.TMDF01 000A 8618h, RSCAN0.TMDF02 000A 8628h, RSCAN0.TMDF03 000A 8638h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TMDB1[7:0]								TMDB0[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	TMDB0[7:0]	Transmit Buffer Data Byte 0	Set transmit buffer data.	R/W
b15 to b8	TMDB1[7:0]	Transmit Buffer Data Byte 1		R/W

Modify this register when the corresponding TMSTSp.TMTRM flag is set to 0 (no transmit request is present). If this register is linked to any transmit/receive FIFO buffer, do not write data to this register.
This register can be read/written when the GRWCR.RPAGE bit is 1.

28.2.71 Transmit Buffer Register pCH (TMDF1p) (p = 0 to 3)

Address(es): RSCAN0.TMDF10 000A 860Ah, RSCAN0.TMDF11 000A 861Ah, RSCAN0.TMDF12 000A 862Ah, RSCAN0.TMDF13 000A 863Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TMDB3[7:0]								TMDB2[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	TMDB2[7:0]	Transmit Buffer Data Byte 2	Set transmit buffer data.	R/W
b15 to b8	TMDB3[7:0]	Transmit Buffer Data Byte 3		R/W

Modify this register when the corresponding TMSTSp.TMTRM flag is set to 0 (no transmit request is present). If this register is linked to any transmit/receive FIFO buffer, do not write data to this register.
This register can be read/written when the GRWCR.RPAGE bit is 1.

28.2.72 Transmit Buffer Register pDL (TMDF2p) (p = 0 to 3)

Address(es): RSCAN0.TMDF20 000A 860Ch, RSCAN0.TMDF21 000A 861Ch, RSCAN0.TMDF22 000A 862Ch, RSCAN0.TMDF23 000A 863Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TMDB5[7:0]								TMDB4[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	TMDB4[7:0]	Transmit Buffer Data Byte 4	Set transmit buffer data.	R/W
b15 to b8	TMDB5[7:0]	Transmit Buffer Data Byte 5		R/W

Modify this register when the corresponding TMSTSp.TMTRM flag is set to 0 (no transmit request is present). If this register is linked to any transmit/receive FIFO buffer, do not write data to this register.
This register can be read/written when the GRWCR.RPAGE bit is 1.

28.2.73 Transmit Buffer Register pDH (TMDF3p) (p = 0 to 3)

Address(es): RSCAN0.TMDF30 000A 860Eh, RSCAN0.TMDF31 000A 861Eh, RSCAN0.TMDF32 000A 862Eh, RSCAN0.TMDF33 000A 863Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TMDB7[7:0]								TMDB6[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	TMDB6[7:0]	Transmit Buffer Data Byte 6	Set transmit buffer data.	R/W
b15 to b8	TMDB7[7:0]	Transmit Buffer Data Byte 7		R/W

Modify this register when the corresponding TMSTSp.TMTRM flag is set to 0 (no transmit request is present). If this register is linked to any transmit/receive FIFO buffer, do not write data to this register.
This register can be read/written when the GRWCR.RPAGE bit is 1.

28.2.74 Transmit History Buffer Control Register (THLCC0)

Address(es): RSCAN0.THLCC0 000A 837Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	THLDTE	THLIM	THLIE	—	—	—	—	—	—	—	THLE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	THLE	Transmit History Buffer Enable	0: Transmit history buffer is not used. 1: Transmit history buffer is used.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	THLIE	Transmit History Interrupt Enable	0: Transmit history interrupt is disabled. 1: Transmit history interrupt is enabled.	R/W
b9	THLIM	Transmit History Interrupt Source Select	0: When 6 sets of data have been stored in the transmit history buffer 1: When a single set of transmit history data has been stored	R/W
b10	THLDTE	Transmit History Target Buffer Select	0: Entry from transmit/receive FIFO buffers 1: Entry from transmit buffers, transmit/receive FIFO buffers	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

THLE Bit (Transmit History Buffer Enable)

Setting this bit to 1 makes the transmit history buffer available. When data transmission from the buffer selected by the THLDTE bit has been completed, the transmit history data of transmit messages is stored in the transmit history buffer. Modify this bit only in channel communication mode or channel halt mode.

THLIE Bit (Transmit History Interrupt Enable)

When the THLIE bit is set to 1 and the source selected by the THLIM bit has occurred, a transmit history interrupt request is generated. Modify the THLIE bit with the THLE bit set to 0.

THLIM Bit (Transmit History Interrupt Source Select)

This bit is used to select a transmit history interrupt source.
Modify this bit only in channel reset mode.

THLDTE Bit (Transmit History Target Buffer Select)

When this bit is set to 0, the transmit history data of messages transmitted from transmit/receive FIFO buffers is stored in the transmit history buffer. When this bit is set to 1, the transmit history data of messages transmitted from transmit buffers and transmit/receive FIFO buffers is stored in the transmit history buffer.
Modify this bit only in channel reset mode.

28.2.75 Transmit History Buffer Status Register (THLSTS0)

Address(es): RSCAN0.THLSTS0 000A 8380h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	THLMC[3:0]				—	—	—	—	THLIF	THLELT	THLFLL	THLEMP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	THLEMP	Transmit History Buffer Empty Status Flag	0: Transmit history buffer contains unread data. 1: Transmit history buffer contains no unread data (buffer empty).	R
b1	THLFLL	Transmit History Buffer Full Status Flag	0: Transmit history buffer is not full. 1: Transmit history buffer is full.	R
b2	THLELT	Transmit History Buffer Overflow Flag	0: Transmit history buffer overflow has not occurred. 1: Transmit history buffer overflow has occurred.	R/(W) *1
b3	THLIF	Transmit History Interrupt Request Flag	0: No transmit history interrupt request is present. 1: A transmit history interrupt request is present.	R/(W) *1
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b11 to b8	THLMC[3:0]	Transmit History Buffer Unread Data Counter	These bits indicate the number of unread data sets stored in the transmit history buffer.	R
b15 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The only effective value for writing to this flag is 0, which clears the flag. Otherwise writing to the flag results in retention of its state.

THLEMP Flag (Transmit History Buffer Empty Status Flag)

The THLEMP flag becomes 0 when even a single set of transmit history data has been stored in the transmit history buffer.

This flag becomes 1 when all the data in the transmit history buffer has been read. This flag also becomes 1 in channel reset mode or when the THLCC0.THLE bit is set to 0 (transmit history buffer is not used).

THLFLL Flag (Transmit History Buffer Full Status Flag)

The THLFLL flag becomes 1 when 8 data sets have been stored in the transmit history buffer, and becomes 0 when the number of data sets stored in the transmit history buffer has decreased to less than 8.

This flag also becomes 0 in channel reset mode or when the THLCC0.THLE bit is set to 0 (transmit history buffer is not used).

THLELT Flag (Transmit History Buffer Overflow Flag)

The THLELT flag becomes 1 when it is attempted to store new transmit history data while the transmit history buffer is full. In this case, the new data is discarded.

This flag becomes 0 in channel reset mode or by writing 0 to this flag by the program.

THLIF Flag (Transmit History Interrupt Request Flag)

The THLIF flag becomes 1 when the interrupt source set by the THLCC0.THLIM bit has occurred.

This flag becomes 0 in channel reset mode or by writing 0 to this flag by the program.

THLMC[3:0] Flags (Transmit History Buffer Unread Data Counter)

These flags indicate the number of unread data sets stored in the transmit history buffer.

28.2.76 Transmit History Buffer Access Register (THLACC0)

Address(es): RSCAN0.THLACC0 000A 8680h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TID[7:0]								—	—	—	BN[1:0]		—	BT[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	BT[1:0]	Buffer Type Data	b1 b0 0 1: Transmit buffer 1 0: Transmit FIFO buffer	R
b2	—	Reserved	This bit is read as 0.	R
b4, b3	BN[1:0]	Buffer Number Data	The buffer number of transmit source (transmit buffer or transmit/receive FIFO) can be read.	R
b7 to b5	—	Reserved	These bits are read as 0.	R
b15 to b8	TID[7:0]	Label Data	The label information of stored data can be read.	R

This register can be read when the GRWCR.RPAGE bit is 1.

BT[1:0] Bits (Buffer Type Data)

These bits indicate the transmit source buffer type of transmit history data stored in the transmit history buffer.

BN[1:0] Bits (Buffer Number Data)

These bits indicate the transmit source buffer number of transmit history data stored in the transmit history buffer.

TID[7:0] Bits (Label Data)

These bits indicate the label information of transmit history data stored in the transmit history buffer.

28.2.77 Transmit History Buffer Pointer Control Register (THLPCTR0)

Address(es): RSCAN0.THLPCTR0 000A 8384h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	THLPC[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	THLPC[7:0]	Transmit History Buffer Pointer	Writing FFh to these bits moves the read pointer to the next unread data in the transmit history buffer.	W
b15 to b8	—	Reserved	The write value should be 0.	W

THLPC[7:0] Bits (Transmit History Buffer Pointer)

When the THLPC [7:0] bits are set to FFh, the read pointer moves to the next data in the transmit history buffer. At this time, the THLSTS0.THLMC[3:0] (transmit history buffer unread data counter) value is decremented. After reading the THLACC0 register, write FFh to the THLPC [7:0] bits.

Write FFh to the THLPC[7:0] bits when the THLCC0.THLE bit is set to 1 (transmit history buffer is used) and the THLSTS0.THLEMP flag is 0.

28.2.78 Global RAM Window Control Register (GRWCR)

Address(es): RSCAN.GRWCR 000A 838Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RPAGE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	RPAGE	RAM Window Select	0: Selects window 0 (receive rule entry registers, RAM test registers) 1: Selects window 1 (receive buffer, receive FIFO buffer, transmit/receive FIFO buffer, transmit buffer, transmit history data access register)	R/W
b15 to b1	—	Reserved	The write value should be 0.	R/W

RPAGE Bit (RAM Window Select)

This bit is used to select a window for the switching of registers that are allocated to addresses from 000A 83A0h to 000A 8681h.

[Registers allocated when the RPAGE bit is set to 0 (window 0 selected)]

- Receive rule entry registers: GAFLIDLj, GAFLIDHj, GAFLMLj, GAFLMHj, GAFLPLj, GAFLPHj (j = 0 to 15)
- RAM test registers: RPGACCr (r = 0 to 127)

[Registers allocated when the RPAGE bit is set to 1 (window 1 selected)]

- Receive buffer registers: RMIDLn, RMIDHn, RMTSn, RMPTRn, RMDF0n to RMDF3n (n = 0 to 15)
- Receive FIFO access registers: RFIDLm, RFIDHm, RFTSm, RFPTRm, RFDF0m to RFDF3m (m = 0, 1)
- Transmit/receive FIFO access registers: CFIDL0, CFIDH0, CFTS0, CFPTR0, CFDF00 to CFDF30
- Transmit buffer registers: TMIDLp, TMIDHp, TMPTRp, TMDF0p to TMDF3p (p = 0 to 3)
- Transmit history buffer access register: THLACC0

28.2.79 Global Test Configuration Register (GTSTCFG)

Address(es): RSCAN.GTSTCFG 000A 838Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	RTMPS[2:0]			—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b10 to b8	RTMPS[2:0]	RAM Test Page Configuration	Set a value within a range of page 0 (00h) to page 2 (02h).	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Modify the GTSTCFG register only in global test mode.

RTMPS[2:0] Bits (RAM Test Page Configuration)

These bits are used to set the RAM test target page number for RAM test. Set a value from 00h to 02h.

28.2.80 Global Test Control Register (GTSTCTRL)

Address(es): RSCAN.GTSTCTRL 000A 838Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	RTME	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b2	RTME	RAM Test Enable	0: RAM test is disabled. 1: RAM test is enabled.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

RTME Bit (RAM Test Enable)

Setting this bit to 1 enables RAM test. Modify this bit only in global test mode.

(1) Set the GCTRL.GMDC[1:0] bits to 10b (global test mode).
(2) Unlock protection by successively writing 7575h and 8A8Ah to the GLOCKK register
(3) Set the RTME bit to 1.
(4) Check that the RTME bit is set to 1.

28.2.81 Global Test Protection Unlock Register (GLOCKK)

Address(es): RSCAN.GLOCKK 000A 8394h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	LOCK[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	LOCK[15:0]	Protection Unlock Data	Write protection unlock data to use test functions. These bits are read as 0000h.	W

Modify the GLOCKK register only in global test mode.

LOCK[15:0] Bits (Protection Unlock Data)

Write the protection unlock data shown in Table 28.3 to the LOCK[15:0] bits in succession to allow writing 1 to the target bit.

Table 28.3 Protection Unlock Data for Test Functions

Test Function	Protection Unlock Data 1	Protection Unlock Data 2	Target Bit
RAM test	7575h	8A8Ah	GTSTCTRL.RTME bit

Writing data to the CAN's register area (000A 8300h to 000A 839Fh) except the RAM area after protection is unlocked enables protection again.
Protection is not enabled even by reading data from the CAN's register area or reading/writing data from/to other areas.

28.2.82 RAM Test Register r (RPGACCr) (r = 0 to 127)

Address(es): RSCAN.RPGACC0 to RSCAN.RPGACC127 000A 8580h to 000A 867Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RDTA[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Description	R/W
Data can be read and written in CAN RAM.	R/W

Modify the RPGACCr register in global test mode with the GTSTCTRL.RTME bit set to 1 (RAM test is enabled). The RPGACCr register is readable and writable when the GTSTCTRL.RTME bit is set to 1.
This register can be read/written when the GRWCR.RPAGE bit is 0.

28.3 CAN Modes

The CAN module has four global modes to control entire CAN module status and four channel modes to control individual channel status.

Details of global modes are described in section 28.3.1, Global Modes, and details of channel modes are described in section 28.3.2, Channel Modes.

- Global stop mode: Stops clocks of entire module to achieve low power consumption.
- Global reset mode: Performs initial settings for entire module.
- Global test mode: Performs test settings and performs RAM test.
- Global operating mode: Makes entire module operable.
- Channel stop mode: Stops channel clock.
- Channel reset mode: Performs initial settings for channels.
- Channel halt mode: Stops CAN communication and enables channel test.
- Channel communication mode: Performs CAN communication.

28.3.1 Global Modes

Figure 28.2 shows the transitions of global modes.

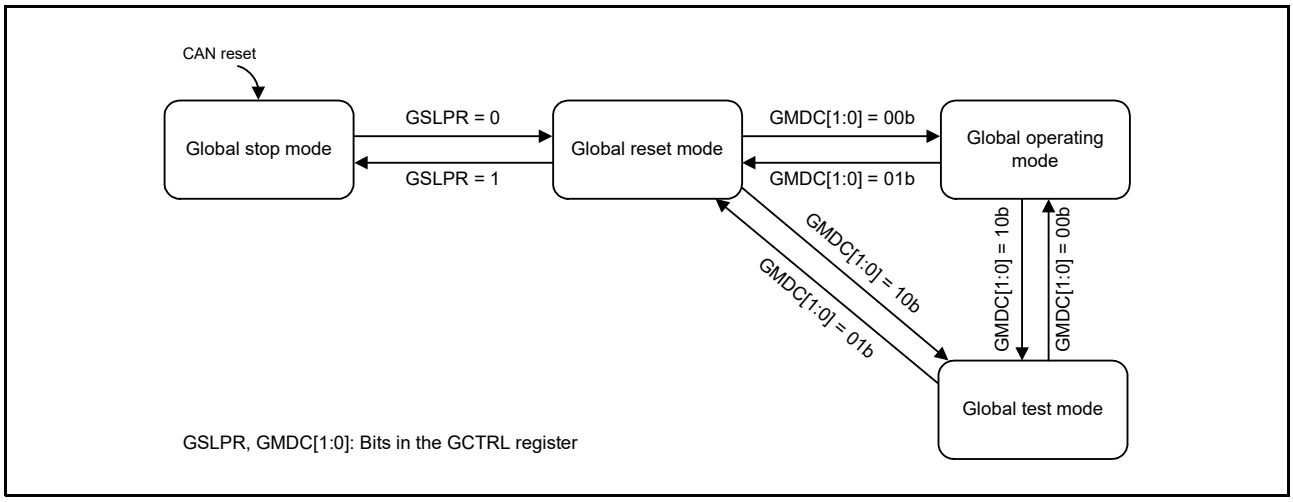


Figure 28.2 Transitions of Global Modes

Channel modes transition in some cases with transitions of global modes. Table 28.4 shows the transitions of channel modes depending on the global mode setting by the GCTRL.GMDC[1:0] bits and the GSLPR bit.

Table 28.4 Transitions of Channel Modes Depending on Global Mode Setting (GCTRL.GMDC[1:0] and GSLPR Bits)

	Channel Mode after Setting			
Channel Mode before Setting	**GMDC[1:0] = 00b GSLPR = 0 (Global Operation)**	**GMDC[1:0] = 10b GSLPR = 0 (Global Test)**	**GMDC[1:0] = 01b GSLPR = 0 (Global Reset)**	**GMDC[1:0] = 01b GSLPR = 1 (Global Stop)**
Channel communication	Channel communication	Channel communication	Channel reset	Transition prohibited
Channel halt	Channel halt	Channel halt	Channel reset	Transition prohibited
Channel reset	Channel reset	Channel reset	Channel reset	Channel stop
Channel stop	Channel stop	Channel stop	Channel stop	Channel stop

Table 28.5 shows the global mode transition time.

Table 28.5 Global Mode Transition Time

Mode before Transition	Mode after Transition	Maximum Transition Time
Global stop	Global reset	3 PCLK cycles
Global reset	Global stop	3 PCLK cycles
Global reset	Global test	10 PCLK cycles
Global reset	Global operating	10 PCLK cycles
Global test	Global reset	3 PCLK cycles
Global test	Global operating	3 PCLK cycles
Global operating	Global reset	3 PCLK cycles
Global operating	Global test	Two CAN frames

(1) Global Stop Mode

In global stop mode, clocks of the CAN do not run and therefore power consumption is reduced. CAN registers can be read, but writing data to them is prohibited. Register values are retained.
After the operation of the CAN module is enabled, the CAN module transitions to global stop mode. Setting the GCTRL.GSLPR bit to 1 (global stop mode) in global reset mode sets the CTRL.CSLPR bit to 1 (channel stop mode). If all channels are forcibly caused to transition to channel stop mode, the CAN module transitions to global stop mode. The GCTRL.GSLPR bit should not be modified in global operating mode and global test mode.

(2) Global Reset Mode

In global reset mode, CAN module settings are performed. When the CAN module transitions to global reset mode, some registers are initialized. Table 28.8 and Table 28.9 list the registers to be initialized.
Setting the GCTRL.GMDC[1:0] bits to 01b sets each of the CTRL.CHMDC[1:0] bits to 01b (channel reset mode). If all channels are forcibly caused to transition to channel reset mode, the CAN module transitions to global reset mode. Channels that are already in channel reset mode or channel stop mode do not transition (because the CTRL.CHMDC[1:0] bits have already been set to 01b).

(3) Global Test Mode

In global test mode, settings for test-related registers are performed. When the CAN module transitions to global test mode, all CAN communications are disabled.
Setting the GCTRL.GMDC[1:0] bits to 10b sets each of the CTRL.CHMDC[1:0] bits to 10b (channel halt mode). If all channels are forcibly caused to transition to channel halt mode, the CAN module transitions to global test mode. Channels that are in channel stop mode, channel reset mode, or channel halt mode do not transition.

(4) Global Operating Mode

In global operating mode, entire CAN module operates.
When the GCTRL.GMDC[1:0] bits are set to 00b, the CAN module transitions to global operating mode.

28.3.2 Channel Modes

Figure 28.3 shows a channel mode state transition chart. Table 28.6 shows the channel mode transition time.

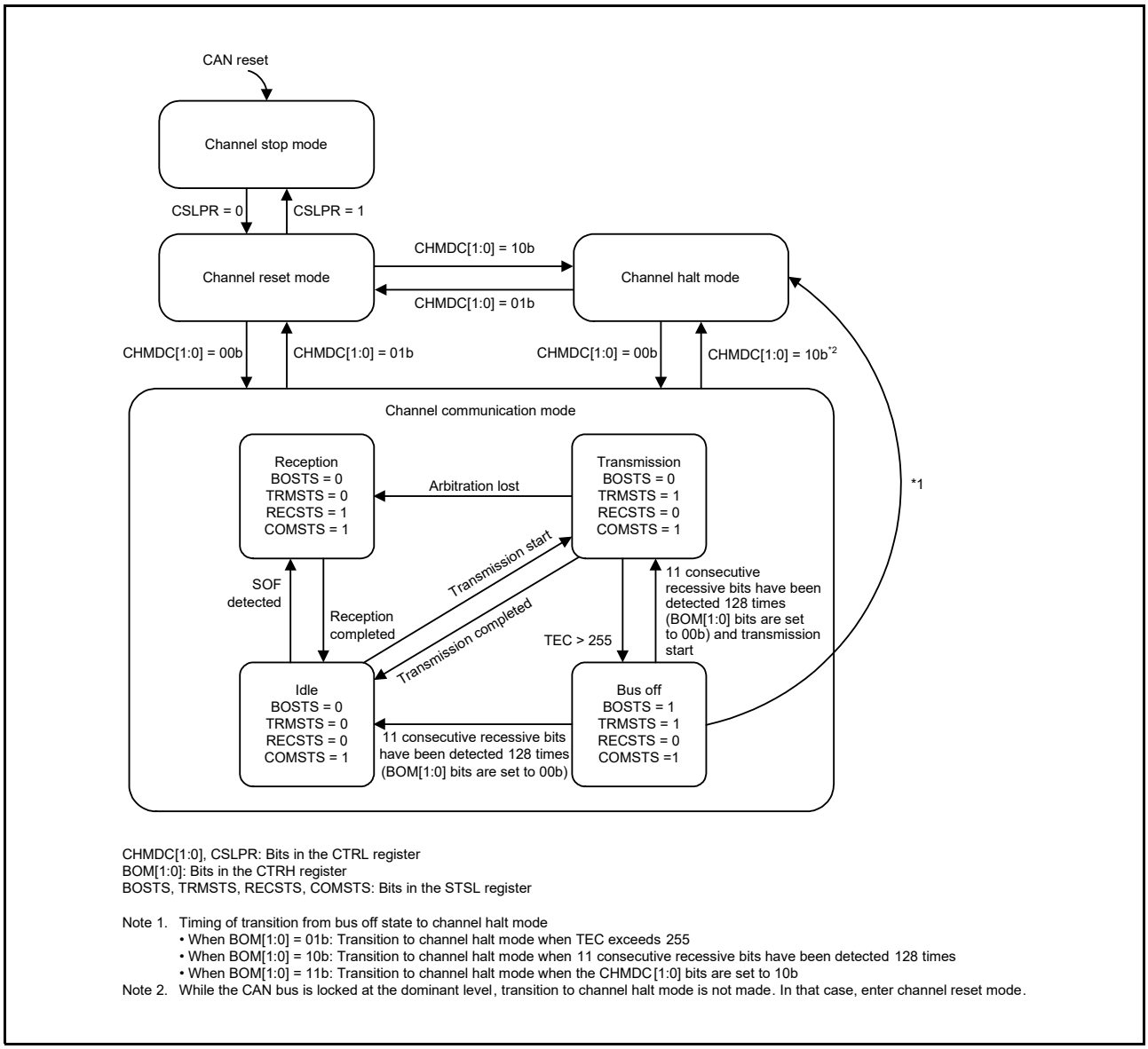


Figure 28.3 Channel Mode State Transition Chart

Table 28.6 Channel Mode Transition Time

Mode before Transition	Mode after Transition	Maximum Transition Time
Channel stop	Channel reset	3 PCLK cycles
Channel reset	Channel stop	3 PCLK cycles
Channel reset	Channel halt	3 CAN bit times
Channel reset	Channel communication	2 CAN bit times
Channel halt	Channel reset	3 PCLK cycles
Channel halt	Channel communication	3 CAN bit times
Channel communication	Channel reset	3 PCLK cycles
Channel communication	Channel halt	2 CAN frames

(1) Channel Stop Mode

In channel stop mode, clocks are not supplied to channels and therefore power consumption is reduced. CAN registers can be read, but writing data to them is prohibited. Register values are retained.
Each channel enters channel stop mode after the operation of the CAN module is enabled. The channel transitions to channel stop mode when the CTRL.CSLPR bit is set to 1 (channel stop mode) in channel reset mode.
The CSLPR bit should not be modified in channel communication mode and channel halt mode.

(2) Channel Reset Mode

In channel reset mode, channel settings are performed. When a channel transitions to channel reset mode, some channel-related registers are initialized. Table 28.8 lists the registers to be initialized.
When the CTRL.CHMDC[1:0] bits are set to 01b (channel reset mode) during CAN communication, communication is terminated before it is completed and the channel transitions to channel reset mode. Table 28.7 shows the operation when the CTRL.CHMDC[1:0] bits are set to 01b (channel reset mode) during CAN communication.

(3) Channel Halt Mode

In channel halt mode, settings for test-related registers of channels are performed. When a channel transitions to channel halt mode, CAN communication of the channel stops.
Table 28.7 shows operation when the CTRL.CHMDC[1:0] bits are set to 10b (channel halt mode) during CAN communication.

Table 28.7 Operation when a Channel Transitions to Channel Reset Mode/Channel Halt Mode

Mode	During Reception	During Transmission	Bus Off State
Channel reset (CHMDC[1:0] = 01b)	Transitions to channel reset mode before reception is completed.*1	Transitions to channel reset mode before transmission is completed.*1	Transitions to channel reset mode before bus off recovery.
Channel halt*3 (CHMDC[1:0] = 10b)	Transitions to channel halt mode after reception is completed.*2	Transitions to channel halt mode after transmission is completed.*2	[When BOM[1:0] = 00b] Transitions to channel halt mode (CHMDC[1:0] = 10b) only after bus off recovery. [When BOM[1:0] = 01b] Transitions to channel halt mode automatically when the condition for transition to bus off state is met. [When BOM[1:0] = 10b] Transitions to channel halt mode automatically after bus off recovery. [When BOM[1:0] = 11b] Transitions to channel halt mode immediately after the CHMDC[1:0] bits are set to 10b before bus off recovery.

Note 1. To allow transition to channel reset mode after communication is completed, set the CHMDC[1:0] bits to 10b and confirm that communication has been completed and transition to channel halt mode has been made, and then set the CHMDC[1:0] bits to 01b.
Note 2. While the CAN bus is locked at the dominant level, transition to channel halt mode is not made. In that case, enter channel reset mode. The CAN bus status can be confirmed with the ERFLL.BLF flag that becomes 1 when dominant lock is detected.
Note 3. In case of a transition from channel reset mode to channel halt mode, transition to channel halt mode after setting the CFGL and CFGH registers in channel reset mode.

(4) Channel Communication Mode

In channel communication mode, CAN communication is performed. Each channel has the following communication states during CAN communication.

- Idle: Neither reception nor transmission is in progress.
- Reception: Receiving a message sent from another node.
- Transmission: Transmitting a message.

- Bus off: Isolated from CAN communication.

When the CTRL.CHMDC[1:0] bits are set to 00b, the channel transitions to channel communication mode. After that, when 11 consecutive recessive bits have been detected, the STSL.COMSTS flag is set to 1 (communication is ready) and transmission and reception are enabled on the CAN network as an active node. At this time, transmission and reception of messages can be started.

(5) Bus Off State

A channel transitions to the bus off state according to the transmit/receive error counter increment/decrement rules of the ISO 11898-1 standard.

How to return from the bus off state is set by the CTRH.BOM[1:0] bits.

- When CTRH.BOM[1:0] = 00b:
  Bus off recovery is compliant with the ISO 11898-1 standard. After 11 consecutive recessive bits have been detected 128 times, a channel returns from the bus off state to the CAN communication ready state (error active state).
  At that time, the STSH.TEC[7:0] and STSH.REC[7:0] flags are initialized to 00h and the ERFLL.BORF flag is set to 1 (bus off recovery is detected). When the CTRL.CHMDC[1:0] bits are set to 10b (channel halt mode) in the bus off state, the channel transitions to channel halt mode after bus off recovery has been completed (11 consecutive recessive bits have been detected 128 times).
- When CTRH.BOM[1:0] = 01b:
  When a channel transitions to the bus off state, the CTRL.CHMDC[1:0] bits are set to 10b and the channel transitions to channel halt mode. At that time, the STSH.TEC[7:0] and STSH.REC[7:0] flags are initialized to 00h but the ERFLL.BORF flag is not set to 1.
- When CTRH.BOM[1:0] = 10b:
  When a channel has transitioned to the bus off state, the CTRL.CHMDC[1:0] bits are set to 10b. After bus off recovery has been completed (11 consecutive recessive bits have been detected 128 times), the channel transitions to channel halt mode. At that time, the STSH.TEC[7:0] and STSH.REC[7:0] flags are initialized to 00h and the ERFLL.BORF flag is set to 1.
- When CTRH.BOM[1:0] = 11b:
  When the CHMDC[1:0] bits are set to 10b in the bus off state, the channel transitions to channel halt mode before bus off recovery is completed. At that time, the STSH.TEC[7:0] and STSH.REC[7:0] flags are initialized to 00h but the ERFLL.BORF flag is not set to 1.
  However, the BORF flag becomes 1 if a CAN module transitions to error active state (by detecting 128 times of 11 consecutive recessive bits) before the CTRL.CHMDC[1:0] bits are set to 10b.

If the channel transitions to channel halt mode simultaneously when the program writes a value to the CTRL.CHMDC[1:0] bits, writing by the program takes precedence. An automatic transition to channel halt mode when the CTRH.BOM[1:0] bits are set to 01b or 10b is made only when the CTRL.CHMDC[1:0] bits are 00b (channel communication mode).

Furthermore, setting the CTRL.RTBO bit to 1 allows forcible return from the bus off state. As soon as the CTRL.RTBO bit is set to 1, the state changes to the error active state. After 11 consecutive recessive bits have been detected, the condition of CAN module becomes ready for communication. In this case, the ERFLL.BORF flag is not set to 1 and the STSH.TEC[7:0] and STSH.REC[7:0] flags are initialized to 00h. Write 1 to the CTRL.RTBO bit when the CTRH.BOM[1:0] value is 00b.

Table 28.8 Registers Initialized in Global Reset Mode or Channel Reset Mode

Register	Bit/Flag
CTRL	CHMDC[1:0]
CTRH	CTMS[1:0], CTME
STSL	CHLTSTS, EPSTS, BOSTS, TRMSTS, RECSTS, COMSTS
STSH	REC[7:0], TEC[7:0]
ERFLL	ADERR, B0ERR, B1ERR, CERR, AERR, FERR, SERR, ALF, BLF, OVLF, BORF, BOEF, EPF, EWF, BEF
ERFLH	CRCREG[14:0]
CFCCL0	When transmit/receive FIFO buffer is in transmit mode: CFE
CFSTS0	When transmit/receive FIFO buffer is in transmit mode: CFMC[5:0], CFTXIF, CFRXIF, CFMLT, CFFLL, CFEMP
TMCp	TMOM, TMTAR, TMTR
TMSTSp	TMTARM, TMTRM, TMTRF[1:0], TMTSTS
TMTRSTS	TMTRSTSp
TMTCSTS	TMTCSTSp
TMTASTS	TMTASTSp
THLCC0	THLE
THLSTS0	THLMC[3:0], THLIF, THLELT, THLFLL, THLEMP
GTINTSTS	THIF0, CFTIF0, TAIF0, TSIF0

Table 28.9 Registers Initialized Only in Global Reset Mode

Register	Bit/Flag
GSTS	GHLTSTS
GERFLL	THLES, MES, DEF
GTSC	TS[15:0]
RMND0	RMNSn
RFCCm	RFE
RFSTSm	RFMC[5:0], RFIF, RFMLT, RFFLL, RFEMP
CFCCL0	When transmit/receive FIFO buffer is in receive mode: CFE
CFSTS0	When transmit/receive FIFO buffer is in receive mode: CFMC[5:0], CFTXIF, CFRXIF, CFMLT, CFFLL, CFEMP
RFMSTS	RFmMLT
CFMSTS	CF0MLT
RFISTS	RFmIF
CFISTS	CF0IF
GTSTCFG	RTMPS[2:0]
GTSTCTRL	RTME

28.4 Reception Function

There are two reception types.

- Reception by receive buffers:
  Zero to 16 receive buffers can be shared by all channels. Since messages stored in receive buffers are overwritten at each reception, the latest receive data can always be read.
- Reception by receive FIFO buffers and transmit/receive FIFO buffers (receive mode):
  Two receive FIFO buffers can be shared by all channels and one dedicated transmit/receive FIFO buffer is provided for each channel. The FIFO buffers can hold the number of received messages set by the RFCCm.RFDC[2:0] bits and CFCCL0.CFDC[2:0] bits, and messages can be read sequentially from the oldest.

28.4.1 Data Processing Using the Receive Rule Table

Data processing using the receive rule table allows selected messages to be stored in the specified buffer. Data processing includes acceptance filter processing, DLC filter processing, routing processing, label addition processing, and mirror function processing.
Up to 16 receive rules can be registered per channel. If receive rules are not set, no message can be received. Figure 28.4 illustrates how receive rules are registered.

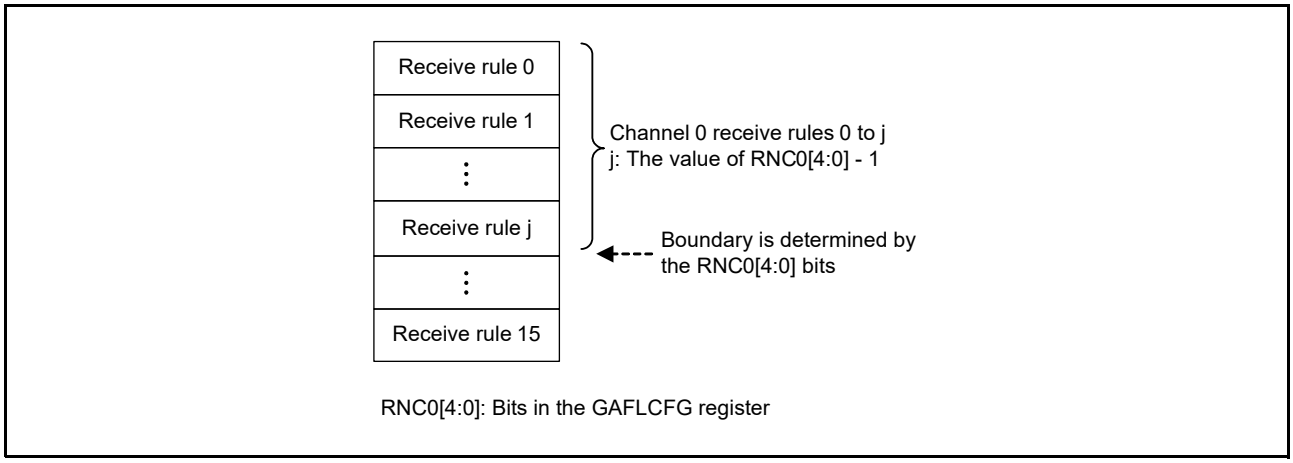


Figure 28.4 Entry of Receive Rules

Each receive rule consists of 12 bytes in the GAFLIDLj, GAFLIDHj, GAFLMLj, GAFLMHj, GAFLPLj, and GAFLPHj registers. The GAFLIDLj and GAFLIDHj registers are used to set ID, IDE bit, RTR bit, and the mirror function, the GAFLMLj and GAFLMHj registers are used to set mask, the GAFLPLj and GAFLPHj registers are used to set label information to be added, DLC value, and storage receive buffer, and storage FIFO buffer.

(1) Acceptance Filter Processing

In the acceptance filter processing, the ID data, IDE bit, and RTR bit in a received message are compared with the ID data, IDE bit, and RTR bit set in the receive rule of the corresponding channel. When all these bits match, the message passes through the acceptance filter processing. The ID data, IDE bit, and RTR bit in a received message which correspond to bits that are set to 0 (bits are not compared) in the GAFLMLj and GAFLMHj registers are not compared and are regarded as matched.
Check begins with the receive rule with the smallest rule number of the corresponding channel. When all the bits to be compared in a received message match the bits set in the receive rule or when all the receive rules are compared without any match, filter processing stops. If there is no matching receive rule, the received message is not stored in the receive buffer or FIFO buffer.

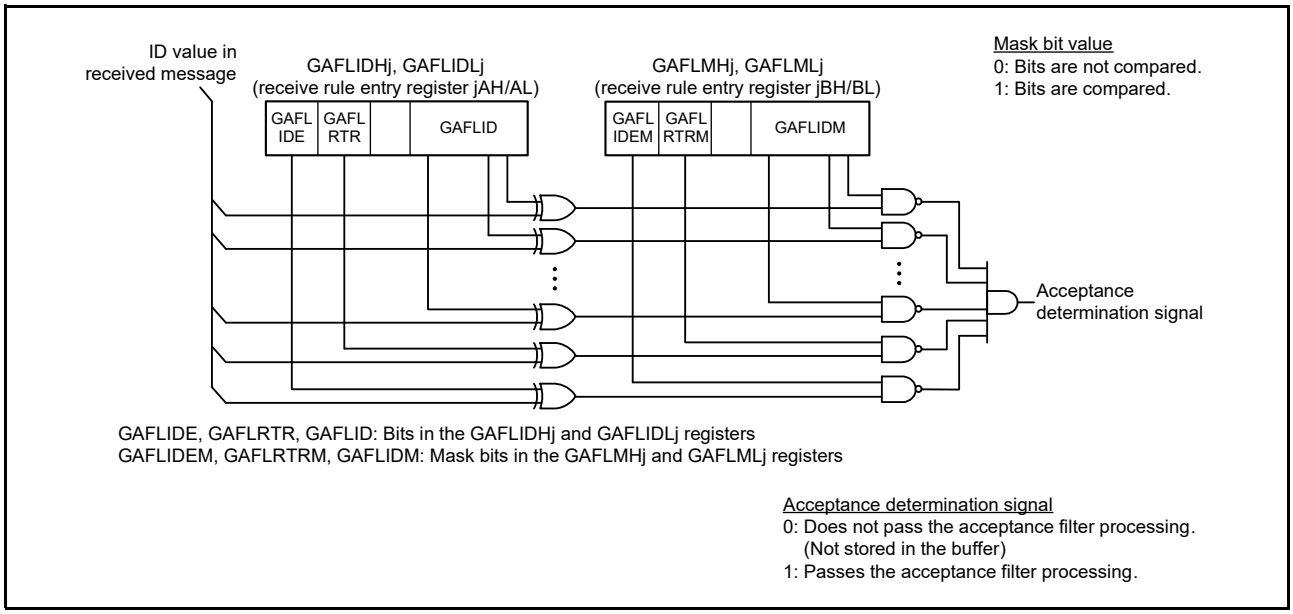


Figure 28.5 Acceptance Filter Function

(2) DLC Filter Processing

When the GCFGL.DCE bit is set to 1 (DLC check is enabled), DLC filter processing is added to messages that passed through the acceptance filter processing. When the DLC value in a message is equal to or larger than the DLC value set in the receive rule, the message passes through the DLC filter processing.

When a message has passed through the DLC filter processing with the GCFGL.DRE bit set to 0 (DLC replacement is disabled), the DLC value in the received message is stored in the buffer. In this case, all the data bytes in the received message are stored in the buffer.

When a message has passed through the DLC filter processing with the GCFGL.DRE bit set to 1 (DLC replacement is enabled), the DLC value in the receive rule is stored in the buffer instead of the DLC value in the received message. In this case, a value of 00h is written to data bytes that are larger than the DLC value in the receive rule.

When the DLC value in the received message is smaller than that in the receive rule, the message does not pass through the DLC filter processing. In this case, the message is not stored in the receive buffer or the FIFO buffer and the GERFLL.DEF flag is set to 1 (a DLC error is present).

(3) Routing Processing

Messages that passed through the acceptance filter processing and the DLC filter processing are stored in receive buffers, receive FIFO buffers, or transmit/receive FIFO buffers (set to receive mode). Message storage destination is set by the GAFLPLj.GAFLRMV, GAFLRMDP[6:0], GAFLFDP4, GAFLFDP1, and GAFLFDP0 bits. Messages that passed through the acceptance filter processing and the DLC filter processing can be stored in up to two buffers.

(4) Label Addition Processing

It is possible to add 12-bit label information to messages that passed through the filter processing and store them in buffers. This label information is set in the GAFLPHj.GAFLPTR[11:0] bits.

(5) Mirror Function Processing

The mirror function allows reception of messages transmitted from the own CAN node. The mirror function is made available by setting the GCFGL.MME bit to 1 (mirror function is enabled).

When the mirror function is in use, receive rules for which the GAFLIDHj.GAFLLB bit is set to 0 are used for data processing when receiving messages transmitted from other CAN nodes. When receiving messages transmitted from the own CAN node, receive rules for which the GAFLIDHj.GAFLLB bit is set to 1 are used for data processing.

28.4.2 Timestamp

The timestamp counter is a 16-bit free-running counter used for recording message receive time. The timestamp counter value is fetched at the start-of-frame (SOF) timing of a message and is then stored in a receive buffer or a FIFO buffer together with the message ID and data. PCLK or the CAN bit time clock is selectable as a timestamp counter clock source from the GCFGL.TSSS bit. The clock obtained by dividing the selected clock source by the GCFGL.TSP[3:0] value is used as the timestamp counter count source.
When the CAN bit time clock is used as a clock source, the timestamp counter stops when the corresponding channel transitions to channel reset mode or channel halt mode. When PCLK is used as a clock source, the timestamp function is not affected by channel mode.
The timestamp counter value is reset to 0000h by setting the GCTRH.TSRST bit to 1.

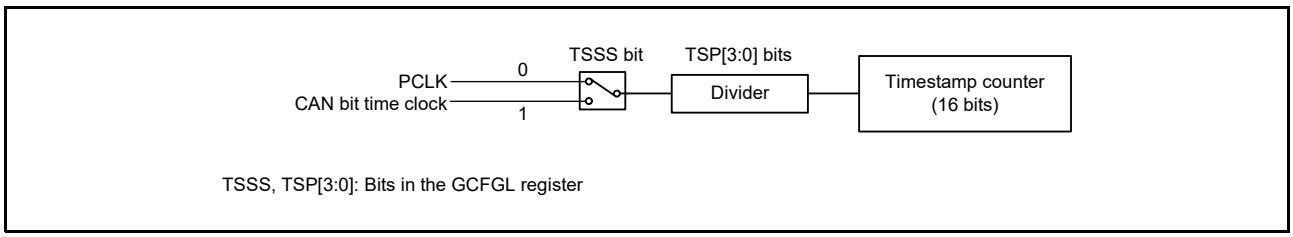


Figure 28.6 Timestamp Function Block Diagram

28.5 Transmission Functions

There are two types of transmission.

- Transmission using transmit buffers:
  Each channel has 4 buffers.
- Transmission using transmit/receive FIFO buffers (transmit mode):
  Each channel has one FIFO buffer. Up to 16 messages can be contained in a single FIFO buffer. Each FIFO buffer is used with a link to a transmit buffer. Only the message to be transmitted next in a FIFO buffer becomes the target of transmit priority determination. Messages are transmitted sequentially on a first-in, first-out basis.

Figure 28.7 shows the allocation of transmit/receive FIFO buffer link.

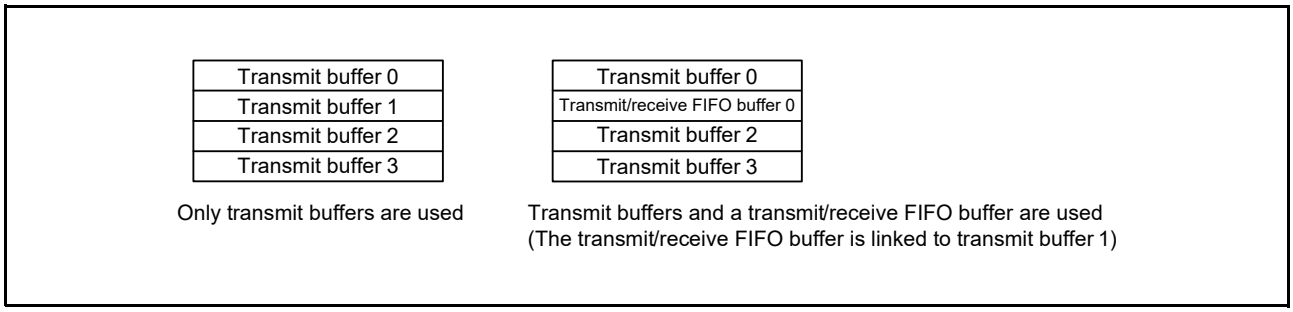


Figure 28.7 Allocation of Transmit/Receive FIFO Buffer Links

28.5.1 Transmit Priority Determination

If transmit requests are issued from multiple buffers in the same channel, transmit priority is determined.
The priority is determined by using one of the following methods.

- ID priority (GCFGL.TPRI bit = 0)
- Transmit buffer number priority (GCFGL.TPRI bit = 1)

The setting of the GCFGL.TPRI bit is enabled in all CAN channels.
When the GCFGL.TPRI bit is set to 0, messages are transmitted according to the priority of stored message IDs. Priority of IDs conforms to the CAN bus arbitration specification defined in the ISO 11898-1 standard. IDs of messages stored in transmit buffers and transmit/receive FIFO buffers (set to transmit mode) are targets of priority determination. When transmit/receive FIFO buffers are used, the oldest message in a FIFO buffer becomes the target of priority determination. When a message is being transmitted from a transmit/receive FIFO buffer, the next message in the FIFO buffer becomes the target of priority determination. When the GCFGL.TPRI bit is set to 1, the message in the transmit buffer of the minimum number among buffers with a transmit request is transmitted first. When transmit/receive FIFO buffers are linked to transmit buffers, transmit priority is determined according to linked transmit buffer numbers.
When messages are retransmitted due to an arbitration lost or an error, transmit priority determination is made again regardless of the GCFGL.TPRI bit setting.

28.5.2 Transmission Using Transmit Buffers

Setting the transmit request bit (TMCp.TMTR bit) in a transmit buffer to 1 (transmission is requested) allows transmission of data frames or remote frames.
Transmit result is shown by the corresponding TMSTSp.TMTRF[1:0] flags. When transmit completes successfully, the TMSTSp.TMTRF[1:0] flags are set to 10b (transmission has been completed (without transmit abort request)) or 11b (transmission has been completed (with transmit abort request)).

(1) Transmit Abort Function

With respect to transmit buffers for which the TMSTSp.TMTRM flag is set to 1 (a transmit request is present), when the TMCp.TMTAR bit is set to 1 (transmit abort is requested), the transmit request is canceled. When transmit abort is completed, the TMSTSp.TMTRF[1:0] flags are set to 01b (transmit abort has been completed) and the transmit request is canceled (the TMSTSp.TMTRM flag becomes 0).
A message that is being transmitted or a message to be transmitted next according to the transmit priority determination cannot be aborted. However, when an arbitration lost or an error has occurred while a message for which the TMCp.TMTAR bit is set to 1 is being transmitted, retransmission is not performed.

(2) One-Shot Transmission Function (Retransmission Disabling Function)

When the TMCp.TMOM bit is set to 1 (one-shot transmission is enabled), transmission is performed only once. Even if an arbitration lost or an error occurs, retransmission is not performed.
One-shot transmit result is shown by the corresponding TMSTSp.TMTRF[1:0] flags. When one-shot transmit completes successfully, the TMSTSp.TMTRF[1:0] flags are set to 10b or 11b. When an arbitration lost or an error has occurred, the TMSTSp.TMTRF[1:0] flags are set to 01b (transmit abort has been completed).

28.5.3 Transmission Using FIFO Buffers

Messages of a volume of the FIFO buffer depth set by the CFCCL0.CFDC[2:0] bits can be stored in a single transmit/receive FIFO buffer. Messages are transmitted sequentially on a first-in, first-out basis.
Transmit/receive FIFO buffers are linked to transmit buffers selected by the CFCCH0.CFTML[1:0] bits.
When the CFCCL0.CFE bit is set to 1 (transmit/receive FIFO buffers are used), transmit/receive FIFO buffers become targets of transmit priority determination. Priority determination is made for only the message to be transmitted next in a FIFO buffer.
When the CFCCL0.CFE bit is set to 0 (no transmit/receive FIFO buffer is used), the CFSTS0.CFEMP flag is set to 1 (the transmit/receive FIFO buffer contains no message (buffer empty)) at the timing below.

- The transmit/receive FIFO buffer becomes empty immediately when the message in it is not being transmitted or is not to be transmitted next.
- The transmit/receive FIFO buffer becomes empty after transmission completion, CAN bus error detection, or arbitration lost when the message in it is being transmitted or to be transmitted next.

When the CFCCL0.CFE bit is set to 0, all messages in transmit/receive FIFO buffers are lost and messages cannot be stored in FIFO buffers. Confirm that the CFSTS0.CFEMP flag is set to 1 before setting the CFCCL0.CFE bit to 1 again.

(1) Interval Transmission Function

To transmit messages from the same FIFO buffer while a transmit/receive FIFO buffer that is set to transmit mode is in use, message transmission interval time can be set.
Immediately after the first message has been transmitted successfully from the FIFO buffer with the CFCCL0.CFE bit set to 1, the interval timer starts counting (after EOF7 of the CAN protocol). After that, when the interval time has passed, the next message is transmitted. The interval timer stops in channel reset mode or by setting the CFCCL0.CFE bit to 0.
The interval time is set by the CFCCH0.CFITT[7:0] bits. When the interval timer is not used, set the CFCCH0.CFITT[7:0] bits to 00h.

Select an interval timer count source by the CFCCH0.CFITR and CFITSS bits. When the CFCCH0.CFITR and CFITSS bits are set to 00b, the clock obtained by frequency-dividing PCLK by the GCFGH.ITRCP[15:0] value is used as a count source. When the CFCCH0.CFITR and CFITSS bits are set to 10b, the clock obtained by frequency-dividing PCLK by the GCFGH.ITRCP[15:0] value × 10 is used as a count source. When the CFCCH0.CFITR and CFITSS bits are set to x1b, the CAN bit time clock is used as a count source.
The interval time is calculated by the following equations where M is the set GCFGH.ITRCP[15:0] value and N is the set CFCCH0.CFITT[7:0] value.

- When CFCCH0.CFITR and CFITSS = 00b

$$\frac{1}{PCLK} \times M \times N$$

- When CFCCH0.CFITR and CFITSS = 10b

$$\frac{1}{PCLK} \times M \times 10 \times N$$

- When CFCCH0.CFITR and CFITSS = x1b
(fCANBIT is CAN bit time clock frequency)

$$\frac{1}{fCANBIT} \times N$$

Figure 28.8 shows the interval timer block diagram.

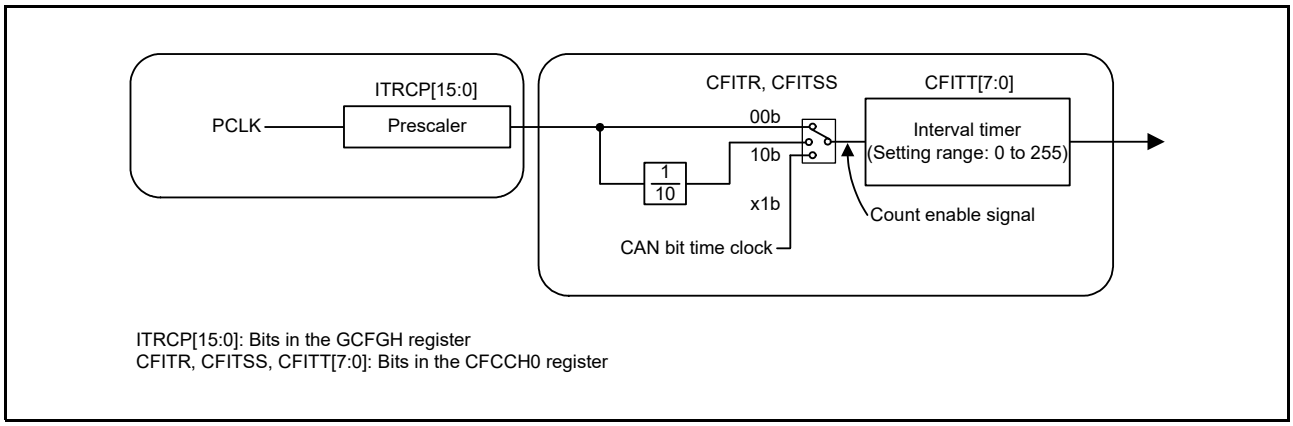


Figure 28.8 Interval Timer Block Diagram

Figure 28.9 shows the interval timer timing chart.

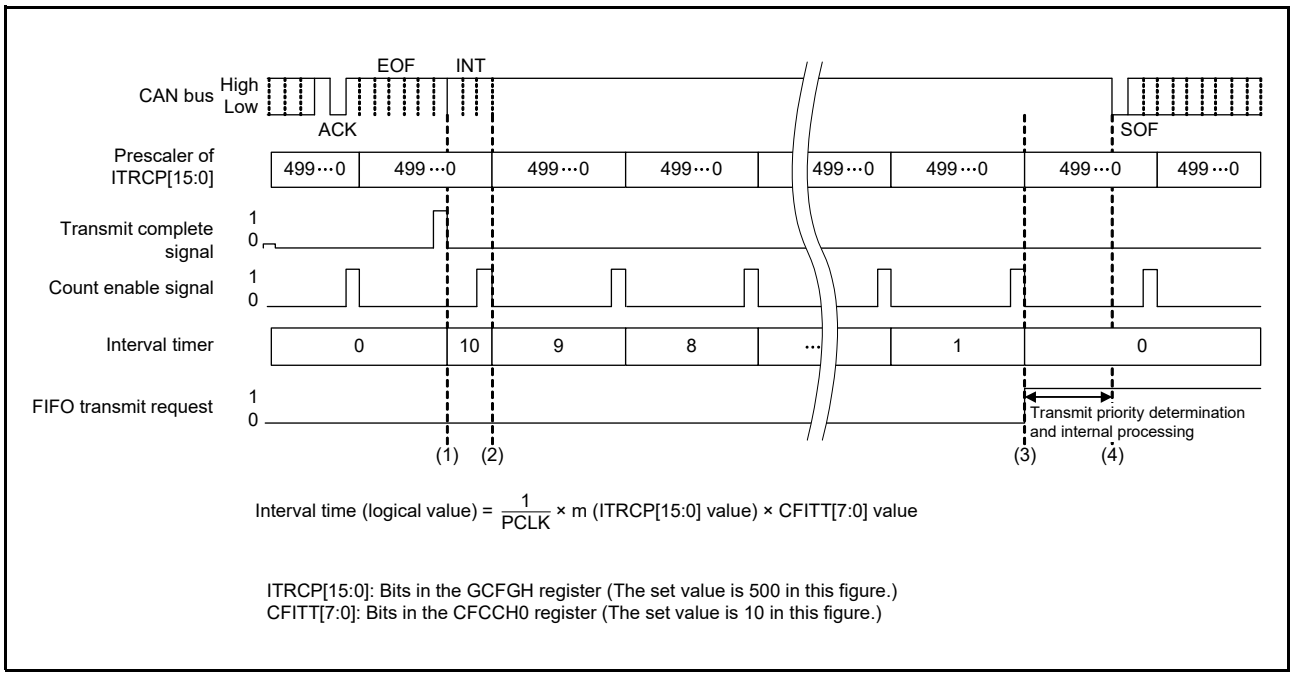


Figure 28.9 Interval Timer Timing Chart

(1) The interval timer starts counting upon completion of transmission. Since the prescaler is not initialized at the time of transmission completion, the first interval time contains an error of up to one count of the interval timer.
(2) The interval timer is decremented by the next count enable signal.
(3) When the interval timer has decreased to 0, the transmit/receive FIFO buffer issues a transmit request.
(4) The transmit/receive FIFO buffer is determined for the next transmission by the priority determination, it starts transmitting data. Transmission starts with a delay of three CAN bit time clock cycles or less from the issue of transmit request.

28.5.4 Transmit History Function

Information of transmitted messages can be stored in the transmit history buffer. Each channel has a single transmit history buffer that can contain 8 sets of transmit history data.
A message transmit source buffer type can be selected by the THLCC0.THLDTE bit. Whether to store transmit history data for each message can be set by the CFIDH0.THLEN bit.
After transmit completes successfully, information of the following transmit messages is stored in the transmit history buffer as transmit history data. After successful completion of transmit, process may be delayed by up to 38 clocks of PCLK before the transmit history data is stored.

- Buffer type 01b: Transmit buffer
  10b: Transmit/receive FIFO buffer
- Buffer number Number of source transmit buffer or transmit/receive FIFO buffer.
  This number depends on buffer types. See Table 28.10.
- Label data Label information of transmit message

Table 28.10 Transmit History Data Buffer Numbers

Buffer Number	Buffer Type	
	01b	10b
00b	Transmit buffer 0	Numbers of transmit buffers linked to transmit/receive FIFO buffers by the CFCCH0.CFTML[1:0] bits.
01b	Transmit buffer 1	
10b	Transmit buffer 2	
11b	Transmit buffer 3	

Label data is used to identify each message. A unique label data can be added to each message transmitted from a transmit buffer or transmit/receive FIFO buffer.
Transmit history data can be read from the THLACC0 register. If it is attempted to store new transmit history data while the buffer is full, the buffer overflows and the new data is discarded.

28.6 Test Function

The test function is classified into communication tests and global tests.
Communication tests: Performed for each channel.

- Standard test mode
- Listen-only mode
- Self-test mode 0 (external loopback mode)
- Self-test mode 1 (internal loopback mode)
  Global tests: Performed in entire module
- RAM test (read/write test)

28.6.1 Standard Test Mode

Standard test mode allows CRC test.

28.6.2 Listen-Only Mode

Listen-only mode allows reception of data frames and remote frames. Only recessive bits are transmitted on the CAN bus, and the ACK bit, overload flag, and active error flag are not transmitted. Listen-only mode is available for detecting the communication speed.
Do not make a transmit request from any buffer in listen-only mode.
Figure 28.10 shows the connection when listen-only mode is selected.

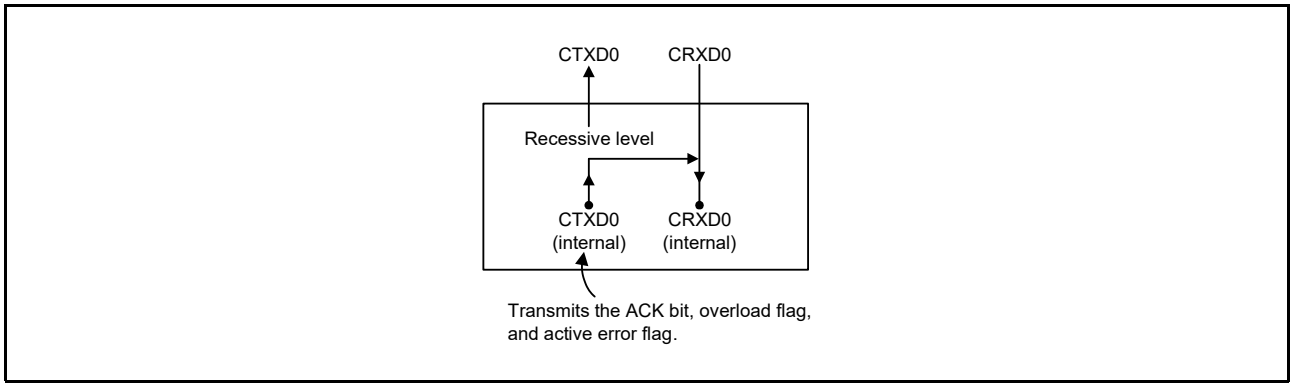


Figure 28.10 Connection When Listen-Only Mode is Selected

28.6.3 Self-Test Mode (Loopback Mode)

In self-test mode, transmitted messages are compared with the receive rule of the own channel and the messages are stored in a buffer if they have passed through the filter processing. Messages transmitted from other CAN nodes are compared only with the receive rule for which the GAFLIDHj.GAFLLB bit is set to 0 (when a message transmitted from another CAN node is received).
If the mirror function and self-test mode are both enabled, the self-test mode setting takes precedence.

(1) Self-Test Mode 0 (External Loopback Mode)

Self-test mode 0 is used to perform a loopback test within a channel including the CAN transceiver.
In self-test mode 0, transmitted messages are handled as messages received through the CAN transceiver and are stored in a buffer. An ACK bit is generated to receive messages transmitted from the own CAN node.
Figure 28.11 shows the connection when self-test mode 0 is selected.

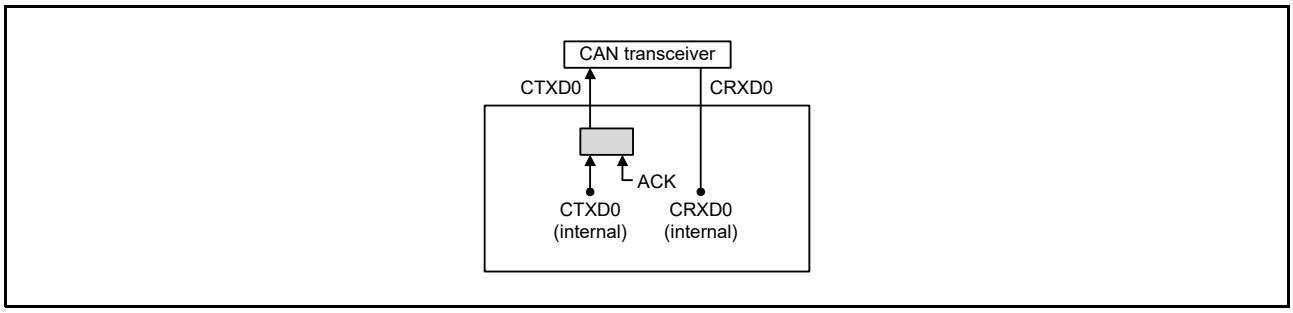


Figure 28.11 Connection When Self-Test Mode 0 is Selected

(2) Self-Test Mode 1 (Internal Loopback Mode)

In self-test mode 1, transmitted messages are handled as received messages and are stored in a buffer. An ACK bit is generated to receive messages transmitted from the own CAN node.
In self-test mode 1, internal feedback from the internal CTXD0 pin to the internal CRXD0 pin is performed. The external CRXD0 pin input is isolated. The external CTXD0 pin outputs only recessive bits.
Figure 28.12 shows the connection when self-test mode 1 is selected.

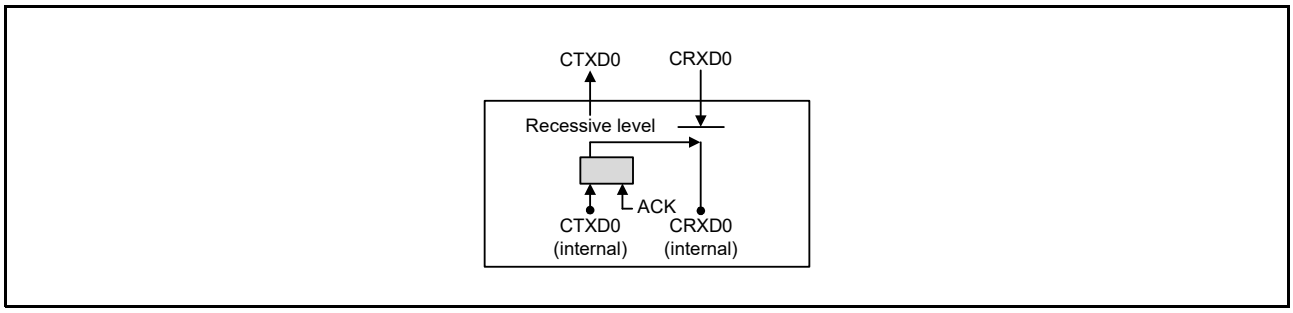


Figure 28.12 Connection When Self-Test Mode 1 is Selected

28.6.4 RAM Test

The RAM test function allows accesses to all CAN RAM addresses.
When the RAM test function is used, the RAM is divided into pages of 256 bytes each. RAM test page is set by the GTSTCFG.RTMPS[2:0] bits. Data in the set page can be read from and written to the RPGACCr register. The available total RAM size is 544 bytes (0220h).

28.7 Interrupt

The CAN module has 5 interrupts that are grouped into global interrupts and channel interrupts.

Global interrupts (2 interrupts):

- Global receive FIFO interrupt (RXINT)
- Global error interrupt (GLERRINT)

Channel interrupts (3 interrupts per channel):

- Channel transmit interrupt (TXINT)
  - Transmit complete interrupt
  - Transmit abort interrupt
  - Transmit/receive FIFO transmit complete interrupt (transmit mode)
  - Transmit history interrupt
- Transmit/receive FIFO receive interrupt (COMFRXINT)
- Channel error interrupt (CHERRINT)

When an interrupt request is generated, the corresponding CAN module interrupt request flag is set to 1 (interrupt request present). In that case, when the interrupt enable bit is set to 1 (enabling interrupts), an interrupt request is output from the CAN module. (Generation of interrupts also is controlled by the interrupt function.)
Setting the interrupt request flag to 0 (no interrupt request present) or setting the interrupt enable bit to 0 (disabling interrupts) clears the current interrupt request. The next interrupt request is not generated until the interrupt request is cleared.

For details on the setting of the interrupt functions, refer to section 14, Interrupt Controller (ICUb).
In the following pages, Table 28.11 lists the CAN interrupt sources, Figure 28.13 shows the CAN global interrupt block diagram, and Figure 28.14 shows the CAN channel interrupt block diagram.

Table 28.11 List of CAN Interrupt Sources

Item	Interrupt Source		Corresponding Interrupt Request Flag*1	Corresponding Interrupt Enable Bit *1
Global interrupts	Global receive FIFO	Receive FIFO 0	RFSTS0.RFIF	RFCC0.RFIE
		Receive FIFO 1	RFSTS1.RFIF	RFCC1.RFIE
	Global error		GERFLL.DEF	GCTRL.DEIE
			GERFLL.MES	GCTRL.MEIE
			GERFLL.THLES	GCTRL.THLEIE
Channel interrupts	Channel transmit	Transmit complete	TMSTSp.TMTRF[1:0]	TMIEC.TMIEp
		Transmit abort	TMSTSp.TMTRF[1:0]	CTRH.TAIE
		Transmit/receive FIFO transmit	CFSTS0.CFTXIF	CFCCL0.CFTXIE
		Transmit history	THLSTS0.THLIF	THLCC0.THLIE
	Transmit/receive FIFO receive		CFSTS0.CFRXIF	CFCCL0.CFRXIE
	Channel error		ERFLL.BEF	CTRL.BEIE
			ERFLL.ALF	CTRL.ALIE
			ERFLL.BLF	CTRL.BLIE
			ERFLL.OVLF	CTRL.OLIE
			ERFLL.BORF	CTRL.BORIE
			ERFLL.BOEF	CTRL.BOEIE
			ERFLL.EPF	CTRL.EPIE
			ERFLL.EWF	CTRL.EWIE
	Wakeup		None	None

Note 1. For details on the interrupt request flags and interrupt enable bits, refer to section 15, Interrupt Controller (ICUb).

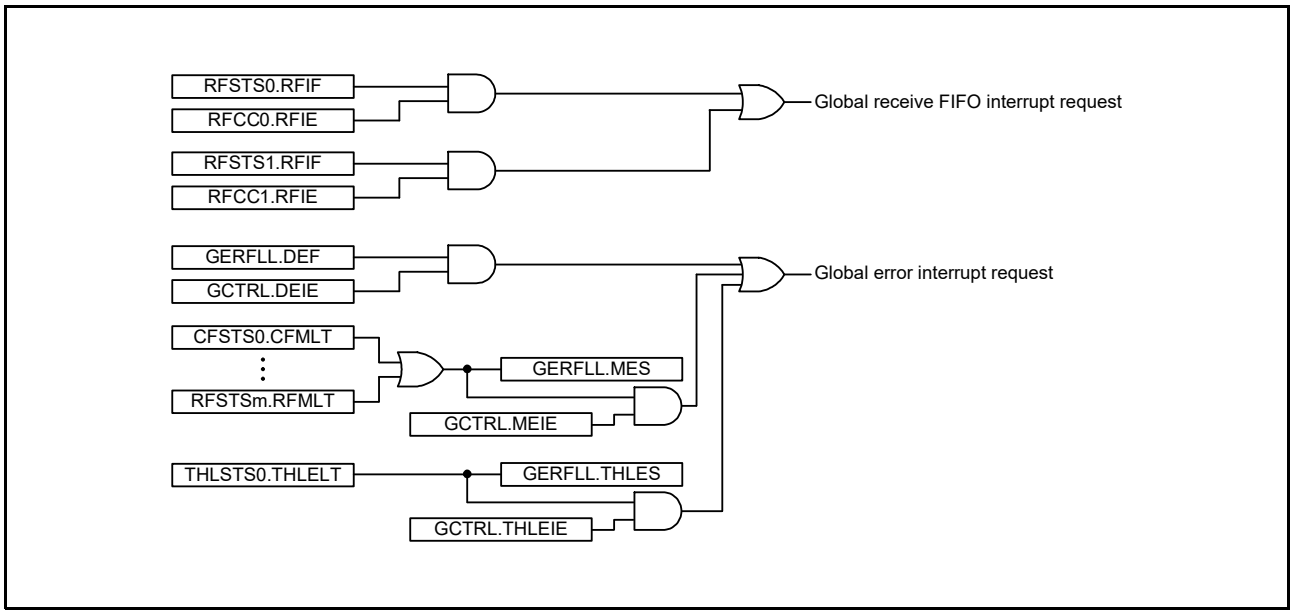


Figure 28.13 CAN Global Interrupt Block Diagram

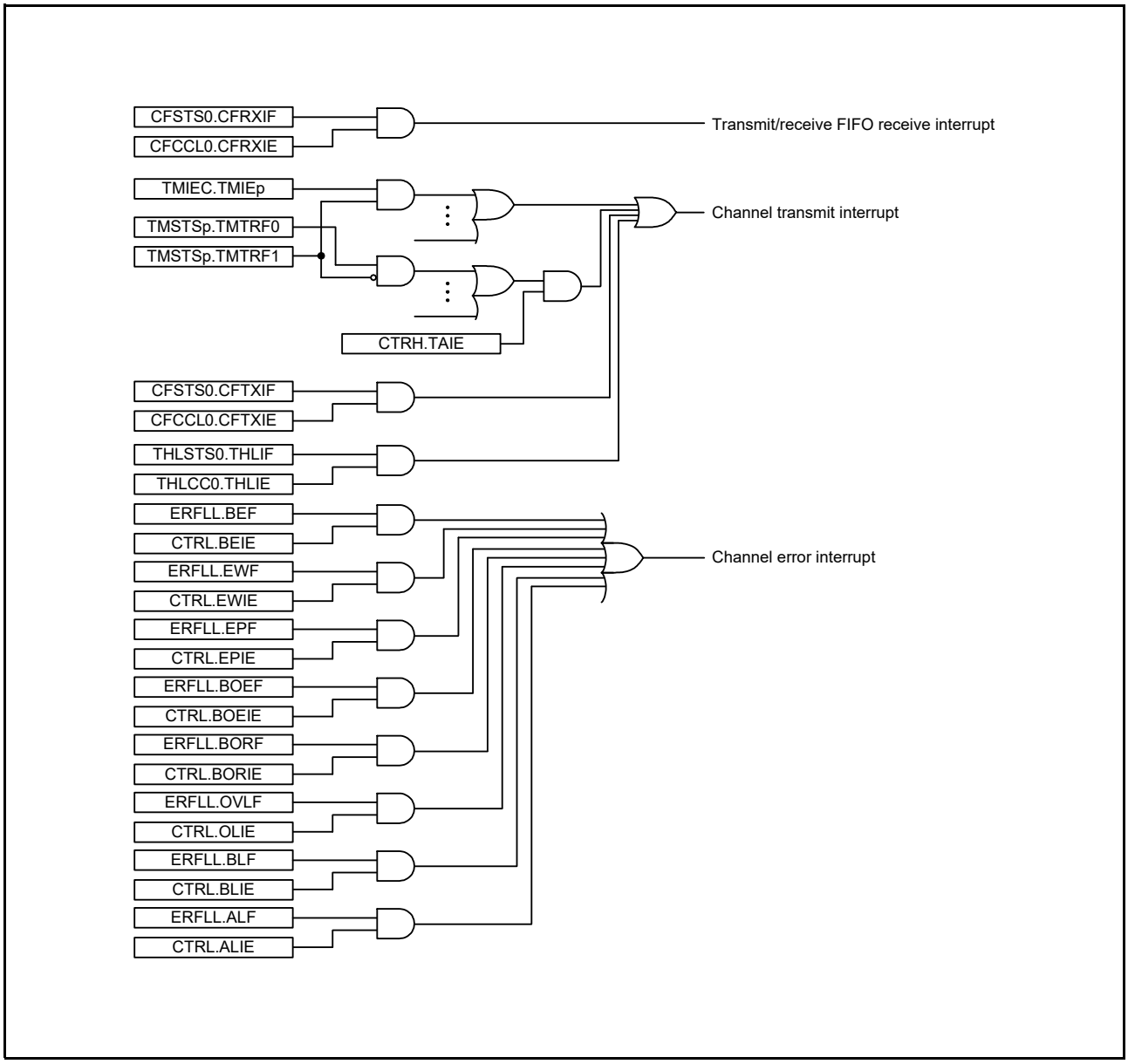


Figure 28.14 CAN Channel Interrupt Block Diagram

28.8 RAM Window

The CAN area from 000A 83A0h to 000A 8681h consists of two windows. The GRWCR.RPAGE bit is used to switch the allocation of registers.

- Registers allocated when the GRWCR.RPAGE bit is set to 0 (window 0 selected)
  Receive rule entry registers: GAFLIDLj, GAFLIDHj, GAFLMLj, GAFLMHj, GAFLPLj, GAFLPHj
  RAM test registers: RPGACCr

- Registers allocated when the GRWCR.RPAGE bit is set to 1 (window 1 selected)
  Receive buffer registers: RMIDLn, RMIDHn, RMTSn, RMPTRn, RMDF0n to RMDF3n
  Receive FIFO access registers: RFIDLm, RFIDHm, RFTSm, RFPTRm, RFDF0m to RFDF3m
  Transmit/receive FIFO access registers: CFIDL0, CFIDH0, CFTS0, CFPTR0, CFDF00 to CFDF30
  Transmit buffer registers: TMIDLp, TMIDHp, TMPTRp, TMDF0p to TMDF3p
  Transmit history buffer access register: THLACC0

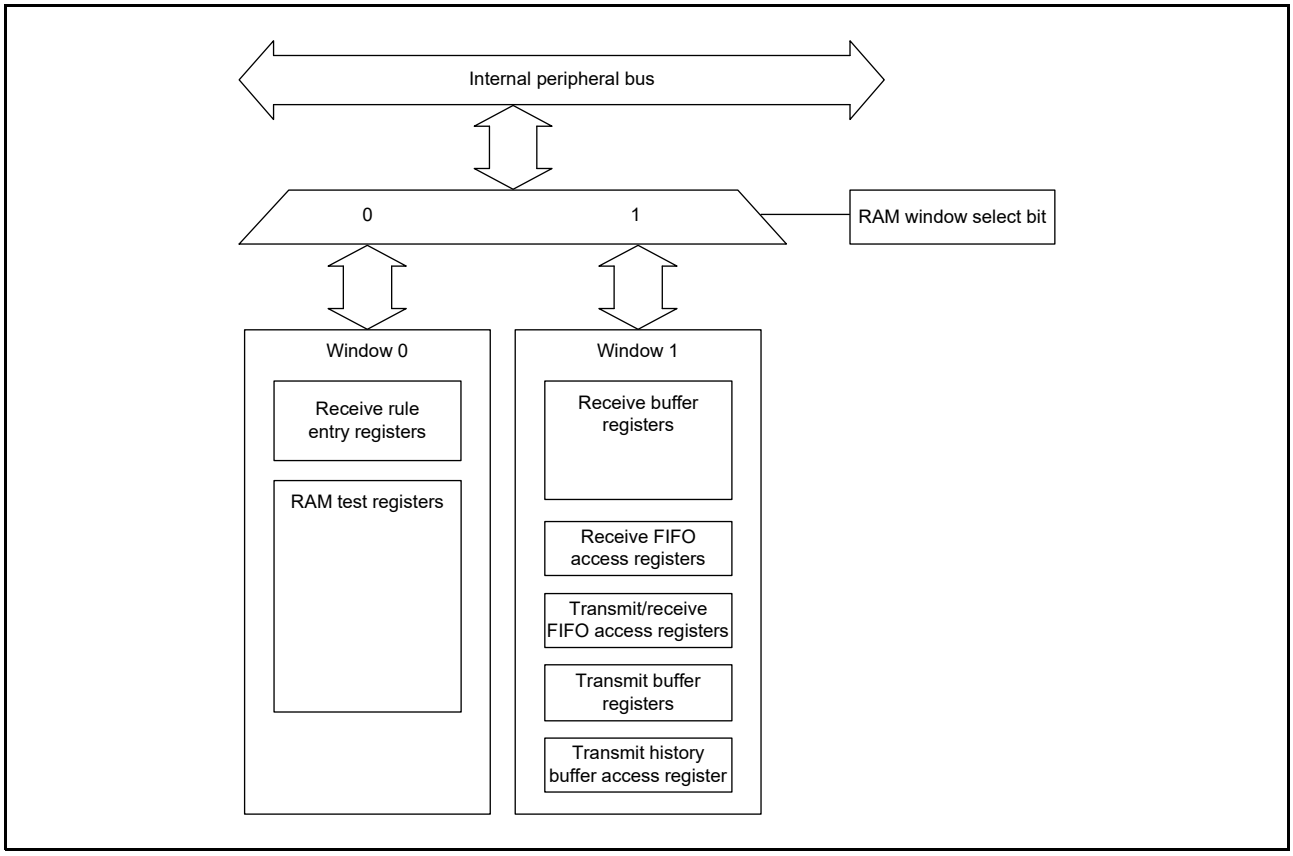
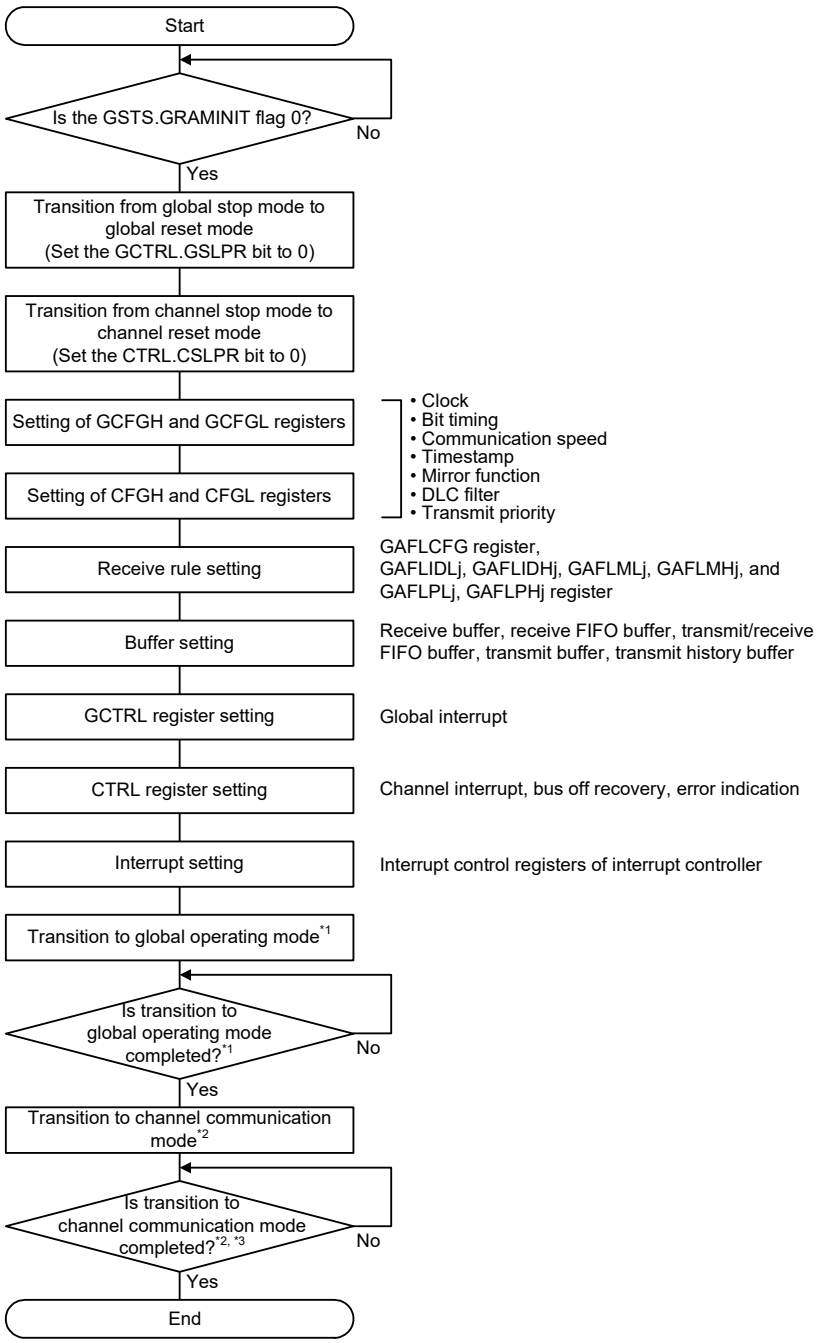


Figure 28.15 RAM Window

28.9 Initial Settings

The CAN module initializes the CAN RAM after the operation of the CAN module is enabled. The RAM initialization time is 276 cycles of PCLK. The GSTS.GRAMINIT flag is set to 1 (CAN RAM initialization is ongoing) during the RAM initialization and is set to 0 (CAN RAM initialization is finished) when the initialization is completed. Make CAN settings after the GSTS.GRAMINIT flag is set to 0.

Figure 28.16 shows the CAN setting procedure after the operation of the CAN module is enabled.



Note 1. When global mode is changed by the GCTRL.GSLPR and GMDC[1:0] bits, use the GSTS register to confirm that the mode is switched. Do not modify the GCTRL.GMDC[1:0] bits until the mode is switched.

Note 2. When channel mode is changed by the CTRL.CSLPR and CHMDC[1:0] bits, use the STSL register to confirm that the mode is switched. Do not modify the CTRL.CHMDC[1:0] bits until the mode is switched.

Note 3. After the channel transitions to channel communication mode, when 11 consecutive recessive bits have been detected, communication is ready (the STSL.COMSTS flag is set to 1) and transmission and reception are enabled on the CAN network as an active node. At this time, transmission and reception of messages can be started.

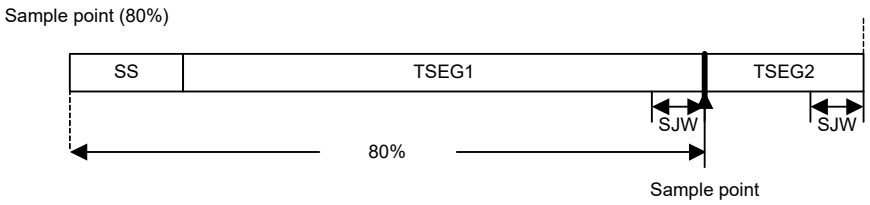
Figure 28.16 CAN Setting Procedure after the Operation of the CAN Module is Enabled

28.9.1 Clock Setting

Set the CAN clock source (fCAN) as a clock source of the CAN module. Select PCLK or CANMCLK with the GCFGL.DCS bit.

28.9.2 Bit Timing Setting

In the CAN protocol, one bit of a communication frame consists of three segments, SS, TSEG1, and TSEG2. Two of the segments, TSEG1 and TSEG2, can be set by the CFGH register for each channel. Sample point timing can be determined by setting two segments. This timing can be adjusted in units of 1 Time Quantum (referred to as Tq hereinafter). 1 Tq equals to one CAN Tq clock cycle. The CAN Tq clock is obtained by selecting the clock source with the GCFGL.DCS bit and selecting the clock division ratio with the CFGL.BRP[9:0] bits.
Figure 28.17 shows the bit timing chart. Table 28.12 shows an example of bit timing setting.



SS = 1 Tq fixed
Set TSEG1 to a range of 4 Tq to 16 Tq.
Set TSEG2 to a range of 2 Tq to 8 Tq.
Set SJW to a range of 1 Tq to 4 Tq.
Set SS + TSEG1 + TSEG2 to a range of 8 Tq to 25 Tq.
TSEG1 > TSEG2 ≥ SJW

- SS (synchronization segment):
  The SS is a segment that performs synchronization by monitoring the edge from recessive to dominant bits in the Interframe Space.
  Interframe Space consists of Intermission, Suspend Transmission, and Bus Idle. All nodes can start transmission during Bus Idle.
- TSEG1 (time segment 1):
  TSEG1 is a segment that absorbs physical delay on the CAN network. The physical delay on the CAN network is twice of the total of the delay on the CAN bus, the delay in the input comparator, and the delay in the output driver.
- TSEG2 (time segment 2):
  TSEG2 is a segment that compensates phase error due to an error in frequency.
- SJW (resynchronization jump width)
  The SJW is a length to extend or reduce time segment to compensate an error in phase due to phase error.

Figure 28.17 Bit Timing Chart

Table 28.12 Example of Bit Timing Setting

1 Bit	Set Value (Tq)				Sample Point (%) Note: See Figure 28.17
	SS	TSEG1	TSEG2	SJW	
8 Tq	1	4	3	1	62.50
	1	5	2	1	75.00
10 Tq	1	6	3	1	70.00
	1	7	2	1	80.00
16 Tq	1	10	5	1	68.75
	1	11	4	1	75.00
20 Tq	1	13	6	1	70.00
	1	15	4	3	80.00
24 Tq	1	15	8	1	66.67
	1	16	7	1	70.83

28.9.3 Communication Speed Setting

Set the CAN communication speed for each channel using the fCAN, baud rate prescaler division value (CFGL.BRP[9:0] bits), and Tq count per bit time.

Figure 28.18 shows the CAN clock control block diagram, and Table 28.13 shows an example of the communication speed setting.

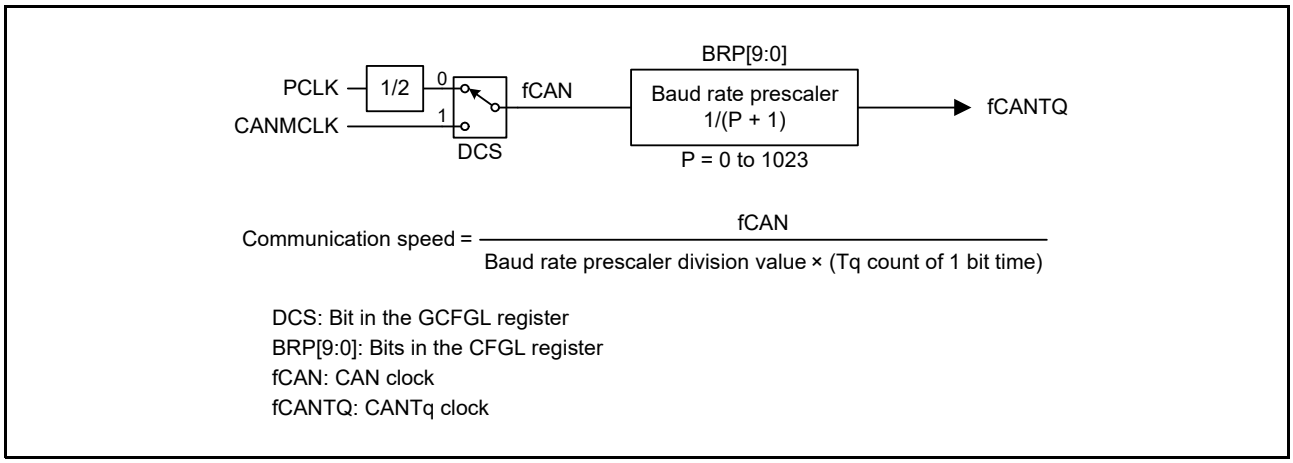


Figure 28.18 CAN Clock Control Block Diagram

Table 28.13 Example of Communication Speed Setting

	fCAN	
Communication Speed	**16 MHz**	**8 MHz**
1 Mbps	8 Tq (2) 16 Tq (1)	8 Tq (1)
500 kbps	8 Tq (4) 16 Tq (2)	8 Tq (2) 16 Tq (1)
250 kbps	8 Tq (8) 16 Tq (4)	8 Tq (4) 16 Tq (2)
83.3 kbps	8 Tq (24) 16 Tq (12)	8 Tq (12) 16 Tq (6)
33.3 kbps	8 Tq (60) 10 Tq (48) 16 Tq (30) 20 Tq (24)	8 Tq (30) 10 Tq (24) 16 Tq (15) 20 Tq (12)

Note: Values in ( ) are baud rate prescaler division values.

28.9.4 Receive Rule Setting

Receive rules can be set using receive rule-related registers.
Up to 16 receive rules can be registered.
Figure 28.19 shows the receive rule setting procedure.

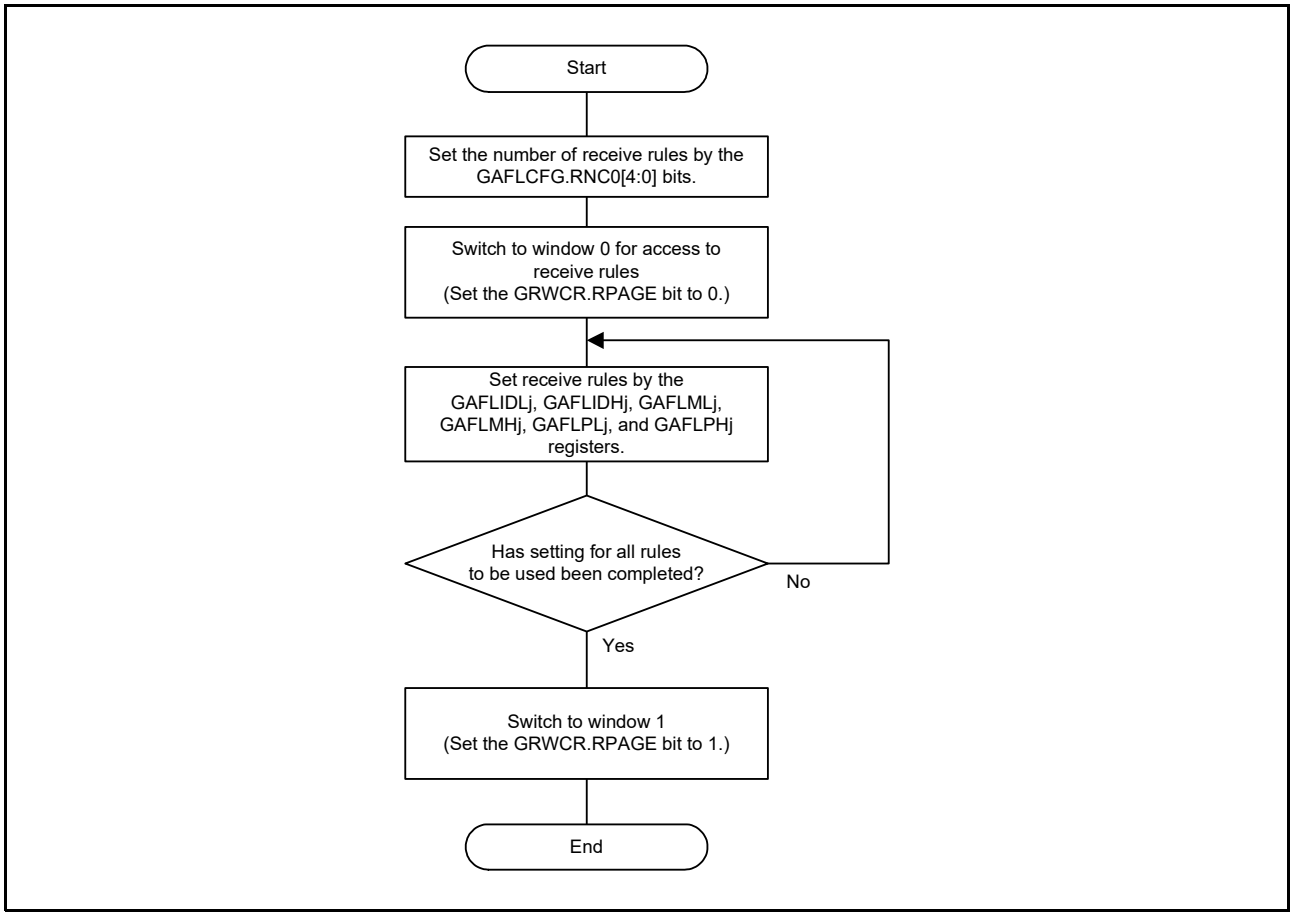


Figure 28.19 Receive Rule Setting Procedure

28.9.5 Buffer Setting

Set sizes and interrupt sources of buffers. For transmit/receive FIFO buffers that are set to transmit mode, set transmit buffers to be linked.

Figure 28.20 shows the buffer configuration. Figure 28.21 shows the buffer setting procedure.

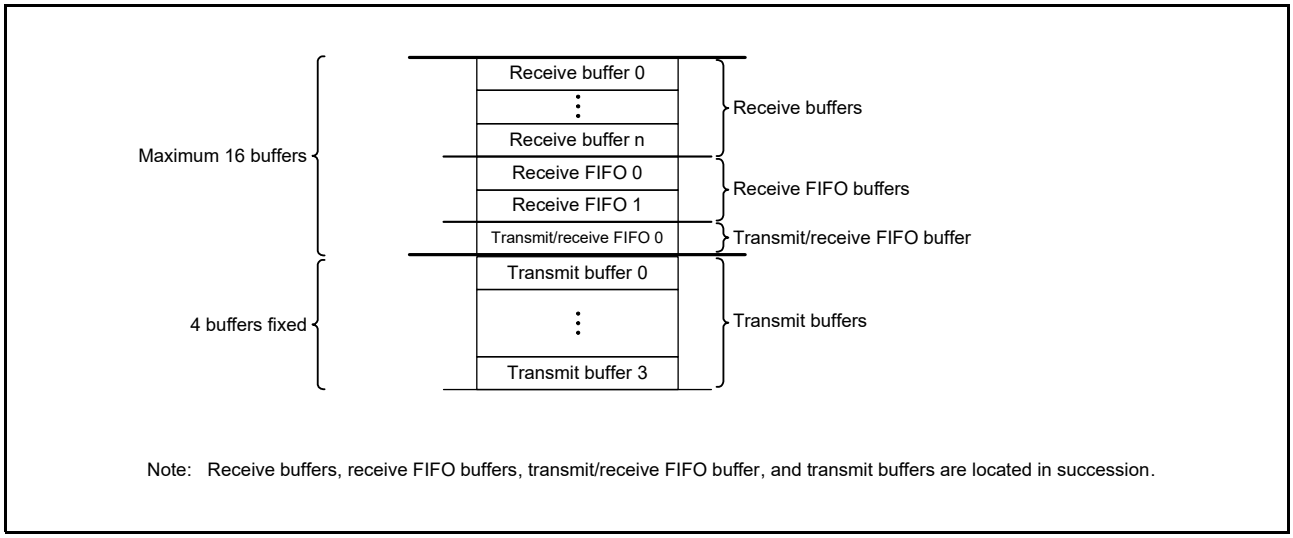


Figure 28.20 Buffer Configuration

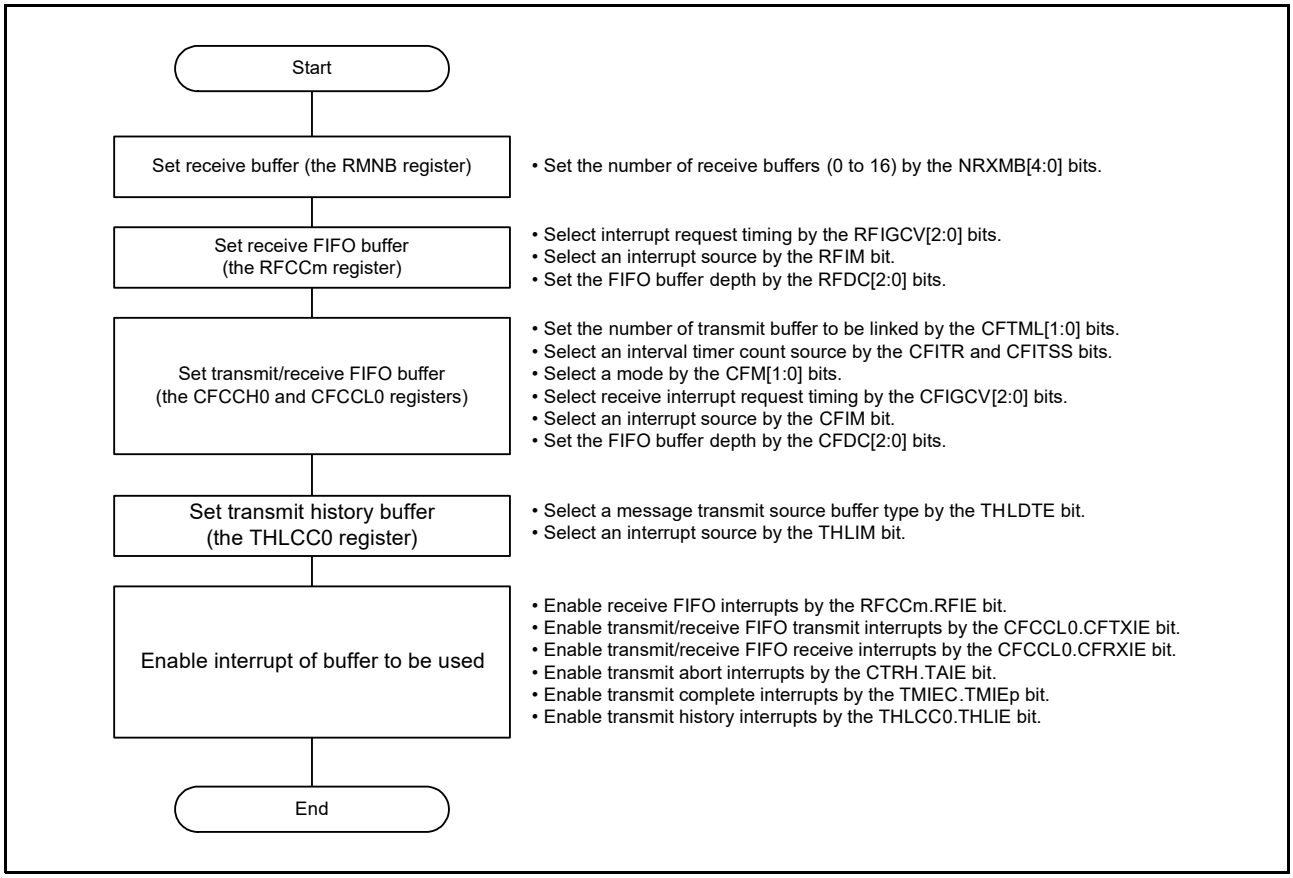


Figure 28.21 Buffer Setting Procedure

28.10 Reception Procedure

28.10.1 Receive Buffer Reading Procedure

When the processing to store received messages in a receive buffer starts, the RMND0.RMNSn flag is set to 1 (receive buffer n contains a new message). Messages can be read from the RMIDLn, RMIDHn, RMTSn, RMPTRn, and RMDF0n to RMDF3n registers. If the next message has been received before the current message is read from the receive buffer, the message is overwritten. Figure 28.22 shows the receive buffer reading procedure.

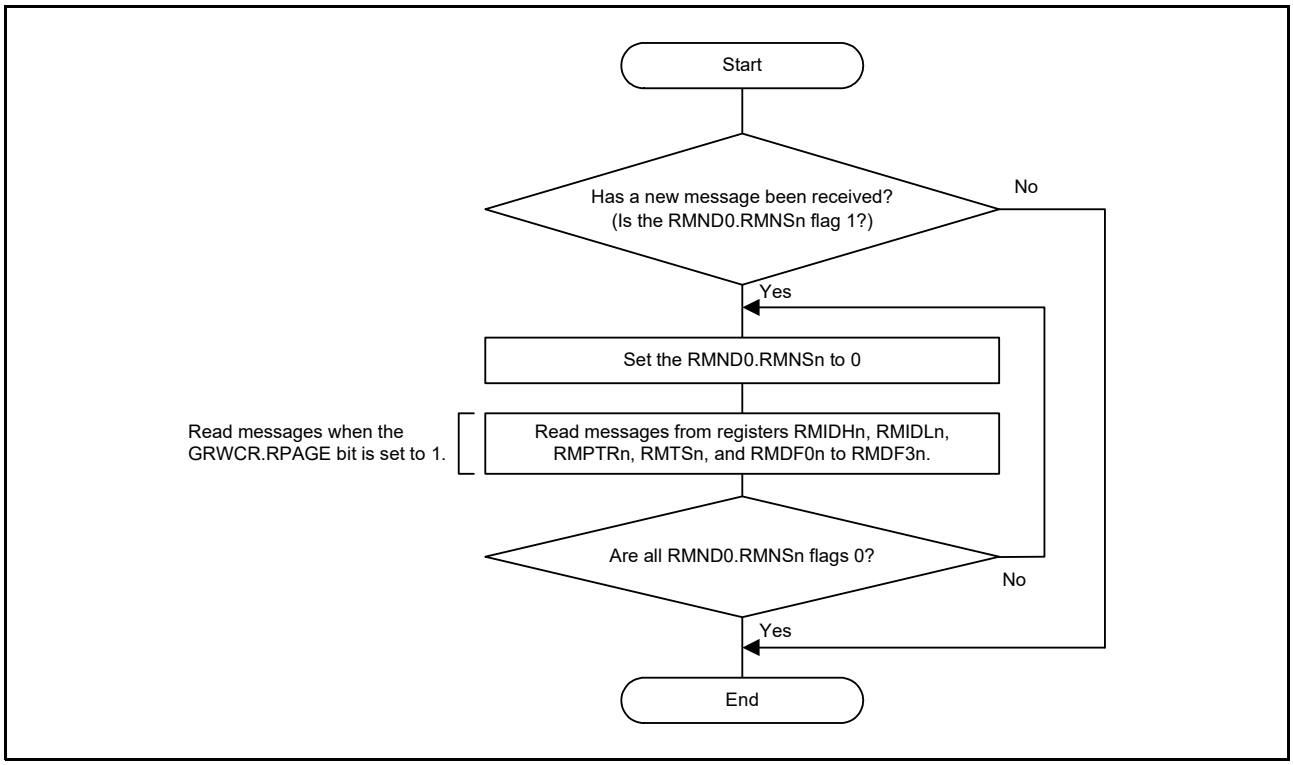


Figure 28.22 Receive Buffer Reading Procedure

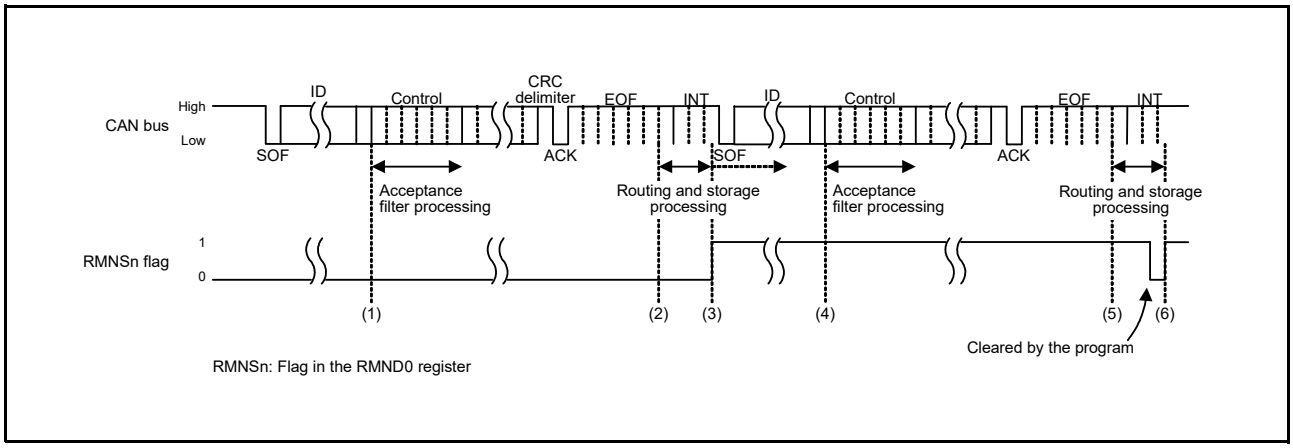


Figure 28.23 Receive Buffer Reception Timing Chart

(1) When the ID field in a message has been received, the acceptance filter processing starts.

(2) When the message matches the receive rule of the corresponding channel and the message has been successfully received, the routing processing to transfer the message to the specified buffer starts. When the GCFGL.DCE bit is set to 1 (DLC check is enabled), the DLC filter processing starts at this time.

(3) When the message has passed through the DLC filter processing, the processing to store the message in the specified receive buffer starts.
When the message storage processing starts, the corresponding RMND0.RMNSn flag is set to 1 (receive buffer contains a new message). If other channels are performing filter processing or transmit priority determination processing, the routing processing and the storage processing may be delayed.

(4) When the ID field of the next message has been received, the acceptance filter processing starts.

(5) When the message matches the receive rule of the corresponding channel and the message has been successfully received, the routing processing to transfer the message to the specified buffer starts. When the GCFGL.DCE bit is set to 1 (DLC check is enabled), the DLC filter processing starts at this time.

(6) When the corresponding RMND0.RMNSn flag is set to 0 (receive buffer contains no new message), this flag is set to 1 again when the message storage processing starts. Even if the RMND0.RMNSn flag remains 1, a new message is overwritten to the receive buffer. The RMND0.RMNSn flag should not be set to 0 during storage of messages.

28.10.2 FIFO Buffer Reading Procedure

When received messages have been stored in one or more receive FIFO buffers or a transmit/receive FIFO buffer that is set to receive mode, the corresponding message count display counter (RFSTSm.RFMC[5:0] flags or CFSTS0.CFMC[5:0] flags) is incremented. At this time, when the RFCCm.RFIE bit (receive FIFO interrupt is enabled) or the CFCCL0.CFRXIE bit (transmit/receive FIFO receive interrupt is enabled) is set to 1, an interrupt request is generated. Received messages can be read from the RFIDLm, RFIDHm, RFTSm, RFPTRm, and RFDF0m to RFDF3m registers (receive FIFO buffers) or the CFIDL0, CFIDH0, CFTS0, CFPTR0, and CFDF00 to CFDF30 registers (transmit/receive FIFO buffers). Messages in FIFO buffers can be read sequentially on a first-in, first-out basis.
When the message count display counter value matches the FIFO buffer depth (a value set by the RFCCm.RFDC[2:0] bits or the CFCCL0.CFDC[2:0] bits), the RFFLL or CFFLL flag is set to 1 (the receive FIFO buffer is full).
When all messages have been read out of the FIFO buffer, the RFSTSm.RFEMP flag or CFSTS0.CFEMP flag is set to 1 (the receive FIFO buffer contains no unread message (buffer empty)).
If the RFCCm.RFE bit or the CFCCL0.CFE bit is set to 0 (no receive FIFO buffer is used) with the interrupt request flag (RFSTSm.RFIF flag or CFSTS0.CFRXIF flag) set to 1 (a receive FIFO interrupt request is present), the interrupt request flag is not automatically set to 0. Set the interrupt request flag to 0 by the program.

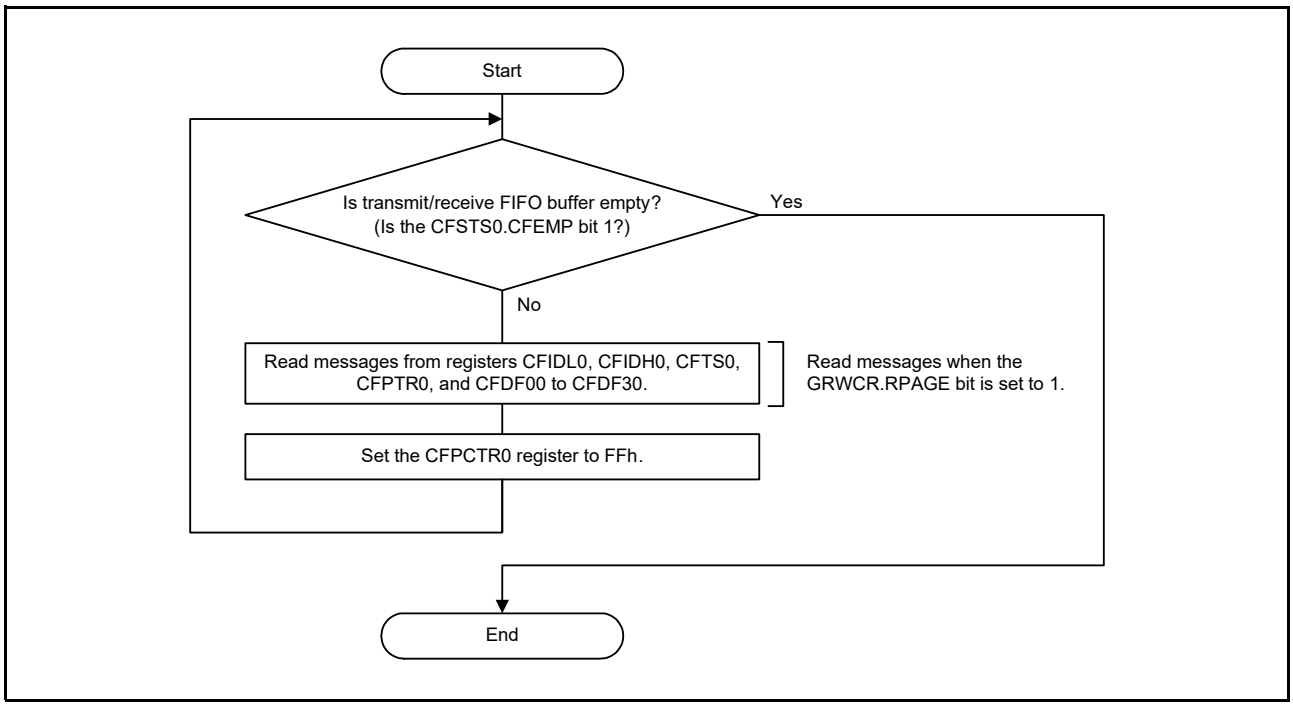


Figure 28.24 Transmit/Receive FIFO Buffer Reading Procedure

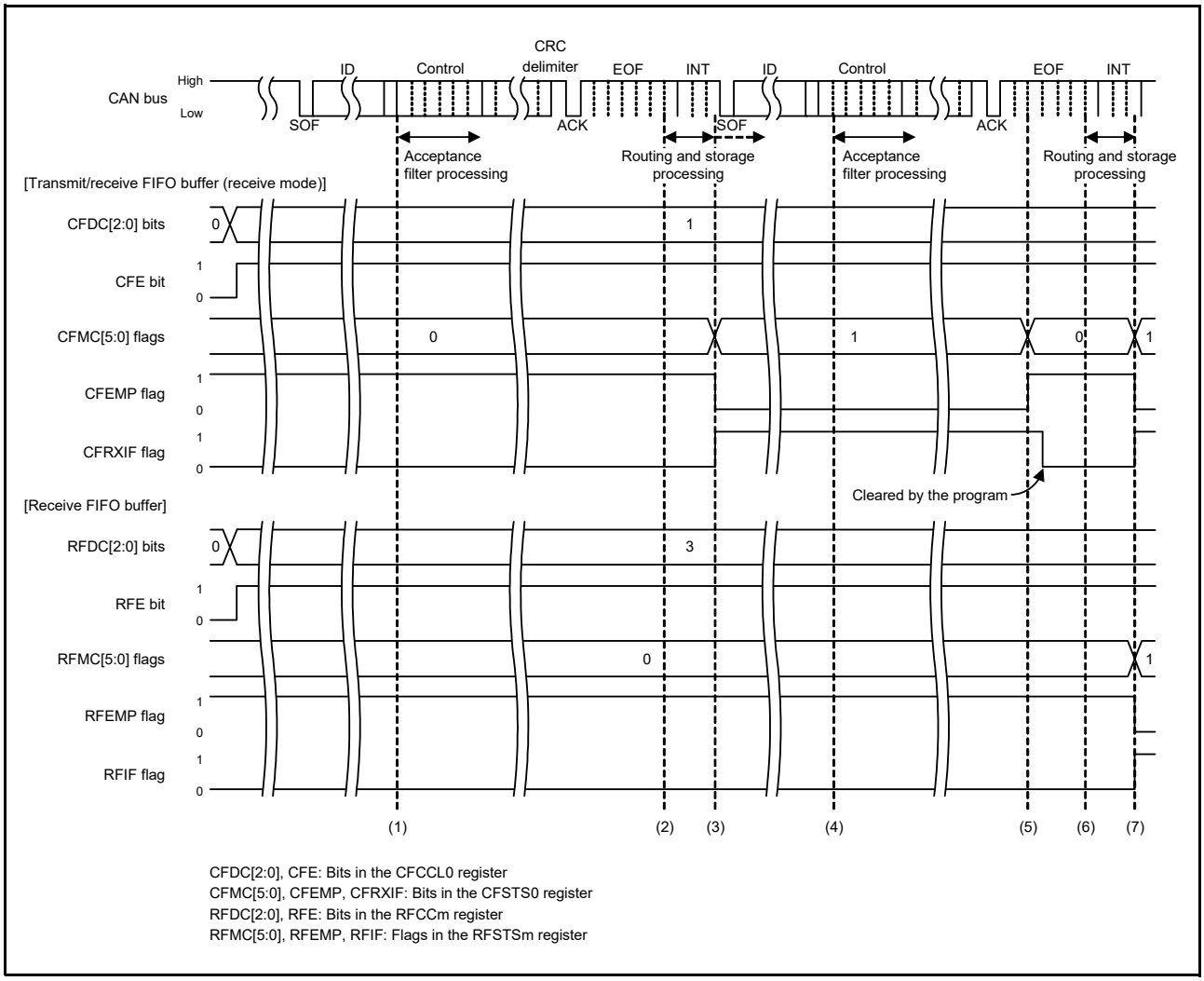


Figure 28.25 FIFO Buffer Reception Timing Chart

(1) When the ID field in a message has been received, the acceptance filter processing starts.

(2) When the message matches the receive rule of the corresponding channel and the message has been successfully received, the routing processing to transfer the message to the specified buffer starts. When the GCFGL.DCE bit is set to 1 (DLC check is enabled), the DLC filter processing starts at this time.

(3) When the message has passed through the DLC filter processing and the CFCCL0.CFE value is 1 (transmit/receive FIFO buffers are used) and the CFCCL0.CFDC[2:0] value is 001b or more, the message is stored in the transmit/receive FIFO buffer that is set to receive mode. The CFSTS0.CFMC[5:0] value is incremented and becomes 01h. When the CFCCL0.CFIM bit is set to 1 (a FIFO receive interrupt request is generated each time a message has been received), the CFSTS0.CFRXIF flag is set to 1 (a transmit/receive FIFO receive interrupt request is present). The CFSTS0.CFRXIF flag can be reset to 0 by the program.

(4) When the ID field of the next message has been received, the acceptance filter processing starts.

(5) Read received messages from the CFIDL0, CFIDH0, CFTS0, CFPTR0, and CFDF00 to CFDF30 registers and write FFh to the CFPCTR0 register. Thereby the CFSTS0.CFMC[5:0] flags are decremented and become 00h, and the CFSTS0.CFEMP flag becomes 1 (the transmit/receive FIFO buffer contains no message (buffer empty)).

(6) When the message matches the receive rule of the corresponding channel and the message has been successfully received, the routing processing to transfer the message to the specified buffer starts. When the GCFGL.DCE bit is set to 1 (DLC check is enabled), the DLC filter processing starts at this time.

(7) The message is stored in the transmit/receive FIFO buffer set in receive mode, when the message has passed through the DLC filter process if the CFCCL0.CFE bit is set to 1 (transmit/receive FIFO buffers are used) and the

CFCCL0.CFDC[2:0] bits are set to 001b or more.
The CFSTS0.CFMC[5:0] value is incremented to 01h. When the CFCCL0.CFIM bit is set to 1 (an interrupt occurs each time a message has been received), the CFSTS0.CFRXIF flag is set to 1 (a transmit/receive FIFO receive interrupt request is present).
The message is stored in the receive FIFO buffer, if the RFCCm.RFE bit is set to 1 (receive FIFO buffers are used) and RFCCm.RFDC[2:0] bits are set to 001b or more. The RFSTSm.RFMC[5:0] value is incremented to 01h. When the RFCCm.RFIM bit is set to 1 (an interrupt occurs each time a message has been received), the RFSTSm.RFIF flag is set to 1 (a receive FIFO interrupt request is present).

28.11 Transmission Procedure

28.11.1 Procedure for Transmission from Transmit Buffers

Figure 28.26 shows the procedure for transmission from transmit buffers.
Figure 28.27 shows a timing chart where messages are transmitted from two transmit buffers and transmission has been successfully completed. Figure 28.28 shows a timing chart where messages are transmitted from two transmit buffers and transmit abort has been completed.

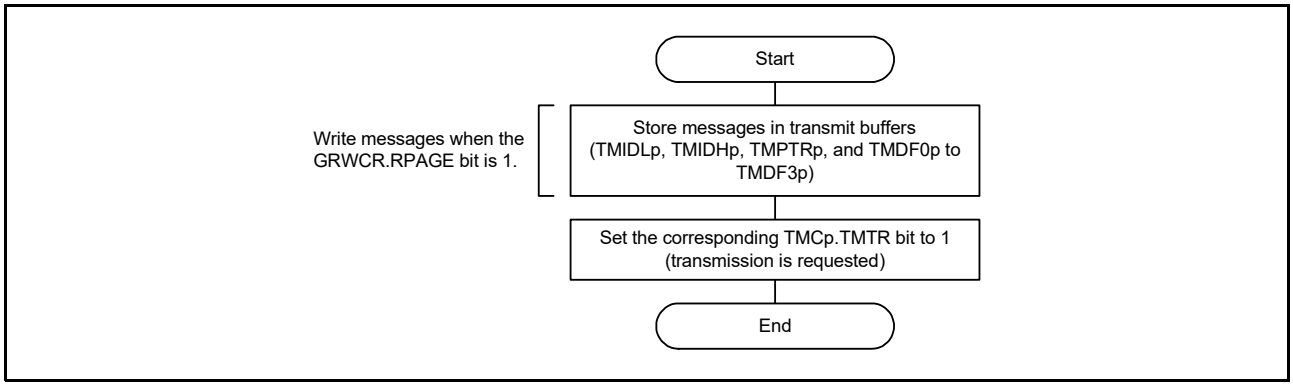


Figure 28.26 Procedure for Transmission from Transmit Buffers

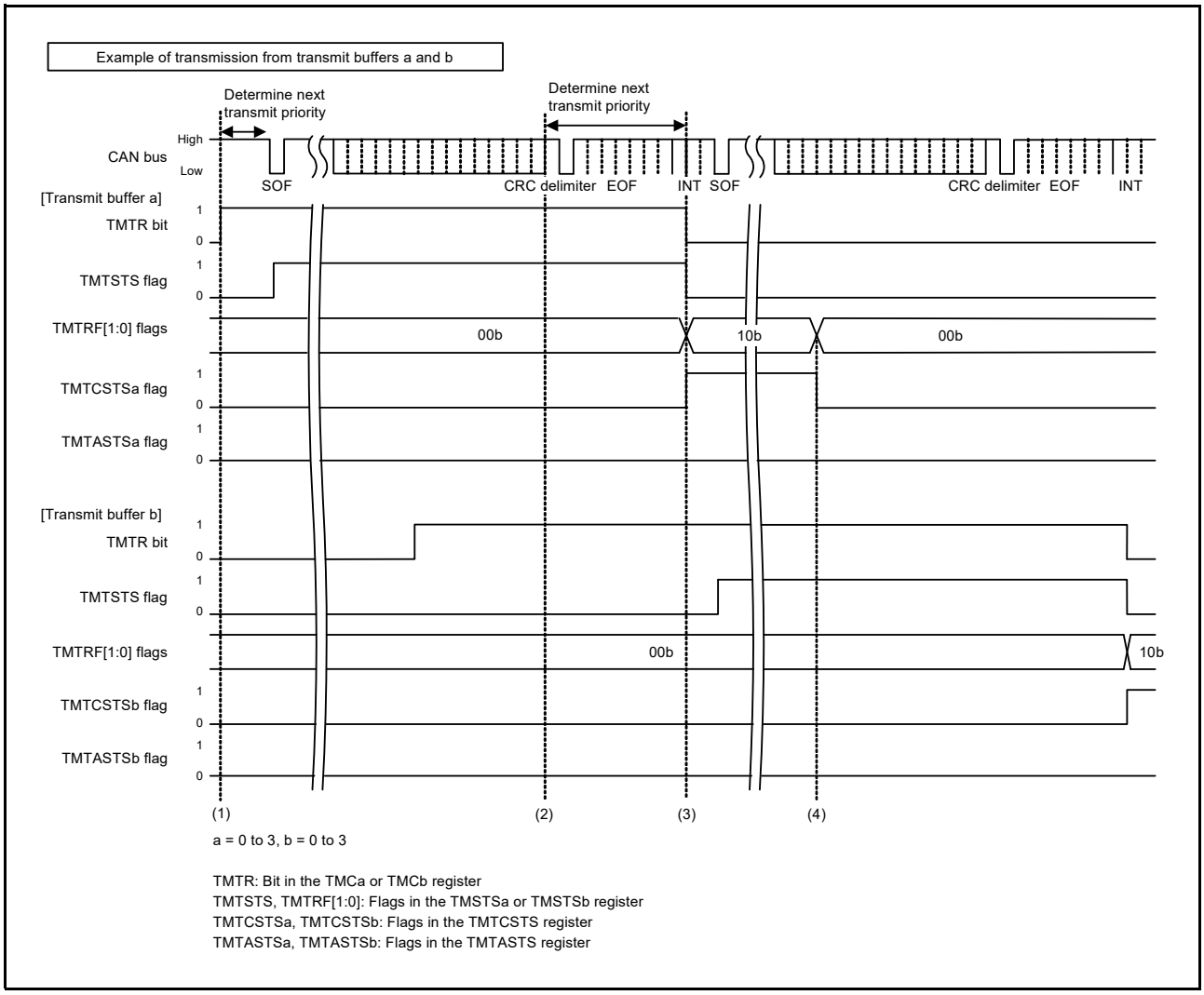


Figure 28.27 Transmit Buffer Transmission Timing Chart (Transmission Completed Successfully)

(1) When the TMCa.TMTR bit (a = 0 to 3) is set to 1 while the CAN bus is idle, the transmit priority determination processing starts to determine the highest-priority transmit buffer. If transmit buffer a is determined to be the highest-priority transmit buffer, the corresponding TMSTSa.TMTSTS flag is set to 1 (transmission is in progress) and the CAN channel starts transmitting data.

(2) When a transmit request from a buffer is present, the priority determination starts with the CRC delimiter for the next transmission.

(3) When transmit completes successfully, the TMSTSa.TMTRF[1:0] flags are set to 10b (transmission has been completed (without transmit abort request)), the TMSTSa.TMTSTS flag and the TMCa.TMTR bit are set to 0, and the TMTCSTS.TMTCSTSa flag is set to 1. When the TMIEC.TMIEa value is 1 (transmit buffer interrupt is enabled), a transmit interrupt request is generated. To clear the interrupt request, set the TMSTSa.TMTRF[1:0] flags to 00b (transmission is in progress or no transmit request is present).

(4) Before starting the next transmission, set the TMSTSa.TMTRF[1:0] flags to 00b. Write the next message to the transmit buffer, and then set the TMCa.TMTR bit to 1 (transmission is requested). The TMCa.TMTR bit can be set to 1 only when the TMSTSa.TMTRF[1:0] flag value is 00b.
If an arbitration lost has occurred after transmission is started, the TMSTSa.TMTSTS flag is set to 0. The transmit priority determination is reexecuted at the beginning of the CRC delimiter to search the highest-priority transmit buffer. If an error has occurred during transmission or after arbitration lost, the priority determination processing is reexecuted during transmission of an error frame.

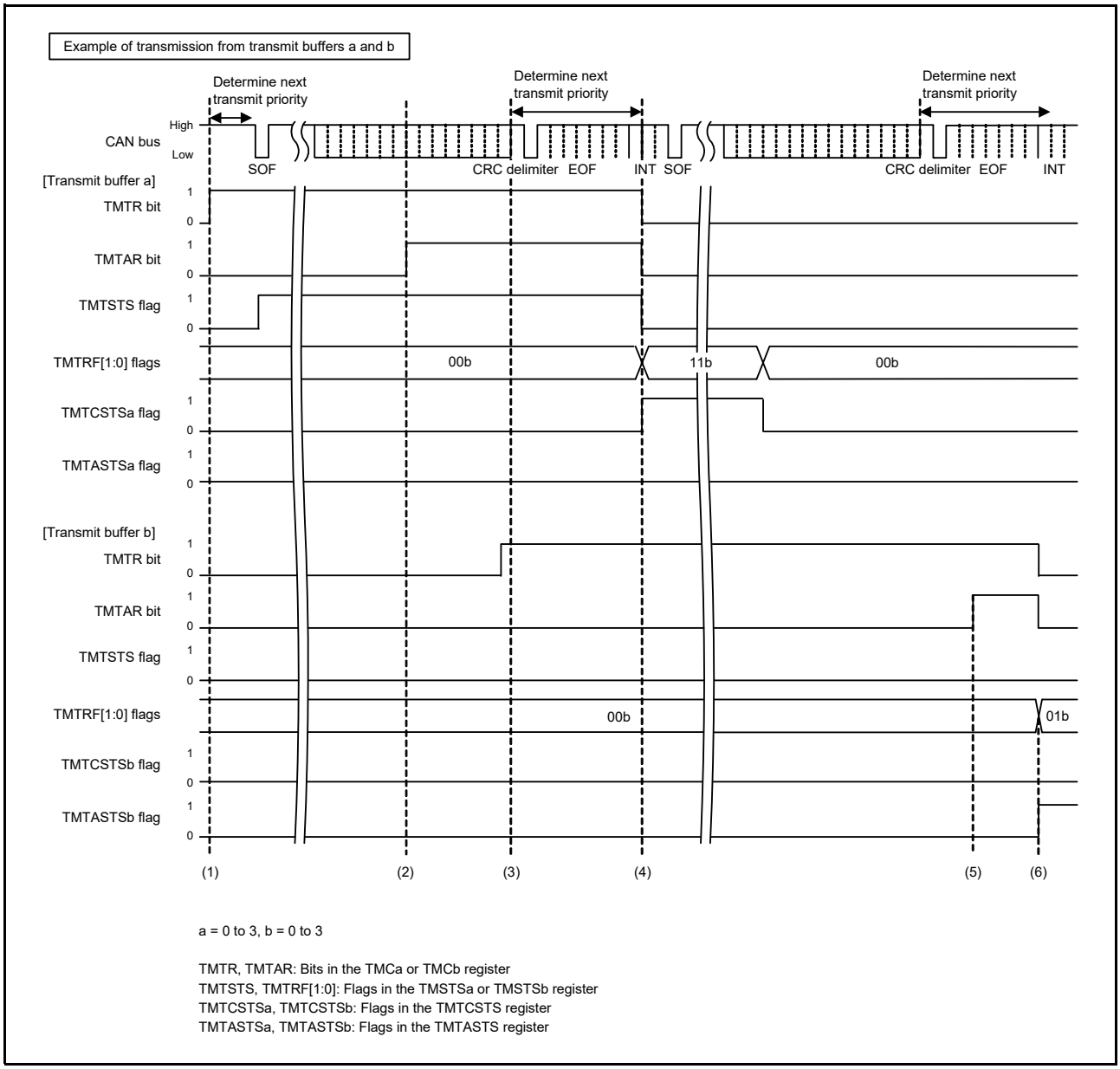


Figure 28.28 Transmit Buffer Transmission Timing Chart (Transmit Abort Completed)

(1) When the TMCa.TMTR bit (a = 0 to 3) is set to 1 while the CAN bus is idle, the transmit priority determination processing starts to determine the highest-priority transmit buffer. If transmit buffer a is determined to be the highest-priority transmit buffer, the corresponding TMSTSa.TMTSTS flag is set to 1 (transmission is in progress) and the CAN channel starts transmitting data.

(2) When it is determined that the transmit buffer is used for the next transmission or transmission is in progress, message transmission is not aborted unless an error or arbitration lost occurs even if the TMCa.TMTAR bit is set to 1 (transmit abort is requested).

(3) The priority determination starts with the CRC delimiter for the next transmission. In this timing chart, buffer b is not selected as the next transmit buffer.

(4) When transmit completes successfully, the TMSTSa.TMTRF[1:0] flags are set to 11b (transmission has been completed (with transmit abort request)), the TMSTSa.TMTSTS flag and the TMCa.TMTR bit are set to 0, and the TMTCSTS.TMTCSTSa flag is set to 1.
When the TMIEC.TMIEa value is 1 (transmit buffer interrupt is enabled), a transmit interrupt request is generated.

To clear the interrupt request, set the TMSTSa.TMTRF[1:0] flags to 00b (transmission is in progress or no transmit request is present).

(5) While another CAN node is transmitting data on the CAN bus (TMSTSa.TMTSTS flag = 0), if the TMCa.TMTAR bit is set to 1 while the corresponding channel is determining transmit priority, the TMCa.TMTR bit cannot be set to 0.

(6) After the internal processing time has passed, the transmission is terminated and the TMSTSa.TMTRF[1:0] flags are set to 01b and the TMTASTS.TMTASTSa flag is set to 1. When the transmit buffer is not transmitting data and is not selected as the next transmit buffer and priority determination is not being made, an abort request is immediately accepted and the TMSTSa.TMTRF flag is set to 01b. At this time, the TMCa.TMTR and TMTAR bits are set to 0.
When transmit abort is completed with the CTRH.TAIE bit set to 1 (transmit abort interrupt is enabled), an interrupt request is generated. To clear the interrupt request, set the TMSTSa.TMTRF[1:0] flags to 00b.

If an arbitration lost has occurred after the CAN channel started transmission, the TMSTSa.TMTSTS flag is set to 0. The transmit priority determination is reexecuted at the beginning of the CRC delimiter to search the highest-priority transmit buffer. If an error has occurred during transmission or after arbitration lost, the priority determination processing is reexecuted during transmission of an error frame.

28.11.2 Procedure for Transmission from Transmit/Receive FIFO Buffers

Figure 28.29 shows the procedure for transmission from transmit/receive FIFO buffers.
Figure 28.30 shows a timing chart where messages are transmitted from the transmit/receive FIFO buffers and transmission has been successfully completed. Figure 28.31 shows a timing chart where messages are transmitted from the transmit/receive FIFO buffers and transmit abort has been completed.

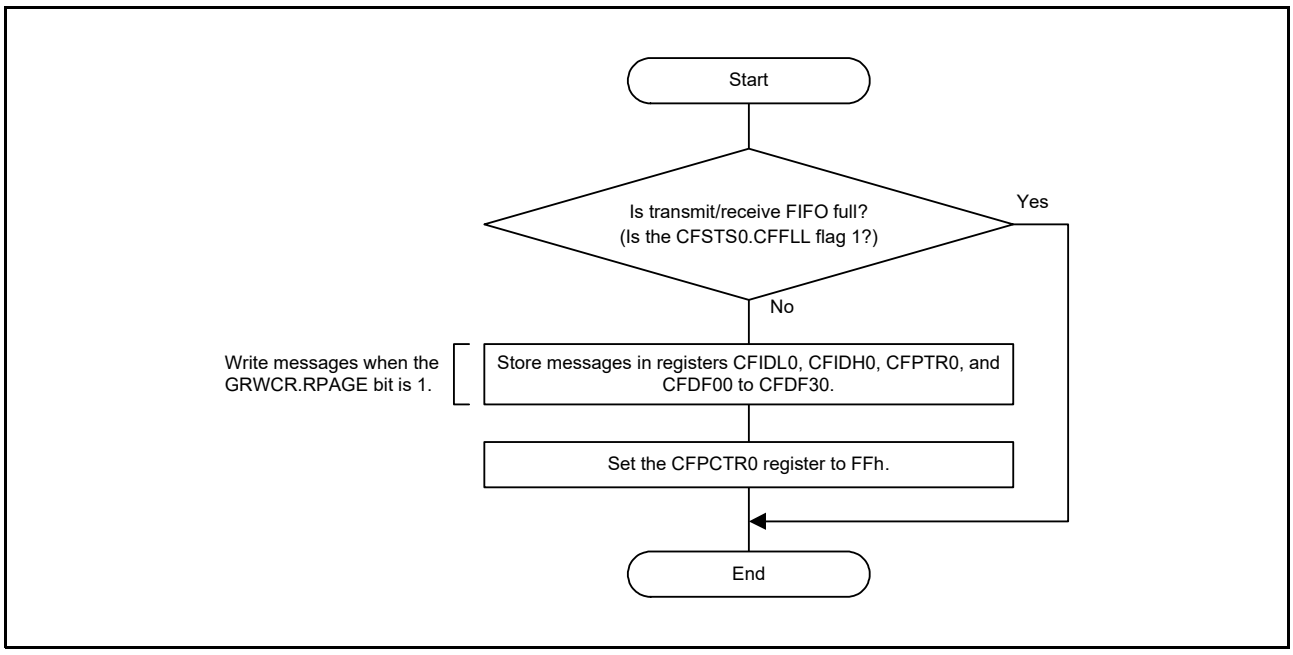


Figure 28.29 Procedure for Transmission from Transmit/Receive FIFO Buffers

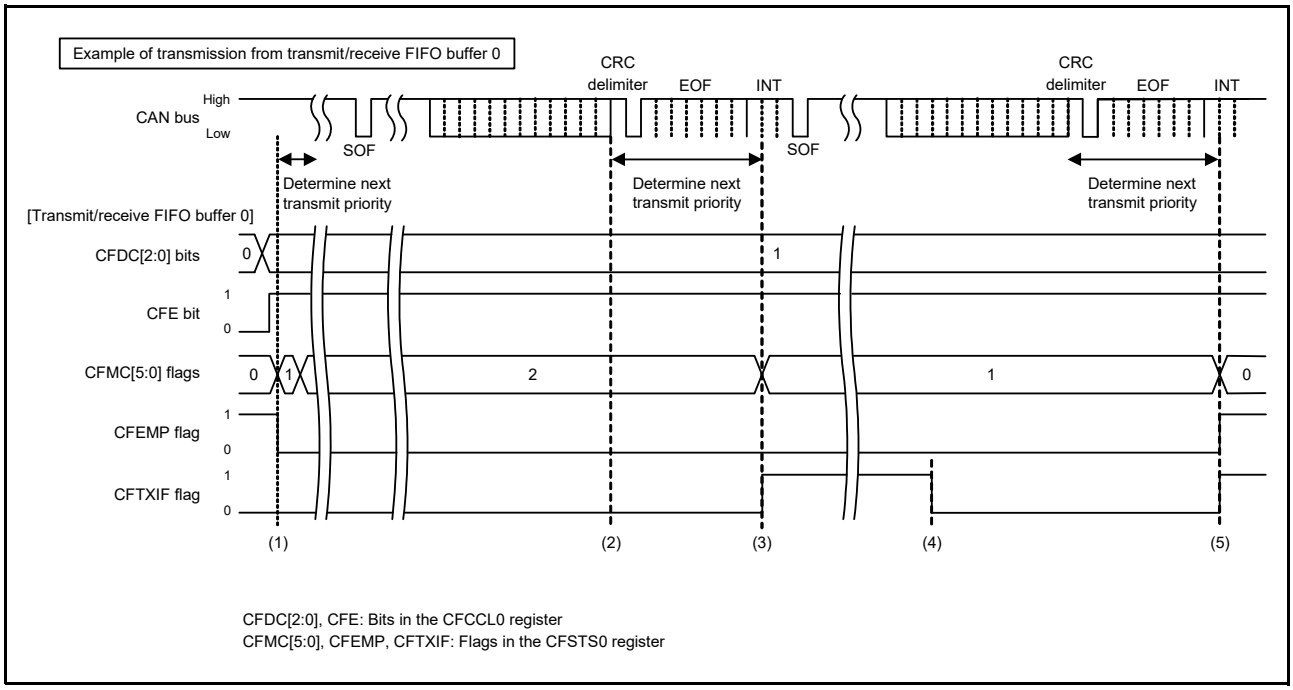


Figure 28.30 Transmit/Receive FIFO Buffer Transmission Timing Chart (Transmission Completed Successfully)

(1) While the CAN bus is idle, when the CFCCL0.CFE value is 1 (transmit/receive FIFO buffer 0 is used) and the CFCCL0.CFDC[2:0] value is 001b (4 messages) or more and the CFSTS0.CFMC[5:0] value is 01h or more, the priority determination processing starts to determine the highest-priority transmit message. When the highest-priority transmit message has been determined, transmission of the message starts.

(2) When a transmit request from a buffer is present, the priority determination starts with the CRC delimiter for the next transmission.

(3) When transmit completes successfully, the CFSTS0.CFMC[5:0] value is decremented. Setting the CFCCL0.CFIM bit to 1 (a FIFO transmit interrupt request is generated each time a message has been transmitted) sets the CFSTS0.CFTXIF flag to 1 (a transmit/receive FIFO transmit interrupt request is present).

(4) The CFSTS0.CFTXIF flag can be cleared by the program.

(5) Message transmission from transmit/receive FIFO buffer 0 has been completed and the CFSTS0.CFMC[5:0] value is decremented. The CFSTS0.CFMC[5:0] flags are set to 00h and therefore the CFSTS0.CFEMP flag is set to 1 (the transmit/receive FIFO buffer contains no message (buffer empty)).
Transmission is continued until the CFSTS0.CFEMP flag is set to 1. It is possible to continuously store transmit messages in FIFO buffers until the CFSTS0.CFFLL flag is set to 1 (the transmit/receive FIFO buffer is full).

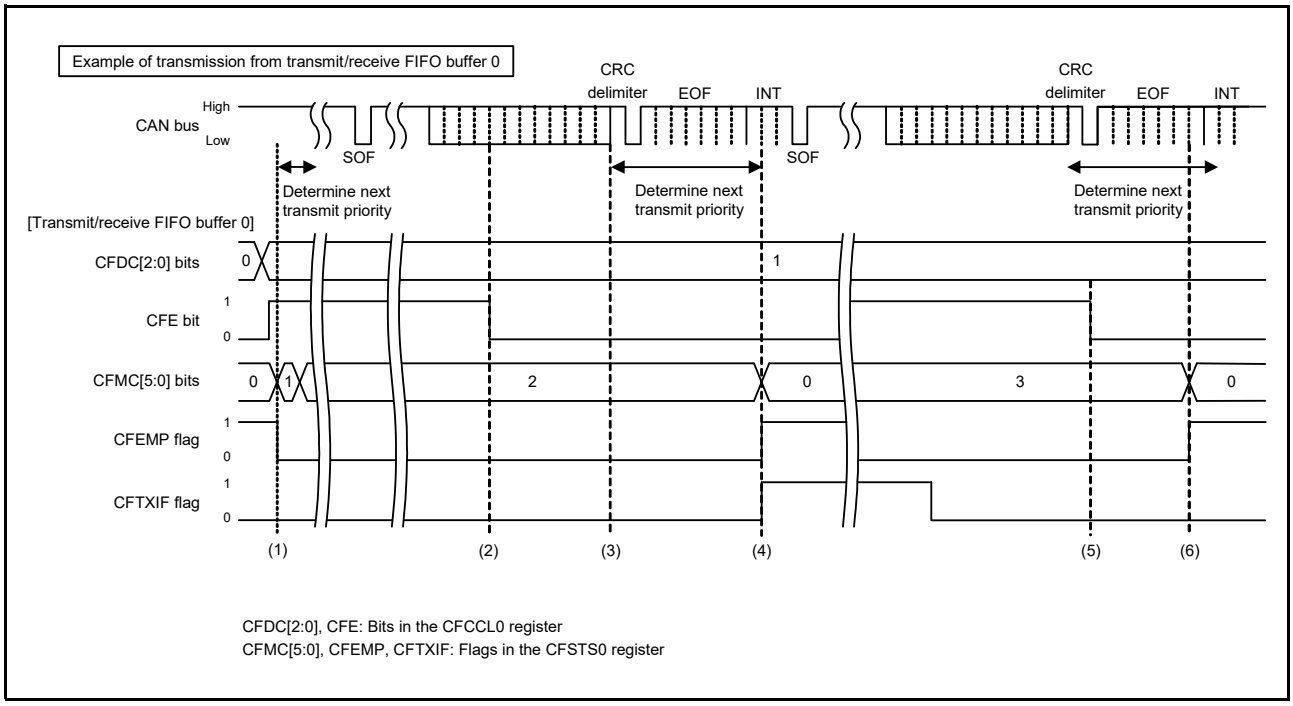


Figure 28.31 Transmit/Receive FIFO Buffer Transmission Timing Chart (Transmit Abort Completed)

(1) While the CAN bus is idle, when the CFCCL0.CFE value is 1 (transmit/receive FIFO buffer 0 is used) and the CFCCL0.CFDC[2:0] value is 001b (4 messages) or more and the CFSTS0.CFMC[5:0] value is 01h or more, the priority determination processing starts to determine the highest-priority transmit message. When the highest-priority transmit message has been determined, transmission of the message starts.

(2) When transmission is in progress or it is determined that the transmit/receive FIFO buffer is used for the next transmission, message transmission is not aborted unless an error or arbitration lost occurs even if the CFCCL0.CFE bit is set to 0 (no transmit/receive FIFO buffer 0 is used).

(3) When a transmit request from a buffer is present, the priority determination starts with the CRC delimiter for the next transmission. In this figure, transmit/receive FIFO buffer 0 is not selected as a buffer for the next transmission.

(4) When transmit completes successfully, the CFSTS0.CFMC[5:0] value is set to 00h. Setting the CFCCL0.CFIM bit to 1 (a FIFO transmit interrupt request is generated each time a message has been transmitted) sets the CFSTS0.CFTXIF flag to 1 (a transmit/receive FIFO transmit interrupt request is present). The CFSTS0.CFTXIF flag can be cleared by the program.

(5) If another CAN node on the CAN bus is transmitting data (not from transmit/receive FIFO buffer 0), transmit/receive FIFO buffer 0 cannot be disabled immediately even if the CFCCL0.CFE bit is set to 0 (no transmit/receive FIFO buffer 0 is used) during transmit priority determination. (The CFSTS0.CFEMP flag is not set to 1 (the transmit/receive FIFO buffer contains no message (buffer empty)) immediately.)

(6) After the internal processing time has passed, transmit/receive FIFO buffers are disabled and the CFSTS0.CFMC[5:0] flags are set to 00h and the CFSTS0.CFEMP flag is set to 1. When the transmit/receive FIFO buffer 0 is not transmitting data and is not selected as the next transmit buffer and priority determination is not in progress, the transmit/receive FIFO buffer 0 is immediately disabled. (The CFSTS0.CFMC[5:0] flags are set to 00h and the CFSTS0.CFEMP flag is set to 1.)

28.11.3 Transmit History Buffer Reading Procedure

Transmit history data can be read from the THLACC0 register. The next data can be accessed by writing FFh to the corresponding THLPCTR0 register after reading a set of data. Figure 28.32 shows the transmit history buffer reading procedure.

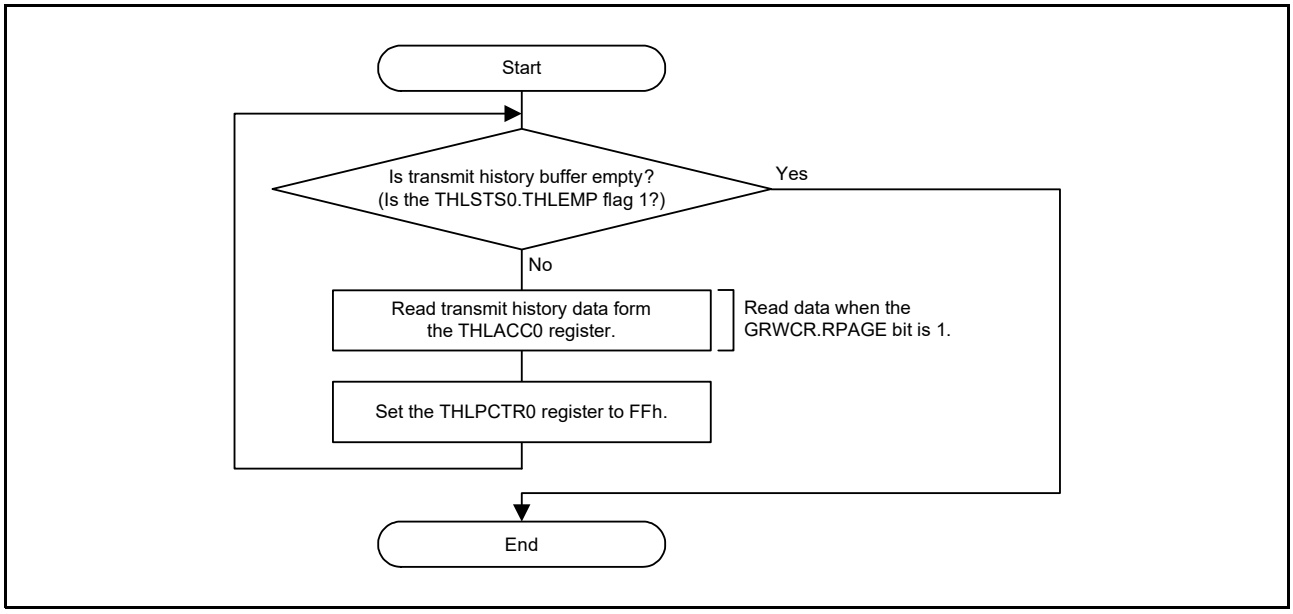


Figure 28.32 Transmit History Buffer Reading Procedure

28.12 Test Settings

28.12.1 Self-Test Mode Setting Procedure

Self-test mode allows communication test on a channel basis by receiving messages transmitted from the own node. Figure 28.33 shows the self-test mode setting procedure.

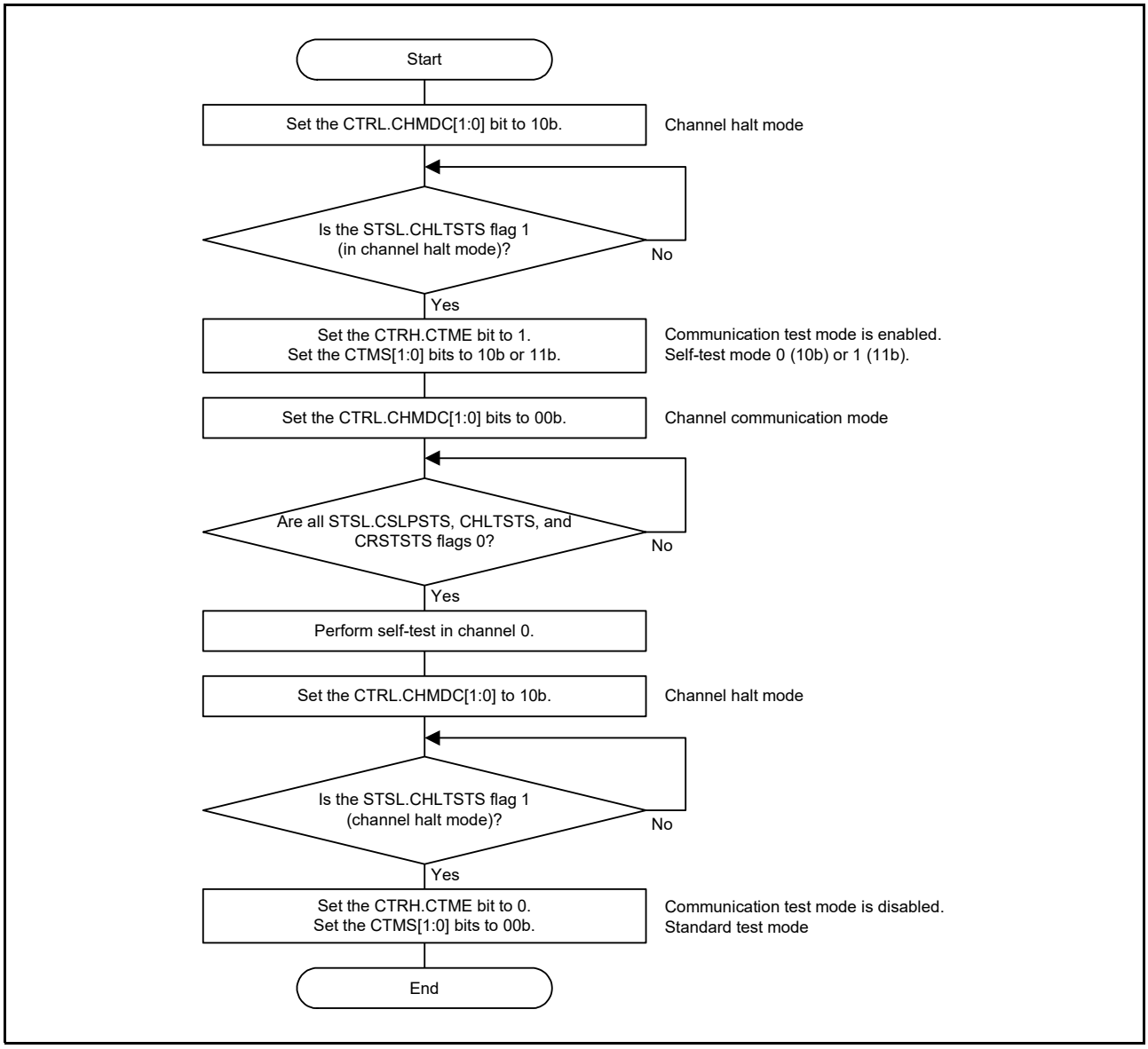


Figure 28.33 Self-Test Mode Setting Procedure

28.12.2 Protection Unlock Procedure

Since the global test functions shown in Table 28.14 are protected, write unlock data 1 and unlock data 2 in succession to the GLOCKK.LOCK[15:0] bits, and then set each test function bit to 1.

Table 28.14 Protection Unlock Data for Test Functions

Test Function	Protection Unlock Data 1	Protection Unlock Data 2	Target Bit
RAM test	7575h	8A8Ah	GTSTCTRL.RTME bit

If an incorrect value has been written to the GLOCKK.LOCK[15:0] bits, retry the procedure above from writing of unlock data 1.
Figure 28.34 shows the protection unlock procedure.

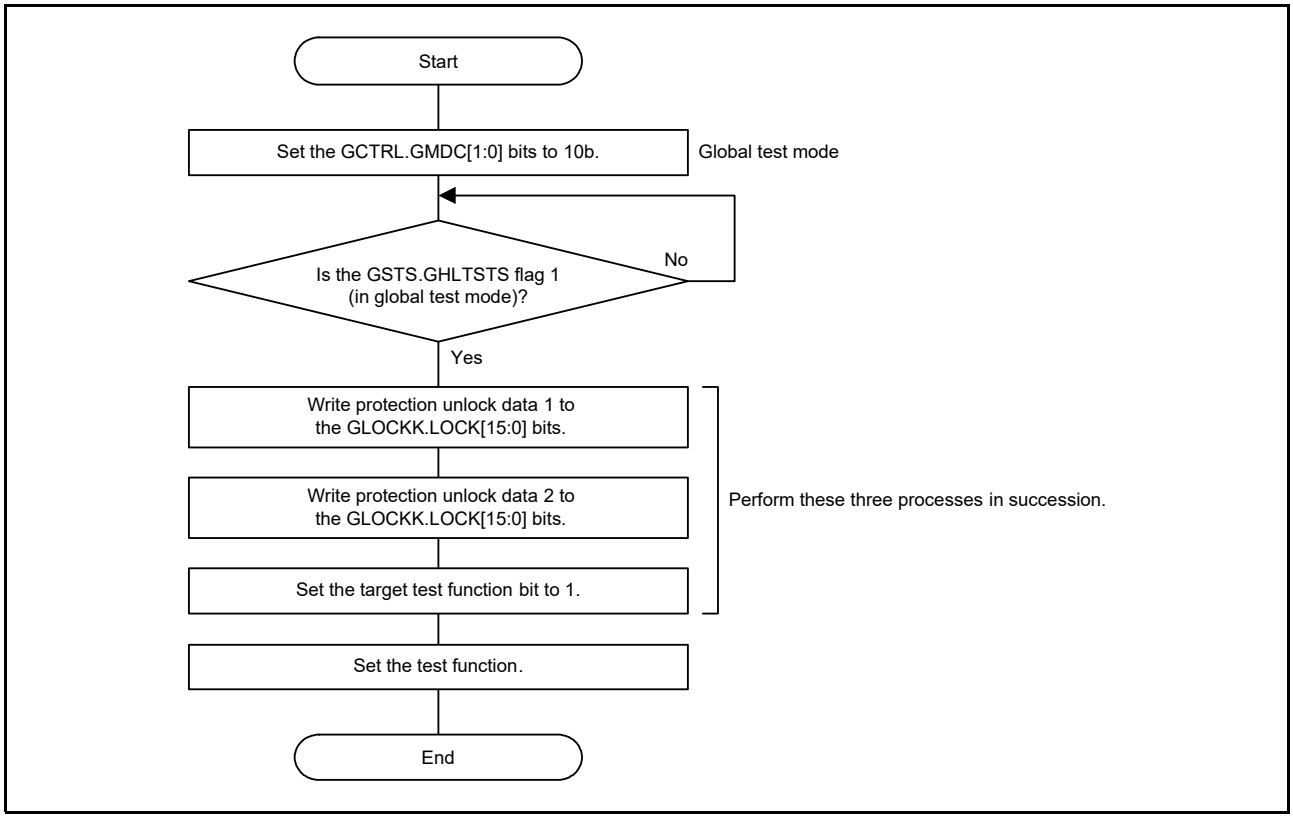


Figure 28.34 Protection Unlock Procedure

28.12.3 RAM Test Setting Procedure

RAM tests include CAN RAM read/write test. The read/write test verifies that data written to the RAM is read correctly. Before closing the RAM test, write 0000h to all pages of the CAN RAM.

Figure 28.35 shows the RAM test setting procedure.

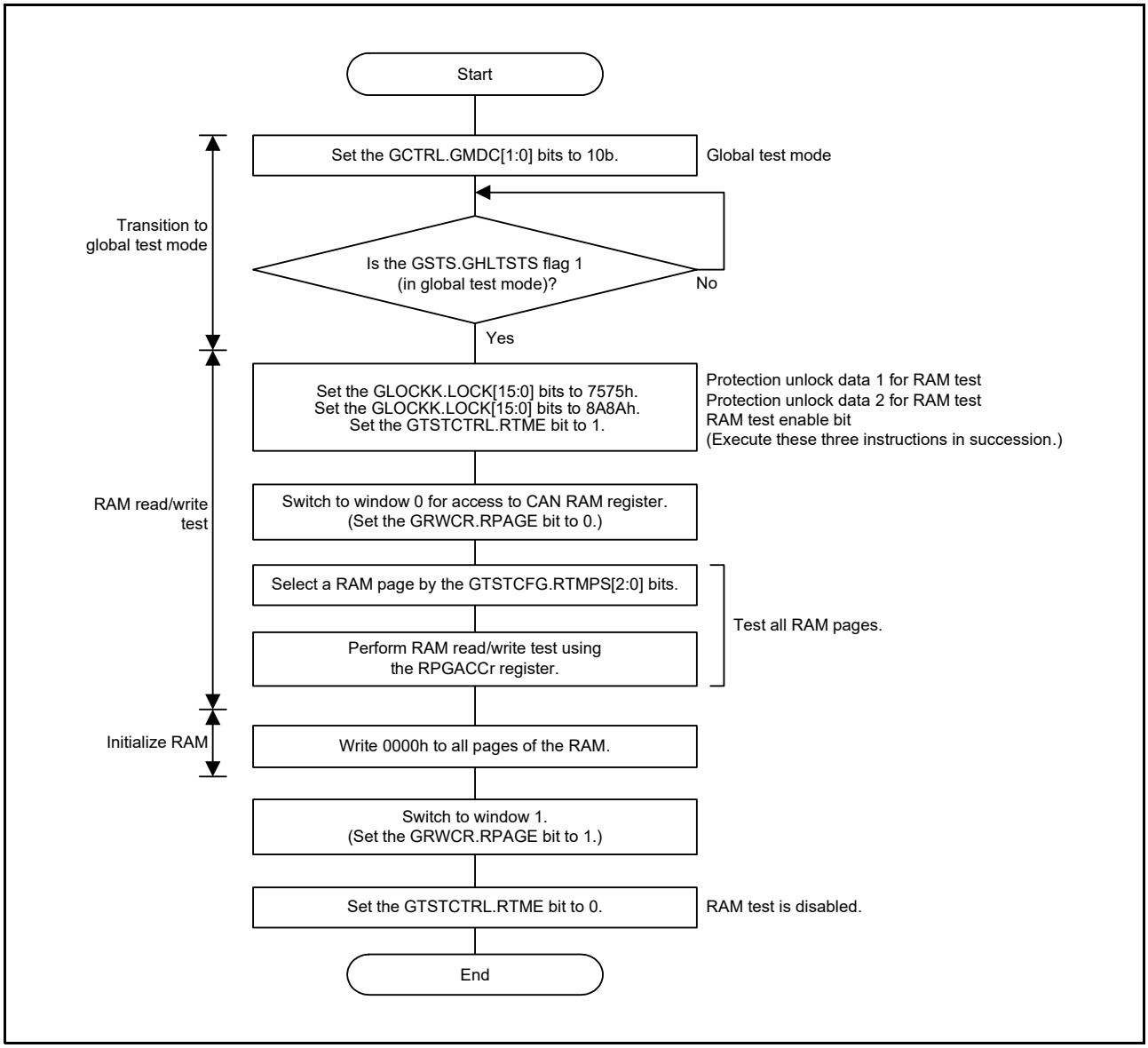


Figure 28.35 RAM Test Setting Procedure

28.13 Notes on the CAN Module

- When changing a global mode, check the GSTS.GSLPSTS, GHLTSTS, and GRSTSTS flags for transitions. When changing a channel mode, check the STSL.CSLPSTS, CHLTSTS, and CRSTSTS flags for transitions.
- The acceptance filter processing checks receive rules sequentially in ascending order from the minimum rule number. If the same ID, IDE bit, or RTR bit value is set for multiple receive rules, the minimum number of receive rule is used for the acceptance filter processing. If the message does not pass through the subsequent DLC filter processing, the data processing is terminated without returning to the acceptance filter processing and the message is not stored in the buffer.
- When linking transmit buffers to transmit/receive FIFO buffers, set the control register (TCMp) of the corresponding transmit buffer to 00h. The status register (TMSTSp) of the corresponding transmit buffer should not be used. Flags in other status registers (registers TMTRSTS, TMTCSTS, and TMTASTS), which correspond to transmit buffers linked to transmit/receive FIFO buffers remain unchanged. Set the enable bit in the corresponding interrupt enable register (the TMIEC register) to 0 (transmit buffer interrupt is disabled).
- When the CAN bit time clock is selected as a timestamp counter clock source, the timestamp counter stops when the corresponding channel has transitioned to channel reset mode or channel halt mode.
- In case of an attempt to store a new receive message when the receive FIFO buffer and the transmit/receive FIFO buffer are full, the new message is discarded. If you wish to store a new transmit message in the transmit/receive FIFO buffer, check that the transmit/receive FIFO buffer is not full.
- Since an interrupt request flag in the CAN module is not automatically set to 0 when an interrupt is accepted, the flags must be set to 0 by software. After the corresponding interrupt request flag has been set to 1, an interrupt is not generated even if an interrupt source condition is satisfied.
- In order to generate the CAN related interrupt that several interrupt sources are gathered, the following condition should be met:
  All interrupt request flags corresponding to these interrupt sources in the CAN module are set to 0 (note that this only applies to those interrupt request flags for which the corresponding interrupt enable bits shown in Table 28.11 are set to 1).
- The values of unused receive buffer registers (RMIDLn, RMIDHn, RMTSn, RMPTRn, and RMDF0n to RMDF3n (n = 0 to 15)), receive FIFO access registers (RFIDLm, RFIDHm, RFTSm, RFPTRm, and RFDF0m to RFDF3m (m = 0, 1)), and transmit/receive FIFO access registers (CFIDL0, CFIDH0, CFTS0, CFPTR0, and CFDF00 to CFDF30) become undefined once the CAN module exits from global reset mode and enters global operating mode or global test mode.

29. Serial Peripheral Interface (RSPIb)

In this section, “PCLK” is used to refer to PCLKB.

29.1 Overview

This MCU includes one channel of Serial Peripheral Interface (RSPI).
The RSPI channels are capable of high-speed, full-duplex synchronous serial communications with multiple processors and peripheral devices.
Table 29.1 lists the specifications of the RSPI, and Figure 29.1 shows a block diagram of the RSPI.
In this section, m as used with the RSPI command registers (SPCMDm) indicates 0 to 7.

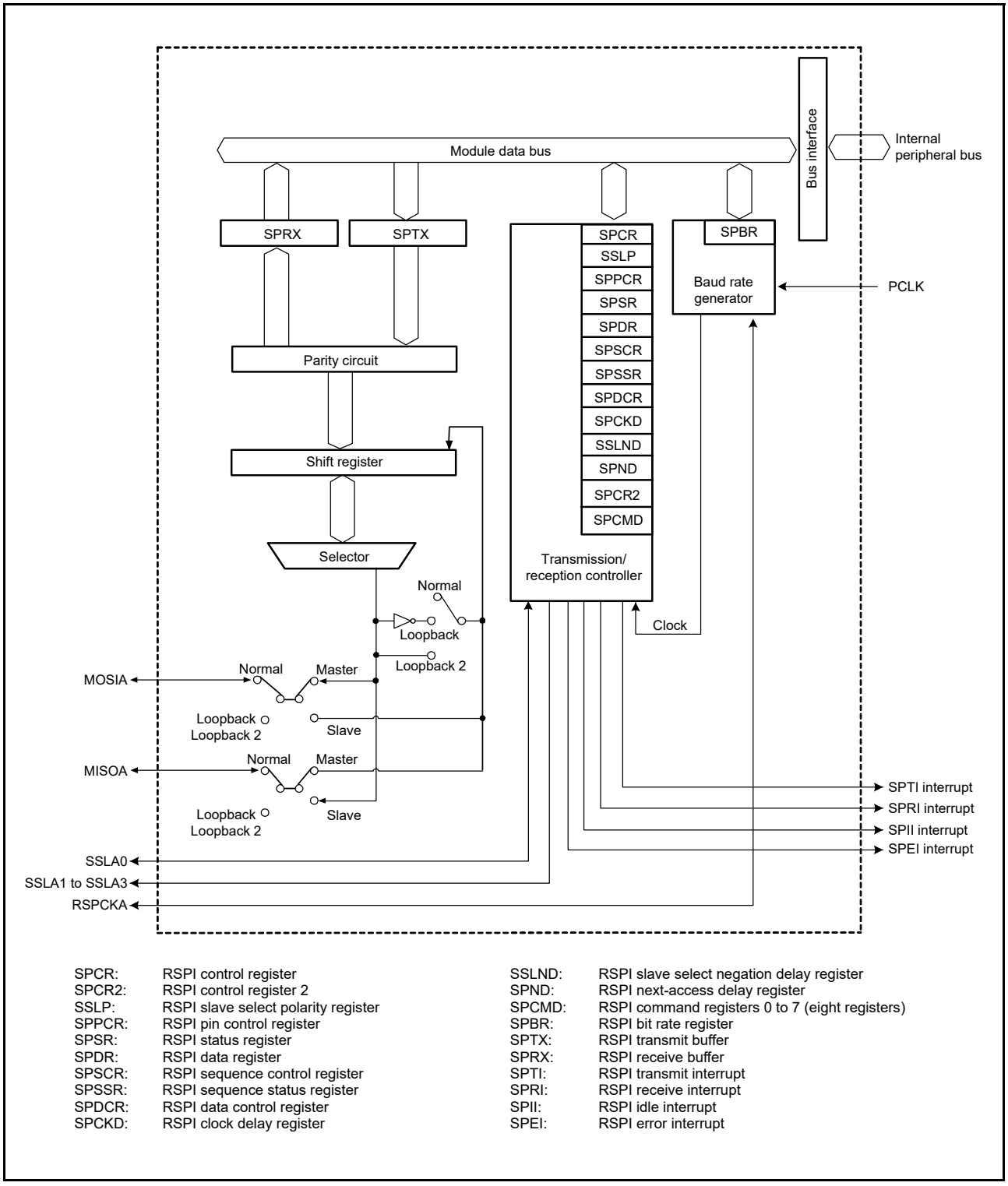
Table 29.1 RSPI Specifications (1/2)

Item	Description
Number of channels	One channel
RSPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Transmit-only operation is available. • Communication mode: Full-duplex or transmit-only can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK
Data format	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits).
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from divided by 2 to divided by 4096). • In slave mode, the minimum PCLK clock divided by 6 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 6). Width at high level: 3 cycles of PCLK; width at low level: 3 cycles of PCLK
Buffer configuration	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers
Error detection	• Mode fault error detection • Overrun error detection*1 • Parity error detection • Underrun error detection
SSL control function	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for either output or unused. • In slave mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity
Control in master transfer	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function

Table 29.1 RSPI Specifications (2/2)

Item	Description
Interrupt sources	• Interrupt sources Receive buffer full interrupt Transmit buffer empty interrupt RSPI error interrupt (mode fault, overrun, underrun, or parity error) RSPI idle interrupt (RSPI idle)
Others	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loopback mode
Low power consumption function	Module stop state can be set.

Note 1. In master reception and when the RSPCK auto-stop function is enabled, an overrun error does not occur because the transfer clock is stopped at the timing of overrun error detection.



SPCR:	RSPI control register	SSLND:	RSPI slave select negation delay register
SPCR2:	RSPI control register 2	SPND:	RSPI next-access delay register
SSLP:	RSPI slave select polarity register	SPCMD:	RSPI command registers 0 to 7 (eight registers)
SPPCR:	RSPI pin control register	SPBR:	RSPI bit rate register
SPSR:	RSPI status register	SPTX:	RSPI transmit buffer
SPDR:	RSPI data register	SPRX:	RSPI receive buffer
SPSCR:	RSPI sequence control register	SPTI:	RSPI transmit interrupt
SPSSR:	RSPI sequence status register	SPRI:	RSPI receive interrupt
SPDCR:	RSPI data control register	SPII:	RSPI idle interrupt
SPCKD:	RSPI clock delay register	SPEI:	RSPI error interrupt

Figure 29.1 RSPI Block Diagram

Table 29.2 lists the I/O pins used in the RSPI.
The RSPI automatically switches the I/O direction of the SSLA0 pin. SSLA0 is set as an output when the RSPI is a single master and as an input when the RSPI is a multi-master or a slave. Pins RSPCKA, MOSIA, and MISOA are automatically set as inputs or outputs according to the setting of master or slave and the level input on the SSLA0 pin. Refer to section 29.3.2, Controlling RSPI Pins for details.

Table 29.2 RSPI Pin Configuration

Channel	Pin Name	I/O	Function
RSPI0	RSPCKA	I/O	Clock I/O
	MOSIA	I/O	Master transmit data I/O
	MISOA	I/O	Slave transmit data I/O
	SSLA0	I/O	Slave selection I/O
	SSLA1	Output	Slave selection output
	SSLA2	Output	Slave selection output
	SSLA3	Output	Slave selection output

29.2 Register Descriptions

29.2.1 RSPI Control Register (SPCR)

Address(es): RSPI0.SPCR 0008 8380h

	b7	b6	b5	b4	b3	b2	b1	b0
	SPRIE	SPE	SPTIE	SPEIE	MSTR	MODFEN	TXMD	SPMS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SPMS	RSPI Mode Select	0: SPI operation (4-wire method) 1: Clock synchronous operation (3-wire method)	R/W
b1	TXMD	Communications Operating Mode Select	0: Full-duplex synchronous serial communications 1: Serial communications consisting of only transmit operations	R/W
b2	MODFEN	Mode Fault Error Detection Enable	0: Disables the detection of mode fault error 1: Enables the detection of mode fault error	R/W
b3	MSTR	RSPI Master/Slave Mode Select	0: Slave mode 1: Master mode	R/W
b4	SPEIE	RSPI Error Interrupt Enable	0: Disables the generation of RSPI error interrupt requests 1: Enables the generation of RSPI error interrupt requests	R/W
b5	SPTIE	Transmit Buffer Empty Interrupt Enable	0: Disables the generation of transmit buffer empty interrupt requests 1: Enables the generation of transmit buffer empty interrupt requests	R/W
b6	SPE	RSPI Function Enable	0: Disables the RSPI function 1: Enables the RSPI function	R/W
b7	SPRIE	RSPI Receive Buffer Full Interrupt Enable	0: Disables the generation of RSPI receive buffer full interrupt requests 1: Enables the generation of RSPI receive buffer full interrupt requests	R/W

If the SPCR.MSTR, SPCR.MODFEN, or SPCR.TXMD bit is changed while the SPCR.SPE bit is 1, subsequent operations should not be performed.

SPMS Bit (RSPI Mode Select)

The SPMS bit selects SPI operation (4-wire method) or clock synchronous operation (3-wire method).
The SSLA0 to SSLA3 pins are not used in clock synchronous operation. The RSPCKA, MOSIA, and MISOA pins handle communications. If clock synchronous operation is to proceed in master mode (SPCR.MSTR = 1), the SPCMDm.CPHA bit can be set to either 0 or 1. Set the CPHA bit to 1 if clock synchronous operation is to proceed in slave mode (SPCR.MSTR = 0). Operation should not be performed if the CPHA bit is set to 0 when clock synchronous operation is to proceed in slave mode (SPCR.MSTR = 0).

TXMD Bit (Communications Operating Mode Select)

The TXMD bit selects full-duplex synchronous serial communications or transmit operations only.
When performing communications with the TXMD bit set to 1, the RSPI performs only transmit operations and not receive operations (refer to section 29.3.6, Communications Operating Mode).
When the TXMD bit is set to 1, receive buffer full interrupt requests cannot be used.

MODFEN Bit (Mode Fault Error Detection Enable)

The MODFEN bit enables or disables the detection of mode fault error (refer to section 29.3.8, Error Detection). In addition, the RSPI determines the I/O direction of the SSLA0 to SSLA3 pins based on combinations of the MODFEN and MSTR bits (refer to section 29.3.2, Controlling RSPI Pins).

MSTR Bit (RSPI Master/Slave Mode Select)

The MSTR bit selects master/slave mode of the RSPI. According to MSTR bit settings, the RSPI determines the direction of pins RSPCKA, MOSIA, MISOA, and SSLA0 to SSLA3.

SPEIE Bit (RSPI Error Interrupt Enable)

The SPEIE bit enables or disables the generation of RSPI error interrupt requests when the RSPI detects a mode fault error or underrun error and sets the SPSR.MODF flag to 1, when the RSPI detects an overrun error and sets the SPSR.OVRF flag to 1, or when the RSPI detects a parity error and sets the SPSR.PERF flag to 1 (refer to section 29.3.8, Error Detection).

SPTIE Bit (Transmit Buffer Empty Interrupt Enable)

The SPTIE bit enables or disables the generation of transmit buffer empty interrupt requests when the RSPI detects when the transmit buffer is empty.

A transmit buffer empty interrupt request when transmission starts is generated by setting the SPE and SPTIE bits to 1 at the same time or by setting the SPE bit to 1 after setting the SPTIE bit to 1.

Note that a transmit buffer interrupt is generated when the SPTIE bit is 1 even if the RSPI function is disabled (the SPTIE bit is changed to 0).

SPE Bit (RSPI Function Enable)

The SPE bit enables or disables the RSPI function.

When the SPSR.MODF flag is 1, the SPE bit cannot be set to 1. For details, refer to section 29.3.8, Error Detection.

Setting the SPE bit to 0 disables the RSPI function, and initializes a part of the module function. For details, refer to section 29.3.9, Initializing RSPI. Furthermore, a transmit buffer empty interrupt request is generated by the state of the SPE bit changing from 0 to 1 or from 1 to 0.

SPRIE Bit (RSPI Receive Buffer Full Interrupt Enable)

If the RSPI has detected a receive buffer full write after completion of a serial transfer, the SPRIE bit enables or disables the generation of an RSPI receive buffer full interrupt request.

29.2.2 RSPI Slave Select Polarity Register (SSLP)

Address(es): RSPI0.SSLP 0008 8381h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	SSL3P	SSL2P	SSL1P	SSL0P
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SSL0P	SSL0 Signal Polarity Setting	0: SSL0 signal is active low 1: SSL0 signal is active high	R/W
b1	SSL1P	SSL1 Signal Polarity Setting	0: SSL1 signal is active low 1: SSL1 signal is active high	R/W
b2	SSL2P	SSL2 Signal Polarity Setting	0: SSL2 signal is active low 1: SSL2 signal is active high	R/W
b3	SSL3P	SSL3 Signal Polarity Setting	0: SSL3 signal is active low 1: SSL3 signal is active high	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

If the contents of SSLP are changed while the SPCR.SPE bit is 1, subsequent operations should not be performed.

29.2.3 RSPI Pin Control Register (SPPCR)

Address(es): RSPI0.SPPCR 0008 8382h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	MOIFE	MOIFV	—	—	SPLP2	SPLP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SPLP	RSPI Loopback	0: Normal mode 1: Loopback mode (data is inverted for transmission)	R/W
b1	SPLP2	RSPI Loopback 2	0: Normal mode 1: Loopback mode (data is not inverted for transmission)	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	MOIFV	MOSI Idle Fixed Value	0: The level output on the MOSIA pin during MOSI idling corresponds to low 1: The level output on the MOSIA pin during MOSI idling corresponds to high	R/W
b5	MOIFE	MOSI Idle Value Fixing Enable	0: MOSI output value equals final data from previous transfer 1: MOSI output value equals the value set in the MOIFV bit	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

If the contents of SPPCR are changed while the SPCR.SPE bit is 1, subsequent operations should not be performed.

SPLP Bit (RSPI Loopback)

The SPLP bit selects the mode of the RSPI pins.

When the SPLP bit is set to 1, the RSPI shuts off the path between the MISOA pin and the shift register if the SPCR.MSTR bit is 1, and between the MOSIA pin and the shift register if the SPCR.MSTR bit is 0, and connects (inverts) the input path and output path for the shift register (loopback mode).

SPLP2 Bit (RSPI Loopback 2)

The SPLP2 bit selects the mode of the RSPI pins.

When the SPLP2 bit is set to 1, the RSPI shuts off the path between the MISOA pin and the shift register if the SPCR.MSTR bit is 1, and between the MOSIA pin and the shift register if the SPCR.MSTR bit is 0, and connects the input path and output path for the shift register (loopback mode).

MOIFV Bit (MOSI Idle Fixed Value)

If the MOIFE bit is 1 in master mode, the MOIFV bit determines the MOSIA pin output value during the SSL negation period (including the SSL retention period during a burst transfer).

MOIFE Bit (MOSI Idle Value Fixing Enable)

The MOIFE bit fixes the MOSIA output value when the RSPI in master mode is in an SSL negation period (including the SSL retention period during a burst transfer). When the MOIFE bit is 0, the RSPI outputs the last data from the previous serial transfer during the SSL negation period to the MOSIA pin. When the MOIFE bit is 1, the RSPI outputs the fixed value set in the MOIFV bit to the MOSIA pin.

29.2.4 RSPI Status Register (SPSR)

Address(es): RSPI0.SPSR 0008 8383h

	b7	b6	b5	b4	b3	b2	b1	b0
	SPRF	—	SPTEF	UDRF	PERF	MODF	IDLNF	OVRF
Value after reset:	0	0	1	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	OVRF	Overrun Error Flag	0: No overrun error occurs 1: An overrun error occurs	R/(W) *1
b1	IDLNF	RSPI Idle Flag	0: RSPI is in the idle state 1: RSPI is in the transfer state	R
b2	MODF	Mode Fault Error Flag	0: Neither a mode fault error nor an underrun error occurs 1: A mode fault error or an underrun error occurs	R/(W) *1
b3	PERF	Parity Error Flag	0: No parity error occurs 1: A parity error occurs	R/(W) *1
b4	UDRF	Underrun Error Flag	This flag is used with the MODF flag to check the state in terms of mode fault errors and underrun errors. b4 b2 0 0: Neither a mode fault error nor an underrun error occurs 0 1: A mode fault error occurs 1 1: An underrun error occurs	R/(W) *1, *2
b5	SPTEF	Transmit Buffer Empty Flag	0: Transmit buffer has valid data 1: Transmit buffer has no valid data	R/(W) *3
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	SPRF	Receive Buffer Full Flag	0: Receive buffer has no valid data 1: Receive buffer has valid data	R/(W) *3

Note 1. Only 0 can be written to clear the flag after reading 1.
Note 2. Clear the MODF and UDRF flags at the same time.
Note 3. The write value should be 1.

OVRF Flag (Overrun Error Flag)

The OVRF flag indicates the occurrence of an overrun error. In master mode (when the SPCR.MSTR bit is 1) and when the RSPCK clock auto-stop function is enabled (the SPCR2.SCKASE bit is 1), an overrun error does not occur; accordingly this flag does not become 1. For details, refer to section 29.3.8.1, Overrun Error.

[Setting condition]

- When the next serial transfer ends while the SPCR.TXMD bit is 0 and the receive buffer is full.

[Clearing condition]

- When SPSR is read while the OVRF flag is 1, and then 0 is written to the OVRF flag.

IDLNF Flag (RSPI Idle Flag)

The IDLNF flag indicates the transfer status of the RSPI.

[Setting condition]

Master mode

- Condition 1 and condition 2 are not satisfied in master mode under the [Clearing condition] below.

Slave mode

- The SPCR.SPE bit is 1 (enables the RSPI function)

[Clearing condition]

Master mode

- The following 1 is satisfied (condition 1) or all of the following 2 to 4 are satisfied (condition 2).

1. The SPCR.SPE bit is 0 (disables the RSPI function)
2. The transmit buffer (SPTX) is empty (data for the next transfer is not set)
3. The SPSSR.SPCP[2:0] bits are 000b (beginning of sequence control)
4. The RSPI internal sequencer has entered the idle state (status in which operations up to the next-access delay have finished)

Slave mode

- The SPCR.SPE bit is 0 (disables the RSPI function)

MODF Flag (Mode Fault Error Flag)

Indicates the occurrence of a mode fault error or an underrun error. The UDRF flag indicates whether the error is a mode fault error or an underrun error.

[Setting condition]

Multi-master mode

- When the input level of the SSLAi pin changes to the active level while the SPCR.MSTR bit is 1 (master mode) and the SPCR.MODFEN bit is 1 (mode fault error detection is enabled), the RSPI detects a mode fault error

Slave mode

- When the SSLAi pin is negated before the RSPCK cycle necessary for data transfer ends while the SPCR.MSTR bit is 0 (slave mode) and the SPCR.MODFEN bit is 1 (mode fault error detection is enabled), the RSPI detects a mode fault error
- When the serial transfer starts while the SPCR.SPE bit is 1 (enables the RSPI function) and the transmit data are not ready for output, the RSPI detects an underrun error

The active level of the SSLAi signal is determined by the SSLP.SSLiP bit (SSLi signal polarity setting bit).

[Clearing condition]

- When SPSR is read while the MODF flag is 1, and then 0 is written to the MODF flag

PERF Flag (Parity Error Flag)

Indicates the occurrence of a parity error.

[Setting condition]

- When a serial transfer ends while the SPCR.TXMD bit is 0 and the SPCR2.SPPE bit is 1, the RSPI detects a parity error

[Clearing condition]

- When SPSR is read while the PERF flag is 1, and then 0 is written to the PERF flag

UDRF Flag (Underrun Error Flag)

Indicates the occurrence of an underrun error. When this flag becomes 1, the MODF flag becomes 1 too. When the MODF flag is 1 and this flag is 0, the error is a mode fault error.

[Setting condition]

- When the serial transfer starts while the SPCR.MSTR bit is 0 (slave mode), the SPCR.SPE bit is 1 (enables the RSPI function) and the transmit data are not ready for output, the RSPI detects an underrun error

[Clearing condition]

- When 0 is written to the UDRF flag after reading the SPSR register while the UDRF flag is 1

SPTEF Flag (Transmit Buffer Empty Flag)

Indicates whether the transmit buffer (SPTX) in the RSPI data register has valid data.

[Setting condition]

- When the SPCR.SPE bit is 0 (disables the RSPI function)
- When data is transferred from the transmit buffer to the shift register

[Clearing condition]

- When the number of frames of transmit data specified by the SPDCR.SPFC[1:0] bits is written to the SPDR register

The SPDR register can be set only when the SPTEF flag is 1. The data in the transmit buffer is not updated when the SPDR register is set while the SPTEF flag is 0.

SPRF Flag (Receive Buffer Full Flag)

Indicates whether the receive buffer (SPRX) in the RSPI data register has valid data.

[Setting condition]

- When the number of frames of receive data specified by the SPDCR.SPFC[1:0] bits is transferred from shift register to the receive buffer (SPRX) while the SPCR.TXMD bit is 0 (full duplex) and the SPRF flag is 0.
  Note that the SPRF flag does not become 1 when the OVRF flag is 1.

[Clearing condition]

- When all of the received data are read from the SPDR register

29.2.5 RSPI Data Register (SPDR)

- When accessing in longword size

Address(es): RSPI0.SPDR 0008 8384h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

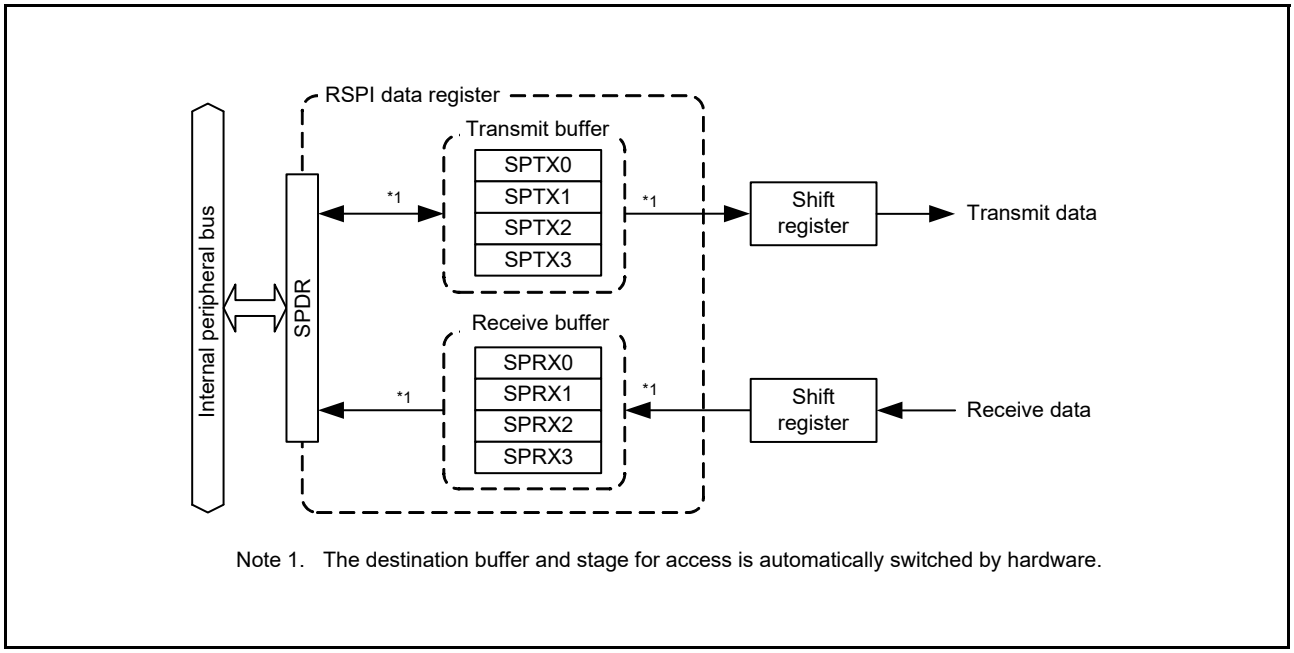
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

- When accessing in word size

Address(es): RSPI0.SPDR.H 0008 8384h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
								H								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SPDR is the interface with the buffers that hold data for transmission and reception by the RSPI.
When accessing in longwords (the SPLW bit is 1), access SPDR in 32-bit units.
When accessing in words (the SPLW bit is 0), access SPDR.H in 16-bit units.
The transmit buffer (SPTX) and receive buffer (SPRX) are independent but are both mapped to SPDR. Figure 29.2 shows the Configuration of SPDR.



Note 1. The destination buffer and stage for access is automatically switched by hardware.

Figure 29.2 Configuration of SPDR

The transmit and receive buffers each have four stages. The number of stages to be used is selectable by the number of frames specification bits in the RSPI data control register (SPDCR.SPFC[1:0]). The eight stages of the buffer are all

mapped to the single address of SPDR.
Data written to SPDR are written to a transmit-buffer stage (SPTXn) (n = 0 to 3) and then transmitted from the buffer. The receive buffer holds received data on completion of reception. The receive buffer is not updated if an overrun is generated.
Furthermore, if the data length is other than 32 bits, bits not referred to in SPTXn (n = 0 to 3) are stored in the corresponding bits in SPRXn. For example, if the data length is 9 bits, received data are stored in the SPRXn[8:0] bits and the SPTXn[31:9] bits are stored in the SPRXn[31:9] bits.

(1) Bus Interface

SPDR is the interface with 32-bit wide transmit and receive buffers, each of which has four stages, for a total of 32 bytes. In other words, the 32 bytes are mapped to the 4-byte address space for SPDR. Furthermore, the unit of access for SPDR is selected by the SPDCR.SPLW bit.
Data for transmission should be flush with the LSB end of the register. Received data are stored flush with the LSB end. Operations involved in writing to and reading from SPDR are described below.

(a) Writing

Data written to SPDR are written to a transmit buffer (SPTXn). This is not influenced by the value of the SPDCR.SPRDTD bit unlike when reading from SPDR.
The transmit buffer includes a transmit buffer write pointer which is automatically updated to indicate the next stage each time data are written to SPDR.
Figure 29.3 shows the configuration of the bus interface with the transmit buffer in the case of writing to SPDR.

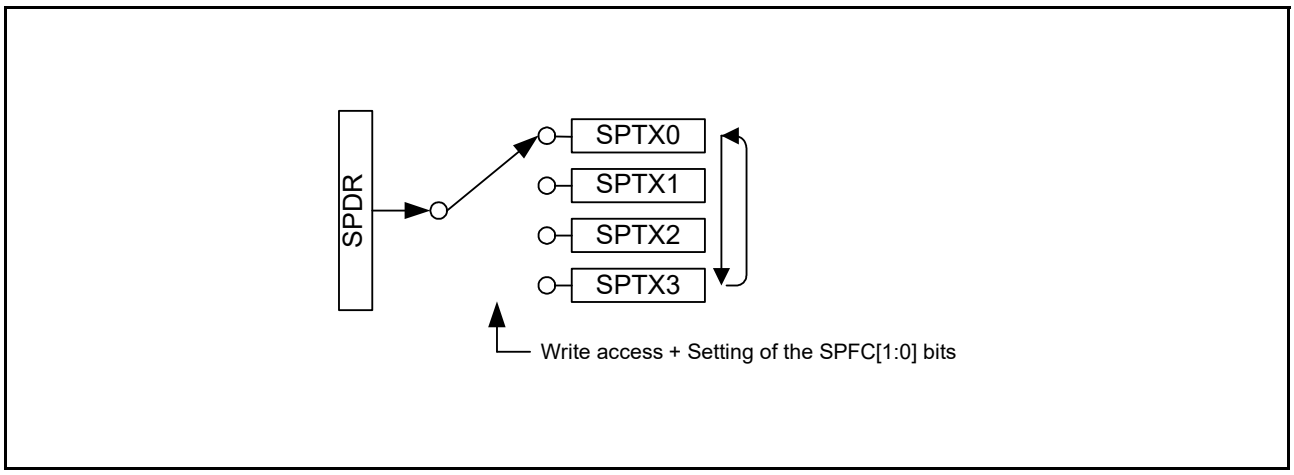


Figure 29.3 Configuration of SPDR (Writing)

The sequence for switching the transmit buffer write pointer differs with the setting of the number of frames specification bits in the RSPI data control register (SPDCR.SPFC[1:0]).

- Settings of the SPFC[1:0] bits and sequence of switching the pointer among SPTX0 to SPTX3.
  When the SPFC[1:0] bits are 00b: SPTX0 → SPTX0 → SPTX0 → …
  When the SPFC[1:0] bits are 01b: SPTX0 → SPTX1 → SPTX0 → SPTX1 → …
  When the SPFC[1:0] bits are 10b: SPTX0 → SPTX1 → SPTX2 → SPTX0 → SPTX1 → …
  When the SPFC[1:0] bits are 11b: SPTX0 → SPTX1 → SPTX2 → SPTX3 → SPTX0 → SPTX1 → …

When 1 is written to the RSPI function enable bit in the RSPI control register (SPCR.SPE) while the bit's current value is 0, SPTX0 will be the destination the next time writing proceeds.
When writing to the transmit buffer (SPTXn) after generation of the transmit buffer empty interrupt (after the SPSR.SPTEF flag becomes 1), write the number of frames set by the number of frames specification bits (SPFC[1:0]) in

the RSPI data control register (SPDCR). Even if the number of frames is written to the transmit buffer (SPTXn), the value of the buffer is not updated after completion of the writing and before generation of the next transmit buffer empty interrupt (while the SPSR.SPTEF flag is 0).

(b) Reading

SPDR can be read to read the value of a receive buffer (SPRXn) or a transmit buffer (SPTXn). The setting of the RSPI receive/transmit data select bit in the RSPI data control register (SPDCR.SPRDTD) selects whether reading is of the receive or transmit buffer.

The sequence of reading the SPDR register is controlled by independent pointers, receive buffer read pointer and transmit buffer read pointer.

Figure 29.4 shows the configuration of the bus interface with the receive and transmit buffers in the case of reading from SPDR.

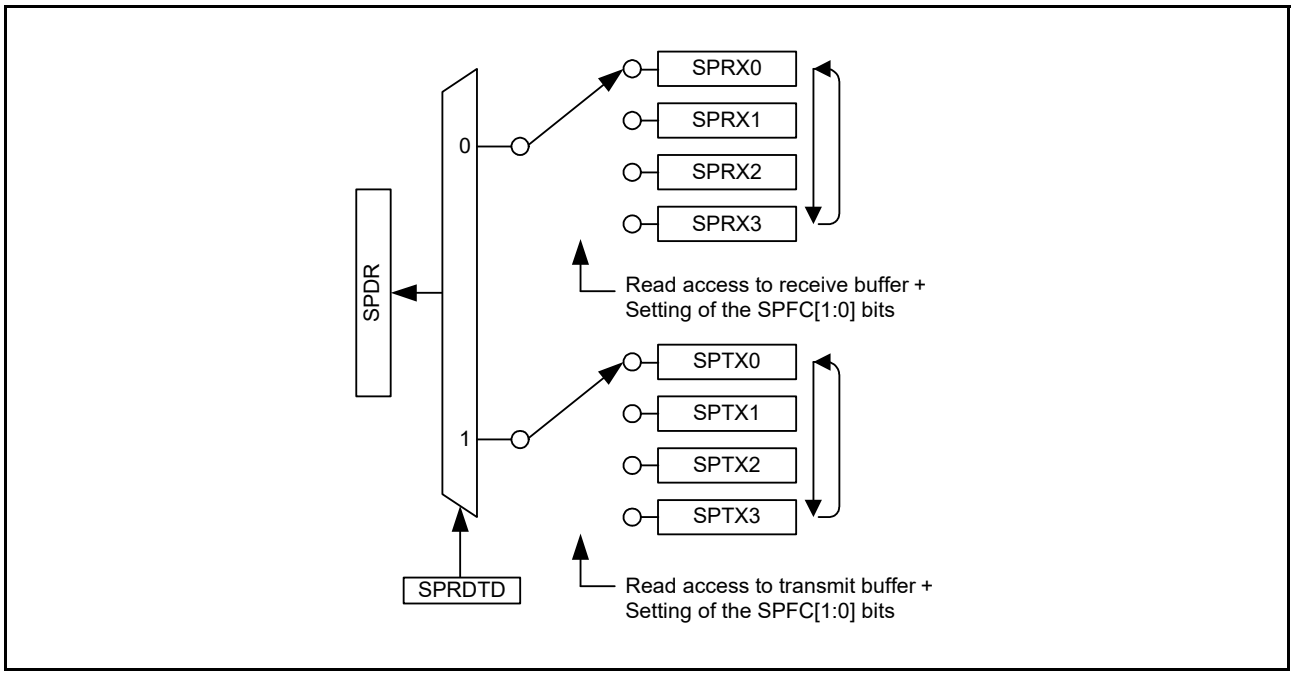


Figure 29.4 Configuration of SPDR (Reading)

Reading the receive buffer switches the receive buffer read pointer to the next buffer automatically.

The sequence of switching the receive buffer read pointer is the same as that for the transmit buffer write pointer. However, when 1 is written to the RSPI function enable bit in the RSPI control register (SPCR.SPE) while the bit's current value is 0, SPRX0 will be indicated by the buffer read pointer the next time reading proceeds.

The transmit buffer read pointer is updated when writing to SPDR, and not updated when reading from the transmit buffer. When reading from the transmit buffer, the value most recently written to SPDR is read. However, after generation of the transmit buffer empty interrupt, the values read from the transmit buffer are all 0 in the interval after completion of writing the number of frames of data specified in the number of frames specification bits (SPDCR.SPFC[1:0]) and before generation of the next buffer empty interrupt (while the SPSR.SPTEF flag is 0).

29.2.6 RSPI Sequence Control Register (SPSCR)

Address(es): RSPI0.SPSCR 0008 8388h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SPSLN[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	SPSLN[2:0]	RSPI Sequence Length Specification	b2 b0 Sequence Length — Referenced SPCMD0 to SPCMD7 (No.) 0 0 0: 1 — 0→0→… 0 0 1: 2 — 0→1→0→… 0 1 0: 3 — 0→1→2→0→… 0 1 1: 4 — 0→1→2→3→0→… 1 0 0: 5 — 0→1→2→3→4→0→… 1 0 1: 6 — 0→1→2→3→4→5→0→… 1 1 0: 7 — 0→1→2→3→4→5→6→0→… 1 1 1: 8 — 0→1→2→3→4→5→6→7→0→… The order in which the SPCMD0 to SPCMD7 registers are to be referenced is changed according to the sequence length that is set in these bits. The relationship among the setting of these bits, sequence length, and SPCMD0 to SPCMD7 registers referenced by the RSPI is shown above. However, the RSPI in slave mode references SPCMD0.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SPSCR sets the sequence length when the RSPI operates in master mode. When changing the SPSCR.SPSLN[2:0] bits while both the SPCR.MSTR and SPCR.SPE bits are 1, the bits should be changed while the SPSR.IDLNF flag is 0.

SPSLN[2:0] Bits (RSPI Sequence Length Specification)

The SPSLN[2:0] bits specify a sequence length when the RSPI in master mode performs sequential operations. The RSPI in master mode changes SPCMD0 to SPCMD7 registers to be referenced and the order in which they are referenced according to the sequence length that is set in the SPSLN[2:0] bits.
In slave mode, SPCMD0 is referred.

29.2.7 RSPI Sequence Status Register (SPSSR)

Address(es): RSPI0.SPSSR 0008 8389h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	SPECM[2:0]			—	SPCP[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	SPCP[2:0]	RSPI Command Pointer	b2 b0 0 0 0: SPCMD0 0 0 1: SPCMD1 0 1 0: SPCMD2 0 1 1: SPCMD3 1 0 0: SPCMD4 1 0 1: SPCMD5 1 1 0: SPCMD6 1 1 1: SPCMD7	R
b3	—	Reserved	This bit is read as 0.	R
b6 to b4	SPECM[2:0]	RSPI Error Command	b6 b4 0 0 0: SPCMD0 0 0 1: SPCMD1 0 1 0: SPCMD2 0 1 1: SPCMD3 1 0 0: SPCMD4 1 0 1: SPCMD5 1 1 0: SPCMD6 1 1 1: SPCMD7	R
b7	—	Reserved	This bit is read as 0.	R

SPSSR indicates the sequence control status when the RSPI operates in master mode.
Any writing to SPSSR is ignored.

SPCP[2:0] Bits (RSPI Command Pointer)

The SPCP[2:0] bits indicate SPCMDm that is currently pointed to by the pointer during sequence control by the RSPI. For the RSPI's sequence control, refer to section 29.3.10.1, Master Mode Operation.

SPECM[2:0] Bits (RSPI Error Command)

The SPECM[2:0] bits indicate SPCMDm that is specified by the SPCP[2:0] bits when an error is detected during sequence control by the RSPI. The RSPI updates the SPECM[2:0] bits only when an error is detected. If both the SPSR.OVRF and SPSR.MODF flags are 0 and there is no error, the values of the SPECM[2:0] bits have no meaning. For the RSPI's error detection function, refer to section 29.3.8, Error Detection. For the RSPI's sequence control, refer to section 29.3.10.1, Master Mode Operation.

29.2.8 RSPI Bit Rate Register (SPBR)

Address(es): RSPI0.SPBR 0008 838Ah

SPBR sets the bit rate in master mode. If the contents of SPBR are changed while both the SPCR.MSTR and SPCR.SPE bits are 1, subsequent operations should not be performed.

When the RSPI is used in slave mode, the bit rate depends on the bit rate of the input clock (bit rate satisfying the electrical characteristics should be used) regardless of the settings of SPBR and the SPCMDm.BRDV[1:0] bits (bit rate division setting bits).
The bit rate is determined by combinations of the SPBR setting and the SPCMDm.BRDV[1:0] bit setting. The equation for calculating the bit rate is given below. In the equation, n denotes an SPBR setting (0, 1, 2, …, 255), and N denotes a BRDV[1:0] bit setting (0, 1, 2, 3).

$$\text{Bit rate} = \frac{f(PCLK)}{2 \times (n+1) \times 2^{N}}$$

Table 29.3 lists examples of the relationship among the SPBR settings, the BRDV[1:0] settings, and bit rates.
Use the bit rate that meets electrical characteristics based on the AC specifications of the target device.

Table 29.3 Relationship among SPBR Settings, BRDV[1:0] Settings, and Bit Rates

SPBR (n)	BRDV[1:0] Bits (N)	Division Ratio	Bit Rate		
			PCLK = 32 MHz	PCLK = 36MHz	PCLK = 40MHz
0	0	2	16.0 Mbps	18.0 Mbps	20.0 Mbps
1	0	4	8.00 Mbps	9.00 Mbps	10.0 Mbps
2	0	6	5.33 Mbps	6.00 Mbps	6.67 Mbps
3	0	8	4.00 Mbps	4.50 Mbps	5.00 Mbps
4	0	10	3.20 Mbps	3.60 Mbps	4.00 Mbps
5	0	12	2.67 Mbps	3.00 Mbps	3.33 Mbps
5	1	24	1.33 Mbps	1.50 Mbps	1.67 Mbps
5	2	48	667 kbps	750 kbps	833 kbps
5	3	96	333 kbps	375 kbps	417 kbps
255	3	4096	7.81 kbps	8.80 kbps	9.78 kbps

29.2.9 RSPI Data Control Register (SPDCR)

Address(es): RSPI0.SPDCR 0008 838Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	SPLW	SPRDTD	—	—	SPFC[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	SPFC[1:0]	Number of Frames Specification	b1 b0 0 0: 1 frame 0 1: 2 frames 1 0: 3 frames 1 1: 4 frames	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	SPRDTD	RSPI Receive/Transmit Data Select	0: SPDR values are read from the receive buffer 1: SPDR values are read from the transmit buffer (but only if the transmit buffer is empty)	R/W
b5	SPLW	RSPI Longword Access/ Word Access Specification	0: SPDR is accessed in words 1: SPDR is accessed in longwords	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Up to four frames can be transmitted or received in one round of transmission or reception activation. The amount of data in each transfer is controlled by the combination of the SPCMDm.SPB[3:0] bits, the SPSCR.SPSLN[2:0] bits, and the SPDCR.SPFC[1:0] bits.
When changing the SPDCR.SPFC[1:0] bits while the SPCR.SPE bit is 1, the bits should be changed while the SPSR.IDLNF flag is 0.

SPFC[1:0] Bits (Number of Frames Specification)

The SPFC[1:0] bits specify the number of frames that can be stored in SPDR (per transfer activation). Up to four frames can be transmitted or received in one round of transmission or reception, and the amount of data is determined by the combination of the SPSCR.SPSLN[2:0] bits, and the SPDCR.SPFC[1:0] bits. Furthermore, the setting of the SPFC[1:0] bits adjusts the number of frames for generation of RSPI receive buffer full interrupt, and start of transmission or generation of transmit buffer empty interrupts.
When the number of frames of transmit data specified by SPFC[1:0] bits is written to the SPDR register, the SPSR.SPTEF flag becomes 0 and transmission starts. Then, when the specified number of frames of transmit data has been transferred to the shift register, the SPTEF flag becomes 1 and the RSPI transmit buffer empty interrupt is generated.
When the number of frames specified by the SPFC[1:0] bits are received, the SPSR.SPRF flag becomes 1 and the RSPI receive buffer full interrupt is generated.
Table 29.4 lists the frame configurations that can be stored in SPDR and examples of combinations of settings for transmission and reception. If combinations of settings other than those shown in the examples are made, subsequent operations should not be performed.

Table 29.4 Settable Combinations of SPSLN[2:0] Bits and SPFC[1:0] Bits

Setting	SPSLN[2:0]	SPFC[1:0]	Number of Frames in a Single Sequence	Number of Frames at which Transmit Buffer or Receive Buffer Status Becomes “Has Valid Data”
1-1	000b	00b	1	1
1-2	000b	01b	2	2
1-3	000b	10b	3	3
1-4	000b	11b	4	4
2-1	001b	01b	2	2
2-2	001b	11b	4	4
3	010b	10b	3	3
4	011b	11b	4	4
5	100b	00b	5	1
6	101b	00b	6	1
7	110b	00b	7	1
8	111b	00b	8	1

SPRDTD Bit (RSPI Receive/Transmit Data Select)

The SPRDTD bit selects whether the SPDR reads values from the receive buffer or from the transmit buffer.
If reading is from the transmit buffer, the value written to SPDR register immediately beforehand is read.
When reading the transmit buffer, do so before writing of the number of frames set in the SPFC[1:0] bits is finished and after generation of the transmit buffer empty interrupt (While the SPSR.SPTEF flag is 1).
For details, refer to section 29.2.5, RSPI Data Register (SPDR).

SPLW Bit (RSPI Longword Access/Word Access Specification)

The SPLW bit specifies the access width for SPDR. Access to the SPDR register in words when the SPLW bit is 0 and in longwords when the SPLW bit is 1.
Also, when the SPLW bit is 0, set the SPCMDm.SPB[3:0] bits (RSPI data length setting bits) to 8 to 16 bits. When 20, 24, or 32 bits is specified, operations should not be performed.

29.2.10 RSPI Clock Delay Register (SPCKD)

Address(es): RSPI0.SPCKD 0008 838Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SCKDL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	SCKDL[2:0]	RSPCK Delay Setting	b2 b0 0 0 0: 1 RSPCK 0 0 1: 2 RSPCK 0 1 0: 3 RSPCK 0 1 1: 4 RSPCK 1 0 0: 5 RSPCK 1 0 1: 6 RSPCK 1 1 0: 7 RSPCK 1 1 1: 8 RSPCK	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SPCKD sets a period from the beginning of SSLAi signal assertion to RSPCK oscillation (RSPCK delay) when the SPCMDm.SCKDEN bit is 1. If the contents of SPCKD are changed while both the SPCR.MSTR and SPCR.SPE bits are 1, subsequent operations should not be performed.

SCKDL[2:0] Bits (RSPCK Delay Setting)

The SCKDL[2:0] bits set an RSPCK delay value when the SPCMDm.SCKDEN bit is 1.
When using the RSPI in slave mode, set the SCKDL[2:0] bits to 000b.

29.2.11 RSPI Slave Select Negation Delay Register (SSLND)

Address(es): RSPI0.SSLND 0008 838Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SLNDL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	SLNDL[2:0]	SSL Negation Delay Setting	b2 b0 0 0 0: 1 RSPCK 0 0 1: 2 RSPCK 0 1 0: 3 RSPCK 0 1 1: 4 RSPCK 1 0 0: 5 RSPCK 1 0 1: 6 RSPCK 1 1 0: 7 RSPCK 1 1 1: 8 RSPCK	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

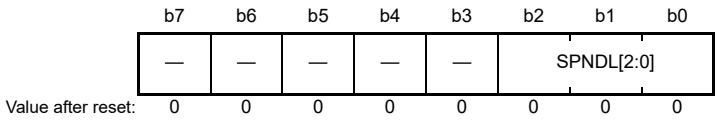
SSLND sets a period (SSL negation delay) from the transmission of a final RSPCK edge to the negation of the SSLAi signal during a serial transfer by the RSPI in master mode. If the contents of SSLND are changed while both the SPCR.MSTR and SPCR.SPE bits are 1, subsequent operations should not be performed.

SLNDL[2:0] Bits (SSL Negation Delay Setting)

The SLNDL[2:0] bits set an SSL negation delay value when the RSPI is in master mode.
When using the RSPI in slave mode, set the SLNDL[2:0] bits to 000b.

29.2.12 RSPI Next-Access Delay Register (SPND)

Address(es): RSPI0.SPND 0008 838Eh



Bit	Symbol	Bit Name	Description	R/W
b2 to b0	SPNDL[2:0]	RSPI Next-Access Delay Setting	b2 b0 0 0 0: 1 RSPCK + 2 PCLK 0 0 1: 2 RSPCK + 2 PCLK 0 1 0: 3 RSPCK + 2 PCLK 0 1 1: 4 RSPCK + 2 PCLK 1 0 0: 5 RSPCK + 2 PCLK 1 0 1: 6 RSPCK + 2 PCLK 1 1 0: 7 RSPCK + 2 PCLK 1 1 1: 8 RSPCK + 2 PCLK	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SPND sets a non-active period (next-access delay) of the SSLAi signal after termination of a serial transfer when the SPCMDm.SPNDEN bit is 1. If the contents of SPND are changed while both the SPCR.MSTR and SPCR.SPE bits are 1, subsequent operations should not be performed.

SPNDL[2:0] Bits (RSPI Next-Access Delay Setting)

The SPNDL[2:0] bits set a next-access delay when the SPCMDm.SPNDEN bit is 1.
When using the RSPI in slave mode, set the SPNDL[2:0] bits to 000b.

29.2.13 RSPI Control Register 2 (SPCR2)

Address(es): RSPI0.SPCR2 0008 838Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SCKASE	PTE	SPIIE	SPOE	SPPE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SPPE	Parity Enable	0: Does not add the parity bit to transmit data and does not check the parity bit of receive data 1: Adds the parity bit to transmit data and checks the parity bit of receive data (when SPCR.TXMD = 0) Adds the parity bit to transmit data but does not check the parity bit of receive data (when SPCR.TXMD = 1)	R/W
b1	SPOE	Parity Mode	0: Selects even parity for use in transmission and reception 1: Selects odd parity for use in transmission and reception	R/W
b2	SPIIE	RSPI Idle Interrupt Enable	0: Disables the generation of idle interrupt requests 1: Enables the generation of idle interrupt requests	R/W
b3	PTE	Parity Self-Diagnosis	0: Disables the self-diagnosis function of the parity circuit 1: Enables the self-diagnosis function of the parity circuit	R/W
b4	SCKASE	RSPCK Auto-Stop Function Enable	0: Disables the RSPCK auto-stop function 1: Enables the RSPCK auto-stop function	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

If the SPPE, SPOE, or SCKASE bit in SPCR2 is changed while the SPCR.SPE bit is 1, subsequent operations should not be performed.

SPPE Bit (Parity Enable)

The SPPE bit enables or disables the parity function.

The parity bit is added to transmit data and parity checking is performed for receive data when the SPCR.TXMD bit is 0 and the SPCR2.SPPE bit is 1.

The parity bit is added to transmit data but parity checking is not performed for receive data when the SPCR.TXMD bit is 1 and the SPCR2.SPPE bit is 1.

SPOE Bit (Parity Mode)

The SPOE bit specifies odd or even parity.

When even parity is set, parity bit addition is performed so that the total number of 1-bits in the transmit/receive character plus the parity bit is even. Similarly, when odd parity is set, parity bit addition is performed so that the total number of 1-bits in the transmit/receive character plus the parity bit is odd.

The SPOE bit is valid only when the SPPE bit is 1.

SPIIE Bit (RSPI Idle Interrupt Enable)

The SPIIE bit enables or disables the generation of RSPI idle interrupt requests when the RSPI being in the idle state is detected and the SPSR.IDLNF flag is set to 0.

PTE Bit (Parity Self-Diagnosis)

The PTE bit enables the self-diagnosis function of the parity circuit in order to check whether the parity function is operating correctly.

SCKASE Bit (RSPCK Auto-Stop Function Enable)

The SCKASE bit enables or disables the RSPCK auto-stop function. When this function is enabled, the RSPCK clock is stopped before an overrun error occurs when data is received in master mode. For details, refer to section 29.3.8.1, Overrun Error.

29.2.14 RSPI Command Registers 0 to 7 (SPCMD0 to SPCMD7)

Address(es): RSPI0.SPCMD0 0008 8390h, RSPI0.SPCMD1 0008 8392h, RSPI0.SPCMD2 0008 8394h, RSPI0.SPCMD3 0008 8396h, RSPI0.SPCMD4 0008 8398h, RSPI0.SPCMD5 0008 839Ah, RSPI0.SPCMD6 0008 839Ch, RSPI0.SPCMD7 0008 839Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SCKDEN	SLNDEN	SPNDEN	LSBF	SPB[3:0]				SSLKP	SSLA[2:0]			BRDV[1:0]		CPOL	CPHA
Value after reset:	0	0	0	0	0	1	1	1	0	0	0	0	1	1	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	CPHA	RSPCK Phase Setting	0: Data sampling on odd edge, data variation on even edge 1: Data variation on odd edge, data sampling on even edge	R/W
b1	CPOL	RSPCK Polarity Setting	0: RSPCK is low when idle 1: RSPCK is high when idle	R/W
b3, b2	BRDV[1:0]	Bit Rate Division Setting	b3 b2 0 0: These bits select the base bit rate 0 1: These bits select the base bit rate divided by 2 1 0: These bits select the base bit rate divided by 4 1 1: These bits select the base bit rate divided by 8	R/W
b6 to b4	SSLA[2:0]	SSL Signal Assertion Setting	b6 b4 0 0 0: SSL0 0 0 1: SSL1 0 1 0: SSL2 0 1 1: SSL3 1 x x: Setting prohibited x: Don't care	R/W
b7	SSLKP	SSL Signal Level Keeping	0: Negates all SSL signals upon completion of transfer 1: Keeps the SSL signal level from the end of transfer until the beginning of the next access	R/W
b11 to b8	SPB[3:0]	RSPI Data Length Setting	b11 b8 0100 to 0111: 8 bits 1 0 0 0: 9 bits 1 0 0 1: 10 bits 1 0 1 0: 11 bits 1 0 1 1: 12 bits 1 1 0 0: 13 bits 1 1 0 1: 14 bits 1 1 1 0: 15 bits 1 1 1 1: 16 bits 0 0 0 0: 20 bits 0 0 0 1: 24 bits 0010, 0011: 32 bits	R/W
b12	LSBF	RSPI LSB First	0: MSB first 1: LSB first	R/W
b13	SPNDEN	RSPI Next-Access Delay Enable	0: A next-access delay of 1 RSPCK + 2 PCLK 1: A next-access delay is equal to the setting of the RSPI next-access delay register (SPND)	R/W
b14	SLNDEN	SSL Negation Delay Setting Enable	0: An SSL negation delay of 1 RSPCK 1: An SSL negation delay is equal to the setting of the RSPI slave select negation delay register (SSLND)	R/W
b15	SCKDEN	RSPCK Delay Setting Enable	0: An RSPCK delay of 1 RSPCK 1: An RSPCK delay is equal to the setting of the RSPI clock delay register (SPCKD)	R/W

SPCMDm register is used to set a transfer format for the RSPI in master mode. Each channel has eight RSPI command registers (SPCMD0 to SPCMD7). Some of the bits in SPCMD0 register is used to set a transfer mode for the RSPI in slave mode. The RSPI in master mode sequentially references SPCMDm register according to the settings in the SPSCR.SPSLN[2:0] bits, and executes the serial transfer that is set in the referenced SPCMDm register.
SPCMDm register should be set while the transmit buffer is empty (data for the next transfer is not set) and before setting of the data that is to be transmitted when that SPCMDm register is referenced.
SPCMDm that is referenced by the RSPI in master mode can be checked by means of the SPSSR.SPCP[2:0] bits. If the contents of SPCMDm are changed while the SPCR.MSTR bit is 0 and the SPCR.SPE bit is 1, subsequent operations should not be performed.

CPHA Bit (RSPCK Phase Setting)

The CPHA bit sets an RSPCK phase of the RSPI in master mode or slave mode. Data communications between RSPI modules require the same RSPCK phase setting between the modules.

CPOL Bit (RSPCK Polarity Setting)

The CPOL bit sets an RSPCK polarity of the RSPI in master mode or slave mode. Data communications between RSPI modules require the same RSPCK polarity setting between the modules.

BRDV[1:0] Bits (Bit Rate Division Setting)

The BRDV[1:0] bits are used to determine the bit rate. A bit rate is determined by combinations of the settings in the BRDV[1:0] bits and SPBR (refer to section 29.2.8, RSPI Bit Rate Register (SPBR)). The settings in SPBR determine the base bit rate. The settings in the BRDV[1:0] bits are used to select a bit rate which is obtained by dividing the base bit rate by 1, 2, 4, or 8. In SPCMDm register, different BRDV[1:0] bit settings can be specified. This enables execution of serial transfers at a different bit rate for each command.

SSLA[2:0] Bits (SSL Signal Assertion Setting)

The SSLA[2:0] bits control the SSLAi signal assertion when the RSPI performs serial transfers in master mode.
Setting the SSLA[2:0] bits controls the assertion for the SSLAi signal. When an SSLAi signal is asserted, its polarity is determined by the set value in the corresponding SSLP. When the SSLA[2:0] bits are set to 000b in multi-master mode, serial transfers are performed with all the SSL signals in the negated state (as the SSLA0 pin acts as input).
When using the RSPI in slave mode, set the SSLA[2:0] bits to 000b.

SSLKP Bit (SSL Signal Level Keeping)

When the RSPI in master mode performs a serial transfer, the SSLKP bit specifies whether the SSLAi signal level for the current command is to be kept or negated between the SSL negation timing associated with the current command and the SSL assertion timing associated with the next command.
Setting the SSLKP bit to 1 enables a burst transfer. For details, refer to section 29.3.10.1, Master Mode Operation (4) Burst Transfer.
When using the RSPI in slave mode, the SSLKP bit should be set to 0.

SPB[3:0] Bits (RSPI Data Length Setting)

The SPB[3:0] bits set a transfer data length for the RSPI in master mode or slave mode. When the SPDCR.SPLW bit is 0, set the SPB[3:0] bits to “0100b” (8 bits) to “1111b” (16 bits).

LSBF Bit (RSPI LSB First)

The LSBF bit sets the data format of the RSPI in master mode or slave mode to MSB first or LSB first.

SPNDEN Bit (RSPI Next-Access Delay Enable)

The SPNDEN bit sets the period from the time the RSPI in master mode terminates a serial transfer and sets the SSLAi signal inactive until the RSPI enables the SSLAi signal assertion for the next access (next-access delay). If the SPNDEN bit is 0, the RSPI sets the next-access delay to 1 RSPCK + 2 PCLK. If the SPNDEN bit is 1, the RSPI inserts a next-access delay in compliance with the SPND setting.

When using the RSPI in slave mode, the SPNDEN bit should be set to 0.

SLNDEN Bit (SSL Negation Delay Setting Enable)

The SLNDEN bit sets the period from the time the RSPI in master mode stops RSPCK oscillation until the RSPI sets the SSLAi signal inactive (SSL negation delay). If the SLNDEN bit is 0, the RSPI sets the SSL negation delay to 1 RSPCK. If the SLNDEN bit is 1, the RSPI negates the SSL signal at an SSL negation delay in compliance with the SSLND setting.

When using the RSPI in slave mode, the SLNDEN bit should be set to 0.

SCKDEN Bit (RSPCK Delay Setting Enable)

The SCKDEN bit sets the period from the point when the RSPI in master mode activates the SSLAi signal until the RSPCK starts oscillation (RSPI clock delay). If the SCKDEN bit is 0, the RSPI sets the RSPCK delay to 1 RSPCK. If the SCKDEN bit is 1, the RSPI starts the oscillation of RSPCK at an RSPCK delay in compliance with the SPCKD setting.

When using the RSPI in slave mode, the SCKDEN bit should be set to 0.

29.3 Operation

In this section, the serial transfer period means a period from the beginning of driving valid data to the fetching of the final valid data.

29.3.1 Overview of RSPI Operations

The RSPI is capable of synchronous serial transfers in slave mode (SPI operation), single-master mode (SPI operation), multi-master mode (SPI operation), slave mode (clock synchronous operation), and master mode (clock synchronous operation). A particular mode of the RSPI can be selected by using the MSTR, MODFEN, and SPMS bits in SPCR. Table 29.5 lists the relationship between RSPI modes and SPCR settings, and a description of each mode.

Table 29.5 Relationship between RSPI Modes and SPCR Settings and Description of Each Mode

Mode	Slave (SPI Operation)	Single-Master (SPI Operation)	Multi-Master (SPI Operation)	Slave (Clock Synchronous Operation)	Master (Clock Synchronous Operation)
MSTR bit setting	0	1	1	0	1
MODFEN bit setting	0 or 1	0	1	0	0
SPMS bit setting	0	0	0	1	1
RSPCKA signal	Input	Output	Output/Hi-Z	Input	Output
MOSIA signal	Input	Output	Output/Hi-Z	Input	Output
MISOA signal	Output/Hi-Z	Input	Input	Output	Input
SSLA0 signal	Input	Output	Input	Hi-Z*1	Hi-Z*1
SSLA1 to SSLA3 signals	Hi-Z*1	Output	Output/Hi-Z	Hi-Z*1	Hi-Z*1
SSL polarity change function	Supported	Supported	Supported	—	—
Transfer rate	Up to PCLK/6	Up to PCLK/2	Up to PCLK/2	Up to PCLK/6	Up to PCLK/2
Clock source	RSPCK input	On-chip baud rate generator	On-chip baud rate generator	RSPCK input	On-chip baud rate generator
Clock polarity	Two				
Clock phase	Two	Two	Two	One (CPHA = 1)	Two
First transfer bit	MSB/LSB				
Transfer data length	8 to 16, 20, 24, 32 bits				
Burst transfer	Possible (CPHA = 1)	Possible (CPHA = 0,1)	Possible (CPHA = 0,1)	—	—
RSPCK delay control	Not supported	Supported	Supported	Not supported	Supported
SSL negation delay control	Not supported	Supported	Supported	Not supported	Supported
Next-access delay control	Not supported	Supported	Supported	Not supported	Supported
Transfer activation method	SSL input active or RSPCK oscillation	Transmit buffer is written to at generation of a transmit buffer empty interrupt request or when the SPTEF flag is 1	Transmit buffer is written to at generation of a transmit buffer empty interrupt request or when the SPTEF flag is 1	RSPCK oscillation	Transmit buffer is written to at generation of a transmit buffer empty interrupt request or when the SPTEF flag is 1
Sequence control	Not supported	Supported	Supported	Not supported	Supported
Transmit buffer empty detection	Supported				
Receive buffer full detection	Supported*2				
Overrun error detection	Supported*2	Supported*2, *4	Supported*2, *4	Supported*2	Supported*2
Underrun error detection	Supported	Not supported	Not supported	Supported	Not supported
Parity error detection	Supported*2,*3				
Mode fault error detection	Supported (MODFEN = 1)	Not supported	Supported	Not supported	Not supported

Note 1. This function is not supported in this mode.
Note 2. When the SPCR.TXMD bit is 1, receiver buffer full detection, overrun error detection, and parity error detection are not performed.
Note 3. When the SPCR2.SPPE bit is 0, parity error detection is not performed.
Note 4. When the SPCR2.SCKASE bit is 1, overrun error detection does not proceed.

29.3.2 Controlling RSPI Pins

According to the MSTR, MODFEN, and SPMS bits in SPCR and the ODRn.Bi bit for I/O ports, the RSPI can switch pin states. Table 29.6 lists the relationship between pin states and bit settings. Setting the ODRn.Bi bit for an I/O port to 0 selects CMOS output; setting it to 1 selects open-drain output. The I/O port settings should follow this relationship.

Table 29.6 Relationship between Pin States and Bit Settings

Mode	Pin	Pin State*2	
		ODRn.Bi Bit for I/O Ports = 0	ODRn.Bi Bit for I/O Ports = 1
Single-master mode (SPI operation) (MSTR = 1, MODFEN = 0, SPMS = 0)	RSPCKA	CMOS output	Open-drain output
	SSLA0 to SSLA3	CMOS output	Open-drain output
	MOSIA	CMOS output	Open-drain output
	MISOA	Input	Input
Multi-master mode (SPI operation) (MSTR = 1, MODFEN = 1, SPMS = 0)	RSPCKA*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	SSLA0	Input	Input
	SSLA1 to SSLA3*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	MOSIA*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	MISOA	Input	Input
Slave mode (SPI operation) (MSTR = 0, SPMS = 0)	RSPCKA	Input	Input
	SSLA0	Input	Input
	SSLA1 to SSLA3*5	Hi-Z*1	Hi-Z*1
	MOSIA	Input	Input
	MISOA*4	CMOS output/Hi-Z	Open-drain output/Hi-Z
Master mode (Clock synchronous operation) (MSTR = 1, MODFEN = 0, SPMS = 1)	RSPCKA	CMOS output	Open-drain output
	SSLA0 to SSLA3*5	Hi-Z*1	Hi-Z*1
	MOSIA	CMOS output	Open-drain output
	MISOA	Input	Input
Slave mode (Clock synchronous operation) (MSTR = 0, SPMS = 1)	RSPCKA	Input	Input
	SSLA0 to SSLA3*5	Hi-Z*1	Hi-Z*1
	MOSIA	Input	Input
	MISOA	CMOS output	Open-drain output

Note 1. This function is not supported in this mode.
Note 2. RSPI settings are not reflected in the multiplex pins for which the RSPI function is not selected.
Note 3. When SSLA0 is at the active level, the pin state is Hi-Z.
Note 4. When SSLA0 is at the non-active level or the SPCR.SPE bit is 0, the pin state is Hi-Z.
Note 5. These pins are available for use as I/O port pins.

The RSPI in single-master mode (SPI operation) or multi-master mode (SPI operation) determines MOSI signal values during the SSL negation period (including the SSL retention period during a burst transfer) according to MOIFE and MOIFV bit settings in SPPCR, as listed in Table 29.7.

Table 29.7 MOSI Signal Value Determination during SSL Negation Period

MOIFE Bit	MOIFV Bit	MOSIA Signal Value during SSL Negation Period
0	0, 1	Final data from previous transfer
1	0	Low
1	1	High

29.3.3 RSPI System Configuration Examples

29.3.3.1 Single Master/Single Slave (with This MCU Acting as Master)

Figure 29.5 shows a single-master/single-slave RSPI system configuration example when this MCU is used as a master. In the single-master/single-slave configuration, the SSLA0 to SSLA3 output of this MCU (master) are not used. The SSL input of the SPI slave is fixed to the low level, and the SPI slave is maintained in a select state.*1
This MCU (master) drives the RSPCKA and MOSIA. The SPI slave drives the MISO.

Note 1. In the transfer format corresponding to the case where the SPCMDm.CPHA bit is 0, there are slave devices for which the SSL signal cannot be fixed to the active level. In situations where the SSL signal cannot be fixed, the SSLAi output of this MCU should be connected to the SSL input of the slave device.

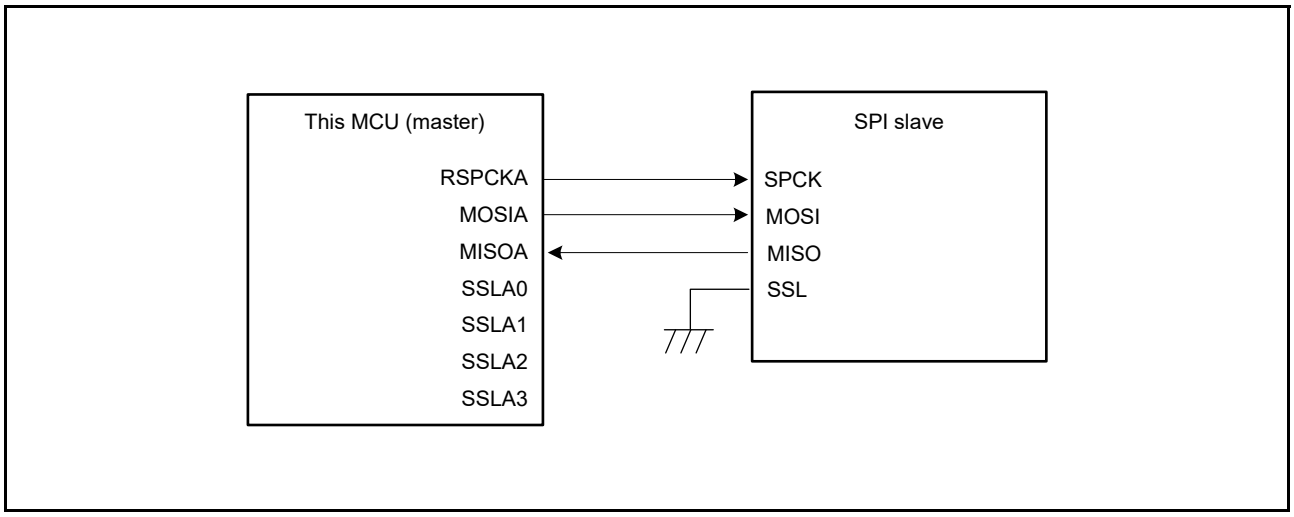


Figure 29.5 Single-Master/Single-Slave Configuration Example (This MCU = Master)

29.3.3.2 Single Master/Single Slave (with This MCU Acting as Slave)

Figure 29.6 shows a single-master/single-slave RSPI system configuration example when this MCU is used as a slave. When this MCU is to operate as a slave, the SSLA0 pin is used as SSL input. The SPI master drives the RSPCK and MOSI. This MCU (slave) drives the MISOA.*1

In the single-slave configuration in which the SPCMDm.CPHA bit is set to 1, the SSLA0 input of this MCU (slave) is fixed to the low level, this MCU (slave) is maintained in a select state, and in this manner it is possible to execute serial transfer (Figure 29.7).

Note 1. When SSLA0 is at the non-active level, the pin state is Hi-Z.

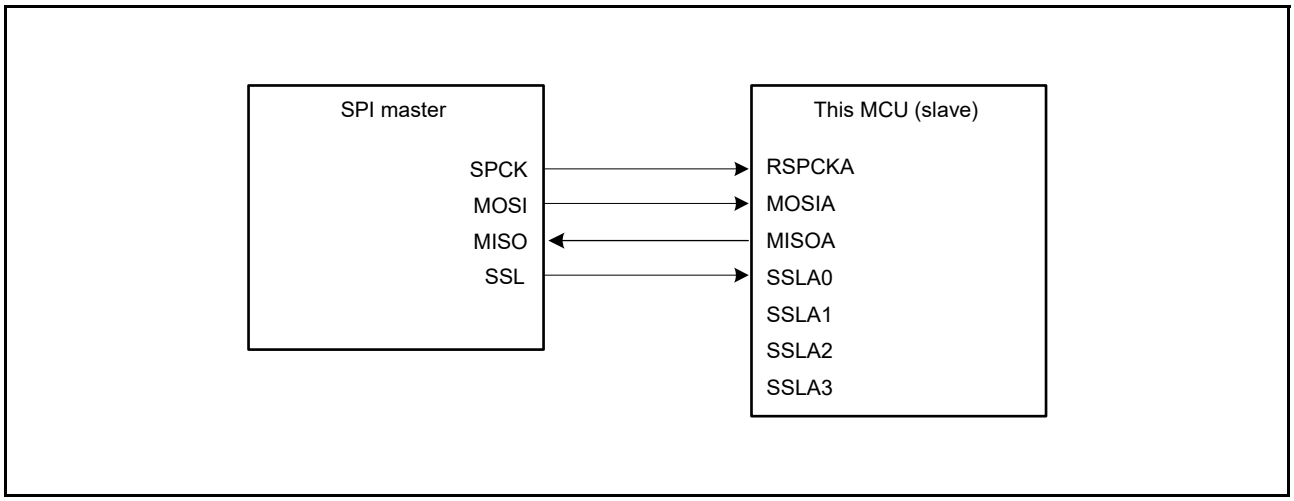


Figure 29.6 Single-Master/Single-Slave Configuration Example (This MCU = Slave, CPHA = 0)

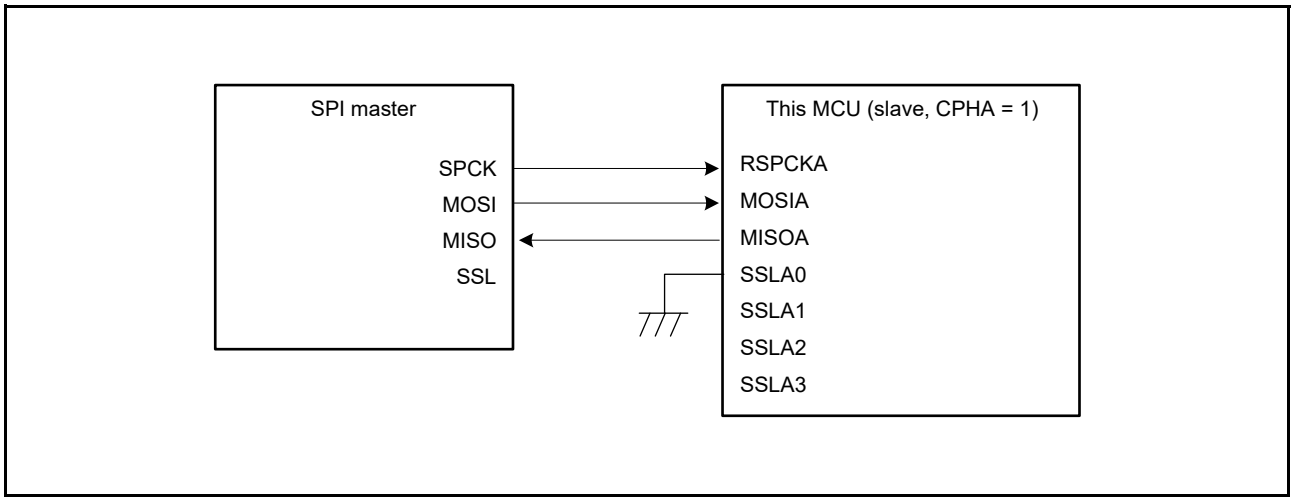


Figure 29.7 Single-Master/Single-Slave Configuration Example (This MCU = Slave, CPHA = 1)

29.3.3.3 Single Master/Multi-Slave (with This MCU Acting as Master)

Figure 29.8 shows a single-master/multi-slave RSPI system configuration example when this MCU is used as a master. In the example of Figure 29.8, the RSPI system is comprised of this MCU (master) and four slaves (SPI slave 0 to SPI slave 3).

The RSPCKA and MOSIA outputs of this MCU (master) are connected to the RSPCK and MOSI inputs of SPI slave 0 to SPI slave 3. The MISO outputs of SPI slave 0 to SPI slave 3 are all connected to the MISOA input of this MCU (master). SSLA0 to SSLA3 outputs of this MCU (master) are connected to the SSL inputs of SPI slave 0 to SPI slave 3, respectively.

This MCU (master) drives RSPCKA, MOSIA, and SSLA0 to SSLA3. Of the SPI slave 0 to SPI slave 3, the slave that receives low-level input into the SSL input drives MISO.

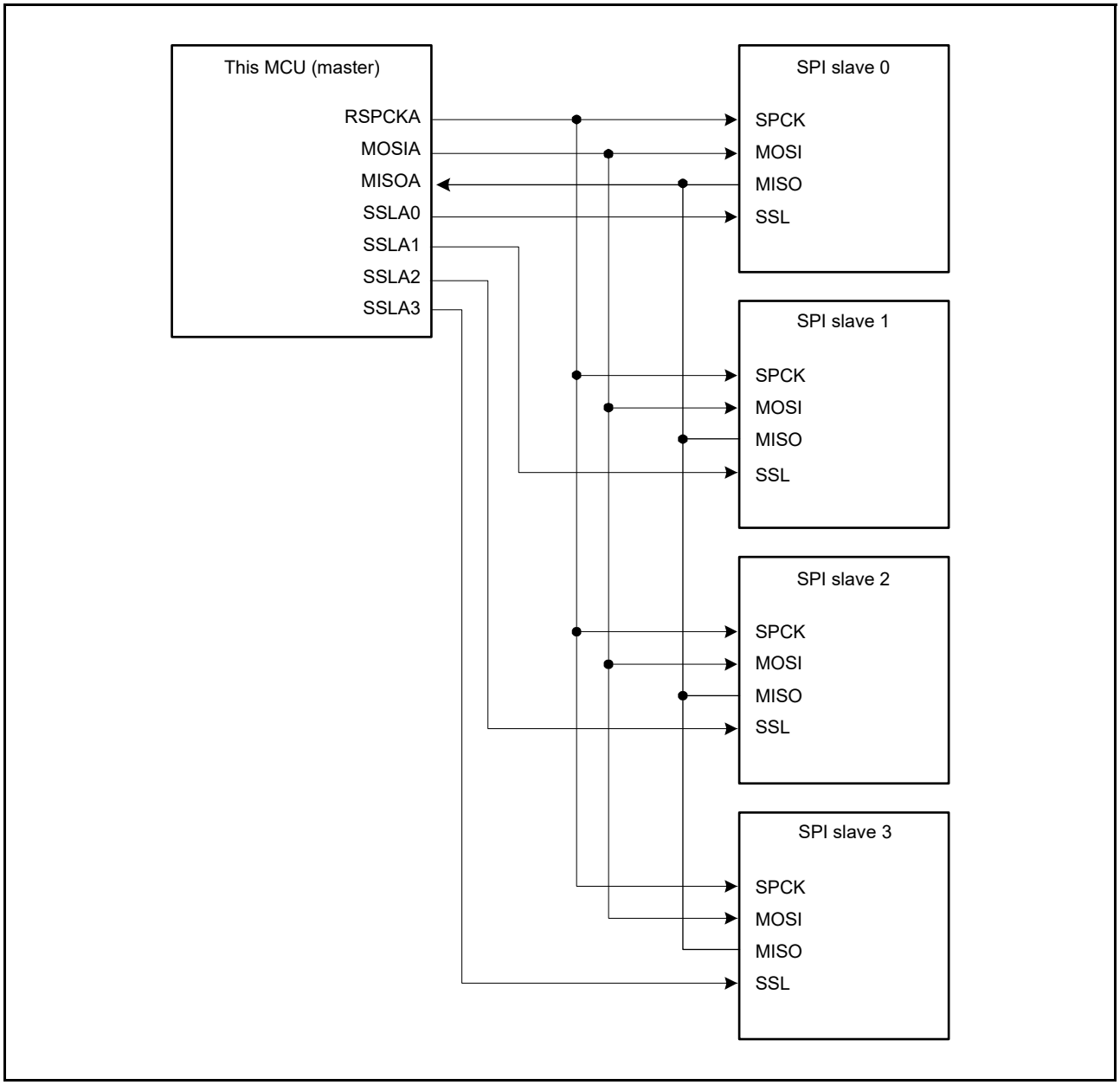


Figure 29.8 Single-Master/Multi-Slave Configuration Example (This MCU = Master)

29.3.3.4 Single Master/Multi-Slave (with This MCU Acting as Slave)

Figure 29.9 shows a single-master/multi-slave RSPI system configuration example when this MCU is used as a slave. In the example of Figure 29.9, the RSPI system is comprised of an SPI master and two MCUs (slave X and slave Y).
The SPCK and MOSI outputs of the SPI master are connected to the RSPCKA and MOSIA inputs of the MCUs (slave X and slave Y). The MISOA outputs of the MCUs (slave X and slave Y) are all connected to the MISO input of the SPI master. SSLX and SSLY outputs of the SPI master are connected to the SSLA0 inputs of the MCUs (slave X and slave Y), respectively.
The SPI master drives SPCK, MOSI, SSLX, and SSLY. Of the MCUs (slave X and slave Y), the slave that receives low-level input into the SSLA0 input drives MISOA.

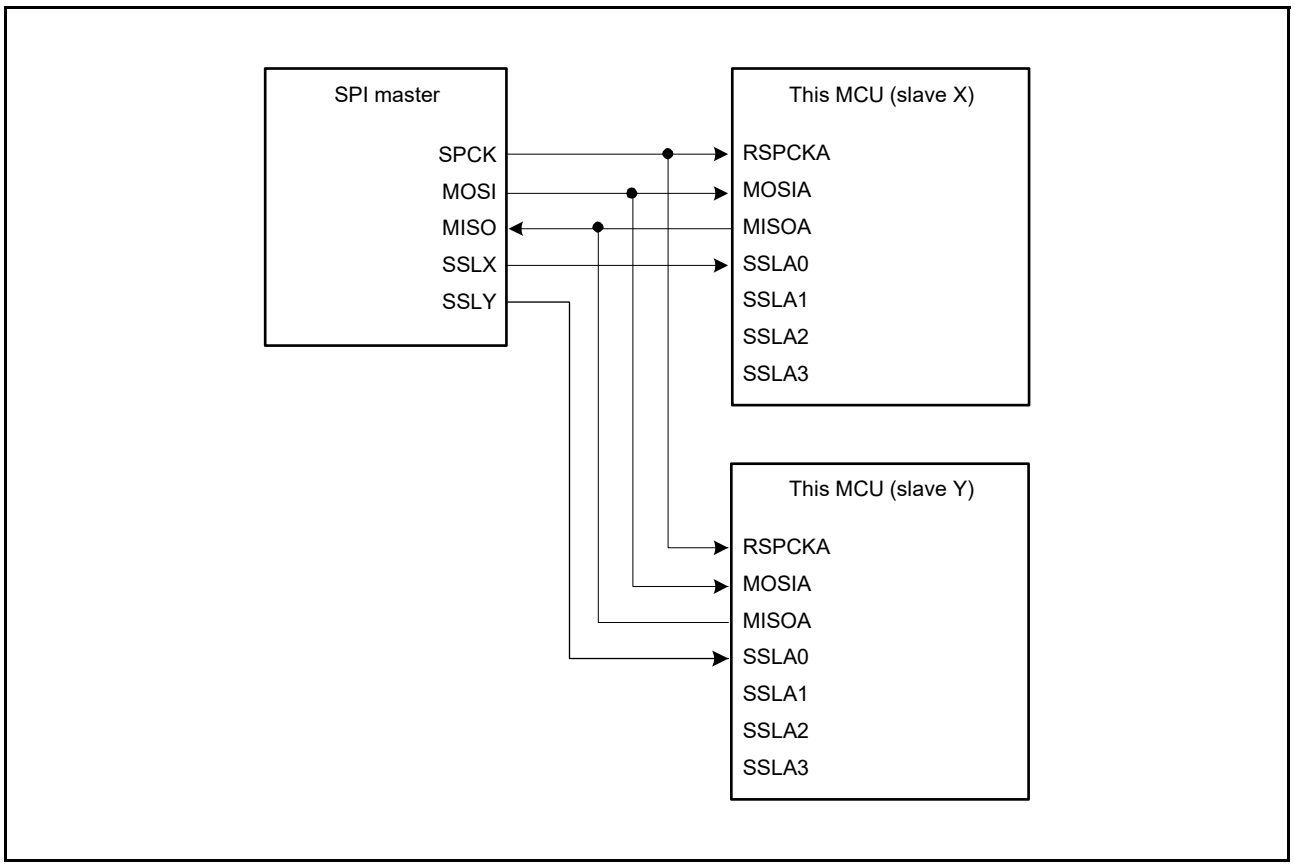


Figure 29.9 Single-Master/Multi-Slave Configuration Example (This MCU = Slave)

29.3.3.5 Multi-Master/Multi-Slave (with This MCU Acting as Master)

Figure 29.10 shows a multi-master/multi-slave RSPI system configuration example when this MCU is used as a master. In the example of Figure 29.10, the RSPI system is comprised of two MCUs (master X and master Y) and two SPI slaves (SPI slave 1 and SPI slave 2).

The RSPCKA and MOSIA outputs of the MCUs (master X and master Y) are connected to the RSPCK and MOSI inputs of SPI slaves 1 and 2. The MISO outputs of SPI slaves 1 and 2 are connected to the MISOA inputs of the MCUs (master X and master Y). Any generic port Y output from this MCU (master X) is connected to the SSLA0 input of this MCU (master Y). Any generic port X output of this MCU (master Y) is connected to the SSLA0 input of this MCU (master X). The SSLA1 and SSLA2 outputs of the MCUs (master X and master Y) are connected to the SSL inputs of the SPI slaves 1 and 2. In this configuration example, since the system can be comprised solely of SSLA0 input, and SSLA1 and SSLA2 outputs for slave connections, the SSLA3 output of this MCU is not required.

This MCU drives RSPCKA, MOSIA, SSLA1, and SSLA2 when the SSLA0 input level is high. When the SSLA0 input level is low, this MCU detects a mode fault error, sets RSPCKA, MOSIA, SSLA1, and SSLA2 to Hi-Z, and releases the RSPI bus right to the other master. Of the SPI slaves 1 and 2, the slave that receives low-level input into the SSL input drives MISO.

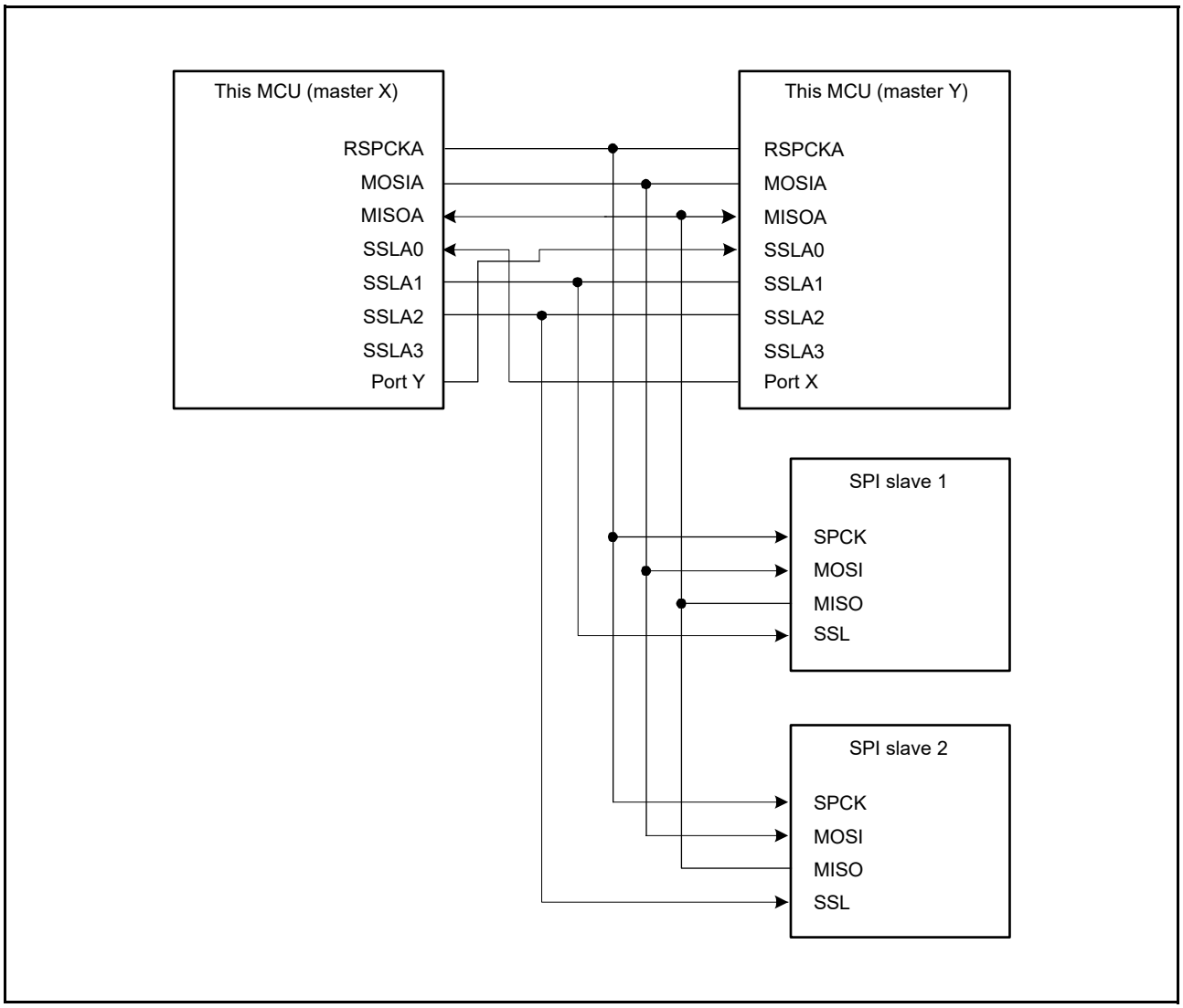


Figure 29.10 Multi-Master/Multi-Slave Configuration Example (This MCU = Master)

29.3.3.6 Master (Clock Synchronous Operation)/Slave (Clock Synchronous Operation) (with This MCU Acting as Master)

Figure 29.11 shows a master (clock synchronous operation)/slave (clock synchronous operation) RSPI system configuration example when this MCU is used as a master. In the master (clock synchronous operation)/slave (clock synchronous operation) configuration, SSLA0 to SSLA3 of this MCU (master) are not used.
This MCU (master) drives the RSPCKA and MOSIA. The SPI slave drives the MISO.

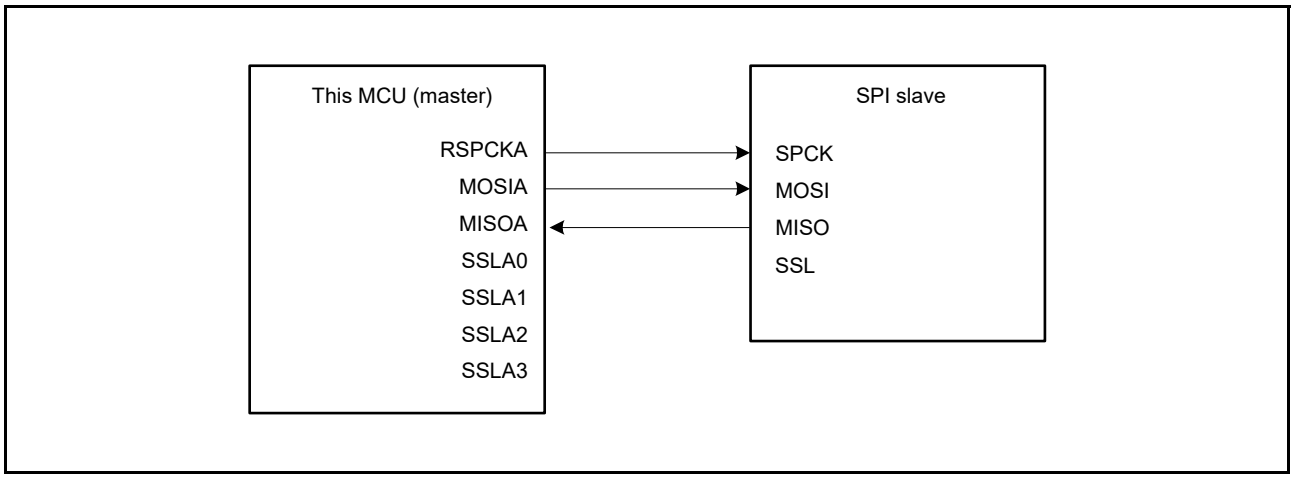


Figure 29.11 Master (Clock Synchronous Operation)/Slave (Clock Synchronous Operation) Configuration Example (This MCU = Master)

29.3.3.7 Master (Clock Synchronous Operation)/Slave (Clock Synchronous Operation) (with This MCU Acting as Slave)

Figure 29.12 shows a master (clock synchronous operation)/slave (clock synchronous operation) RSPI system configuration example when this MCU is used as a slave. When this MCU is to operate as a slave (clock synchronous operation), this MCU (slave) drives the MISOA and the SPI master drives the SPCK and MOSI. In addition, SSLA0 to SSLA3 of this MCU (slave) are not used.
Only in the single-slave configuration in which the SPCMDm.CPHA bit is set to 1, this MCU (slave) can execute serial transfer.

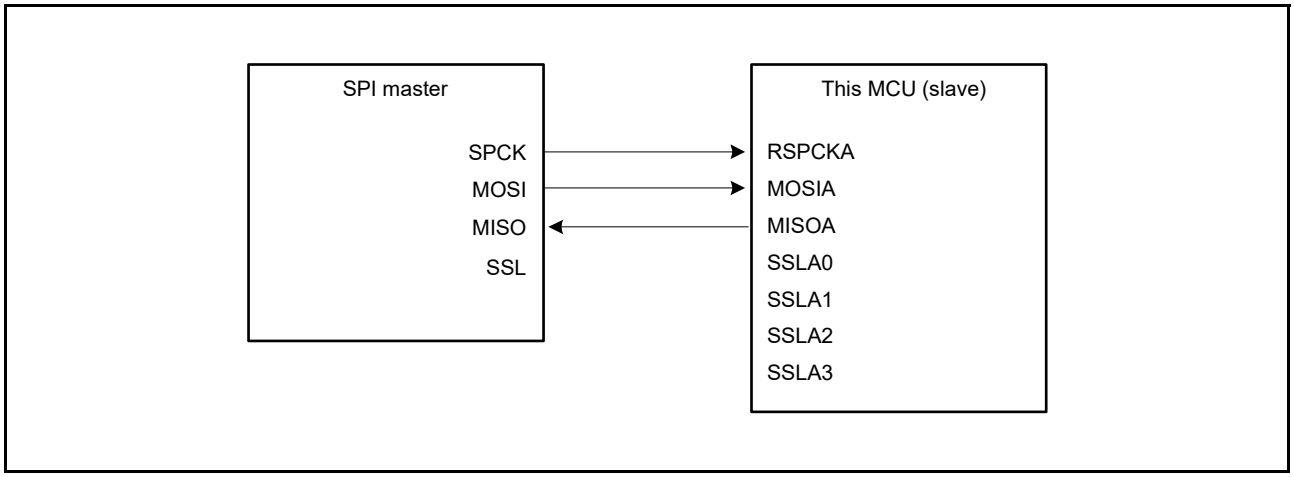


Figure 29.12 Master (Clock Synchronous Operation)/Slave (Clock Synchronous Operation) Configuration Example (This MCU = Slave, CPHA = 1)

29.3.4 Data Format

The RSPI's data format depends on the settings in RSPI command register m (SPCMDm) (m = 0 to 7) and the parity enable bit in RSPI control register 2 (SPCR2.SPPE). Regardless of whether the MSB or LSB is first, the RSPI treats the range from the LSB bit in the RSPI data register (SPDR) to the selected data length as transfer data.
The format of one frame of data before or after transfer is shown below.

(a) With Parity Disabled

When parity is disabled, transmission or reception of data proceeds with the length in bits selected in the RSPI data length setting bits in RSPI command register m (SPCMDm.SPB[3:0]).

(b) With Parity Enabled

When parity is enabled, transmission or reception of data proceeds with the length in bits selected in the RSPI data length setting bits in RSPI command register m (SPCMDm.SPB[3:0]). In this case, however, the last bit is a parity bit.

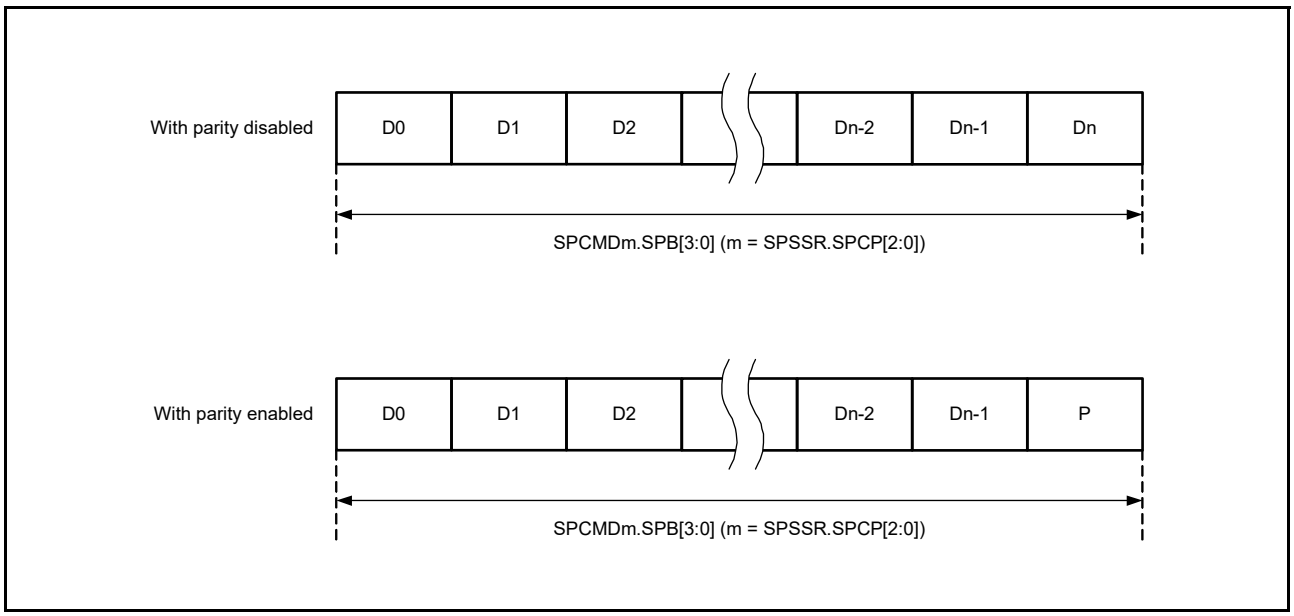


Figure 29.13 Outline of the Data Format (with Parity Disabled/Enabled)

29.3.4.1 When Parity is Disabled (SPCR2.SPPE = 0)

When parity is disabled, data for transmission are copied to the shift register with no prior processing. A description of the connection between the RSPI data register (SPDR) and the shift register in terms of the combination of MSB or LSB first and data length is given below.

(1) MSB First Transfer (32-Bit Data)

Figure 29.14 shows details of operations by the RSPI data register (SPDR) and the shift register in transfer with parity disabled, an RSPI data length of 32 bits, and MSB first selected.
In transmission, bits T31 to T00 from the current stage of the transmit buffer are copied to the shift register. Data for transmission are shifted out from the shift register in order from T31, through T30, and so on to T00.
In reception, received data are shifted in bit by bit through bit 0 of the shift register. When bits R31 to R00 have been collected after input of the required number of cycles of RSPCK, the value in the shift register is copied to the receive buffer.

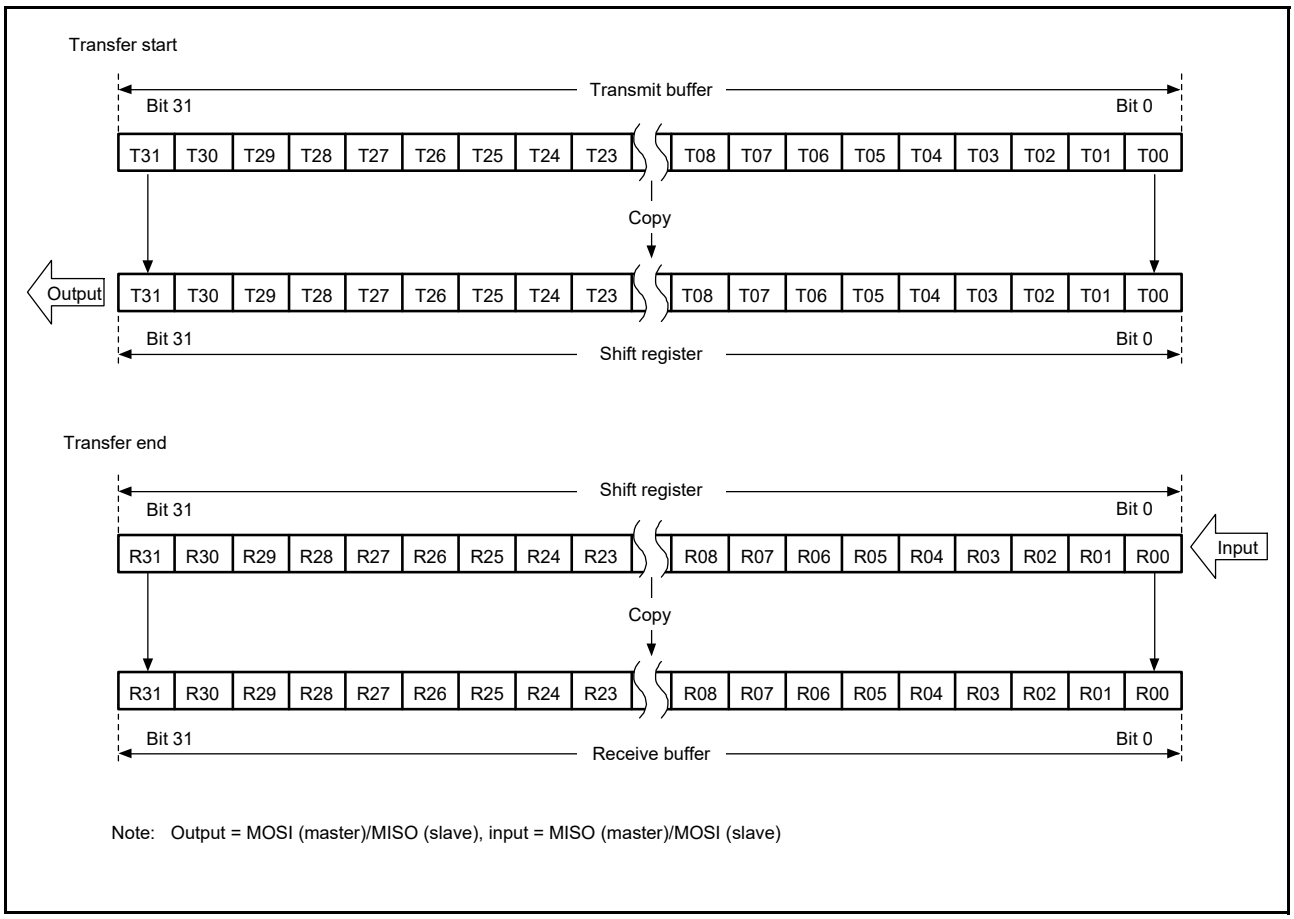


Figure 29.14 MSB First Transfer (32-Bit Data, Parity Disabled)

(2) MSB First Transfer (24-Bit Data)

Figure 29.15 shows details of operations by the RSPI data register (SPDR) and the shift register in transfer with parity disabled, 24 bits as the RSPI data length for an example that is not 32 bits, and MSB first selected.

In transmission, the lower-order 24 bits (T23 to T00) from the current stage of the transmit buffer are copied to the shift register. Data for transmission are shifted out from the shift register in order from T23, through T22, and so on to T00.

In reception, received data are shifted in bit by bit through bit 0 of the shift register. When bits R23 to R00 have been collected after input of the required number of cycles of RSPCK, the value in the shift register is copied to the receive buffer. At this time, the higher-order 8 bits of the transmit buffer are stored in the higher-order 8 bits of the receive buffer.

Writing 0 to bits T31 to T24 at the time of transmission leads to 0 being inserted in the higher-order 8 bits of the receive buffer.

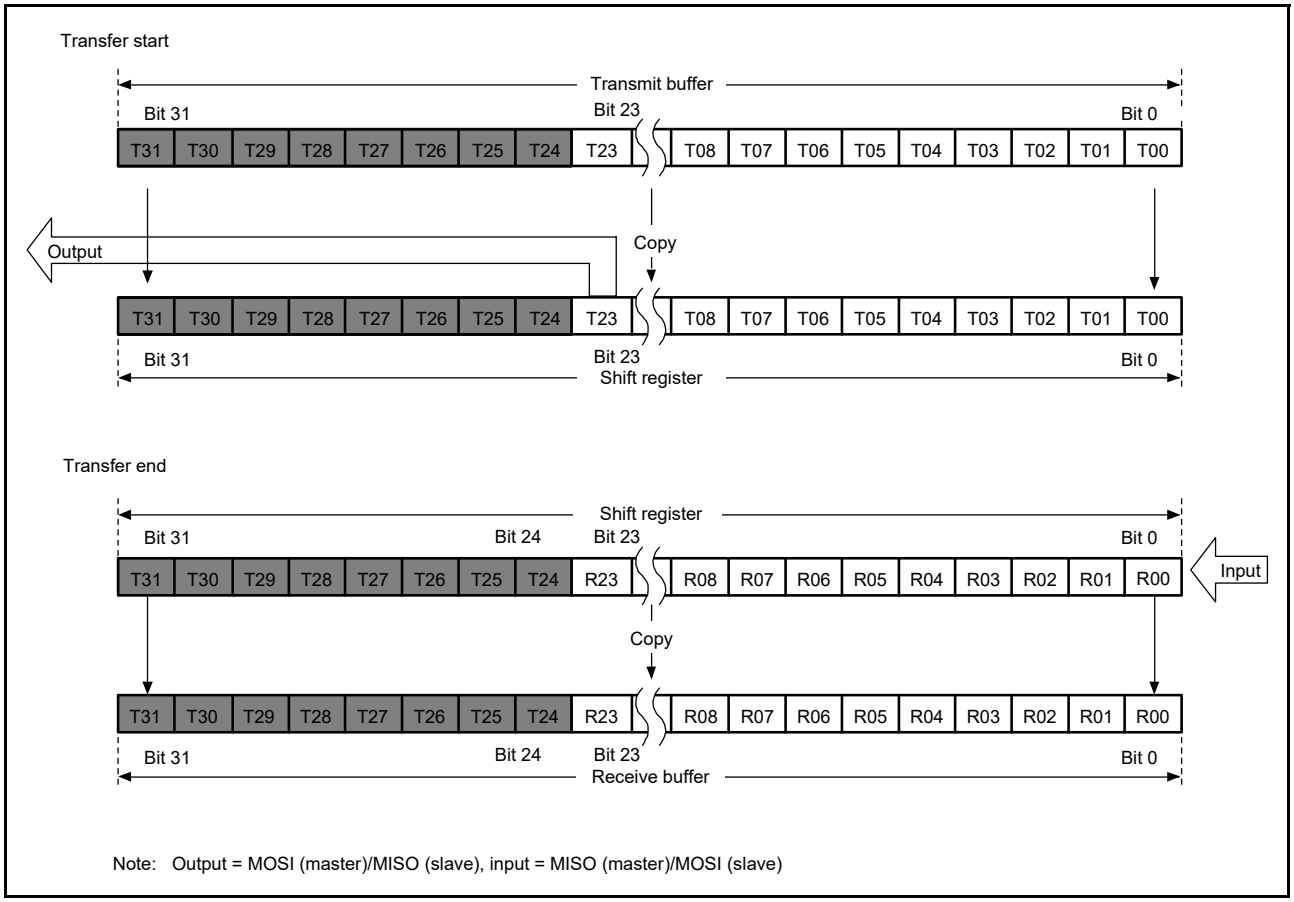


Figure 29.15 MSB First Transfer (24-Bit Data, Parity Disabled)

(3) LSB First Transfer (32-Bit Data)

Figure 29.16 shows details of operations by the RSPI data register (SPDR) and the shift register in transfer with parity disabled, an RSPI data length of 32 bits, and LSB first selected.

In transmission, bits T31 to T00 from the current stage of the transmit buffer are reordered bit by bit to obtain the order T00 to T31 for copying to the shift register. Data for transmission are shifted out from the shift register in order from T00, through T01, and so on to T31.

In reception, received data are shifted in bit by bit through bit 0 of the shift register. When bits R00 to R31 have been collected after input of the required number of cycles of RSPCK, the value in the shift register is copied to the receive buffer.

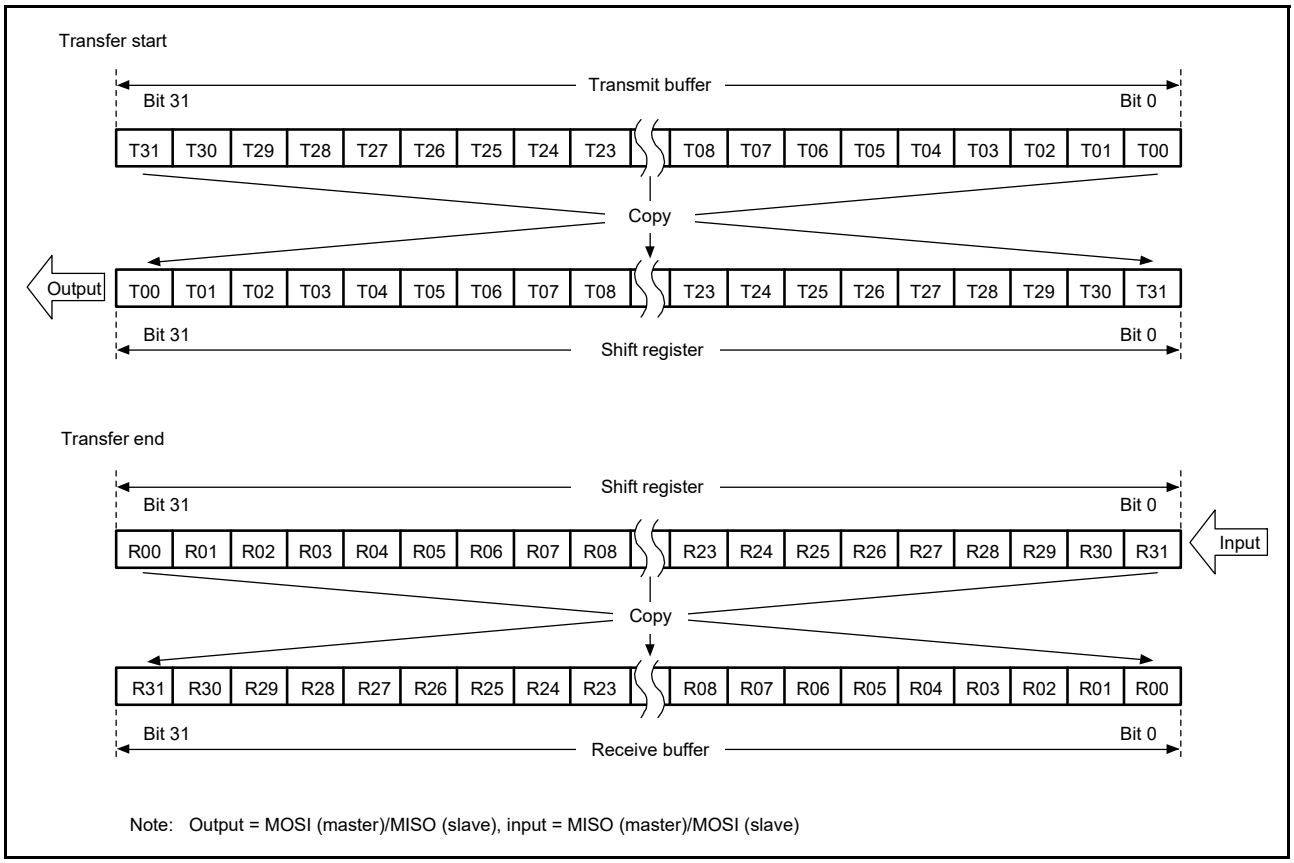


Figure 29.16 LSB First Transfer (32-Bit Data, Parity Disabled)

(4) LSB First Transfer (24-Bit Data)

Figure 29.17 shows details of operations by the RSPI data register (SPDR) and the shift register in transfer with parity disabled, 24 bits as the RSPI data length for an example that is not 32 bits, and LSB first selected.

In transmission, the lower-order 24 bits (T23 to T00) from the current stage of the transmit buffer are reordered bit by bit to obtain the order T00 to T23 for copying to the shift register. Data for transmission are shifted out from the shift register in order from T00, through T01, and so on to T23.

In reception, received data are shifted in bit by bit through bit 8 of the shift register. When bits R00 to R23 have been collected after input of the required number of cycles of RSPCK, the value in the shift register is copied to the receive buffer.

At this time, the higher-order 8 bits of the transmit buffer are stored in the higher-order 8 bits of the receive buffer.

Writing 0 to bits T31 to T24 at the time of transmission leads to 0 being inserted in the higher-order 8 bits of the receive buffer.

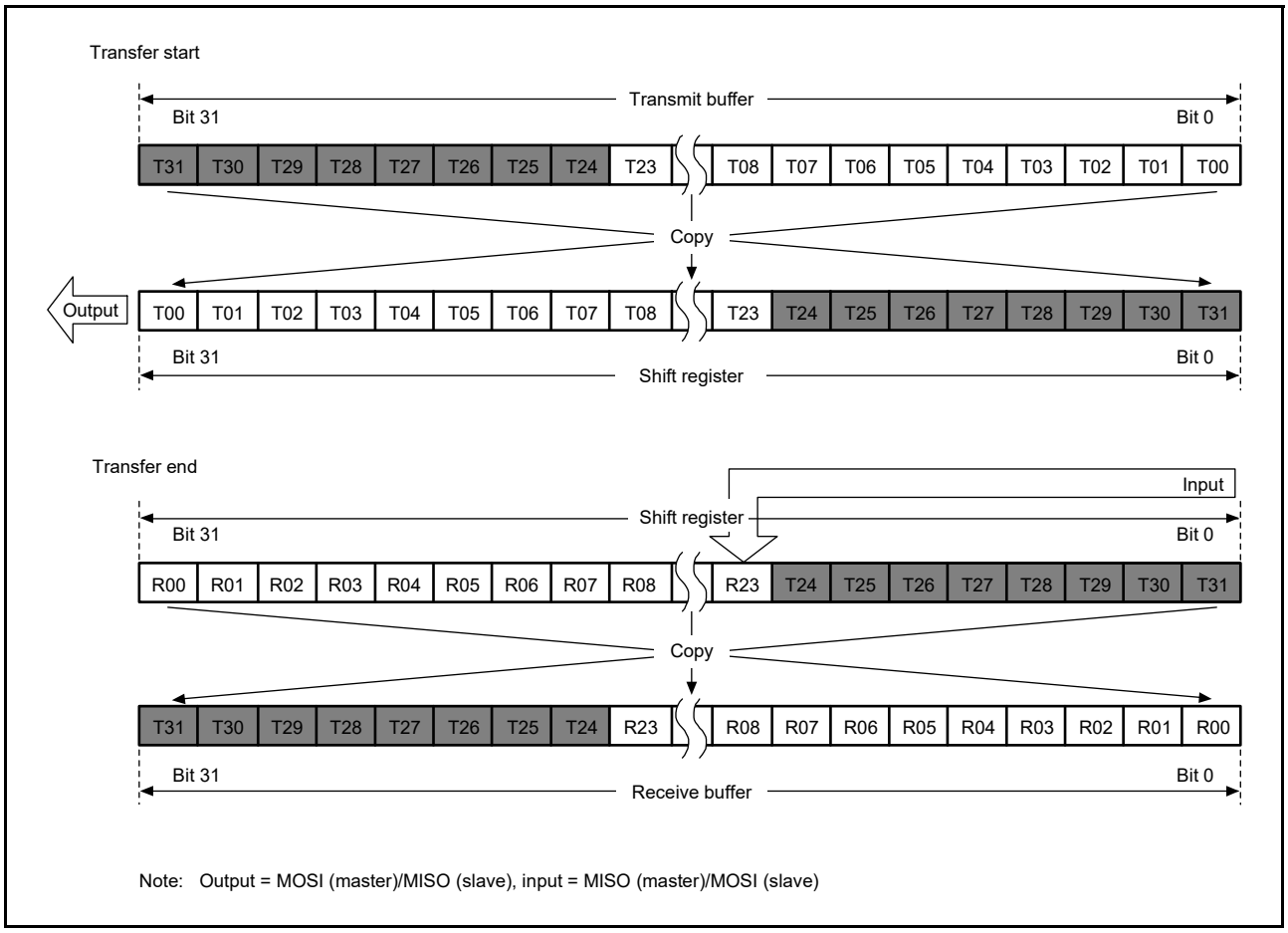


Figure 29.17 LSB First Transfer (24-Bit Data, Parity Disabled)

29.3.4.2 When Parity is Enabled (SPCR2.SPPE = 1)

When parity is enabled, the lowest-order bit of the data for transmission becomes a parity bit. Hardware calculates the value of the parity bit.

(1) MSB First Transfer (32-Bit Data)

Figure 29.18 shows details of operations by the RSPI data register (SPDR) and the shift register in transfer with parity enabled, an RSPI data length of 32 bits, and MSB first selected.

In transmission, the value of the parity bit (P) is calculated from bits T31 to T01. This replaces the final bit, T00, and the whole is copied to the shift register. Data are transmitted in the order T31, T30, …, T01, and P.

In reception, received data are shifted in bit by bit through bit 0 of the shift register. When bits R31 to P have been collected after input of the required number of cycles of RSPCK, the value in the shift register is copied to the receive buffer. On copying of data to the shift register, the data from R31 to P are checked by judging the parity.

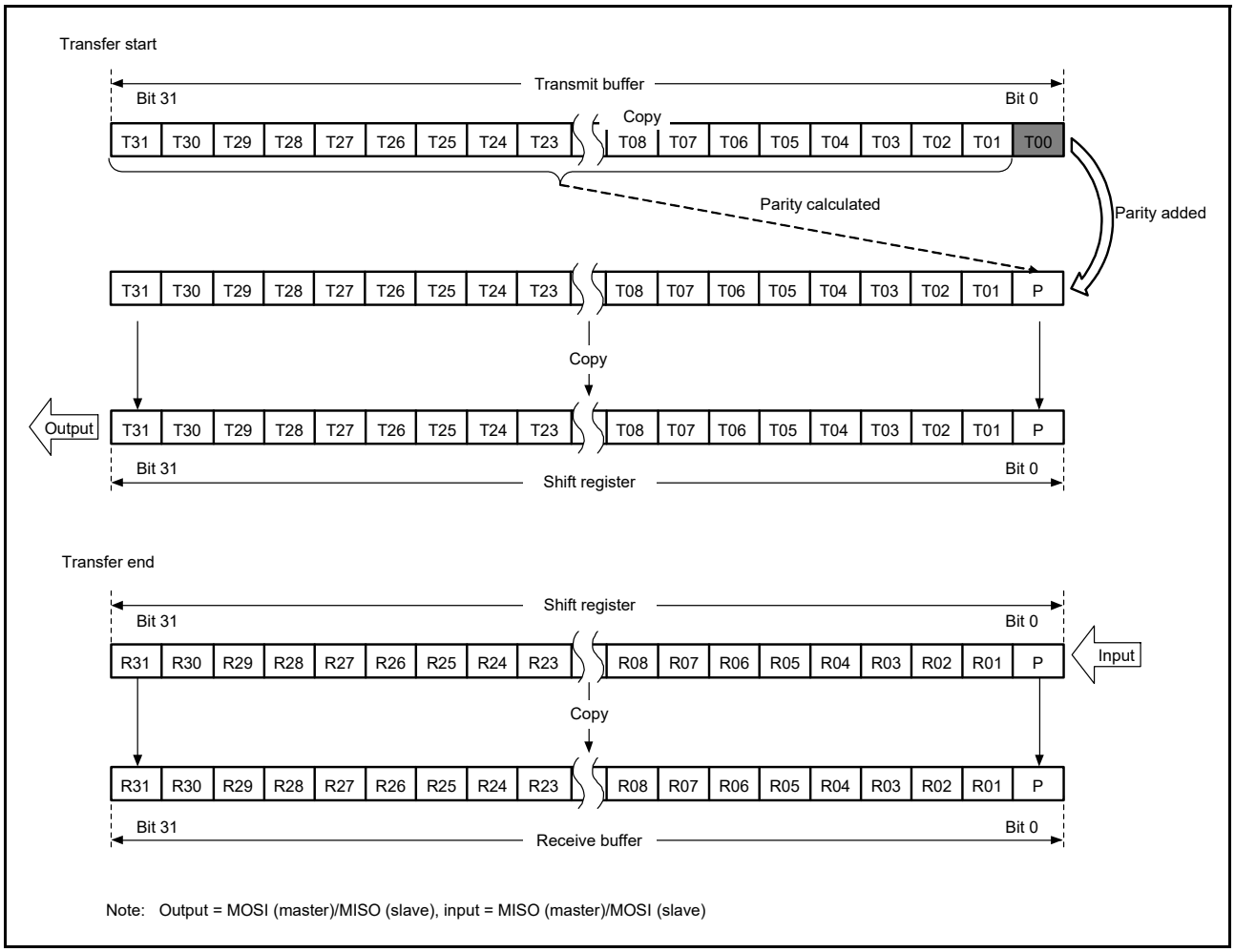


Figure 29.18 MSB First Transfer (32-Bit Data, Parity Enabled)

(2) MSB First Transfer (24-Bit Data)

Figure 29.19 shows details of operations by the RSPI data register (SPDR) and the shift register in transfer with parity enabled, 24 bits as the RSPI data length for an example that is not 32 bits, and MSB first selected.
In transmission, the value of the parity bit (P) is calculated from bits T23 to T01. This replaces the final bit, T00, and the whole is copied to the shift register. Data are transmitted in the order T23, T22, …, T01, and P.
In reception, received data are shifted in bit by bit through bit 0 of the shift register. When bits R23 to P have been collected after input of the required number of cycles of RSPCK, the value in the shift register is copied to the receive buffer. On copying of data to the shift register, the data from R23 to P are checked by judging the parity. At this time, the higher-order 8 bits of the transmit buffer are stored in the higher-order 8 bits of the receive buffer. Writing 0 to bits T31 to T24 at the time of transmission leads to 0 being inserted in the higher-order 8 bits of the receive buffer.

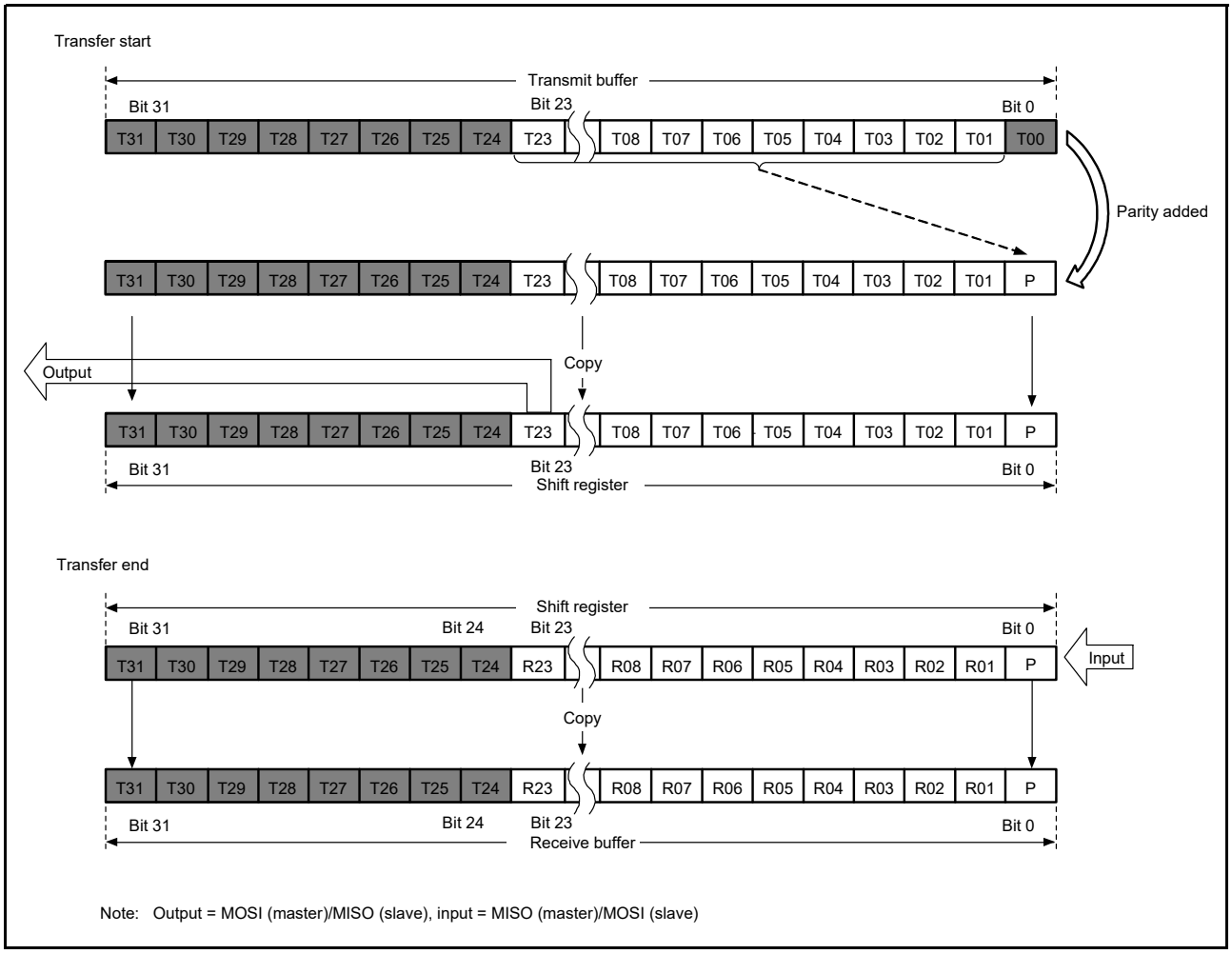


Figure 29.19 MSB First Transfer (24-Bit Data, Parity Enabled)

(3) LSB First Transfer (32-Bit Data)

Figure 29.20 shows details of operations by the RSPI data register (SPDR) and the shift register in transfer with parity enabled, an RSPI data length of 32 bits, and LSB first selected.

In transmission, the value of the parity bit (P) is calculated from bits T30 to T00. This replaces the final bit, T31, and the whole is copied to the shift register. Data are transmitted in the order T00, T01, …, T30, and P.

In reception, received data are shifted in bit by bit through bit 0 of the shift register. When bits R00 to P have been collected after input of the required number of cycles of RSPCK, the value in the shift register is copied to the receive buffer. On copying of data to the shift register, the data from R00 to P are checked by judging the parity.

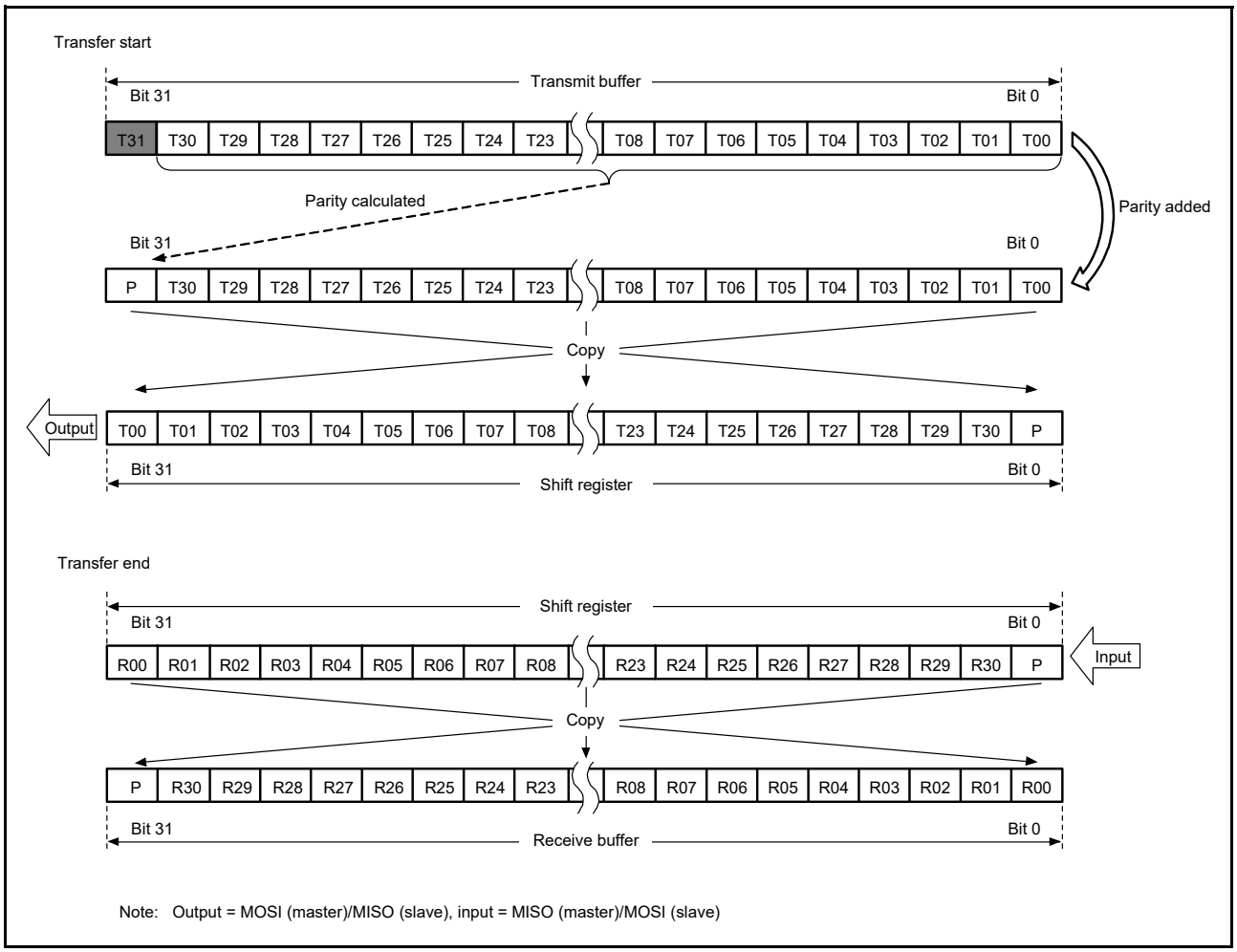


Figure 29.20 LSB First Transfer (32-Bit Data, Parity Enabled)

(4) LSB First Transfer (24-Bit Data)

Figure 29.21 shows details of operations by the RSPI data register (SPDR) and the shift register in transfer with parity enabled, 24 bits as the RSPI data length for an example that is not 32 bits, and LSB first selected.
In transmission, the value of the parity bit (P) is calculated from bits T22 to T00. This replaces the final bit, T23, and the whole is copied to the shift register. Data are transmitted in the order T00, T01, …, T22, and P.
In reception, received data are shifted in bit by bit through bit 8 of the shift register. When bits R00 to P have been collected after input of the required number of cycles of RSPCK, the value in the shift register is copied to the receive buffer. On copying of data to the shift register, the data from R00 to P are checked by judging the parity. At this time, the higher-order 8 bits of the transmit buffer are stored in the higher-order 8 bits of the receive buffer. Writing 0 to bits T31 to T24 at the time of transmission leads to 0 being inserted in the higher-order 8 bits of the receive buffer.

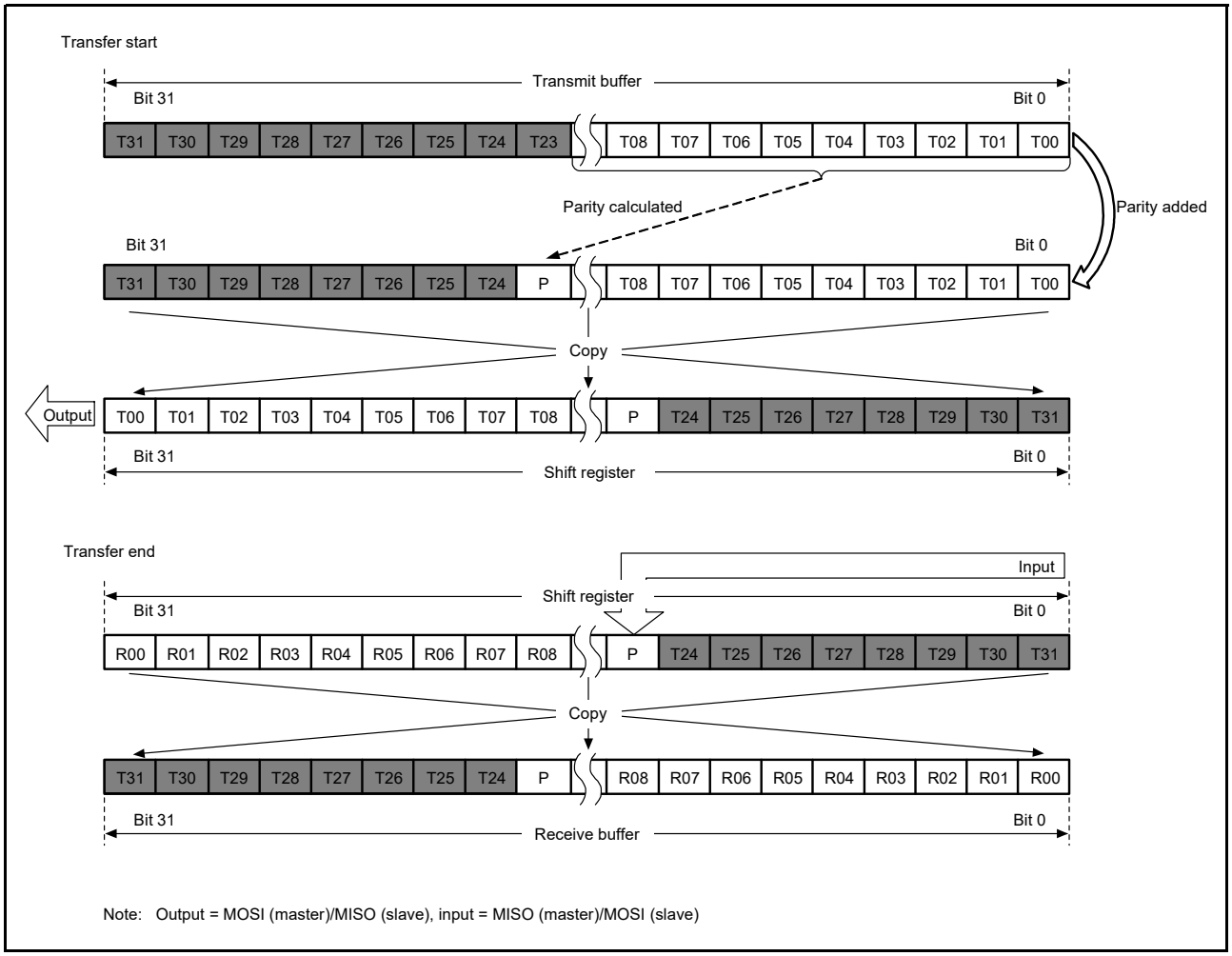


Figure 29.21 LSB First Transfer (24-Bit Data, Parity Enabled)

29.3.5 Transfer Format

29.3.5.1 CPHA = 0

Figure 29.22 shows a sample transfer format for the serial transfer of 8-bit data when the SPCMDm.CPHA bit is 0. Note that clock synchronous operation (the SPCR.SPMS bit is 1) should not performed when the RSPI operates in slave mode (SPCR.MSTR = 0) and the CPHA bit is 0. In Figure 29.22, RSPCKA (CPOL = 0) indicates the RSPCKA signal waveform when the SPCMDm.CPOL bit is 0; RSPCKA (CPOL = 1) indicates the RSPCKA signal waveform when the CPOL bit is 1. The sampling timing represents the timing at which the RSPI fetches serial transfer data into the shift register. The I/O directions of the signals depend on the RSPI settings. For details, refer to section 29.3.2, Controlling RSPI Pins.

When the SPCMDm.CPHA bit is 0, the driving of valid data to the MOSIA and MISOA signals commences at an SSLAi signal assertion timing. The first RSPCKA signal change timing that occurs after the SSLAi signal assertion becomes the first transfer data fetch timing. After this timing, data is sampled at every 1 RSPCK cycle. The change timing for MOSIA and MISOA signals is 1/2 RSPCK cycles after the transfer data fetch timing. The CPOL bit setting does not affect the RSPCKA signal operation timing; it only affects the signal polarity.

t1 denotes a period from an SSLAi signal assertion to RSPCKA oscillation (RSPCK delay). t2 denotes a period from the termination of RSPCKA oscillation to an SSLAi signal negation (SSL negation delay). t3 denotes a period in which SSLAi signal assertion is suppressed for the next transfer after the end of serial transfer (next-access delay). t1, t2, and t3 are controlled by a master device running on the RSPI system. For a description of t1, t2, and t3 when the RSPI of this MCU is in master mode, refer to section 29.3.10.1, Master Mode Operation.

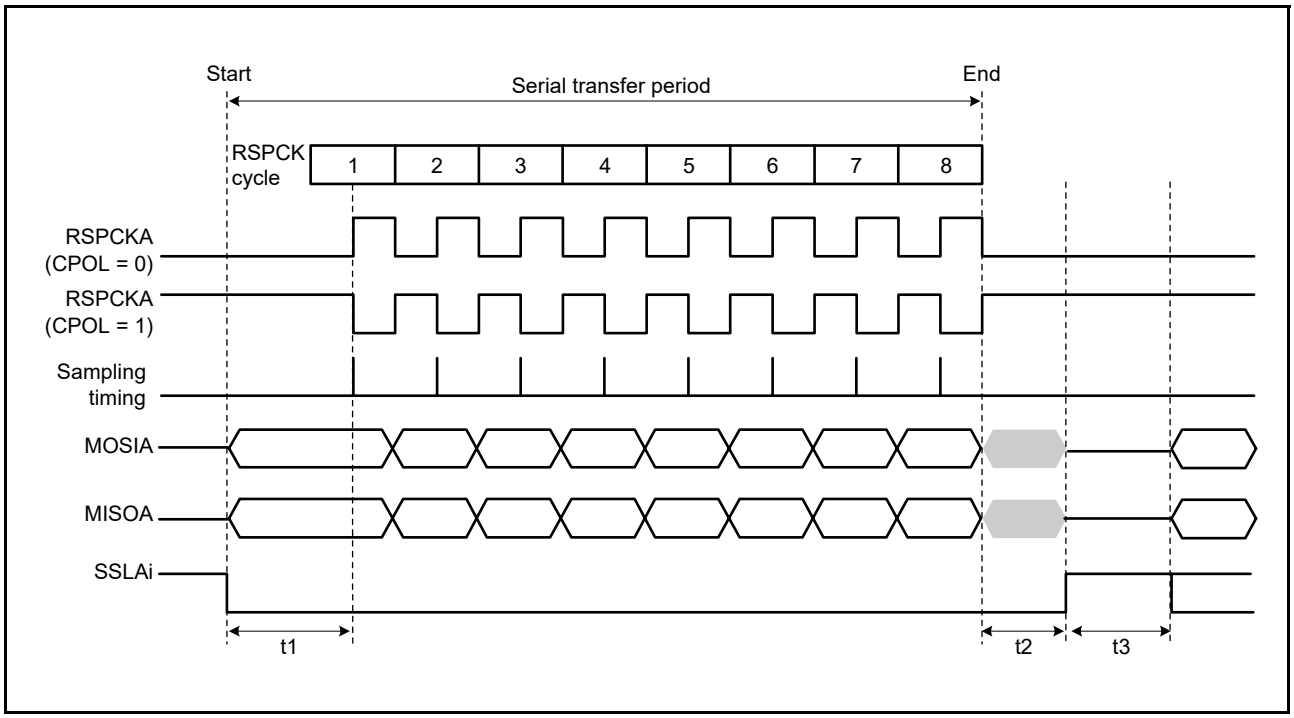


Figure 29.22 RSPI Transfer Format (CPHA = 0)

29.3.5.2 CPHA = 1

Figure 29.23 shows a sample transfer format for the serial transfer of 8-bit data when the SPCMDm.CPHA bit is 1. However, when the SPCR.SPMS bit is 1, the SSLAi signals are not used, and only the three signals RSPCKA, MOSIA, and MISOA handle communications. In Figure 29.23, RSPCK (CPOL = 0) indicates the RSPCKA signal waveform when the SPCMDm.CPOL bit is 0; RSPCKA (CPOL = 1) indicates the RSPCKA signal waveform when the CPOL bit is 1. The sampling timing represents the timing at which the RSPI fetches serial transfer data into the shift register. The I/O directions of the signals depend on the RSPI mode (master or slave). For details, refer to section 29.3.2, Controlling RSPI Pins.

When the SPCMDm.CPHA bit is 1, the driving of invalid data to the MISOA signal commences at an SSLAi signal assertion timing. The output of valid data to the MOSIA and MISOA signals commences at the first RSPCKA signal change timing that occurs after the SSLAi signal assertion. After this timing, data is updated at every 1 RSPCK cycle. The transfer data fetch timing is 1/2 RSPCK cycles after the data update timing. The SPCMDm.CPOL bit setting does not affect the RSPCKA signal operation timing; it only affects the signal polarity.

t1, t2, and t3 are the same as those in the case of CPHA = 0. For a description of t1, t2, and t3 when the RSPI of this MCU is in master mode, refer to section 29.3.10.1, Master Mode Operation.

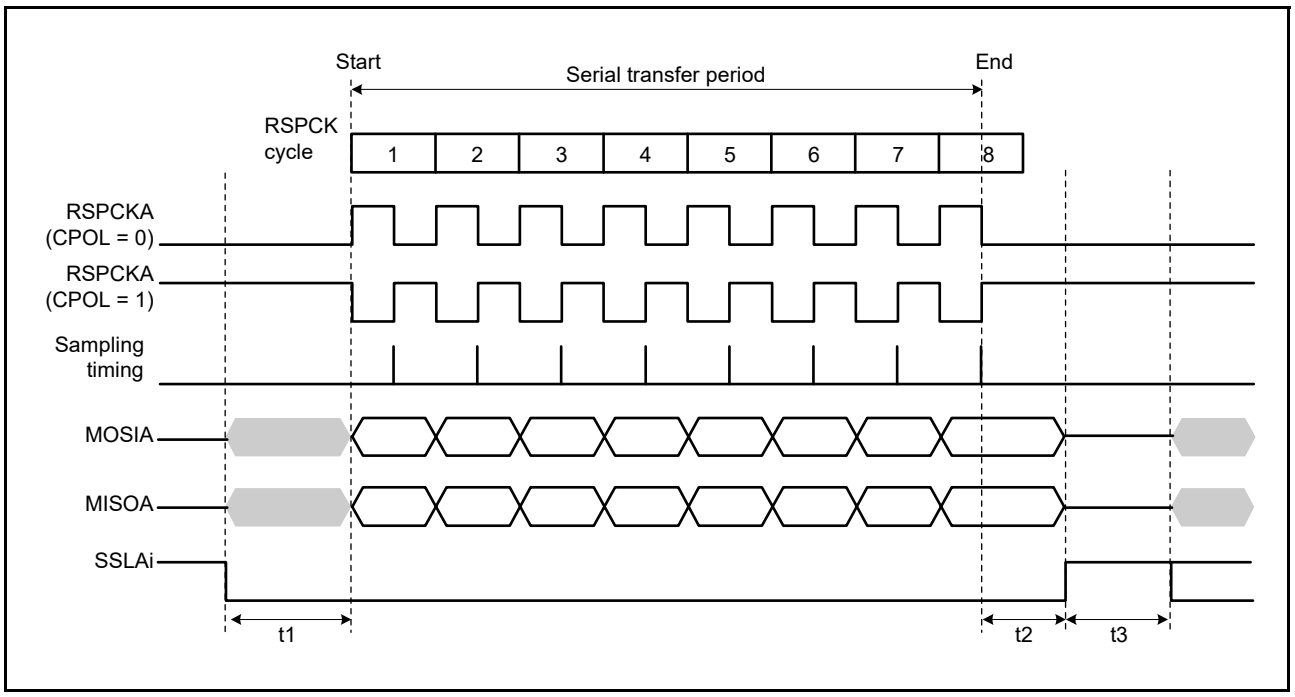


Figure 29.23 RSPI Transfer Format (CPHA = 1)

29.3.6 Communications Operating Mode

Full-duplex synchronous serial communications or transmit operations only can be selected by the communications operating mode select bit (SPCR.TXMD). The SPDR access shown in Figure 29.24 and Figure 29.25 indicate the condition of access to the SPDR register, where W denotes a write cycle.

29.3.6.1 Full-Duplex Synchronous Serial Communications (SPCR.TXMD = 0)

Figure 29.24 shows an example of operation when the communications operating mode select bit (SPCR.TXMD) is set to 0. In the example in Figure 29.24, the RSPI performs an 8-bit serial transfer in which the SPDCR.SPFC[1:0] bits are 00b, the SPCMDm.CPHA bit is 1, and the SPCMDm.CPOL bit is 0. The numbers given under the RSPCKA waveform represent the number of RSPCK cycles (i.e., the number of transferred bits).

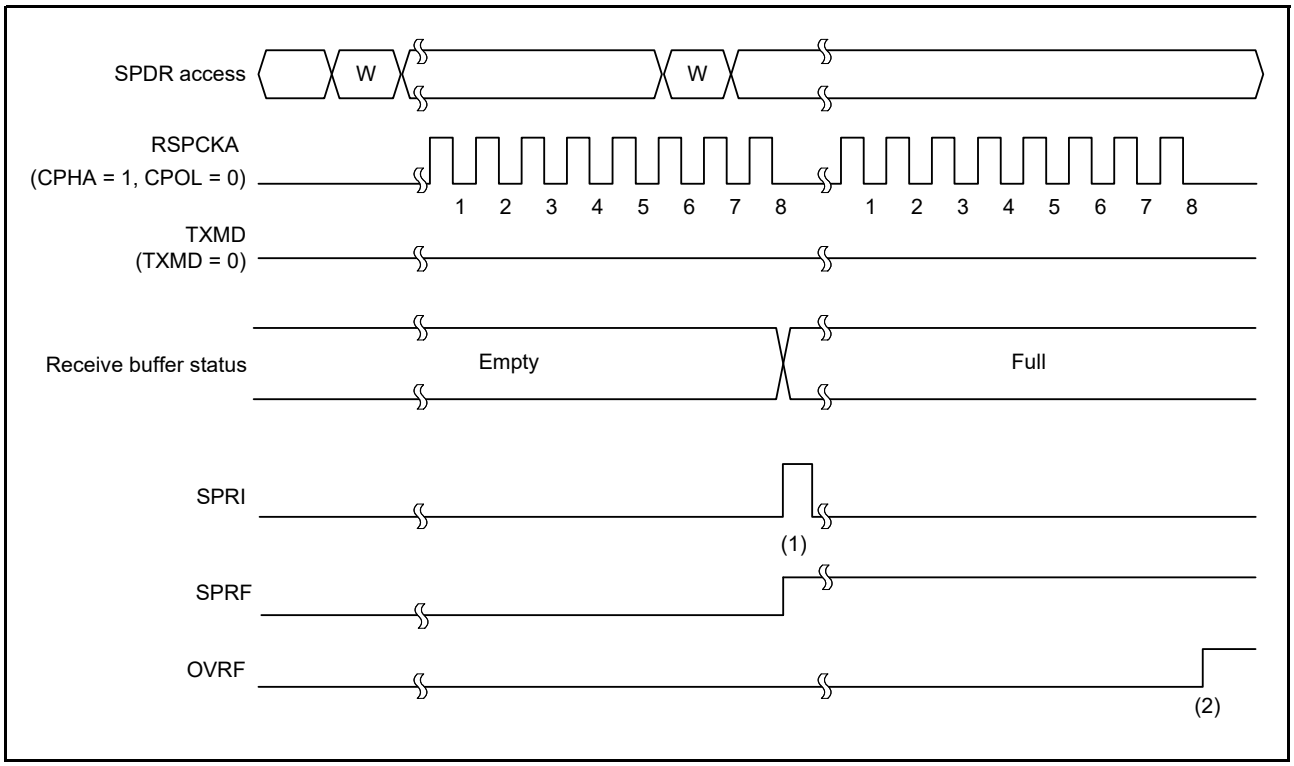


Figure 29.24 Operation Example of SPCR.TXMD = 0

The operation of the flags at timings shown in steps (1) and (2) in the figure is described below.

(1) When a serial transfer ends with the receive buffer of SPDR empty, the RSPI generates a receive buffer full interrupt request (SPRI) (sets the SPSR.SPRF flag to 1) and copies the received data in the shift register to the receive buffer.

(2) When a serial transfer ends with the receive buffer of SPDR holding data that was received in the previous serial transfer, the RSPI sets the SPSR.OVRF flag to 1 and discards the received data in the shift register.

When full-duplex synchronous serial communications (SPCR.TXMD = 0) is selected, reception occurs simultaneously with transmit operations. As such, the SPRF and OVRF flags in the SPSR register become 1 at the timing described in (1) and (2), respectively, according to the state of the receive buffer.

29.3.6.2 Transmit Operations Only (SPCR.TXMD = 1)

Figure 29.25 shows an example of operation when the communications operating mode select bit (SPCR.TXMD) is set to 1. In the example in Figure 29.25, the RSPI performs an 8-bit serial transfer in which the SPDCR.SPFC[1:0] bits are 00b, the SPCMDm.CPHA bit is 1, and the SPCMDm.CPOL bit is 0. The numbers given under the RSPCKA waveform represent the number of RSPCK cycles (i.e., the number of transferred bits).

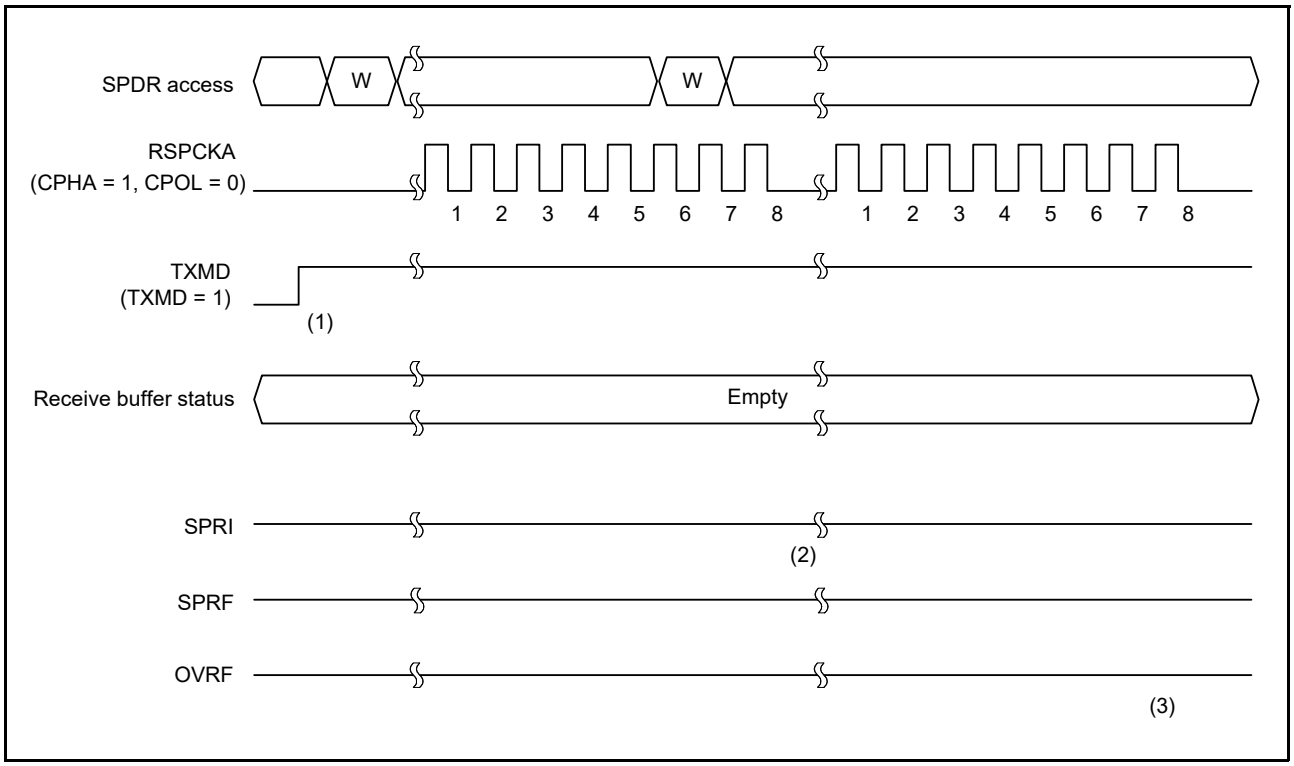


Figure 29.25 Operation Example of SPCR.TXMD = 1

The operation of the flags at timings shown in steps (1) to (3) in the figure is described below.

(1) Make sure there is no data left in the receive buffer and the SPSR.SPRF, OVRF flags are 0 before entering the mode of transmit operations only (SPCR.TXMD = 1).

(2) When a serial transfer ends with the receive buffer of SPDR empty, if the mode of transmit operations only is selected (SPCR.TXMD = 1), the SPRF flag remains 0 and the RSPI does not copy the data from the shift register to the receive buffer.

(3) Since the receive buffer of SPDR does not hold data that was received in the previous serial transfer, even when a serial transfer ends, the SPSR.OVRF flag retains the value of 0, and the data in the shift register is not copied to the receive buffer.

When performing transmit operations only (SPCR.TXMD = 1), the RSPI transmits data but does not receive data. Therefore, the SPSR.SPRF, OVRF flags remain 0 at the timings of (1) to (3).

29.3.7 Transmit Buffer Empty/Receive Buffer Full Interrupts

Figure 29.26 shows an example of operation of the transmit buffer empty interrupt (SPTI) and the receive buffer full interrupt (SPRI). The SPDR register access shown in Figure 29.26 indicates the condition of access to the SPDR register, where W denotes a write cycle, and R a read cycle. In the example in Figure 29.26, the RSPI performs an 8-bit serial transfer in which the SPCR.TXMD bit is 0, the SPDCR.SPFC[1:0] bits are 00b, the SPCMDm.CPHA bit is 1, and the SPCMDm.CPOL bit is 0. The numbers given under the RSPCKA waveform represent the number of RSPCK cycles (i.e., the number of transferred bits).

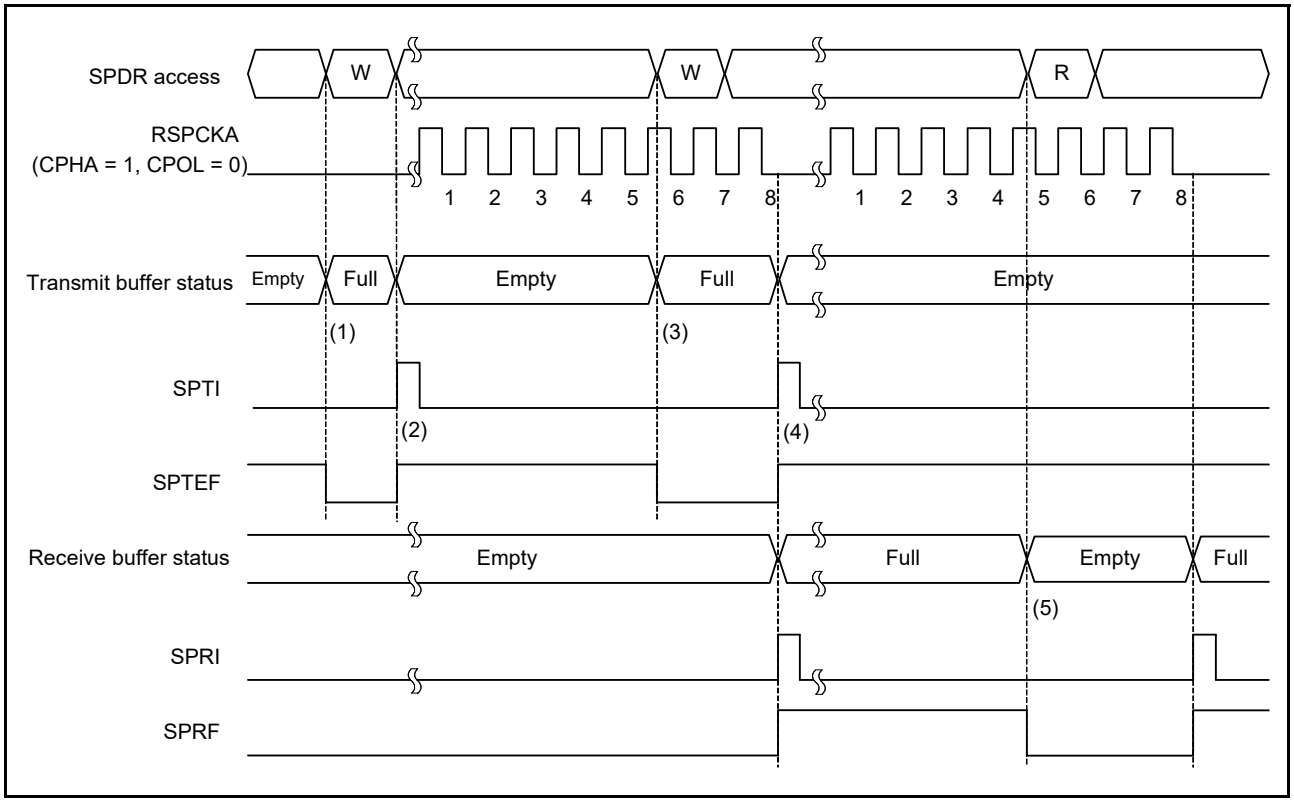


Figure 29.26 Operation Example of SPTI and SPRI Interrupts

The operation of the interrupts at timings shown in steps (1) to (5) in the figure is described below.

(1) When transmit data is written to SPDR when the transmit buffer of SPDR is empty (data for the next transfer is not set), the RSPI writes data to the transmit buffer and sets the SPSR.SPTEF flag to 0.

(2) If the shift register is empty, the RSPI copies the data from the transmit buffer to the shift register and generates a transmit buffer empty interrupt request (SPTI) and sets the SPSR.SPTEF flag to 1. How a serial transfer is started depends on the mode of the RSPI. For details, refer to section 29.3.10, SPI Operation, and section 29.3.11, Clock Synchronous Operation.

(3) When transmit data is written to SPDR in the transmit buffer empty interrupt routine or in the transmit buffer empty detecting process by polling the SPTEF flag, the data is transferred to the transmit buffer and the SPSR.SPTEF flag becomes 0. Because the data being transmitted is stored in the shift register, the RSPI does not copy the data from the transmit buffer to the shift register.

(4) When the serial transfer ends with the receive buffer of SPDR being empty, the RSPI copies the receive data from the shift register to the receive buffer, generates a receive buffer full interrupt request (SPRI), and sets the SPSR.SPRF flag to 1. Since the shift register becomes empty upon completion of serial transfer, when the transmit buffer had been full before the serial transfer ended, the RSPI sets the SPSR.SPTEF flag to 1 and copies the data from the transmit buffer to the shift register. Even when received data is not copied from the shift register to the receive buffer in an overrun error status, upon completion of the serial transfer, the RSPI determines that the shift register is empty, thus data transfer from the transmit buffer to the shift register is enabled.

(5) When SPDR is read in the receive buffer full interrupt routine or in the receive buffer full detecting process by polling the SPRF flag, the receive data can be read. When the receive data is read, the SPRF flag becomes 0.

If transmit data is written to SPDR while the transmit buffer holds data that has not yet been transmitted (the SPTEF flag is 0), the RSPI does not update the data in the transmit buffer. Transmit data should be written to SPDR in the transmit buffer empty interrupt request routine or in the transmit buffer empty detecting process by polling the SPTEF flag. To use a transmit buffer empty interrupt, set the SPTIE bit in SPCR to 1.
When setting the SPCR.SPE bit to 0 (RSPI disabled), the SPCR.SPTIE bit should also be set to 0. Otherwise (if the SPCR.SPE bit is 0 and the SPCR.SPTIE is 1), a transmit buffer empty interrupt request will occur.
When serial transfer ends with the receive buffer being full (the SPRF flag is 1), the RSPI does not copy data from the shift register to the receive buffer, and detects an overrun error (refer to section 29.3.8, Error Detection). To prevent a receive data overrun error, read the received data using a receive buffer full interrupt request before the next serial transfer ends. To use an RSPI receive buffer full interrupt, set the SPCR.SPRIE bit to 1.
Transmit and receive interrupts or the corresponding IRn.IR flags (where n is the interrupt vector number) in the ICU can be used to confirm the states of the transmit and receive buffers. Refer to section 14, Interrupt Controller (ICUb), for the interrupt vector numbers. The status of the transmit and receive buffers can be also confirmed by the SPTEF and SPRF flags.

29.3.8 Error Detection

In the normal RSPI serial transfer, the data written to the transmit buffer of SPDR is transmitted, and the received data can be read from the receive buffer of SPDR. If access is made to SPDR, depending on the status of the transmit/receive buffer or the status of the RSPI at the beginning or end of serial transfer, in some cases non-normal transfers can be executed.

If a non-normal transfer operation occurs, the RSPI detects the event as an underrun error, overrun error, parity error, or mode fault error. Table 29.8 lists the relationship between non-normal transfer operations and the RSPI's error detection function.

Table 29.8 Relationship between Non-Normal Transfer Operations and RSPI Error Detection Function

	Occurrence Condition	RSPI Operation	Error Detection
1	SPDR is written when the transmit buffer is full.	• The contents of the transmit buffer are kept. • Missing write data.	None
2	SPDR is read when the receive buffer is empty.	If reception has completed, then the received data is output to the bus. Otherwise, data received previously is output instead.	None
3	Serial transfer is started in slave mode when transmit data is still not loaded on the shift register.	• Serial transfer is suspended • Transmit/receive data is missing • The MISO signal output is disabled • RSPI function is disabled	Underrun error
4	Serial transfer terminates when the receive buffer is full.	• The contents of the receive buffer are kept. • Missing receive data.	Overrun error
5	An incorrect parity bit is received when performing full-duplex synchronous serial communications with the parity function enabled.	The parity error flag is asserted.	Parity error
6	The SSLA0 input signal is asserted when the serial transfer is idle in multi-master mode.	• Driving of the RSPCKA, MOSIA, SSLA1 to SSLA3 output signals is stopped. • RSPI function is disabled.	Mode fault error
7	The SSLA0 input signal is asserted during serial transfer in multi-master mode.	• Serial transfer is suspended. • Missing transmit/receive data. • Driving of the RSPCKA, MOSIA, SSLA1 to SSLA3 output signals is stopped. • RSPI function is disabled.	Mode fault error
8	The SSLA0 input signal is negated during serial transfer in slave mode.	• Serial transfer is suspended. • Missing transmit/receive data. • Driving of the MISOA output signal is stopped. • RSPI function is disabled.	Mode fault error

On operation 1 described in Table 29.8, the RSPI does not detect an error. To prevent data omission during the writing to SPDR, the SPDR register should be written when a transmit buffer empty interrupt request occurs or while the SPSR.SPTEF flag is 1.

Likewise, the RSPI does not detect an error on operation 2. To prevent extraneous data from being read, the SPDR register should be read when an RSPI receive buffer full interrupt request occurs or while the SPSR.SPRF flag is 1.

An underrun error shown in 3 is described in section 29.3.8.4, Underrun Error. An overrun error shown in 4 is described in section 29.3.8.1, Overrun Error. A parity error shown in 5 is described in section 29.3.8.2, Parity Error. A mode fault error shown in 6 to 8 is described in section 29.3.8.3, Mode Fault Error.

For the transmit and receive interrupts, refer to section 29.3.7, Transmit Buffer Empty/Receive Buffer Full Interrupts.

29.3.8.1 Overrun Error

If a serial transfer ends when the receive buffer of SPDR is full, the RSPI detects an overrun error, and sets the SPSR.OVRF flag to 1. When the OVRF flag is 1, the RSPI does not copy data from the shift register to the receive buffer so that the data prior to the occurrence of the error is retained in the receive buffer. To set the OVRF flag to 0, write 0 to the OVRF flag after the CPU has read SPSR with the OVRF flag set to 1.
Figure 29.27 shows an example of operations of the SPRF and OVRF flags. The SPSR and SPDR accesses shown in Figure 29.27 indicate the condition of accesses to SPSR and SPDR, respectively, where W denotes a write cycle, and R a read cycle. In the example in Figure 29.27, the RSPI performs an 8-bit serial transfer in which the SPCMDm.CPHA bit is 1 and the SPCMDm.CPOL bit is 0. The numbers given under the RSPCKA waveform represent the number of RSPCK cycles (i.e., the number of transferred bits).

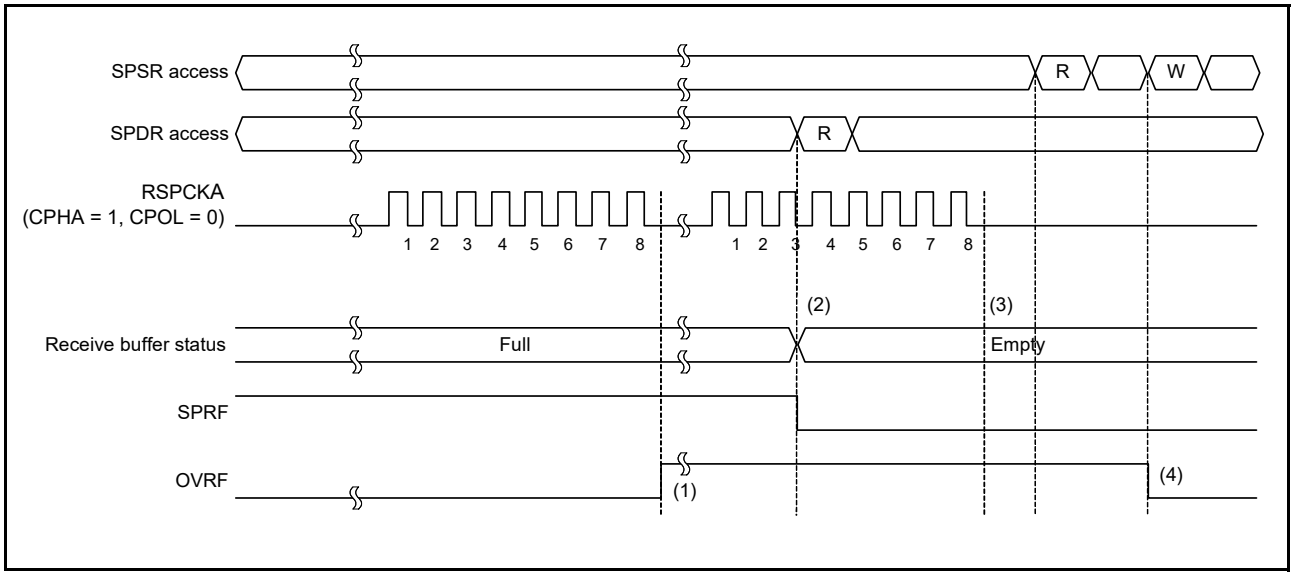


Figure 29.27 Operation Example of SPRF and OVRF Flags

The operation of the flags at the timing shown in steps (1) to (4) in the figure is described below.

(1) If a serial transfer terminates with the receive buffer full (the SPRF flag is 1), the RSPI detects an overrun error, and sets the OVRF flag to 1. The RSPI does not copy the data in the shift register to the receive buffer. Even if the SPPE bit is 1, parity errors are not detected. In master mode, the RSPI copies the pointer value to SPCMDm register to the SPSSR.SPECM[2:0] bits.

(2) When SPDR is read, the RSPI outputs the data in the receive buffer. At this time the SPRF flag becomes 0. Even if the receive buffer becomes empty, the OVRF flag does not become 0.

(3) If the serial transfer ends with the OVRF flag being 1 (an overrun error occurs), the RSPI does not copy the data in the shift register to the receive buffer (the SPRF flag remains 0). A receive buffer full interrupt is not generated. Even if the SPPE bit is 1, parity errors are not detected. When in master mode, the RSPI does not update the SPSSR.SPECM[2:0] bits. When in an overrun error state and the RSPI does not copy the received data from the shift register to the receive buffer, upon termination of the serial transfer, the RSPI determines that the shift register is empty; in this manner, data transfer from the transmit buffer to the shift register is enabled.

(4) If 0 is written to the OVRF flag after SPSR is read when the OVRF flag is 1, the OVRF flag is set to 0.

The occurrence of an overrun can be checked either by reading SPSR or by using an RSPI error interrupt and reading SPSR. When executing a serial transfer, measures should be taken to ensure the early detection of overrun errors, such as reading SPSR immediately after SPDR is read. When the RSPI is used in master mode, the pointer value to SPCMDm register at the occurrence of the error can be checked by reading the SPSSR.SPECM[2:0] bits.
If an overrun error occurs and the OVRF flag is set to 1, normal reception operations cannot be performed until the OVRF flag is set to 0.

When the RSPCK auto-stop function is enabled in master mode, an overrun error does not occur. Figure 29.28 and Figure 29.29 show the clock stop waveform when a serial transfer continues while the receive buffer is full in master mode.

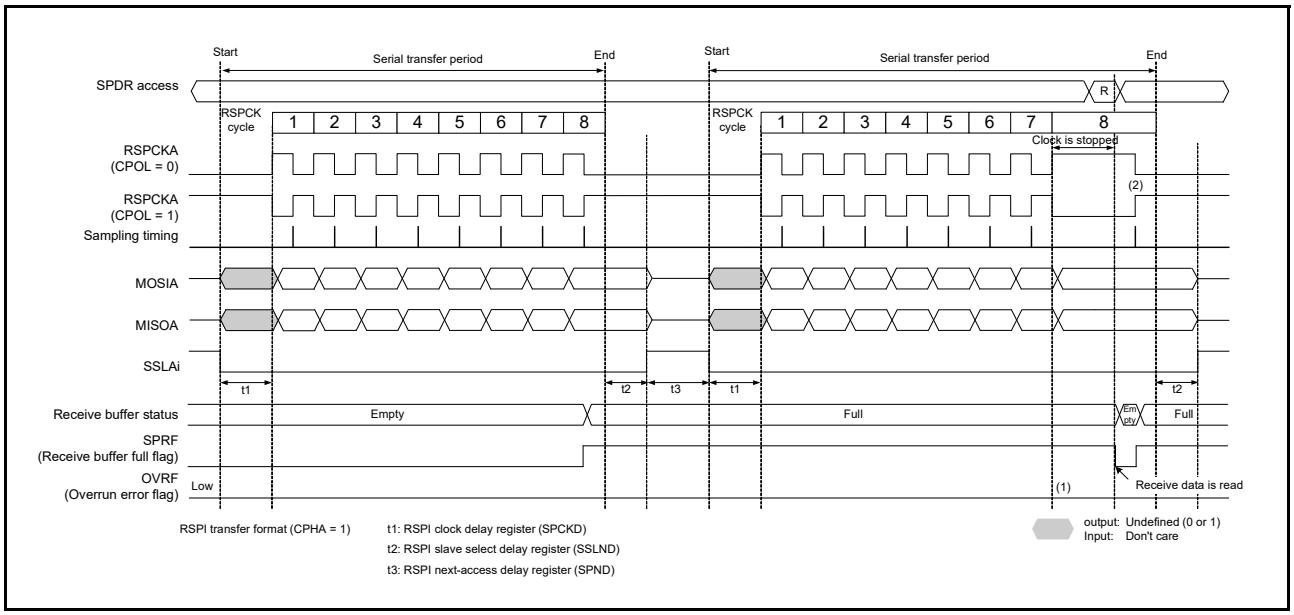


Figure 29.28 Clock Stop Waveform When a Serial Transfer Continues While the Receive Buffer is Full in Master Mode (CPHA = 1)

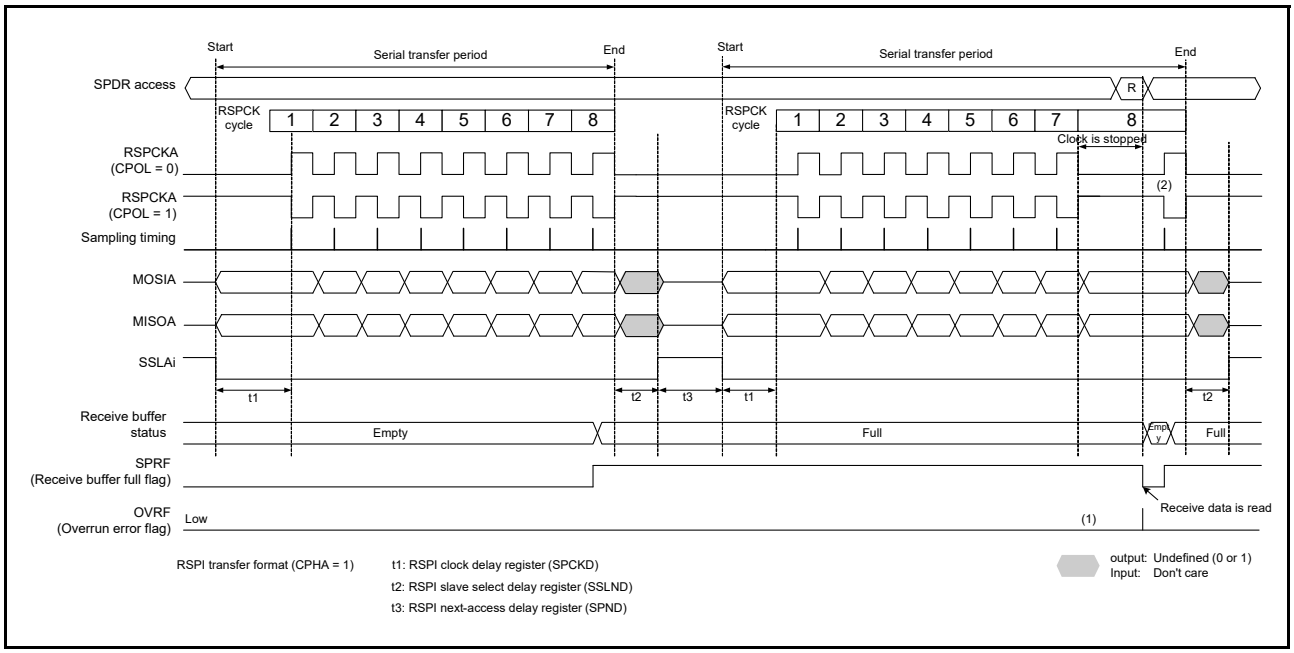


Figure 29.29 Clock Stop Waveform When a Serial Transfer Continues While the Receive Buffer is Full in Master Mode (CPHA = 0)

The operation of the flags at the timings shown in steps (1) and (2) in the figure is described below.

(1) When the receive buffer is full, an overrun error does not occur because the RSPCK clock is stopped.

(2) If SPDR is read while the clock is stopped, data in the receive buffer can be read. The RSPCK clock restarts after reading the receive buffer (after the SPRF flag becomes 0).

29.3.8.2 Parity Error

If full-duplex synchronous serial communications is performed with the SPCR.TXMD bit set to 0 and the SPCR2.SPPE bit set to 1, when serial transfer ends, the RSPI checks whether there are parity errors. Upon detecting a parity error in the received data, the RSPI sets the SPSR.PERF flag to 1. Since the RSPI does not copy the data in the shift register to the receive buffer when the SPSR.OVRF flag is set to 1, parity error detection is not performed for the received data. To set the PERF flag to 0, write 0 to the PERF flag after SPSR register is read with the PERF flag set to 1.
Figure 29.30 shows an example of operation of the OVRF and PERF flags. The SPSR access shown in Figure 29.30 indicates the condition of access to SPSR register, where W denotes a write cycle, and R a read cycle. In the example of Figure 29.30, full-duplex synchronous serial communications is performed while the SPCR.TXMD bit is 0 and the SPCR2.SPPE bit is 1. The RSPI performs an 8-bit serial transfer in which the SPCMDm.CPHA bit is 1 and the SPCMDm.CPOL bit is 0. The numbers given under the RSPCKA waveform represent the number of RSPCK cycles (i.e., the number of transferred bits).

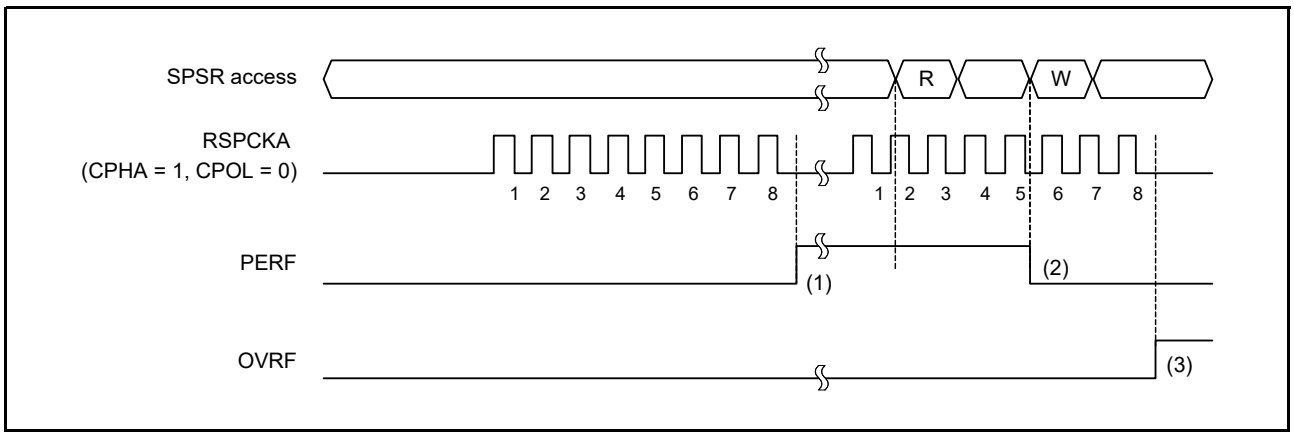


Figure 29.30 Operation Example of PERF Flag

The operation of the flags at the timing shown in steps (1) to (3) in the figure is described below.

(1) If a serial transfer terminates with the RSPI not detecting an overrun error, the RSPI copies the data in the shift register to the receive buffer. The RSPI judges the received data at this timing, and sets the PERF flag to 1 if a parity error is detected. In master mode, the RSPI copies the pointer value to SPCMDm register to the SPSSR.SPECM[2:0] bits.

(2) If 0 is written to the PERF flag after SPSR register is read when the PERF flag is 1, the PERF flag is set to 0.

(3) When the RSPI detects an overrun error and serial transfer is terminated, the data in the shift register is not copied to the receive buffer. The RSPI does not perform parity error detection at this timing.

The occurrence of a parity error can be checked either by reading the SPSR register or by using an RSPI error interrupt and reading the SPSR register. When executing a serial transfer, measures should be taken to ensure the early detection of parity errors, such as reading SPSR. When the RSPI is used in master mode, the pointer value to SPCMDm register at the occurrence of the error can be checked by reading the SPSSR.SPECM[2:0] bits.

29.3.8.3 Mode Fault Error

The RSPI operates in multi-master mode when the SPCR.MSTR bit is 1, the SPCR.SPMS bit is 0, and the SPCR.MODFEN bit is 1. If the active level is input with respect to the SSLA0 input signal of the RSPI in multi-master mode, the RSPI detects a mode fault error irrespective of the status of the serial transfer, and sets the SPSR.MODF flag to 1. Upon detecting the mode fault error, the RSPI copies the value of the pointer to SPCMDm to the SPSSR.SPECM[2:0] bits. The active level of the SSLA0 signal is determined by the SSLP.SSL0P bit.

When the MSTR bit is 0, the RSPI operates in slave mode. The RSPI detects a mode fault error if the MODFEN bit of the RSPI in slave mode is 1, and the SPMS bit is 0, and if the SSLA0 input signal is negated during the serial transfer period (from the time the driving of valid data is started to the time the final valid data is fetched).

Upon detecting a mode fault error, the RSPI stops driving of the output signals and clears the SPCR.SPE bit to 0 (refer to section 29.3.9, Initializing RSPI). In the case of multi-master configuration, detection of a mode fault error is used to stop driving of the output signals and the RSPI function, which allows the master right to be released.

The occurrence of a mode fault error can be checked either by reading SPSR or by using an RSPI error interrupt and reading SPSR. Detecting mode fault errors without utilizing the RSPI error interrupt requires polling of SPSR. When using the RSPI in master mode, the pointer value to SPCMDm register at the occurrence of the error can be checked by reading the SPSSR.SPECM[2:0] bits.

When the MODF flag is 1, writing of the value 1 to the SPE bit is ignored by the RSPI. To enable the RSPI function after the detection of a mode fault error, set the MODF flag to 0. When setting the MODF flag to 0, the SPE bit becomes 1.

29.3.8.4 Underrun Error

If a serial transfer is started in slave mode (the SPCR.MSTR bit is 0) when the SPCR.SPE bit is 1 (RSPI function is enabled) and transmit data is still not loaded on the shift register, the RSPI detects an underrun error, and sets the SPSR.MODF and SPSR.UDRF flags to 1. Upon detecting an underrun error, the RSPI stops driving of the output signals and clears the SPCR.SPE bit to 0. Clearing of the SPE bit disables the RSPI function. (Refer to section 29.3.9, Initializing RSPI). The occurrence of an underrun error can be checked either by reading SPSR or by using an RSPI error interrupt and reading SPSR. Detecting underrun errors without utilizing the RSPI error interrupt requires polling of SPSR. When the MODF flag is 1, writing of the value 1 to the SPE bit is ignored by the RSPI. To enable the RSPI function after the detection of an underrun error, set the MODF flag to 0. When setting the MODF flag to 0, the SPE bit becomes 1.

29.3.9 Initializing RSPI

If 0 is written to the SPCR.SPE bit or the RSPI sets the SPE bit to 0 because of the detection of a mode fault error or an underrun error, the RSPI disables the RSPI function, and initializes some of the module functions. When a system reset is generated, the RSPI initializes all of the module functions. The following describes initialization by the clearing of the SPCR.SPE bit and initialization by a system reset.

29.3.9.1 Initialization by Clearing the SPE Bit

When the SPCR.SPE bit is set to 0, the RSPI performs the following initialization:

- Suspending any serial transfer that is being executed
- Stopping the driving of output signals (Hi-Z) in slave mode
- Initializing the internal state of the RSPI
- Initializing the transmit buffer of the RSPI (Set the SPTEF flag to 1)

Initialization by the clearing of the SPE bit does not initialize the control bits of the RSPI. For this reason, the RSPI can be started in the same transfer mode as prior to the initialization if the SPE bit is set to 1 again.
The SPSR.SPRF, SPSR.OVRF, SPSR.MODF, SPSR.PERF, and SPSR.UDRF flags are not initialized, nor is the value of the RSPI sequence status register (SPSSR) initialized. For this reason, even after the RSPI is initialized, data from the receive buffer can be read in order to check the status of error occurrence during an RSPI transfer.
The transmit buffer is initialized to an empty state (the SPTEF flag is 1). Therefore, if the SPCR.SPTIE bit is set to 1 after RSPI initialization, a transmit buffer empty interrupt is generated. When the RSPI is initialized, in order to disable any transmit buffer empty interrupt, 0 should be written to the SPTIE bit simultaneously with the writing of 0 to the SPE bit.

29.3.9.2 System Reset

The initialization by a system reset completely initializes the RSPI through the initialization of all bits for controlling the RSPI, initialization of the status bits, and initialization of data registers, in addition to the requirements described in section 29.3.9.1, Initialization by Clearing the SPE Bit.

29.3.10 SPI Operation

29.3.10.1 Master Mode Operation

The only difference between single-master mode operation and multi-master mode operation lies in mode fault error detection (refer to section 29.3.8, Error Detection). When operating in single-master mode, the RSPI does not detect mode fault errors whereas the RSPI running in multi-master mode does detect mode fault errors. This section explains operations that are common to single-master mode and multi-master mode.

(1) Starting a Serial Transfer

The RSPI updates the data in the transmit buffer (SPTX) when data is written to the RSPI data register (SPDR) with the RSPI transmit buffer being empty (the SPTEF flag is 1 and data for the next transfer is not set). When the shift register is empty after the number of frames set in the SPDCR.SPFC[1:0] bits are written to the SPDR, the RSPI copies data from the transmit buffer to the shift register and starts serial transfer. Upon copying transmit data to the shift register, the RSPI changes the status of the shift register to “full”, and upon termination of serial transfer, it changes the status of the shift register to “empty”. The status of the shift register cannot be referenced.
For details on the RSPI transfer format, refer to section 29.3.5, Transfer Format. The polarity of the SSLAi output pins depends on the SSLP register settings.

(2) Terminating a Serial Transfer

Irrespective of the SPCMDm.CPHA bit, the RSPI terminates the serial transfer after transmitting an RSPCKA edge corresponding to the final sampling timing. If free space is available in the receive buffer (SPRX) (the SPRF flag is 0), upon termination of serial transfer, the RSPI copies data from the shift register to the receive buffer of the SPDR register. It should be noted that the final sampling timing varies depending on the bit length of transfer data. In master mode, the RSPI data length depends on the SPCMDm.SPB[3:0] bit setting. The polarity of the SSLAi output pin depends on the SSLP register settings.
For details on the RSPI transfer format, refer to section 29.3.5, Transfer Format.

(3) Sequence Control

The transfer format that is employed in master mode is determined by SPSCR, SPCMDm, SPBR, SPCKD, SSLND, and SPND registers.

SPSCR is a register used to determine the sequence configuration for serial transfers that are executed by the RSPI in master mode. The following items are set in SPCMDm register: SSLAi pin output signal value, MSB/LSB first, data length, some of the bit rate settings, RSPCK polarity/phase, whether SPCKD is to be referenced, whether SSLND is to be referenced, and whether SPND is to be referenced. SPBR holds some of the bit rate settings; SPCKD, an RSPI clock delay value; SSLND, an SSL negation delay; and SPND, a next-access delay value.

According to the sequence length that is assigned to SPSCR, the RSPI makes up a sequence comprised of a part or all of SPCMDm register. The RSPI contains a pointer to the SPCMDm register that makes up the sequence. The value of this pointer can be checked by reading the SPSSR.SPCP[2:0] bits. When the SPCR.SPE bit is set to 1 and the RSPI function is enabled, the RSPI loads the pointer to the commands in SPCMD0, and incorporates the SPCMD0 settings into the transfer format at the beginning of serial transfer. The RSPI increments the pointer each time the next-access delay period for a data transfer ends. Upon completion of the serial transfer that corresponds to the final command comprising the sequence, the RSPI sets the pointer in SPCMD0, and in this manner the sequence is executed repeatedly.

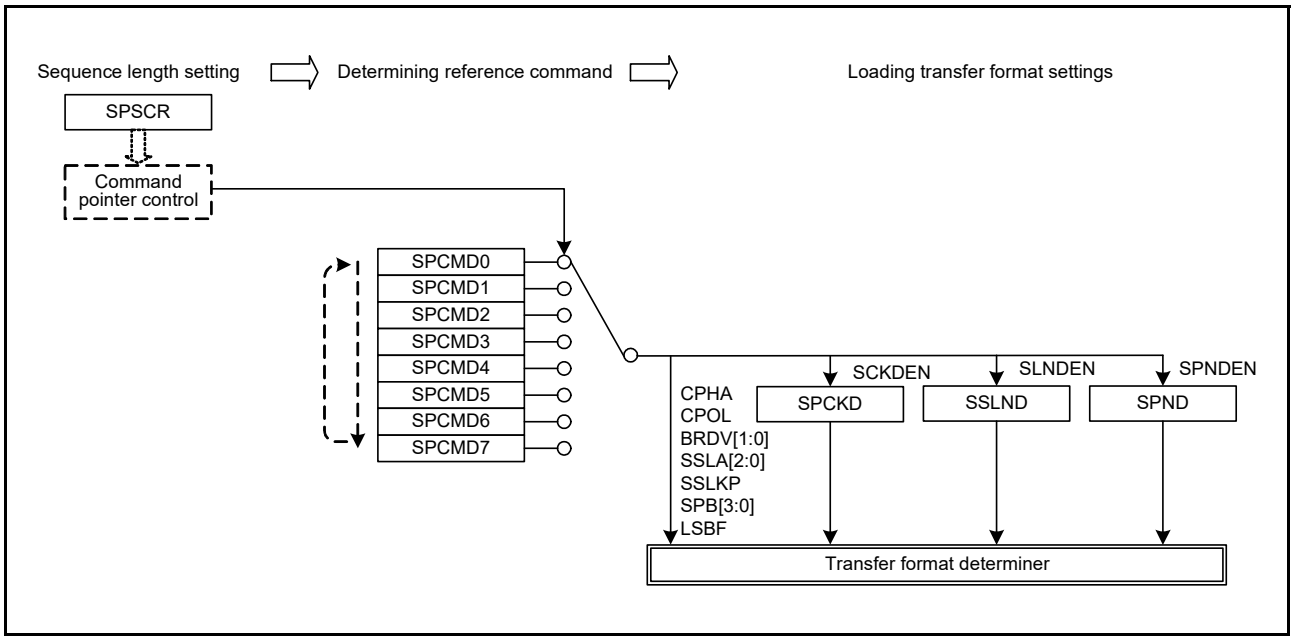


Figure 29.31 Procedure for Determining the Form of Serial Transfer in Master Mode

In this section, a frame is the combination of the data (SPDR) and the settings (SPCMDm).

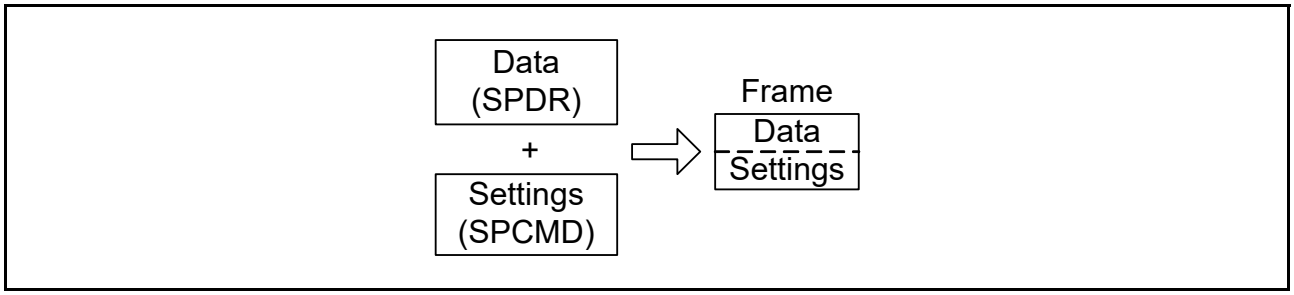


Figure 29.32 Concept of a Frame

Figure 29.33 shows the relationship between the command and the transmit and receive buffers in the sequence of operations specified by the settings in Table 29.4.

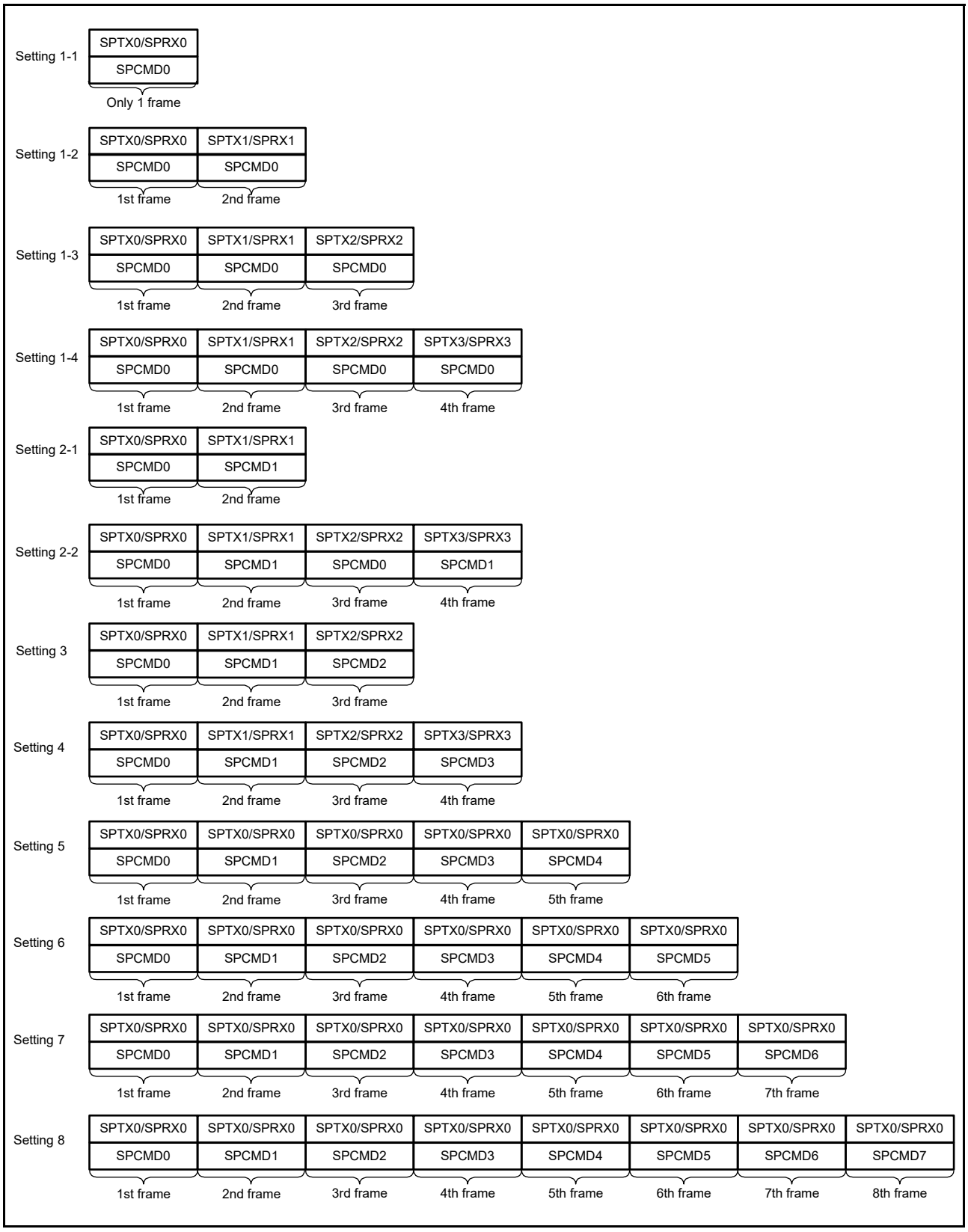


Figure 29.33 Correspondence between the RSPI Command Register and Transmit/Receive Buffers in Sequence Operations

(4) Burst Transfer

If the SPCMDm.SSLKP bit that the RSPI references during the current serial transfer is 1, the RSPI keeps the SSLAi signal level during the serial transfer until the beginning of the SSLAi signal assertion for the next serial transfer. If the SSLAi signal level for the next serial transfer is the same as the SSLAi signal level for the current serial transfer, the RSPI can execute continuous serial transfers while keeping the SSLAi signal assertion status (burst transfer).
Figure 29.34 shows an example of an SSLAi signal operation for the case where a burst transfer is implemented using SPCMD0 and SPCMD1 register settings. The text below explains the RSPI operations (1) to (7) as shown in Figure 29.34. It should be noted that the polarity of the SSLAi output signal depends on the SSLP register settings.

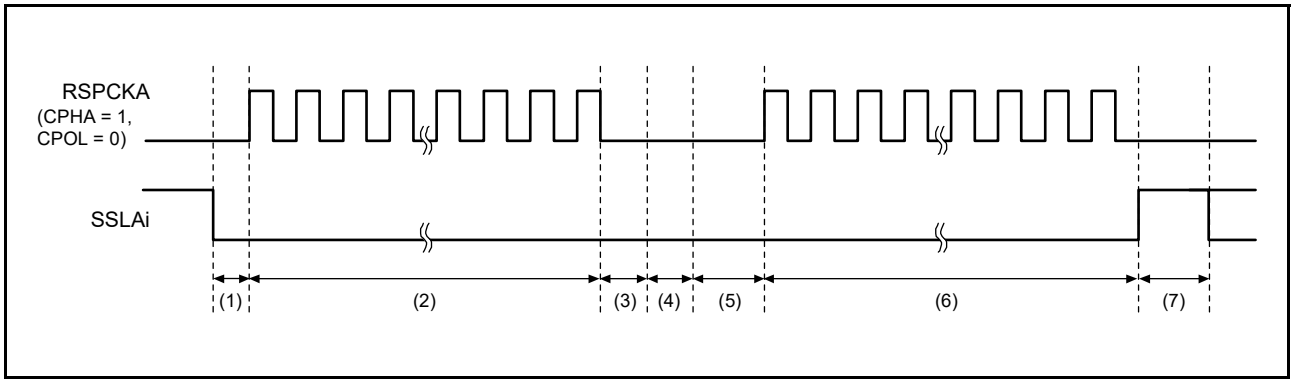


Figure 29.34 Example of Burst Transfer Operation Using SSLKP Bit

(1) Based on SPCMD0, the RSPI asserts the SSLAi signal and inserts RSPCK delays.
(2) The RSPI executes serial transfers according to SPCMD0.
(3) The RSPI inserts SSL negation delays.
(4) Since the SPCMD0.SSLKP bit is 1, the RSPI keeps the SSLAi signal value on SPCMD0. This period is sustained, at the shortest, for a period equal to the next-access delay of SPCMD0. If the shift register is empty after the passage of a minimum period, this period is sustained until the transmit data is stored in the shift register for the next transfer.
(5) Based on SPCMD1, the RSPI asserts the SSLAi signal and inserts RSPCK delays.
(6) The RSPI executes serial transfers according to SPCMD1.
(7) Because the SPCMD1.SSLKP bit is 0, the RSPI negates the SSLAi signal. In addition, a next-access delay is inserted according to SPCMD1.

If the SSLAi signal output settings in the SPCMDm register in which 1 is assigned to the SSLKP bit are different from the SSLAi signal output settings in the SPCMDm register to be used in the next transfer, the RSPI switches the SSLAi signal status to SSLAi signal assertion ((5) in Figure 29.34) corresponding to the command for the next transfer. Note that if such an SSLAi signal switching occurs, the slaves that drive the MISOA signal compete, and collision of signal levels may occur.
The RSPI in master mode references the SSLAi signal operation within the module for the case where the SSLKP bit is not used. Even when the SPCMDm.CPHA bit is 0, the RSPI can accurately start serial transfers by using the SSLAi signal assertion for the next transfer that is detected internally.

(5) RSPCK Delay (t1)

The RSPCK delay value of the RSPI in master mode depends on the SPCMDm.SCKDEN bit setting and the SPCKD register setting. The RSPI determines the SPCMDm register to be referenced during serial transfer by pointer control, and determines an RSPCK delay value during serial transfer by using the SPCMDm.SCKDEN bit and SPCKD, as listed in Table 29.9. For a definition of RSPCK delay, refer to section 29.3.5, Transfer Format.

Table 29.9 Relationship among SCKDEN Bit, SPCKD, and RSPCK Delay Value

SPCMDm.SCKDEN Bit	SPCKD.SCKDL[2:0] Bits	RSPCK Delay Value
0	000b to 111b	1 RSPCK
1	000b	1 RSPCK
	001b	2 RSPCK
	010b	3 RSPCK
	011b	4 RSPCK
	100b	5 RSPCK
	101b	6 RSPCK
	110b	7 RSPCK
	111b	8 RSPCK

(6) SSL Negation Delay (t2)

The SSL negation delay value of the RSPI in master mode depends on the SPCMDm.SLNDEN bit setting and the SSLND register setting. The RSPI determines the SPCMDm register to be referenced during serial transfer by pointer control, and determines an SSL negation delay value during serial transfer by using the SPCMDm.SLNDEN bit and SSLND, as listed in Table 29.10. For a definition of SSL negation delay, refer to section 29.3.5, Transfer Format.

Table 29.10 Relationship among SLNDEN Bit, SSLND, and SSL Negation Delay Value

SPCMDm.SLNDEN Bit	SSLND.SLNDL[2:0] Bits	SSL Negation Delay Value
0	000b to 111b	1 RSPCK
1	000b	1 RSPCK
	001b	2 RSPCK
	010b	3 RSPCK
	011b	4 RSPCK
	100b	5 RSPCK
	101b	6 RSPCK
	110b	7 RSPCK
	111b	8 RSPCK

(7) Next-Access Delay (t3)

The next-access delay value of the RSPI in master mode depends on the SPCMDm.SPNDEN bit setting and the SPND setting. The RSPI determines the SPCMDm register to be referenced during serial transfer by pointer control, and determines a next-access delay value during serial transfer by using the SPCMDm.SPNDEN bit and SPND, as listed in Table 29.11. For a definition of next-access delay, refer to section 29.3.5, Transfer Format.

Table 29.11 Relationship among SPNDEN Bit, SPND, and Next-Access Delay Value

SPCMDm.SPNDEN Bit	SPND.SPNDL[2:0] Bits	Next-Access Delay Value
0	000b to 111b	1 RSPCK + 2 PCLK
1	000b	1 RSPCK + 2 PCLK
	001b	2 RSPCK + 2 PCLK
	010b	3 RSPCK + 2 PCLK
	011b	4 RSPCK + 2 PCLK
	100b	5 RSPCK + 2 PCLK
	101b	6 RSPCK + 2 PCLK
	110b	7 RSPCK + 2 PCLK
	111b	8 RSPCK + 2 PCLK

(8) Initialization Flowchart

Figure 29.35 is a flowchart illustrating an example of initialization in SPI operation when the RSPI is used in master mode. For a description of how to set up the interrupt controller and I/O ports, refer to the descriptions given in the individual blocks.

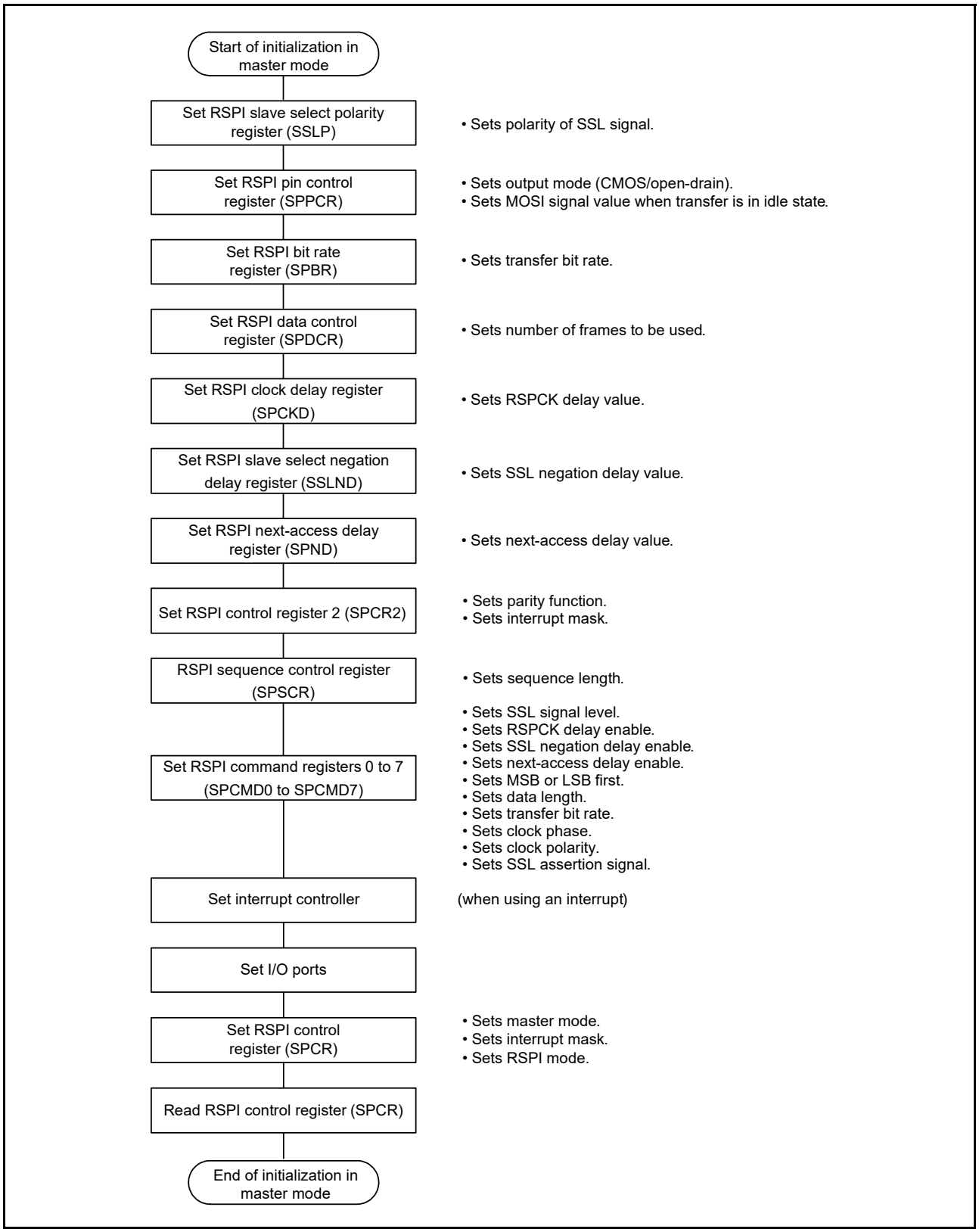


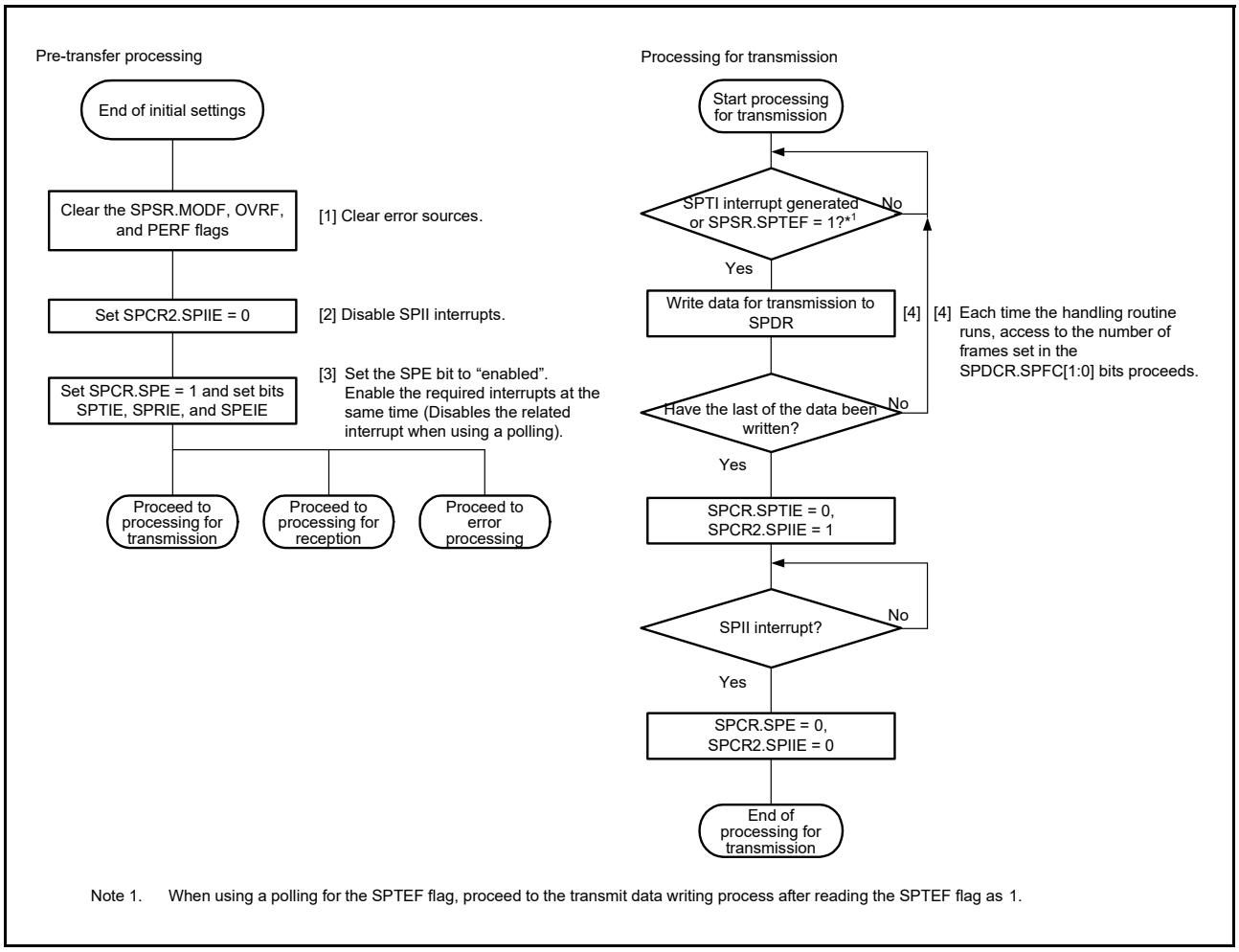
Figure 29.35 Example of Initialization Flowchart in Master Mode (SPI Operation)

(9) Software Processing Flow

Figure 29.36 to Figure 29.38 show examples of the flow of software processing.

(a) Transmit Processing Flow

When transmitting data, the CPU will be notified of the completion of data transmission by enabling the SPI interrupt after the last writing of data for transmission.
The completion of data transmission can also be checked by polling to see if the SPSR.IDLNF flag has become 0, instead of using the SPII interrupt. However, one cycle of PCLK is required for the time from when data for transmission is written in the SPDR register to when the IDLNF flag becomes 1. After the last data is written in the SPDR register, discard the value of the SPSR register once not to judge the condition with the IDLNF flag which has not yet become 1, and read and use the value of the SPSR.IDLNF flag to confirm the completion of data transmission.



Note 1. When using a polling for the SPTEF flag, proceed to the transmit data writing process after reading the SPTEF flag as 1.

Figure 29.36 Flowchart in Master Mode (Transmission)

(b) Receive Processing Flow

The RSPI does not handle receive-only operation, so processing for transmission is required.

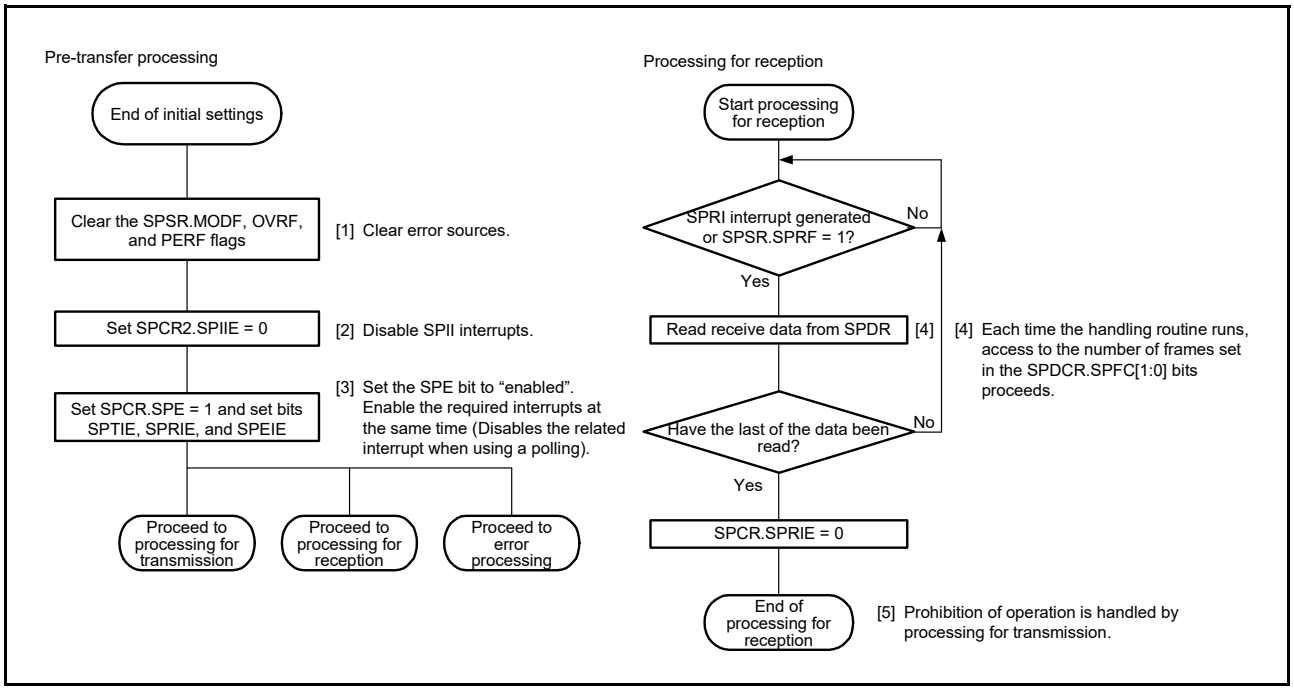


Figure 29.37 Flowchart in Master Mode (Reception)

(c) Flow of Error Processing

The RSPI has three types of error. When a mode fault error is generated, the SPCR.SPE bit is automatically cleared, stopping operations for transmission and reception. For errors from other sources, however, the SPCR.SPE bit is not cleared and operations for transmission and reception continue; accordingly, we recommend clearing of the SPCR.SPE bit to stop operations in the case of errors other than mode fault errors. Not doing so will lead to updating of the SPSSR.SPECM[2:0] bits.

When interrupts are used and an error occurs, if the ICU.IRn.IR flag for the SPTI or SPRI interrupt request is set to 1, clear the ICU.IRn.IR flag in the error processing routine. If the SPRI interrupt request is indicated, read the receive buffer and initialize the sequencer in the RSPI.

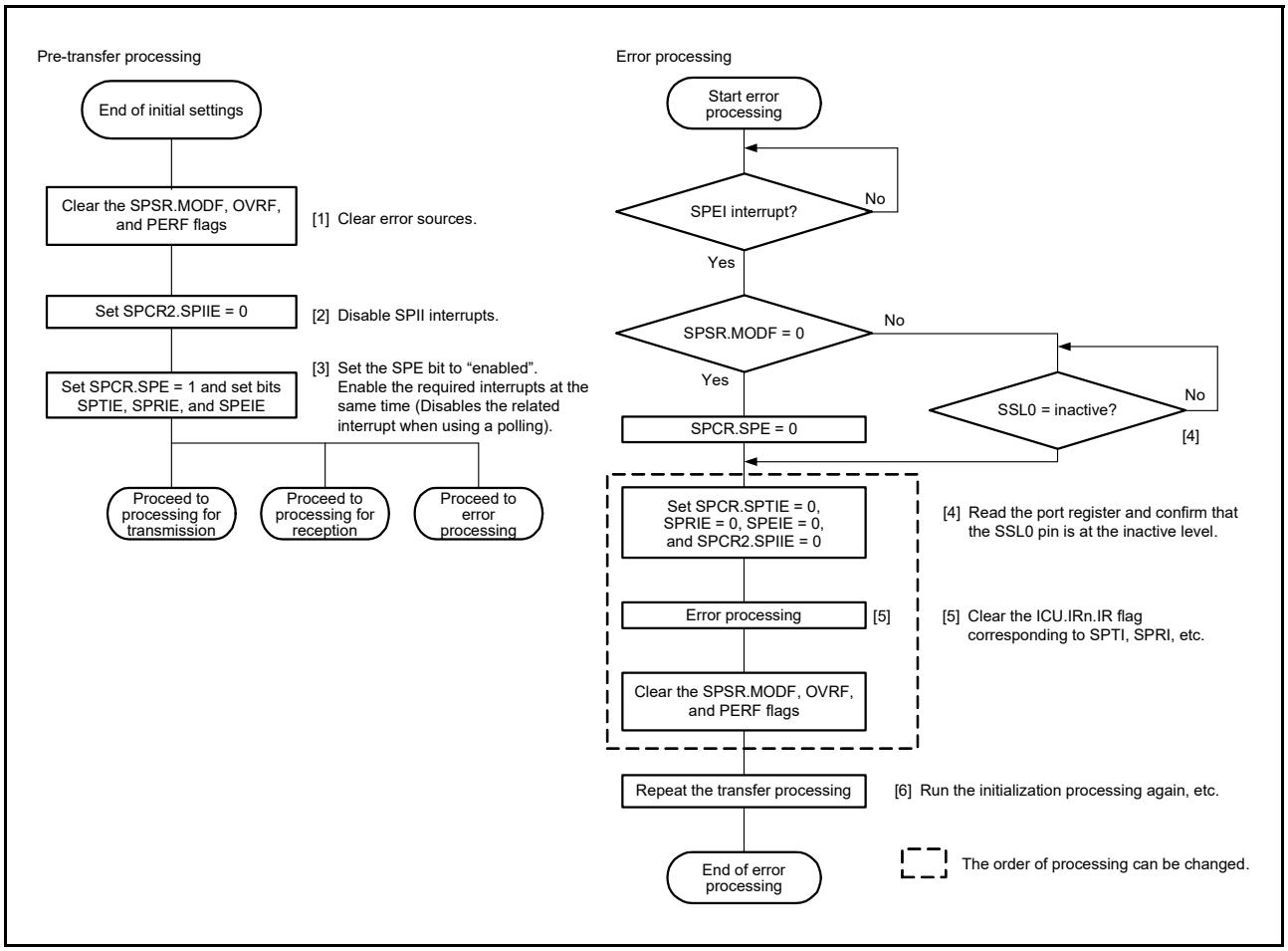


Figure 29.38 Flowchart for Master Mode (Error Processing)

29.3.10.2 Slave Mode Operation

(1) Starting a Serial Transfer

If the SPCMD0.CPHA bit is 0, when detecting an SSLA0 input signal assertion, the RSPI needs to start driving valid data to the MISOA output signal. For this reason, when the CPHA bit is 0, the assertion of the SSLA0 input signal triggers the start of a serial transfer.
If the CPHA bit is 1, when detecting the first RSPCKA edge in an SSLA0 signal asserted condition, the RSPI needs to start driving valid data to the MISOA output signal. For this reason, when the CPHA bit is 1, the first RSPCKA edge in an SSLA0 signal asserted condition triggers the start of a serial transfer.
Irrespective of the CPHA bit setting, the timing at which the RSPI starts driving of the MISOA output signal is the SSLA0 signal assertion timing. The data which is output by the RSPI is either valid or invalid, depending on the CPHA bit setting.
For details on the RSPI transfer format, refer to section 29.3.5, Transfer Format. The polarity of the SSLA0 input signal depends on the setting of the SSLP.SSL0P bit.

(2) Terminating a Serial Transfer

Irrespective of the SPCMD0.CPHA bit, the RSPI terminates the serial transfer after detecting an RSPCKA edge corresponding to the final sampling timing. When free space is available in the receive buffer (the SPRF flag is 0), upon termination of serial transfer the RSPI copies received data from the shift register to the receive buffer of the SPDR register. Upon termination of a serial transfer the RSPI changes the status of the shift register to “empty”, regardless of the receive buffer state. A mode fault error occurs if the RSPI detects an SSLA0 input signal negation from the beginning of serial transfer to the end of serial transfer (refer to section 29.3.8, Error Detection).
The final sampling timing changes depending on the bit length of transfer data. In slave mode, the RSPI data length depends on the SPCMD0.SPB[3:0] bit setting. The polarity of the SSLA0 input signal depends on the SSLP.SSL0P bit setting.
For details on the RSPI transfer format, refer to section 29.3.5, Transfer Format.

(3) Notes on Single-Slave Operations

If the SPCMD0.CPHA bit is 0, the RSPI starts serial transfers when it detects the assertion edge for an SSLA0 input signal. In the type of configuration shown in Figure 29.7 as an example, if the RSPI is used in single-slave mode, the SSLA0 signal is fixed at the active state. Therefore, when the CPHA bit is set to 0, the RSPI cannot correctly start a serial transfer. To correctly execute transmit/receive operations by the RSPI in slave mode in a configuration in which the SSLA0 input signal is fixed at the active state, the CPHA bit should be set to 1. If there is a need for setting the CPHA bit to 0, the SSLA0 input signal should not be fixed.

(4) Burst Transfer

If the SPCMD0.CPHA bit is 1, continuous serial transfer (burst transfer) can be executed while retaining the assertion state for the SSLA0 input signal. If the CPHA bit is 1, the period from the first RSPCKA edge to the sampling timing for the reception of the final bit in an SSLA0 signal active state corresponds to a serial transfer period. Even when the SSLA0 input signal remains at the active level, the RSPI can accommodate burst transfers because it can detect the start of an access.
If the CPHA bit is 0, the second and subsequent serial transfers during burst transfer cannot be executed correctly.

(5) Initialization Flowchart

Figure 29.39 is a flowchart illustrating an example of initialization in SPI operation when the RSPI is used in slave mode. For a description of how to set up the interrupt controller and I/O ports, refer to the descriptions given in the individual blocks.

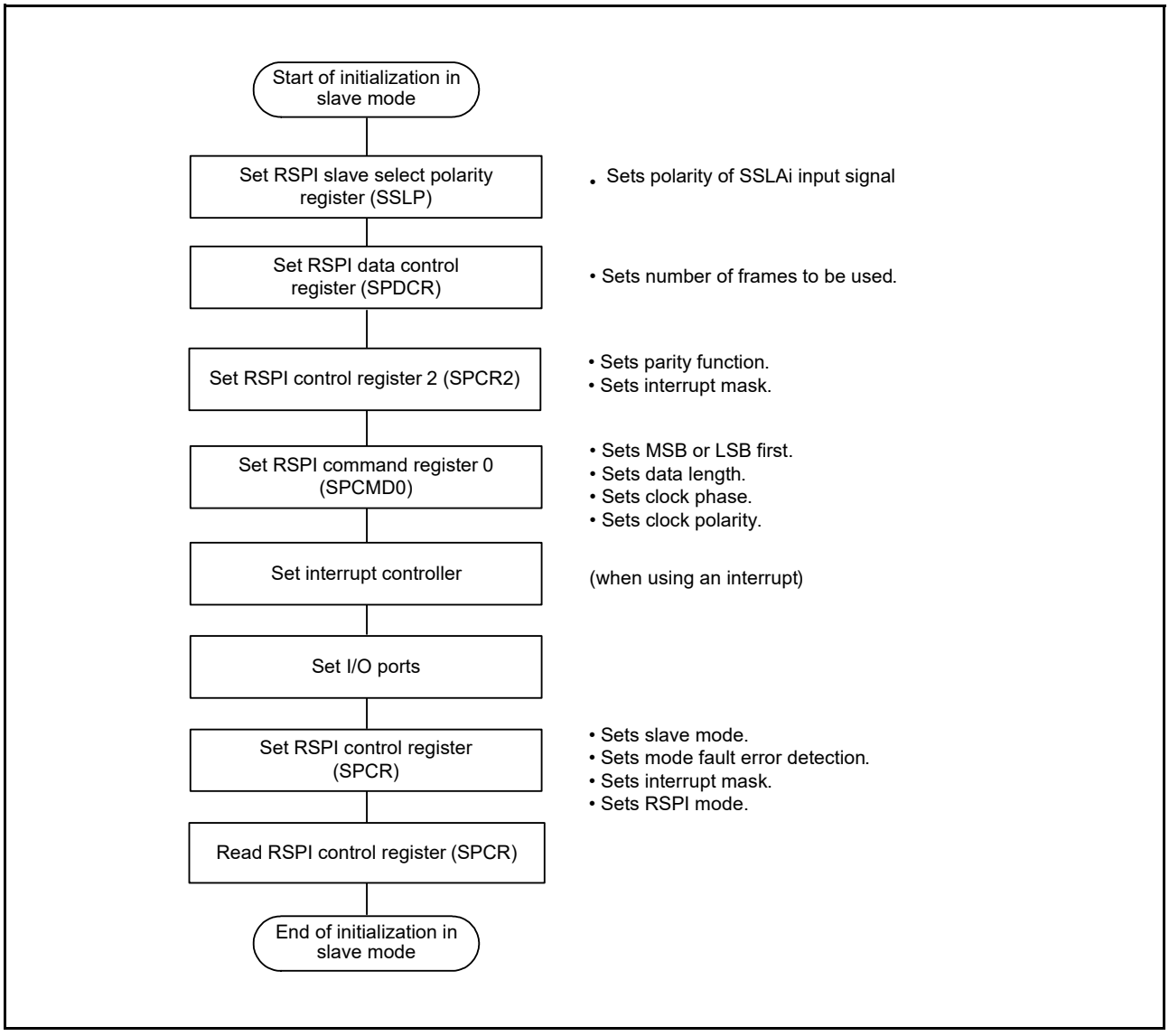


Figure 29.39 Example of Initialization Flowchart in Slave Mode (SPI Operation)

(6) Software Processing Flow

Figure 29.40 to Figure 29.42 show examples of the flow of software processing.

(a) Transmit Processing Flow

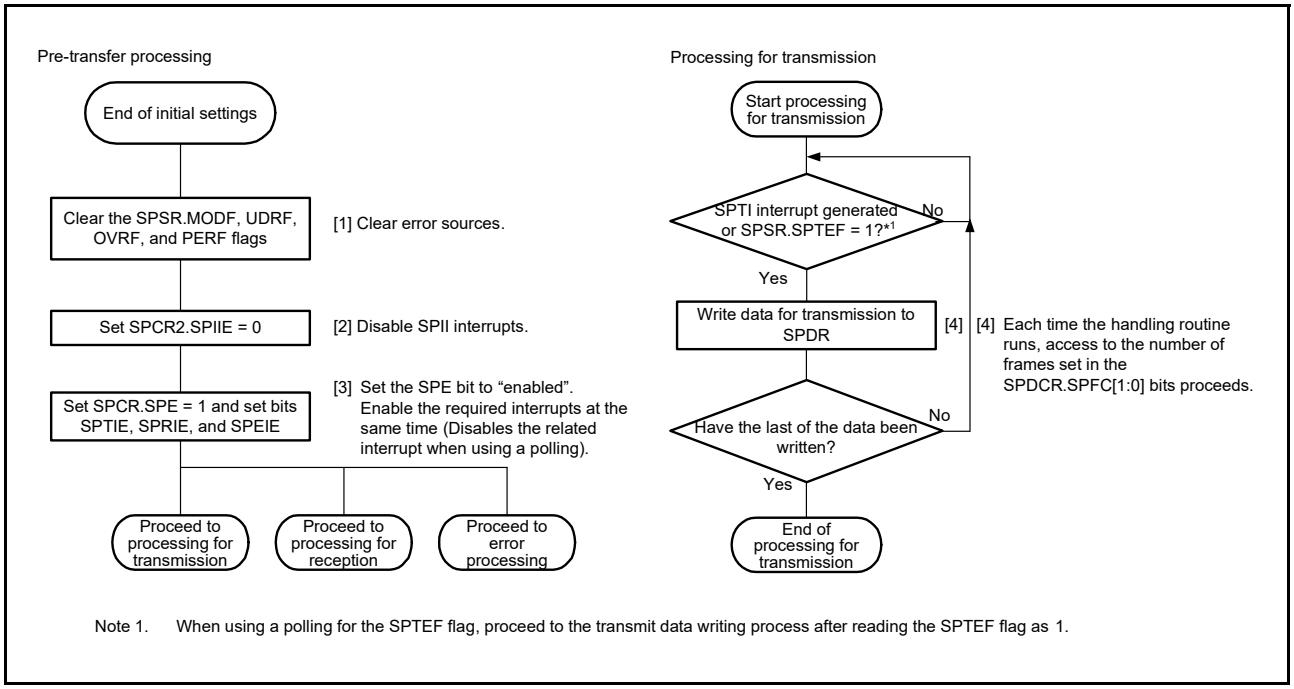


Figure 29.40 Flowchart in Slave Mode (Transmission)

(b) Receive Processing Flow

The RSPI does not handle receive-only operation, so processing for transmission is required.

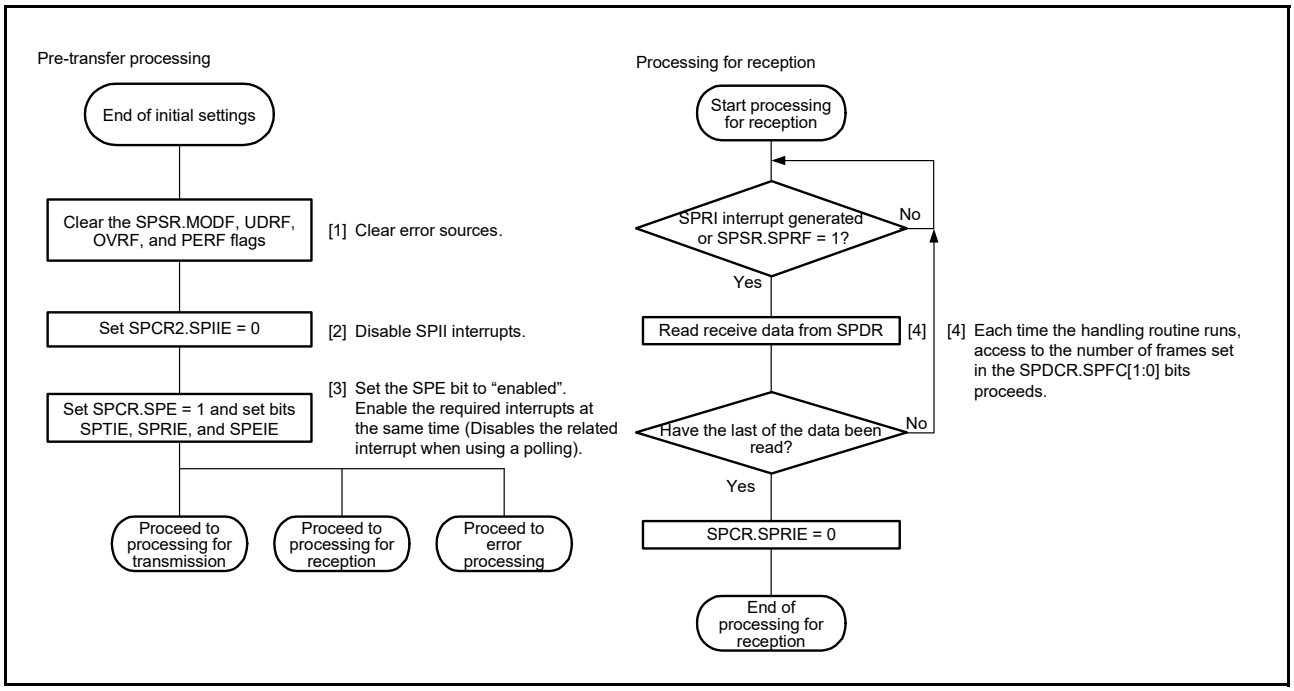


Figure 29.41 Flowchart in Slave Mode (Reception)

(c) Flow of Error Processing

In slave operation, even when a mode fault error is generated, the SPSR.MODF flag can be cleared regardless of the status of the SSLA0 pin.

When interrupts are used and an error occurs, if the ICU.IRn.IR flag for the SPTI or SPRI interrupt request is set to 1, clear the ICU.IRn.IR flag in the error processing routine. If the SPRI interrupt request is indicated, read the receive buffer and initialize the sequencer in the RSPI.

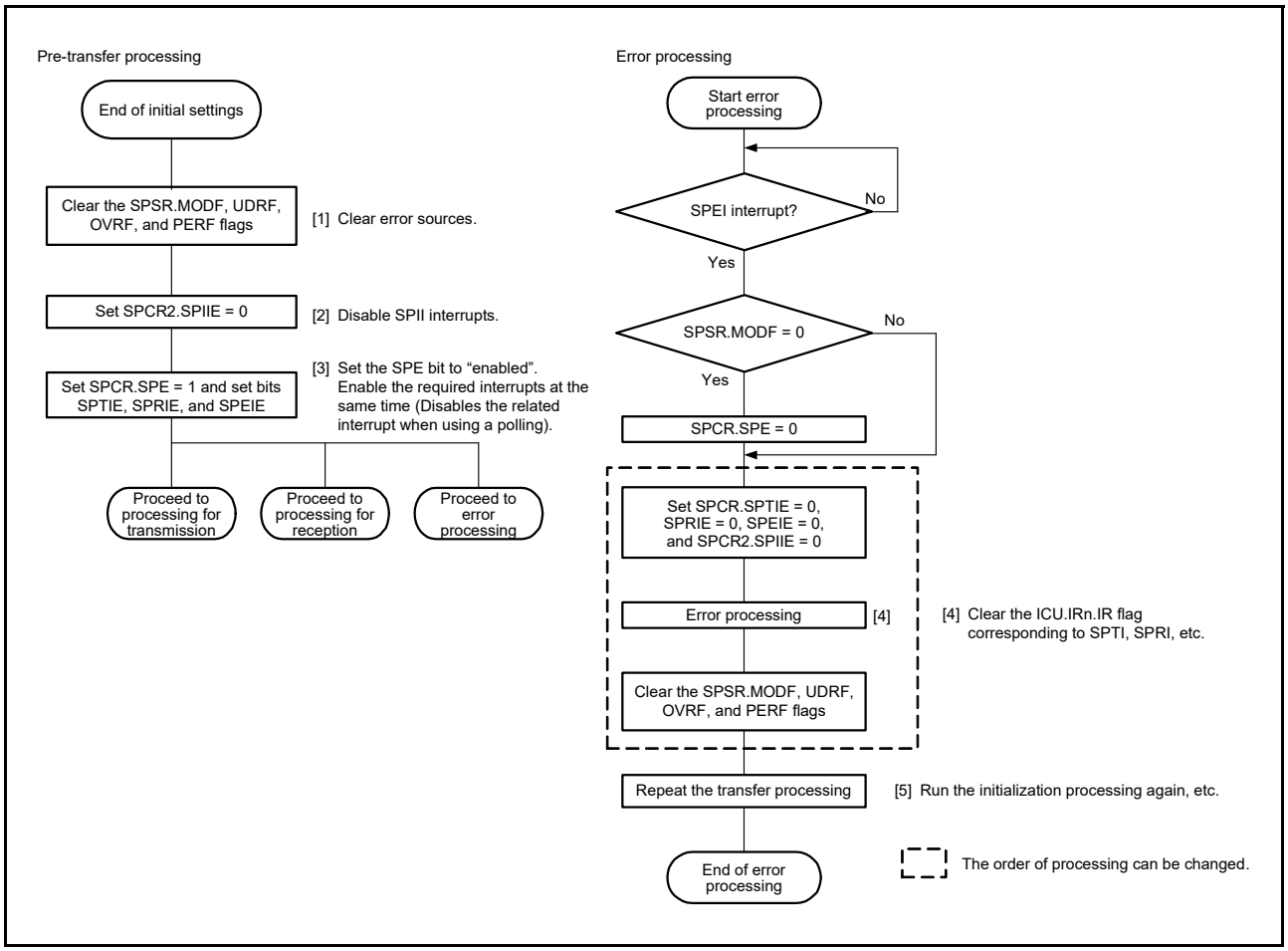


Figure 29.42 Flowchart for Slave Mode (Error Processing)

29.3.11 Clock Synchronous Operation

Setting the SPCR.SPMS bit to 1 selects clock synchronous operation of the RSPI. In clock synchronous operation, the SSLAi pin is not used, and the three pins of RSPCKA, MOSIA, and MISOA handle communications. The SSLAi pin is available as I/O port pins.
Although clock synchronous operation does not require use of the SSLAi pin, operation of the module is the same as in SPI operation. That is, in both master and slave operations, communications can be performed with the same flow as in SPI operation. However, mode fault errors are not detected because the SSLAi pin is not used.
Furthermore, operation should not be performed if clock synchronous operation proceeds when the SPCMDm.CPHA bit is set to 0 in slave mode (SPCR.MSTR = 0).

29.3.11.1 Master Mode Operation

(1) Starting a Serial Transfer

The RSPI updates the data in the transmit buffer (SPTX) of SPDR when data is written to the SPDR register with the transmit buffer being empty (the SPTEF flag is 1 and data for the next transfer is not set). When the shift register is empty after the number of frames set in the SPDCR.SPFC[1:0] bits are written to the SPDR, the RSPI copies data from the transmit buffer to the shift register and starts serial transmission. Upon copying transmit data to the shift register, the RSPI changes the status of the shift register to “full”, and upon termination of serial transfer, it changes the status of the shift register to “empty”. The status of the shift register cannot be referenced.
For details on the RSPI transfer format, refer to section 29.3.5, Transfer Format.
However, transfer in clock synchronous operation is conducted without the SSLA0 output signal.

(2) Terminating a Serial Transfer

The RSPI terminates the serial transfer after transmitting an RSPCKA edge corresponding to the sampling timing. If free space is available in the receive buffer (SPRX) (the SPRF flag is 0), upon termination of serial transfer, the RSPI copies data from the shift register to the receive buffer of the RSPI data register (SPDR).
It should be noted that the final sampling timing varies depending on the bit length of transfer data. In master mode, the RSPI data length depends on the SPCMDm.SPB[3:0] bit setting.
For details on the RSPI transfer format, refer to section 29.3.5, Transfer Format.
However, transfer in clock synchronous operation is conducted without the SSLA0 output signal.

(3) Sequence Control

The transfer format employed in master mode is determined by SPSCR, SPCMDm, SPBR, SPCKD, SSLND, and SPND registers. Although the SSLAi signals are not output in clock synchronous operation, these settings are valid.
SPSCR is a register used to determine the sequence configuration for serial transfers that are executed by the RSPI in master mode. The following items are set in SPCMDm register: SSLAi output signal value, MSB/LSB first, data length, some of the bit rate settings, RSPCKA polarity/phase, whether SPCKD is to be referenced, whether SSLND is to be referenced, and whether SPND is to be referenced. SPBR holds some of the bit rate settings; SPCKD, an RSPI clock delay value; SSLND, an SSL negation delay; and SPND, a next-access delay value.
According to the sequence length that is assigned to SPSCR, the RSPI makes up a sequence comprised of a part or all of SPCMDm register. The RSPI contains a pointer to the SPCMDm register that makes up the sequence. The value of this pointer can be checked by reading the SPSSR.SPCP[2:0] bits. When the SPCR.SPE bit is set to 1 and the RSPI function is enabled, the RSPI loads the pointer to the commands in SPCMD0 register, and incorporates the SPCMD0 register setting into the transfer format at the beginning of serial transfer. The RSPI increments the pointer each time the next-access delay period for a data transfer ends. Upon completion of the serial transfer that corresponds to the final command comprising the sequence, the RSPI sets the pointer in SPCMD0 register, and in this manner the sequence is executed repeatedly.

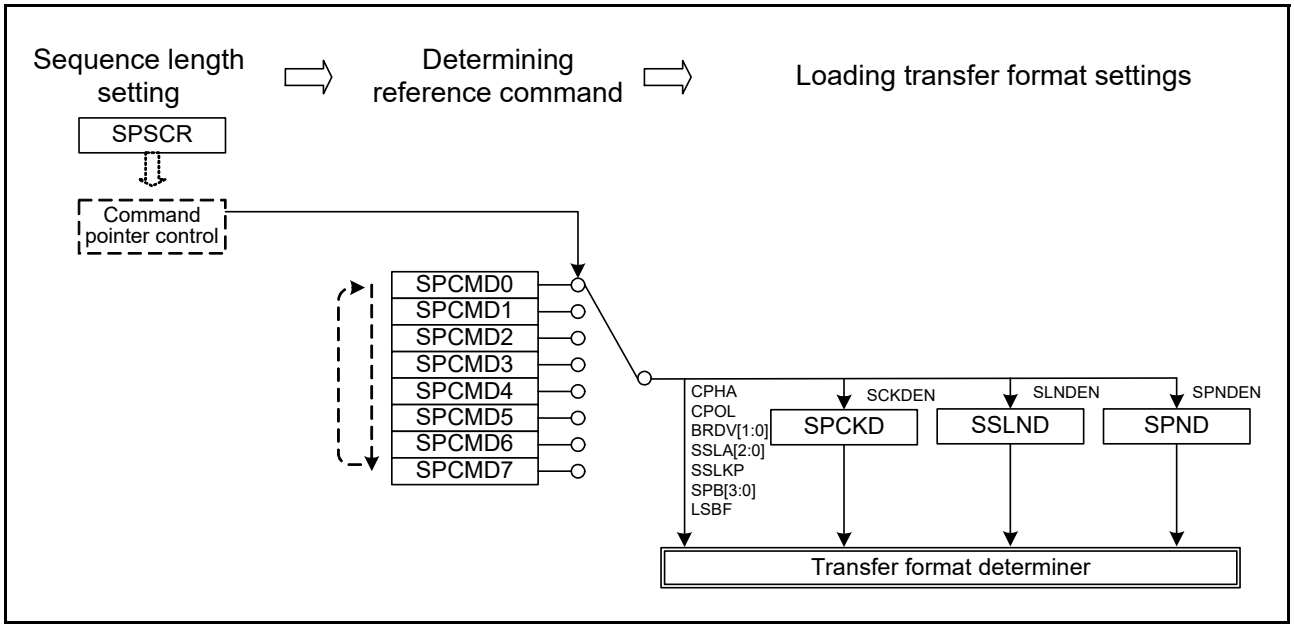


Figure 29.43 Procedure for Determining the Form of Serial Transmission in Master Mode

In this section, a frame is the combination of the data (SPDR) and the settings (SPCMDm).

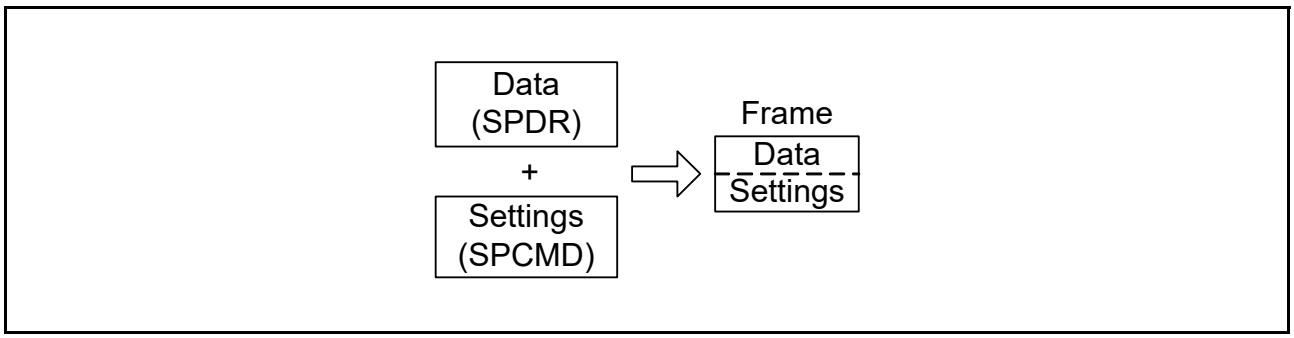


Figure 29.44 Concept of a Frame

Figure 29.45 shows the relationship between the command and the transmit and receive buffers in the sequence of operations specified by the settings in Table 29.4.

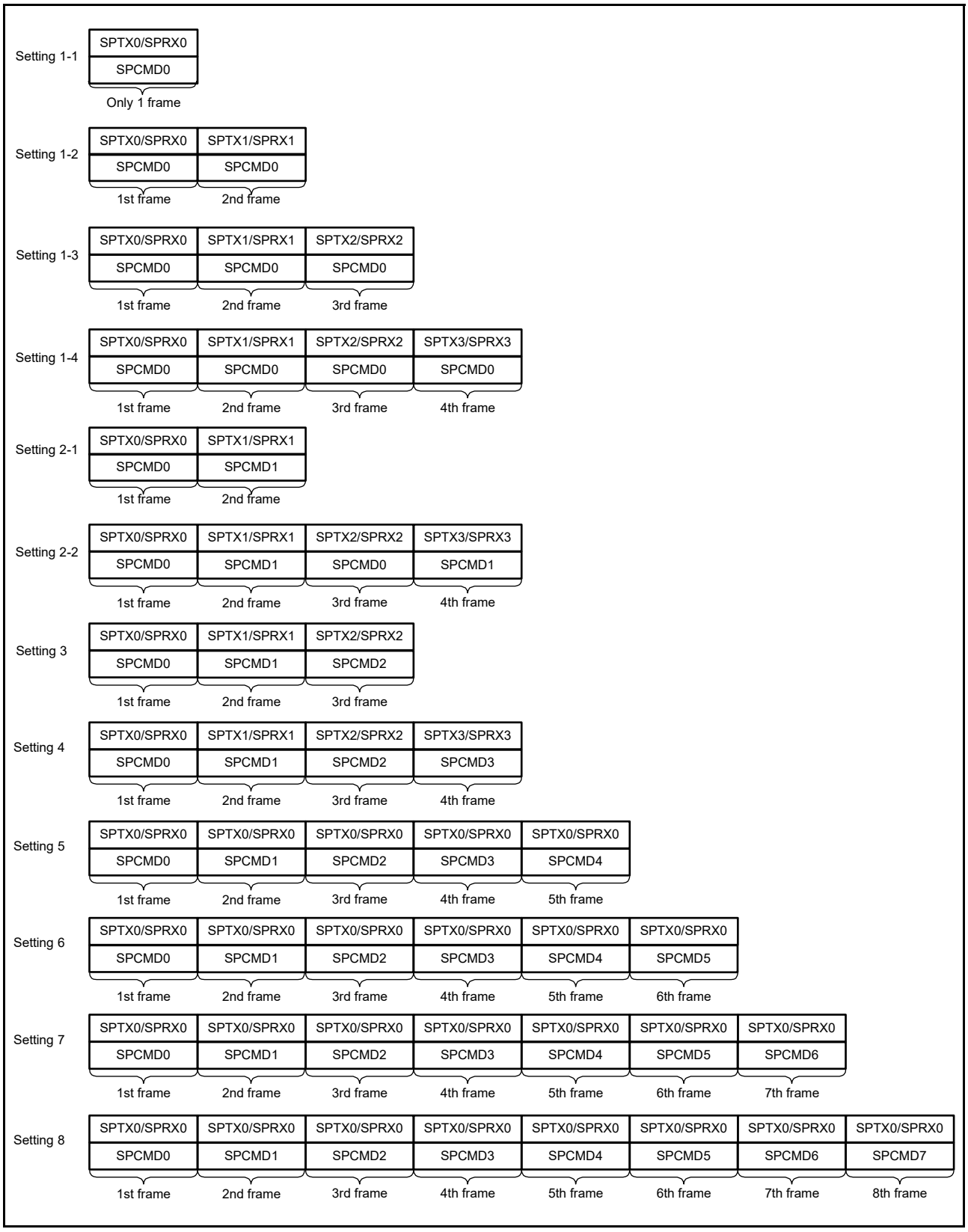


Figure 29.45 Correspondence between the RSPI Command Register and Transmit/Receive Buffers in Sequence Operations

(4) Initialization Flowchart

Figure 29.46 is a flowchart illustrating an example of initialization in clock synchronous operation when the RSPI is used in master mode. For a description of how to set up the interrupt controller and I/O ports, refer to the descriptions given in the individual blocks.

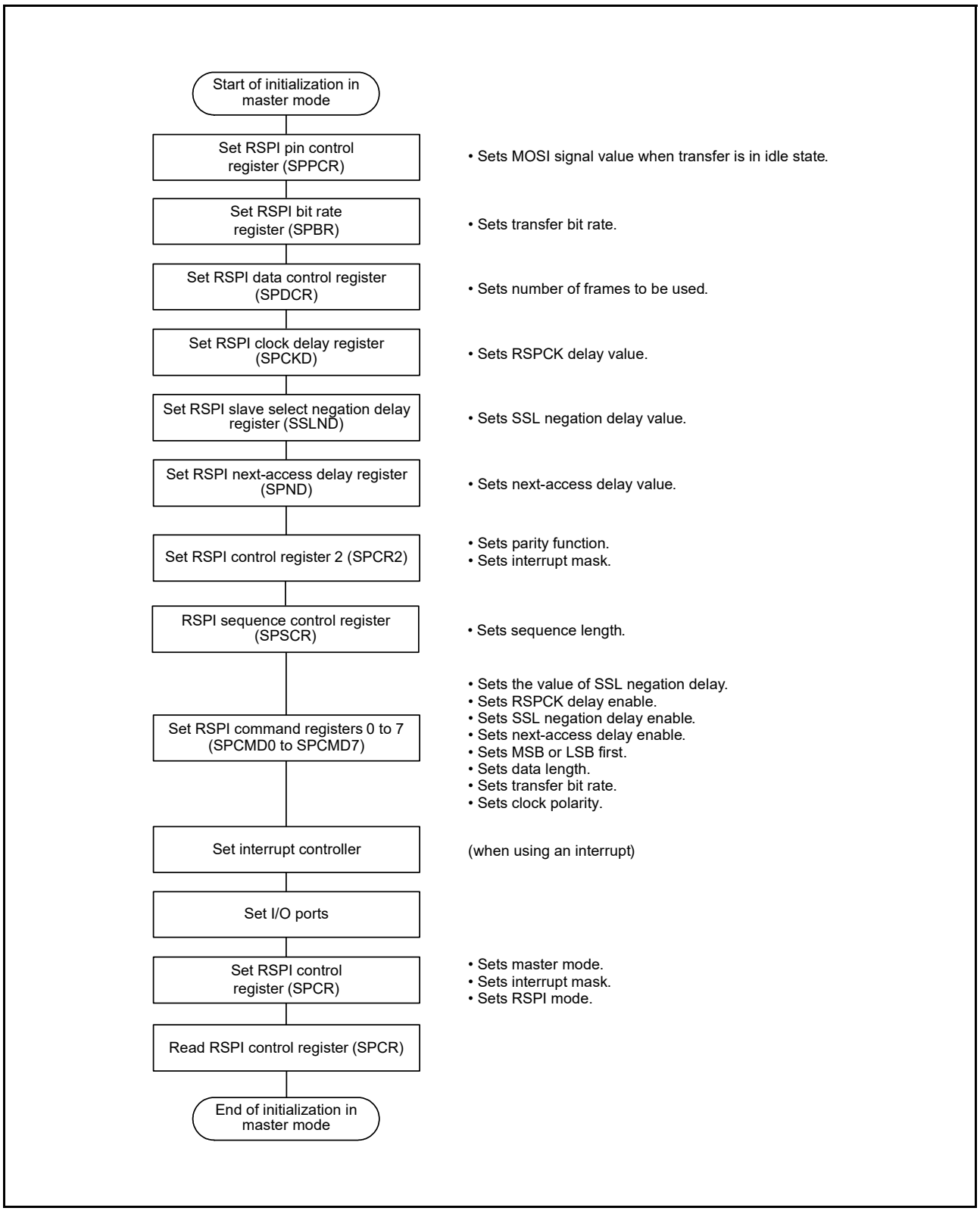


Figure 29.46 Example of Initialization Flowchart in Master Mode (Clock Synchronous Operation)

(5) Flow of Software Processing

Software processing during clock-synchronous master operation is the same as that for SPI master operation. For details, refer to section 29.3.10.1, (9) Software Processing Flow. Note that mode fault errors will not occur.

29.3.11.2 Slave Mode Operation

(1) Starting a Serial Transfer

When the SPCR.SPMS bit is 1, the first RSPCKA edge triggers the start of a serial transfer in the RSPI.
When the SPMS bit is 1, the RSPI drives the MISOA output signal.
For details on the RSPI transfer format, refer to section 29.3.5, Transfer Format.
It should be noted that the SSLA0 input signal is not used in clock synchronous operation.

(2) Terminating a Serial Transfer

The RSPI terminates the serial transfer after detecting an RSPCKA edge corresponding to the final sampling timing. When free space is available in the receive buffer (the SPRF flag is 0), upon termination of serial transfer the RSPI copies received data from the shift register to the receive buffer of the SPDR register. Upon termination of a serial transfer the RSPI changes the status of the shift register to “empty” regardless of the receive buffer status. The final sampling timing changes depending on the bit length of transfer data. In slave mode, the RSPI data length depends on the SPCMD0.SPB[3:0] bit setting.
For details on the RSPI transfer format, refer to section 29.3.5, Transfer Format.

(3) Initialization Flowchart

Figure 29.47 is a flowchart illustrating an example of initialization in clock synchronous operation when the RSPI is used in slave mode. For a description of how to set up the interrupt controller and I/O ports, refer to the descriptions given in the individual blocks.

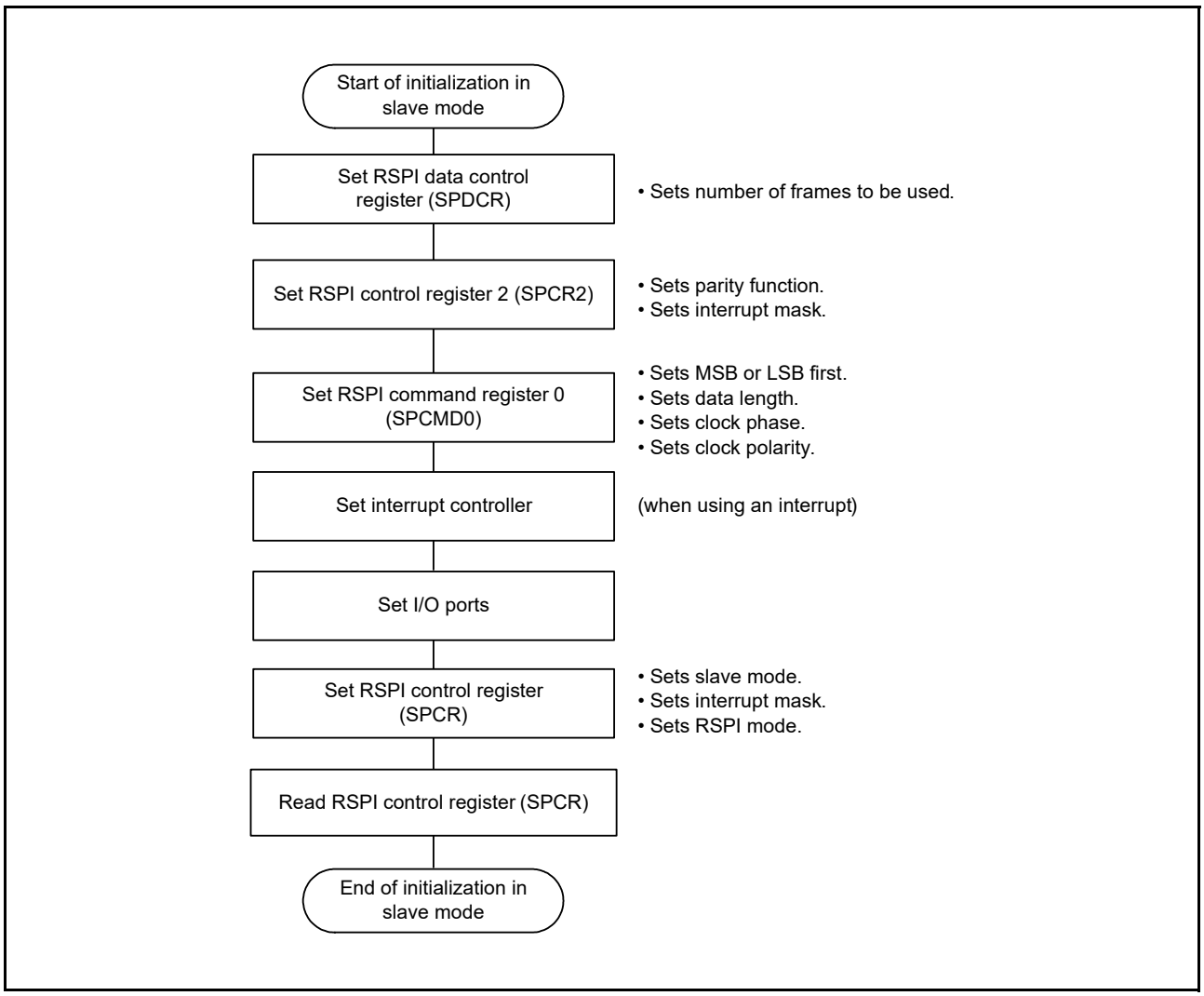


Figure 29.47 Example of Initialization Flowchart in Slave Mode (Clock Synchronous Operation)

(4) Flow of Software Processing

Software processing during clock-synchronous slave operation is the same as that for SPI slave operation. For details, refer to section 29.3.10.2, (6) Software Processing Flow. Note that mode fault errors will not occur.

29.3.12 Loopback Mode

When 1 is written to the SPPCR.SPLP2 bit or SPPCR.SPLP bit, the RSPI shuts off the path between the MISOA pin and the shift register if the SPCR.MSTR bit is 1, and between the MOSIA pin and the shift register if the SPCR.MSTR bit is 0, and connects the input path and output path of the shift register. The RSPI does not shut off the path between the MOSIA pin and the shift register if the SPCR.MSTR bit is 1, and between the MISOA pin and the shift register if the SPCR.MSTR bit is 0. This is called loopback mode. When a serial transfer is executed in loopback mode, the transmit data for the RSPI or the reversed transmit data becomes the received data for the RSPI.
Table 29.12 lists the relationship among the SPLP2 and SPLP bits and the received data. Figure 29.48 shows the configuration of the shift register I/O paths for the case where the RSPI in master mode is set in loopback mode (SPPCR.SPLP2 = 0, SPPCR.SPLP = 1).

Table 29.12 SPLP2 and SPLP Bit Settings and Received Data

SPPCR.SPLP2 Bit	SPPCR.SPLP Bit	Received Data
0	0	Input data from the MOSIA pin or MISOA pin
0	1	Inverted transmit data
1	0	Transmit data
1	1	Transmit data

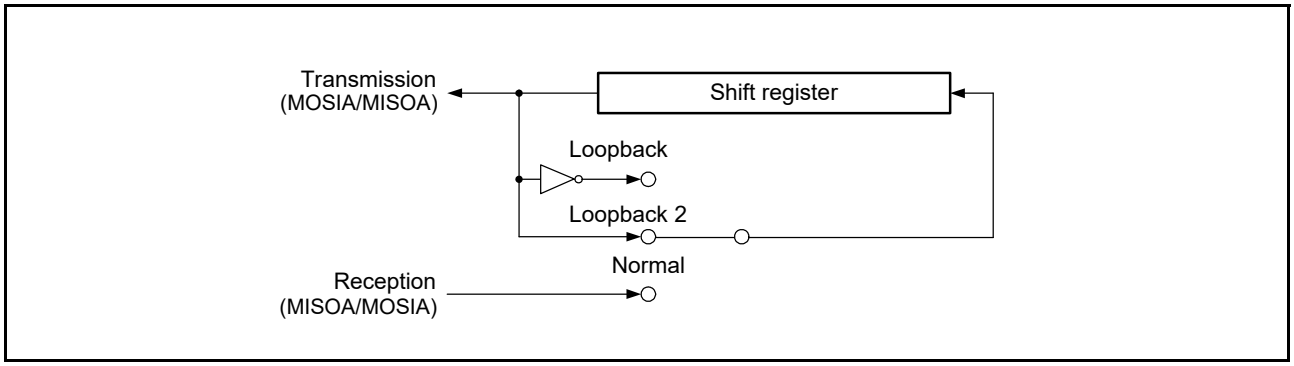


Figure 29.48 Configuration of Shift Register I/O Paths in Loopback Mode (Master Mode)

29.3.13 Self-Diagnosis of Parity Bit Function

The parity circuit consists of a parity bit adding unit used for transmit data and an error detecting unit used for received data. In order to detect defects in the parity bit adding unit and error detecting unit of the parity circuit, self-diagnosis is executed for the parity circuit following the flowchart shown in Figure 29.49.

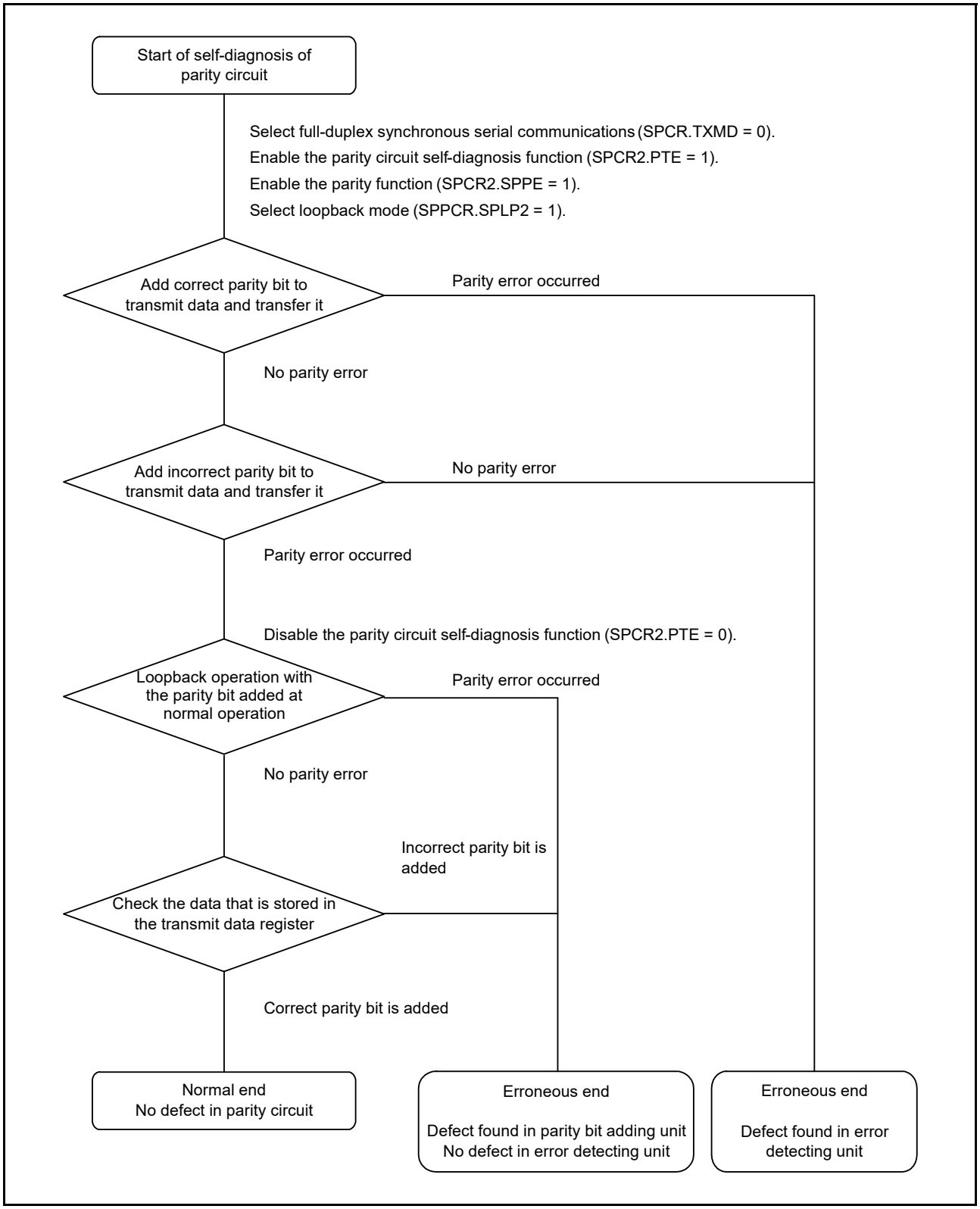


Figure 29.49 Flowchart for Self-Diagnosis of Parity Circuit

29.3.14 Interrupt Sources

The RSPI has interrupt sources of receive buffer full, transmit buffer empty, mode fault, underrun, overrun, parity error, and RSPI idle. In addition, the DTC can be activated by the receive buffer full or transmit buffer empty interrupt to perform data transfer.

Since the vector address for SPEI is allocated to interrupt requests due to mode fault, underrun, overrun, and parity errors, the actual interrupt source must be determined from the flags. Interrupt sources for the RSPI are listed in Table 29.13. An interrupt is generated on satisfaction of an interrupt condition in Table 29.13. Clear the receive buffer full and transmit buffer empty sources through data transfer.

When using the DTC to perform data transmission/reception, the DTC must be set up first to be in a status in which transfer is enabled before making the RSPI settings. For the method for setting the DTC, refer to section 17, Data Transfer Controller (DTCa).

If the conditions for generating a transmit buffer empty or receive buffer full interrupt are generated while the ICU.IRn.IR flag is 1, the interrupt is not output as a request for ICU but is retained internally (the capacity for retention is one request per source). A retained interrupt request is output when the ICU.IRn.IR flag becomes 0. A retained interrupt request is automatically discarded once it is output as an actual interrupt request. The interrupt enable bit (the SPCR.SPTIE or SPCR.SPRIE bit) for an internally retained interrupt request can also be cleared to 0.

Table 29.13 Interrupt Sources of RSPI

Interrupt Source	Symbol	Interrupt Condition	DTC Activation
Receive buffer full	SPRI	The receive buffer becomes full (the SPRF flag becomes 1) while the SPCR.SPRIE bit is 1.	Possible
Transmit buffer empty	SPTI	The transmit buffer becomes empty (the SPTEF flag becomes 1) while the SPCR.SPTIE bit is 1.	Possible
RSPI errors (mode fault, underrun, overrun and parity error)	SPEI	The SPSR.MODF, OVRF, or PERF flag is set to 1 while the SPCR.SPEIE bit is 1.	Impossible
RSPI idle	SPII	The SPSR.IDLNF flag is set to 0 while the SPCR2.SPIIE bit is 1.	Impossible

29.4 Usage Notes

29.4.1 Setting Module Stop Function

Module stop control register B (MSTPCRB) can be used to enable or disable the RSPI. Immediately after a reset, operation of the RSPI is disabled. Register access is enabled by releasing the module stop state. For details, refer to section 11, Low Power Consumption.

29.4.2 Note on Low Power Consumption Functions

When using the module stop function and entering a low power consumption mode other than sleep mode, set the SPCR.SPE bit to 0 before completing communication.

29.4.3 Notes on Starting Transfer

If the ICU.IRn.IR flag is 1 at the time transfer is to be started, an interrupt request is internally retained after transfer starts, and this can lead to unanticipated behavior of the ICU.IRn.IR flag.
When the ICU.IRn.IR flag is 1 at the time transfer is to start, follow the procedure below to clear interrupt requests before enabling operations (by setting the SPCR.SPE bit to 1).

1. Confirm that transfer has stopped (i.e. that the SPCR.SPE bit is 0).
2. Set the relevant interrupt enable bit (the SPCR.SPTIE or SPCR.SPRIE bit) to 0.
3. Read the relevant interrupt enable bit (the SPCR.SPTIE or SPCR.SPRIE bit) and confirm that its value is 0.
4. Set the ICU.IRn.IR flag to 0.

29.4.4 Notes on the SPRF and SPTEF flags

When polling the SPSR.SPRF flag and/or SPSR.SPTEF flag, set the SPCR.SPRIE bit and/or SPCR.SPTIE bit to 0.

30. CRC Calculator (CRC)

The CRC (Cyclic Redundancy Check) calculator generates CRC codes.

30.1 Overview

Table 30.1 lists the specifications of the CRC calculator, and Figure 30.1 shows a block diagram of the CRC calculator.

Table 30.1 CRC Specifications

Item	Description
Data for CRC calculation*1	CRC codes are generated for any desired data in 8n-bit units (where n is a whole number)
CRC processor unit	8-bit parallel processing
CRC generating polynomial	One of three generating polynomials is selectable • 8-bit CRC $X^8 + X^2 + X + 1$ • 16-bit CRC $X^{16} + X^{15} + X^2 + 1$ $X^{16} + X^{12} + X^5 + 1$
CRC calculation switching	The bit order of CRC calculation results can be switched for LSB first or MSB first communication
Low power consumption function	Module stop state can be set.

Note 1. The circuit does not have a function to divide data for calculation into CRC calculation units. Write data in 8-bit units.

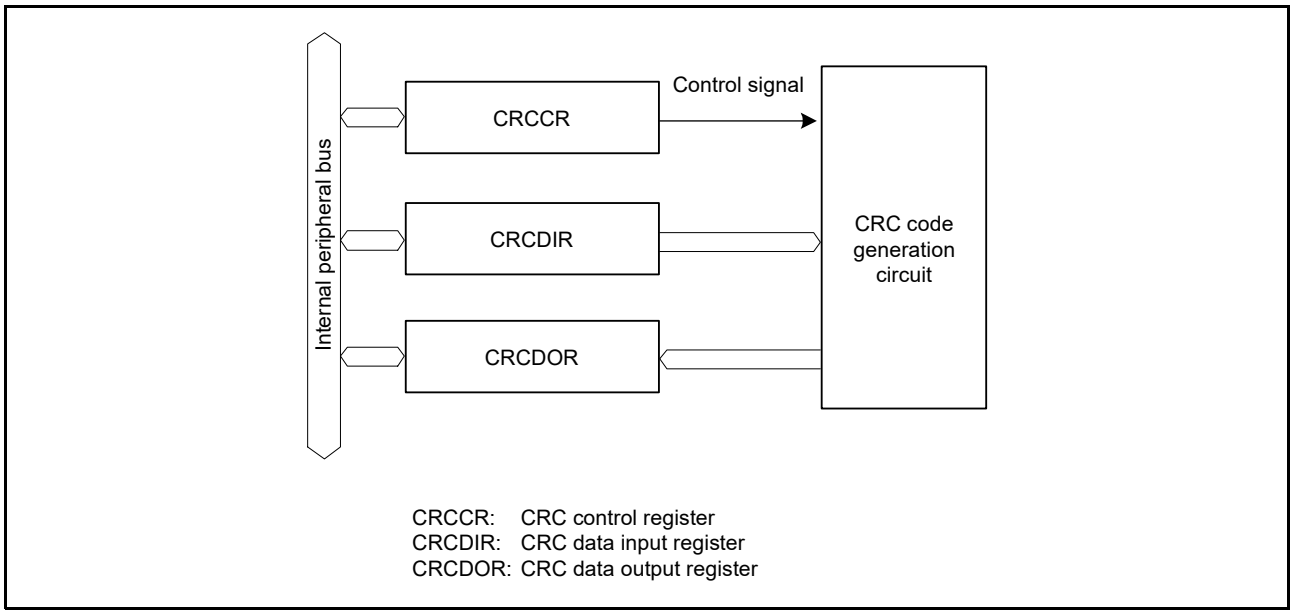


Figure 30.1 CRC Block Diagram

30.2 Register Descriptions

30.2.1 CRC Control Register (CRCCR)

Address(es): 0008 8280h

	b7	b6	b5	b4	b3	b2	b1	b0
	DORCLR	—	—	—	—	LMS	GPS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	GPS[1:0]	CRC Generating Polynomial Switching	b1 b0 0 0: No calculation is executed. 0 1: 8-bit CRC ($X^8 + X^2 + X + 1$) 1 0: 16-bit CRC ($X^{16} + X^{15} + X^2 + 1$) 1 1: 16-bit CRC ($X^{16} + X^{12} + X^5 + 1$)	R/W
b2	LMS	CRC Calculation Switching	0: Generates CRC for LSB first communication. 1: Generates CRC for MSB first communication.	R/W
b6 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	DORCLR	CRCDOR Register Clear	1: Clears the CRCDOR register. This bit is read as 0.	R/W*1

Note 1. Only 1 can be written.

LMS Bit (CRC Calculation Switching)

This bit selects the bit order of generated 16-bit CRC code. Transmit the lower-order byte (b7 to b0) of the CRC code first for LSB first communication and the higher-order byte (b15 to b8) first for MSB first communication. For details on the transmission and reception of CRC codes, refer to section 30.3, Operation.

DORCLR Bit (CRCDOR Register Clear)

Write 1 to this bit so that the CRCDOR register is set to 0000h.
This bit is read as 0. Only 1 can be written.

30.2.2 CRC Data Input Register (CRCDIR)

Address(es): 0008 8281h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0

CRCDIR is a readable and writable register. Write data for CRC calculation to this register.

30.2.3 CRC Data Output Register (CRCDOR)

Address(es): 0008 8282h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CRCDOR is a readable and writable register.
Since its initial value is 0000h, rewrite the CRCDOR register to perform calculation using a value other than the initial value.
Data written to the CRCDIR register is CRC calculated and the result is stored in the CRCDOR register. If the CRC code is calculated following the transferred data and the result is 0000h, there is no CRC error.
When an 8-bit CRC ($X^8 + X^2 + X + 1$ polynomial) is in use, the valid CRC code is obtained in the low-order byte (b7 to b0). The high-order byte (b15 to b8) is not updated.

30.3 Operation

The CRC calculator generates CRC codes for use in LSB first or MSB first transfer.
The following shows examples of generating the CRC code for input data (F0h) using the 16-bit CRC generating polynomial ($X^{16} + X^{12} + X^5 + 1$). In these examples, the value of the CRC data output register (CRCDOR) is cleared before CRC calculation.
When an 8-bit CRC (with the polynomial $X^8 + X^2 + X + 1$) is in use, the valid bits of the CRC code are obtained in the lower-order byte of the CRCDOR register.

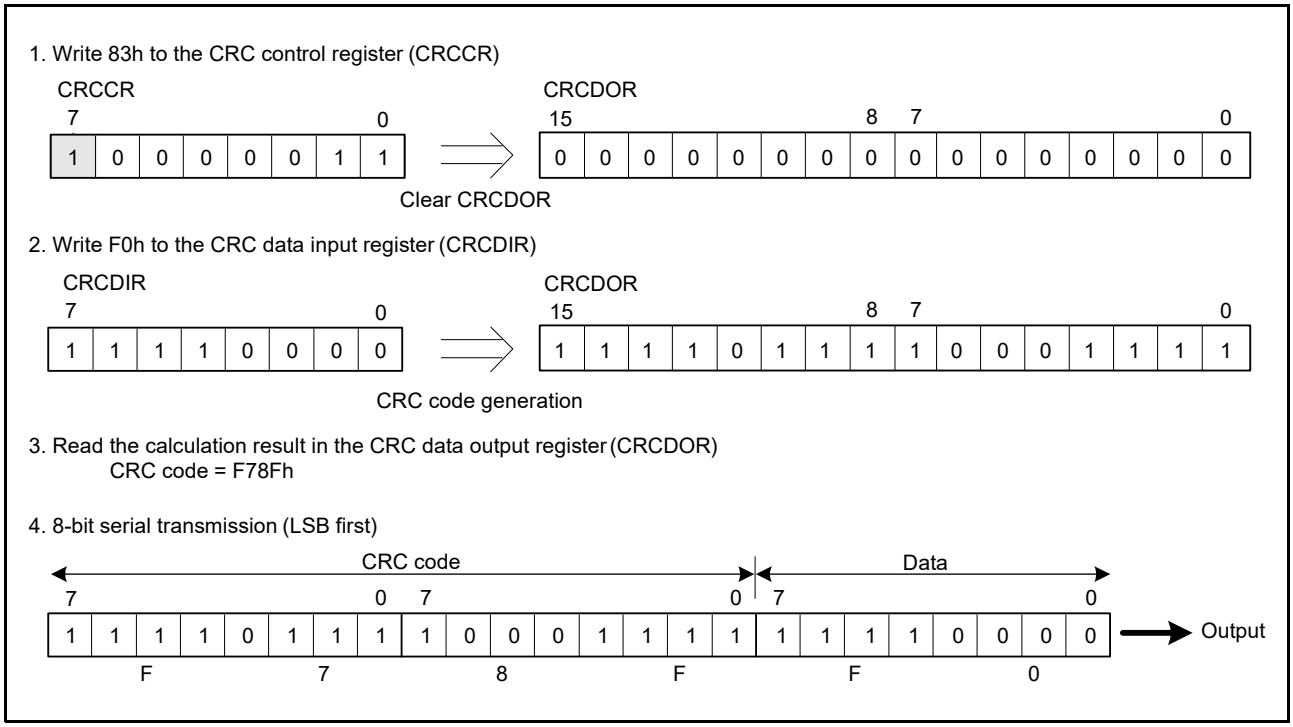


Figure 30.2 LSB First Data Transmission

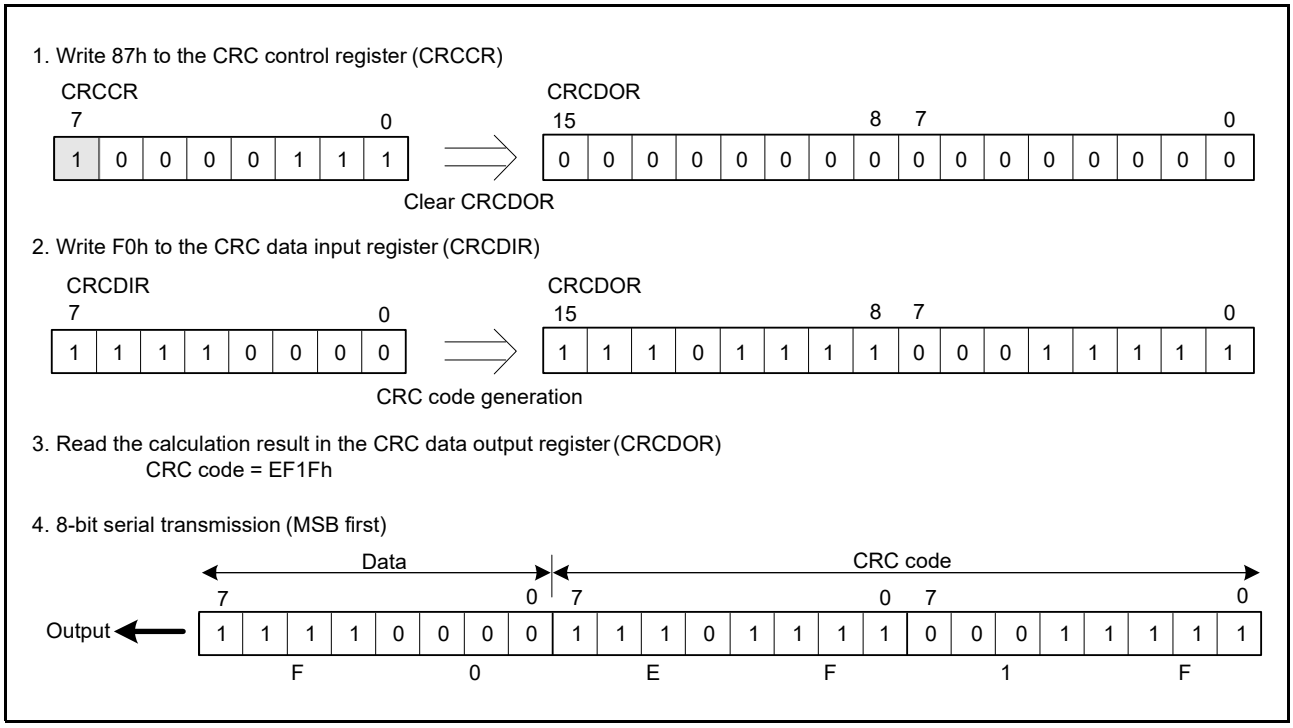


Figure 30.3 MSB First Data Transmission

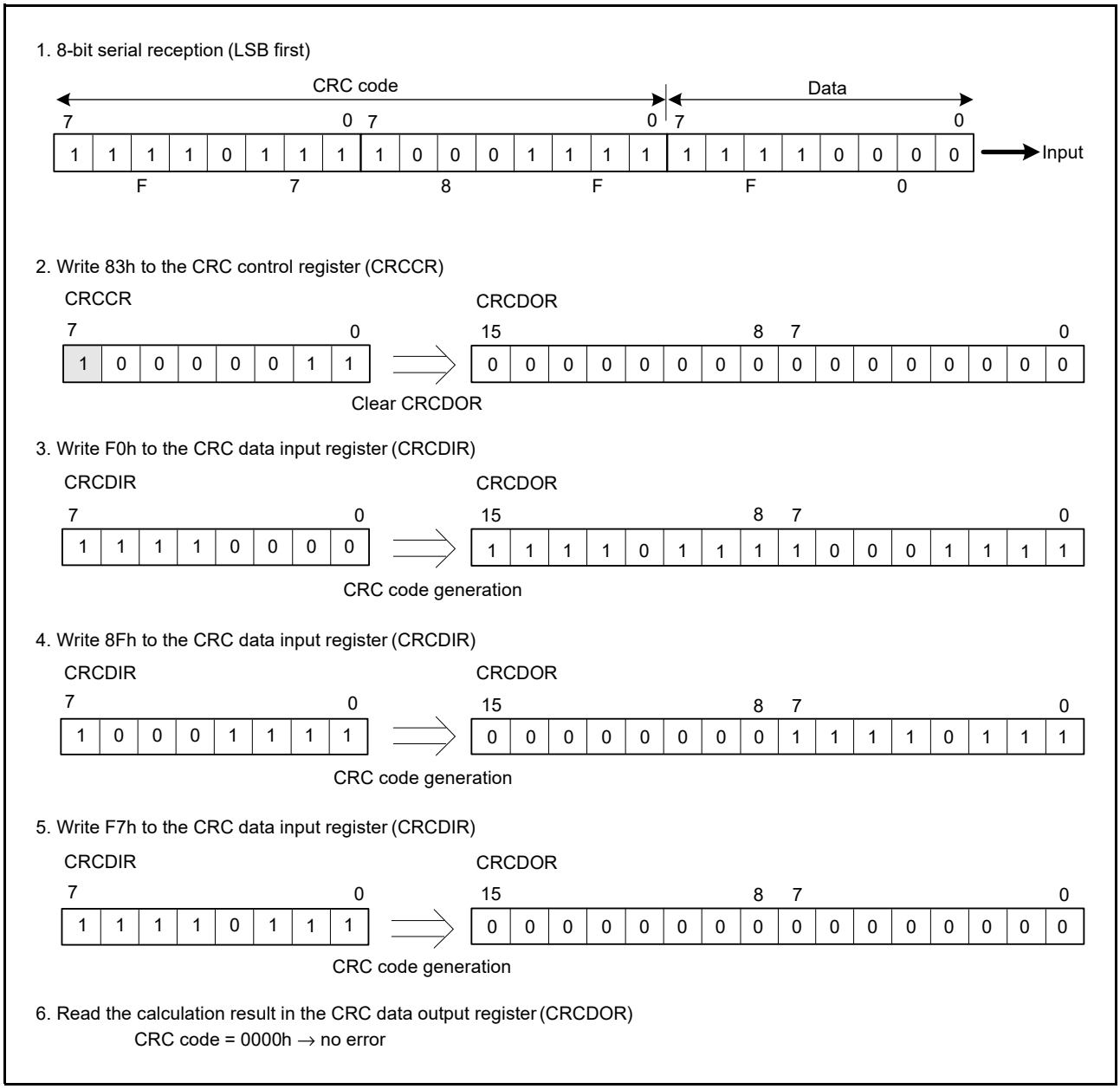


Figure 30.4 LSB First Data Reception

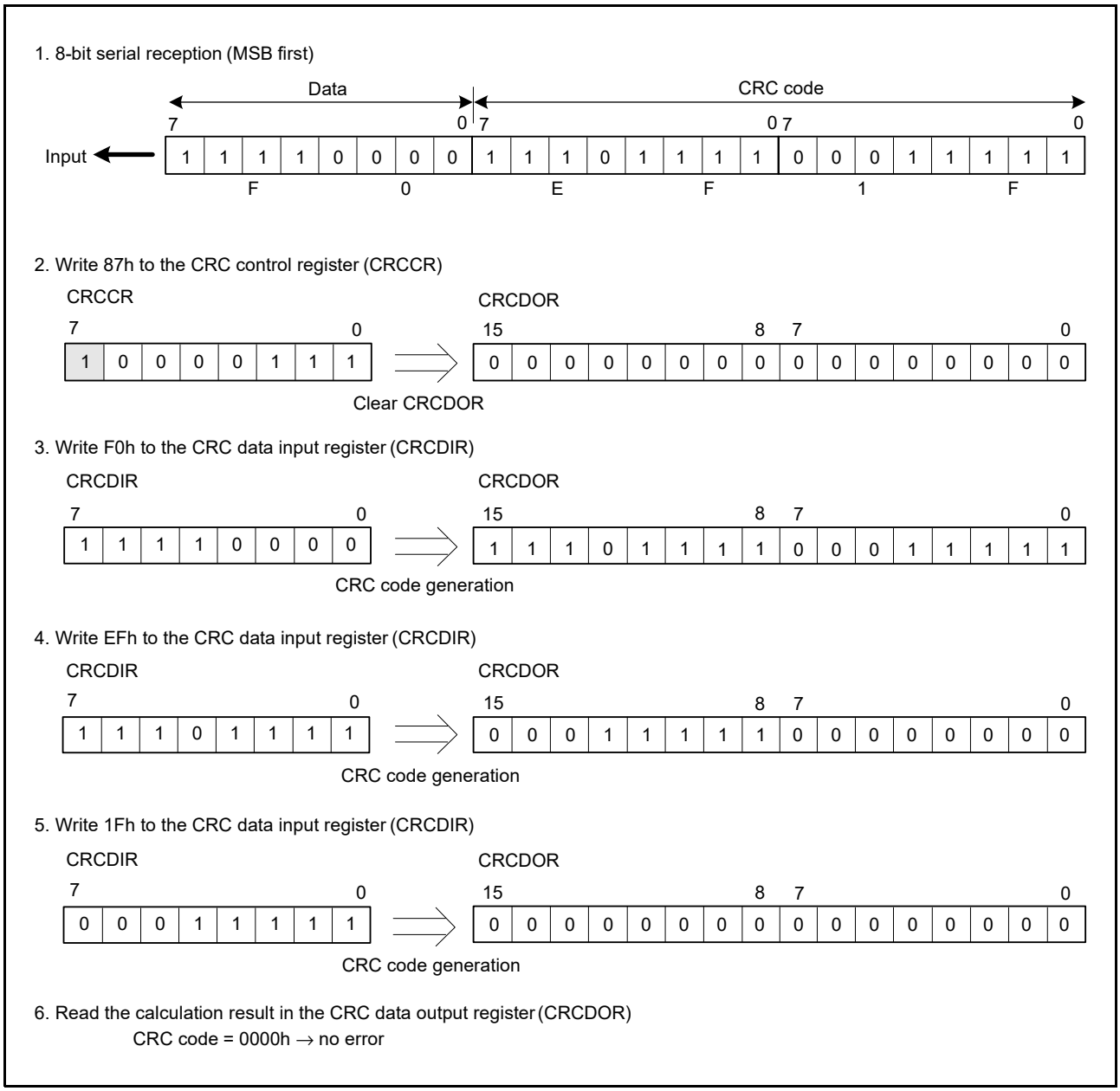


Figure 30.5 MSB First Data Reception

30.4 Usage Notes

30.4.1 Module Stop Function Setting

Operation of the CRC calculator can be disabled or enabled using the module stop control register B (MSTPCRB). After a reset, the CRC is in the module stop state. Register access is enabled by releasing the module stop state. For details, refer to section 11, Low Power Consumption.

30.4.2 Note on Transmission

Note that the sequence of transmission for the CRC code differs according to whether transmission is LSB first or MSB first.

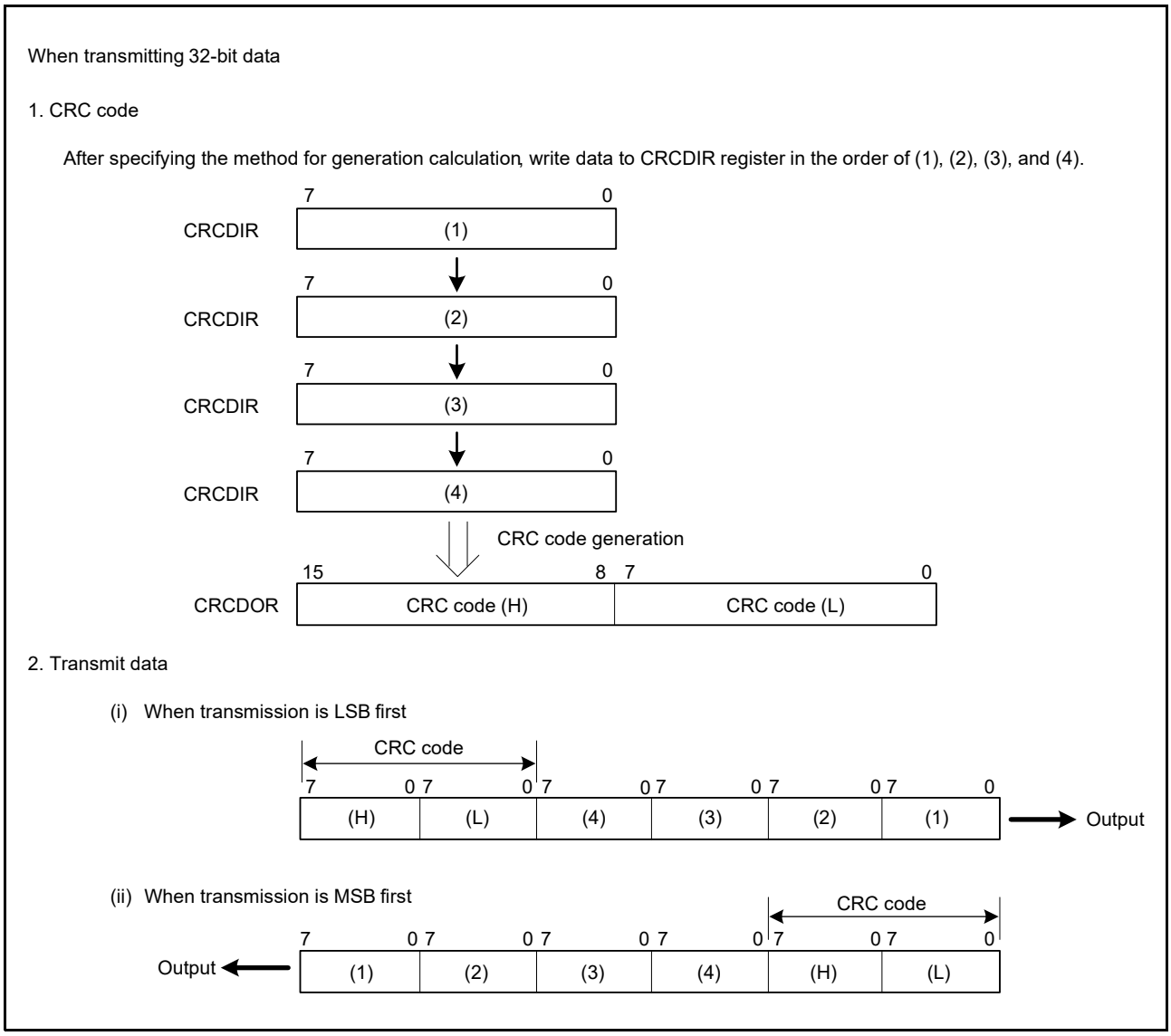


Figure 30.6 LSB First and MSB First Data Transmission

31. 12-Bit A/D Converter (S12ADF)

In this section, “PCLK” is used to refer to PCLKB.

31.1 Overview

This MCU incorporates three units of a 12-bit successive approximation A/D converter. There are two A/D converter units (units 0 and 1) that can use five channels, and one unit (unit 2) that can use 12 channels. Each unit can select analog input and only unit 2 can select internal reference voltage.

The 12-bit A/D converter converts a maximum of 12 selected channels of analog inputs and internal reference voltage (for unit 2 only), into a 12-bit digital value through successive approximation.

The A/D converter has three operating modes: single scan mode in which the analog inputs of five arbitrarily selected channels (units 0 and 1) and 12 channels (unit 2) are converted in ascending channel order; continuous scan mode in which the analog inputs of five arbitrarily selected channels (units 0 and 1) and 12 channels (unit 2) are continuously converted in ascending channel order; and group scan mode in which five arbitrarily selected channels (units 0 and 1) and 12 channels (unit 2) are arbitrarily divided into two groups (groups A and B) or three groups (groups A, B, and C) and converted in ascending channel order in each group.

In group scan mode, either two groups (groups A and B) or three groups (groups A, B, and C) is selected.

The conditions for scanning start of each group (A and B or A, B, and C) (synchronous trigger) can be independently selected, thus allowing A/D conversion of each group to be started independently.

In group scan mode, either two groups (groups A and B) or three groups (groups A, B, and C) is selected.

The conditions for scanning start of each group (A and B or A, B, and C) (synchronous trigger) can be independently selected, thus allowing A/D conversion of each group to be started independently.

During group priority operation, in addition to the above-mentioned operation, a trigger to start scanning for the priority group is accepted during scan for the low-priority group, and scan for the priority group is started after scan for the low-priority group was discontinued. The priority order is group A > group B > group C. Accordingly, as priority operation, when a trigger to start scanning for group B is accepted during scan for group C, group C scan is discontinued, and scan for group B is started. Likewise, when a trigger to start scanning for group A is accepted during scan for group C, group C scan is discontinued and scan for group A is started. In the same way, when a trigger to start scanning for group A is accepted during scan for group B, group B scan is discontinued and scan for group A is started. Note, however, that only the unit 2 can be selected from the internal reference voltage (VBG2AD).

The discontinued scan operation can be restarted after the scanning of the priority group is completed.

In double trigger mode, one analog input channel arbitrarily selected is converted in single scan mode or group scan mode (group A), and the resulting data of A/D conversion started by the first and second synchronous triggers are stored into different registers (duplication of A/D conversion data).

Self-diagnosis is executed once at the beginning of each scan, and one of the three voltages internally generated in the 12-bit A/D converter is converted.

Table 31.1 lists the specifications of the 12-bit A/D converter and Table 31.2 lists the functions of the 12-bit A/D converter. Figure 31.1 to Figure 31.3 show block diagrams of the 12-bit A/D converter.

Table 31.1 Specifications of 12-Bit A/D Converter (1/2)

Item	Description
Number of units	Three units (S12AD, S12AD1, and S12AD2)
Input channels	Five channels for S12AD, five channels for S12AD1, and 12 channels for S12AD2
Extended analog function	Internal reference voltage (S12AD2 only)
A/D conversion method	Successive approximation method
Resolution	12 bits
Conversion time	1 µs per channel (when A/D conversion clock ADCLK = 40 MHz)
A/D conversion clock	Peripheral module clock PCLK*1 and A/D conversion clock ADCLK*1 can be set so that the frequency ratio should be one of the following. PCLK to ADCLK frequency ratio = 1:1, 1:2, 2:1, 4:1, 8:1 ADCLK is set using the clock generation circuit.
Data registers	• 22 registers for analog input (five for S12AD, five for S12AD1, and 12 for S12AD2), 1 for A/D-converted data duplication in double trigger mode, and 2 for A/D-converted data duplication during extended operation in double trigger mode unit. • One register for internal reference (S12AD2) • One register for self-diagnosis per unit • The results of A/D conversion are stored in 12-bit A/D data registers. • 12-bit accuracy output for the results of A/D conversion • The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits*2 in the A/D data registers in A/D-converted value addition mode. • Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers): A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.
Operating modes	Operating modes can be set independently for three units. • Single scan mode: A/D conversion is performed only once on the analog inputs arbitrarily selected. A/D conversion is performed only once on the internal reference voltage (S12AD2). • Continuous scan mode: A/D conversion is performed repeatedly on the analog inputs arbitrarily selected. • Group scan mode: Two (groups A and B) or three (groups A, B, and C) can be selected as the number of the groups to be used. Only the combination of groups A and B can be selected when the number of the groups is two. Analog inputs arbitrarily selected are divided into two groups (group A and B) or three groups (group A, B, and C), and A/D conversion of the analog input selected on a group basis is performed only once. The conditions for scanning start of groups A, B, and C (synchronous trigger) can be independently selected, thus allowing A/D conversion of each group to be started independently. • Group scan mode (when group priority control selected): If a priority-group trigger is input during scanning of the low-priority group, scan of the low-priority group is stopped and scan of the priority group is started. The priority order is group A (highest) > group B > group C (lowest). Whether or not to restart scanning of the low-priority group after processing for the high-priority group completes, is selectable. Rescan can also be set to start either from the beginning of the selected channel or the channel on which A/D conversion is not completed.
Conditions for A/D conversion start	• Software trigger • Synchronous trigger Trigger by the multi-function timer pulse unit (MTU), general PWM timer (GPT), or 8-bit timer (TMR). • Asynchronous trigger A/D conversion can be triggered by the external trigger ADTRG0# (S12AD), ADTRG1# (S12AD1), or ADTRG2# (S12AD2) pin (independently for three units).

Table 31.1 Specifications of 12-Bit A/D Converter (2/2)

Item	Description
Functions	• Channel-dedicated sample-and-hold function (three channels for S12AD1 only) • Input signal amplification function of the programmable gain amplifier (1 channel for S12AD and 3 channels for S12AD1) • Variable sampling state count (settable for each channel) • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection assist function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Automatic clear function of A/D data registers
Interrupt sources	• In the modes except double trigger mode and group scan mode, a scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of single scan. (independently for three units). • In double trigger mode, a scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of double scan. (independently for three units). • In group scan mode, a scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of group A scan, whereas a scan end interrupt request (GBADI, GBADI1, or GBADI2) for group B can be generated on completion of group B scan, and a group C scan end interrupt request (GCADI, GCADI1, or GCADI2) can be generated on completion of group C scan. • When double trigger mode is selected in group scan mode, an A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of double scan of group A, and the corresponding scan end interrupt request (GBADI/GCADI, GBADI1/GCADI1, or GBADI2/GCADI2) can be generated on completion of group B and group C scan. • The S12ADI/S12ADI1/S12ADI2, GBADI/GBADI1/GBADI2, and GCADI/GCADI1/GCADI2 interrupts can activate the data transfer controller (DTC).
Low power consumption function	• Module stop state can be set.*3, *4

Note 1. The peripheral module clock PCLK frequency is set according to the setting of the SCKCR.PCKB[3:0] bits and the A/D conversion clock ADCLK frequency is set according to the setting of the SCKCR.PCKD[3:0] bits.
Note 2. The number of extended bits during addition differs depending on the addition count.
2-bit extension: 1-time to 4-time conversion (add zero to three times)
4-bit extension: 16-time conversion (add 15 times)
Note 3. See section 11, Low Power Consumption for details.
Note 4. Wait for 1 µs or longer to start A/D conversion after release from the module stop state.

Table 31.2 Functions of 12-Bit A/D Converter (1/2)

Item			Pin Name, Abbreviation		
			Unit 0 (S12AD)	Unit 1 (S12AD1)	Unit 2 (S12AD2)
Analog input channels			AN000 to AN003, AN016	AN100 to AN103, AN116	AN200 to AN211, internal reference voltage
Conditions for A/D conversion start	Software	Software trigger	Enabled		
	Asynchronous trigger	Trigger input pin	ADTRG0#	ADTRG1#	ADTRG2#
	Synchronous trigger	Compare match/input capture from MTU0.TGRA	TRGA0N		
		Compare match/input capture from MTU1.TGRA	TRGA1N		
		Compare match/input capture from MTU2.TGRA	TRGA2N		
		Compare match/input capture from MTU3.TGRA	TRGA3N		
		Compare match/input capture from MTU4.TGRA or underflow (trough) of MTU4.TCNT in complementary PWM mode	TRGA4N		
		Compare match/input capture from MTU6.TGRA	TRGA6N		
		Compare match/input capture from MTU7.TGRA or underflow (trough) of MTU7.TCNT in complementary PWM mode	TRGA7N		
		Compare match from MTU0.TGRE	TRG0N		
		Compare match between MTU4.TADCORA and MTU4.TCNT	TRG4AN		
		Compare match between MTU4.TADCORB and MTU4.TCNT	TRG4BN		
		Compare match between MTU4.TADCORA and MTU4.TCNT, or compare match between MTU4.TADCORB and MTU4.TCNT	TRG4AN or TRG4BN		
		Compare match between MTU4.TADCORA and MTU4.TCNT, and compare match between MTU4.TADCORB and MTU4.TCNT (when interrupt skipping function 2 is used)	TRG4ABN		
		Compare match between MTU7.TADCORA and MTU7.TCNT	TRG7AN		
		Compare match between MTU7.TADCORB and MTU7.TCNT	TRG7BN		
		Compare match between MTU7.TADCORA and MTU7.TCNT, or compare match between MTU7.TADCORB and MTU7.TCNT	TRG7AN or TRG7BN		
		Compare match between MTU7.TADCORA and MTU7.TCNT, and compare match between MTU7.TADCORB and MTU7.TCNT (when interrupt skipping function 2 is used)	TRG7ABN		
		Compare match/input capture from MTU9.TGRA	TRGA9N		
		Compare match from MTU9.TGRE	TRG9N		
		Compare match/input capture from MTU0.TGRA, or compare match from MTU0.TGRE	TRGA0N or TRG0N		
		Compare match/input capture from MTU9.TGRA, or compare match from MTU9.TGRE	TRGA9N or TRG9N		
		Compare match/input capture from MTU0.TGRA, or compare match/input capture from MTU9.TGRA.	TRGA0N or TRGA9N		
		Compare match from MTU0.TGRE, or compare match from MTU9.TGRE	TRG0N or TRG9N		
		Compare match between TMR0.TCORA and TMR0.TCNT	TMTRG0AN_0		
		Compare match between TMR2.TCORA and TMR2.TCNT	TMTRG0AN_1		
		Compare match between TMR4.TCORA and TMR4.TCNT	TMTRG0AN_2		
		Compare match between TMR6.TCORA and TMR6.TCNT	TMTRG0AN_3		

Table 31.2 Functions of 12-Bit A/D Converter (2/2)

Item			Pin Name, Abbreviation		
			Unit 0 (S12AD)	Unit 1 (S12AD1)	Unit 2 (S12AD2)
Conditions for A/D conversion start	Synchronous trigger	Compare match/input capture from MTU9.TGRA, and compare match from MTU9.TGRE.	TRG9AEN		
		Compare match/input capture from MTU0.TGRA, and compare match from MTU0.TGRE.	TRG0AEN		
		Compare match/input capture from MTU0.TGRA, and compare match/input capture from MTU9.TGRA.	TRGA09N		
		Compare match from MTU0.TGRE, and compare match from MTU9.TGRE.	TRG09N		
		Compare match with GPT0.GTADTRA	GTADTRA0N		
		Compare match with GPT0.GTADTRB	GTADTRB0N		
		Compare match with GPT1.GTADTRA	GTADTRA1N		
		Compare match with GPT1.GTADTRB	GTADTRB1N		
		Compare match with GPT2.GTADTRA	GTADTRA2N		
		Compare match with GPT2.GTADTRB	GTADTRB2N		
		Compare match with GPT3.GTADTRA	GTADTRA3N		
		Compare match with GPT3.GTADTRB	GTADTRB3N		
		Compare match with GPT0.GTADTRA or GPT0.GTADTRB	GTADTRA0N or GTADTRB0N		
		Compare match with GPT1.GTADTRA or GPT1.GTADTRB	GTADTRA1N or GTADTRB1N		
		Compare match with GPT2.GTADTRA or GPT2.GTADTRB	GTADTRA2N or GTADTRB2N		
		Compare match with GPT3.GTADTRA or GPT3.GTADTRB	GTADTRA3N or GTADTRB3N		
Channel-dedicated sample-and-hold function		Target channels	—	AN100 to AN102	—
PGA		Target channels	AN000	AN100 to AN102	—
Interrupts			S12ADI, GBADI, GCADI interrupt	S12ADI1, GBADI1, GCADI1 interrupt	S12ADI2, GBADI2, GCADI2 interrupt
Setting of module stop function*1, *2			MSTPCRA.MSTPA17 bit	MSTPCRA.MSTPA16 bit	MSTPCRA.MSTPA23 bit

Note: When setting an A/D conversion start trigger to ADTRG0#, ADTRG1#, or ADTRG2#, set the pin mode control bit in the port mode register for the corresponding pin to 1 (peripheral functions), and set the pin function select bit in the pin function control register to ADTRG0#, ADTRG1#, or ADTRG2#,. See section 18, I/O Ports for details.

Note 1. See section 11, Low Power Consumption for details.

Note 2. Wait for 1 µs or longer to start A/D conversion after release from the module stop state.

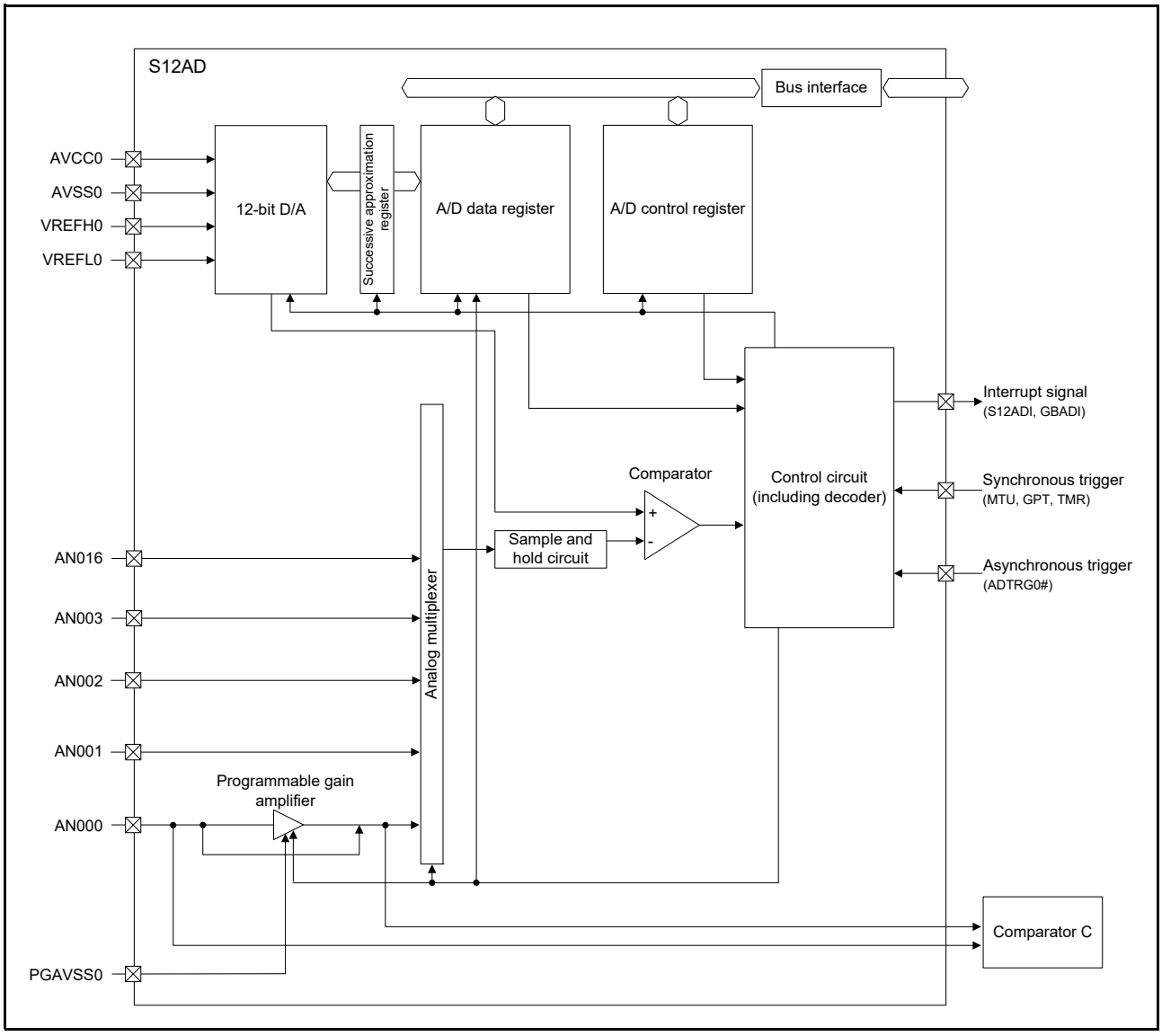


Figure 31.1 Block Diagram of 12-Bit A/D Converter (Unit 0)

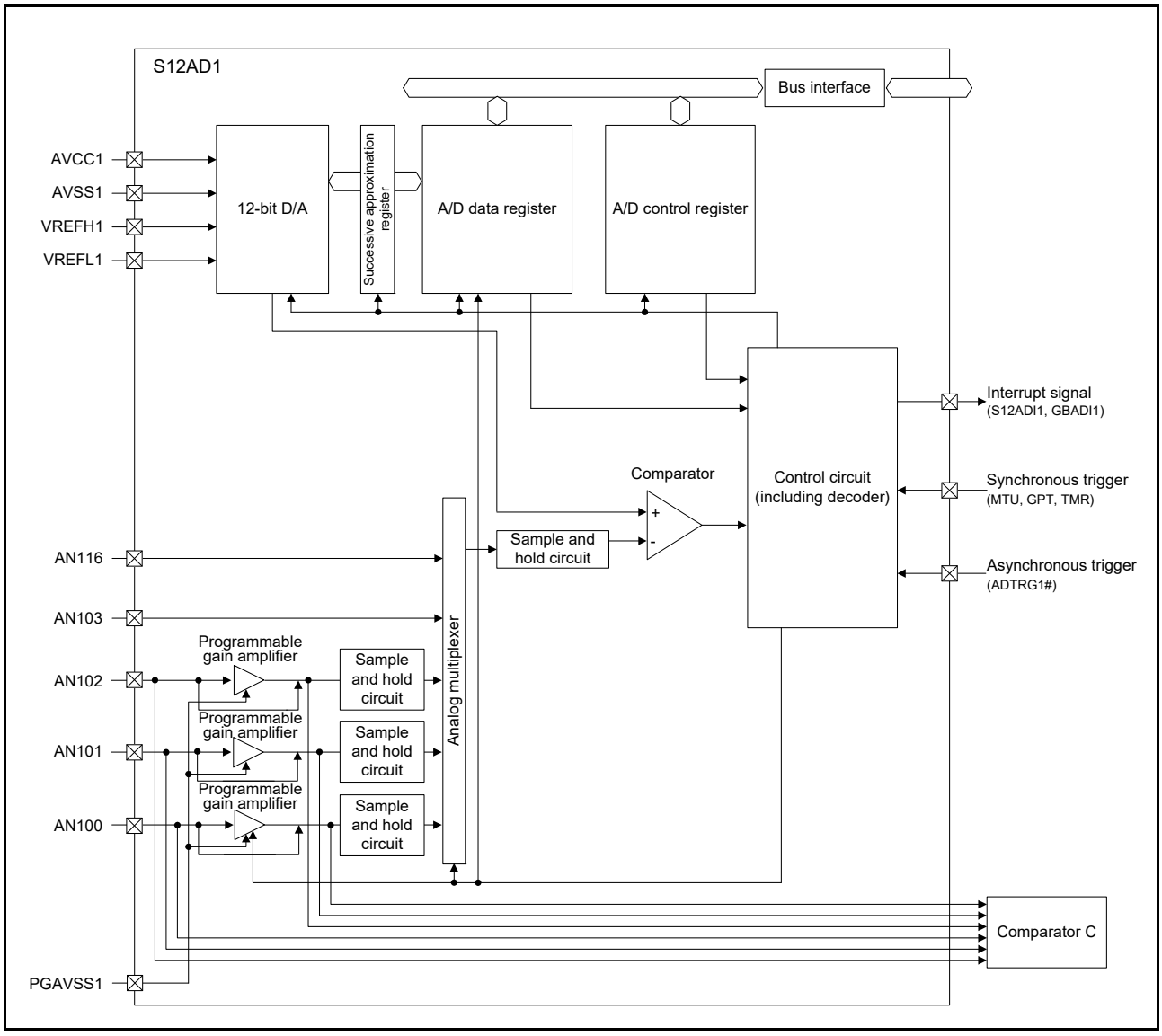


Figure 31.2 Block Diagram of 12-Bit A/D Converter (Unit 1)

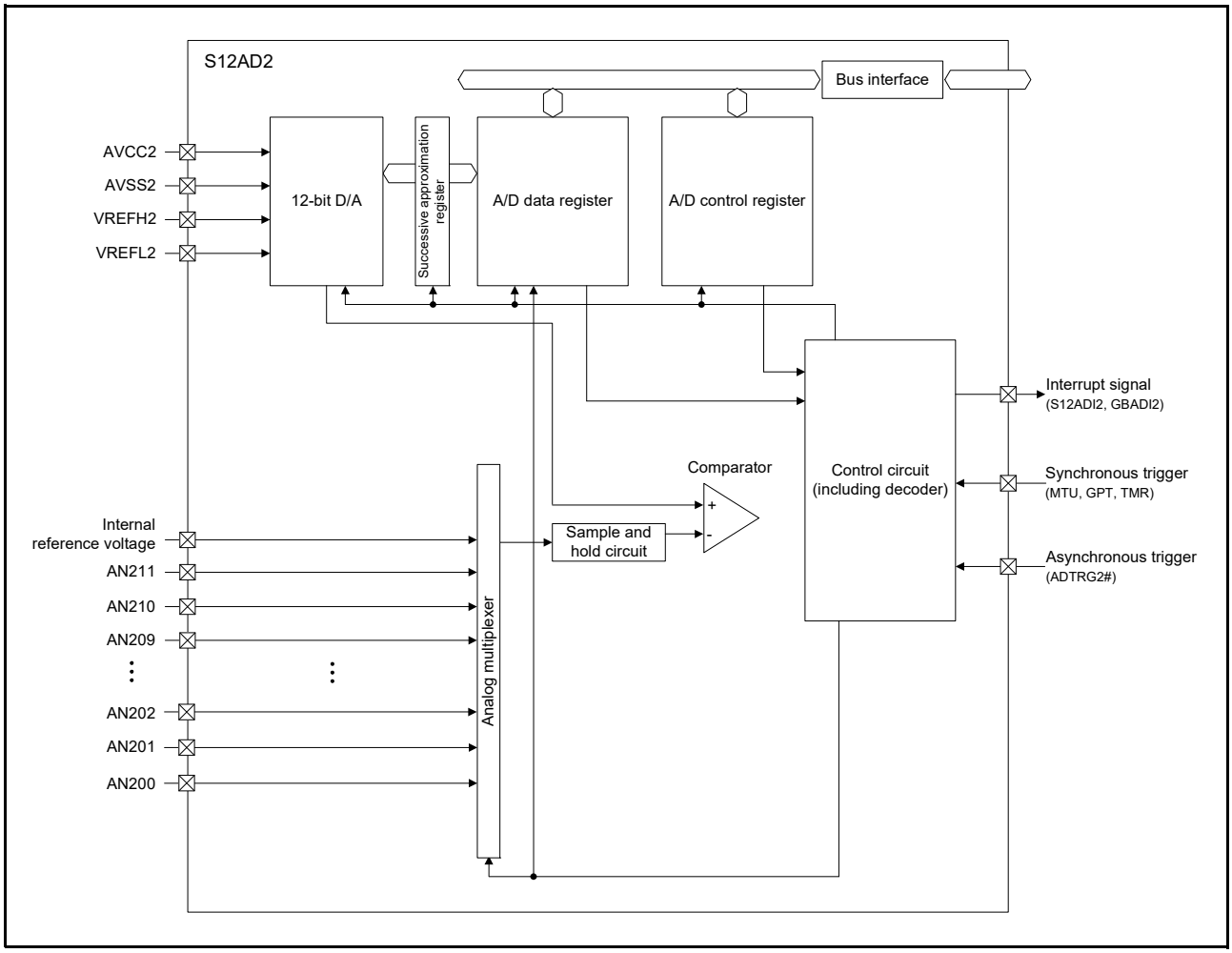


Figure 31.3 Block Diagram of 12-Bit A/D Converter (Unit 2)

Table 31.3 lists the input/output pins of the 12-bit A/D converter.

The 12-bit A/D converter consists of three units, unit 0 (S12AD), unit 1 (S12AD1), and unit 2 (S12AD2). These units can be operated independently. The input channels of S12AD, S12AD1, and S12AD2 can be divided into three groups for operation. A programmable gain amplifier (PGA) is included in AN000 and AN100 to AN102.

Table 31.3 Input/Output Pins of 12-Bit A/D Converter (1/2)

Unit	Pin Name	I/O	Function	PGA	Internal Sample & Hold Circuit for the Pin
Unit 0 (S12AD)	AN000	Input	Analog input pin	Incorporated	—
	AN001	Input	Analog input pin	—	—
	AN002	Input	Analog input pin	—	—
	AN003	Input	Analog input pin	—	—
	AN016	Input	Analog input pin	—	—
	ADTRG0#	Input	External trigger input pin for starting A/D conversion	—	—
	ADST0	Output	ADST bit state output pin	—	—
	AVCC0	—	Analog block power supply pin	—	—
	AVSS0	—	Analog block ground pin	—	—
	VREFH0	—	Reference power supply pin	—	—
	VREFL0	—	Reference power supply ground pin	—	—
	PGAVSS0	Input	PGA gain setting resistor reference ground pin (AN000)	—	—
Unit 1 (S12AD1)	AN100	Input	Analog input pin	Incorporated	Incorporated
	AN101	Input	Analog input pin	Incorporated	Incorporated
	AN102	Input	Analog input pin	Incorporated	Incorporated
	AN103	Input	Analog input pin	—	—
	AN116	Input	Analog input pin	—	—
	ADTRG1#	Input	External trigger input pin for starting A/D conversion	—	—
	ADST1	Output	ADST bit state output pin	—	—
	AVCC1	—	Analog block power supply pin	—	—
	AVSS1	—	Analog block ground pin	—	—
	VREFH1	—	Reference power supply pin	—	—
	VREFL1	—	Reference power supply ground pin	—	—
	PGAVSS1	Input	PGA gain setting resistor reference ground pin (AN100 to AN102)	—	—

Table 31.3 Input/Output Pins of 12-Bit A/D Converter (2/2)

Unit	Pin Name	I/O	Function	PGA	Internal Sample & Hold Circuit for the Pin
Unit 2 (S12AD2)	AN200	Input	Analog input pin	—	—
	AN201	Input	Analog input pin	—	—
	AN202	Input	Analog input pin	—	—
	AN203	Input	Analog input pin	—	—
	AN204	Input	Analog input pin	—	—
	AN205	Input	Analog input pin	—	—
	AN206	Input	Analog input pin	—	—
	AN207	Input	Analog input pin	—	—
	AN208	Input	Analog input pin	—	—
	AN209	Input	Analog input pin	—	—
	AN210	Input	Analog input pin	—	—
	AN211	Input	Analog input pin	—	—
	ADTRG2#	Input	External trigger input pin for starting A/D conversion	—	—
	ADST2	Output	ADST bit state output pin	—	—
	AVCC2	—	Analog block power supply pin	—	—
	AVSS2	—	Analog block ground pin	—	—
	VREFH2	—	Reference power supply pin	—	—
	VREFL2	—	Reference power supply ground pin	—	—

31.2 Register Descriptions

31.2.1 A/D Data Registers y (ADDRy)
A/D Data Duplication Register (ADDBLDR)
A/D Data Duplication Register A (ADDBLDRA)
A/D Data Duplication Register B (ADDBLDRB)
A/D Internal Reference Voltage Data Register (ADOCDR)

Address(es): S12AD.ADDR0 0008 9020h, S12AD.ADDR1 0008 9022h, S12AD.ADDR2 0008 9024h, S12AD.ADDR3 0008 9026h, S12AD.ADDR16 0008 9040h, S12AD.ADDBLDR 0008 9018h, S12AD.ADDBLDRA 0008 9084h, S12AD.ADDBLDRB 0008 9086h, S12AD1.ADDR0 0008 9220h, S12AD1.ADDR1 0008 9222h, S12AD1.ADDR2 0008 9224h, S12AD1.ADDR3 0008 9226h, S12AD1.ADDR16 0008 9240h, S12AD1.ADDBLDR 0008 9218h, S12AD1.ADDBLDRA 0008 9284h, S12AD1.ADDBLDRB 0008 9286h, S12AD2.ADDR0 0008 9420h, S12AD2.ADDR1 0008 9422h, S12AD2.ADDR2 0008 9424h, S12AD2.ADDR3 0008 9426h, S12AD2.ADDR4 0008 9428h, S12AD2.ADDR5 0008 942Ah, S12AD2.ADDR6 0008 942Ch, S12AD2.ADDR7 0008 942Eh, S12AD2.ADDR8 0008 9430h, S12AD2.ADDR9 0008 9432h, S12AD2.ADDR10 0008 9434h, S12AD2.ADDR11 0008 9436h, S12AD2.ADDBLDR 0008 9418h, S12AD2.ADDBLDRA 0008 9484h, S12AD2.ADDBLDRB 0008 9486h, S12AD2.ADOCDR 0008 941Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The ADDRy registers (y = 0 to 3, 16 for S12AD and S12AD1; y = 0 to 11 for S12AD2) are 16-bit read-only registers which store the A/D conversion results.
The ADDBLDR register is a 16-bit read-only register used in double trigger mode. The ADDBLDR register stores the results of A/D conversion when the conversion is started by the second trigger.
The ADDBLDRA and ADDBLDRB registers are 16-bit read-only registers that store the A/D conversion results in response to the respective triggers during extended operation in double trigger mode.
The ADOCDR register is a 16-bit read-only register that stores the A/D conversion results of the internal reference voltage.
The format of each register differs depending on the conditions below.

- Settings of the A/D data register format select bit (ADCER.ADRFMT) (flush-right or flush-left)
- Settings of the addition count select bits (ADADC.ADC[2:0]) (2-, 3-, 4-, or 16-time conversion)
- Settings of the average mode enable bit (ADADC.AVEE) (add or average)

The data formats for each given condition are shown below.

(1) When A/D-Converted Value Addition/Average Mode is Not Selected

- Flush-right format
  The A/D-converted value is stored in bits 11 to 0. Bits 15 to 12 are read as 0.
- Flush-left format
  The A/D-converted value is stored in bits 15 to 4. Bits 3 to 0 are read as 0.

(2) When A/D-Converted Average Mode is Selected

- Flush-right format
  The mean value of the A/D-converted results of the same channel is stored in bits 11 to 0.
  Bits 15 to 12 are read as 0.
- Flush-left format
  The mean value of the A/D-converted results of the same channel is stored in bits 15 to 4.
  Bits 3 to 0 are read as 0.

A/D-converted value average mode can be set only when 2- or 4-time conversion is selected in A/D-converted value addition mode.

(3) When A/D-Converted Value Addition Mode is Selected

- Flush-right format (in A/D-converted value addition mode and when number of conversions is selected for 1 to 4 times)
  The value added by the A/D-converted value of the same channel is stored in bits 13 to 0.
  Bits 15 and 14 are read as 0.
- Flush-right format (in A/D-converted value addition mode and when number of conversions is selected for 16 times)
  The value added by the A/D-converted value of the same channel is stored in bits 15 to 0.
- Flush-left format (in A/D-converted value addition mode and when number of conversions is selected for 1 to 4 times)
  The value added by the A/D-converted value of the same channel is stored in bits 15 to 2.
  Bits 1 and 0 are read as 0.
- Flush-left format (in A/D-converted value addition mode and when number of conversions is selected for 16 times)
  The value added by the A/D-converted value of the same channel is stored in bits 15 to 0.

When A/D-converted addition mode is selected, the value added by the A/D-converted value of the same channel is indicated. The number of A/D conversions can be set to 1, 2, 3, 4, or 16 times. If A/D-converted addition mode is selected, when the conversion count is set to 1 to 4 times, the value added by the A/D conversion result is retained in the A/D data register as 2-bit extended data of the conversion accuracy bits; when the conversion count is set to 16 times, the value added by the A/D conversion result is retained in the A/D data register as 4-bit extended data of the conversion accuracy bits. Even if A/D-converted value addition mode is selected, the value is stored in the A/D data register according to the settings of the A/D data register format select bits.

31.2.2 A/D Self-Diagnosis Data Register (ADRD)

Address(es): S12AD.ADRD 0008 901Eh, S12AD1.ADRD 0008 921Eh, S12AD2.ADRD 0008 941Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ADRD is a 16-bit read-only register that stores the A/D conversion results based on the 12-bit A/D converter's self-diagnosis. In addition to the A/D-converted value, the self-diagnosis status is included in. In the ADRD register, the different formats are used depending on the conditions below.

- Settings of the A/D data register format select bit (ADCER.ADRFMT) (flush-right or flush-left)

The A/D-converted value addition mode and A/D-converted value average mode cannot be applied to the A/D self-diagnosis function. For details of self-diagnosis, see section 31.2.13, A/D Control Extended Register (ADCER).

The data formats for each given condition are shown below.

- Flush-right format
  The A/D-converted value is stored in bits 11 to 0. The self-diagnosis status is stored in bits 15 and 14.
  Bits 13 and 12 are read as 0.
- Flush-left format
  The A/D-converted value is stored in bits 15 to 4. The self-diagnosis status is stored in bits 1 and 0.
  Bits 3 and 2 are read as 0.

Table 31.4 Self-Diagnosis Status Description

Bits 15 and 14 for flush-right format setting Bits 1 and 0 for flush-left format setting	Self-diagnosis status
00b	Self-diagnosis has never been executed since power-on.
01b	Self-diagnosis using the voltage of 0 V has been executed.
10b	Self-diagnosis using the voltage of reference power supply × 1/2 has been executed.
11b	Self-diagnosis using the voltage of reference power supply has been executed.

Note: For details of self-diagnosis, see section 31.2.13, A/D Control Extended Register (ADCER).

31.2.3 A/D Control Register (ADCSR)

Address(es): S12AD.ADCSR 0008 9000h, S12AD1. ADCSR 0008 9200h, S12AD2. ADCSR 0008 9400h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ADST	ADCS[1:0]		ADIE	—	—	TRGE	EXTRG	DBLE	GBADIE	—	DBLANS[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	DBLANS[4:0]	Double Trigger Channel Select	These bits select one analog input channel for double triggered operation. The setting is only effective while double trigger mode is selected.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	GBADIE	Group B Scan End Interrupt Enable	0: Disables interrupt generation upon group B scan completion. 1: Enables interrupt generation upon group B scan completion.	R/W
b7	DBLE	Double Trigger Mode Select	0: Deselects double trigger mode. 1: Selects double trigger mode.	R/W
b8	EXTRG	Trigger Select*1	0: A/D conversion is started by synchronous trigger. 1: A/D conversion is started by asynchronous trigger.	R/W
b9	TRGE	Trigger Start Enable	0: Disables A/D conversion to be started by synchronous or asynchronous trigger. 1: Enables A/D conversion to be started by synchronous or asynchronous trigger.	R/W
b11, b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12	ADIE	Scan End Interrupt Enable	0: Disables interrupt generation upon scan completion. 1: Enables interrupt generation upon scan completion.	R/W
b14, b13	ADCS[1:0]	Scan Mode Select	b14 b13 0 0: Single scan mode 0 1: Group scan mode 1 0: Continuous scan mode 1 1: Setting prohibited	R/W
b15	ADST	A/D Conversion Start	0: Stops A/D conversion process. 1: Starts A/D conversion process.	R/W

Note 1. Starting A/D conversion using an external pin (asynchronous trigger)
Set the ADCSR.TRGE and EXTRG bits to 1 while a high-level signal is input to the external pin (ADTRG0#, ADTRG1#, or ADTRG2#). Then, if the ADTRG0#, ADTRG1#, or ADTRG2# signal is changed to low, the falling edge is detected and the scan process is started. In this case, the pulse width of the low-level input must be at least 1.5 clock cycles of PCLK.
The relationship between each unit and the external pin (asynchronous trigger) is shown below.

Unit	External pin (asynchronous trigger)
S12AD	ADTRG0#
S12AD1	ADTRG1#
S12AD2	ADTRG2#

ADCSR sets double trigger mode, A/D conversion start trigger; enables/disables scan end interrupt; selects the scan mode; and starts or stops A/D conversion.

DBLANS[4:0] Bits (Double Trigger Channel Select)

The DBLANS[4:0] bits select one of the channels for A/D conversion data duplication in double trigger mode. The A/D conversion results of the analog input of the channel selected by the DBLANS[4:0] bits are stored into the A/D data register y when conversion is started by the first trigger, and into the A/D data duplication register when started by the second trigger. Table 31.5 shows selection of the channel for double triggered operation.
When double trigger mode is selected, the channels selected by the ADANSA0 and ADANSA1 registers are invalid, and the channel selected by the DBLANS[4:0] bits is subjected to A/D conversion instead.

When double trigger mode is selected in group scan mode, double trigger mode operation is performed for group A only and not performed for group B or C. Also, in double trigger mode, the analog inputs of multiple channels and internal reference voltage cannot be selected for group A, but can be selected for groups B and C. However, the internal reference voltage can be selected for S12AD2 only.
The DBLANS[4:0] bits should be set while the ADST bit is 0. They should not be set simultaneously when 1 is written to the ADST bit.

Table 31.5 Relationship between DBLANS[4:0] Bits Settings and Double Trigger Enabled Channels

S12AD (Unit 0)		S12AD1 (Unit 1)		S12AD2 (Unit 2)	
DBLANS[4:0]	Duplication Channel	DBLANS[4:0]	Duplication Channel	DBLANS[4:0]	Duplication Channel
00000b	AN000	00000b	AN100	00000b	AN200
00001b	AN001	00001b	AN101	00001b	AN201
00010b	AN002	00010b	AN102	00010b	AN202
00011b	AN003	00011b	AN103	00011b	AN203
10000b	AN016	10000b	AN116	00100b	AN204
				00101b	AN205
				00110b	AN206
				00111b	AN207
				01000b	AN208
				01001b	AN209
				01010b	AN210
				01011b	AN211

Note: Duplication cannot be selected for the A/D conversion data of self-diagnosis and internal reference voltage.

GBADIE Bit (Group B Scan End Interrupt Enable)

The GBADIE bit enables or disables group B scan end interrupt in group scan mode.
A scan end interrupt for group B is provided individually for each unit. Table 31.6 shows the relationship between each unit and the scan end interrupt for group B.

Table 31.6 Relationship between Each Unit and Group B Scan End Interrupt

Unit	Group B Scan End Interrupt
S12AD	GBADI
S12AD1	GBADI1
S12AD2	GBADI2

DBLE Bit (Double Trigger Mode Select)

Double trigger mode has a function to store the resulting data of A/D conversion started by the first and second synchronous triggers into separate registers.
When double trigger mode is selected, the channels specified in the ADANSA0 and ADANSA1 registers are invalid and the channel selected by the DBLANS[4:0] bits is effective instead. Double trigger mode can be only operated by the synchronous trigger selected by the ADSTRGR.TRSA[5:0] bits. Do not generate an asynchronous or software trigger.
The A/D conversion results started by the first trigger are stored into the A/D data register y and those started by the second trigger are stored into the A/D data duplication register. In this case, if the ADIE bit is set to 1, the interrupt is generated not upon completion of the first conversion but upon completion of the second conversion.
In continuous scan mode, double trigger mode should not be selected. In addition, double trigger mode should not be used for self-diagnosis or conversion of the internal reference voltage. When using double trigger mode in group scan mode, A/D conversion of the internal reference voltage should not be selected for group A.
The DBLE bit should be set after the ADST bit has been set to 0.

EXTRG Bit (Trigger Select)

The EXTRG bit selects the synchronous trigger or the asynchronous trigger as the trigger for starting A/D conversion.
In group scan mode, the setting of this bit is valid for the selected trigger of group A.
For groups B and C, A/D conversion is started by the selected synchronous trigger regardless of this bit setting.

TRGE Bit (Trigger Start Enable)

The TRGE bit enables or disables A/D conversion by the synchronous trigger and the asynchronous trigger.
This bit should be set to 1 in group scan mode.

ADIE Bit (Scan End Interrupt Enable)

The ADIE bit enables or disables the A/D scan end interrupt (S12ADI) in scans except for groups B and C scan in group scan mode.
With double trigger mode deselected, the A/D scan conversion end is generated after the first scan is completed if the ADIE bit is set to 1.
With double trigger mode selected, the A/D scan conversion end is generated after the second scan is completed if the ADIE bit is set to 1 as long as the scan is started by the synchronous trigger selected by the ADSTRGR.TRSA[5:0] bits.
When scan is started by a software trigger, even with double trigger mode selected, the A/D scan conversion end interrupt is generated if the ADIE bit is set to 1 when the scan is completed. The A/D scan conversion end interrupt is provided individually for each unit. Table 31.7 shows the relationship between each unit and the A/D scan conversion end interrupt.

Table 31.7 Relationship between Each Unit and A/D scan conversion end Interrupt

Unit	A/D scan conversion end interrupt
S12AD	S12ADI
S12AD1	S12ADI1
S12AD2	S12ADI2

ADCS[1:0] Bits (Scan Mode Select)

The ADCS[1:0] bits select the scan mode.
In single scan mode, A/D conversion is performed for the analog inputs selected with the ADANSA0 and ADANSA1 registers in the ascending order of the channel number, and when one cycle of A/D conversion is completed for all the selected channels, the scan conversion is stopped.
In continuous scan mode, while the ADCSR.ADST bit is 1, A/D conversion is performed for the analog inputs selected with the ADANSA0 and ADANSA1 registers in the ascending order of the channel number, and when one cycle of A/D conversion is completed for all the selected channels, A/D conversion is repeated from the first channel. If the ADCSR.ADST bit is set to 0 during continuous scan, A/D conversion is stopped even if scanning is in progress.
In group scan mode, A/D conversion is performed for the analog inputs (group A) selected with the ADANSA0 and ADANSA1 registers in the ascending order of the channel number after scanning is started by the synchronous trigger selected by the ADSTRGR.TRSA[5:0] bits, and when one cycle of A/D conversion is completed for all the selected channels, A/D conversion is stopped. A/D conversion is also performed for the analog inputs (group B or C) selected with the ADANSB0 and ADANSB1 registers and the ADANSC0 and ADANSC1 registers in the ascending order of the channel number after A/D conversion is started by the synchronous trigger selected by the ADSTRGR.TRSB[5:0] bits and ADGCTRGR.TRSC[5:0] bits, and when A/D conversion is completed for all the selected channels, A/D conversion is stopped.
When selecting group scan mode, different channels and triggers should be selected for groups A, B, and C.
When using two groups while group scan mode is set, use groups A and B (ADGCTRGR.GRCE bit = 0). When using three groups, use groups A, B, and C (ADGCTRGR.GRCE bit = 1).
When selecting the internal reference voltage for S12AD2, select single scan mode, and deselect all the channels selected with the ADANSA0 and ADANSA1 registers before performing A/D conversion. When A/D conversion of the selected

internal reference voltage is completed, A/D conversion is stopped.
The ADCS[1:0] bits should be set while the ADST bit is 0. They should not be set simultaneously when 1 is written to the ADST bit.

ADST Bit (A/D Conversion Start)

The ADST bit starts or stops A/D conversion process.
Before the ADST bit is set to 1, set the A/D conversion clock, the conversion mode, and conversion target analog input.
[Setting conditions]

- 1 is written by software.
- The synchronous trigger selected by the ADSTRGR.TRSA[5:0] bits is detected with ADCSR.EXTRG and ADCSR.TRGE bits being set to 0 and 1, respectively.
- The synchronous trigger selected by the ADSTRGR.TRSB[5:0] bits is detected with the ADCSR.TRGE bit being set to 1 in group scan mode.
- The asynchronous trigger is detected with the ADCSR.TRGE and ADCSR.EXTRG bits being set to 1 and the ADSTRGR.TRSA[5:0] bits being set to 000000b.
- With group priority control operation mode enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1), a group B or C trigger is detected and A/D conversion of group B or C is started.
- With group priority control operation mode enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1), the ADGSPCR.GBRSCN bit is set to 1 and A/D conversion of group B or C is restarted.
- With group priority control operation mode enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1), the ADGSPCR.GBRP bit is set to 1 and A/D conversion of the lowest-priority group is started.

[Clearing conditions]

- 0 is written by software.
- The A/D conversion of all the selected channels or the internal reference voltage (for S12AD2 only) is completed in single scan mode.
- Group A scan is completed in group scan mode.
- Group B scan is completed in group scan mode.
- Group C scan is completed in group scan mode.
- With group priority control operation mode enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1), the ADGSPCR.GBRSCN bit is set to 1 and the scanning of the low-priority group started by a trigger is stopped.

Note: When group priority control operation mode has been enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1), do not set the ADST bit to 1.
Note: When group priority control operation mode has been enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1) and ADGSPCR.GBRP = 1, do not set the ADST bit to 0. When forcibly terminating A/D conversion, follow the procedure for clearing the ADST bit.
Note: When the single-scan continuous function is used (ADGSPCR.GBRP bit = 1) with group priority control operation mode enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1), the ADST bit remains as 1.

31.2.4 A/D Channel Select Register A0 (ADANSA0)

(1) S12AD.ADANSA0

Address(es): 0008 9004h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	ANSA003	ANSA002	ANSA001	ANSA000
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ANSA000	A/D Conversion Channel Select	0: AN000 to AN003 are not subjected to conversion. 1: AN000 to AN003 are subjected to conversion.	R/W
b1	ANSA001			R/W
b2	ANSA002			R/W
b3	ANSA003			R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

S12AD.ADANSA0 selects analog input channels for A/D conversion from among AN000 to AN003. In group scan mode, this register selects group A channels.

ANSA0n Bit (n = 00 to 03) (A/D Conversion Channel Select)

The ANSA0n bit select analog input channels for A/D conversion from among AN000 to AN003. The channels to be selected and the number of channels can be arbitrarily set. The ANSA000 bit corresponds to AN000 and the ANSA003 bit corresponds to AN003.

When double trigger mode is selected, the channel selected by S12AD.ADCSR.DBLANS[4:0] bits is selected in group A, and the ANSA0n bit setting is invalid.

The ANSA0n bit should be set while the S12AD.ADCSR.ADST bit is 0.

(2) S12AD1.ADANSA0

Address(es): 0008 9204h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	ANSA003	ANSA002	ANSA001	ANSA000
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ANSA000	A/D Conversion Channel Select	0: AN100 to AN103 are not subjected to conversion. 1: AN100 to AN103 are subjected to conversion.	R/W
b1	ANSA001			R/W
b2	ANSA002			R/W
b3	ANSA003			R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

S12AD1.ADANSA0 selects analog input channels for A/D conversion from among AN100 to AN103. In group scan mode, this register selects group A channels.

ANSA0n Bit (n = 00 to 03) (A/D Conversion Channel Select)

The ANSA0n bit select analog input channels for A/D conversion from among AN100 to AN103. The channels to be selected and the number of channels can be arbitrarily set. The ANSA000 bit corresponds to AN100 and the ANSA003 bit corresponds to AN103.

When double trigger mode is selected, the channel selected by the S12AD1.ADCSR.DBLANS[4:0] bits is selected in group A, and the ANSA0n bit setting is invalid.

The ANSA0n bit should be set while the S12AD1.ADCSR.ADST bit is 0.

(3) S12AD2.ADANSA0

Address(es): 0008 9404h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	ANSA011	ANSA010	ANSA009	ANSA008	ANSA007	ANSA006	ANSA005	ANSA004	ANSA003	ANSA002	ANSA001	ANSA000
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ANSA000	A/D Conversion Channel Select	0: AN200 to AN211 are not subjected to conversion. 1: AN200 to AN211 are subjected to conversion.	R/W
b1	ANSA001			R/W
b2	ANSA002			R/W
b3	ANSA003			R/W
b4	ANSA004			R/W
b5	ANSA005			R/W
b6	ANSA006			R/W
b7	ANSA007			R/W
b8	ANSA008			R/W
b9	ANSA009			R/W
b10	ANSA010			R/W
b11	ANSA011			R/W
b15 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

S12AD.ADANSA0 selects analog input channels for A/D conversion from among AN200 to AN211. In group scan mode, this register selects group A channels.

ANSA0n Bit (n = 00 to 11) (A/D Conversion Channel Select)

The ANSA0n bit select analog input channels for A/D conversion from among AN200 to AN211. The channels to be selected and the number of channels can be arbitrarily set. When performing A/D conversion of the internal reference voltage, do not select analog input channels. The setting value of this register should be 0000h. The ANSA000 bit corresponds to AN200 and the ANSA011 bit corresponds to AN211.

When double trigger mode is selected, the channel selected by the S12AD2.ADCSR.DBLANS[4:0] bits is selected in group A, and the ANSA0n bit setting is invalid.

The ANSA0n bit should be set while the S12AD2.ADCSR.ADST bit is 0.

31.2.5 A/D Channel Select Register A1 (ADANSA1)

(1) S12AD.ADANSA1

Address(es): 0008 9006h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ANSA100
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ANSA100	A/D Conversion Channel Select	0: AN016 is not subjected to conversion. 1: AN016 is subjected to conversion.	R/W
b15 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

S12AD.ADANSA1 selects an analog input channel AN016 for A/D conversion. In group scan mode, group A channels are to be selected.

ANSA100 Bit (A/D Conversion Channel Select)

The ANSA100 bit selects analog input channel AN016 for A/D conversion.
When double trigger mode is selected, the channel selected by the S12AD.ADCSR.DBLANS[4:0] bits is selected in group A, and the ANSA100 bit setting is invalid.
The ANSA100 bit should be set while the S12AD.ADCSR.ADST bit is 0.

(2) S12AD1.ADANSA1

Address(es): 0008 9206h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ANSA100
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ANSA100	A/D Conversion Channel Select	0: AN116 is not subjected to conversion. 1: AN116 is subjected to conversion.	R/W
b15 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

S12AD.ADANSA1 selects an analog input channel AN116 for A/D conversion. In group scan mode, group A channels are to be selected.

ANSA100 Bit (A/D Conversion Channel Select)

The ANSA100 bit selects analog input channel AN116 for A/D conversion.
When double trigger mode is selected, the channel selected by the S12AD1.ADCSR.DBLANS[4:0] bits is selected in group A, and the ANSA100 bit setting is invalid.
The ANSA100 bit should be set while the S12AD1.ADCSR.ADST bit is 0.

31.2.6 A/D Channel Select Register B0 (ADANSB0)

(1) S12AD.ADANSB0

Address(es): 0008 9014h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	ANSB003	ANSB002	ANSB001	ANSB000
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ANSB000	A/D Conversion Channel Select	0: AN000 to AN003 are not subjected to conversion. 1: AN000 to AN003 are subjected to conversion.	R/W
b1	ANSB001			R/W
b2	ANSB002			R/W
b3	ANSB003			R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

S12AD.ADANSB0 selects analog input channels for A/D conversion from among AN000 to AN003 in group B when group scan mode is selected. The S12AD.ADANSB0 register is not used in any scan mode other than group scan mode.

ANSB0n Bit (n = 00 to 03) (A/D Conversion Channel Select)

The ANSB0n bit select analog input channels for A/D conversion from among AN000 to AN003 in group B when group scan mode is selected. The S12AD.ADANSB0 register is used for group scan mode only; not used for any other modes. The channels specified in group A (the channels corresponding to group A, selected with the S12AD.ADANSA0 and S12AD.ADANSA1 registers and the S12AD.ADCSR.DBLANS[4:0] bits in double trigger mode) should be excluded as the channels to be selected and the number of channels to be set.

The ANSB000 bit corresponds to AN000 and the ANSB003 bit corresponds to AN003.

The ANSB0n bit should be set while the S12AD.ADCSR.ADST bit is 0.

(2) S12AD1.ADANSB0

Address(es): 0008 9214h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	ANSB003	ANSB002	ANSB001	ANSB000
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ANSB000	A/D Conversion Channel Select	0: AN100 to AN103 are not subjected to conversion. 1: AN100 to AN103 are subjected to conversion.	R/W
b1	ANSB001			R/W
b2	ANSB002			R/W
b3	ANSB003			R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

S12AD1.ADANSB0 selects analog input channels for A/D conversion from among AN100 to AN103 in group B when group scan mode is selected. The S12AD1.ADANSB0 register is not used in any scan mode other than group scan mode.

ANSB0n Bit (n = 00 to 03) (A/D Conversion Channel Select)

The ANSB0n bit select analog input channels for A/D conversion from among AN100 to AN103 in group B when group scan mode is selected. The S12AD1.ADANSB0 register is used for group scan mode only; not used for any other modes. The channels specified in group A (the channels corresponding to group A, selected with the S12AD1.ADANSA0 and S12AD1.ADANSA1 registers and the ADCSR.DBLANS[4:0] bits in double trigger mode) should be excluded as the channels to be selected and the number of channels to be set.

The ANSB000 bit corresponds to AN100 and the ANSB003 bit corresponds to AN103.

The ANSB0n bit should be set while the S12AD1.ADCSR.ADST bit is 0.

(3) S12AD2.ADANSB0

Address(es): 0008 9414h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	ANSB011	ANSB010	ANSB009	ANSB008	ANSB007	ANSB006	ANSB005	ANSB004	ANSB003	ANSB002	ANSB001	ANSB000
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ANSB000	A/D Conversion Channel Select	0: AN200 to AN211 are not subjected to conversion. 1: AN200 to AN211 are subjected to conversion.	R/W
b1	ANSB001			R/W
b2	ANSB002			R/W
b3	ANSB003			R/W
b4	ANSB004			R/W
b5	ANSB005			R/W
b6	ANSB006			R/W
b7	ANSB007			R/W
b8	ANSB008			R/W
b9	ANSB009			R/W
b10	ANSB010			R/W
b11	ANSB011			R/W
b15 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

S12AD2.ADANSB0 selects analog input channels for A/D conversion from among AN200 to AN211 in group B when group scan mode is selected. The S12AD2.ADANSB0 register is not used in any scan mode other than group scan mode.

ANSB0n Bit (n = 00 to 11) (A/D Conversion Channel Select)

The ANSB0n bit select analog input channels for A/D conversion from among AN200 to AN211 in group B when group scan mode is selected. The S12AD2.ADANSB0 register is used for group scan mode only; not used for any other modes. The channels specified in group A (the channels corresponding to group A, selected with the S12AD2.ADANSA0 and S12AD2.ADANSA1 registers and the S12AD2.ADCSR.DBLANS[4:0] bits in double trigger mode) should be excluded as the channels to be selected and the number of channels to be set.

The ANSB000 bit corresponds to AN200 and the ANSB011 bit corresponds to AN211.

When performing A/D conversion of the internal reference voltage, do not select any analog input channel. The setting value of this register should be 0000h.

The ANSB0n bit should be set while the S12AD2.ADCSR.ADST bit is 0.

31.2.7 A/D Channel Select Register B1 (ADANSB1)

(1) S12AD.ADANSB1

Address(es): 0008 9016h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ANSB100
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ANSB100	A/D Conversion Channel Select	0: AN016 is not subjected to conversion. 1: AN016 is subjected to conversion.	R/W
b15 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

S12AD.ADANSB1 selects analog input channel AN016 for A/D conversion in group B when group scan mode is selected. The S12AD.ADANSB1 register is not used in any scan mode other than group scan mode.

ANSB100 Bit (A/D Conversion Channel Select)

The ANSB100 bit selects analog input channel AN016 for A/D conversion in group B when group scan mode is selected. The ADANSB1 register is used for group scan mode only; not used for any other modes. The channels specified in group A (the channels corresponding to group A, selected with the S12AD.ADANSA0, S12AD.ADANSA1 registers and the S12AD.ADCSR.DBLANS[4:0] bits in double trigger mode) should be excluded as the channels to be selected and the number of channels to be set.

The ANSB100 bit should be set while the S12AD.ADCSR.ADST bit is 0.

(2) S12AD1.ADANSB1

Address(es): 0008 9216h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ANSB100
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ANSB100	A/D Conversion Channel Select	0: AN116 is not subjected to conversion. 1: AN116 is subjected to conversion.	R/W
b15 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

S12AD1.ADANSB1 selects analog input channel AN116 for A/D conversion in group B when group scan mode is selected. The S12AD1.ADANSB1 register is not used in any scan mode other than group scan mode.

ANSB100 Bit (A/D Conversion Channel Select)

The ANSB100 bit select analog input channel AN116 for A/D conversion in group B when group scan mode is selected. The S12AD1.ADANSB1 register is used for group scan mode only; not used for any other modes. The channels specified in group A (the channels corresponding to group A, selected with the S12AD1.ADANSA0, S12AD1.ADANSA1 registers and the S12AD1.ADCSR.DBLANS[4:0] bits in double trigger mode) should be excluded as the channels to be selected and the number of channels to be set.
The ANSB100 bit should be set while the S12AD1.ADCSR.ADST bit is 0.

31.2.8 A/D Channel Select Register C0 (ADANSC0)

(1) S12AD.ADANSC0

Address(es): 0008 90D4h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	ANSC003	ANSC002	ANSC001	ANSC000
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ANSC000	A/D Conversion Channel Select	0: AN000 to AN003 are not subjected to conversion. 1: AN000 to AN003 are subjected to conversion.	R/W
b1	ANSC001			R/W
b2	ANSC002			R/W
b3	ANSC003			R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

S12AD.ADANSC0 selects analog input channels for A/D conversion from among AN000 to AN003 in group C when group scan mode is selected. The S12AD.ADANSC0 register is not used in any scan mode other than group scan mode.

ANSC0n Bit (n = 00 to 03) (A/D Conversion Channel Select)

The ANSC0n bit select analog input channels for A/D conversion from among AN000 to AN003 in group C when group scan mode is selected. The S12AD.ADANSC0 register is used for group scan mode only; not used for any other modes. The ANSC000 bit corresponds to AN000 and the ANSC003 bit corresponds to AN003.
The ANSC0n bit should be set while the S12AD.ADCSR.ADST bit is 0.

(2) S12AD1.ADANSC0

Address(es): 0008 92D4h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	ANSC003	ANSC002	ANSC001	ANSC000
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ANSC000	A/D Conversion Channel Select	0: AN100 to AN103 are not subjected to conversion. 1: AN100 to AN103 are subjected to conversion.	R/W
b1	ANSC001			R/W
b2	ANSC002			R/W
b3	ANSC003			R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

S12AD1.ADANSC0 selects analog input channels for A/D conversion from among AN100 to AN103 in group C when group scan mode is selected. The S12AD1.ADANSC0 register is not used in any scan mode other than group scan mode.

ANSC0n Bit (n = 00 to 03) (A/D Conversion Channel Select)

The ANSC0n bit select analog input channels for A/D conversion from among AN100 to AN103 in group C when group scan mode is selected. The S12AD1.ADANSC0 register is used for group scan mode only; not used for any other modes.

The ANSC000 bit corresponds to AN100 and the ANSC003 bit corresponds to AN103.
The ANSC0n bit should be set while the S12AD1.ADCSR.ADST bit is 0.

(3) S12AD2.ADANSC0

Address(es): 0008 94D4h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	ANSC011	ANSC010	ANSC009	ANSC008	ANSC007	ANSC006	ANSC005	ANSC004	ANSC003	ANSC002	ANSC001	ANSC000
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ANSC000	A/D Conversion Channel Select	0: AN200 to AN211 are not subjected to conversion. 1: AN200 to AN211 are subjected to conversion.	R/W
b1	ANSC001			R/W
b2	ANSC002			R/W
b3	ANSC003			R/W
b4	ANSC004			R/W
b5	ANSC005			R/W
b6	ANSC006			R/W
b7	ANSC007			R/W
b8	ANSC008			R/W
b9	ANSC009			R/W
b10	ANSC010			R/W
b11	ANSC011			R/W
b15 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

S12AD2.ADANSC0 selects analog input channels for A/D conversion from among AN200 to AN211 in group C when group scan mode is selected. The S12AD2.ADANSC0 register is not used in any scan mode other than group scan mode.

ANSC0n Bit (n = 00 to 11) (A/D Conversion Channel Select)

The ANSC0n bit select analog input channels for A/D conversion from among AN200 to AN211 in group C when group scan mode is selected. The S12AD2.ADANSC0 register is used for group scan mode only; not used for any other modes.
The ANSC000 bit corresponds to AN200 and the ANSC011 bit corresponds to AN211.
When performing A/D conversion of the internal reference voltage, do not select analog input channels. The setting value of this register should be 0000h.
The ANSC0n bit should be set while the S12AD2.ADCSR.ADST bit is 0.

31.2.9 A/D Channel Select Register C1 (ADANSC1)

(1) S12AD.ADANSC1

Address(es): 0008 90D6h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ANSC100
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ANSC100	A/D Conversion Channel Select	0: AN016 is not subjected to conversion. 1: AN016 is subjected to conversion.	R/W
b15 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

S12AD.ADANSC1 selects analog input channel AN016 for A/D conversion in group C when group scan mode is selected. The S12AD.ADANSC1 register is not used in any scan mode other than group scan mode.

ANSC100 Bit (A/D Conversion Channel Select)

The ANSC100 bit selects analog input channel AN016 for A/D conversion in group C when group scan mode is selected. The S12AD.ADANSC1 register is used for group scan mode only; not used for any other modes.
The ANSC100 bit should be set while the S12AD.ADCSR.ADST bit is 0.

(2) S12AD1.ADANSC1

Address(es): 0008 92D6h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ANSC100
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ANSC100	A/D Conversion Channel Select	0: AN116 is not subjected to conversion. 1: AN116 is subjected to conversion.	R/W
b15 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

S12AD1.ADANSC1 selects analog input channel AN116 for A/D conversion in group C when group scan mode is selected. The S12AD1.ADANSC1 register is not used in any scan mode other than group scan mode.

ANSC100 Bit (A/D Conversion Channel Select)

The ANSC100 bit selects analog input channel AN116 for A/D conversion in group C when group scan mode is selected. The S12AD1.ADANSC1 register is used for group scan mode only; not used for any other modes.
The ANSC100 bit should be set while the S12AD1.ADCSR.ADST bit is 0.

31.2.10 A/D-Converted Value Addition/Average Function Channel Select Register 0 (ADADS0)

(1) S12AD.ADADS0

Address(es): 0008 9008h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	ADS003	ADS002	ADS001	ADS000
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ADS000	A/D-Converted Value Addition/ Average Channel Select	0: A/D-converted value addition/average mode for AN000 to AN003 is not selected. 1: A/D-converted value addition/average mode for AN000 to AN003 is selected.	R/W
b1	ADS001			R/W
b2	ADS002			R/W
b3	ADS003			R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

S12AD.ADADS0 selects channels AN000 to AN003 on which A/D conversion is performed successively 2, 3, 4, or 16 times and then converted values are added (integrated) or averaged.

ADS0n Bit (n = 00 to 03) (A/D-Converted Value Addition/Average Channel Select)

When the ADS0n bit of the number that is the same as that of A/D-converted channel selected by the S12AD.ADANSA0.ANSA0n bit (n = 00 to 03) or S12AD.ADCSR.DBLANS[4:0] bits and S12AD.ADANSB0.ANSB0n bit is set to 1, A/D conversion of analog input of the selected channels is performed successively 2, 3, 4, or 16 times that is set with the S12AD.ADADC.ADC[2:0] bits.

When the S12AD.ADADC.AVEE bit is 0, the value obtained by addition (integration) is stored in the A/D data register.

When the S12AD.ADADC.AVEE bit is 1, the mean value of the results obtained by addition (integration) is stored in the A/D data register.

As for the channel on which the A/D conversion is performed and addition/average mode is not selected, a normal one-time conversion is executed and the conversion result is stored to the A/D data register.

The ADS0n bit should be set while the S12AD.ADCSR.ADST bit is 0.

(2) S12AD1.ADADS0

Address(es): 0008 9208h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	ADS003	ADS002	ADS001	ADS000
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ADS000	A/D-Converted Value Addition/ Average Channel Select	0: A/D-converted value addition/average mode for AN100 to AN103 is not selected. 1: A/D-converted value addition/average mode for AN100 to AN103 is selected.	R/W
b1	ADS001			R/W
b2	ADS002			R/W
b3	ADS003			R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

S12AD1.ADADS0 selects channels AN100 to AN103 on which A/D conversion is performed successively 2, 3, 4, or 16 times and then converted values are added (integrated) or averaged.

ADS0n Bit (n =00 to 03) (A/D-Converted Value Addition/Average Channel Select)

When the ADS0n bit of the number that is the same as that of A/D-converted channel selected by the S12AD1.ADANSA0.ANSA0n bit (n = 00 to 03) or S12AD1.ADCSR.DBLANS[4:0] bits and S12AD1.ADANSB0.ANSB0n bit and S12AD1.ADANSC0.ANSC0n bit is set to 1, A/D conversion of analog input of the selected channels is performed successively 2, 3, 4, or 16 times that is set with the S12AD1.ADADC.ADC[2:0] bits.
When the S12AD1.ADADC.AVEE bit is 0, the value obtained by addition (integration) is stored in the A/D data register.
When the S12AD1.ADADC.AVEE bit is 1, the mean value of the results obtained by addition (integration) is stored in the A/D data register.
As for the channel on which the A/D conversion is performed and addition/average mode is not selected, a normal one-time conversion is executed and the conversion result is stored to the A/D data register.
The ADS0n bit should be set while the S12AD1.ADCSR.ADST bit is 0.

(3) S12AD2.ADADS0

Address(es): 0008 9408h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	ADS011	ADS010	ADS009	ADS008	ADS007	ADS006	ADS005	ADS004	ADS003	ADS002	ADS001	ADS000
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ADS000	A/D-Converted Value Addition/ Average Channel Select	0: A/D-converted value addition/average mode for AN200 to AN211 is not selected. 1: A/D-converted value addition/average mode for AN200 to AN211 is selected.	R/W
b1	ADS001			R/W
b2	ADS002			R/W
b3	ADS003			R/W
b4	ADS004			R/W
b5	ADS005			R/W
b6	ADS006			R/W
b7	ADS007			R/W
b8	ADS008			R/W
b9	ADS009			R/W
b10	ADS010			R/W
b11	ADS011			R/W
b15 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

S12AD2.ADADS0 selects channels AN200 to AN211 on which A/D conversion is performed successively 2, 3, 4, or 16 times and then converted values are added (integrated) or averaged.

ADS0n Bit (n = 00 to 11) (A/D-Converted Value Addition/Average Channel Select)

When the ADS0n bit of the number that is the same as that of A/D-converted channel selected by the S12AD2.ADANSA0.ANSA0n bit (n = 00 to 11) or S12AD2.ADCSR.DBLANS[4:0] bits and S12AD2.ADANSB0.ANSB0 bit and S12AD2.ADANSC0.ANSC0n bit is set to 1, A/D conversion of analog input of the selected channels is performed successively 2, 3, 4, or 16 times that is set with the S12AD2.ADADC.ADC[2:0] bits.
When the S12AD2.ADADC.AVEE bit is 0, the value obtained by addition (integration) is stored in the A/D data register.
When the S12AD2.ADADC.AVEE bit is 1, the mean value of the results obtained by addition (integration) is stored in the A/D data register.
As for the channel on which the A/D conversion is performed and addition/average mode is not selected, a normal one-time conversion is executed and the conversion result is stored to the A/D data register.
The ADS0n bit should be set while the S12AD2.ADCSR.ADST bit is 0.

31.2.11 A/D-Converted Value Addition/Average Function Channel Select Register 1 (ADADS1)

(1) S12AD.ADADS1

Address(es): 0008 900Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ADS100
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ADS100	A/D-Converted Value Addition/ Average Channel Select	0: A/D-converted value addition/average mode for AN016 is not selected. 1: A/D-converted value addition/average mode for AN016 is selected.	R/W
b15 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

S12AD.ADADS1 selects channel AN016 on which A/D conversion is performed successively 2, 3, 4, or 16 times and then converted values are added (integrated) or averaged.

ADS100 Bit (A/D-Converted Value Addition/Average Channel Select)

When the ADS100 bit of the number that is the same as that of A/D-converted channel selected by the S12AD.ADANSA1.ADS100 bit or S12AD.ADCSR.DBLANS[4:0] bits and S12AD.ADANSB1.ANSB100 bit is set to 1, A/D conversion of analog input of the selected channels is performed successively 2, 3, 4, or 16 times that is set with the S12AD.ADADC.ADC[2:0] bits. When the S12AD.ADADC.AVEE bit is 0, the value obtained by addition (integration) is stored in the A/D data register. When the S12AD.ADADC.AVEE bit is 1, the mean value of the results obtained by addition (integration) is stored in the A/D data register. As for the channel on which the A/D conversion is performed and addition/average mode is not selected, a normal one-time conversion is executed and the conversion result is stored to the A/D data register.

The ADS100 bit should be set while the S12AD.ADCSR.ADST bit is 0.

(2) S12AD1.ADADS1

Address(es): 0008 920Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ADS100
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ADS100	A/D-Converted Value Addition/ Average Channel Select	0: A/D-converted value addition/average mode for AN116 is not selected. 1: A/D-converted value addition/average mode for AN116 is selected.	R/W
b15 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

S12AD1.ADADS1 selects channel AN116 on which A/D conversion is performed successively 2, 3, 4, or 16 times and then converted values are added (integrated) or averaged.

ADS100 Bit (A/D-Converted Value Addition/Average Channel Select)

When the ADS100 bit of the number that is the same as that of A/D-converted channel selected by the S12AD1.ADANSA1.ADS100 bit or S12AD1.ADCSR.DBLANS[4:0] bits and S12AD1.ADANSB1.ANSB100 bit is set to 1, A/D conversion of analog input of the selected channels is performed successively 2, 3, 4, or 16 times that is set with the S12AD1.ADADC.ADC[2:0] bits. When the S12AD1.ADADC.AVEE bit is 0, the value obtained by addition (integration) is stored in the A/D data register. When the S12AD1.ADADC.AVEE bit is 1, the mean value of the results obtained by addition (integration) is stored in the A/D data register. As for the channel on which the A/D conversion is performed and addition/average mode is not selected, a normal one-time conversion is executed and the conversion result is stored to the A/D data register.
The ADS100 bit should be set while the S12AD1.ADCSR.ADST bit is 0.

Figure 31.4 shows a scanning operation sequence in which both the S12AD2.ADADS0.ADS002 and S12AD2.ADADS0.ADS006 bits are set to 1.
It is assumed that addition mode is selected (S12AD2.ADADC.AVEE = 0) in continuous scan mode (S12AD2.ADCSR.ADCS[1:0] = 10b), the addition count is set to three times (S12AD2.ADADC.ADC[2:0] = 011b), and channels AN200 to AN207 are selected (S12AD2.ADANSA0.ANSA0n = FFh). The conversion process begins with AN200. The AN202 conversion is performed successively four times (add three times), and the added (integrated) value is stored in A/D data register 2. After that the AN203 conversion is started. The AN206 conversion is performed successively four times and the added (integrated) value is stored in A/D data register 6. After conversion of AN207, the conversion operation is once again performed in the same sequence from AN200.

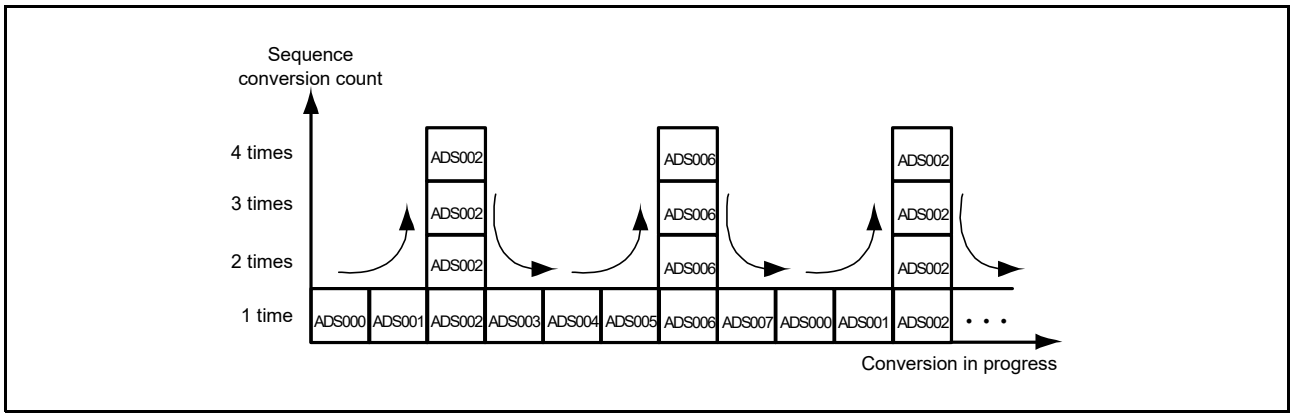


Figure 31.4 Scan Conversion Sequence with S12AD2.ADADC.ADC[2:0] = 011b, S12AD2.ADADC.AVEE = 0, S12AD2.ADADS0.ADS002 = 1, and S12AD2.ADADS0.ADS006 = 1

31.2.12 A/D-Converted Value Addition/Average Count Select Register (ADADC)

Address(es): S12AD.ADADC 0008 900Ch, S12AD1.ADADC 0008 920Ch, S12AD2.ADADC 0008 940Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	AVEE	—	—	—	—	ADC[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	ADC[2:0]	Addition Count Select	b2 b0 0 0 0: 1-time conversion (no addition; same as normal conversion) 0 0 1: 2-time conversion (addition once) 0 1 0: 3-time conversion (addition twice)*1 0 1 1: 4-time conversion (addition three times) 1 0 1: 16-time conversion (addition 15 times)*1 Settings other than above are prohibited.	R/W
b6 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	AVEE	Average Mode Enable	0: Addition mode is selected. 1: Average mode is selected.	R/W

Note 1. The AVEE bit is enabled only when 2-time or 4-time conversion is selected. When average mode is selected (ADADC.AVEE bit = 1), do not set 3-time conversion (ADADC.ADC[2:0] = 010b) nor 16-time conversion (ADADC.ADC[2:0] = 101b).

ADADC sets the addition count for A/D conversion of the channel, and internal reference voltage (S12AD2 only) for which A/D-converted value addition/average mode is selected, and selects either addition or average mode.

ADC[2:0] Bits (Addition Count Select)

The ADC[2:0] bits set the addition count common to the channels for which A/D conversion and A/D-converted value addition/average mode is selected, including the channels selected in double trigger mode (by ADCSR.DBLANS[4:0] bits), and to A/D conversion of internal reference voltage.
When average mode is selected by setting the ADADC.AVEE bit to 1, do not set the addition count to one time (ADADC.ADC[2:0] = 000b), three times (ADADC.ADC[2:0] = 010b), or 16 times (ADADC.ADC[2:0] = 101b).
The ADC[2:0] bits should be set while the ADCSR.ADST bit is 0.

AVEE Bit (Average Mode Enable)

The AVEE bit selects addition or average mode for A/D conversion of the channel for which A/D conversion and A/D-converted value addition/average mode is selected, including the channels selected in double trigger mode (by ADCSR.DBLANS[4:0] bits) and internal reference voltage.
When average mode is selected by setting the ADADC.AVEE bit to 1, do not set the addition count to one time (ADADC.ADC[2:0] = 000b), three times (ADADC.ADC[2:0] = 010b), or 16 times (ADADC.ADC[2:0] = 101b). The mean value of 1-time, 3-time, and 16-time conversion cannot be obtained.
The AVEE bit should be set while the ADCSR.ADST bit is 0.

31.2.13 A/D Control Extended Register (ADCER)

Address(es): S12AD.ADCER 0008 900Eh, S12AD1.ADCER 0008 920Eh, S12AD2.ADCER 0008 940Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ADRFMT	—	—	—	DIAGM	DIAGLD	DIAGVAL[1:0]		—	—	ACE	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5	ACE	A/D Data Register Automatic Clearing Enable	0: Disables automatic clearing. 1: Enables automatic clearing.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b9, b8	DIAGVAL[1:0]	Self-Diagnosis Conversion Voltage Select	b9 b8 0 0: Setting prohibited in self-diagnosis voltage fixed mode 0 1: Uses the voltage of 0 V for self-diagnosis. 1 0: Uses the voltage of reference power supply × 1/2 for self-diagnosis. 1 1: Uses the voltage of reference power supply for self-diagnosis.	R/W
b10	DIAGLD	Self-Diagnosis Mode Select	0: Rotation mode for self-diagnosis voltage 1: Fixed mode for self-diagnosis voltage	R/W
b11	DIAGM	Self-Diagnosis Enable	0: Disables self-diagnosis of 12-bit A/D converter. 1: Enables self-diagnosis of 12-bit A/D converter.	R/W
b14 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	ADRFMT	A/D Data Register Format Select	0: Flush-right is selected for the A/D data register format. 1: Flush-left is selected for the A/D data register format.	R/W

ADCER sets self-diagnosis mode, format of A/D data registers y (ADDRy), and automatic clearing of A/D data registers.

ACE Bit (A/D Data Register Automatic Clearing Enable)

The ACE bit enables or disables automatic clearing (all 0) of ADDRy, ADRD, ADDBLDR, ADDBLDRA, ADDBLDRB, or ADOCDR after any of these registers have been read by the CPU and DTC. Automatic clearing of the A/D data register is enabled to detect a failure which has not been updated in the A/D data register.

DIAGVAL[1:0] Bits (Self-Diagnosis Conversion Voltage Select)

The DIAGVAL[1:0] bits select the voltage value used in self-diagnosis voltage fixed mode. For details, refer to the descriptions of the ADCER.DIAGLD bit.

Self-diagnosis should not be executed by setting the ADCER.DIAGLD bit to 1 when the ADCER.DIAGVAL[1:0] bits are set to 00b.

DIAGLD Bit (Self-Diagnosis Mode Select)

The DIAGLD bit selects whether the three voltage values are rotated or the fixed voltage is used in self-diagnosis. Setting this bit (ADCER.DIAGLD) to 0 allows conversion of the voltages in rotation mode where 0, the reference power supply × 1/2, and the reference power supply are converted in this order. When self-diagnosis rotation mode is selected after a reset, self-diagnosis is performed from 0 V. When self-diagnosis voltage fixed mode is selected, the fixed voltage specified by the ADCER.DIAGVAL[1:0] bits is converted. In self-diagnosis voltage rotation mode, the self-diagnosis voltage value does not return to 0 when scan conversion is completed. When scan conversion is restarted, therefore, rotation starts at the voltage value following the previous value. If fixed mode is switched to rotation mode, rotation

starts at the fixed voltage value.
The DIAGLD bit should be set while the ADCSR.ADST bit is 0.

DIAGM Bit (Self-Diagnosis Enable)

The DIAGM bit enables or disables self-diagnosis.
Self-diagnosis is used to detect a failure of the 12-bit A/D converter. Specifically, one of the internally generated voltage values 0, the reference power supply × 1/2, and the reference power supply is converted. When conversion is completed, information on the converted voltage and the conversion result is stored into the self-diagnosis data register (ADRD). ADRD can then be read out by software to determine whether the conversion result falls within the normal range (normal) or not (abnormal). Self-diagnosis is executed once at the beginning of each scan, and one of the three voltages is converted. When self-diagnosis is selected in group scan mode, self-diagnosis is separately executed in groups A, B, and C.
The DIAGM bit should be set while the ADCSR.ADST bit is 0.

ADRFMT Bit (A/D Data Register Format Select)

The ADRFMT bit specifies flush-right or flush-left for the data to be stored in ADDRy, ADDBLDR, ADDBLDRA, ADDBLDRB, ADOCDR, or ADRD.
The ADRFMT bit should be set while the ADCSR.ADST bit is 0.

For details on the format of each data register, see section 31.2.1, A/D Data Registers y (ADDRy) A/D Data Duplication Register (ADDBLDR) A/D Data Duplication Register A (ADDBLDRA) A/D Data Duplication Register B (ADDBLDRB) A/D Internal Reference Voltage Data Register (ADOCDR), and section 31.2.2, A/D Self-Diagnosis Data Register (ADRD) .

31.2.14 A/D Conversion Start Trigger Select Register (ADSTRGR)

Address(es): S12AD.ADSTRGR 0008 9010h, S12AD1.ADSTRGR 0008 9210h, S12AD2.ADSTRGR 0008 9410h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	TRSA[5:0]						—	—	TRSB[5:0]					
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	TRSB[5:0]	A/D Conversion Start Trigger Select for Group B	Select the A/D conversion start trigger for group B in group scan mode.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13 to b8	TRSA[5:0]	A/D Conversion Start Trigger Select	Select the A/D conversion start trigger in single scan mode and continuous mode. In group scan mode, the A/D conversion start trigger for group A is selected.	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ADSTRGR selects the A/D conversion start trigger.

TRSB[5:0] Bits (A/D Conversion Start Trigger Select for Group B)

The TRSB[5:0] bits select the trigger to start scanning of the analog input selected in group B. The TRSB[5:0] bits require to be set only in group scan mode and are not used in any other scan mode. For the scan conversion start trigger for group B, setting a software trigger or an asynchronous trigger is prohibited. Therefore, the TRSB[5:0] bits should be set to the value other than 000000b and the ADCSR.TRGE bit should be set to 1 in group scan mode.

When two groups are selected (ADGCTRGR.GRCE = 0) during group priority operation in group scan mode, setting the ADGSPCR.GBRP bit to 1 allows group B to continuously operate in single scan mode. When setting the ADGSPCR.GBRP bit to 1, set the TRSB[5:0] bits to 3Fh. Note that the issuance period of trigger for A/D conversion must be more than or equal to the actual scan conversion time (t_{SCAN}). If the issuance period is less than t_{SCAN}, A/D conversion by the trigger may have no effect.

When the trigger from the modules (MTU and GPT) operated in 80 MHz is selected as an A/D conversion start trigger, a delay of the period for synchronization processing occurs. See section 31.3.5, Analog Input Sampling Time and Scan Conversion Time for details.

Table 31.8 lists the A/D conversion startup sources selected by the TRSB[5:0] bits.

TRSA[5:0] Bits (A/D Conversion Start Trigger Select)

The TRSA[5:0] bits select the trigger to start A/D conversion in single scan mode and continuous scan mode. In group scan mode, the trigger to start scanning of the analog input selected in group A is selected. When scanning is executed in group scan mode or double trigger mode, set the ADCSR.TRGE bit to 1.

- When using the A/D conversion startup source of a synchronous trigger, set the ADCSR.TRGE bit to 1 and set the ADCSR.EXTRG bit to 0.
- When using the asynchronous trigger, set the ADCSR.TRGE bit to 1 and set the ADCSR.EXTRG bit to 1.
- Software trigger (ADCSR.ADST) is enabled regardless of the settings of the ADCSR.TRGE bit, the ADCSR.EXTRG bit, and the TRSA[5:0] bits.

Note that the issuance period of trigger for A/D conversion must be more than or equal to the actual scan conversion time (t_{SCAN}). If the issuance period is less than t_{SCAN}, A/D conversion by a trigger may have no effect. When the trigger from the modules (MTU and GPT) operated in 80 MHz is selected as an A/D conversion start trigger, a delay of the period for synchronization processing occurs. See section 31.3.5, Analog Input Sampling Time and Scan Conversion Time

for details.

Table 31.9 lists the selection of A/D conversion start sources selected by the TRSA[5:0] bits.

Table 31.8 Selection of A/D Activation Sources by the TRSB[5:0] Bits (1/2)

Module	Source	Remarks	TRSB[5]	TRSB[4]	TRSB[3]	TRSB[2]	TRSB[1]	TRSB[0]
Trigger source deselection state			1	1	1	1	1	1
MTU3	TRGA0N	Compare match/input capture from MTU0.TGRA	0	0	0	0	0	1
	TRGA1N	Compare match/input capture from MTU1.TGRA	0	0	0	0	1	0
	TRGA2N	Compare match/input capture from MTU2.TGRA	0	0	0	0	1	1
	TRGA3N	Compare match/input capture from MTU3.TGRA	0	0	0	1	0	0
	TRGA4N	Compare match/input capture from MTU4.TGRA or underflow (trough) of MTU4.TCNT in complementary PWM mode	0	0	0	1	0	1
	TRGA6N	Compare match/input capture from MTU6.TGRA	0	0	0	1	1	0
	TRGA7N	Compare match/input capture from MTU7.TGRA or underflow (trough) of MTU7.TCNT in complementary PWM mode	0	0	0	1	1	1
	TRG0N	Compare match from MTU0.TGRE	0	0	1	0	0	0
	TRG4AN	Compare match between MTU4.TADCORA and MTU4.TCNT	0	0	1	0	0	1
	TRG4BN	Compare match between MTU4.TADCORB and MTU4.TCNT	0	0	1	0	1	0
	TRG4AN or TRG4BN	Compare match between MTU4.TADCORA and MTU4.TCNT, or compare match between MTU4.TADCORB and MTU4.TCNT	0	0	1	0	1	1
	TRG4ABN	Compare match between MTU4.TADCORA and MTU4.TCNT, and compare match between MTU4.TADCORB and MTU4.TCNT (when interrupt skipping function 2 is used)	0	0	1	1	0	0
	TRG7AN	Compare match between MTU7.TADCORA and MTU7.TCNT	0	0	1	1	0	1
	TRG7BN	Compare match between MTU7.TADCORB and MTU7.TCNT	0	0	1	1	1	0
	TRG7AN or TRG7BN	Compare match between MTU7.TADCORA and MTU7.TCNT, or compare match between MTU7.TADCORB and MTU7.TCNT	0	0	1	1	1	1
	TRG7ABN	Compare match between MTU7.TADCORA and MTU7.TCNT, and compare match between MTU7.TADCORB and MTU7.TCNT (when interrupt skipping function 2 is used)	0	1	0	0	0	0
	TRGA9N	Compare match/input capture from MTU9.TGRA	0	1	0	0	1	1
	TRG9N	Compare match from MTU9.TGRE	0	1	0	1	0	0
	TRGA0N or TRG0N	Compare match/input capture from MTU0.TGRA, or compare match from MTU0.TGRE	0	1	1	0	0	1
	TRGA9N or TRG9N	Compare match/input capture from MTU9.TGRA, or compare match from MTU9.TGRE	0	1	1	0	1	0
	TRGA0N or TRGA9N	Compare match/input capture from MTU0.TGRA, or compare match/input capture from MTU9.TGRA.	0	1	1	0	1	1
	TRG0N or TRG9N	Compare match from MTU0.TGRE, or compare match from MTU9.TGRE	0	1	1	1	0	0
TMR	TMTRG0AN_0	Compare match between TMR0.TCORA and TMR0.TCNT	0	1	1	1	0	1
	TMTRG0AN_1	Compare match between TMR2.TCORA and TMR2.TCNT	0	1	1	1	1	0
	TMTRG0AN_2	Compare match between TMR4.TCORA and TMR4.TCNT	0	1	1	1	1	1
	TMTRG0AN_3	Compare match between TMR6.TCORA and TMR6.TCNT	1	0	0	0	0	0
MTU3	TRG9AEN	Compare match/input capture from MTU9.TGRA, and compare match from MTU9.TGRE.	1	0	0	0	0	1
	TRG0AEN	Compare match/input capture from MTU0.TGRA, and compare match from MTU0.TGRE.	1	0	0	0	1	0
	TRGA09N	Compare match/input capture from MTU0.TGRA, and compare match/input capture from MTU9.TGRA.	1	0	0	0	1	1
	TRG09N	Compare match from MTU0.TGRE, and Compare match from MTU9.TGRE.	1	0	0	1	0	0

Table 31.8 Selection of A/D Activation Sources by the TRSB[5:0] Bits (2/2)

Module	Source	Remarks	TRSB[5]	TRSB[4]	TRSB[3]	TRSB[2]	TRSB[1]	TRSB[0]
GPT	GTADTRA0N	Compare match with GPT0.GTADTRA	1	1	0	0	1	0
	GTADTRB0N	Compare match with GPT0.GTADTRB	1	1	0	0	1	1
	GTADTRA1N	Compare match with GPT1.GTADTRA	1	1	0	1	0	0
	GTADTRB1N	Compare match with GPT1.GTADTRB	1	1	0	1	0	1
	GTADTRA2N	Compare match with GPT2.GTADTRA	1	1	0	1	1	0
	GTADTRB2N	Compare match with GPT2.GTADTRB	1	1	0	1	1	1
	GTADTRA3N	Compare match with GPT3.GTADTRA	1	1	1	0	0	0
	GTADTRB3N	Compare match with GPT3.GTADTRB	1	1	1	0	0	1
	GTADTRA0N or GTADTRB0N	Compare match with GPT0.GTADTRA or GPT0.GTADTRB	1	1	1	0	1	0
	GTADTRA1N or GTADTRB1N	Compare match with GPT1.GTADTRA or GPT1.GTADTRB	1	1	1	0	1	1
	GTADTRA2N or GTADTRB2N	Compare match with GPT2.GTADTRA or GPT2.GTADTRB	1	1	1	1	0	0
	GTADTRA3N or GTADTRB3N	Compare match with GPT3.GTADTRA or GPT3.GTADTRB	1	1	1	1	0	1

Table 31.9 Selection of A/D Activation Sources by the TRSA[5:0] Bits (1/2)

Module	Source	Remarks	TRSA[5]	TRSA[4]	TRSA[3]	TRSA[2]	TRSA[1]	TRSA[0]
Trigger source deselection state			1	1	1	1	1	1
MTU3	TRGA0N	Compare match/input capture from MTU0.TGRA	0	0	0	0	0	1
	TRGA1N	Compare match/input capture from MTU1.TGRA	0	0	0	0	1	0
	TRGA2N	Compare match/input capture from MTU2.TGRA	0	0	0	0	1	1
	TRGA3N	Compare match/input capture from MTU3.TGRA	0	0	0	1	0	0
	TRGA4N	Compare match/input capture from MTU4.TGRA or underflow (trough) of MTU4.TCNT in complementary PWM mode	0	0	0	1	0	1
	TRGA6N	Compare match/input capture from MTU6.TGRA	0	0	0	1	1	0
	TRGA7N	Compare match/input capture from MTU7.TGRA or underflow (trough) of MTU7.TCNT in complementary PWM mode	0	0	0	1	1	1
	TRG0N	Compare match from MTU0.TGRE	0	0	1	0	0	0
	TRG4AN	Compare match between MTU4.TADCORA and MTU4.TCNT	0	0	1	0	0	1
	TRG4BN	Compare match between MTU4.TADCORB and MTU4.TCNT	0	0	1	0	1	0
	TRG4AN or TRG4BN	Compare match between MTU4.TADCORA and MTU4.TCNT, or compare match between MTU4.TADCORB and MTU4.TCNT	0	0	1	0	1	1
	TRG4ABN	Compare match between MTU4.TADCORA and MTU4.TCNT, and compare match between MTU4.TADCORB and MTU4.TCNT (when interrupt skipping function 2 is used)	0	0	1	1	0	0
	TRG7AN	Compare match between MTU7.TADCORA and MTU7.TCNT	0	0	1	1	0	1
	TRG7BN	Compare match between MTU7.TADCORB and MTU7.TCNT	0	0	1	1	1	0
	TRG7AN or TRG7BN	Compare match between MTU7.TADCORA and MTU7.TCNT, or compare match between MTU7.TADCORB and MTU7.TCNT	0	0	1	1	1	1
	TRG7ABN	Compare match between MTU7.TADCORA and MTU7.TCNT, and compare match between MTU7.TADCORB and MTU7.TCNT (when interrupt skipping function 2 is used)	0	1	0	0	0	0
	TRGA9N	Compare match/input capture from MTU9.TGRA	0	1	0	0	1	1
	TRG9N	Compare match from MTU9.TGRE	0	1	0	1	0	0
	TRGA0N or TRG0N	Compare match/input capture from MTU0.TGRA, or compare match from MTU0.TGRE	0	1	1	0	0	1
	TRGA9N or TRG9N	Compare match/input capture from MTU9.TGRA, or compare match from MTU9.TGRE	0	1	1	0	1	0
	TRGA0N or TRGA9N	Compare match/input capture from MTU0.TGRA, or compare match/input capture from MTU9.TGRA.	0	1	1	0	1	1
	TRG0N or TRG9N	Compare match from MTU0.TGRE, or compare match from MTU9.TGRE	0	1	1	1	0	0
TMR	TMTRG0AN_0	Compare match between TMR0.TCORA and TMR0.TCNT	0	1	1	1	0	1
	TMTRG0AN_1	Compare match between TMR2.TCORA and TMR2.TCNT	0	1	1	1	1	0
	TMTRG0AN_2	Compare match between TMR4.TCORA and TMR4.TCNT	0	1	1	1	1	1
	TMTRG0AN_3	Compare match between TMR6.TCORA and TMR6.TCNT	1	0	0	0	0	0
MTU3	TRG9AEN	Compare match/input capture from MTU9.TGRA, and compare match from MTU9.TGRE.	1	0	0	0	0	1
	TRG0AEN	Compare match/input capture from MTU0.TGRA, and compare match from MTU0.TGRE.	1	0	0	0	1	0
	TRGA09N	Compare match/input capture from MTU0.TGRA, and compare match/input capture from MTU9.TGRA.	1	0	0	0	1	1
	TRG09N	Compare match from MTU0.TGRE, and Compare match from MTU9.TGRE.	1	0	0	1	0	0

Table 31.9 Selection of A/D Activation Sources by the TRSA[5:0] Bits (2/2)

Module	Source	Remarks	TRSA[5]	TRSA[4]	TRSA[3]	TRSA[2]	TRSA[1]	TRSA[0]
GPT	GTADTRA0N	Compare match with GPT0.GTADTRA	1	1	0	0	1	0
	GTADTRB0N	Compare match with GPT0.GTADTRB	1	1	0	0	1	1
	GTADTRA1N	Compare match with GPT1.GTADTRA	1	1	0	1	0	0
	GTADTRB1N	Compare match with GPT1.GTADTRB	1	1	0	1	0	1
	GTADTRA2N	Compare match with GPT2.GTADTRA	1	1	0	1	1	0
	GTADTRB2N	Compare match with GPT2.GTADTRB	1	1	0	1	1	1
	GTADTRA3N	Compare match with GPT3.GTADTRA	1	1	1	0	0	0
	GTADTRB3N	Compare match with GPT3.GTADTRB	1	1	1	0	0	1
	GTADTRA0N or GTADTRB0N	Compare match with GPT0.GTADTRA or GPT0.GTADTRB	1	1	1	0	1	0
	GTADTRA1N or GTADTRB1N	Compare match with GPT1.GTADTRA or GPT1.GTADTRB	1	1	1	0	1	1
	GTADTRA2N or GTADTRB2N	Compare match with GPT2.GTADTRA or GPT2.GTADTRB	1	1	1	1	0	0
	GTADTRA3N or GTADTRB3N	Compare match with GPT3.GTADTRA or GPT3.GTADTRB	1	1	1	1	0	1

31.2.15 A/D Conversion Extended Input Control Register (ADEXICR)

Address(es): S12AD2.ADEXICR 0008 9412h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	OCSA	—	—	—	—	—	—	—	OCSAD	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b1	OCSAD	Internal Reference Voltage A/D-Converted Value Addition/Average Mode Select	0: Internal reference voltage A/D-converted value addition/average mode is not selected. 1: Internal reference voltage A/D-converted value addition/average mode is selected.	R/W
b8 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b9	OCSA	Internal Reference Voltage A/D Conversion Select	0: A/D conversion of internal reference voltage is not performed. 1: A/D conversion of internal reference voltage is performed.	R/W
b15 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ADEXICR specifies the settings of A/D conversion of the internal reference voltage.

OCSAD Bit (Internal Reference Voltage A/D-Converted Value Addition/Average Mode Select)

When the OCSAD bit is set to 1, A/D conversion of the internal reference voltage is selected and performed successively 2, 3, 4, or 16 times that is set with the ADADC.ADC[2:0] bits. When the ADADC.AVEE bit is 0, the value obtained by addition (integration) is stored in the A/D internal reference voltage data register (ADOCDR). When the ADADC.AVEE bit is 1, the mean value is stored in ADOCDR.

The OCSAD bit should be set while the ADCSR.ADST bit is 0.

OCSA Bit (Internal Reference Voltage A/D Conversion Select)

This bit selects A/D conversion of the internal reference voltage in single scan mode. When A/D conversion of the internal reference voltage is to be performed, set all the bits in the ADANSA0, ADANSA1, ADANSB0, and ADANSB1 registers and the ADCSR.DBLE bit should be set to all 0 in single scan mode.

The OCSA bit should be set while the ADCSR.ADST bit is 0. For A/D conversion of the internal reference voltage, the ADDISCR.ADNDIS[4:0] bits should be automatically set to 0Fh to discharge the A/D converter before sampling. The sampling time should be 5 µs or longer.

Sampling starts after discharging is completed during A/D conversion of the internal reference voltage, so an auto-discharging period of 15 ADCLK cycles is inserted before sampling.

31.2.16 A/D Group C Trigger Select Register (ADGCTRGR)

Address(es): S12AD.ADGCTRGR 0008 90D9h, S12AD1.ADGCTRGR 0008 92D9h, S12AD2.ADGCTRGR 0008 94D9h

	b7	b6	b5	b4	b3	b2	b1	b0
	GRCE	GCADIE	TRSC[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	TRSC[5:0]	Group C A/D Conversion Start Trigger Select	Select the A/D conversion start trigger for group C in group scan mode.	R/W
b6	GCADIE	Group C Scan End Interrupt Enable	0: Disables interrupt generation after completion of group C scan 1: Enables interrupt generation after completion of group C scan	R/W
b7	GRCE	Group C A/D Conversion Operation Enable	Enables A/D conversion operation for group C. 0: Group C is not used 1: Group C is used	R/W

ADGCTRGR enables operation for group C and selects the A/D conversion start trigger. For details on group priority operation, see Table 31.14 and Table 31.15.

TRSC[5:0] Bits (Group C A/D Conversion Start Trigger Select)

These bits select the trigger to start scanning of the analog input selected in group C. These bits are used for group scan mode only; not used for any other modes. Software trigger or asynchronous trigger cannot be set as the scan conversion trigger for group C. When using group C in group scan mode, set the TRSC[5:0] bits to a value other than 000000b, set the ADCSR.TRGE bit to 1, and set the GRCE bit to 1.

When group C is used during group priority control in group scan mode and the ADGSPCR.GBRP bit is set to 1, group C can be continuously operated in single scan mode. When continuously operating group C in single scan mode, set the TRSC[5:0] bits to 3Fh and disable trigger selection.

Note that the issuance period of trigger for A/D conversion must be more than or equal to the actual scan conversion time (t_{SCAN}). If the issuance period is less than tSCAN, A/D conversion by a trigger may have no effect.

When the trigger from the modules (MTU and GPT) operated in 80 MHz is selected as an A/D conversion start trigger, a delay of the period for synchronization processing occurs. See section 31.3.5, Analog Input Sampling Time and Scan Conversion Time for details.

Table 31.10 lists the selection of A/D conversion start sources selected by the TRSA[5:0] bits for group C.

Table 31.10 Selection of A/D Activation Sources by the TRSC[5:0] Bits (1/2)

Module	Source	Remarks	TRSC[5]	TRSC[4]	TRSC[3]	TRSC[2]	TRSC[1]	TRSC[0]
Trigger source deselection state			1	1	1	1	1	1
MTU3	TRGA0N	Compare match/input capture from MTU0.TGRA	0	0	0	0	0	1
	TRGA1N	Compare match/input capture from MTU1.TGRA	0	0	0	0	1	0
	TRGA2N	Compare match/input capture from MTU2.TGRA	0	0	0	0	1	1
	TRGA3N	Compare match/input capture from MTU3.TGRA	0	0	0	1	0	0
	TRGA4N	Compare match/input capture from MTU4.TGRA or underflow (trough) of MTU4.TCNT in complementary PWM mode	0	0	0	1	0	1
	TRGA6N	Compare match/input capture from MTU6.TGRA	0	0	0	1	1	0
	TRGA7N	Compare match/input capture from MTU7.TGRA or underflow (trough) of MTU7.TCNT in complementary PWM mode	0	0	0	1	1	1
	TRG0N	Compare match from MTU0.TGRE	0	0	1	0	0	0
	TRG4AN	Compare match between MTU4.TADCORA and MTU4.TCNT	0	0	1	0	0	1
	TRG4BN	Compare match between MTU4.TADCORB and MTU4.TCNT	0	0	1	0	1	0
	TRG4AN or TRG4BN	Compare match between MTU4.TADCORA and MTU4.TCNT, or compare match between MTU4.TADCORB and MTU4.TCNT	0	0	1	0	1	1
	TRG4ABN	Compare match between MTU4.TADCORA and MTU4.TCNT, and compare match between MTU4.TADCORB and MTU4.TCNT (when interrupt skipping function 2 is used)	0	0	1	1	0	0
	TRG7AN	Compare match between MTU7.TADCORA and MTU7.TCNT	0	0	1	1	0	1
	TRG7BN	Compare match between MTU7.TADCORB and MTU7.TCNT	0	0	1	1	1	0
	TRG7AN or TRG7BN	Compare match between MTU7.TADCORA and MTU7.TCNT, or compare match between MTU7.TADCORB and MTU7.TCNT	0	0	1	1	1	1
	TRG7ABN	Compare match between MTU7.TADCORA and MTU7.TCNT, and compare match between MTU7.TADCORB and MTU7.TCNT (when interrupt skipping function 2 is used)	0	1	0	0	0	0
	TRGA9N	Compare match/input capture from MTU9.TGRA	0	1	0	0	1	1
	TRG9N	Compare match from MTU9.TGRE	0	1	0	1	0	0
	TRGA0N or TRG0N	Compare match/input capture from MTU0.TGRA, or compare match from MTU0.TGRE	0	1	1	0	0	1
	TRGA9N or TRG9N	Compare match/input capture from MTU9.TGRA, or compare match from MTU9.TGRE	0	1	1	0	1	0
	TRGA0N or TRGA9N	Compare match/input capture from MTU0.TGRA, or compare match/input capture from MTU9.TGRA.	0	1	1	0	1	1
	TRG0N or TRG9N	Compare match from MTU0.TGRE, or compare match from MTU9.TGRE	0	1	1	1	0	0
TMR	TMTRG0AN_0	Compare match between TMR0.TCORA and TMR0.TCNT	0	1	1	1	0	1
	TMTRG0AN_1	Compare match between TMR2.TCORA and TMR2.TCNT	0	1	1	1	1	0
	TMTRG0AN_2	Compare match between TMR4.TCORA and TMR4.TCNT	0	1	1	1	1	1
	TMTRG0AN_3	Compare match between TMR6.TCORA and TMR6.TCNT	1	0	0	0	0	0
MTU3	TRG9AEN	Compare match/input capture from MTU9.TGRA, and compare match from MTU9.TGRE.	1	0	0	0	0	1
	TRG0AEN	Compare match/input capture from MTU0.TGRA, and compare match from MTU0.TGRE.	1	0	0	0	1	0
	TRGA09N	Compare match/input capture from MTU0.TGRA, and compare match/input capture from MTU9.TGRA.	1	0	0	0	1	1
	TRG09N	Compare match from MTU0.TGRE, and Compare match from MTU9.TGRE.	1	0	0	1	0	0

Table 31.10 Selection of A/D Activation Sources by the TRSC[5:0] Bits (2/2)

Module	Source	Remarks	TRSC[5]	TRSC[4]	TRSC[3]	TRSC[2]	TRSC[1]	TRSC[0]
GPT	GTADTRA0N	Compare match with GPT0.GTADTRA	1	1	0	0	1	0
	GTADTRB0N	Compare match with GPT0.GTADTRB	1	1	0	0	1	1
	GTADTRA1N	Compare match with GPT1.GTADTRA	1	1	0	1	0	0
	GTADTRB1N	Compare match with GPT1.GTADTRB	1	1	0	1	0	1
	GTADTRA2N	Compare match with GPT2.GTADTRA	1	1	0	1	1	0
	GTADTRB2N	Compare match with GPT2.GTADTRB	1	1	0	1	1	1
	GTADTRA3N	Compare match with GPT3.GTADTRA	1	1	1	0	0	0
	GTADTRB3N	Compare match with GPT3.GTADTRB	1	1	1	0	0	1
	GTADTRA0N or GTADTRB0N	Compare match with GPT0.GTADTRA or GPT0.GTADTRB	1	1	1	0	1	0
	GTADTRA1N or GTADTRB1N	Compare match with GPT1.GTADTRA or GPT1.GTADTRB	1	1	1	0	1	1
	GTADTRA2N or GTADTRB2N	Compare match with GPT2.GTADTRA or GPT2.GTADTRB	1	1	1	1	0	0
	GTADTRA3N or GTADTRB3N	Compare match with GPT3.GTADTRA or GPT3.GTADTRB	1	1	1	1	0	1

GCADIE Bit (Group C Scan End Interrupt Enable)

This bit enables or disables scan end interrupt generation for group C. A scan end interrupt for group C is provided individually for each unit. Table 31.11 shows the relationship between each unit and the scan end interrupt for group C.

Table 31.11 Relationship between Each Unit and Group C Scan End Interrupt

Unit	Group C Scan End Interrupt
S12AD	GCADI
S12AD1	GCADI1
S12AD2	GCADI2

GRCE Bit (Group C A/D Conversion Operation Enable)

When using group C in group scan mode, set the GRCE bit to 1.

When the GRCE bit is 0, trigger input for group C is disabled.

During group priority operation (the ADGSPCR.PGS bit is 1) with group C used, when the ADGSPCR.GBRP bit is set to 1, single scan for group C is continuously operated. When the GRCE bit is set to 1, single scan for group B is not continuously operated.

The GRCE bit should be set while the ADCSR.ADST bit is 0.

31.2.17 A/D Sampling State Register n (ADSSTRn) (n = 0 to 11, L, O)

Address(es): S12AD.ADSSTRL 0008 90DDh,
S12AD.ADSSTR0 0008 90E0h, S12AD.ADSSTR1 0008 90E1h, S12AD.ADSSTR2 0008 90E2h,
S12AD.ADSSTR3 0008 90E3h,
S12AD1.ADSSTRL 0008 92DDh,
S12AD1.ADSSTR0 0008 92E0h, S12AD1.ADSSTR1 0008 92E1h, S12AD1.ADSSTR2 0008 92E2h,
S12AD1.ADSSTR3 0008 92E3h,
S12AD2.ADSSTRO 0008 94DFh,
S12AD2.ADSSTR0 0008 94E0h, S12AD2.ADSSTR1 0008 94E1h, S12AD2.ADSSTR2 0008 94E2h,
S12AD2.ADSSTR3 0008 94E3h, S12AD2.ADSSTR4 0008 94E4h, S12AD2.ADSSTR5 0008 94E5h,
S12AD2.ADSSTR6 0008 94E6h, S12AD2.ADSSTR7 0008 94E7h, S12AD2.ADSSTR8 0008 94E8h,
S12AD2.ADSSTR9 0008 94E9h, S12AD2.ADSSTR10 0008 94EAh, S12AD2.ADSSTR11 0008 94EBh

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	1	1	0	1

The ADSSTRn register sets the sampling time for analog input.
If one state is one ADCLK (A/D conversion clock) cycle and the ADCLK clock is 40 MHz, one state is 25 ns. The initial value is 13 states. If the impedance of analog input signal source is too high to secure sufficient sampling time or if the ADCLK clock is slow, the sampling time can be adjusted. The ADSSTRn register should be set while the ADCSR.ADST bit is 0. The lower-limit value for sampling time differs depending on the PCLK to ADCLK frequency ratio.
Set a value that is 5 states or more when PCLK to ADCLK frequency ratio = 1:1, 2:1, 4:1, or 8:1.
Set a value that is 6 states or more when PCLK to ADCLK frequency ratio = 1:2.

Table 31.12 shows the relationship between the A/D sampling state register and the relevant channels.
For details, refer to section 31.3.5, Analog Input Sampling Time and Scan Conversion Time.

Table 31.12 Relationship between A/D Sampling State Register and Relevant Channels

Unit	Register Name	Relevant Channels
S12AD	ADSSTR0 register	AN000, Self-Diagnosis
	ADSSTR1 register	AN001
	ADSSTR2 register	AN002
	ADSSTR3 register	AN003
	ADSSTRL register	AN016
S12AD1	ADSSTR0 register	AN100, Self-Diagnosis
	ADSSTR1 register	AN101
	ADSSTR2 register	AN102
	ADSSTR3 register	AN103
	ADSSTRL register	AN116
S12AD2	ADSSTR0 register	AN200, Self-Diagnosis
	ADSSTR1 register	AN201
	ADSSTR2 register	AN202
	ADSSTR3 register	AN203
	ADSSTR4 register	AN204
	ADSSTR5 register	AN205
	ADSSTR6 register	AN206
	ADSSTR7 register	AN207
	ADSSTR8 register	AN208
	ADSSTR9 register	AN209
	ADSSTR10 register	AN210
	ADSSTR11 register	AN211
	ADSSTRO register	Internal reference voltage*1

Note 1. When performing A/D conversion of the internal reference voltage, the sampling time should be 5 µs or longer.

31.2.18 A/D Sample-and-Hold Circuit Control Register (ADSHCR)

Address(es): S12AD1.ADSHCR 0008 9266h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SHANS[2:0]			SSTSH[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	SSTSH[7:0]	Channel-Dedicated Sample-and-Hold Circuit Sampling Time Setting	Set the sampling time (4 to 255 states).	R/W
b10 to b8	SHANS[2:0]	Channel-Dedicated Sample-and-Hold Circuit Bypass Select	Select whether to use or not use (bypass) AN100 to AN102 channel-dedicated sample-and-hold circuits. 0: Bypass the channel-dedicated sample-and-hold circuits. 1: Use the channel-dedicated sample-and-hold circuits.	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ADSHCR sets the parameters related to channel-dedicated sample-and-hold circuits.

SSTSH[7:0] Bits (Channel-Dedicated Sample-and-Hold Circuit Sampling Time Setting)

These bits set the sampling time for the channel-dedicated sample-and-hold circuits. If one state is one ADCLK (A/D conversion clock) cycle and the ADCLK clock is 40 MHz, one state is 25 ns. The initial value is 26 states. If the impedance of analog input signal source is too high to secure sufficient sampling time or if the ADCLK clock is slow, the sampling time can be adjusted. The SSTSH[7:0] bits should be set while the ADCSR.ADST bit is 0. The sampling time must be set to a value that is 4 states or more and is 255 or less.Also, the sampling state setting value should be at least the specified test condition in section 37.4, A/D Conversion Characteristics.

SHANS[2:0] Bits (Channel-Dedicated Sample-and-Hold Circuit Bypass Select)

These bits select whether to use or not use (bypass) AN100 to AN102 channel-dedicated sample-and-hold circuits. The SHANS[0] bit selects AN100, SHANS[1] bit selects AN101, and SHANS[2] bit selects AN102. The SHANS[2:0] bits should be set while the ADCSR.ADST bit is 0.

If any channel from among AN100 to AN102 is selected for group B or C while operation is in group scan mode under group priority control, make the setting to bypass the channel-dedicated sample-and-hold circuit.

31.2.19 A/D Disconnection Detection Control Register (ADDISCR)

Address(es): S12AD.ADDISCR 0008 907Ah, S12AD1.ADDISCR 0008 927Ah, S12AD2.ADDISCR 0008 947Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	ADNDIS[4:0]				
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	ADNDIS[4:0]	A/D Disconnection Detection Assist Setting	b4 ADNDIS[4]: Discharge/precharge selected 0: Discharge 1: Precharge b3 to b0 ADNDIS[3:0]: Discharge/precharge period	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ADDISCR sets the disconnection detection assist function.

ADNDIS[4:0] Bits (A/D Disconnection Detection Assist Setting)

These bits selects either precharge or discharge and the period of precharge/discharge for the A/D disconnection detection assist function. Setting the ADNDIS[4] bit = 1 allows to select precharge and setting the ADNDIS[4] bit = 0 allows to select discharge. The period of precharge/discharge can be set with the ADNDIS[3:0] bits. When the ADNDIS[3:0] bits = 0000b, the disconnection detection assist function is not effective. Setting of the ADNDIS[3:0] bits to 0001b is prohibited. Except for the case of ADNDIS[3:0] = 0000b or 0001b, the specified value indicates the number of states for the period of precharge/discharge. The ADNDIS[4:0] bits should be set when the ADCSR.ADST bit is 0. When ADNDIS[3:0] are set to any value other than 0000b and the disconnection detection assist function is enabled, the channel-dedicated disconnection detection assist function is also enabled. Be sure to secure the wait time for the sample-and-hold circuit when using the channel-dedicated disconnection detection assist function.
When the ADEXICR.OCSA bit is set to 1 to perform A/D conversion of the internal reference voltage, ADNDIS[4:0] are automatically fixed to 0Fh, and discharging is executed prior to A/D conversion (auto-discharging). An auto-discharge period of 15 ADCLK cycles is inserted before sampling each time the internal reference voltage is A/D-converted. However, A/D conversion of the internal reference voltage can be selected for S12AD2 only.

31.2.20 A/D Group Scan Priority Control Register (ADGSPCR)

Address(es): S12AD.ADGSPCR 0008 9080h, S12AD1.ADGSPCR 0008 9280h, S12AD2.ADGSPCR 0008 9480h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	GBRP	LGRRS	—	—	—	—	—	—	—	—	—	—	—	—	GBRSCN	PGS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	PGS	Group Priority Control Setting*1	0: Operation is without group priority control 1: Operation is with group priority control	R/W
b1	GBRSCN	Low-Priority Group Restart Setting*2	(Enabled only when PGS = 1. Reserved when PGS = 0.) 0: Scanning for the group is not restarted after having been discontinued due to group priority control. 1: Scanning for the group is restarted after having been discontinued due to group priority control.	R/W
b13 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b14	LGRRS	Restart Channel Select	(Enabled when PGS = 1 and GBRSCN = 1. Reserved when PGS = 0 or GBRSCN = 0.) 0: Scanning is restarted from the scan start channel. 1: Scanning is restarted from the channel on which A/D conversion is not completed.	R/W
b15	GBRP	Single Scan Continuous Start*3	(Enabled only when PGS = 1. Reserved when PGS = 0.) 0: Single scan is not continuously activated. 1: Single scan for the lowest-priority group is continuously activated.	R/W

Note 1. When the PGS bit is to be set to 1, the ADCSR.ADCS[1:0] bits must be set to 01b (group scan mode). If the bits are set to any other values, proper operation is not guaranteed.
Note 2. When the GBRSCN bit is to be set to 1, the frequency ratio of peripheral module clock PCLK to A/D conversion clock ADCLK should be set to 1:1.
Note 3. When the GBRP bit has been set to 1, single scan is performed continuously for the lowest-priority group regardless of the setting of the GBRSCN bit.

ADGSPCR is used to discontinue scanning of the low-priority group and make settings for priority control of scanning for the priority group in group scan mode.
For the settings on group priority operation, see Table 31.14 and Table 31.15.

PGS Bit (Group Priority Control Setting)

This bit sets the priority of operation in group scan mode. Set this bit to 1 when giving priority to operation on the group. When the PGS bit is to be set to 1, the ADCSR.ADCS[1:0] bits must be set to 01b (group scan mode).
During group priority operation, a trigger to start scanning for the priority group is accepted during scan for the low-priority group, and scan for the priority group is started after scan for the low-priority group was discontinued. The priority order is group A > group B > group C.
When a trigger to start scanning for group B is accepted during scan for group C, group C scan is discontinued, and scan for group B is started. When a trigger to start scanning for group A is accepted during scan for group C, group C scan is discontinued, and scan for group A is started.
Likewise, when a trigger to start scanning for group A is accepted during scan for group B, group B scan is discontinued and scan for group A is started.
When setting the PGS bit to 0, clearing should be performed by software according to section 31.6.2, Notes on Stopping A/D Conversion. When setting the PGS bit to 1, follow the procedure described in section 31.3.4.3, Operation under Group Priority Control.

GBRSCN Bit (Low-Priority Group Restart Setting)

This bit controls the restarting of scan operation during group priority control.
If a scan operation on the low-priority group has been stopped by a priority group trigger input with the GBRSCN bit set to 1, the scan operation is restarted after the scanning of the priority group is completed. Also, if a low-priority trigger is input during scan for the priority group, the scan operation on the low-priority group is restarted after the scan for the priority group is completed.
If the GBRSCN bit has been set to 0, triggers that are input during A/D conversion are ignored. Also, the ADCSR.ADST bit must be 0 when the GBRSCN bit is to be set.
The setting of the GBRSCN bit is enabled when the PGS bit is set to 1.

LGRRS Bit (Restart Channel Select)

This bit sets the channel on which scan is restarted during group priority control. The setting of the LGRRS bit is enabled when the PGS and GBRSCN bits are set to 1.
If a scan operation on the low-priority group has been stopped due to group priority operation with the LGRRS bit set to 0, the scan operation is restarted from the start channel after the scan for the priority group is completed.
If a scan operation on the low-priority group has been stopped due to group priority operation with the LGRRS bit set to 1, the scan operation is restarted*1 on the channel on which A/D conversion is not competed after the scan for the priority group is completed.
The LGRRS bit should be set while the ADCSR.ADST bit is 0.

Note 1. If A/D conversion on the addition set channel is not completed for the set number of times when scanning is stopped, A/D conversion on the channel is restarted for the set number of times when scanning is restarted.

GBRP Bit (Single Scan Continuous Start)

This bit is set when the lowest-priority group is continuously operated in single scan mode while group priority operation is set. The lowest-priority group is group C when groups A, B, and C are used; group B when groups A and B are used.
Setting the GBRP bit to 1 starts a single scan on the lowest-priority group. On completion of the scan, another single scan on the lowest-priority group is automatically started.
If scanning has been stopped due to group priority operation, single scan on the lowest-priority group is automatically restarted on completion of the A/D conversion on the priority group.
Disable the trigger input for the lowest-priority group before setting the GBRP bit to 1. When the GBRP bit is set to 1, only the lowest-priority group is scanned again even if the GBRSCN bit is 0.
The ADCSR.ADST bit must be 0 when the GBRP bit is to be set.
The setting of the GBRP bit is enabled when the PGS bit is 1.

31.2.21 A/D Programmable Gain Amplifier Control Register (ADPGACR)

(1) S12AD.ADPGACR

Address(es): 0008 91A0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	P000ENAMP	P000SEL1	—
Value after reset:	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b1	P000SEL1	PGA P000 Amplifier Pass-Through Enable	0: Does not pass through the amplifier in the PGA. 1: Passes through the amplifier in the PGA.	R/W
b2	P000ENAMP	PGA P000 Amplifier Enable	0: Does not use the amplifier in the PGA. 1: Uses the amplifier in the PGA.	R/W
b4, b3	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b6, b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8, b7	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b10, b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12, b11	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b14, b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	—	Reserved	This bit is read as 1. The write value should be 1.	R/W

The S12AD.ADPGACR register is used to set whether or not to use programmable gain amplifier P000 of unit 0.

P000SEL1 Bit (PGA P000 Amplifier Pass-Through Enable)

This bit is used to select whether or not to pass through the amplifier in programmable gain amplifier P000 of unit 0.

P000ENAMP Bit (PGA P000 Amplifier Enable)

This bit is used to select whether or not to use the amplifier in programmable gain amplifier P000 of unit 0.

(2) S12AD1.ADPGACR

Address(es): 0008 93A0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	P102ENAMP	P102SEL1	—	—	P101ENAMP	P101SEL1	—	—	P100ENAMP	P100SEL1	—
Value after reset:	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b1	P100SEL1	PGA P100 Amplifier Pass-Through Enable	0: Does not pass through the amplifier in the PGA. 1: Passes through the amplifier in the PGA.	R/W
b2	P100ENAMP	PGA P100 Amplifier Enable	0: Does not use the amplifier in the PGA. 1: Uses the amplifier in the PGA.	R/W
b4, b3	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b5	P101SEL1	PGA P101 Amplifier Pass-Through Enable	0: Does not pass through the amplifier in the PGA. 1: Passes through the amplifier in the PGA.	R/W
b6	P101ENAMP	PGA P101 Amplifier Enable	0: Does not use the amplifier in the PGA. 1: Uses the amplifier in the PGA.	R/W
b8, b7	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b9	P102SEL1	PGA P102 Amplifier Pass-Through Enable	0: Does not pass through the amplifier in the PGA. 1: Passes through the amplifier in the PGA.	R/W
b10	P102ENAMP	PGA P102 Amplifier Enable	0: Does not use the amplifier in the PGA. 1: Uses the amplifier in the PGA.	R/W
b12, b11	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b14, b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	—	Reserved	This bit is read as 1. The write value should be 1.	R/W

The S12AD1.ADPGACR register is used to set whether or not use programmable gain amplifiers P100 to P102 of unit 1.

P100SEL1 Bit (PGA P100 Amplifier Pass-Through Enable)

This bit is used to select whether or not to pass through the amplifier in programmable gain amplifier P100 of unit 1.

P100ENAMP Bit (PGA P100 Amplifier Enable)

This bit is used to select whether or not to use the amplifier in programmable gain amplifier P100 of unit 1.

P101SEL1 Bit (PGA P101 Amplifier Pass-Through Enable)

This bit is used to select whether or not to pass through the amplifier in programmable gain amplifier P101 of unit 1.

P101ENAMP Bit (PGA P101 Amplifier Enable)

This bit is used to select whether or not to use the amplifier in programmable gain amplifier P101 of unit 1.

P102SEL1 Bit (PGA P102 Amplifier Pass-Through Enable)

This bit is used to select whether or not to pass through the amplifier in programmable gain amplifier P102 of unit 1.

P102ENAMP Bit (PGA P102 Amplifier Enable)

This bit is used to select whether or not to use the amplifier in programmable gain amplifier P102 of unit 1.

31.2.22 A/D Programmable Gain Amplifier Gain Setting Register 0 (ADPGAGS0)

(1) S12AD.ADPGAGS0

Address(es): 0008 91A2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	P000GAIN[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	P000GAIN[3:0]	PGA P000 Gain Setting	The relationship between each setting and the gain is as follows: b3 b0 0 0 0 0: × 2.000 0 0 0 1: × 2.500 0 1 0 0: × 3.077 0 1 1 0: × 3.636 0 1 1 1: × 4.000 1 0 0 0: × 4.444 1 0 0 1: × 5.000 1 0 1 1: × 6.667 1 1 0 0: × 8.000 1 1 0 1: × 10.000 1 1 1 0: × 13.333 Settings other than above are prohibited.	R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The S12AD.ADPGAGS0 register is used to set the gain of programmable gain amplifier P000 of unit 0.

P000GAIN[3:0] Bits (PGA P000 Gain Setting)

These bits are used to set the gain of programmable gain amplifier P000 of unit 0.

(2) S12AD1.ADPGAGS0

Address(es): 0008 93A2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	P102GAIN[3:0]				P101GAIN[3:0]				P100GAIN[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	P100GAIN[3:0]	PGA P100 Gain Setting	The relationship between each setting and the gain is as follows: b3 b0 0 0 0 0: × 2.000 0 0 0 1: × 2.500 0 1 0 0: × 3.077 0 1 1 0: × 3.636 0 1 1 1: × 4.000 1 0 0 0: × 4.444 1 0 0 1: × 5.000 1 0 1 1: × 6.667 1 1 0 0: × 8.000 1 1 0 1: × 10.000 1 1 1 0: × 13.333 Settings other than above are prohibited.	R/W
b7 to b4	P101GAIN[3:0]	PGA P101 Gain Setting		
b11 to b8	P102GAIN[3:0]	PGA P102 Gain Setting		
b15 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The S12AD.ADPGAGS0 register is used to set the gain of programmable gain amplifiers P100 to P102 of unit 1.

P100GAIN[3:0] Bits (PGA P100 Gain Setting)

These bits are used to set the gain of programmable gain amplifier P100 of unit 1.

P101GAIN[3:0] Bits (PGA P101 Gain Setting)

These bits are used to set the gain of programmable gain amplifier P101 of unit 1.

P102GAIN[3:0] Bits (PGA P102 Gain Setting)

These bits are used to set the gain of programmable gain amplifier P102 of unit 1.

31.3 Operation

31.3.1 Scanning Operation

In scanning, A/D conversion is performed sequentially on the analog inputs of the specified channels.
A scan conversion is performed in three operating modes: single scan mode, continuous scan mode, and group scan mode. In single scan mode, one or more specified channels are scanned once. In continuous scan mode, one or more specified channels are scanned repeatedly until the ADCSR.ADST bit is cleared to 0 from 1 by software. In group scan mode, the selected channels of groups A, B, and C are scanned once after starting to be scanned according to the respective synchronous trigger.
In single scan mode and continuous scan mode, A/D conversion is performed for ANn channels selected by the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n. In group scan mode, A/D conversion is performed for ANn channels of groups A, B, and C selected by the ADANSA0 and ADANSA1 registers, ADANSB0 and ADANSB1 registers, and ADANSC0 and ADANSC1 registers, respectively, starting from the channel with the smallest number n.
When self-diagnosis is selected, it is executed once at the beginning of each scan and one of the three voltages internally generated in the 12-bit A/D converter is converted.
Double trigger mode is to be used with single scan mode or group scan mode. With double trigger mode being enabled, A/D conversion data of a channel selected by the ADCSR.DBLANS[4:0] bits is duplicated only if the conversion is started by the synchronous trigger selected by the ADSTRGR.TRSA[5:0] bits. In group scan mode, the double trigger function can be used only for group A.
Extended double trigger mode indicates a state when the following synchronous trigger (two synchronous trigger sources enabled) is selected by the TRSA[5:0] bits in the A/D conversion start trigger select register (ADSTRGR) in double trigger mode.

- TRG4AN or TRG4BN (the ADSTRGR.TRSA[5:0] bits are set to 001011b)
- TRG7AN or TRG7BN (the ADSTRGR.TRSA[5:0] bits are set to 001111b)
- TRGA0N or TRG0N (the ADSTRGR.TRSA[5:0] bits are set to 011001b)
- TRGA9N or TRG9N (the ADSTRGR.TRSA[5:0] bits are set to 011010b)
- TRGA0N or TRGA9N (the ADSTRGR.TRSA[5:0] bits are set to 011011b)
- TRG0N or TRG9N (the ADSTRGR.TRSA[5:0] bits are set to 011100b)
- GTADTRA0N or GTADTRB0N (the ADSTRGR.TRSA[5:0] bits are set to 111010b)
- GTADTRA1N or GTADTRB1N (the ADSTRGR.TRSA[5:0] bits are set to 111011b)
- GTADTRA2N or GTADTRB2N (the ADSTRGR.TRSA[5:0] bits are set to 111100b)
- GTADTRA3N or GTADTRB3N (the ADSTRGR.TRSA[5:0] bits are set to 111101b)

In extended double trigger mode, in addition to normal operations in double trigger mode, A/D conversion data is stored in A/D data duplication register A (ADDBLDRA) or A/D data duplication register B (ADDBLDRB) depending on the trigger type. If two types of triggers have occurred simultaneously in this mode, A/D conversion data is not sorted by the trigger sources and is stored in data duplication register B (ADDBLDRB).
Note that if a new trigger is input during A/D conversion caused by another trigger, the new trigger is ignored.
When any of AN100 to AN102 channels is set as a channel-dedicated sample-and-hold circuit by the S12AD1.ADSHCR.SHANS[2:0] bits, the target analog input is sampled and held before the first A/D conversion of each scan.
The ADST0 output is used to output the S12AD.ADCSR.ADST bit state, the ADST1 output is used to output the S12AD1.ADCSR.ADST bit state, and the ADST2 output is used to output the S12AD2.ADCSR.ADST bit state.

31.3.2 Single Scan Mode

31.3.2.1 Basic Operation (Without Channel-Dedicated Sample-and-Hold Circuits)

In basic operation of single scan mode, A/D conversion is performed once on the analog input of the specified channels as below.

(1) When the ADCSR.ADST bit is set to 1 (A/D conversion start) by software, or synchronous or asynchronous trigger input, A/D conversion is performed for ANn channels selected by the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
(2) Each time A/D conversion of a single channel is completed, the A/D conversion result is stored into the corresponding A/D data register (ADDRy).
(3) When A/D conversion of all the selected channels is completed, a scan end interrupt request is generated if the ADCSR.ADIE bit is 1 (interrupt generation upon scanning completion enabled).
(4) The ADCSR.ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion of all the selected channels is completed. Then the 12-bit A/D converter enters a wait state.

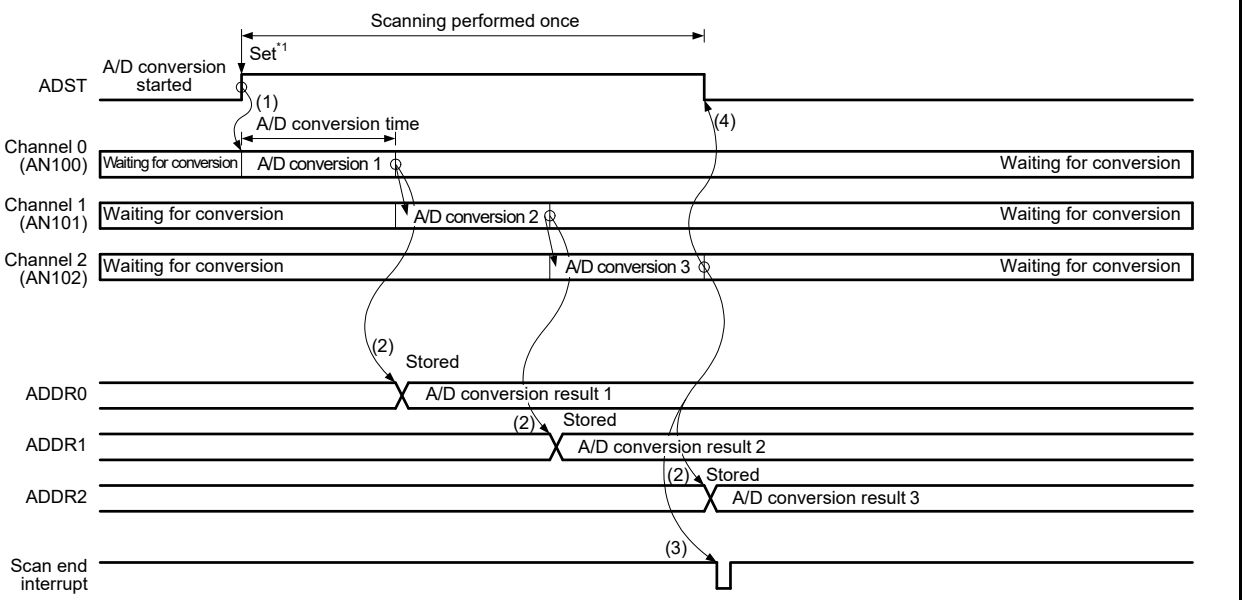


Figure 31.5 Example of Operation in Single Scan Mode (Basic Operation: AN100, AN101, AN102 Selected)

31.3.2.2 Basic Operation (With Channel-Dedicated Sample-and-Hold Circuits)

When a channel-dedicated sample-and-hold circuit is used, sample-and-hold operations are performed first, and this is followed by A/D conversion once of the analog inputs on all selected channels. The ADSHCR.SHANS[2:0] bits are used to select the channels for which the channel-dedicated sample-and-hold circuits are to be used.

(1) Analog input sampling of all channels for which the channel-dedicated sample-and-hold circuits are to be used is started when the ADCSR.ADST bit is set to 1 (A/D conversion start) by software, or synchronous or asynchronous trigger input.
(2) After sample-and-hold operation, A/D conversion is performed for ANn channels selected by the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
(3) Each time A/D conversion of a single channel is completed, the result of A/D conversion is stored in the corresponding A/D data register (ADDRy).
(4) When A/D conversion of all the selected channels is completed, a scan end interrupt request is generated if the ADCSR.ADIE bit is 1 (interrupt generation upon scanning completion enabled).
(5) The ADCSR.ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion of all the selected channels is completed. Then the 12-bit A/D converter enters a waiting state.

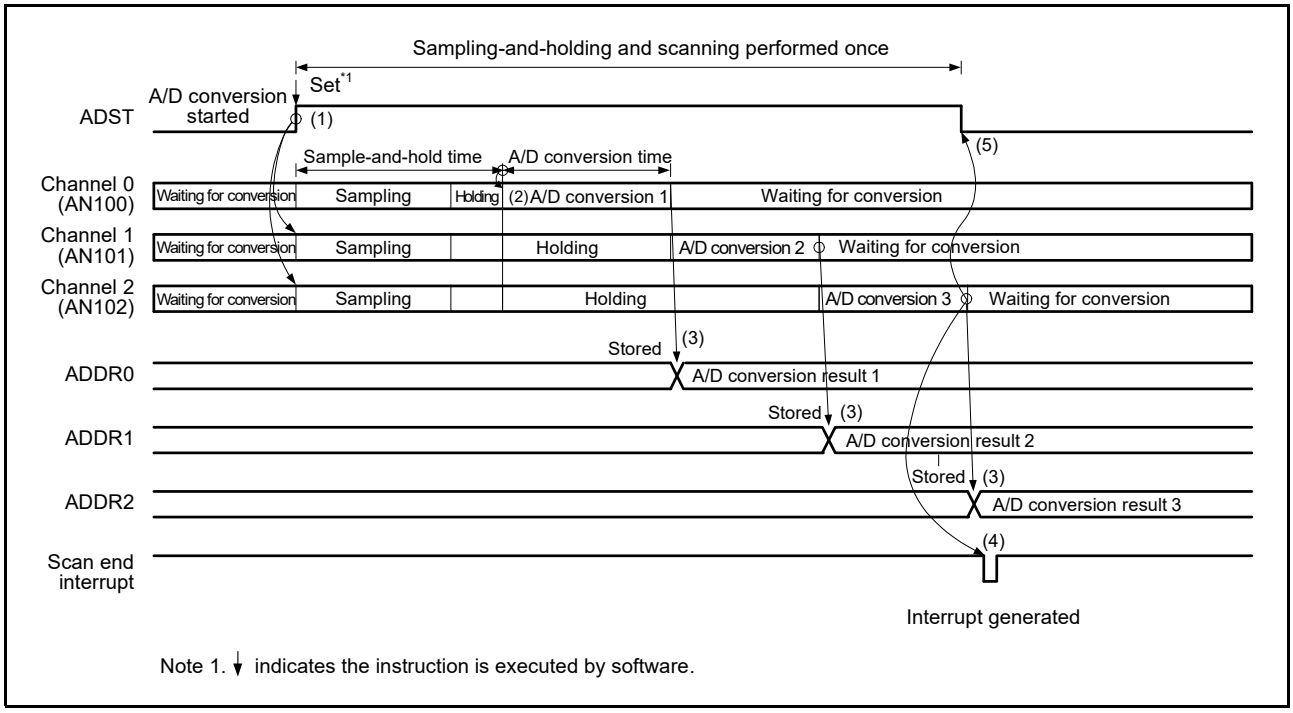


Figure 31.6 Example of Operation in Single Scan Mode (Channel-Dedicated Sample-and-Hold Circuits Used; AN100, AN101, AN102 Selected)

31.3.2.3 Channel Selection and Self-Diagnosis (Without Channel-Dedicated Sample-and-Hold Circuits)

When channels and self-diagnosis are selected, A/D conversion is performed once for the reference voltage supplied to the 12-bit A/D converter as below. After that, A/D conversion is performed only once on the analog input of the selected channels.

(1) A/D conversion for self-diagnosis is started when the ADCSR.ADST bit is set to 1 (A/D conversion start) by software, or synchronous or asynchronous trigger input.
(2) When A/D conversion for self-diagnosis is completed, A/D conversion result is stored into the A/D self-diagnosis data register (ADRD), and A/D conversion is performed for ANn channels selected by the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
(3) Each time A/D conversion of a single channel is completed, the A/D conversion result is stored into the corresponding A/D data register (ADDRy).
(4) When A/D conversion of all the selected channels is completed, a scan end interrupt request is generated if the ADCSR.ADIE bit is 1 (interrupt generation upon scanning completion enabled).
(5) The ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion of all the selected channels is completed. Then the 12-bit A/D converter enters a wait state.

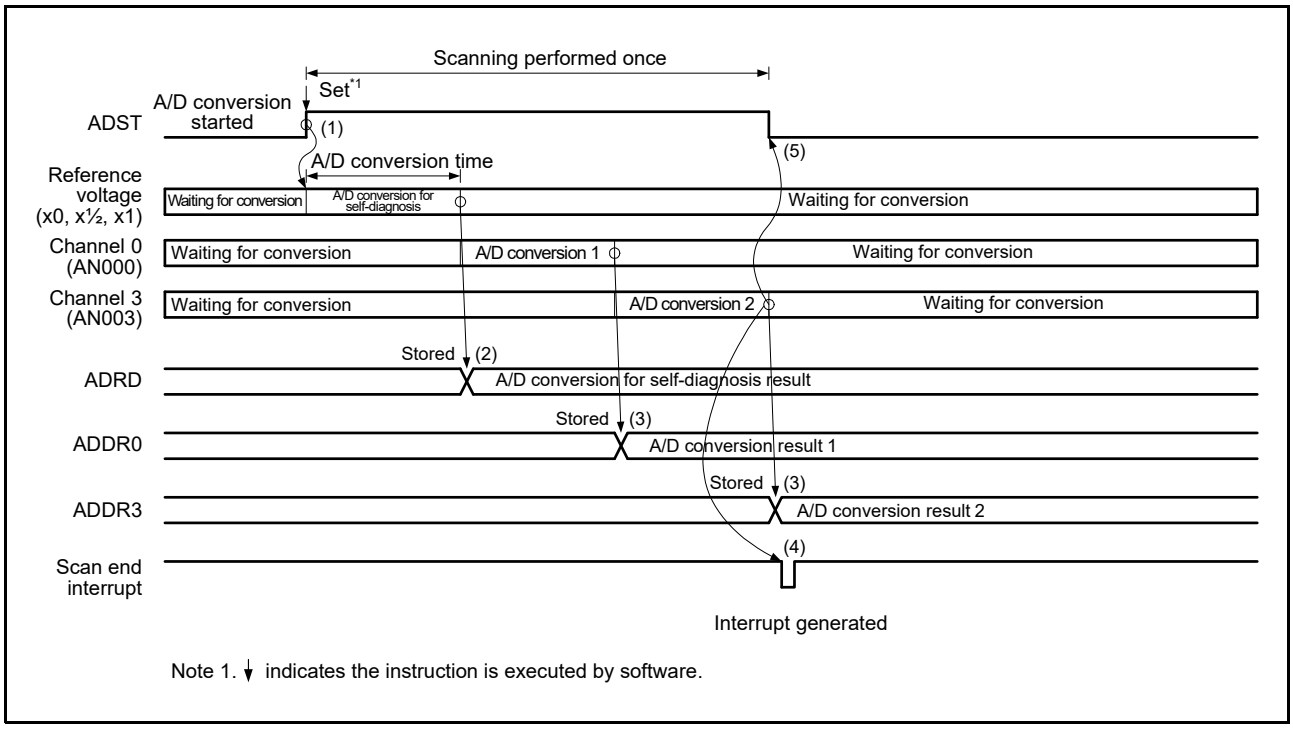


Figure 31.7 Example of Operation in Single Scan Mode (Basic Operation: AN000, AN003 Selected + Self-Diagnosis)

31.3.2.4 Channel Selection and Self-Diagnosis (With Channel-Dedicated Sample-and-Hold Circuits)

When channels and self-diagnosis are selected and a channel-dedicated sample-and-hold circuit is used, sample-and-hold operations are performed first, and A/D conversion is performed once for the reference voltage supplied to the 12-bit A/D converter as below. After that, A/D conversion is performed only once on the analog input of the selected channels.

(1) Analog input sampling of all channels for which the channel-dedicated sample-and-hold circuits are to be used is started when the ADCSR.ADST bit is set to 1 (A/D conversion start) by software, or synchronous or asynchronous trigger input.
(2) A/D conversion for self-diagnosis is started after completion of sampling and holding.
(3) When A/D conversion for self-diagnosis is completed, A/D conversion result is stored into the A/D self-diagnosis data register (ADRD), and A/D conversion is performed for ANn channels selected by the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
(4) Each time A/D conversion of a single channel is completed, the A/D conversion result is stored into the corresponding A/D data register (ADDRy).
(5) When A/D conversion of all the selected channels is completed, a scan end interrupt request is generated if the ADCSR.ADIE bit is 1 (interrupt upon scanning completion enabled).
(6) The ADCSR.ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion of all the selected channels is completed. Then the 12-bit A/D converter enters a wait state.

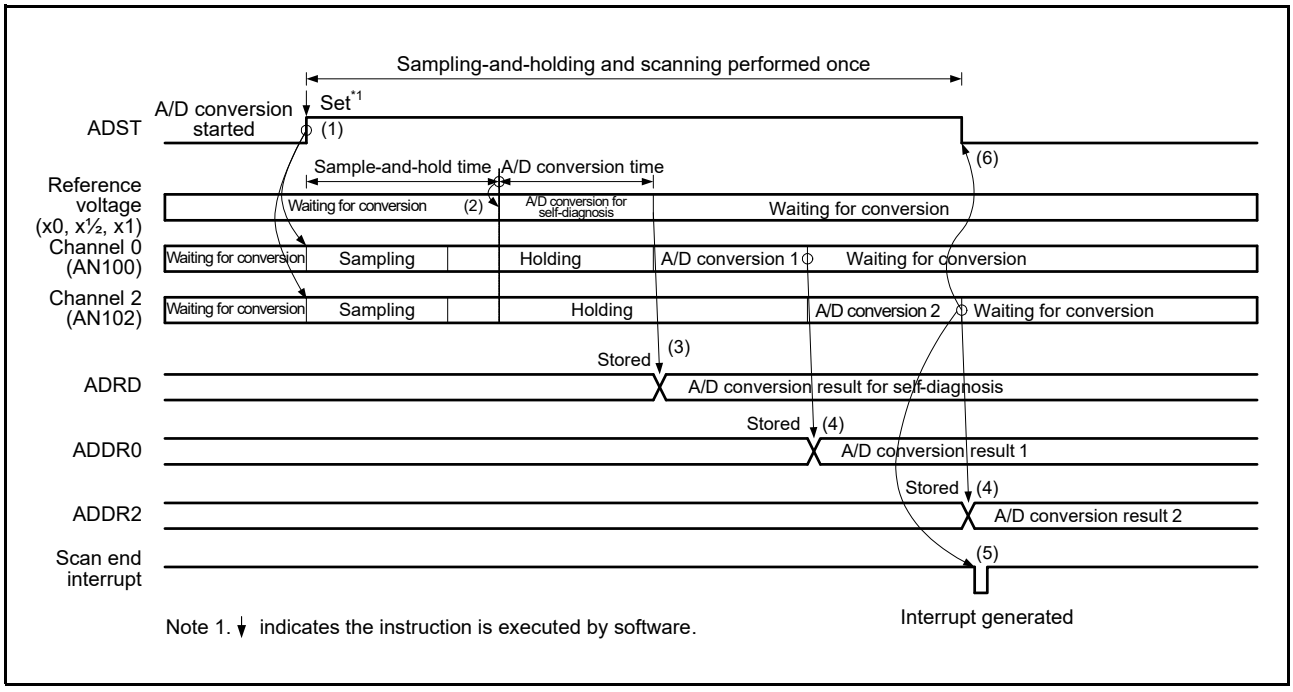


Figure 31.8 Example of Operation in Continuous Scan Mode (Channel-Dedicated Sample-and-Hold Circuits Used: AN100, AN102 Selected + Self-Diagnosis)

31.3.2.5 A/D Conversion of Internal Reference Voltage

A/D conversion of the internal reference voltage can be selected for S12AD2 only. A/D conversion of the internal reference voltage is performed in single scan mode as below.
All channels should be deselected (by setting the ADANSA0 and ADANSA1 register bits to all 0 and the ADCSR.DBLE bit to 0).

(1) Set the sampling time to 5 µs or longer.
(2) After switching to A/D conversion of the internal reference voltage, start A/D conversion by setting the ADST bit to 1.
(3) When A/D conversion is completed, the conversion result is stored into the A/D internal reference voltage data register (ADOCDR). If the ADCSR.ADIE bit is 1 (interrupt generation upon scanning completion enabled), a scan end interrupt request is generated.
(4) The ADST bit remains 1 during A/D conversion, and is automatically cleared to 0 upon completion of A/D conversion. Then the 12-bit A/D converter enters a wait state.

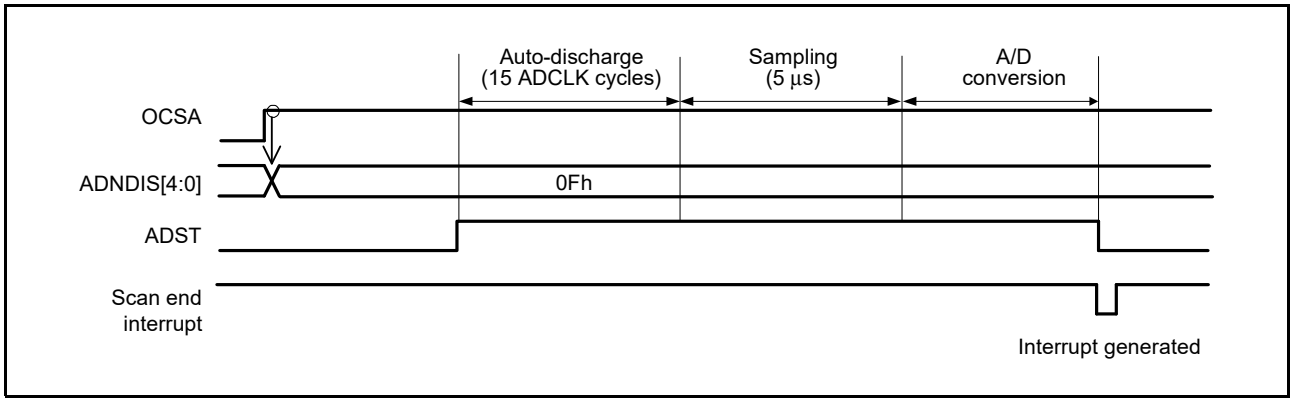


Figure 31.9 Example of Operation in Single Scan Mode (Internal Reference Voltage Selected: S12AD2 only)

31.3.2.6 A/D Conversion in Double Trigger Mode

In single scan mode with double trigger mode, single scan operation started by synchronous trigger is performed twice as below.

Self-diagnosis should be deselected, and the internal reference voltage A/D conversion select bit (S12AD2.ADEXICR.OCSA) should be set to 0.

Duplication of A/D conversion data is enabled by setting the channel numbers to be duplicated to the ADCSR.DBLANS[4:0] bits and setting the ADCSR.DBLE bit to 1. When the ADCSR.DBLE bit is set to 1, channel selection using the ADANSA0 and ADANSA1 registers is invalid. In double trigger mode, synchronous triggers should be selected using the ADSTRGR.TRSA[5:0] bits, the ADCSR.EXTRG bit should be set to 0, and the ADCSR.TRGE bit should be set to 1. Software trigger should not be used.

(1) When the ADCSR.ADST bit is set to 1 (A/D conversion start) by synchronous trigger input, A/D conversion is started on the single channel selected by the ADCSR.DBLANS[4:0] bits.
(2) When A/D conversion is completed, the A/D conversion result is stored into the corresponding A/D data register (ADDRy).
(3) The ADCSR.ADST bit is automatically cleared to 0 and the 12-bit A/D converter enters a wait state. Here, a scan end interrupt request is not generated irrespective of the ADCSR.ADIE bit setting (interrupt generation upon scanning completion enabled).
(4) When the ADCSR.ADST bit is set to 1 (A/D conversion start) by the second trigger input, A/D conversion is started on the single channel selected by the ADCSR.DBLANS[4:0] bits.
(5) When A/D conversion is completed, the A/D conversion result is stored into the A/D data duplication register (ADDBLDR), which is exclusively used in double trigger mode.
(6) If the ADCSR.ADIE bit is 1 (interrupt generation upon scanning completion enabled), a scan end interrupt request is generated.
(7) The ADCSR.ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion is completed. Then the 12-bit A/D converter enters a wait state.

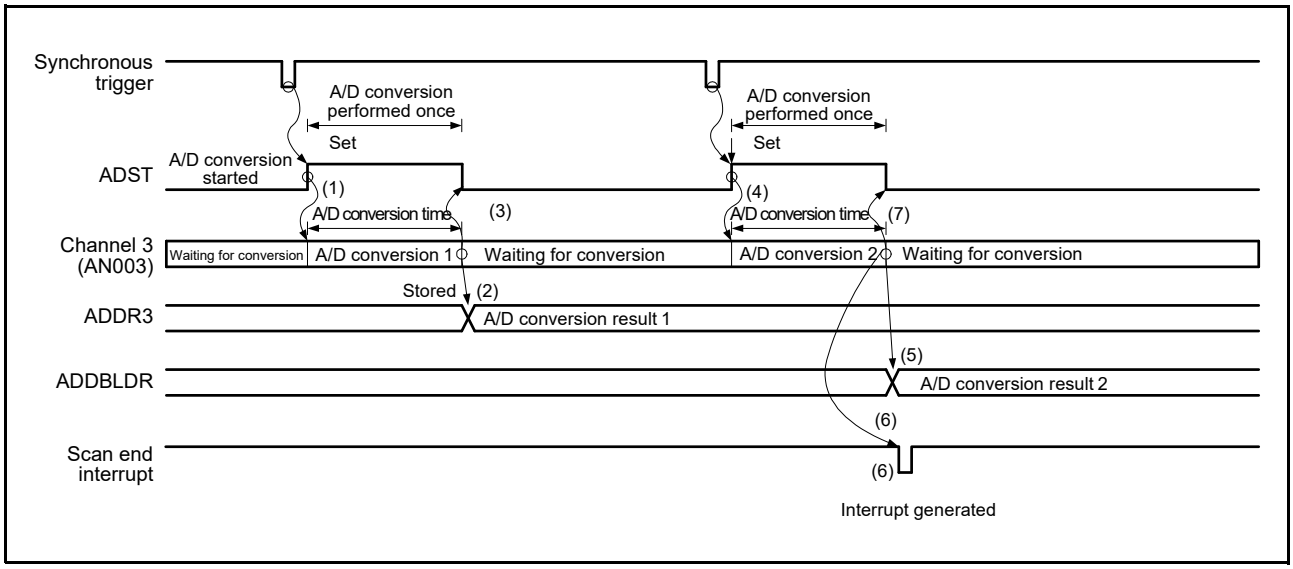


Figure 31.10 Example of Operation in Single Scan Mode (Double Trigger Mode Selected; AN003 Duplicated)

31.3.2.7 A/D Conversion in Extended Double Trigger Mode

When double trigger mode is selected in single scan mode, and TRG4AN or TRG4BN, TRG7AN or TRG7BN, TRGA0N or TRG0N, TRGA9N or TRG9N, TRGA0N or TRGA9N, or TRG0N or TRG9N, GTADTRA0N or GTADTRB0N, GTADTRA1N or GTADTRB1N, GTADTRA2N or GTADTRB2N, or GTADTRA3N or GTADTRB3N is selected by the TRSA[5:0] bits in the A/D conversion start trigger select register (ADSTRGR), single scan operation are performed twice as below.
Self-diagnosis should be deselected, and the internal reference voltage A/D conversion select bit (S12AD2.ADEXICR.OCSA) should be set to 0.
Duplication of A/D conversion data is enabled by setting the channel numbers to be duplicated to the ADCSR.DBLANS[4:0] bits and setting the ADCSR.DBLE bit to 1. When the ADCSR.DBLE bit is set to 1, channel selection using the ADANSA0 and ADANSA1 registers is invalid. In extended double trigger mode, the ADCSR.EXTRG bit should be set to 0, and the ADCSR.TRGE bit should be set to 1. Software trigger should not be used.

(1) When the ADCSR.ADST bit is set to 1 (A/D conversion start) by TRG4AN input, A/D conversion is started on the single channel selected by the ADCSR.DBLANS[4:0] bits.
(2) When A/D conversion is completed, the A/D conversion result is stored into the corresponding A/D data register (ADDRy) and A/D data-duplication register A (ADDBLDRA).
(3) The ADCSR.ADST bit is automatically cleared to 0 and the 12-bit A/D converter enters a wait state. Here, a scan end interrupt request is not generated irrespective of the ADCSR.ADIE bit setting (interrupt generation upon scanning completion enabled).
(4) When the ADCSR.ADST bit is set to 1 (A/D conversion start) by TRG4BN input, A/D conversion is started on the single channel selected by the ADCSR.DBLANS[4:0] bits.
(5) When A/D conversion is completed, the A/D conversion result is stored into A/D data duplication register (ADDBLDR) and A/D data duplication register B (ADDBLDRB).
(6) If the ADCSR.ADIE bit is 1 (interrupt generation upon scanning completion enabled), a scan end interrupt request is generated.
(7) The ADCSR.ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion is completed. Then the 12-bit A/D converter enters a wait state.

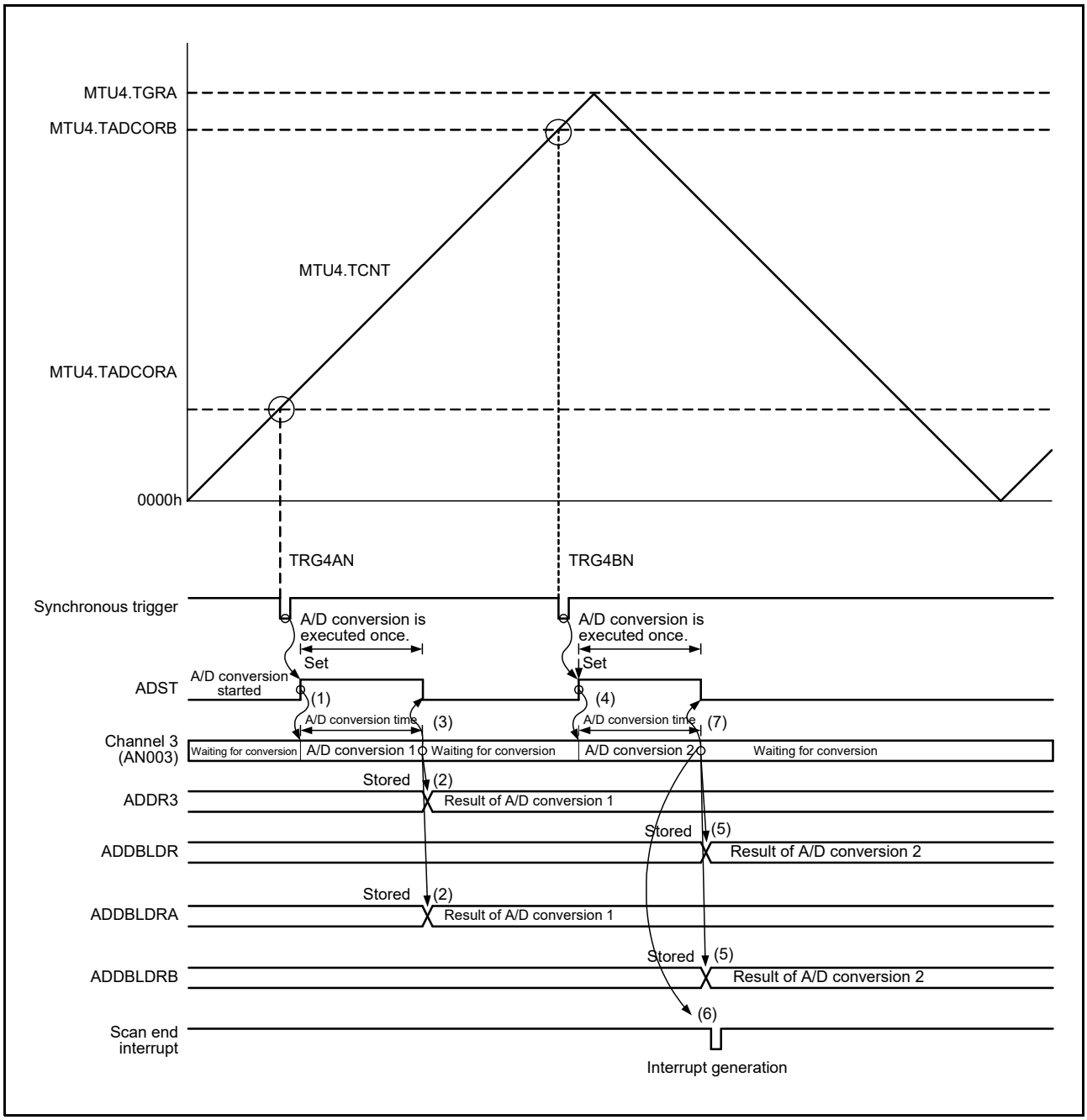


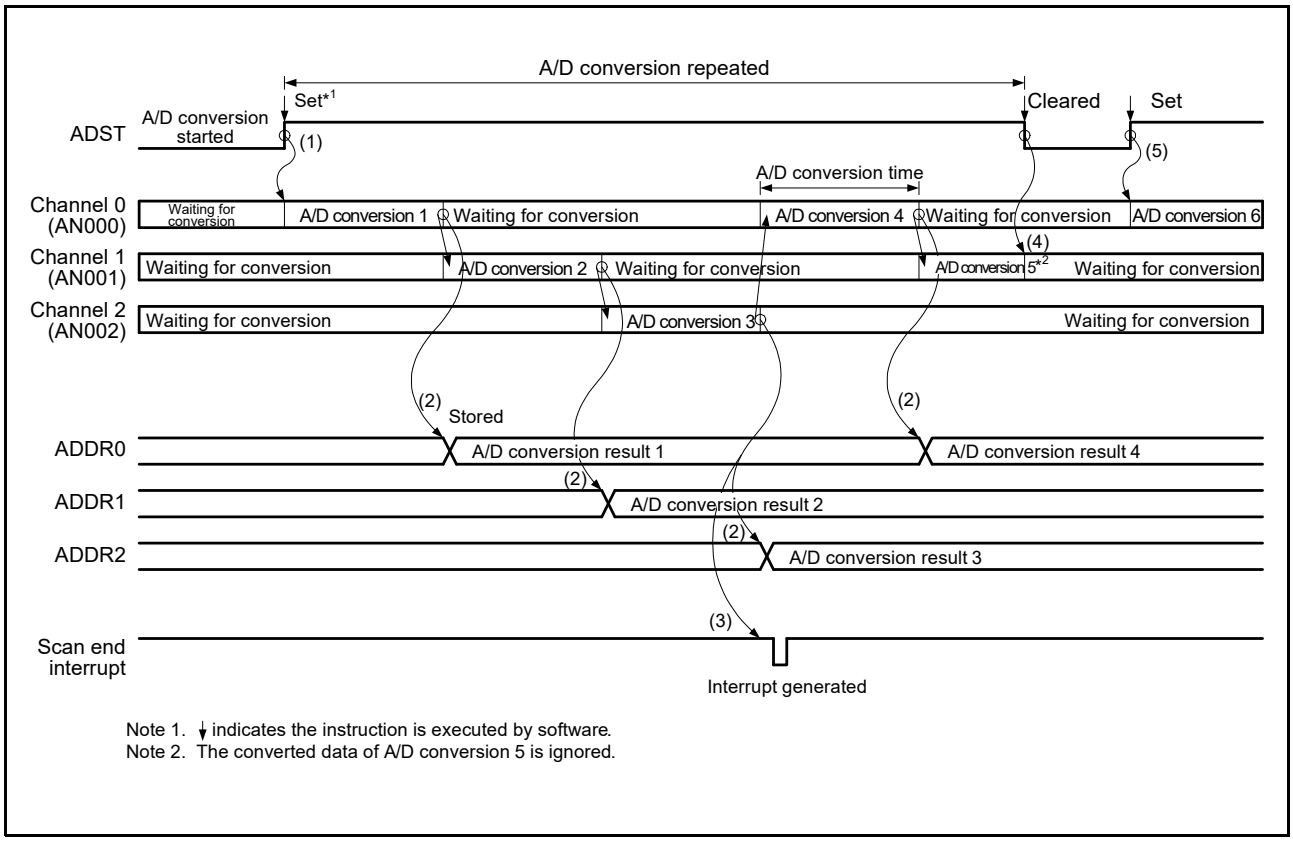
Figure 31.11 Example of Extended Operation in Double Trigger Mode (1)
(Duplication Selected for AN003, TRG4AN or TRG4BN Selected, First Trigger is TRG4AN)

31.3.3 Continuous Scan Mode

31.3.3.1 Basic Operation (Without Channel-Dedicated Sample and-Hold Circuits)

In basic operation of continuous scan mode, A/D conversion is performed repeatedly on the analog input of the specified channels as below.
In continuous scan mode, the internal reference voltage A/D conversion select bit (S12AD2.ADEXICR.OCSA) should be set to 0 (deselected).

(1) When the ADCSR.ADST bit is set to 1 (A/D conversion start) by software, or synchronous or asynchronous trigger input, A/D conversion is performed for ANn channels selected by the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
(2) Each time A/D conversion of a single channel is completed, the A/D conversion result is stored into the corresponding A/D data register (ADDRy).
(3) When A/D conversion of all the selected channels is completed, a scan end interrupt request is generated if the ADCSR.ADIE bit is 1 (interrupt generation upon scanning completion enabled).
The 12-bit A/D converter sequentially starts A/D conversion for ANn channels selected by the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
(4) The ADCSR.ADST bit is not automatically cleared to 0 and steps 2 and 3 are repeated as long as the bit remains 1 (A/D conversion start). When the ADCSR.ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the 12-bit A/D converter enters a wait state.
(5) When the ADST bit is later set to 1 (A/D conversion start), A/D conversion is started again for ANn channels selected by the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.



Note 1. ↓ indicates the instruction is executed by software.
Note 2. The converted data of A/D conversion 5 is ignored.

Figure 31.12 Example of Operation in Continuous Scan Mode (Basic Operation: AN000 to AN002 Selected)

31.3.3.2 Basic Operation (With Channel-Dedicated Sample-and-Hold Circuits)

When a channel-dedicated sample-and-hold circuit is used, sample-and-hold operations are performed first, after which the analog inputs on all selected channels are A/D converted as below. The channels for which the channel-dedicated sample-and-hold circuits are to be used can be selected by the ADSHCR.SHANS[2:0] bits.
In continuous scan mode, the internal reference voltage A/D conversion select bit (S12AD2.ADEXICR.OCSA) should be set to 0 (deselected).

(1) Analog input sampling of all channels for which the channel-dedicated sample-and-hold circuits are to be used is started when the ADCSR.ADST bit is set to 1 (A/D conversion start) by software, synchronous trigger input, or asynchronous trigger input.
(2) After sample-and-hold operation, A/D conversion is performed for ANn channels selected by the ADANSA0, ADANSA1 registers, starting from the channel with the smallest number n.
(3) Each time A/D conversion of a single channel is completed, the result of A/D conversion is stored in the corresponding A/D data register (ADDRy).
(4) When A/D conversion of all the selected channels is completed, a scan end interrupt request is generated if the ADCSR.ADIE bit is 1 (interrupt generation upon scanning completion enabled). At the same time, analog input sampling is started for all the channels for which the channel-dedicated sample-and-hold circuits are to be used.
(5) The ADCSR.ADST bit is not automatically cleared and steps 2 to 4 are repeated as long as the bit remains 1. When the ADCSR.ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the 12-bit A/D converter enters a wait state.
(6) When the ADCSR.ADST bit is then set to 1 (A/D conversion start), analog input sampling is started again for all the channels for which the channel-dedicated sample-and-hold circuits are to be used.

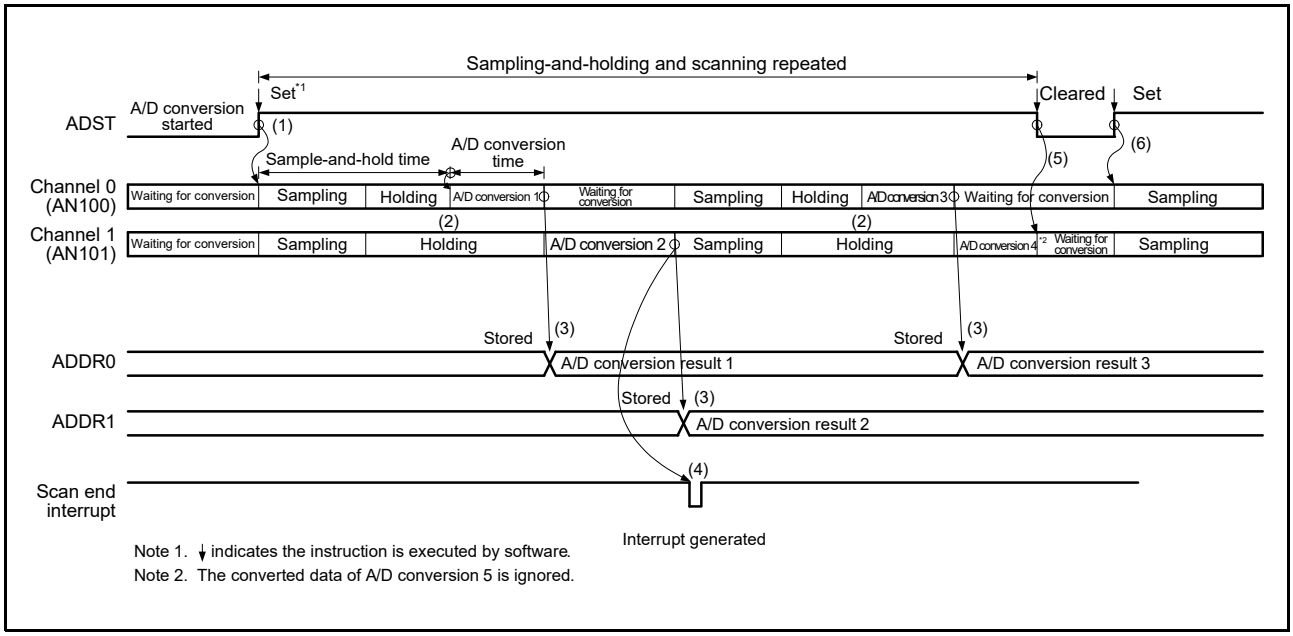
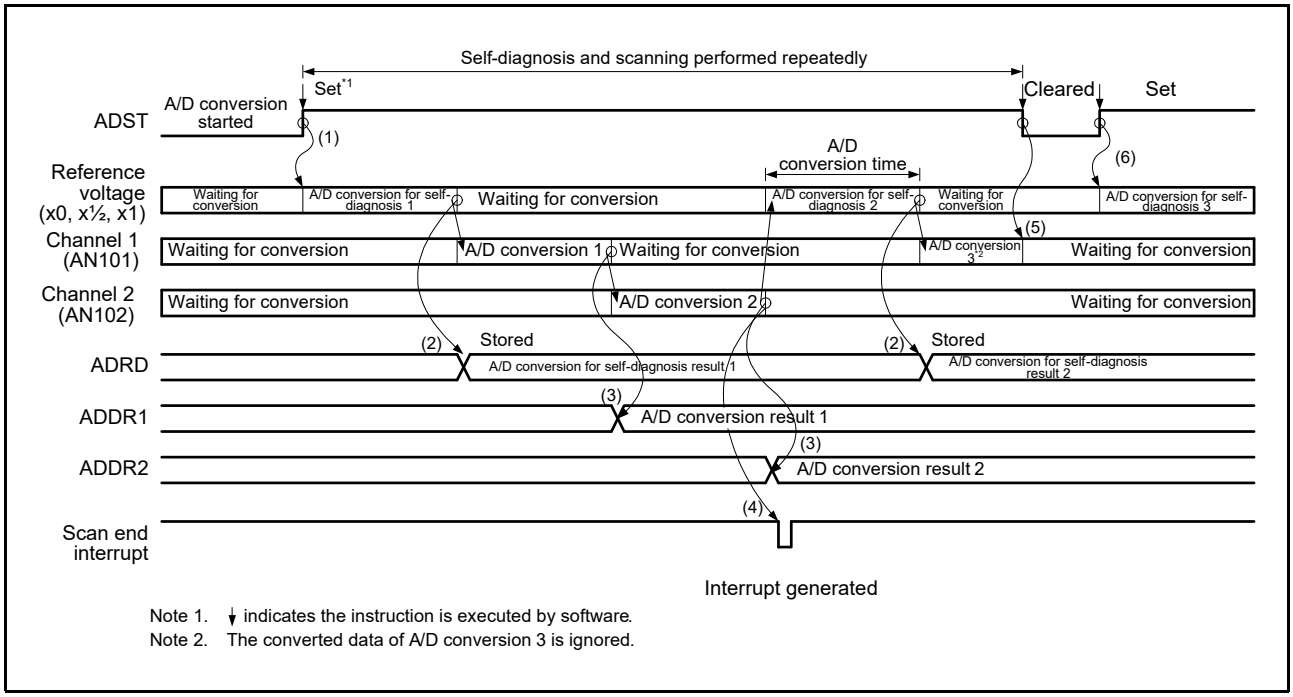


Figure 31.13 Example of Operation in Continuous Scan Mode (Channel-Dedicated Sample-and-Hold Circuits Used)

31.3.3.3 Channel Selection and Self-Diagnosis (Without Channel-Dedicated Sample-and-Hold Circuits)

When channels and self-diagnosis are selected at the same time, A/D conversion is first performed for the reference voltage supplied to the 12-bit A/D converter, and then A/D conversion is performed on the analog input of the selected channels, which sequence is repeated as below. In continuous scan mode, the internal reference voltage A/D conversion select bit (S12AD2.ADEXICR.OCSA) should be set to 0 (deselected).

(1) When the ADCSR.ADST bit is set to 1 (A/D conversion start) by software, or synchronous or asynchronous trigger input, A/D conversion for self-diagnosis is started first.
(2) When A/D conversion for self-diagnosis is completed, the A/D conversion result is stored into the A/D self-diagnosis data register (ADRD). A/D conversion is then performed for ANn channels selected by the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
(3) Each time A/D conversion of a single channel is completed, the A/D conversion result is stored into the corresponding A/D data register (ADDRy).
(4) When A/D conversion of all the selected channels is completed, a scan end interrupt request is generated if the ADCSR.ADIE bit is 1 (interrupt generation upon scanning completion enabled). At the same time, the 12-bit A/D converter starts A/D conversion for self-diagnosis and then starts A/D conversion on ANn channels selected by the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
(5) The ADCSR.ADST bit is not automatically cleared and steps 2 to 4 are repeated as long as the bit remains 1. When the ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the 12-bit A/D converter enters a wait state.
(6) When the ADCSR.ADST bit is later set to 1 (A/D conversion start), the A/D conversion for self-diagnosis is started again.



Note 1. ↓ indicates the instruction is executed by software.
Note 2. The converted data of A/D conversion 3 is ignored.

Figure 31.14 Example of Operation in Continuous Scan Mode (Basic Operation; AN101 and AN102 Selected + Self-Diagnosis)

31.3.3.4 Channel Selection and Self-Diagnosis (With Channel-Dedicated Sample-and-Hold Circuits)

When channels and self-diagnosis are selected and a channel-dedicated sample-and-hold circuit is used, sample-and-hold operations are performed first, and A/D conversion is performed for the reference voltage supplied to the 12-bit A/D converter as below. After that, A/D conversion is performed repeatedly on the analog input of the selected channels. In continuous scan mode, the internal reference voltage A/D conversion select bit (S12AD2.ADEXICR.OCSA) should be set to 0 (deselected).

(1) Analog input sampling of all channels for which the channel-dedicated sample-and-hold circuits are to be used is started when the ADCSR.ADST bit is set to 1 (A/D conversion start) by software, or synchronous or asynchronous trigger input.
(2) A/D conversion for self-diagnosis is started after completion of sampling and holding.
(3) When A/D conversion for self-diagnosis is completed, A/D conversion result is stored into the A/D self-diagnosis data register (ADRD), and A/D conversion is performed for ANn channels selected by the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
(4) Each time A/D conversion of a single channel is completed, the A/D conversion result is stored into the corresponding A/D data register (ADDRy).
(5) When A/D conversion of all the selected channels is completed, a scan end interrupt request is generated if the ADCSR.ADIE bit is 1 (interrupt upon scanning completion enabled). At the same time, analog input sampling is started for all the channels for which the channel-dedicated sample-and-hold circuits are to be used.
(6) The ADCSR.ADST bit is not automatically cleared and steps 2 to 5 are repeated as long as the ADCSR.ADST bit remains 1. When the ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the 12-bit A/D converter enters a wait state.
(7) When the ADST bit is later set to 1 (A/D conversion start), the A/D conversion for self-diagnosis is started again.

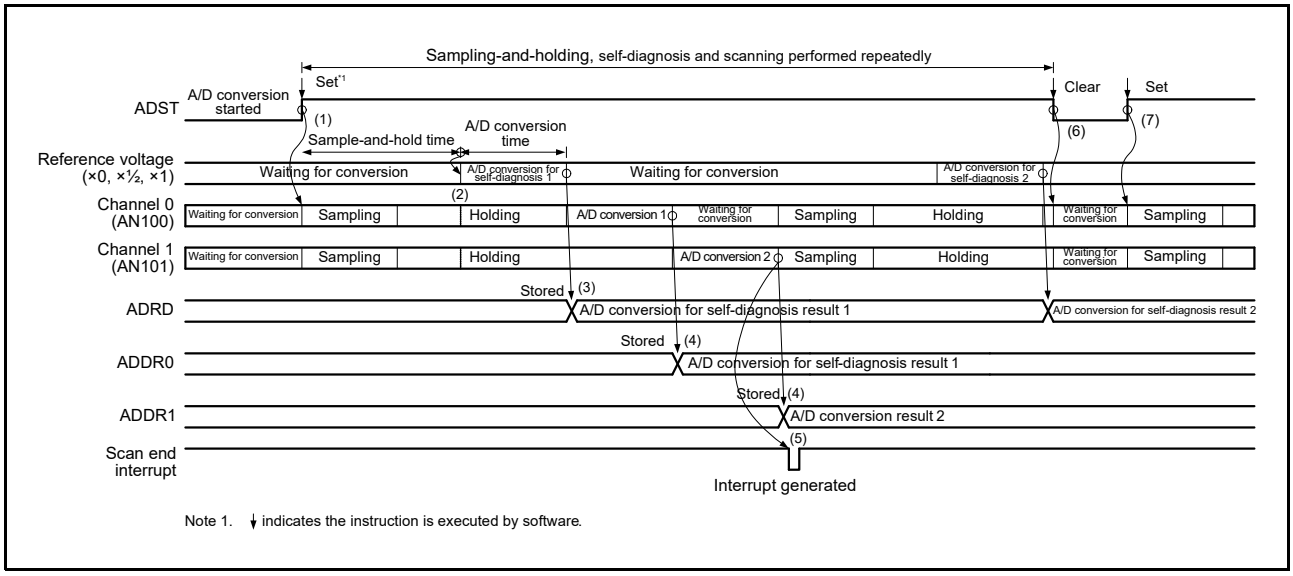


Figure 31.15 Example of Operation in Continuous Scan Mode (Channel-Dedicated Sample-and-Hold Circuits Used: AN100 and AN101 Selected + Self-Diagnosis)

31.3.4 Group Scan Mode

31.3.4.1 Basic Operation

Either two (groups A and B) or three (groups A, B, and C) can be selected as the number of the groups to be used in group scan mode.

In basic operation of group scan mode, A/D conversion is performed once on the analog inputs of all the specified channels in groups A and B, or groups A, B, and C after scan is started by a synchronous trigger as below. Scan operation of each group is similar to the scan operation in single scan mode.

The synchronous triggers of groups A and B, or groups A, B, and C can be selected using the TRSA[5:0], TRSB[5:0], and TRSC[5:0] bits in ADSTRGR, respectively. Different triggers should be used for each group A, B, and C so that scanning of groups A, B, and C does not occur simultaneously. Software trigger should not be used.

The channels to be scanned are selected using registers ADANSA0 and ADANSA1 for group A, registers ADANSB0 and ADANSB1 for group B, and registers ADANSC0 and ADANSC1 for group C.

In group scan mode, the internal reference voltage A/D conversion select bit (S12AD2.ADEXICR.OCSA) should be set to 0 (deselected).

When self-diagnosis is selected in group scan mode, self-diagnosis is separately executed for groups A and B, or groups A, B, and C.

The following describes operation in group scan mode using a trigger from the MTU. The TRG4AN, TRG4BN, and TRG4ABN triggers from the MTU are assumed to be used to start conversion of groups A, B and C, respectively.

(1) Scanning of group A is started by the TRG4AN trigger from the MTU.
(2) When group A scanning is completed, a scan end interrupt is generated if the ADCSR.ADIE bit is 1 (interrupt generation upon scanning completion enabled).
(3) Scanning of group B is started by the TRG4BN trigger from the MTU.
(4) When group B scanning is completed, a group B scan end interrupt is generated if the ADCSR.GBADIE bit is 1 (interrupt generation upon group B scan completion enabled).
(5) Scanning of group C is started by the TRG4ABN trigger from the MTU.
(6) When group C scanning is completed, a group C scan end interrupt is generated if the ADGCTRGR.GCADIE bit is 1 (interrupt generation upon group C scan completion enabled).

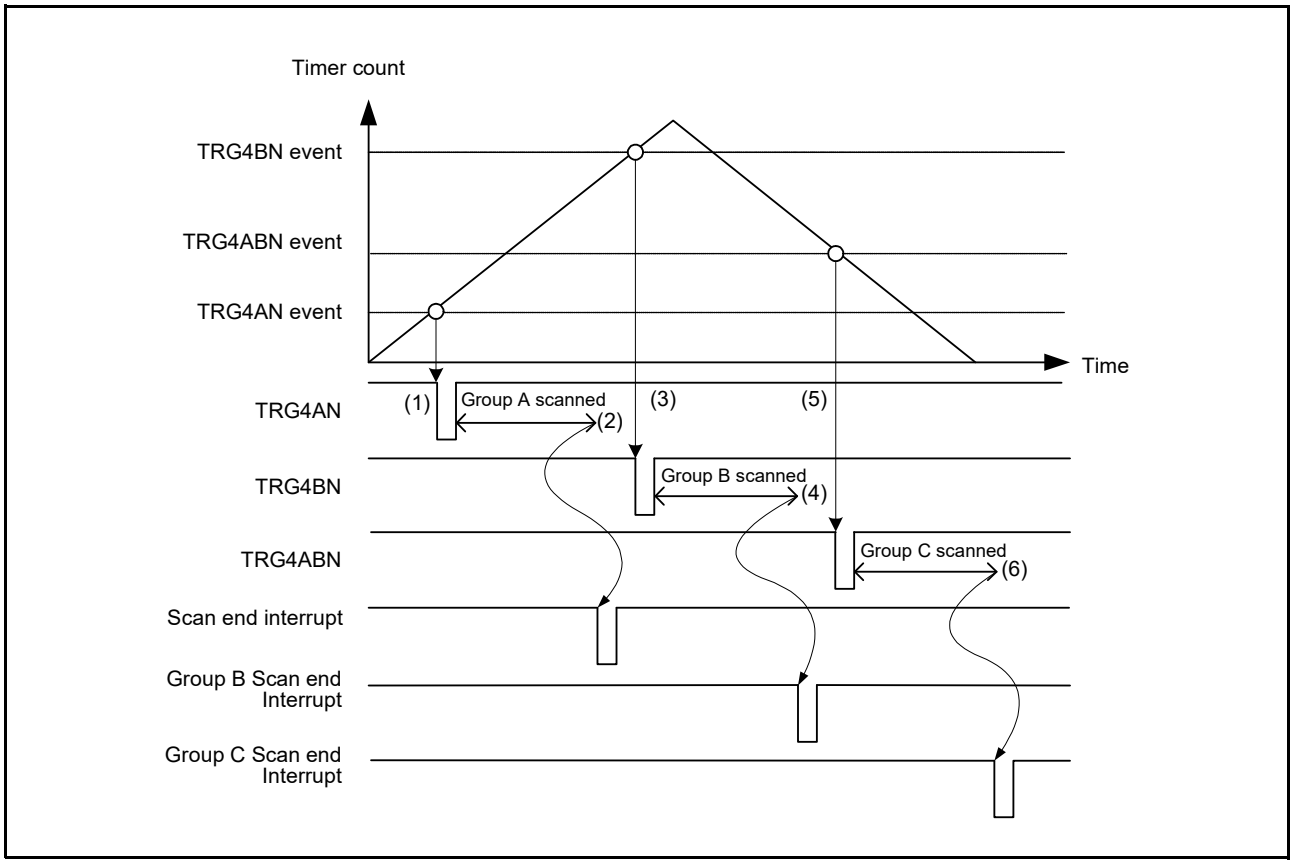


Figure 31.16 Example of Operation in Group Scan Mode (Basic Operation: Synchronous Triggers from MTU Used)

31.3.4.2 A/D Conversion in Double Trigger Mode

When double trigger mode is selected in group scan mode, two rounds of single scan operation started by a synchronous trigger are performed as a sequence for group A. For groups B and C, single scan operation started by a synchronous trigger is performed once.

In group scan mode, the synchronous triggers of groups A and B, or groups A, B, and C can be selected using the TRSA[5:0], TRSB[5:0], and TRSC[5:0] bits in ADSTRGR, respectively. Different triggers should be used for each group A, B, and C so that scanning of groups A, B, and C does not occur simultaneously. Software trigger and asynchronous trigger should not be used. When TRG4AN or TRG4BN, TRG7AN or TRG7BN, TRGA0N or TRG0N, TRGA9N or TRG9N, TRGA0N or TRGA9N, or TRG0N or TRG9N, GTADTRA0N or GTADTRB0N, GTADTRA1N or GTADTRB1N, GTADTRA2N or GTADTRB2N, or GTADTRA3N or GTADTRB3N is selected as the synchronous trigger of group A by the ADSTRGR.TRSA[5:0] bits, operation is performed in extended double trigger mode.

The channels to be scanned are selected using bits ADCSR.DBLANS[4:0] for group A, registers ADANSB0 and ADANSB1 for group B, and registers ADANSC0 and ADANSC1 for group C.

In group scan mode, the internal reference voltage A/D conversion select bit (S12AD2.ADEXICR.OCSA) should be set to 0 (deselected).

When double trigger mode is selected in group scan mode, self-diagnosis cannot be selected.

Duplication of A/D conversion data is enabled by setting the channel numbers to be duplicated to the ADCSR.DBLANS[4:0] bits and setting the ADCSR.DBLE bit to 1.

The following describes operation in group scan mode with double trigger mode using a synchronous trigger from the MTU. The TRG4ABN, TRGA0N, and TRGA1N triggers from the MTU are assumed to be used to start conversion of groups A, B, and C, respectively.

(1) Scanning of group C is started by the TRGA1N trigger from the MTU.
(2) When group C scanning is completed, a group C scan interrupt is generated if the ADGCTRGR.GCADIE bit is 1 (interrupt generation upon group C scan completion enabled).
(3) Scanning of group B is started by the TRGA0N trigger from the MTU.
(4) When group B scanning is completed, a group B scan end interrupt is generated if the ADCSR.GBADIE bit is 1 (interrupt generation upon group B scan enabled).
(5) The first scanning of group A is started by the first TRG4ABN trigger from the MTU.
(6) When the first scanning of group A is completed, the conversion result is stored into the corresponding A/D data register (ADDRy); a scan end interrupt request is not generated irrespective of the ADIE bit setting in ADCSR.
(7) The second scanning of group A is started by the second TRG4ABN trigger from the MTU.
(8) When the second scanning of group A is completed, the conversion result is stored into ADDBLDR. a scan end interrupt is generated if the ADCSR.ADIE bit is 1 (interrupt generation upon scanning completion enabled).
(9) The second scanning of group B is started by the second TRGA0N trigger from the MTU.
(10) When the second scanning of group B is completed, a group B scan interrupt is generated if the ADCSR.GBADIE bit is 1 (interrupt generation upon group B scan completion enabled).
(11) The second scanning of group C is started by the second TRGA1N trigger from the MTU.
(12) When the second scanning of group C is completed, a group C scan interrupt is generated if the ADGCTRGR.GCADIE bit is 1 (interrupt generation upon group C scan completion enabled).

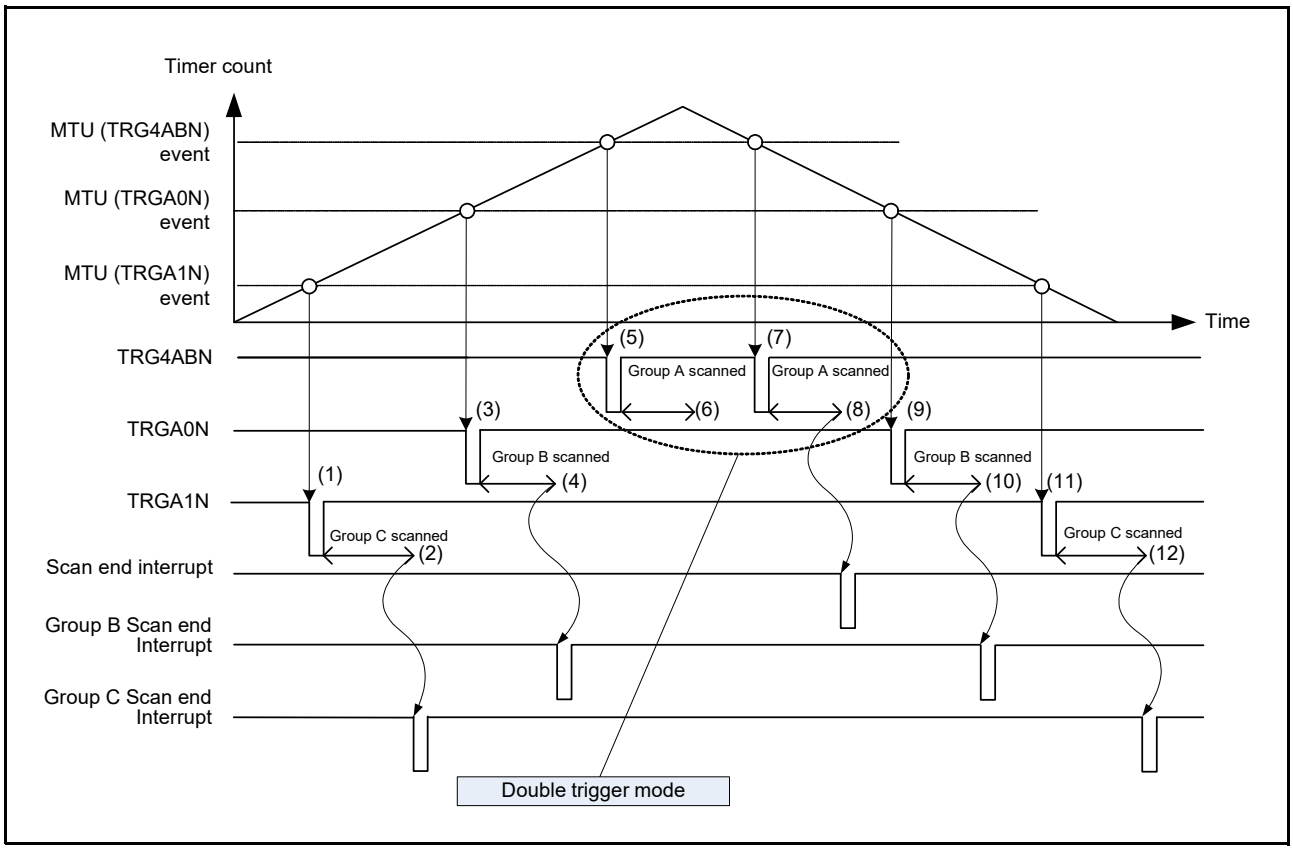


Figure 31.17 Example of Operation in Group Scan Mode with Double Trigger Mode (Basic Operation: Synchronous Triggers from MTU Used)

31.3.4.3 Operation under Group Priority Control

Setting the ADGSPCR.PGS bit to 1 in group scan mode makes operation proceed under group priority control. The group priority order is group A > group B > group C. Either two (groups A and B) or three (groups A, B, and C) can be selected as the number of the groups to be used in group scan mode. When setting the ADGSPCR.PGS bit to 1, follow the procedure described in Figure 31.18. If the procedure is not followed, proper scanning operation and data storage are not guaranteed.

In basic operation of group scan mode, if group A, B, or C is scanning, all other trigger inputs are ignored. Under group priority control, if a priority group trigger is input during A/D conversion for the low-priority group, A/D conversion for the low-priority group is discontinued and A/D conversion for the priority group proceeds.

If the ADGSPCR.GBRSCN bit is 0, the converter enters a wait state for the low-priority group on completion of the A/D conversion for the priority group.

The trigger input for the low-priority group during scanning is ignored.

If the ADGSPCR.GBRSCN bit is 1, the converter automatically restarts scanning for the low-priority group from the head of the group after A/D conversion for the priority group.

Also, the trigger input for the low-priority group generated during scanning for the priority group is enabled, and the converter automatically restarts scanning for the low-priority group after scanning for the priority group.

When the ADGSPCR.LGRRS bit is 0 while the ADGSPCR.GBRSCN bit is 1, the converter restarts scanning for the low-priority group from the head of the group. When the ADGSPCR.LGRRS bit is 1, the converter restarts scanning for the low-priority group from the channel on which scanning is discontinued.

However, when self-diagnosis is used, the converter restarts scanning from the channel on which scanning is discontinued after self-diagnosis is completed.

Table 31.13 summarizes operations in response to the input of a trigger during scanning with the settings of the ADGSPCR.GBRSCN bit.

When the ADGSPCR.GBRP bit is set to 1, scan operations in the lowest-priority group are continuously performed.

For the trigger settings in group scan mode, select a synchronous trigger for group A using the ADSTRGR.TRSA[5:0] bits, select a synchronous trigger different from that of group A for group B using the ADSTRGR.TRSB[5:0] bits, and select a synchronous trigger different from those of groups A and B for group C using the ADGCTRGR.TRSC[5:0] bits.

Set the ADSTRGR.TRSB[5:0] bits to 3Fh when setting group scan mode for two groups (the ADGCTRGR.GRCE bit to 0) and setting the ADGSPCR.GBRP bit to 1.

Set the ADGCTRGR.TRSC[5:0] bits to 3Fh when setting group scan mode for three groups (the ADGCTRGR.GRCE bit to 1) and setting the ADGSPCR.GBRP bit to 1.

Furthermore, as targets for scanning, select channels for group A using the ADANSA0 and ADANSA1 registers, select channels for group B using the ADANSB0 and ADANSB1 registers, and select channels for group C using the ADANSC0 and ADANSC1 registers.

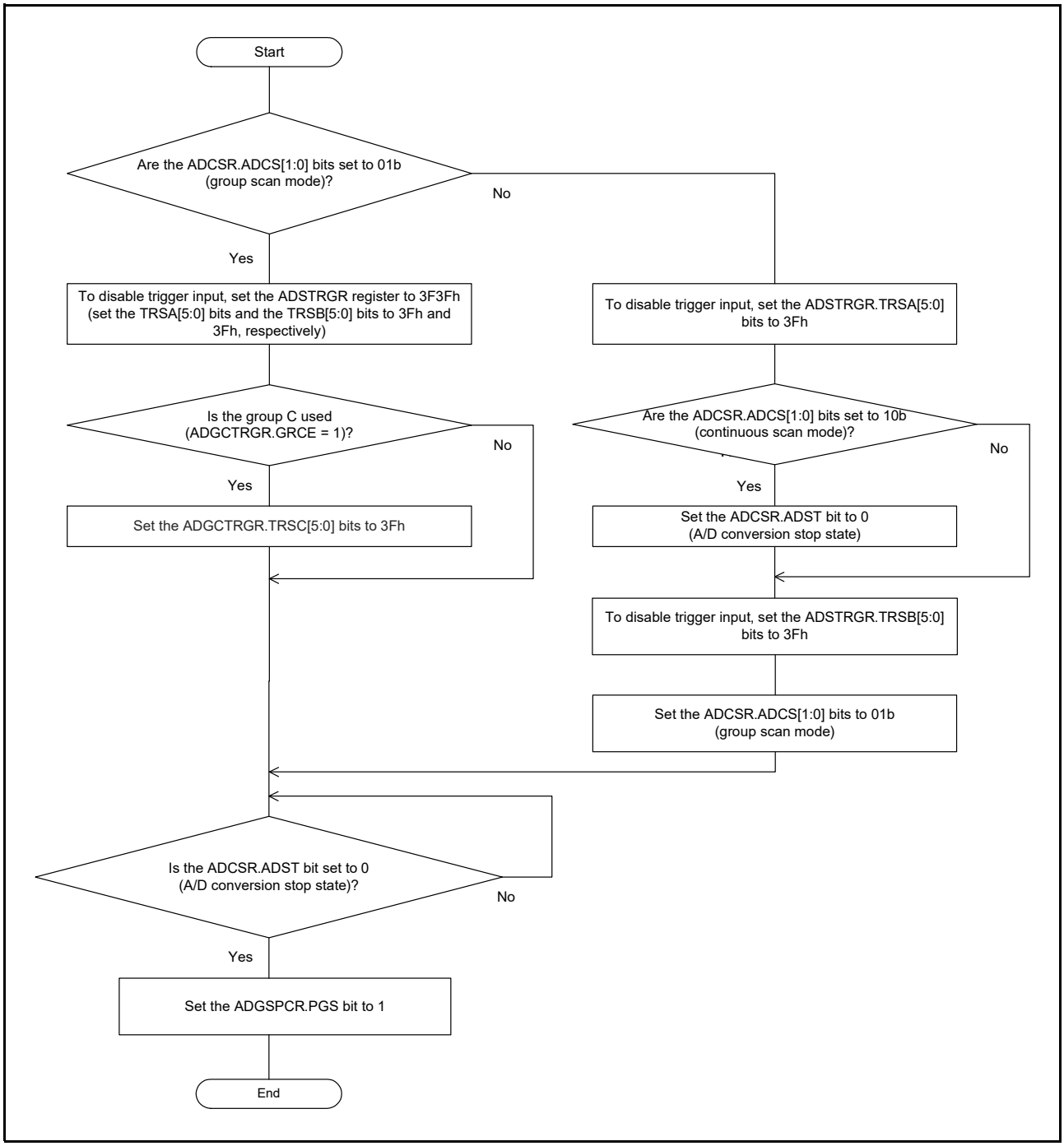


Figure 31.18 Flow of Setting the ADGSPCR.PGS Bit

Table 31.13 Control of Scanning Operations According to the Settings of the ADGSPCR.GBRSCN Bit

Scanning Operation	Trigger Input	ADGSPCR.GBRSCN = 0	ADGSPCR.GBRSCN = 1
When A/D conversion for group A is in progress	Input of trigger for group A	Trigger input is ineffective.	Trigger input is ineffective.
	Input of trigger for group B	Trigger input is ineffective.	A/D conversion is performed on group B after A/D conversion on group A is completed.
	Input of trigger for group C	Trigger input is ineffective.	A/D conversion is performed on group C after A/D conversion on group A is completed.
When A/D conversion for group B is in progress	Input of trigger for group A	A/D conversion in progress for group B discontinued and conversion for group A starts.	• A/D conversion in progress for group B is discontinued and conversion for group A starts. • A/D conversion for group B starts after conversion for group A is completed.
	Input of trigger for group B	Trigger input is ineffective.	Trigger input is ineffective.
	Input of trigger for group C	Trigger input is ineffective.	A/D conversion is performed on group C after A/D conversion on group B is completed.
When A/D conversion for group C is in progress	Input of trigger for group A	A/D conversion in progress for group C discontinued and conversion for group A starts.	• A/D conversion in progress for group C is discontinued and conversion for group A starts. • A/D conversion for group C starts after conversion for group A is completed.
	Input of trigger for group B	A/D conversion in progress for group C is discontinued and conversion for group B starts.	• A/D conversion in progress for group C is discontinued and conversion for group B starts. • A/D conversion for group C starts after conversion for group B is completed.
	Input of trigger for group C	Trigger input is ineffective.	Trigger input is ineffective.

When using group priority operation mode, refer to the following tables to select the desirable operating mode and set the registers.

Table 31.14 Group Priority Operation Setting and Operating Mode for Two Groups (ADGSPCR.PGS = 1, ADGCTRGR.GRCE = 0)

ADGSPCR			
GBRSCN	**LGRRS**	**GBRP**	**Operation**
0	x	0	Group priority operation for two groups (groups A and B) • When a group A trigger is input, group B scan is completed (not restarted)
1	0	0	Group priority operation for two groups (groups A and B) • After group B scan is discontinued, group B scan is restarted from the head of the channel selected with the ADANSB0 and ADANSB1 registers after group A scan is completed.
1	1	0	Group priority operation for two groups (groups A and B) • After group B scan is discontinued, group B scan is restarted from the channel on which scan was discontinued*1, among the channels selected with the ADANSB0 and ADANSB1 registers after group A scan is completed.
x	0	1	Group priority operation for two groups (groups A and B) • Single scan for group B is started continuously without start trigger input. After group B scan is discontinued, single scan is restarted from the head of the channel selected with the ADANSB0 and ADANSB1 registers after scan for group A is completed.
1	1	1	Group priority operation for two groups (groups A and B) • Single scan for group B is started continuously without start trigger input. After group B scan was discontinued, single scan is restarted from the channel on which scan was discontinued*1, among the channels selected with the ADANSB0 and ADANSB1 registers after group A scan is completed.

x = Don’t care

Note 1. When self-diagnosis is used (ADCER.DIAGM = 1), A/D conversion of the discontinued channel is started after self-diagnosis.

Table 31.15 Group Priority Operation Setting and Operating Mode for Three Groups (ADGSPCR.PGS = 1, ADGCTRGR.GRCE = 1)

ADGSPCR			
GBRSCN	LGRRS	GBRP	Operation
0	x	0	Group priority operation for three groups (groups A, B, and C) • When a group A trigger is input, group B scan is completed (not restarted) • When a trigger for group A or B is input, group C scan is not completed (not restarted).
0	x	1	Group priority operation for three groups (groups A, B, and C) • When a group A trigger is input, group B scan is completed (not restarted) • After group C scan is discontinued, scan is restarted from the channel on which scan was discontinued, among the channels selected with the ADANSC0 and ADANSC1 registers after scan for groups A and B is completed.
1	0	0	Group priority operation for three groups (groups A, B, and C) • After group B scan is discontinued, scan is restarted from the head of the channel selected with the ADANSB0 and ADANSB1 registers after group A scan is completed. • After group C scan is discontinued, scan is restarted from the head of the channel selected with the ADANSC0 and ADANSC1 registers after scan for groups A and B is completed.
1	1	0	Group priority operation for three groups (groups A, B, and C) • After group B scan is discontinued, scan is restarted from the head of the channel selected with the ADANSB0 and ADANSB1 registers after group A scan is completed. • After group C scan is discontinued, scan is restarted from the channel on which scan was discontinued*1, among the channels selected with the ADANSC0 and ADANSC1 registers after scan for groups A and B is completed.
1	0	1	Group priority operation for three groups (groups A, B, and C) • After group B scan is discontinued, scan is restarted from the head of the channel selected with the ADANSB0 and ADANSB1 registers after group A scan is completed. • Single scan for group C is started continuously without start trigger input. After group C scan is discontinued, single scan is restarted from the head of the channel selected with the ADANSC0 and ADANSC1 registers after scan for groups A and B is completed.
1	1	1	Group priority operation for three groups (groups A, B, and C) • After scanning for group B is discontinued, once scanning for group A completes, scanning is resumed starting from the channel on which scanning was discontinued*1, among those channels selected with the ADANSB0 and ADANSB1 registers. • Single scan for group C is started continuously without start trigger input. After group C scan is discontinued, single scan is restarted from the channel on which scan was discontinued*1, among the channels selected with the ADANSC0 and ADANSC1 registers after scan for groups A and B is completed.

x = Don’t care

Note 1. When self-diagnosis is used (ADCER.DIAGM = 1), A/D conversion of the discontinued channel is started after self-diagnosis.

(1) Group Priority Operation for Two Groups (ADGSPCR.PGS = 1, ADGCTRGR.GRCE = 0)

The following examples 1 to 5 show group priority operation in group scan mode (ADGSPCR.GBRSCN = 1, ADGSPCR.GBRP = 0, ADGSPCR.LGRRS = 0) when channel 0 is selected for group A and channels 1 to 3 are selected for group B.

Operation example 1: Group A trigger input during group B scan, with rescan setting

(1) When a group B trigger input sets the ADCSR.ADST bit to 1 (A/D conversion start), scan for the ANn channels selected in the ADANSB0 and ADANSB1 registers, starts from the channel with the smallest number n.

(2) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).

(3) If a group A trigger is input during scan for group B, group B scan is discontinued while the ADCSR.ADST bit remains 1, and scan for the ANn channels of group A selected in the ADANSA0 and ADANSA1 registers, starts from the channel with the smallest number n.
If A/D conversion is not completed when scan was discontinued, the result is not stored in the corresponding A/D data register (ADDRy).

(4) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).

(5) A scan end interrupt request is generated if the ADCSR.ADIE bit is 1 (interrupt generation upon scanning completion enabled).

(6) If the ADGSPCR.GBRSCN bit is 1 (scan for the group is restarted after having been discontinued due to group priority operation), scan for the ANn channels of group B selected in the ADANSB0 and ADANSB1 registers, restarts from the channel with the smallest number n while the ADCSR.ADST bit remains 1.

(7) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).

(8) A group B scan end interrupt request is generated if the ADCSR.GBADIE bit is 1 (interrupt generation upon group B scan completion enabled).

(9) The ADCSR.ADST bit is automatically cleared to 0 when scan of all selected channels is completed, and the 12-bit A/D converter enters a wait state.

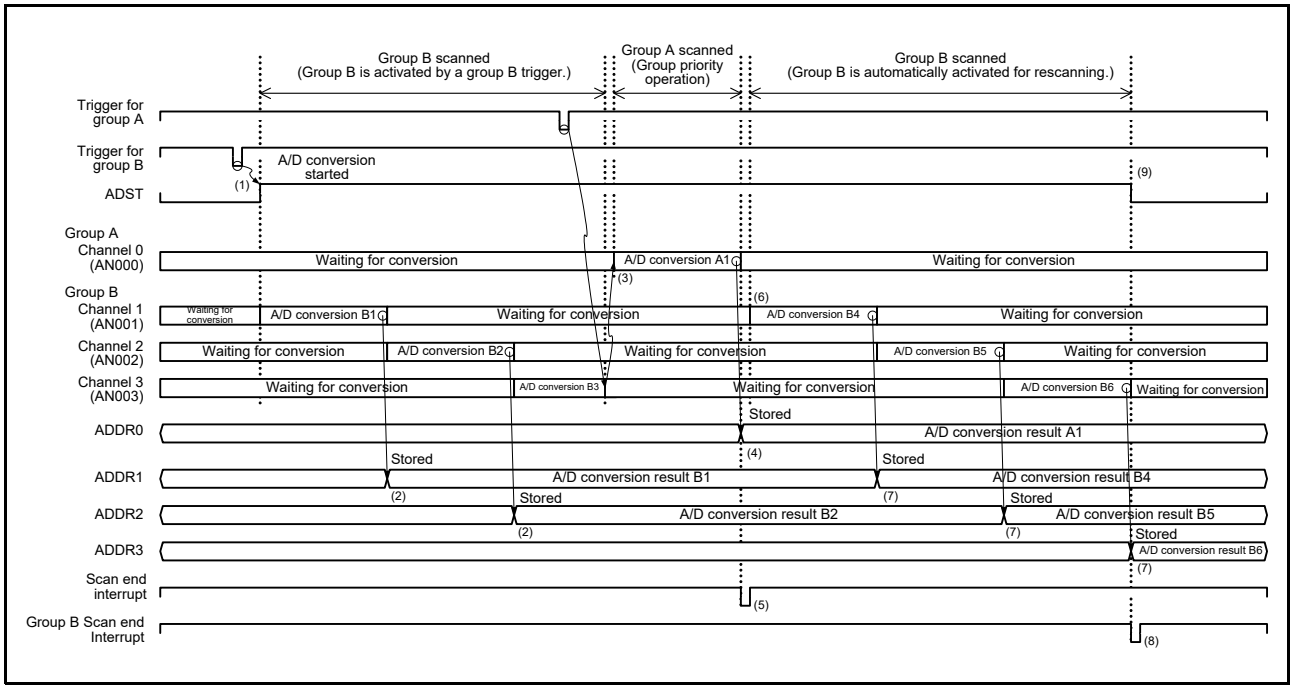


Figure 31.19 Example 1 of Group Priority Operation: Group A Trigger Input during Group B Scan, With Rescan Setting (ADGSPCR.GBRSCN = 1, ADGSPCR.GBRP = 0, ADGSPCR.LGRRS = 0)

Operation example 2: Group A trigger input during group B rescan, with rescan setting

Figure 31.20 shows an example when a group A trigger is input during rescan operation on group B.

If a group A trigger is input, scan for group A starts even while rescan operation is in progress. Scan for group B starts after scan for group A is completed.

Operations of the ADCSR.ADST bit, storing to the A/D conversion result in the A/D data register (ADDRy), and interrupt requests are the same as example 1.

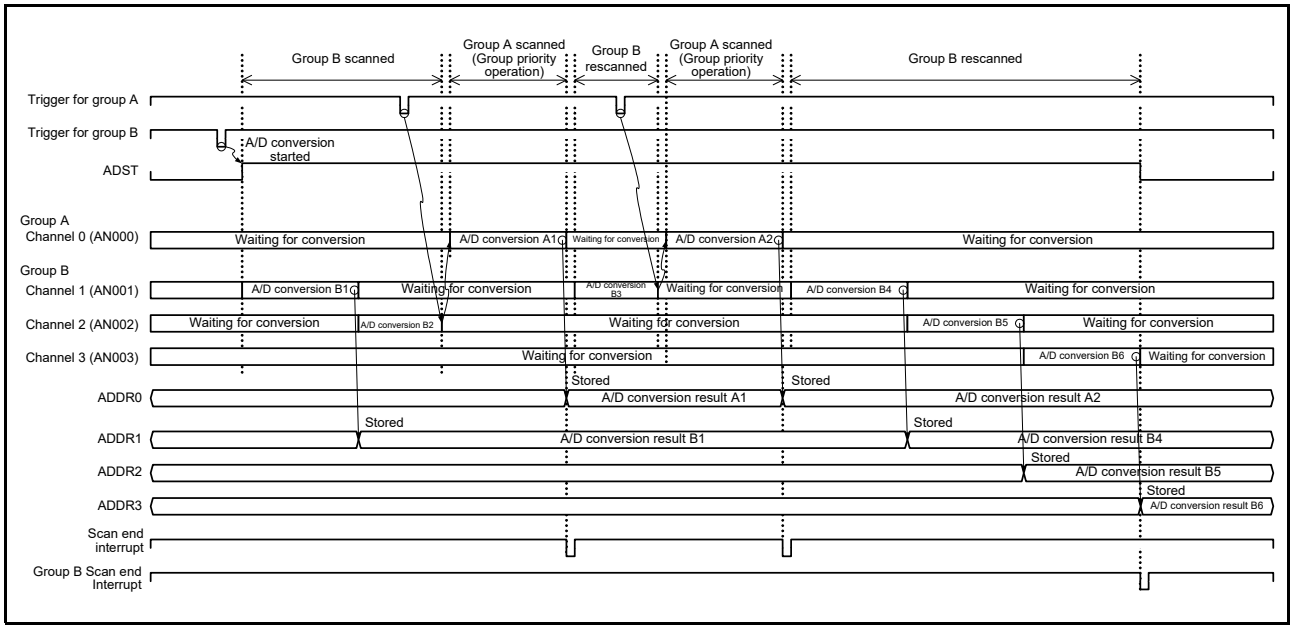


Figure 31.20 Example 2 of Group Priority Operation: Group A Trigger Input during Group B Rescan, With Rescan Setting (ADGSPCR.GBRSCN = 1, ADGSPCR.GBRP = 0, ADGSPCR.LGRRS = 0)

Operation example 3: Group B trigger input during group A scan, with rescan setting

The following describes an example when a group B trigger is input during scan operation on group A when the ADGPSCR.GBRSCN bit is 1 (scan for the group is restarted after having been discontinued due to group priority operation).
If the ADGPSCR.GBRSCN bit is 0, all group B triggers that are input during scan operation on group A are disabled.

(1) When a group A trigger input sets the ADCSR.ADST bit to 1 (A/D conversion start), scan for the ANn channels of group A selected in the ADANSA0 and ADANSA1 registers, starts from the channel with the smallest number n.
(2) If a group B trigger is input during scan for group A, scan for group B can be started.
(3) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).
(4) After scan for group A is completed, a scan end interrupt request is generated if the ADCSR.ADIE bit is 1 (interrupt generation upon scanning completion enabled).
(5) After scan for group A is completed, scan for the ANn channels of group B selected in the ADANSB0 and ADANSB1 registers, starts from the channel with the smallest number n while the ADCSR.ADST bit remains 1. When a group A trigger is input during scan for group B, group A scan starts as in example 1, and group B scan starts after group A scan is completed.
(6) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).
(7) After scan for group B is completed, a group B scan end interrupt request is generated if the ADCSR.GBADIE bit is 1 (interrupt generation upon group B scan completion enabled).
(8) The ADCSR.ADST bit is automatically cleared to 0 when scan of all selected channels is completed, and the 12-bit A/D converter enters a wait state.

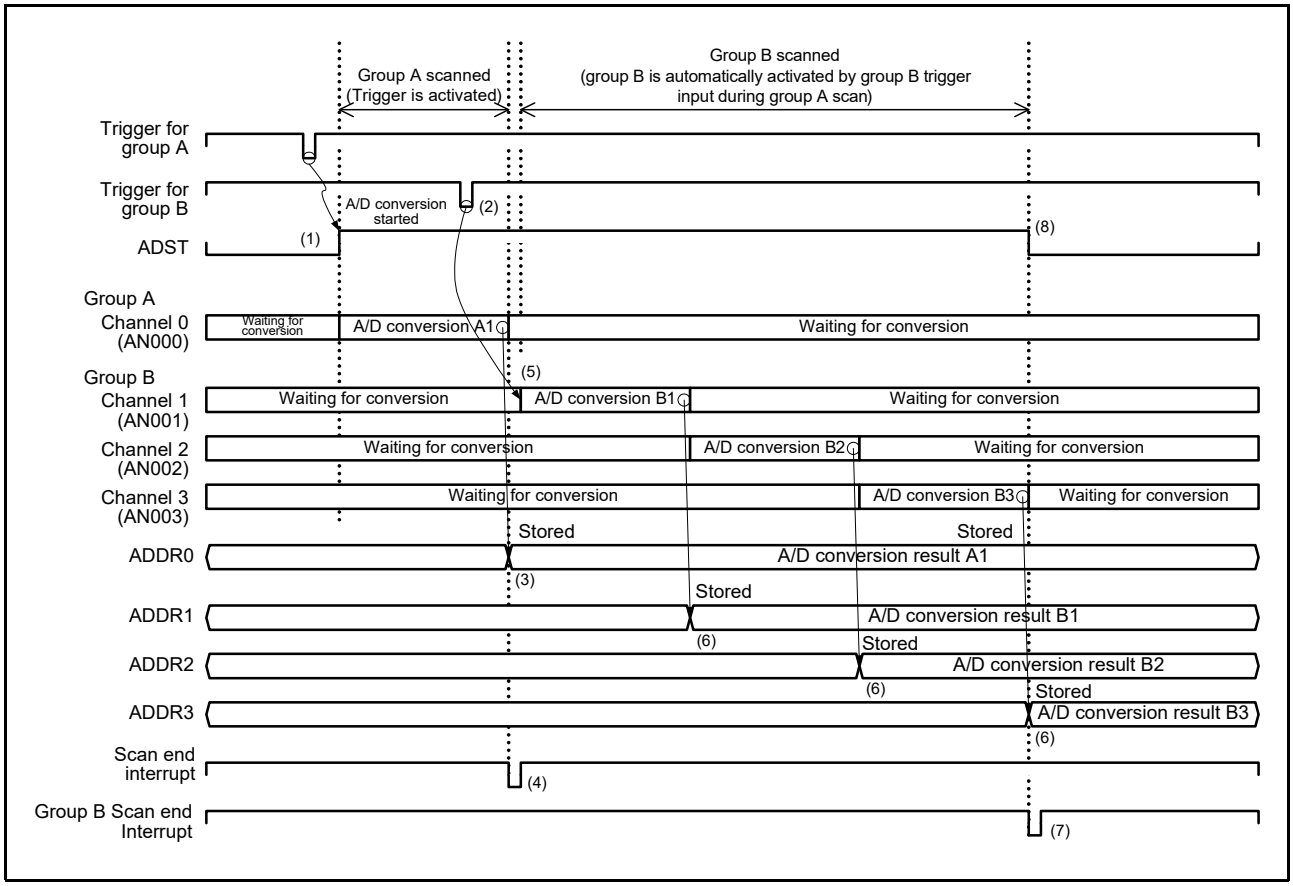


Figure 31.21 Example 3 of Group Priority Operation: Group B Trigger Input during Group A Scan, With Rescan Setting (ADGSPCR.GBRSCN = 1, ADGSPCR.GBRP = 0, ADGSPCR.LGRRS = 0)

Operation example 4 shows group priority operation in group scan mode (ADGSPCR.GBRSCN = 0, ADGSPCR.GBRP = 0, ADGSPCR.LGRRS = 0) when channel 0 is selected for group A and channels 1 to 3 are selected for group B.

Operation example 4: Group A trigger input during group B scan, without rescan setting

(1) When a group B trigger input sets the ADCSR.ADST bit to 1 (A/D conversion start), scan for the ANn channels of group B selected in the ADANSB0 and ADANSB1 registers, starts from the channel with the smallest number n.

(2) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).

(3) If a group A trigger is input during scan for group B, group B scan is discontinued while the ADCSR.ADST bit remains 1, and scan for the ANn channels of group A selected in the ADANSA0 and ADANSA1 registers, starts from the channel with the smallest number n.
If A/D conversion is not completed when scan was discontinued, the result is not stored in the corresponding A/D data register (ADDRy).

(4) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).

(5) After scan for group A is completed, a scan end interrupt request is generated if the ADCSR.ADIE bit is 1 (interrupt generation upon scanning completion enabled).

(6) The ADST bit is automatically cleared to 0 when scan for group A is completed, and the 12-bit A/D converter enters a wait state. Scan for group B is not started until the next group B trigger is input.

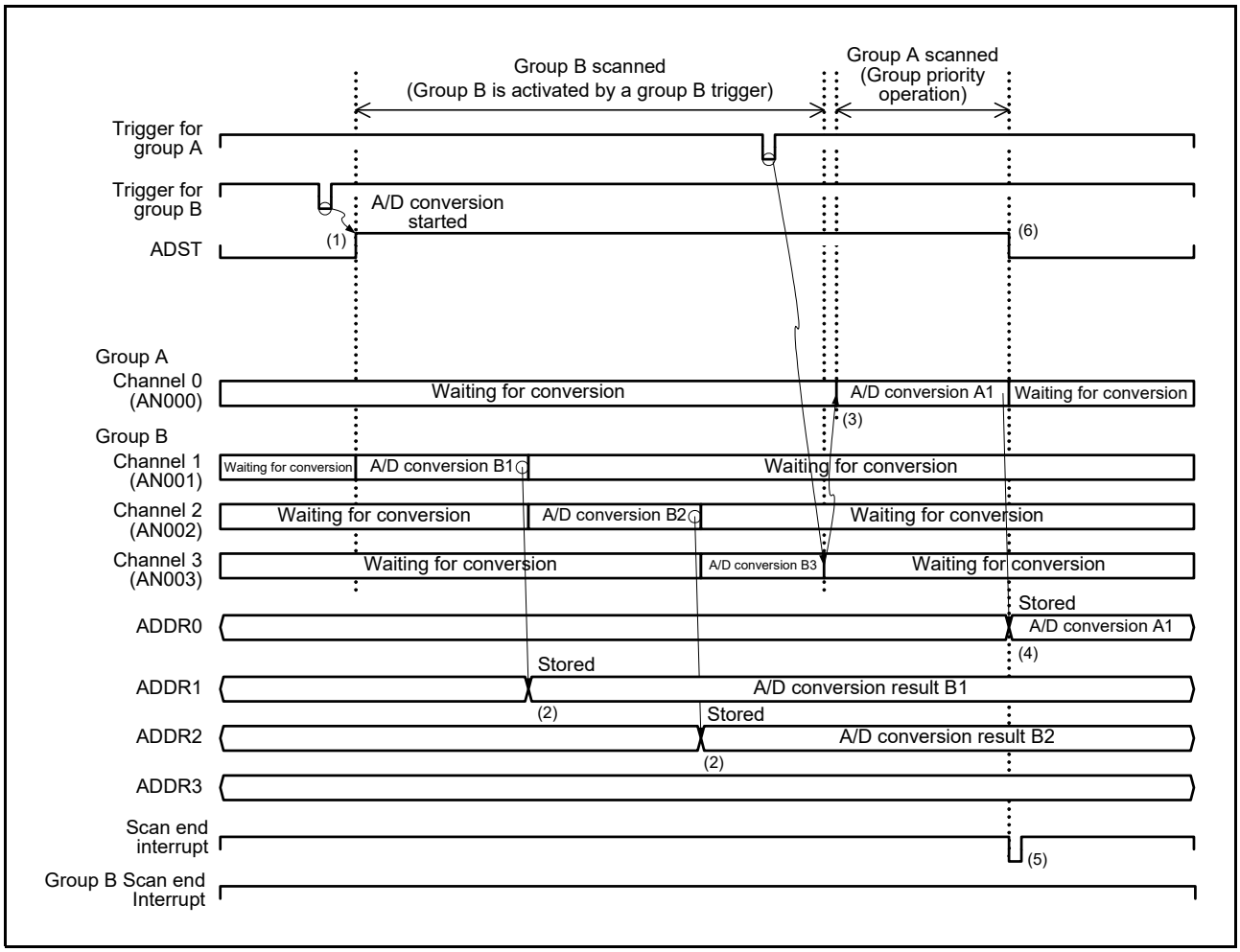


Figure 31.22 Example 4 of Group Priority Operation: Group A Trigger Input during Group B Scan, Without Rescan Setting (ADGSPCR.GBRSCN = 0, ADGSPCR.GBRP = 0, ADGSPCR.LGRRS = 0)

Operation example 5 shows group priority operation in group scan mode (ADGSPCR.GBRSCN = 1, ADGSPCR.GBRP = 1, ADGSPCR.LGRRS = 0) when channel 0 is selected for group A and channels 1 and 2 are selected for group B. When the ADGCTRGR.GRCE bit is set to 1, single scan mode is continuously operated on group C and scan for group B is started by trigger input.

Operation example 5: Continuous single scan operation on group B

(1) When setting ADGSPCR.GBRP to 1 sets the ADCSR.ADST bit to 1 (A/D conversion start), scan for the ANn channels selected in the ADANSB0 and ADANSB1 registers, starts from the channel with the smallest number n.
(2) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).
(3) If a group A trigger is input during scan for group B, group B scan is discontinued while the ADCSR.ADST bit remains 1, and scan for the ANn channels of group A selected in the ADANSA0 and ADANSA1 registers, starts from the channel with the smallest number n. If A/D conversion is not completed when scan was discontinued, the result is not stored in the corresponding A/D data register (ADDRy).
(4) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).
(5) After scan for group A is completed, a scan end interrupt request is generated if the ADCSR.ADIE bit is 1 (interrupt generation upon scanning completion enabled).
(6) If the ADGSPCR.GBRP bit is set to 1 (single scan is continuously operated), scan for the ANn channels of group B selected in the ADANSB0, ADANSB1 registers, restarts from the channel with the smallest number n while the ADCSR.ADST bit remains 1.
(7) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).
(8) A group B scan end interrupt request is generated if the ADCSR.GBADIE bit is 1 (interrupt generation upon group B scan completion enabled).
(9) If the ADGSPCR.GBRP bit is set to 1 (single scan is continuously operated), scan for the ANn channels of group B selected in the ADANSB0 and ADANSB1 registers, restarts from the channel with the smallest number n while the ADCSR.ADST bit remains 1.

To continuously operate single scan for group B, disable trigger input for group B.
Steps 6 to 9 are repeated as long as the ADGSPCR.GBRP bit remains 1. Clearing of the ADCSR.ADST bit to 0 is prohibited while the ADGSPCR.GBRP bit is set to 1. To forcibly stop scanning when ADGSPCR.GBRP = 1, follow the procedures for clear operation by software through the ADCSR.ADST bit shown in section 31.6.2, Notes on Stopping A/D Conversion.

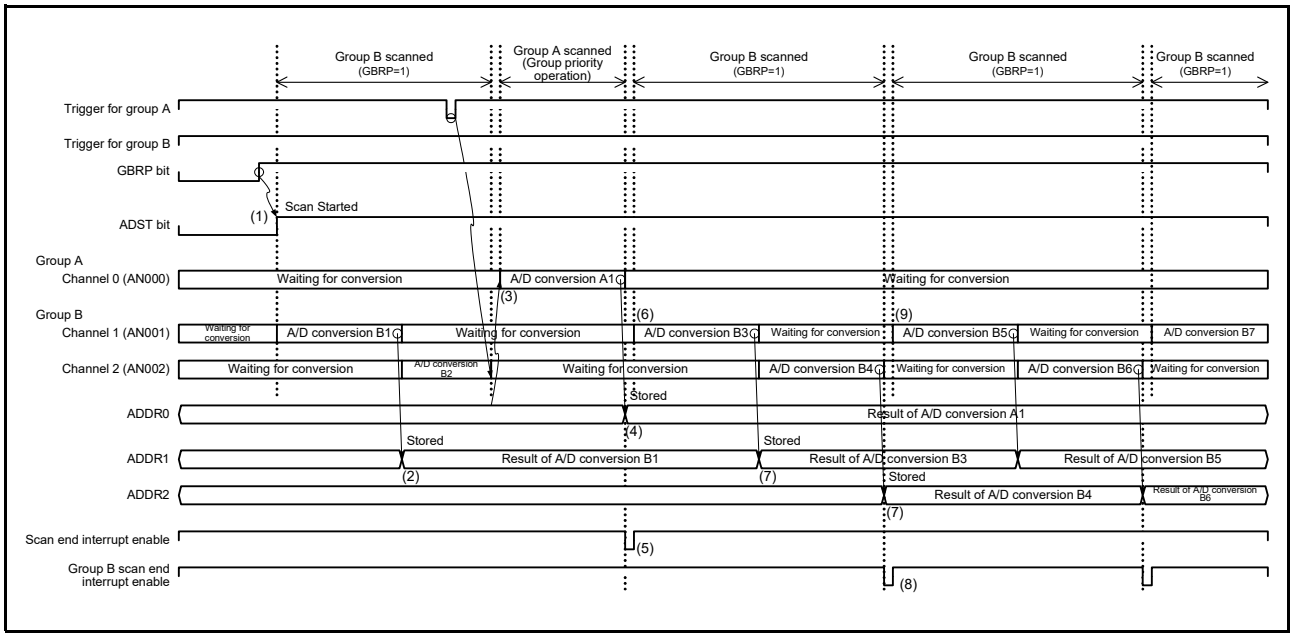


Figure 31.23 Example 5 for Group Priority Operation: Continuous Single Scan Operation on Group B (ADGSPCR.GBRP = 1, ADGSPCR.LGRRS = 1, ADGCTRGR.GRCE = 0)

(2) Group Priority Operation for Three Groups (ADGSPCR.PGS = 1, ADGCTRGR.GRCE = 1)

The following examples 1 to 5 show group priority operation in group scan mode (ADGSPCR.GBRSCN = 1, ADGSPCR.GBRP = 0, ADGSPCR.LGRRS = 1) when channel 0 is selected for group A, channels 1 and 2 are selected for group B, and channels 3 and 4 are selected for group C.
The priority groups mean groups A and B for group C and group A for group B.

Operation example 1: Priority group trigger input during low-priority group scan, with rescan setting

(1) When a group C trigger input sets the ADCSR.ADST bit to 1 (A/D conversion start), scan for the ANn channels selected in the ADANSC0 and ADANSC1 registers, starts from the channel with the smallest number n.
(2) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy)
(3) If a group B trigger is input during scan for group C, group C scan is discontinued while the ADCSR.ADST bit remains 1, and scan for the ANn channels of group B selected in the ADANSB0 and ADANSB1 registers, starts from the channel with the smallest number n. On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy)
(4) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy)
(5) If a group A trigger is input during scan for group B, group B scan is discontinued while the ADCSR.ADST bit remains 1, and scan for the ANn channels of group A selected in the ADANSA0 and ADANSA1 registers, starts from the channel with the smallest number n. If A/D conversion is not completed when scan was discontinued, the result is not stored in the corresponding A/D data register (ADDRy).
(6) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy)
(7) A scan end interrupt request is generated if the ADCSR.ADIE bit is 1 (interrupt generation upon scanning completion enabled).
(8) If the ADGSPCR.GBRSCN bit is 1 (scan for the group is restarted after having been discontinued due to group priority operation), scan for the ANn channels of group B selected in the ADANSB0 and ADANSB1 registers, restarts from the channel with the smallest number n while the ADCSR.ADST bit remains 1. If the ADGSPCR.LGRRS bit is set to 1 at this time, scan for group B starts from the channel on which A/D conversion was discontinued.
(9) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy)
(10) A group B scan end interrupt request is generated if the ADCSR.GBADIE bit is 1 (interrupt generation upon group B scan completion enabled).
(11) If the ADGSPCR.GBRSCN bit is 1, scan for the ANn channels of group C selected in the ADANSC0 and ADANSC1 registers, restarts from the channel with the smallest number n while the ADCSR.ADST bit remains 1. If the ADGSPCR.LGRRS bit is set to 1 at this time, scan for group C starts from the channel on which A/D conversion was discontinued.
(12) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy)
(13) A group C scan end interrupt is generated if the ADGCTRGR.GCADIE bit is 1 (interrupt generation upon group C scan completion enabled).
(14) The ADST bit is automatically cleared to 0 when scan for group A is completed, and the 12-bit A/D converter enters a wait state.

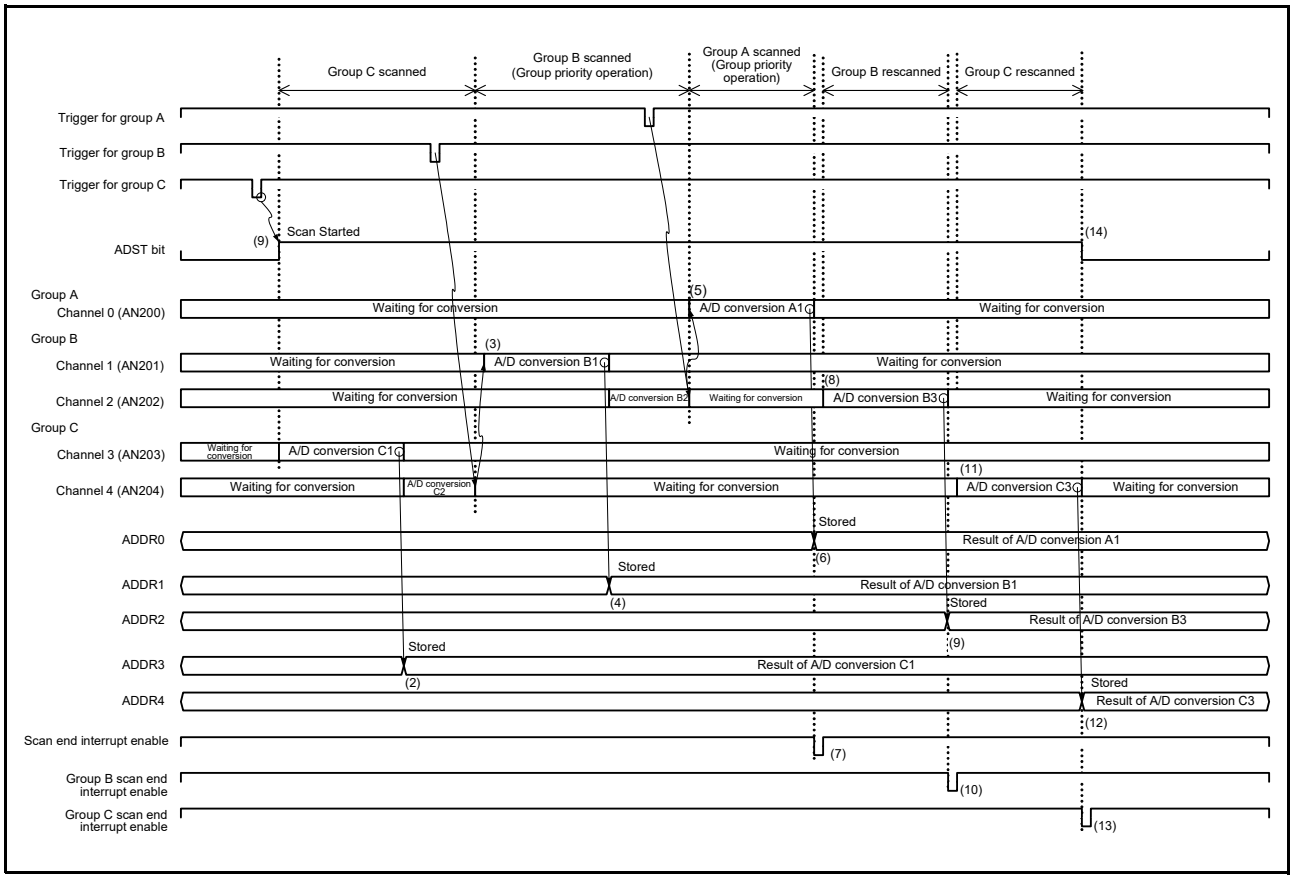


Figure 31.24 Example 1 of Group Priority Operation: Priority Group Trigger Input during Low-Priority Group Scan, With Rescan Setting (ADGSPCR.GBRSCN = 1, ADGSPCR.GBRP = 0, ADGSPCR.LGRRS = 1)

Operation example 2: Priority group trigger input during low-priority group rescan, with rescan setting

Figure 31.25 shows an example when a group A trigger is input during rescan operation on group B.

If a trigger for the priority groups (groups A and B for group C and group A for group B) is input, scan for the priority group starts even while rescan operation on the low-priority group is in progress. After scan for the priority group is completed, scan for the low-priority group is restarted after having been discontinued.

Operations of the ADCSR.ADST bit, storing to the A/D conversion result in the A/D data register (ADDRy), and interrupt requests are the same as example 1.

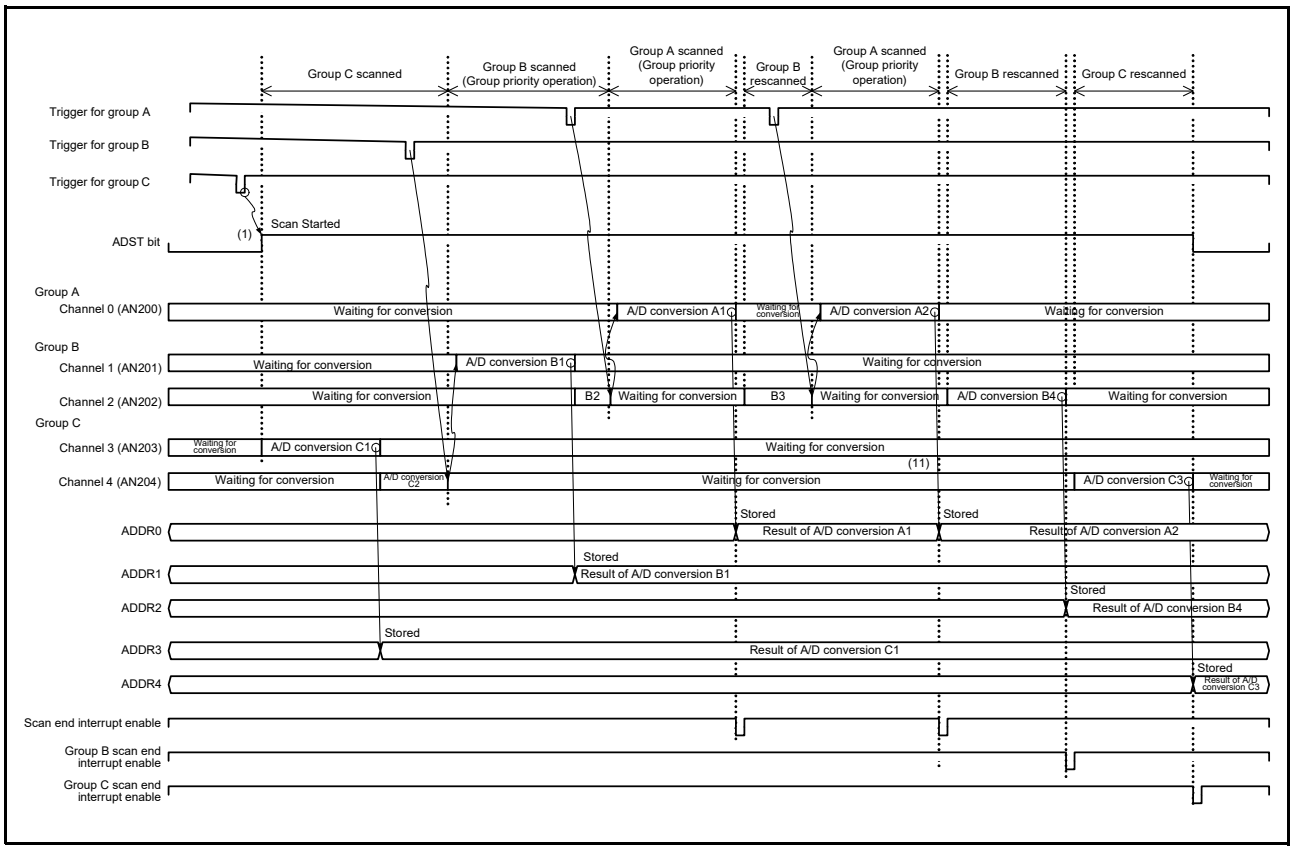


Figure 31.25 Example 2 of Group Priority Operation: Priority Group Trigger Input during Low-Priority Group Rescan, With Rescan Setting (ADGSPCR.GBRSCN = 1, ADGSPCR.GBRP = 0, ADGSPCR.LGRRS = 1)

Operation example 3: Low-priority group trigger input during priority group scan, with rescan setting

The following describes an example when a trigger for the low-priority group is input during scan operation on the priority group when the ADGPSCR.GBRSCN bit is 1 (scan for the group is restarted after having been discontinued due to group priority operation). If the ADGPSCR.GBRSCN bit is 0, all triggers for the low-priority group that are input during scan operation on the priority group are disabled.

(1) When a group A trigger input sets the ADCSR.ADST bit to 1 (A/D conversion start), scan for the ANn channels of group A selected in the ADANSA0 and ADANSA1 registers, starts from the channel with the smallest number n.
(2) If a group B trigger is input during scan for group A, scan for group B can be started.
(3) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy)
(4) After scan for group A is completed, a scan end interrupt request is generated if the ADCSR.ADIE bit is 1 (interrupt generation upon scanning completion enabled).
(5) After scan for group A is completed, scan for the ANn channels of group B selected in the ADANSB0 and ADANSB1 registers, starts from the channel with the smallest number n while the ADCSR.ADST bit remains 1. If the ADGSPCR.LGRRS bit is set to 1 at this time, scan for group B starts from the channel on which A/D conversion was discontinued.
When a group A trigger is input during scan for group B, group A scan starts as in example 1, and group B scan starts after group A scan is completed.
(6) If a group C trigger is input during scan for group B, scan for group C can be started.
(7) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy)
(8) After scan for group B is completed, a group B scan end interrupt request is generated if the ADCSR.GBADIE bit is 1 (interrupt generation upon group B scan completion enabled).
(9) After scan for group B is completed, scan for the ANn channels of group C selected in the ADANSC0 and ADANSC1 registers, starts from the channel with the smallest number n while the ADCSR.ADST bit remains 1. If the ADGSPCR.LGRRS bit is set to 1 at this time, scan for group C starts from the channel on which A/D conversion was discontinued.
When a group A or B trigger is input during scan for group C, group A or B scan starts as in example 1, and group C scan starts after group A or B scan is completed.
(10) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy)
(11) After scan for group C is completed, a group C scan end interrupt request is generated if the ADCSR.GBADIE bit is 1 (interrupt generation upon group C scan completion enabled).
(12) The ADCSR.ADST bit is automatically cleared to 0 when scan of all selected channels is completed, and the 12-bit A/D converter enters a wait state.

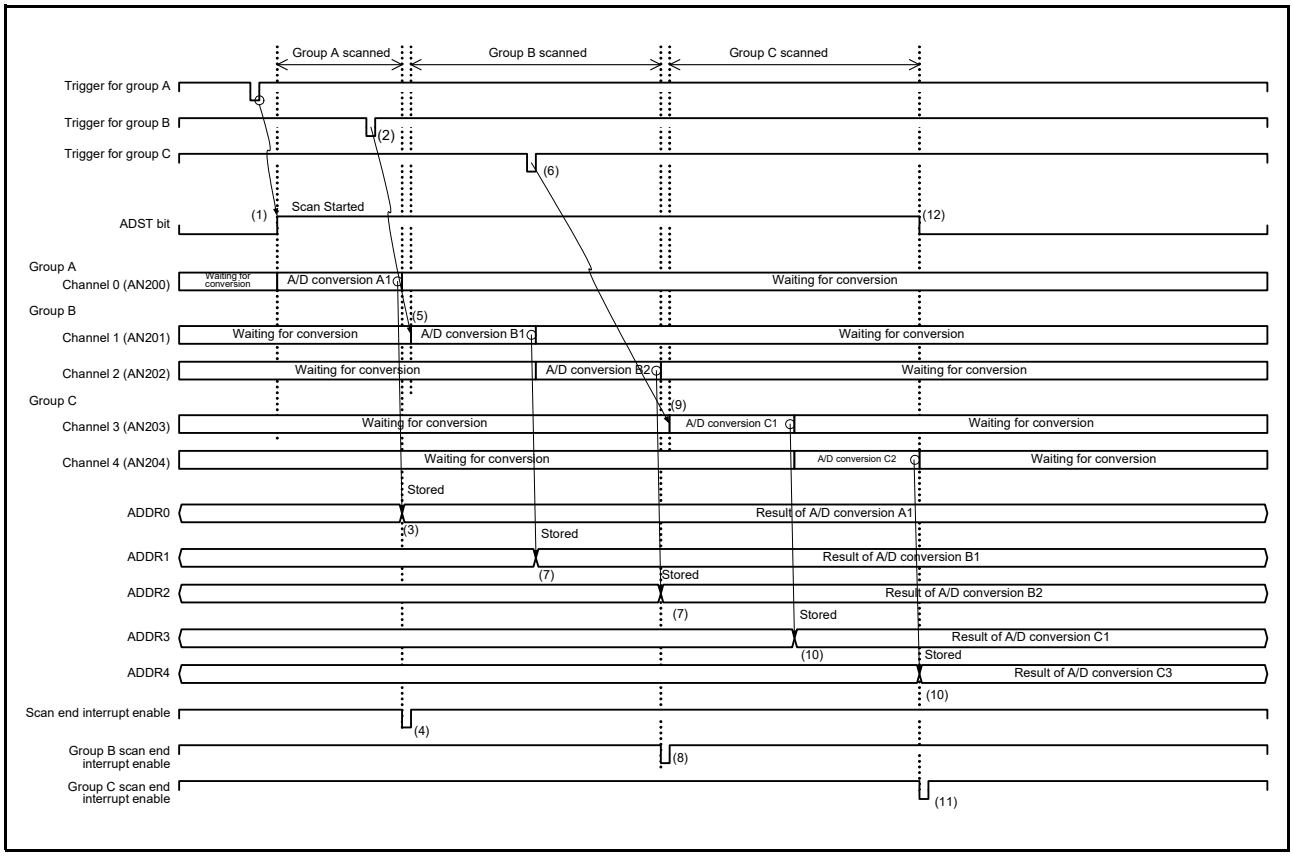


Figure 31.26 Example 3 of Group Priority Operation: Low-Priority Group Trigger Input during Priority Group Scan, With Rescan Setting (ADGSPCR.GBRSCN = 1, ADGSPCR.GBRP = 0, ADGSPCR.LGRRS = 1, ADGCTRGR.GRCE = 1)

Operation example 4 shows group priority operation in group scan mode (ADGSPCR.GBRSCN = 0, ADGSPCR.GBRP = 0, ADGSPCR.LGRRS = 0) when channel 0 is selected for group A, channels 1 and 2 are selected for group B, and channels 3 and 4 are selected for group C.

Operation example 4: Priority group trigger input during low-priority group scan, without rescan setting

(1) When a group C trigger input sets the ADCSR.ADST bit to 1 (A/D conversion start), scan for the ANn channels selected in the ADANSC0 and ADANSC1 registers, starts from the channel with the smallest number n.

(2) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy)

(3) If a group B trigger is input during scan for group C, group C scan is discontinued while the ADCSR.ADST bit remains 1, and scan for the ANn channels of group B selected in the ADANSB0 and ADANSB1 registers, starts from the channel with the smallest number n. If A/D conversion is not completed when scan was discontinued, the result is not stored in the corresponding A/D data register (ADDRy).

(4) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy)

(5) If a group A trigger is input during scan for group B, group B scan is discontinued while the ADCSR.ADST bit remains 1, and scan for the ANn channels of group A selected in the ADANSB0 and ADANSB1 registers, starts from the channel with the smallest number n. If A/D conversion is not completed when scan was discontinued, the result is not stored in the corresponding A/D data register (ADDRy).

(6) After scan for group A is completed, a scan end interrupt request is generated if the ADCSR.ADIE bit is 1 (interrupt generation upon scanning completion enabled).

(7) The ADST bit is automatically cleared to 0 when scan for group A is completed, and the 12-bit A/D converter enters a wait state. Scan for groups C and B is not started until the next trigger corresponding to the group is input.

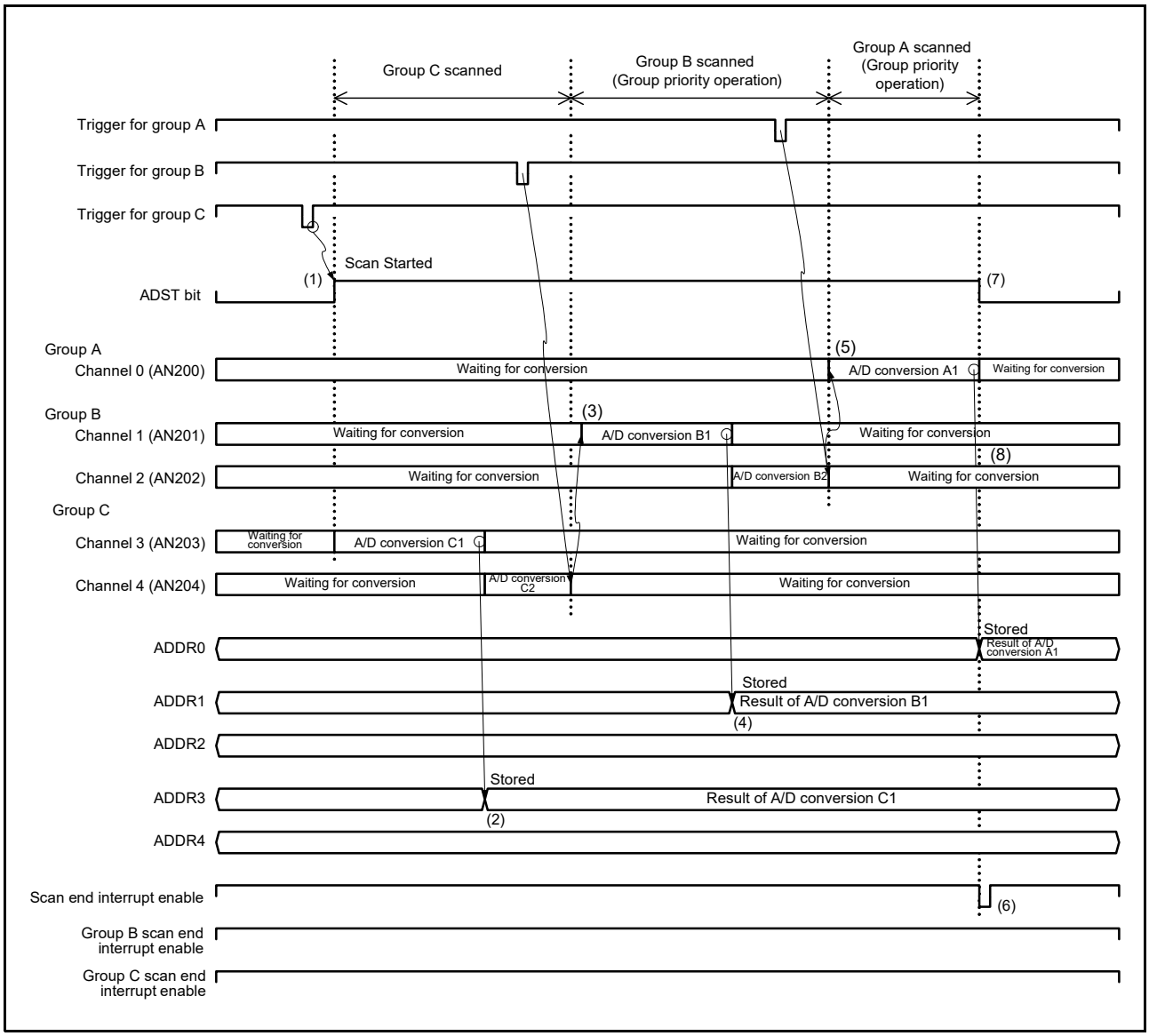


Figure 31.27 Example 4 of Group Priority Operation: Priority Group Trigger Input during Low-Priority Group Scan, Without Rescan Setting (ADGSPCR.GBRSCN = 0, ADGSPCR.GBRP = 0, ADGSPCR.LGRRS = 1)

Operation example 5 shows group priority operation in group scan mode (ADGSPCR.GBRSCN = 1, ADGSPCR.GBRP = 1, ADGSPCR.LGRRS = 1) when channel 0 is selected for group A, channel 1 is selected for group B, and channels 2 and 3 are selected for group C.
When the ADGCTRGR.GRCE bit is set to 1, single scan mode is continuously operated on group B and trigger input for group C is disabled.

Operation example 5: Continuous single scan operation on group C

(1) When setting ADGSPCR.GBRP to 1 sets the ADCSR.ADST bit to 1 (A/D conversion start), scan for the ANn channels selected in the ADANSC0 and ADANSC1 registers, starts from the channel with the smallest number n.
(2) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy)
(3) If a group B trigger is input during scan for group C, group C scan is discontinued while the ADCSR.ADST bit remains 1, and scan for the ANn channels of group B selected in the ADANSB0 and ADANSB1 registers, starts from the channel with the smallest number n. If A/D conversion is not completed when scan was discontinued, the result is not stored in the corresponding A/D data register (ADDRy).
(4) If a group A trigger is input during scan for group B, group B scan is discontinued while the ADCSR.ADST bit remains 1, and scan for the ANn channels of group A selected in the ADANSA0 and ADANSA1 registers, starts from the channel with the smallest number n. If A/D conversion is not completed when scan was discontinued, the result is not stored in the corresponding A/D data register (ADDRy).
(5) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy)
(6) A scan end interrupt request is generated if the ADCSR.ADIE bit is 1 (interrupt generation upon scanning completion enabled).
(7) If the ADGSPCR.GBRSCN bit is 1 (scan for the group is restarted after having been discontinued due to group priority operation), scan for the ANn channels of group B selected in the ADANSB0 and ADANSB1 registers, restarts from the channel with the smallest number n while the ADCSR.ADST bit remains 1. If the ADGSPCR.LGRRS bit is set to 1 at this time, scan for group B starts from the channel on which A/D conversion was discontinued.
(8) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy)
(9) A group B scan end interrupt request is generated if the ADCSR.GBADIE bit is 1 (interrupt generation upon group B scan completion enabled).
(10) If the ADGSPCR.GBRSCN bit is 1 (scan for the group is restarted after having been discontinued due to group priority operation), scan for the ANn channels of group C selected in the ADANSC0 and ADANSC1 registers, restarts from the channel with the smallest number n while the ADCSR.ADST bit remains 1. If the ADGSPCR.LGRRS bit is set to 1 at this time, scan for group C starts from the channel on which A/D conversion was discontinued.
(11) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy)
(12) A group C scan end interrupt request is generated if the ADCSR.GBADIE bit is 1 (interrupt generation upon group C scan completion enabled).
(13) If the ADGSPCR.GBRP bit is set to 1 (single scan is continuously operated), scan for the ANn channels of group C selected in the ADANSC0 and ADANSC1 registers, restarts from the channel with the smallest number n while the ADCSR.ADST bit remains 1.

To continuously operate single scan for group C, disable trigger input for group B.
Steps 13, 11, 12, and then 13 are repeated as long as the ADGSPCR.GBRP bit remains 1.
Clearing of the ADCSR.ADST bit to 0 is prohibited while the ADGSPCR.GBRP bit is set to 1.
To forcibly stop scanning when ADGSPCR.GBRP = 1, follow the procedures for clear operation by software through the

ADCSR.ADST bit shown in section 31.6.2, Notes on Stopping A/D Conversion.

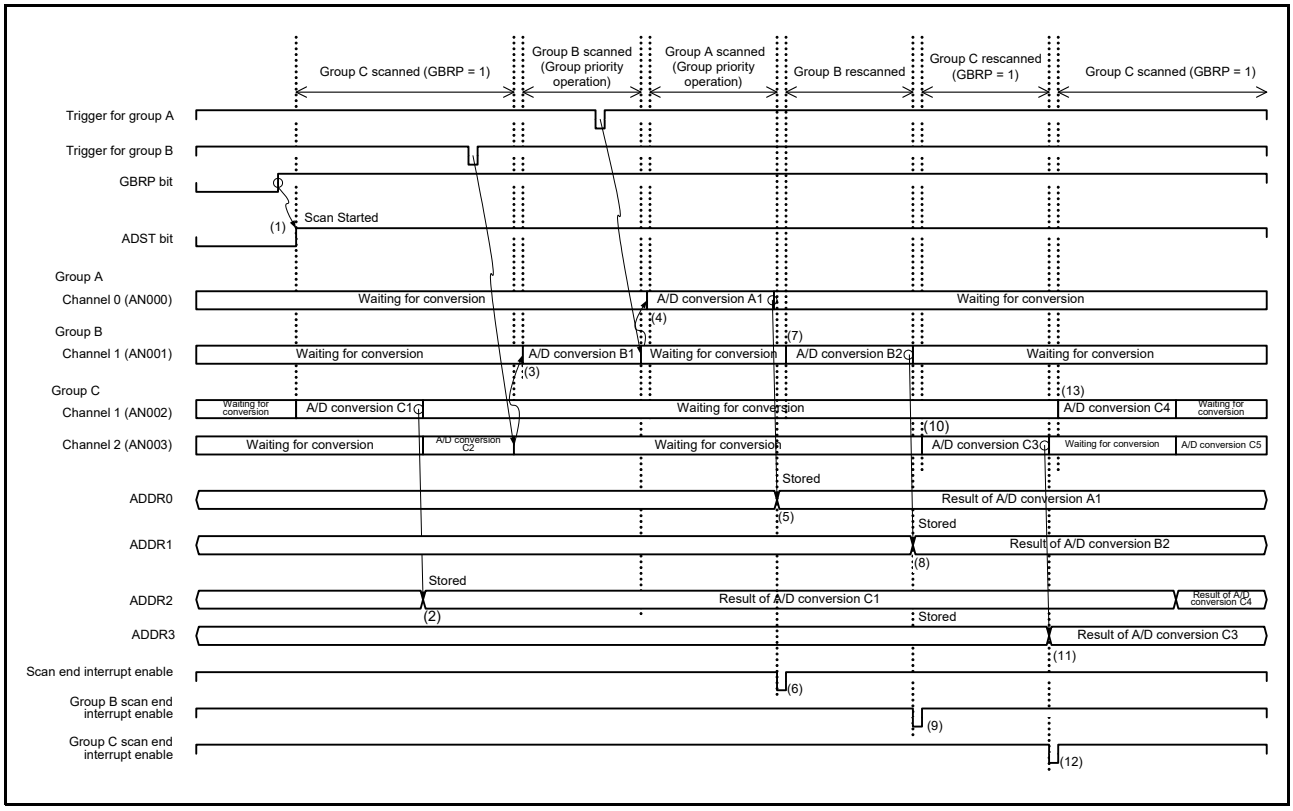


Figure 31.28 Example 5 for Group Priority Operation: Continuous Single Scan Operation on Group C (ADGSPCR.GBRP = 1, ADGSPCR.LGRRS = 1)

31.3.5 Analog Input Sampling Time and Scan Conversion Time

Figure 31.29 shows the scan conversion timing in single scan mode, in which scan conversion is activated by software or a synchronous trigger. Figure 31.30 shows the scan conversion timing in single scan mode, in which scan conversion is activated by an asynchronous trigger. The scan conversion time (t_{SCAN}) includes the start-of-scanning-delay time (t_D), channel-dedicated sample-and-hold circuit processing time (t_{SPLSH})*1, disconnection detection assistance processing time (t_{DIS})*2, self-diagnosis A/D conversion processing time (t_{DIAG})*3, A/D conversion processing time (t_{CONV}), channel-dedicated sample-and-hold circuit end time (t_{SHED})*4, and end-of-scanning-delay time (t_{ED}).
The A/D conversion processing time (t_{CONV}) consists of sampling time (t_{SPL}) and time for conversion by successive approximation (t_{SAM}). The sampling time (t_{SPL}) is used to charge sample-and-hold circuits in the A/D converter. If there is not sufficient sampling time due to the high impedance of an analog input signal source, or if the A/D conversion clock (ADCLK) is slow, sampling time can be adjusted using the ADSSTR register.
The time for conversion by successive approximation (t_{SAM}) is at 32 ADCLK states. Table 31.16 shows the scan conversion time.

The scan conversion time (t_{SCAN}) in single scan mode for which the number of selected channels is n can be determined as follows:

$$t_{SCAN} = t_D + t_{SPLSH} + (t_{DIS} \times n) + t_{DIAG} + (t_{CONV} \times n)^{*5} + t_{ED}$$

The scan conversion time for the first cycle in continuous scan mode is t_{SCAN} for single scan minus t_{ED} plus t_{SHED}.
The scan conversion time for the second and subsequent cycles in continuous scan mode is fixed to $t_{SPLSH} + (t_{DIS} \times n) + t_{DIAG} + t_{DSD} + (t_{CONV} \times n)^{*5} + t_{SHED}$.

Note 1. When no channel-dedicated sample-and-hold circuits are used, t_{SPLSH} = 0.
Note 2. When disconnection detection assistance is not selected, t_{DIS} = 0. The auto-discharge period of 15 ADCLK states is inserted only when internal reference voltage is A/D-converted.
Note 3. When the self-diagnosis function is not used, t_{DIAG} = 0, t_{DSD} = 0.
Note 4. When no channel-dedicated sample-and-hold circuits are used, t_{SHED} = 0. Here, continuous scan mode is assumed. In single scan mode and group scan mode, t_{SHED} is included in the end-of-scanning-delay time (t_{ED}).
Note 5. t_{CONV} × n when the sampling time (t_{SPL}) of selected channels is the same, but it is the total of the sampling time of each channel and time for conversion by successive approximation (t_{SAM}).

Table 31.16 Times for Conversion during Scanning (in Numbers of Cycles of ADCLK and PCLK)

Item			Symbol		Type/Conditions: Synchronous Trigger (MTU)	Synchronous Trigger (TMR)	Asynchronous Trigger	Software Trigger	Unit
Scan start processing time*1, *2	A/D conversion on group under group priority control.	The low-priority group is to be stopped. (The priority group is activated after low-priority group B is stopped due to an A/D conversion source of the priority group.)	t_D		1 PCLKA + 4 PCLKB + 6 ADCLK	3 PCLKB + 6 ADCLK	—	—	Cycle
		The low-priority group is not to be stopped. (Activation by an A/D conversion source of the priority group.)			1 PCLKA + 3 PCLKB + 4 ADCLK	2 PCLKB + 4 ADCLK	—	—	
	A/D conversion when self-diagnosis is enabled	A/D conversion for self-diagnosis is to be started.			1 PCLKA + 3 PCLKB + 6 ADCLK	2 PCLKB + 6 ADCLK	4 PCLKB+ 6 ADCLK	6 ADCLK	
	Other than above				1 PCLKA + 3 PCLKB + 4 ADCLK	2 PCLKB + 4 ADCLK	2 PCLKB + 4 ADCLK	4 ADCLK	
Channel-dedicated sample-and-hold processing time*1	Sampling time		t_{SPLSH}	t_{SH}	The setting of ADSHCR.SSTSH[7:0] (initial value = 1Ah) × ADCLK				
	Wait time between sampling and A/D conversion			t_W	13 ADCLK				
Disconnection detection assistance processing time			t_{DIS}		The setting of ADNDIS[3:0] (initial value = 00h) × ADCLK*3				
Self-diagnosis conversion processing time*1	Sampling time		t_{DIAG}	t_{SPL}	The setting of ADSSTR0 (initial value = 0Dh) × ADCLK				
	Time for conversion by successive approximation			t_{SAM}	32 ADCLK				
	Normal A/D conversion is to be started after completion of self-diagnosis conversion.		t_{DED}		2 ADCLK				
	A/D conversion for self-diagnosis is to be started after completion of conversion for continuous scan on the last channel specified.		t_{DSD}		2 ADCLK				
A/D conversion processing time*1	Sampling time		t_{CONV}	t_{SPL}	The setting of ADSSTRn (n = 0 to 11, L, O) (initial value = 0Dh) × ADCLK				
	Time for conversion by successive approximation			t_{SAM}	32 ADCLK				
Channel-dedicated sample-and-hold end processing time			t_{SHED}		3 ADCLK				
Scan end processing time*1			t_{ED}		1 PCLKB + 3 ADCLK				

Note 1. For t_D, t_{SPLSH}, t_{DIAG}, t_{CONV}, and t_{ED}, see Figure 31.29 and Figure 31.30.
Note 2. This is the maximum time required from software writing or trigger input to A/D conversion start.
Note 3. The value is fixed to 0Fh (15 ADCLK) when the internal reference voltage is A/D-converted.

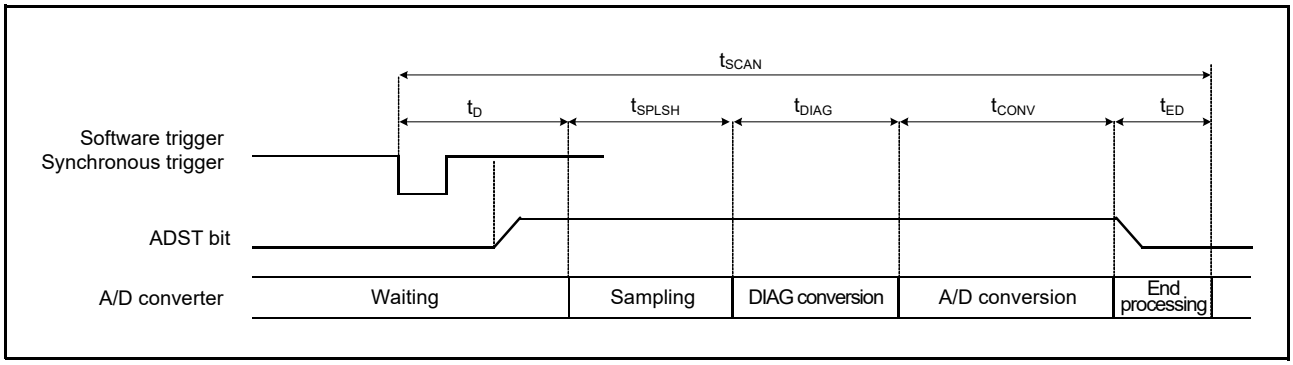


Figure 31.29 Scan Conversion Timing (Activated by Software or Synchronous Trigger)

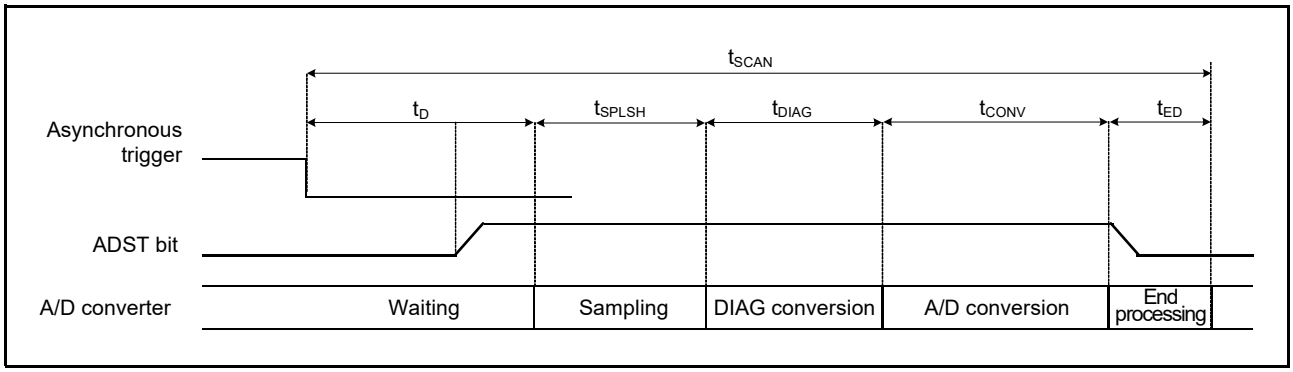


Figure 31.30 Scan Conversion Timing (Activated by Asynchronous Trigger)

31.3.6 Usage Example of A/D Data Register Automatic Clearing Function

Setting the ADCER.ACE bit to 1 automatically clears the A/D data registers (ADDRy, ADRD, ADOCDR, ADDBLDR, ADDBLDRA, ADDBLDRB) to 0000h when the A/D data registers (ADDRy, ADRD, ADOCDR, ADDBLDR, ADDBLDRA, ADDBLDRB) are read by the CPU or DTC.
This function enables detection of update failures of the A/D data registers (ADDRy, ADRD, ADOCDR, ADDBLDR, ADDBLDRA, ADDBLDRB). The following describes the examples in which the function to automatically clear the ADDRy register is enabled and disabled.
In a case where the ADCER.ACE bit is 0 (automatic clearing disabled), if the A/D conversion result (0222h) is not written to the ADDRy register for some reason, the old data (0111h) will be the ADDRy value. Furthermore, if this ADDRy value is read into a general register using an A/D scan end interrupt, the old data (0111h) can be saved in the general register. When checking whether there is an update failure, it is necessary to frequently save the old data in the RAM or a general register.
In a case where the ADCER.ACE bit is 1 (automatic clearing enabled), when ADDRy = 0111h is read by the CPU or DTC, ADDRy is automatically cleared to 0000h. After that, if the A/D conversion result 0222h cannot be transferred to ADDRy for some reason, the cleared data (0000h) remains as the ADDRy value. If this ADDRy value is read into a general register using an A/D scan end interrupt at this point, 0000h will be saved in the general register.
Occurrence of an ADDRy update failure can be determined by simply checking that the read data value is 0000h.

31.3.7 A/D-Converted Value Addition/Average Mode

In A/D-converted value addition mode, the same channel is A/D-converted 2, 3, 4, or 16 consecutive times and the sum of the converted values is stored in the data register. In A/D-converted value average mode, the same channel is A/D-converted two or four consecutive times and the mean of the converted values is stored in the data register. The use of the average of these results can improve the accuracy of A/D conversion, depending on the types of noise components that are present. This function, however, cannot always guarantee an improvement in A/D conversion accuracy.
The A/D-converted value addition/average mode can be used when A/D conversion of the channel select analog input or internal reference voltage (for S12AD2 only) is selected.

31.3.8 Disconnection Detection Assist Function

This converter incorporates the function to fix the charge for sampling capacitance to the specified state (reference voltage selected by the A/D high-potential/low-potential reference voltage control register) before start of A/D conversion. This function enables disconnection detection in wiring of analog inputs. The disconnection detection assist function should be used while ADPGACR.PnENAMP = 0 (does not use the amplifier in the PGA) and ADSHCR.SHANS = 0 (bypass the sample-and-hold circuits).
Figure 31.31 illustrates the A/D conversion operation when the disconnection detection assist function is used. Figure 31.32 shows an example of disconnection detection when precharge is selected. Figure 31.33 shows an example of disconnection detection when discharge is selected.

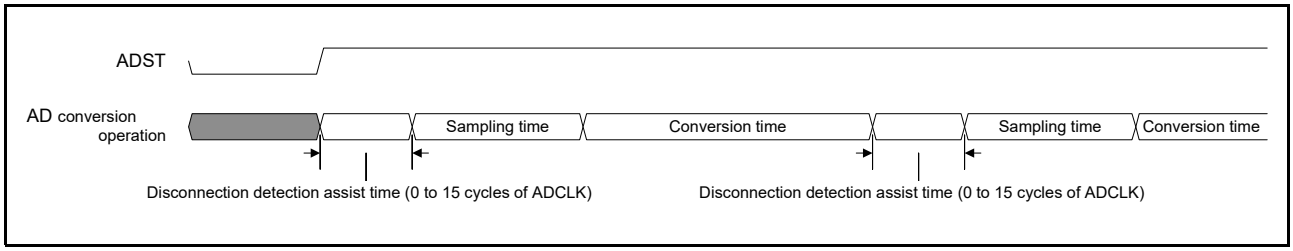
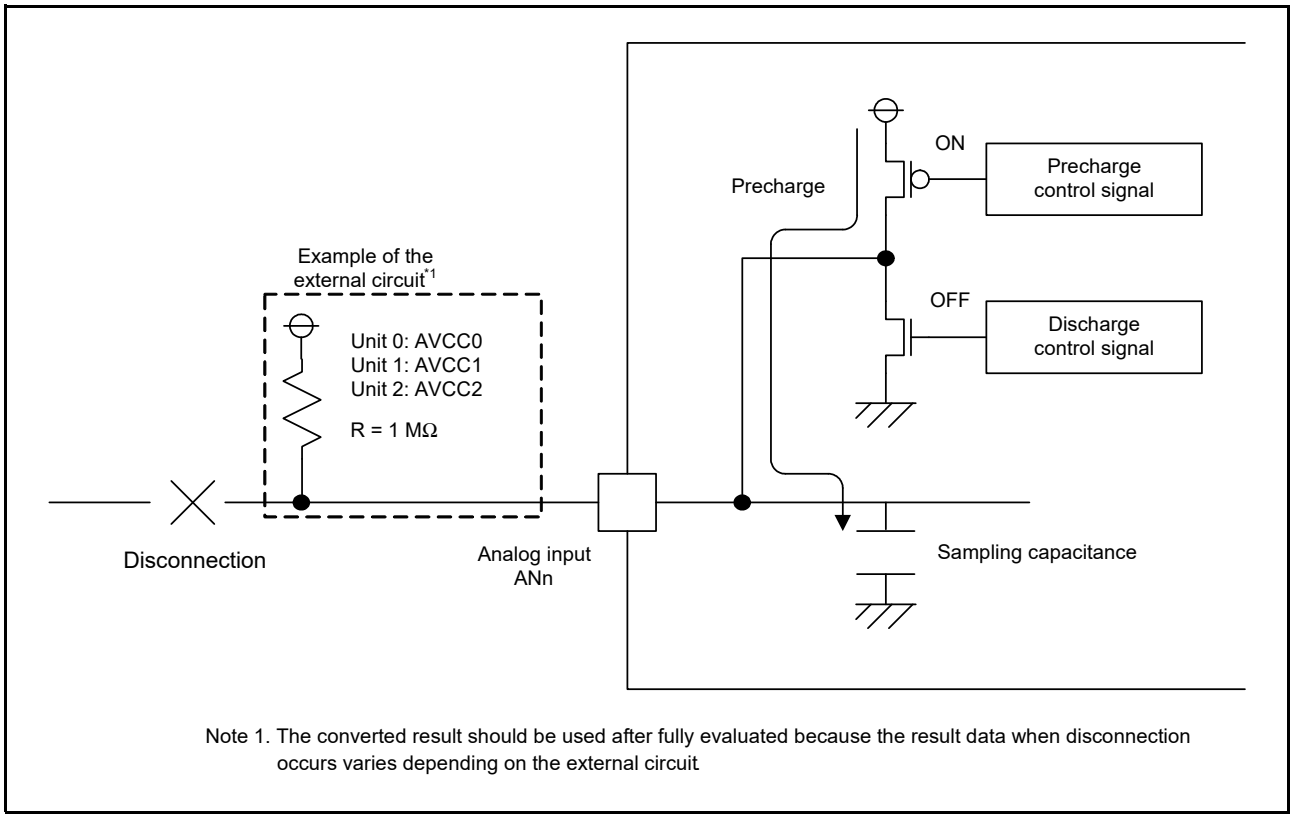
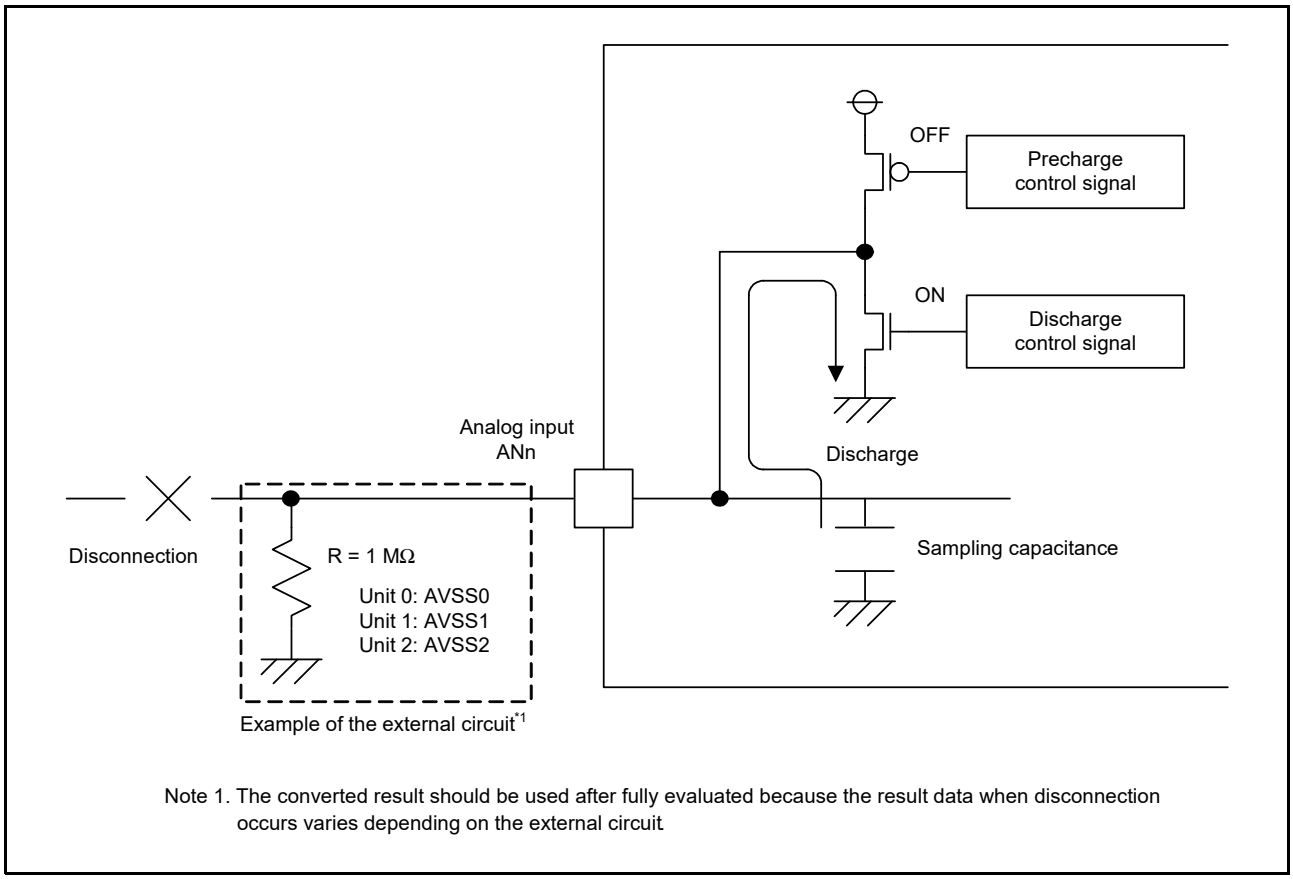


Figure 31.31 Operation of A/D Conversion When the Disconnection Detection Assist Function is Used



Note 1. The converted result should be used after fully evaluated because the result data when disconnection occurs varies depending on the external circuit.

Figure 31.32 Example of Disconnection Detection When Precharge is Selected



Note 1. The converted result should be used after fully evaluated because the result data when disconnection occurs varies depending on the external circuit.

Figure 31.33 Example of Disconnection Detection When Discharge is Selected

31.3.9 Starting A/D Conversion with Asynchronous Trigger

The A/D conversion can be started by the input of an asynchronous trigger. To start up the A/D converter by an asynchronous trigger, the A/D conversion start trigger select bits (ADSTRGR.TRSA[5:0]) should be set to 000000b, and a high-level signal should be input to the asynchronous trigger (ADTRG0# pin). Then, the ADCSR.TRGE and ADCSR.EXTRG bits should be set to 1. Figure 31.34 shows a timing of the asynchronous trigger input.
For the time from when the ADST bit is set to 1 until conversion starts, refer to section 31.6.3, A/D Conversion Restarting Timing and Termination Timing. An asynchronous trigger cannot be selected for group B used in group scan mode.

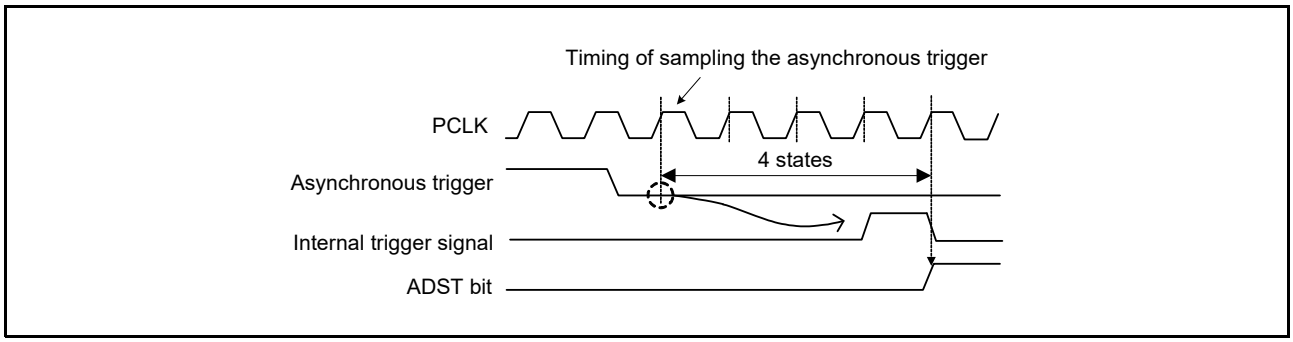


Figure 31.34 Timing of Sampling Asynchronous Trigger

31.3.10 Starting A/D Conversion with Synchronous Trigger from Peripheral Module

The A/D conversion can be started by a synchronous trigger. To start the A/D conversion by a synchronous trigger, the ADCSR.TRGE bit should be set to 1, the ADCSR.EXTRG bit should be cleared to 0, and the relevant sources should be selected by the ADSTRGR.TRSA[5:0] and ADSTRGR.TRSB[5:0] bits.

31.3.11 Programmable Gain Amplifier

A programmable gain amplifier is included in AN000 and AN100 to AN102. Select the gain by setting the S12AD.ADPGAGS.P000GAIN[3:0] bits for the AN000 pin and the S12AD1.ADPGAGS.PnGAIN[3:0] bits (n = 100 to 102) for the AN100 to AN102 pins. Select the operational amplifier to be used by setting the S12AD.ADPGACR.P000SEL1 bit for the AN000 pin and the S12AD1.ADPGACR.PnSEL1 bit (n = 100 to 102) for the AN100 to AN102 pins.
The relationship between pin voltage and conversion voltage can be converted into the following formula.

$$Vpout = G \times (Vpin - Vpgavss) + Vpgavss$$

Vpout: Conversion voltage of the A/D converter
G: Gain selected in the S12AD.ADPGAGS.P000GAIN[3:0] bits and S12AD1.ADPGAGS.PnGAIN[3:0] bits (n = 100 to 102)
Vpin: AN000, AN100 to AN102 pin voltage
Vpgavss: PGAVSS0, PGAVSS1 pin voltage

After setting the S12AD.ADPGACR.P000ENAMP bit for the AN000 pin or the S12AD1.ADPGACR.PnENAMP bit (n = 100 to 102) for the AN100 to AN102 pins to 1, wait for the period for stabilizing of the programmable gain amplifier operation and set the ADCSR.ADST bit of the unit to 1.

31.4 Interrupt Sources and DTC Transfer Requests

31.4.1 Interrupt Requests

The 12-bit A/D converter can send scan end interrupt requests S12ADI/S12ADI1/S12ADI2, GBADI/GBADI1/GBADI2, and GCADI/GCADI1/GCADI2 to the CPU.
Setting the ADCSR.ADIE bit to 1 and 0 enables and disables an S12ADI/S12ADI1/S12ADI2 interrupt, respectively; similarly, setting the ADCSR.GBADIE bit to 1 and 0 enables and disables a GBADI/GBADI1/GBADI2 interrupt, respectively.
In addition, the DTC can be activated when an S12ADI/S12ADI1/S12ADI2, a GBADI/GBADI1/GBADI2, or GCADI/GCADI1/GCADI2 interrupt is generated. Using an S12ADI/S12ADI1/S12ADI2, a GBADI/GBADI1/GBADI2, or GCADI/GCADI1/GCADI2 interrupt to allow the DTC to read the converted data enables sequence conversion without burden on software.
For details on DTC settings, see section 17, Data Transfer Controller (DTCa).

31.5 Allowable Impedance of Signal Source

To achieve high-speed conversion of 1.0 µs, the analog input pins of this MCU are designed so that the conversion accuracy is guaranteed if the impedance of the input signal source is 0.3 kΩ or less. If an external capacitor of large capacitance is attached in the application in which only a single pin input is converted in single scan mode, the only load on input is virtually 1.0 kΩ of the internal input resistor; therefore, the impedance of the signal source can be ignored. Being a low-pass filter, however, an analog input circuit may not follow the analog signal with a large differential coefficient. When high-speed analog signals are to be converted or multiple pins are to be converted in scan mode, a low-impedance buffer should be used.
Figure 31.35 shows an equivalent circuit of an analog input pin and an external sensor.
To perform A/D conversion accurately, charging of the internal capacitor C shown in Figure 31.35 must be completed within the specified period of time. This specified period is referred to as sampling time.

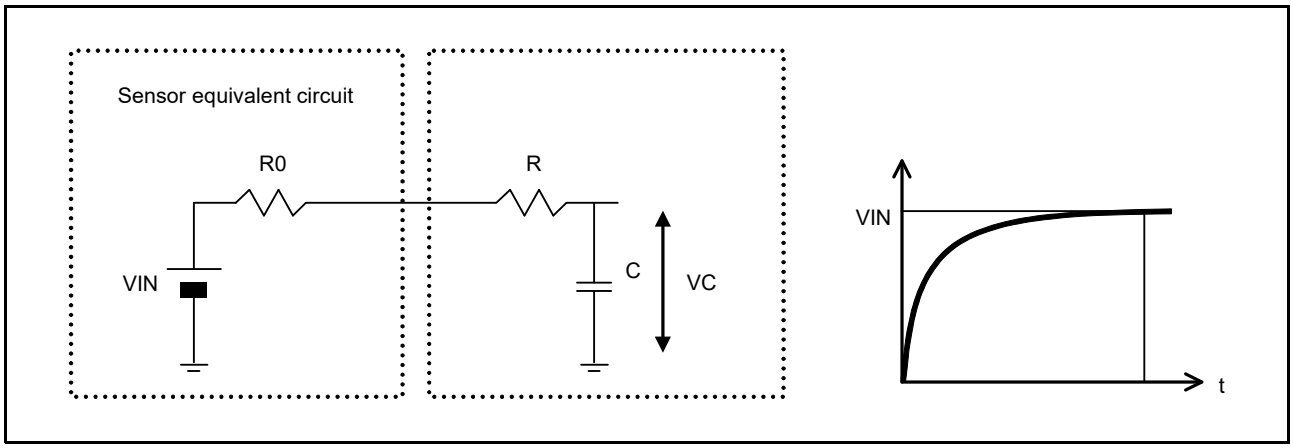


Figure 31.35 Equivalent Circuit of Analog Input Pin and External Sensor

31.6 Usage Notes

31.6.1 Notes on Reading Data Registers

The A/D data registers, A/D data duplication registers, A/D data duplication register A, A/D data duplication register B A/D internal reference voltage data register (for S12AD2 only), and A/D self-diagnosis data register should be read in 16-bit units. If a register is read twice in 8-bit units, that is, the higher-order byte and lower-order byte are separately read, the A/D-converted value having been read first may disagree with the A/D-converted value having been read for the second time. To prevent this, the data registers should never be read in 8-bit units.

31.6.2 Notes on Stopping A/D Conversion

To stop A/D conversion when an asynchronous trigger or a synchronous trigger has been selected as the condition for starting A/D conversion, follow the procedure in Figure 31.36.

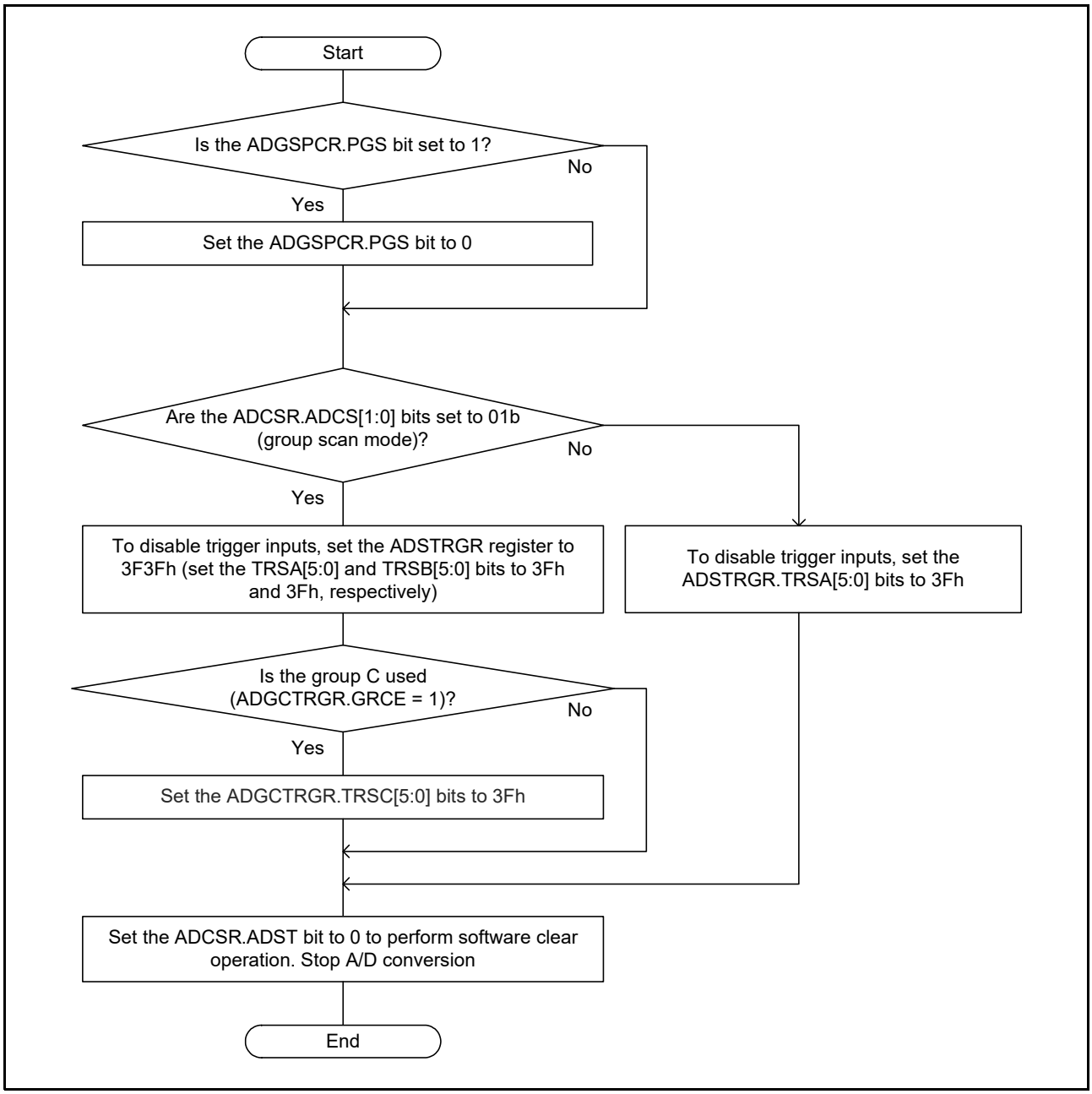


Figure 31.36 Procedure for Clear Operation by Software through the ADCSR.ADST Bit

31.6.3 A/D Conversion Restarting Timing and Termination Timing

It takes a maximum of six ADCLK cycles for the idle analog unit of the 12-bit A/D converter to be restarted by setting the ADCSR.ADST bit to 1. It takes a maximum of three ADCLK cycles for the operating analog unit of the 12-bit A/D converter to be terminated by setting the ADCSR.ADST bit to 0.

31.6.4 Notes on Scan End Interrupt Handling

When scanning the same analog input twice using any trigger, the first A/D-converted data is overwritten with the second A/D-converted data in the case that the CPU does not complete reading the A/D-converted data by the time the A/D conversion of the first analog input for the second scan ends after the first scan end interrupt is generated.

31.6.5 Module Stop Function Setting

Operation of the 12-bit A/D converter can be disabled or enabled by setting module stop control register. The initial setting is for operation of the 12-bit A/D converter to be halted. Register access is enabled by releasing the module stop state.
After the module stop state is released, wait for 1 µs to start A/D conversion. For details, refer to section 11, Low Power Consumption.

31.6.6 Notes on Entering Low Power Consumption States

Before entering the module stop state or software standby mode, make sure to stop A/D conversion. Here, set the ADCSR.ADST bit to 0, and secure certain period of time until the analog unit of the 12-bit A/D converter is stopped. Follow the procedure given below to secure this time.
Set the ADCSR.ADST bit to 0 by following the procedure in Figure 31.36 Procedure for Clear Operation by Software through the ADCSR.ADST Bit. Then wait for three clock cycles of ADCLK before entering the module stop mode or software standby mode.

31.6.7 Notes on Canceling Software Standby Mode

After software standby mode is canceled, wait until the crystal oscillation stabilization time or the PLL circuit stabilization time elapses, and then wait for 1 µs before starting A/D conversion. For details, refer to section 11, Low Power Consumption.

31.6.8 Error in Absolute Accuracy When Disconnection Detection Assistance is in Use

Using disconnection detection assistance leads to an error in absolute accuracy of the A/D converter. This is because an error voltage is input to the analog input pins due to the resistive voltage division between the pull-up or pull-down resistor (Rp) and the resistance of the signal source (Rs). The disconnection detection assist function should be used while ADPGACR.PnENAMP = 0 (does not use the amplifier in the PGA) and ADSHCR.SHANS = 0 (bypass the sample-and-hold circuits). This error in absolute accuracy is calculated from the following formula. Only use disconnection detection assistance after thorough evaluation.

Maximum error in absolute accuracy (LSB) = 4095 × Rs / Rp

31.6.9 Voltage Range of Analog Power Supply Pins

If this MCU is used with the voltages outside the following ranges, the reliability of the MCU may be affected.

- Analog input voltage range
  Voltage applied to analog input pins AN000 to AN003, AN100 to AN103, AN200 to AN211, AN016, and AN116:
  AVSSn ≤ VANn ≤ AVCCn (n = 0 to 2)
- Relationship between power supply pin pairs (AVCCn–AVSSn, VREFHn–VREFLn, VCC–VSS)
  The following condition should be satisfied: AVSSn = VSS (n = 0 to 2). The relationship between VREFHn and AVCCn must be set as VREFHn = AVCCn (n = 0 to 2) and the relationship between VREFLn and AVSSn must be set as VREFLn = AVSSn (n = 0 to 2).
  When performing A/D conversion of analog input pins AN016 and AN116, the following condition should be satisfied: AVCCn = VREFHn = VCC.
  A 0.1-µF capacitor should be connected between each pair of power supply pins to create a closed loop with the shortest route possible as shown in Figure 31.37, and connection should be made so that the following condition is satisfied at the supply side: AVSSn = VREFLn = VSS
  When the 12-bit A/D converter is not used, the following conditions should be satisfied:
  AVCCn = VREFHn = VCC and AVSSn = VREFLn = VSS

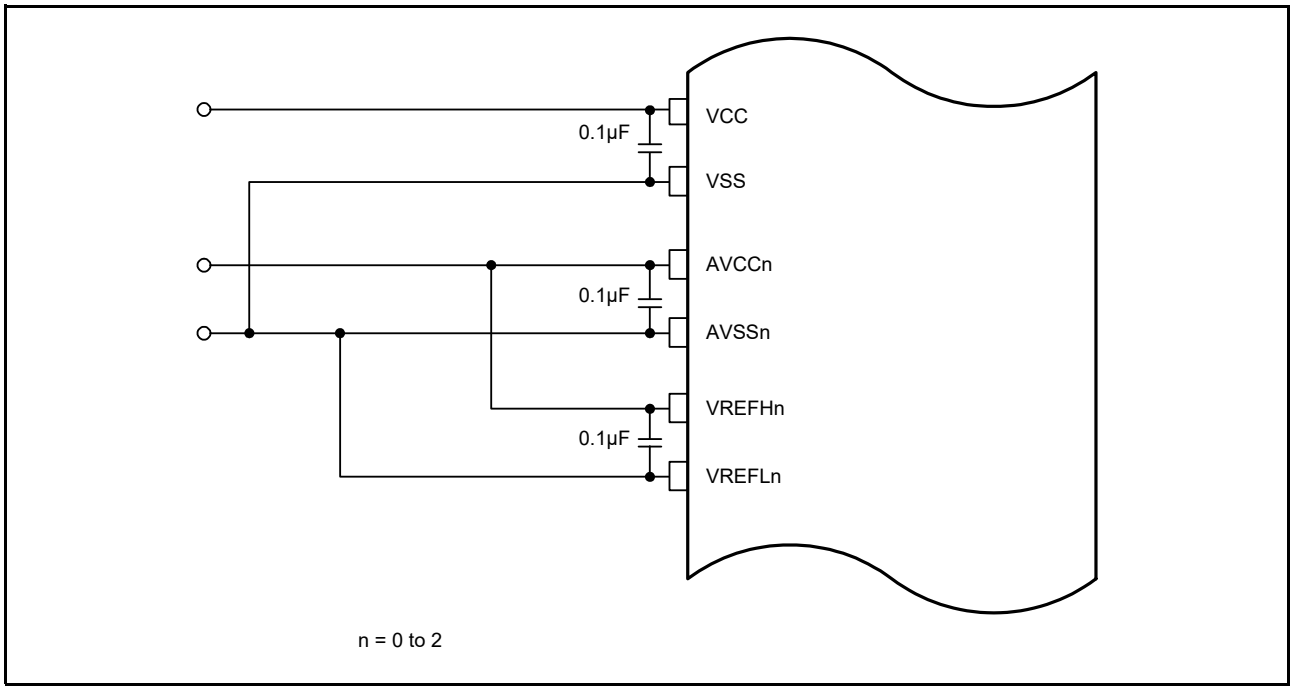


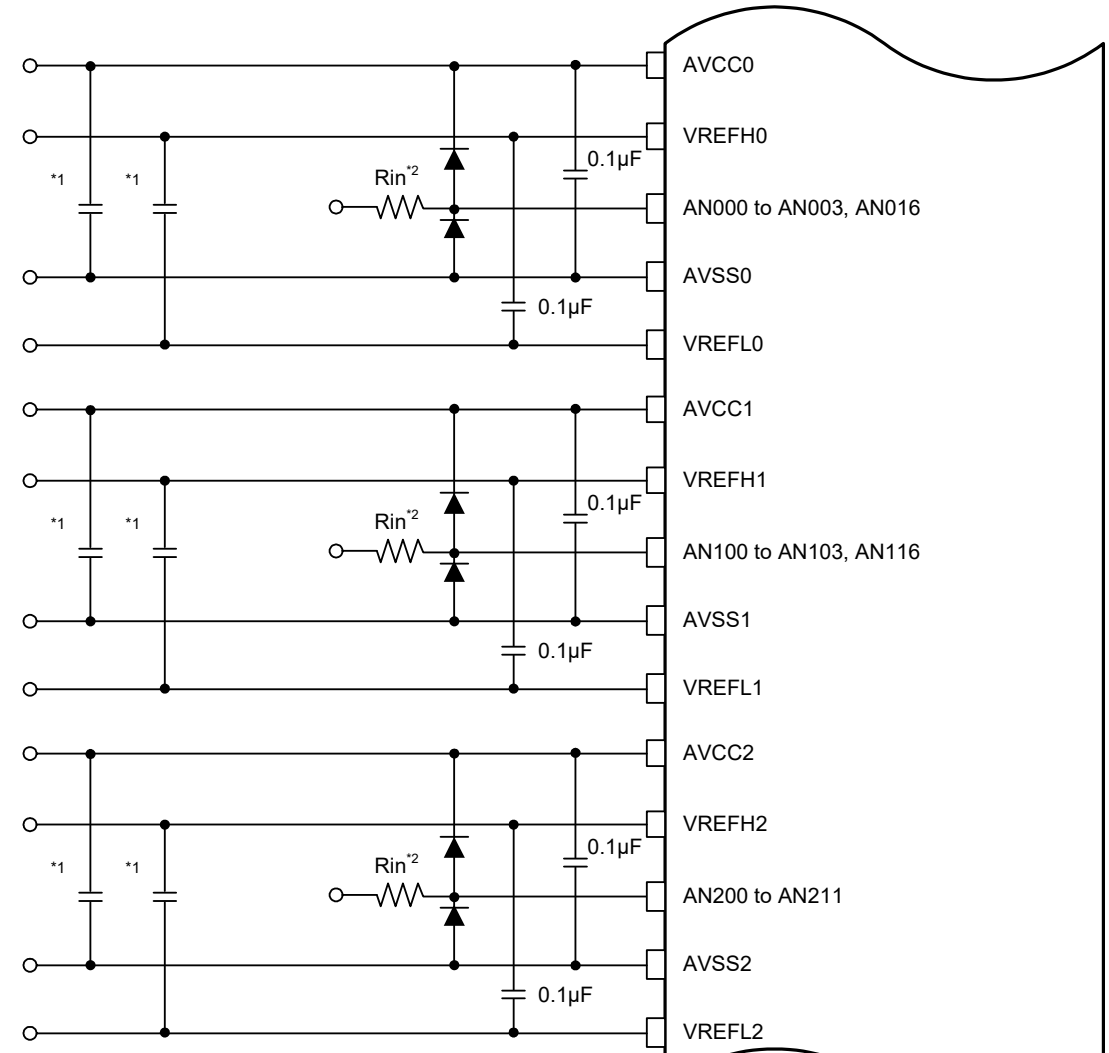
Figure 31.37 Power Supply Pin Connection Example

31.6.10 Notes on Board Design

The board should be designed so that digital circuits and analog circuits are separated from each other as far as possible. In addition, digital circuit signal lines and analog circuit signal lines should not intersect or placed near each other. If these rules are not followed, noise will be produced on analog signals and A/D conversion accuracy will be affected. The analog input pins (AN000 to AN003, AN100 to AN103, AN200 to AN211, AN016, and AN116), reference power supply pin (VREFHn), reference ground pin (VREFLn), and analog power supply (AVCCn) should be separated from digital circuits using the analog ground (AVSSn). The analog ground (AVSSn) should be connected to a stable digital ground (VSS) on the board (single-point ground plane connection).

31.6.11 Notes on Noise Prevention

To prevent the analog input pins (AN000 to AN003, AN100 to AN103, AN200 to AN211, AN016, and AN116) from being destroyed by abnormal voltage such as excessive surge, a capacitor should be inserted between AVCCn and AVSSn, VREFHn and VREFLn, and a protection circuit should be connected to protect the above analog input pins as shown Figure 31.38.



Note 1. The values shown here are reference values.

Note 2. Rin: Signal source impedance

Figure 31.38 Sample Protection Circuit for Analog Inputs

32. D/A Converter (DAa)

32.1 Overview

This MCU includes two channels of 8-bit D/A converter.
Table 32.1 lists the specifications of the 8-bit D/A converter and Figure 32.1 shows a block diagram of the 8-bit D/A converter.

Table 32.1 Specifications of 8-Bit D/A Converter

Item	Specifications
Resolution	8 bits
Output channels	Two channels
Measure against mutual interference between analog modules	Measure against interference between D/A and A/D conversion D/A converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable input signal from the 12-bit A/D converter (unit 2). Therefore, the degradation of A/D conversion accuracy due to interference is reduced by controlling the timing in which the 8-bit D/A converter inrush current occurs, with the enable signal.
Low power consumption function	Module stop state can be set.

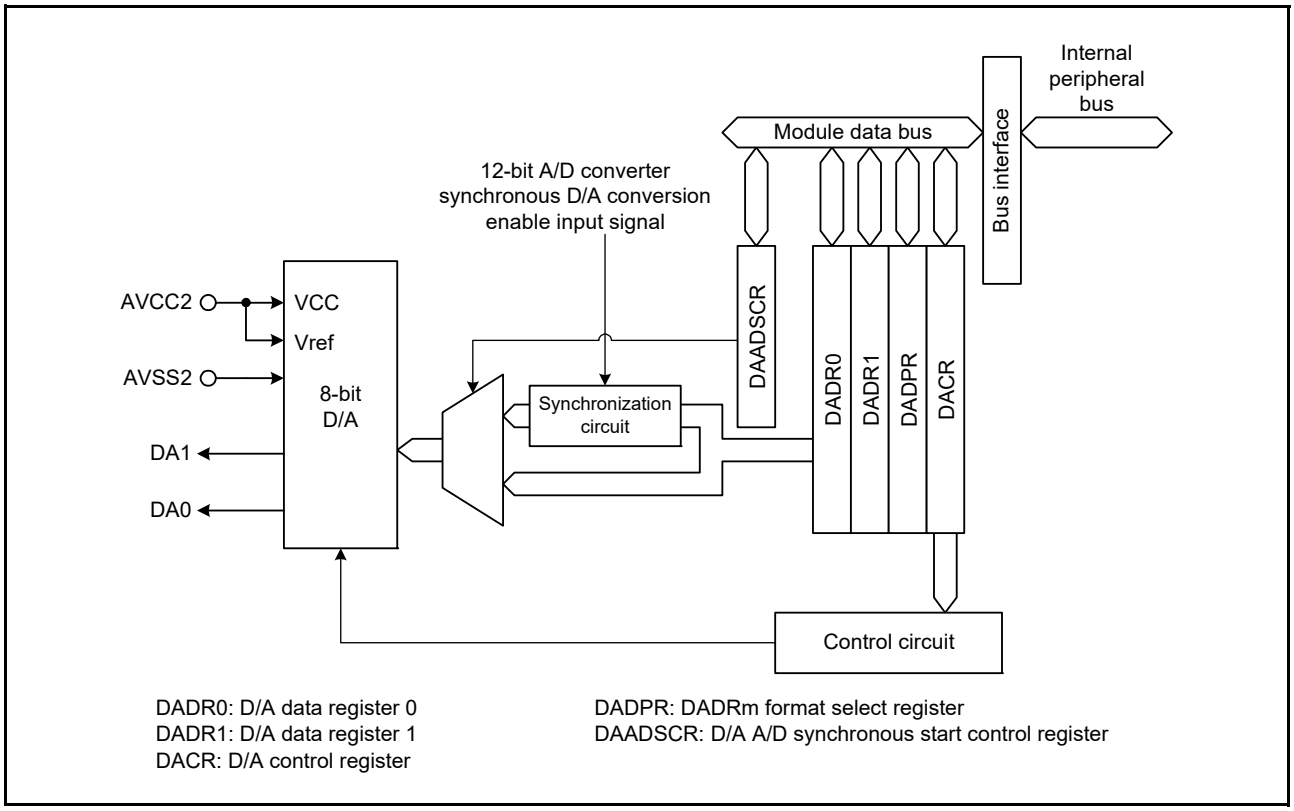


Figure 32.1 Block Diagram of 8-Bit D/A Converter

Table 32.2 lists the pin configuration of the 8-bit D/A converter.

Table 32.2 Pin Configuration of 8-Bit D/A Converter

Pin Name	I/O	Function
AVCC2	Input	Analog voltage supply pin for the 12-bit A/D converter (unit 2), the comparator C, and the 8-bit D/A converter. Connect this pin to AVCC0 or AVCC1 when not using these modules. Connect this pin to VCC when not using the 12-bit A/D converter unit 0 or unit 1 in addition to the above.
AVSS2	Input	Analog ground pin for the 12-bit A/D converter (unit 2), the comparator C, and the 8-bit D/A converter. Connect this pin to AVSS0 or AVSS1 when not using these modules. Connect this pin to VSS when not using the 12-bit A/D converter unit 0 or unit 1 in addition to the above.
DA0	Output	Channel 0 analog output pin
DA1	Output	Channel 1 analog output pin

32.2 Register Descriptions

32.2.1 D/A Data Register m (DADRm) (m = 0, 1)

Address(es): DA.DADR0 0008 80C0h, DA.DADR1 0008 80C2h

• DADPR.DPSEL bit = 0 (data is flush with the right end of the register)

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

• DADPR.DPSEL bit = 1 (data is flush with the left end of the register)

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
									—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The DADRm register is a 16-bit readable/writable register, which stores data to which D/A conversion is to be performed. Whenever an analog output is enabled, the values in DADRm are converted and output to the analog output pins.
8-bit data can be relocated by setting the DADPR.DPSEL bit.
Bits "—" are read as 0. The write value should be 0.

32.2.2 D/A Control Register (DACR)

Address(es): DA.DACR 0008 80C4h

	b7	b6	b5	b4	b3	b2	b1	b0
	DAOE1	DAOE0	—	—	—	—	—	—
Value after reset:	0	0	0	1	1	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R
b6	DAOE0	D/A Output Enable 0	0: Analog output of channel 0 (DA0) is disabled. 1: D/A conversion of channel 0 is enabled. Analog output of channel 0 (DA0) is enabled.	R/W
b7	DAOE1	D/A Output Enable 1	0: Analog output of channel 1 (DA1) is disabled. 1: D/A conversion of channel 1 is enabled. Analog output of channel 1 (DA1) is enabled.	R/W

This register should be set when the DAADSCR.DAADST bit is 1 (measure against interference between D/A and A/D conversion is enabled) while the 12-bit A/D converter (unit 2) is halted (the ADCSR.ADST bit is 0). At that time, the software trigger should be selected for the 12-bit A/D converter (unit 2) trigger to securely stop the 12-bit A/D converter (unit 2).

DAOE0 Bit (D/A Output Enable 0)

The DAOE0 bit controls the D/A conversion and analog output.

DAOE1 Bit (D/A Output Enable 1)

The DAOE1 bit controls the D/A conversion and analog output.

32.2.3 DADRm Format Select Register (DADPR) (m = 0, 1)

Address(es): DA.DADPR 0008 80C5h

	b7	b6	b5	b4	b3	b2	b1	b0
	DPSEL	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	DPSEL	DADRm Format Select	0: Data is flush with the right end of the D/A data register. 1: Data is flush with the left end of the D/A data register.	R/W

32.2.4 D/A A/D Synchronous Start Control Register (DAADSCR)

Address(es): DA.DAADSCR 0008 80C6h

	b7	b6	b5	b4	b3	b2	b1	b0
	DAADST	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	DAADST	D/A A/D Synchronous Conversion	0: 8-bit D/A converter operation does not synchronize with 12-bit A/D converter (unit 2) operation. (measure against interference between D/A and A/D conversion is disabled) 1: 8-bit D/A converter operation synchronizes with 12-bit A/D converter (unit 2) operation. (measure against interference between D/A and A/D conversion is enabled)	R/W

As a measure against interference between D/A and A/D conversion, the DAADSCR register selects whether or not the timing for starting 8-bit D/A conversion is synchronized with the 12-bit A/D converter synchronous D/A conversion enable input signal from the 12-bit A/D converter (unit 2).
This register should be set while the 12-bit A/D converter (unit 2) is halted (while the ADCSR.ADST bit is 0 after selecting software trigger as the 12-bit A/D converter (unit 2) trigger).

DAADST Bit (D/A A/D Synchronous Conversion)

Setting the DAADST bit to 0 allows the DADRm register value (m = 0, 1) to be converted into analog data at any time.
Setting the DAADST bit to 1 allows synchronous D/A conversion with the 12-bit A/D converter synchronous D/A conversion enable input signal from the 12-bit A/D converter (unit 2). Therefore, even if the DADRm register value is modified, D/A conversion does not start until the 12-bit A/D converter (unit 2) completes A/D conversion.
Set this bit while the ADCSR.ADST bit is set to 0. At this time, the software trigger should be selected for the 12-bit A/D converter trigger to securely stop the 12-bit A/D converter (unit 2).

32.3 Operation

The 8-bit D/A converter includes D/A conversion circuits for two channels, each of which can operate independently. When the DACR.DAOEm bit (m = 0, 1) is set to 1, D/A converter is enabled and the conversion result is output. An operation example of D/A conversion on channel 0 is shown below. Figure 32.2 shows the timing of this operation.

(1) Set the data for D/A conversion in the DADPR.DPSEL bit and the DADR0 register.

(2) Set the DACR.DAOE0 bit to 1 to start D/A conversion. The conversion result is output from the analog output pin DA0 after the conversion time tDCONV has elapsed. The conversion result continues to be output until the DADR0 register is written to again or the DAOE0 bit is cleared to 0. The output value (reference) is expressed by the following formula:

$$\frac{\text{Value of DADRm register}}{256} \times \text{AVCC2}$$

(3) If the DADR0 register is written to again, the conversion is started. The conversion result is output after the conversion time tDCONV has elapsed.
When the DAADSCR.DAADST bit is 1 (measure against interference between D/A and A/D conversion is enabled), it takes a maximum of one A/D conversion time for D/A conversion to start. When ADCLK is faster than the peripheral module clock, it may take longer than one A/D conversion time.

(4) If the DAOE0 bit is set to 0, analog output is disabled.

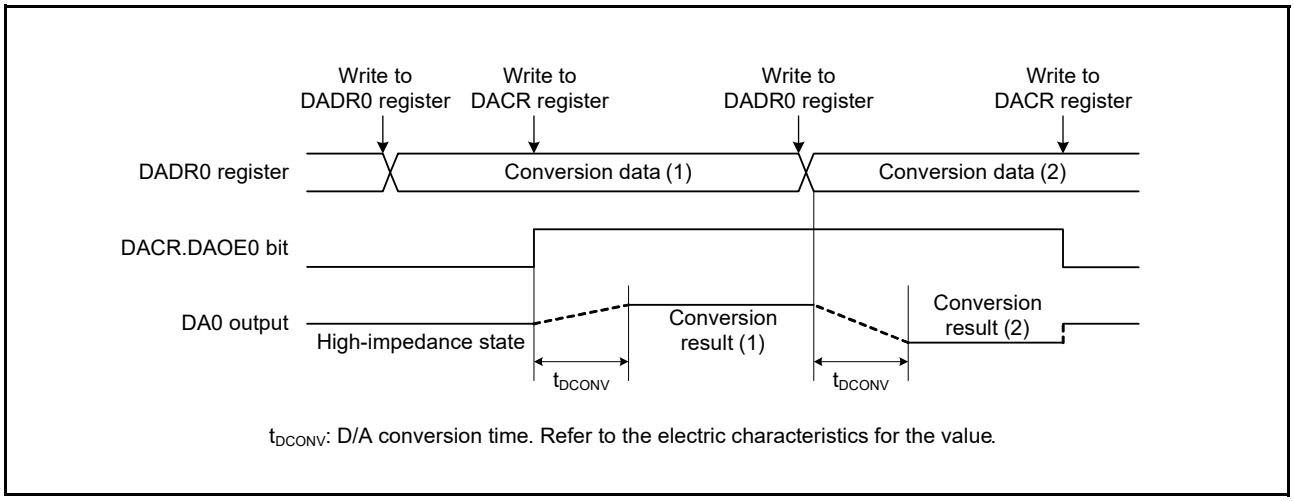


Figure 32.2 Example of 8-Bit D/A Converter Operation

32.3.1 Measure against Interference between D/A and A/D Conversion

When D/A conversion starts, an inrush current occurs to the 8-bit D/A converter. Since the same analog power supply is shared by the 8-bit D/A converter and 12-bit A/D converter (unit 2), the inrush current may interfere with the proper operation of the 12-bit A/D converter (unit 2).
With the DAADSCR.DAADST bit being 1, even if the DADRm register data (m = 0, 1) is modified during 12-bit A/D converter (unit 2) operation, D/A conversion does not start immediately but starts synchronously with A/D conversion completion. It takes a maximum of one A/D conversion time for the DADRm register data update to be reflected as the D/A conversion circuit input. Before reflection, the DADRm register value does not correspond to the analog output value.
When this function is enabled, it is impossible to check by any software means whether the DADRm register value has been D/A converted or not.
Even with the DAADSCR.DAADST bit being 1, when the DADRm register data is modified while the 12-bit A/D converter (unit 2) is halted, D/A conversion starts in one PCLKB cycle.
Figure 32.3 shows an example of channel 0 D/A conversion, in which the 8-bit D/A converter operates synchronously with the 12-bit A/D converter (unit 2).

(1) Confirm that the 12-bit A/D converter (unit 2) is halted. Set the DAADSCR.DAADST bit to 1.
(2) Confirm that the 12-bit A/D converter (unit 2) is halted. Set the DACR.DAOE0 bit to 1.
(3) Set the DADR0 register. When ADCLK is faster than the peripheral module clock, it may take longer than one A/D conversion time.

- If the 12-bit A/D conversion is halted (ADCSR.ADST bit = 0) when the DADR0 register is modified, D/A conversion starts in one PCLKB cycle.
- If the 12-bit A/D conversion is in progress (ADCSR.ADST bit = 1) when the DADR0 register is modified, D/A conversion starts upon A/D conversion completion. If the DADR0 register is modified twice during A/D conversion, the first update may not be converted.

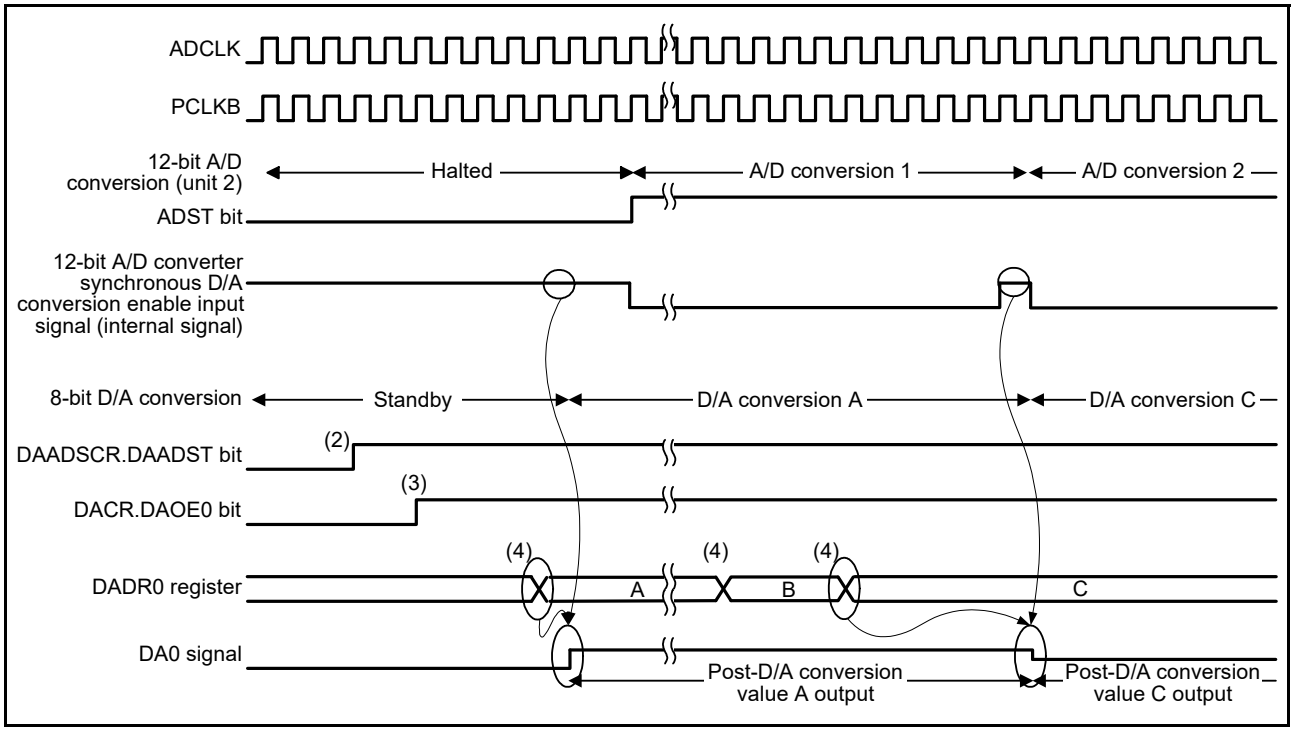


Figure 32.3 Example of Conversion When the 8-Bit D/A Converter is Synchronized with the 12-Bit A/D Converter (Unit 2)

When ADCLK is faster than PCLKB, the 8-bit D/A converter may not be able to capture a 12-bit A/D converter synchronous D/A conversion enable input signal for one ADCLK cycle which is output between A/D conversion 1 and A/D conversion 2.

Figure 32.4 shows example when the 8-bit D/A converter cannot capture the 12-bit A/D converter synchronous D/A conversion enable input signal. In this case, post-D/A conversion value A is continuously output as the DA0 signal.

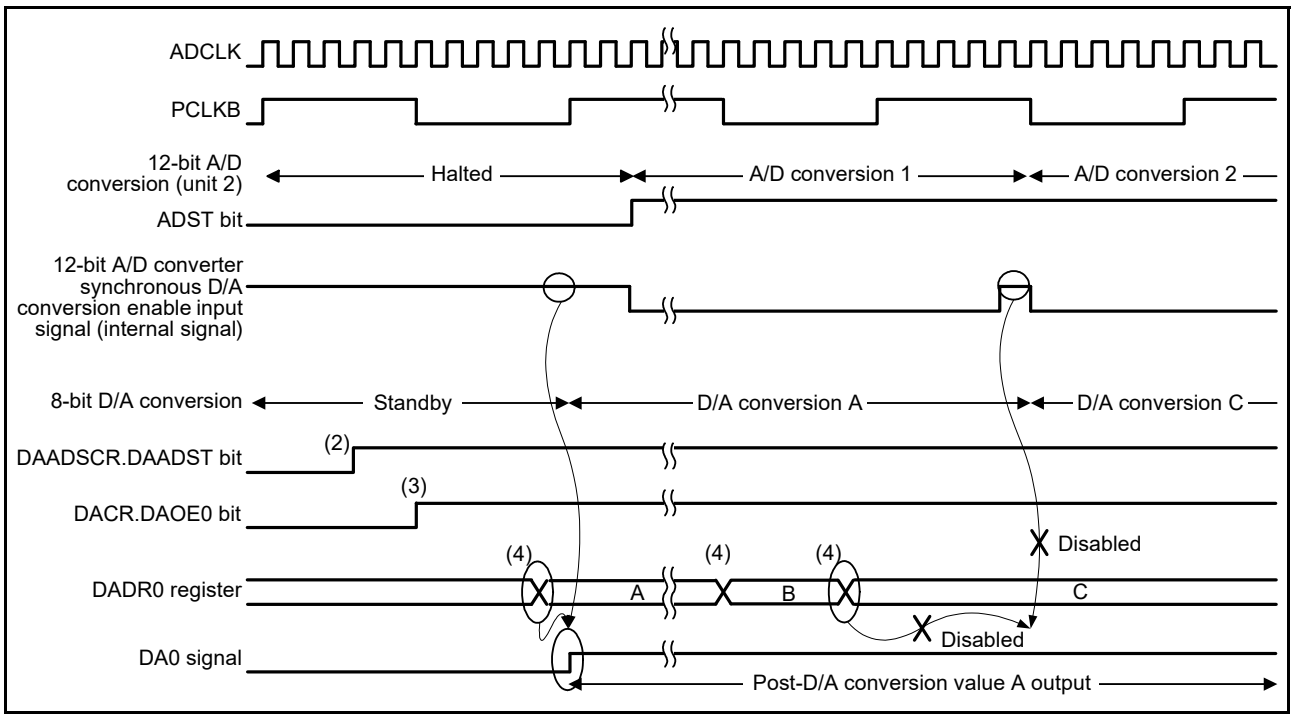


Figure 32.4 Example When the 8-Bit D/A Converter Cannot Capture the 12-Bit A/D Converter Synchronous D/A Conversion Enable Input Signal

32.4 Usage Notes

32.4.1 Module Stop Function Setting

Operation of the 8-bit D/A converter can be disabled or enabled using the module stop control register. The initial setting is for operation of the 8-bit D/A converter to be stopped. Register access is enabled by releasing the module stop state. For details, refer to section 11, Low Power Consumption.

32.4.2 Operation of the D/A Converter in Module Stop State

When the MCU enters the module stop state with D/A conversion enabled, the D/A converter outputs are retained, and the analog power supply current is the same as during D/A conversion. If the analog power supply current has to be reduced in the module stop state, disable D/A conversion by setting the DACR.DAOE1, and DAOE0 bits to 0.

32.4.3 Operation of the D/A Converter in Software Standby Mode

When the MCU enters software standby mode with D/A conversion enabled, the D/A converter outputs are retained, and the analog power supply current is the same as during D/A conversion. If the analog power supply current has to be reduced in software standby mode, disable D/A conversion by setting the DACR.DAOE1, and DAOE0 bits to 0.

32.4.4 Note on Usage When Measure against Interference between D/A and A/D Conversion is Enabled

When the DAADSCR.DAADST bit is 1 (measure against interference between D/A and A/D conversion is enabled), do not place the 12-bit A/D converter (unit 2) in the module stop state. It may halt D/A conversion in addition to A/D conversion.

32.4.5 Voltage Relationship between AVCC2 and VCC

AVCC2 and VCC voltages can be set individually, but the following restrictions apply.

- When the P23 and P24 pins are used as D/A converter output pins, make sure that the D/A converter output voltage does not exceed the VCC voltage.
- When the P23 and P24 pins are not used, these restrictions do not apply.

33. Comparator C (CMPC)

33.1 Overview

Comparator C compares a reference input voltage to an analog input voltage.
The comparison result can be read by software and output externally, and an interrupt request can be generated upon any changes to the comparison result.
The reference input voltage of comparator C is selectable as the on-chip D/A converter 0 output or the on-chip D/A converter 1 output.
There are four analog inputs, one of which is to be selected.
Table 33.1 lists the specification of comparator C, Figure 33.1 show a block diagram of comparator C, Table 33.2 shows comparator C pin configuration, and Table 33.3 shows analog input pin connections for comparator C.
In this section, “PCLK” is used to refer to PCLKB.

Table 33.1 Comparator C Specifications

Item	Specification
Number of channels	Four (comparator C0 to comparator C3)
Analog input voltages	Input voltage to the CMPCnm pin (n = channel number; m = 0 to 3)
Reference input voltage	Output voltage from on-chip D/A converter 0 or on-chip D/A converter 1
Comparison result	The comparison result can be output externally.
Digital filter function	• One of three sampling periods can be selected. • The filter function can also be disabled. • A noise-filtered signal can be used to generate the interrupt request output, POE source output, and GPT internal trigger source output, and the signal can be used to read the comparison result via registers.
Interrupt request	• An interrupt request is generated upon detecting a valid edge of the comparison result. • Rising edge, falling edge, or both edges of the comparison result can be selected.
Low power consumption function	Module stop state can be set.

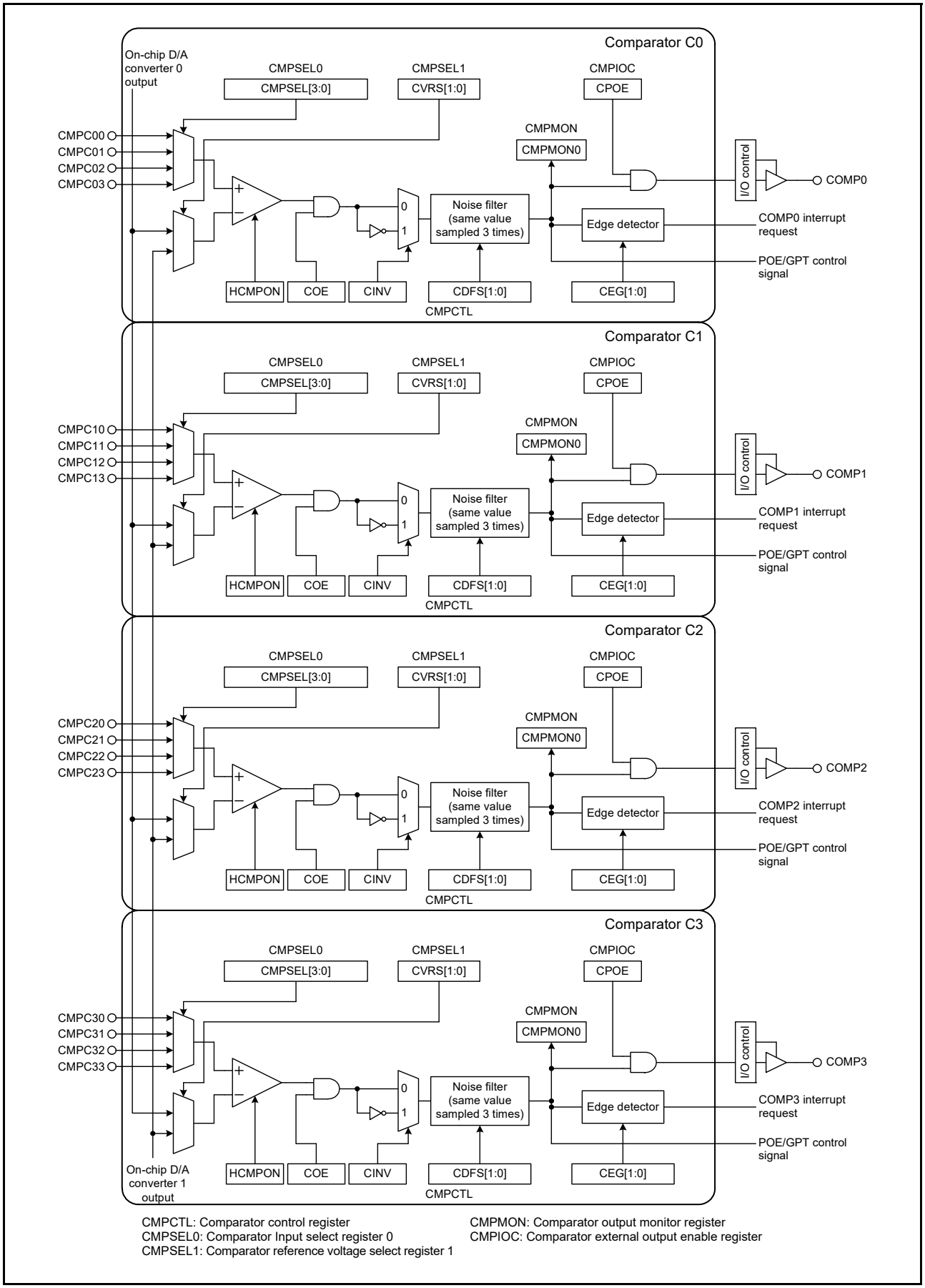


Figure 33.1 Block Diagram of Comparator C

Table 33.2 Comparator C Pin Configuration

Pin Name	I/O	Function
CMPC00, CMPC01, CMPC02, CMPC03	Input	Comparator C0 analog input pins
CMPC10, CMPC11, CMPC12, CMPC13	Input	Comparator C1 analog input pins
CMPC20, CMPC21, CMPC22, CMPC23	Input	Comparator C2 analog input pins
CMPC30, CMPC31, CMPC32, CMPC33	Input	Comparator C3 analog input pins
COMP0	Output	Comparator C0 comparison result output pin
COMP1	Output	Comparator C1 comparison result output pin
COMP2	Output	Comparator C2 comparison result output pin
COMP3	Output	Comparator C3 comparison result output pin

Table 33.3 Analog Input Pin Connections for Comparator C

Analog Input Pin	Connection
CMPC00	AN000 pin
CMPC01	Programmable gain amplifier output for AN000 pin
CMPC02	AN101 pin
CMPC03	Programmable gain amplifier output for AN101 pin
CMPC10	AN100 pin
CMPC11	Programmable gain amplifier output for AN100 pin
CMPC12	AN102 pin
CMPC13	Programmable gain amplifier output for AN102 pin
CMPC20	AN101 pin
CMPC21	Programmable gain amplifier output for AN101 pin
CMPC22	AN000 pin
CMPC23	Programmable gain amplifier output for AN000 pin
CMPC30	AN102 pin
CMPC31	Programmable gain amplifier output for AN102 pin
CMPC32	AN100 pin
CMPC33	Programmable gain amplifier output for AN100 pin

33.2 Register Descriptions

33.2.1 Comparator Control Register (CMPCTL)

Address(es): CMPC0.CMPCTL 000A 0C80h, CMPC1.CMPCTL 000A 0CA0h, CMPC2.CMPCTL 000A 0CC0h, CMPC3.CMPCTL 000A 0CE0h

	b7	b6	b5	b4	b3	b2	b1	b0
	HCMPON	CDFS[1:0]		CEG[1:0]		—	COE	CINV
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CINV	Comparator Output Polarity Select *1, *4	0: Comparator output not inverted 1: Comparator output inverted	R/W
b1	COE	Comparator Output Enable	0: Comparator output disabled (the output signal is fixed to 0) 1: Comparator output enabled	R/W
b2	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4, b3	CEG[1:0]	Comparator Edge Select	b4 b3 0 0: Interrupt request is not generated. 0 1: Rising edge 1 0: Falling edge 1 1: Both edges	R/W
b6, b5	CDFS[1:0]	Noise Filter Sampling Select*1, *2, *4	b6 b5 0 0: Noise filter not used 0 1: Sampling frequency is PCLK/8. 1 0: Sampling frequency is PCLK/16. 1 1: Sampling frequency is PCLK/32.	R/W
b7	HCMPON	Comparator Operation Enable*3	0: Operation stopped (the output signal is fixed to 0) 1: Operation enabled (input to the comparator pins is enabled)	R/W

Note: If comparator detection is used as a POE source, note that write access to this register after the setting of any register in the POE may generate a POE source.

Note: If comparator detection is used as a GPT source, note that write access to this register after the setting of any register in the GPT may generate a GPT source.

Note 1. Rewrite the CDFS[1:0] and CINV bits only after disabling the comparator output (COE bit = 0).

Note 2. If the CDFS[1:0] bits are changed from 00b (noise filter not used) to a value other than 00b (noise filter used), allow four sampling times to elapse until the filter output is updated, and then use the comparator interrupt request.

Note 3. The operation stabilization wait time is required after enabling comparator operation (HCMPON bit = 1).

Note 4. Rewriting the CINV bit or CDFS[1:0] bits may generate a comparator interrupt request, POE source and GPT internal trigger source. Before changing these bits, set the registers in the POE so that comparator output is not used for high-impedance control and set the registers in the GPT so that comparator detection is not used as an internal trigger source. After changing these bits, also set the corresponding interrupt status flag (IR) in the interrupt request register and the POE comparator channel n detection flag (n = 0 to 3) to 0.

CEG[1:0] Bits (Comparator Edge Select)

These bits select which edge of comparator output signal is used to generate an interrupt request.

The valid edge is set for the signal after the comparator polarity is selected by the CINV bit and the filter is selected by CDFS[1:0] bits.

33.2.2 Comparator Input Select Register (CMPSEL0)

Address(es): CMPC0.CMPSEL0 000A 0C84h, CMPC1.CMPSEL0 000A 0CA4h, CMPC2.CMPSEL0 000A 0CC4h, CMPC3.CMPSEL0 000A 0CE4h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	CMPSEL[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	CMPSEL[3:0]	Comparator Input Select*1, *2, *3	• Comparator C0 b3 b0 0 0 0 0 : No input 0 0 0 1 : CMPC00 selected 0 0 1 0 : CMPC01 selected 0 1 0 0 : CMPC02 selected 1 0 0 0 : CMPC03 selected Settings other than above are prohibited. • Comparator C1 b3 b0 0 0 0 0 : No input 0 0 0 1 : CMPC10 selected 0 0 1 0 : CMPC11 selected 0 1 0 0 : CMPC12 selected 1 0 0 0 : CMPC13 selected Settings other than above are prohibited. • Comparator C2 b3 b0 0 0 0 0 : No input 0 0 0 1 : CMPC20 selected 0 0 1 0 : CMPC21 selected 0 1 0 0 : CMPC22 selected 1 0 0 0 : CMPC23 selected Settings other than above are prohibited. • Comparator C3 b3 b0 0 0 0 0 : No input 0 0 0 1 : CMPC30 selected 0 0 1 0 : CMPC31 selected 0 1 0 0 : CMPC32 selected 1 0 0 0 : CMPC33 selected Settings other than above are prohibited.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Rewrite the CMPSEL[3:0] bits in the following procedure. Writing a value other than 0000b while the value of these bits is not 0000b is invalid. Writing 1 to two or more bits is also invalid. In both cases, the previous value is retained.
(1) Set the CMPCTL.COE bit to 0.
(2) Set the CMPSEL[3:0] bits to 0000b.
(3) Set a new value to the CMPSEL[3:0] bits (with 1 set in only one of the bits).
(4) Wait for the stabilization time for input selection.
(5) Set the CMPCTL.COE bit to 1.
(6) Set the corresponding interrupt status flag (IR) in the interrupt request register to 0.

Note 2. If comparator detection is used as a GPT source, note that write access to this bit after the setting of any register in the GPT may generate a GPT source.

Note 3. If comparator detection is used as a POE source, note that write access to this bit after the setting of any register in the POE may generate a POE source.

33.2.3 Comparator Reference Voltage Select Register (CMPSEL1)

Address(es): CMPC0.CMPSEL1 000A 0C88h, CMPC1.CMPSEL1 000A 0CA8h, CMPC2.CMPSEL1 000A 0CC8h, CMPC3.CMPSEL1 000A 0CE8h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	CVRS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	CVRS[1:0]	Reference Input Voltage Select *1, *2, *3, *4	b1 b0 0 0: No input 0 1: On-chip D/A converter 1 output voltage selected as reference input voltage 1 0: On-chip D/A converter 0 output voltage selected as reference input voltage Settings other than above are prohibited.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. When the on-chip D/A converter output voltage is used, set the D/A converter for generating comparator C reference voltage before enabling comparator operation (CMPCTL.HCMPON bit = 1). For details on setting the D/A converter, refer to section 32, D/A Converter (DAa).

Note 2. Rewrite the CVRS[1:0] bits in the following procedure. Be sure to set the CVRS[1:0] bits to 00b before changing the set value. Rewriting the value directly from 01b to 10b or 10b to 01b is not possible.
(1) Set the CMPCTL.COE bit to 0.
(2) Set the CVRS[1:0] bits to 00b.
(3) Set a new value to the CVRS[1:0] bits (with 1 set in only one of the bits).
(4) Wait for the stabilization time for input selection.
(5) Set the CMPCTL.COE bit to 1.
(6) Set the corresponding interrupt status flag (IR) in the interrupt request register to 0.

Note 3. If comparator detection is used as a GPT source, note that write access to this bit after the setting of any register in the GPT may generate a GPT source.

Note 4. If comparator detection is used as a POE source, note that write access to this bit after the setting of any register in the POE may generate a POE source.

33.2.4 Comparator Output Monitor Register (CMPMON)

Address(es): CMPC0.CMPMON 000A 0C8Ch, CMPC1.CMPMON 000A 0CACh, CMPC2.CMPMON 000A 0CCCh, CMPC3.CMPMON 000A 0CECh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CMPMON0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CMPMON0	Comparator Output Monitor Flag *1	0: Comparator output is 0. 1: Comparator output is 1.	R
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. When comparator operation is enabled (CMPCTL.HCMPON and COE bits are 1) while the noise filter is disabled (CMPCTL.CDFS[1:0] bits are 00b), read the CMPMON0 bit twice and use the value only when the results match.

33.2.5 Comparator External Output Enable Register (CMPIOC)

Address(es): CMPC0.CMPIOC 000A 0C90h, CMPC1.CMPIOC 000A 0CB0h, CMPC2.CMPIOC 000A 0CD0h, CMPC3.CMPIOC 000A 0CF0h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CPOE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CPOE	External Pin Output Enable	0: Output to the comparator external pin is disabled (the output signal is fixed to low) 1: Output to the comparator external pin is enabled	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

33.3 Operation

33.3.1 Comparator Operation Example

Figure 33.2 shows an operation example of the comparator. The COMPn (n = 0 to 3) output becomes high when the analog input voltage is higher than the reference input voltage, and the COMPn output becomes low when the analog input voltage is lower than the reference input voltage (when the CMPCTL.CINV bit is 0). When the comparator output changes, an interrupt request is output.

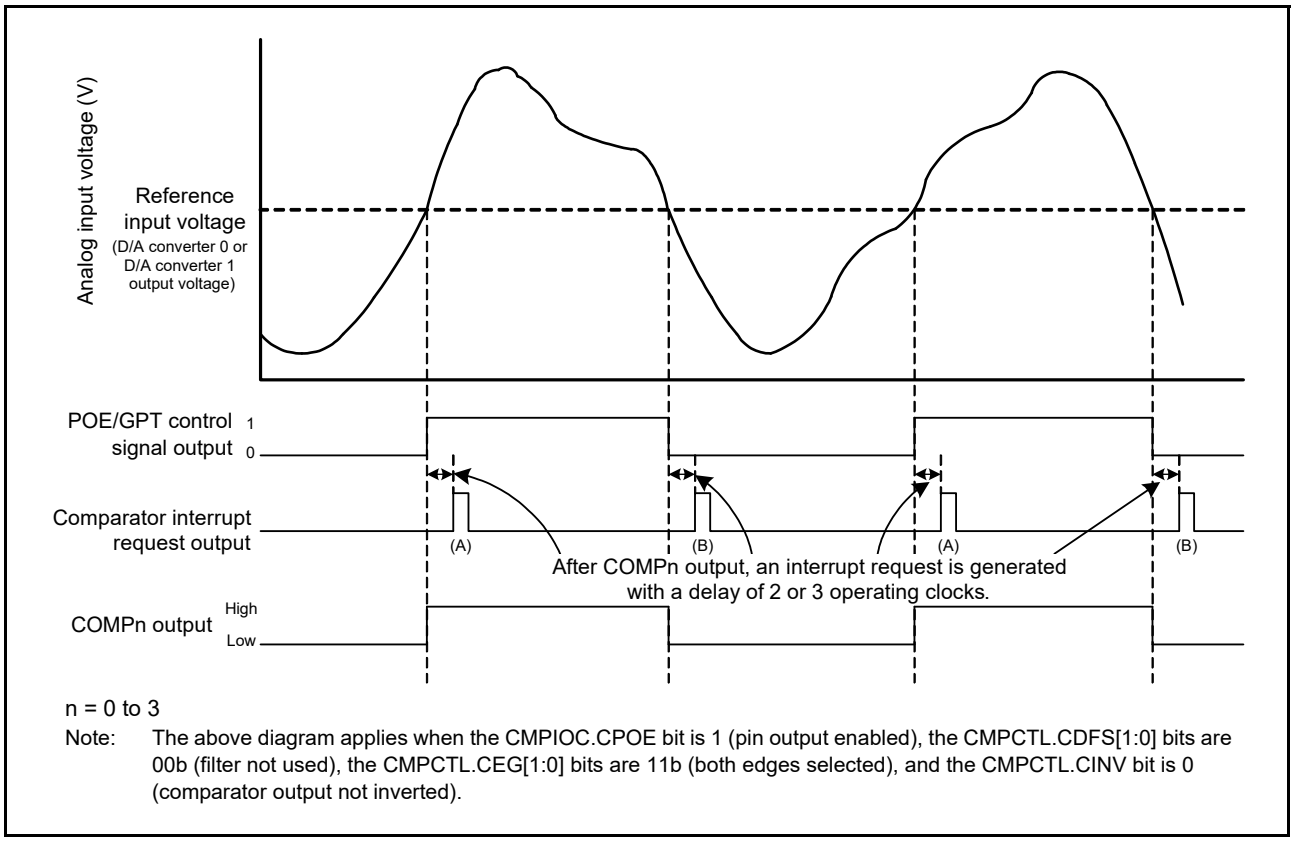


Figure 33.2 Comparator Operation Example

33.3.2 Noise Filter

Comparator C contains a noise filter. The sampling clock can be selected by the CMPCTL.CDFS[1:0] bits.
The comparator output signal is sampled every sampling clock, and if the same value is sampled three times, that value is determined as the noise filter output at the next sampling clock.
Figure 33.3 shows the configuration of the noise filter and edge detector and Figure 33.4 shows an example of the comparator noise filter and interrupt operation.

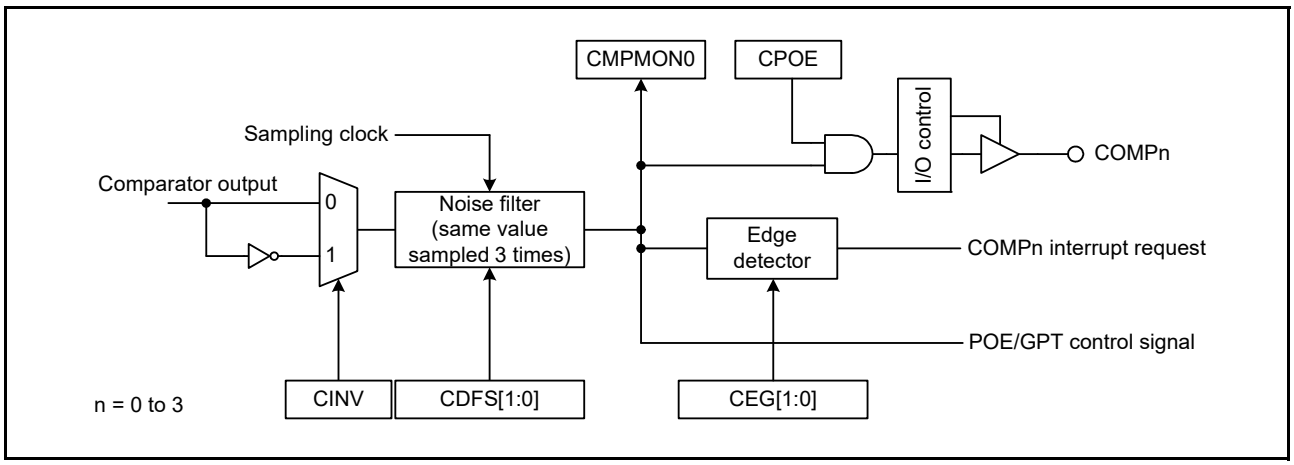
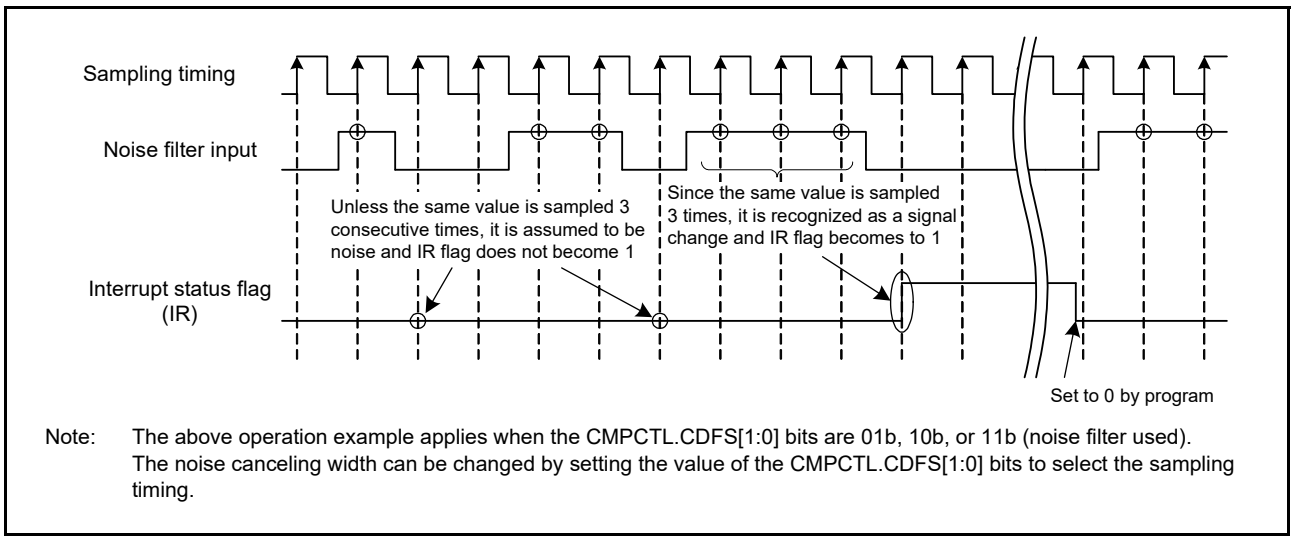


Figure 33.3 Noise Filter and Edge Detector Configuration



Note: The above operation example applies when the CMPCTL.CDFS[1:0] bits are 01b, 10b, or 11b (noise filter used).
The noise canceling width can be changed by setting the value of the CMPCTL.CDFS[1:0] bits to select the sampling timing.

Figure 33.4 Comparator Noise Filter and Interrupt Operation Example

33.3.3 Comparator Interrupts

Comparator C generates an interrupt request upon detecting any changes in the comparison result.
When using the comparator interrupt, set at least one of bits CMPCTL.CEG[1:0] to 1 (to a value other than 00b (interrupt request is not generated)).
To use the comparator interrupt, use the following setting procedure. Note that steps (1), (2), and (3) can be set in any order.

(1) When using the on-chip D/A converter output voltage as the reference input voltage, set the D/A converter for generating comparator C reference voltage and enable operation.
(2) Set the CMPSEL0 or CMPSEL1 register to set the input of the comparator.
(3) Set the CMPCTL.CINV and CDFS[1:0] bits to select inversion or non-inversion processing and the sampling timing of the noise filter.
(4) Enable the edge detection for the comparator output (set the CMPCTL.CEG[1:0] bits to a value other than 00b).
(5) Enable input of the comparator (set the CMPCTL.HCMPON bit to 1) and wait for the time until the comparator operation is stabilized.
(6) Enable output of the comparator (set the CMPCTL.COE bit to 1).

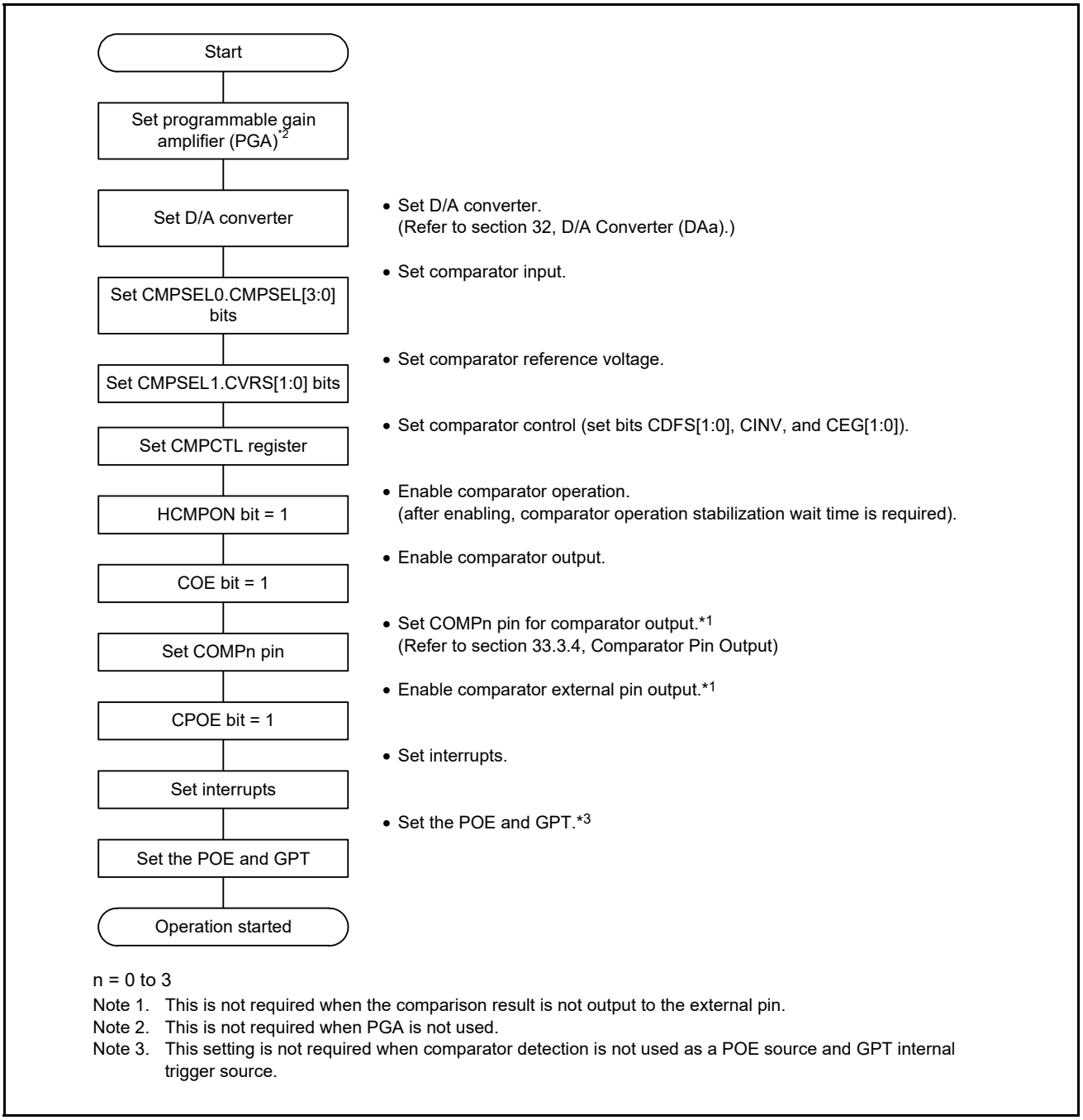
33.3.4 Comparator Pin Output

The comparison results can be output to the COMPn pins (n = 0 to 3). The CMPCTL.CINV bit can be used to set the output polarity (non-inverted output or inverted output), and the CMPIOC.CPOE bit can be used to enable or disable the output.
To output the comparison result to the external pin COMPn, use the following setting procedure. Note that the ports are set to input after reset.

(1) Execute steps (1) to (3) and steps (5) and (6) shown in section 33.3.3, Comparator Interrupts.
(2) Enable output of the comparison result to the external pin (set the CMPIOC.CPOE bit to 1).
(3) Set the port register and the pin function control register corresponding to each comparator output pin.

33.3.5 Comparator Setting Flowchart

Figure 33.5 shows the flowchart for setting the comparator-related registers.



n = 0 to 3

Note 1. This is not required when the comparison result is not output to the external pin.
Note 2. This is not required when PGA is not used.
Note 3. This setting is not required when comparator detection is not used as a POE source and GPT internal trigger source.

Figure 33.5 Comparator Operation Setting Flowchart

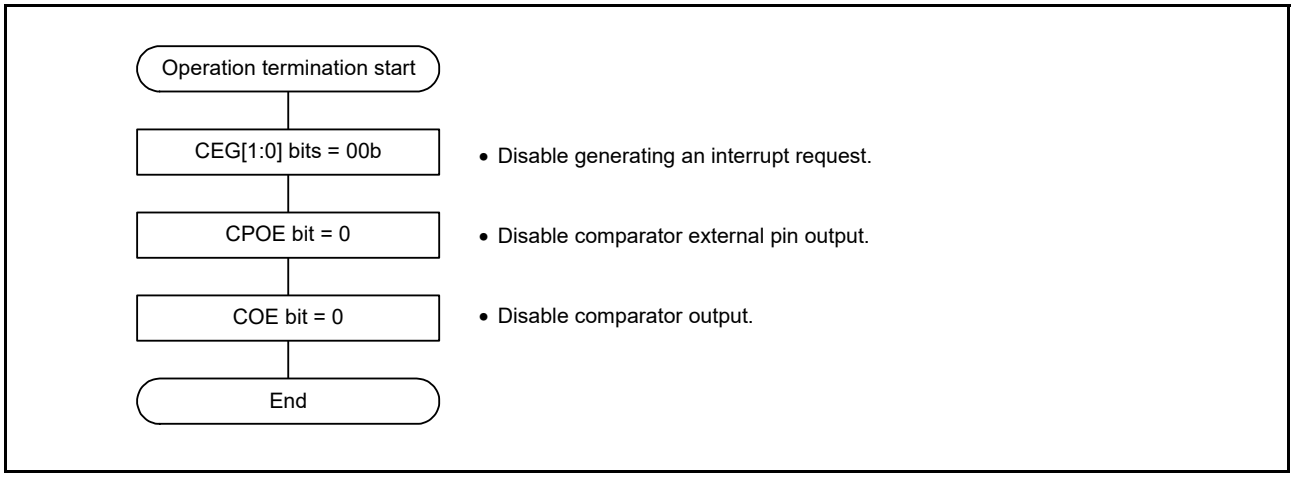


Figure 33.6 Comparator Operation Termination Flowchart

33.4 Usage Notes

33.4.1 Module Stop Function Setting

Operation of comparator C can be disabled or enabled using module stop control register B (MSTPCRB). After the reset, comparator C is halted. Register access is enabled by releasing the module stop state. For details, refer to section 11, Low Power Consumption.

33.4.2 Comparator C Operation in Module Stop State

When the module stop state is entered while comparator C is operating, analog circuits in the comparator C is not stopped and the analog power supply current is the same as that when comparator C is being used. If the analog power supply current needs to be reduced in the module stop state, set the CMPCTL.HCMPON bit to 0 to stop comparator C.

33.4.3 Comparator C Operation in Software Standby Mode

When software standby mode is entered while comparator C is operating, analog circuits in the comparator C is not stopped and the analog power supply current is the same as that when comparator C is being used. If the analog power supply current needs to be reduced in software standby mode, set the CMPCTL.HCMPON bit to 0 to stop comparator C.

33.4.4 Comparator Operation while the 12-Bit A/D Convertor is in the Module-Stop State

The same module stop signal controls the programmable gain amplifiers (PGAs) and the 12-bit A/D convertor. The comparison of PGA output for the following pins is not possible while the 12-bit A/D convertor is in the module stop state.

- PGA output for AN000 pin
- PGA output for AN100 pin
- PGA output for AN101 pin
- PGA output for AN102 pin

The comparison for the following analog input pins is possible since they are directly connected to the comparator, even if the 12-bit A/D convertor is in the module-stop state.

- AN000 pin
- AN100 pin
- AN101 pin
- AN102 pin

33.4.5 Setting the D/A Converter

Set the D/A converter and wait for the D/A converter output settling time before enabling the comparator. Similarly, before making any changes to the settings of the D/A converter stop the comparator temporarily, and after the changes are made, wait for the D/A converter output settling time before enabling the comparator.

34. Data Operation Circuit (DOC)

34.1 Overview

The data operation circuit (DOC) is used to compare, add, and subtract 16-bit data.
Table 34.1 lists the data operation circuit specifications and Figure 34.1 shows a block diagram of the data operation circuit.
16-bit data is compared and an interrupt can be generated when a selected condition applies.

Table 34.1 DOC Specifications

Item	Description
Data operation function	16-bit data comparison, addition, and subtraction
Lower power consumption function	Module stop state can be set.
Interrupts	An interrupt occurs at the following timings: • The compared values either match or mismatch • The result of data addition is greater than FFFFh • The result of data subtraction is less than 0000h

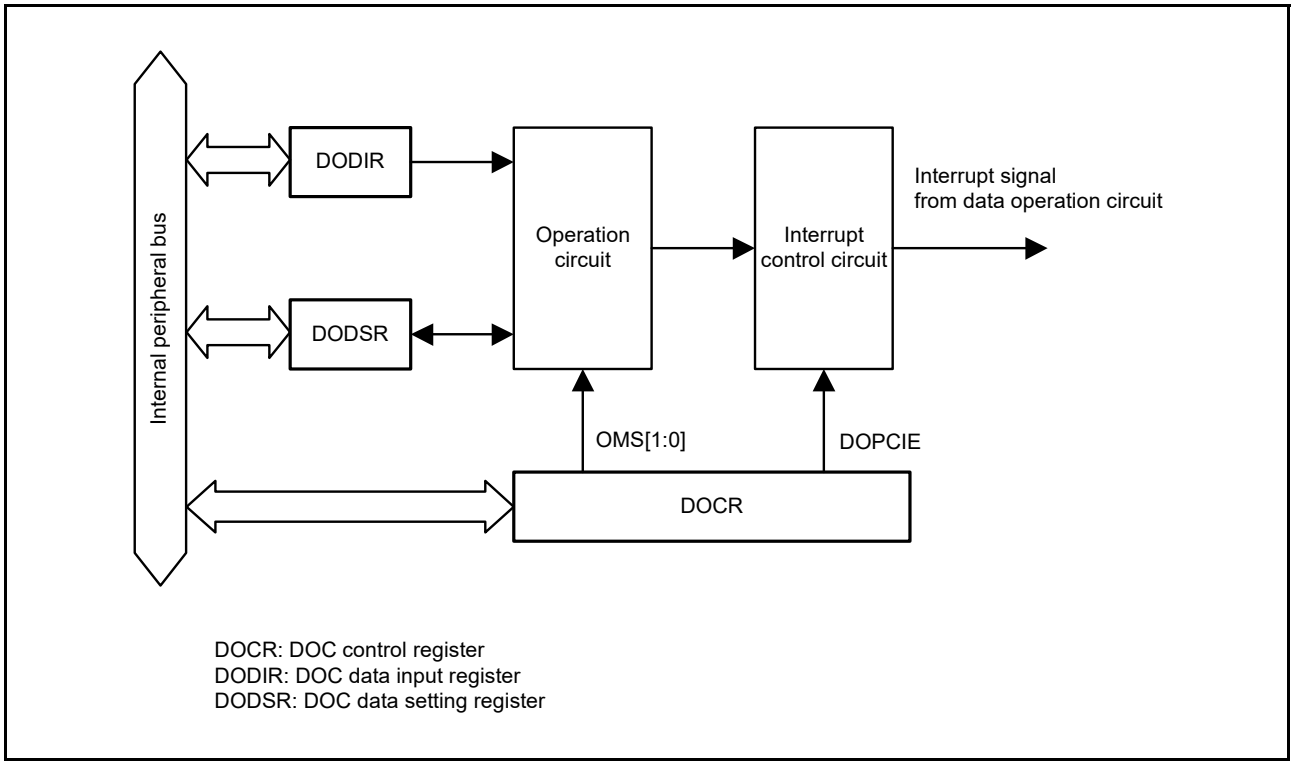


Figure 34.1 DOC Block Diagram

34.2 Register Descriptions

34.2.1 DOC Control Register (DOCR)

Address(es): 0008 B080h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	DOPCFCL	DOPCF	DOPCIE	—	DCSEL	OMS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	OMS[1:0]	Operating Mode Select	b1 b0 0 0: Data comparison mode 0 1: Data addition mode 1 0: Data subtraction mode 1 1: Setting prohibited	R/W
b2	DCSEL*1	Detection Condition Select	Result of data comparison 0: Data mismatch is detected. 1: Data match is detected.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	DOPCIE	Data Operation Circuit Interrupt Enable	0: Disables interrupts from the data operation circuit. 1: Enables interrupts from the data operation circuit.	R/W
b5	DOPCF	Data Operation Circuit Flag	Indicates the result of an operation.	R
b6	DOPCFCL	DOPCF Clear	0: Maintains the DOPCF flag state. 1: Clears the DOPCF flag.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note 1. Valid only when data comparison mode is selected.

OMS[1:0] Bits (Operating Mode Select)

These bits select the operating mode of the data operation circuit.

DCSEL Bit (Detection Condition Select)

This bit is valid only when data comparison mode is selected.

This bit selects the condition for detection in data comparison mode.

DOPCIE Bit (Data Operation Circuit Interrupt Enable)

Setting this bit to 1 enables interrupts from the data operation circuit.

DOPCF Flag (Data Operation Circuit Flag)

[Setting conditions]

- The condition selected by the DCSEL bit is met
- A result of data addition is greater than FFFFh
- A result of data subtraction is less than 0000h

[Clearing condition]

- Writing 1 to the DOPCFCL bit

DOPCFCL Bit (DOPCF Clear)

Setting this bit to 1 clears the DOPCF flag.

This bit is read as 0.

34.2.2 DOC Data Input Register (DODIR)

Address(es): 0008 B082h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DODIR is a 16-bit readable/writable register in which 16-bit data for use in the operations are stored.

34.2.3 DOC Data Setting Register (DODSR)

Address(es): 0008 B084h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DODSR is a 16-bit readable/writable register. This register stores 16-bit data for use as a reference in data comparison mode. This register also stores the results of operations in data addition and data subtraction modes.

34.3 Operation

34.3.1 Data Comparison Mode

Figure 34.2 shows an example of the steps involved in data comparison mode operation by the data operation circuit. The following is an example of operation when DCSEL is set to 0 (data mismatch is detected as a result of data comparison).

(1) Writing 00b to the DOCR.OMS[1:0] bits selects data comparison mode.
(2) The 16-bit reference data is set in DODSR.
(3) 16-bit data for comparison is written to DODIR.
(4) Writing of 16-bit data continues until all data for comparison have been written to DODIR.
(5) If a value written to DODIR does not match that in DODSR*1, the DOCR.DOPCF flag is set to 1. When the DOCR.DOPCIE bit is 1, a data operation circuit interrupt is also generated.

Note 1. When DOCR.DCSEL = 0

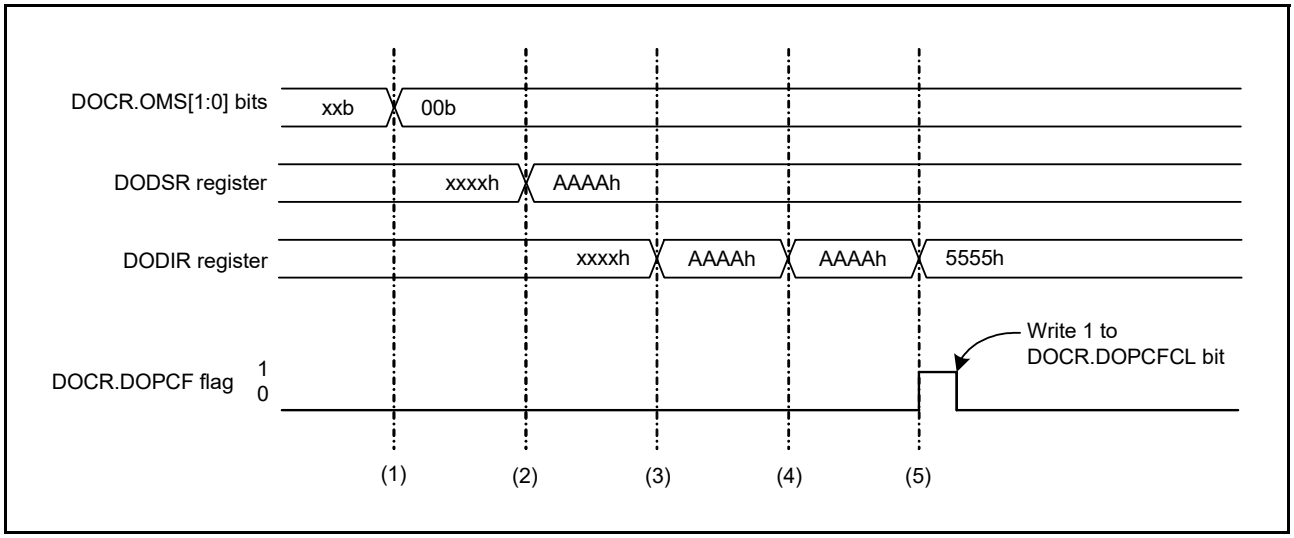


Figure 34.2 Example of Operation in Data Comparison Mode

34.3.2 Data Addition Mode

Figure 34.3 shows an example of the steps involved in data addition mode operation by the data operation circuit.

(1) Writing 01b to the DOCR.OMS[1:0] bits selects data addition mode.
(2) 16-bit data is set in the DODSR register as the initial value.
(3) 16-bit data to be added is written to DODIR. The result of the operation is stored in DODSR.
(4) Writing of 16-bit data continues until all data for addition have been written to DODIR.
(5) If the result of an operation is greater than FFFFh, the DOCR.DOPCF flag is set to 1. When the DOCR.DOPCIE bit is 1, a data operation circuit interrupt is also generated.

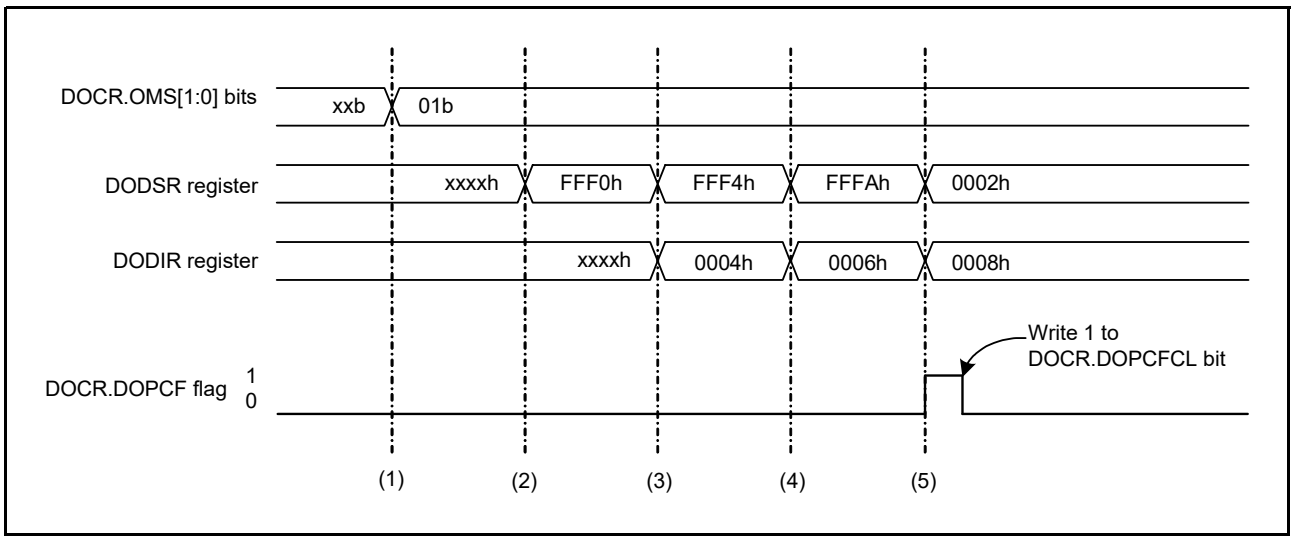


Figure 34.3 Example of Operation in Data Addition Mode

34.3.3 Data Subtraction Mode

Figure 34.4 shows an example of the steps involved in data subtraction mode operation by the data operation circuit.

(1) Writing 10b to the DOCR.OMS[1:0] bits selects data subtraction mode.
(2) 16-bit data is set in the DODSR register as the initial value.
(3) 16-bit data to be subtracted is written to DODIR. The result of the operation is stored in DODSR.
(4) Writing of 16-bit data continues until all data for subtraction have been written to DODIR.
(5) If the result of an operation is less than 0000h, the DOCR.DOPCF flag is set to 1. When the DOCR.DOPCIE bit is 1, a data operation circuit interrupt is also generated.

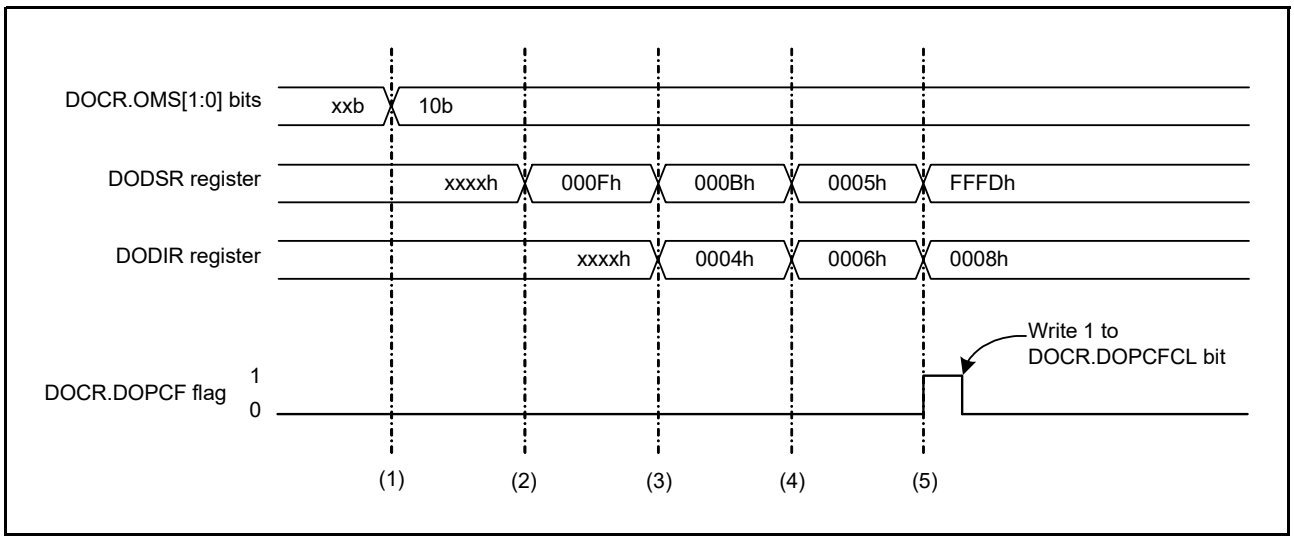


Figure 34.4 Example of Operation in Data Subtraction Mode

34.4 Interrupt Requests

The data operation circuit generates the data operation circuit interrupt as an interrupt request. When an interrupt source is generated, the data operation circuit flag corresponding to the interrupt is set to 1. Table 34.2 describes the interrupt request.

Table 34.2 Interrupt Request from Data Operation Circuit

Interrupt Request	Data Operation Circuit Flag	Interrupt Generation Timing
Data operation circuit interrupt	DOPCF	• The compared values either match or mismatch • The result of data addition is greater than FFFFh • The result of data subtraction is less than 0000h

34.5 Usage Note

34.5.1 Module Stop Function Setting

Operation of the data operation circuit can be disabled or enabled using module stop control register B (MSTPCRB). The initial setting is for the data operation circuit to be stopped. Register access is enabled by releasing the module stop state. For details, refer to section 11, Low Power Consumption.

35. RAM

This MCU has an on-chip high-speed static RAM.

35.1 Overview

Table 35.1 lists the specifications of the RAM.

Table 35.1 Specifications of RAM

Item	Description
RAM capacity	32 Kbytes (RAM0: 32 Kbytes)
RAM address	RAM0: 0000 0000h to 0000 7FFFh
Access	• Single-cycle access is possible for both reading and writing. • On-chip RAM can be enabled or disabled.*1
Low power consumption function	The module stop state is selectable for RAM0.

Note 1. Selectable by the RAME bit in SYSCR1. For details on SYSCR1, see section 3.2.2, System Control Register 1 (SYSCR1).

35.2 Operation

35.2.1 Low Power Consumption Function

Power consumption can be reduced by setting module stop control register C (MSTPCRC) to stop supply of the clock signal to the RAM.
Setting the MSTPCRC.MSTPC0 bit to 1 stops supply of the clock signal to RAM0.
Stopping supply of the clock signal places the RAM0 in the module stop state. The RAM operates after initialization by a reset.
The RAM is not accessible in the module stop state. Do not allow transitions to the module stop state while access to RAM is in progress.
For details on the MSTPCRC register, see section 11, Low Power Consumption.

36. Flash Memory

This MCU has packages with 256, 384, and 512 Kbyte flash memory (ROM) for storing code and 8-Kbyte flash memory (E2 DataFlash) for storing data.
In this section, “PCLK” is used to refer to PCLKB.

36.1 Overview

Table 36.1 lists the Flash Memory Specifications.
Table 36.7 lists the I/O Pins Used in Boot Mode.

Table 36.1 Flash Memory Specifications

Item	Description
Memory space	• User area: Up to 512 Kbytes • Data area: 8 Kbytes • Extra area: Stores the start-up area information, access window information, and unique ID
ROM cache	• Cache size: 2 Kbytes
Software commands	• The following commands are implemented: Program, blank check, block erase, all-block erase • The following commands are implemented for programming the extra area: Start-up area information program, access window information program
Value after erase	• ROM: FFh • E2 DataFlash: FFh
Interrupt	An interrupt (FRDYI) is generated upon completion of software command processing or forced stop processing.
On-board programming	Boot mode (SCI)*1 • Channel 1 of the serial communications interface (SCI1) is used for asynchronous serial communication. • The user area and data area are rewritable. Boot mode (FINE interface)*1 • The FINE is used. • The user area and data area are rewritable. Self-programming in single-chip mode • The user area and data area are rewritable using the flash rewrite routine in the user program.
Off-board programming	The user area and data area are rewritable using a flash programmer (serial programmer or parallel programmer) compatible with this MCU.
ID code protection	• Connection with the serial programmer can be enabled or disabled using ID codes in boot mode. • Connection with the on-chip debugging emulator can be enabled or disabled using ID codes. • Connection with the parallel programmer can be enabled or disabled using ROM codes.
Start-up program protection	This function is used to safely rewrite block 0 to block 7.
Area protection	This function enables rewriting only the selected blocks in the user area and disables the other blocks during self-programming.
Background Operation (BGO)	Programs on the ROM can be executed while rewriting the E2 DataFlash.

Note 1. Refer to “PG-FP5 Flash Memory Programmer User’s Manual” and “Renesas Flash Programmer Flash memory programming software User’s Manual” for more details.

36.2 ROM Area and Block Configuration

The maximum ROM size of this MCU is 512 Kbytes. The ROM area is divided into blocks. A block is 2-Kbyte area. When executing the block erase command, the memory is erased by the block. Figure 36.1 shows the ROM Area and Block Configuration.

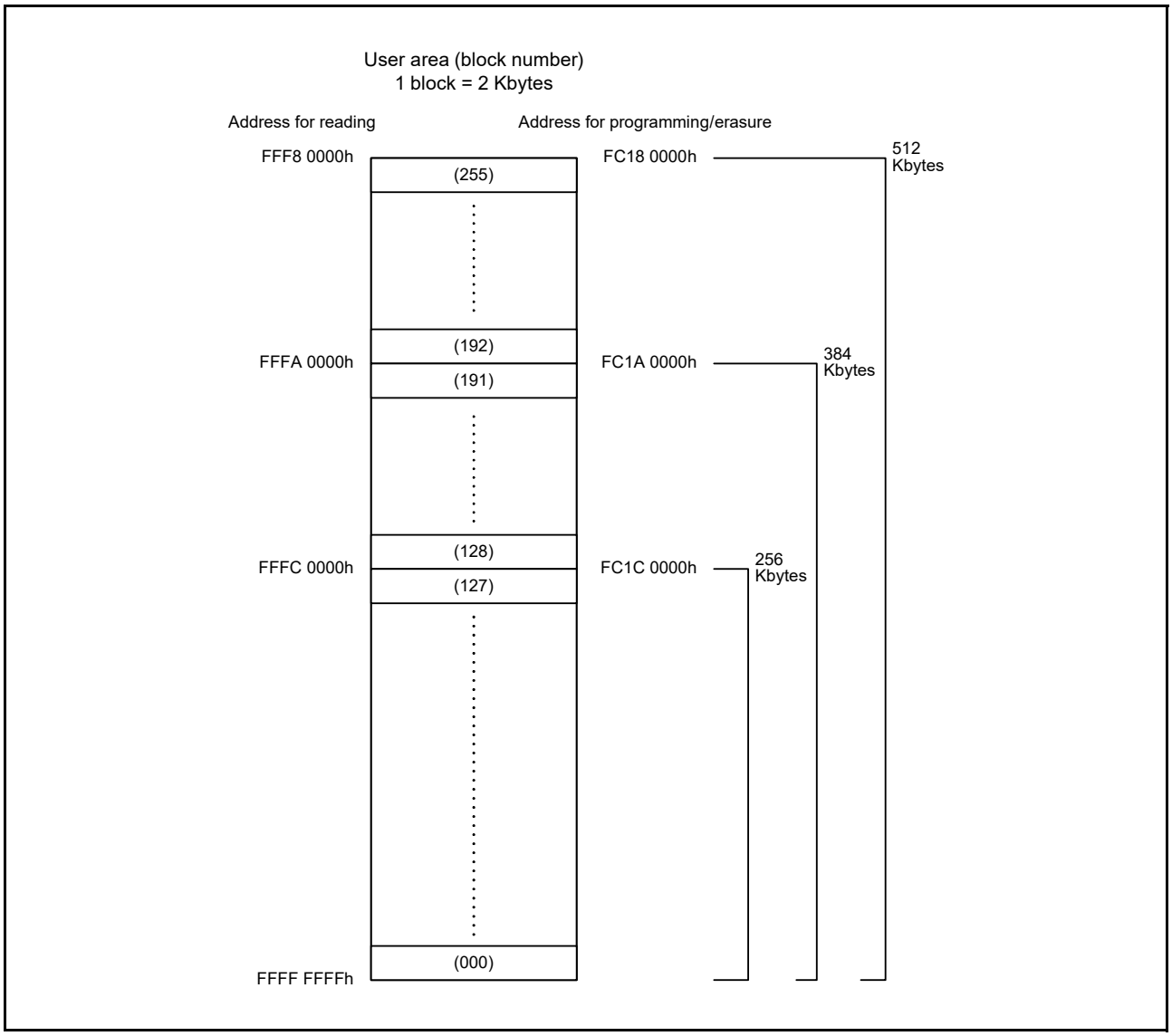


Figure 36.1 ROM Area and Block Configuration

Table 36.2 Correspondence Between ROM Capacity and Addresses for Reading

ROM Capacity	Addresses for Reading
512 Kbytes	FFF8 0000h to FFFF FFFFh
384 Kbytes	FFFA 0000h to FFFF FFFFh
256 Kbytes	FFFC 0000h to FFFF FFFFh

36.3 E2 DataFlash Area and Block Configuration

The E2 DataFlash is 8 Kbytes in the MCU. The E2 DataFlash is divided into blocks and erased in block units. Figure 36.2 shows the E2 DataFlash Area and Block Configuration.

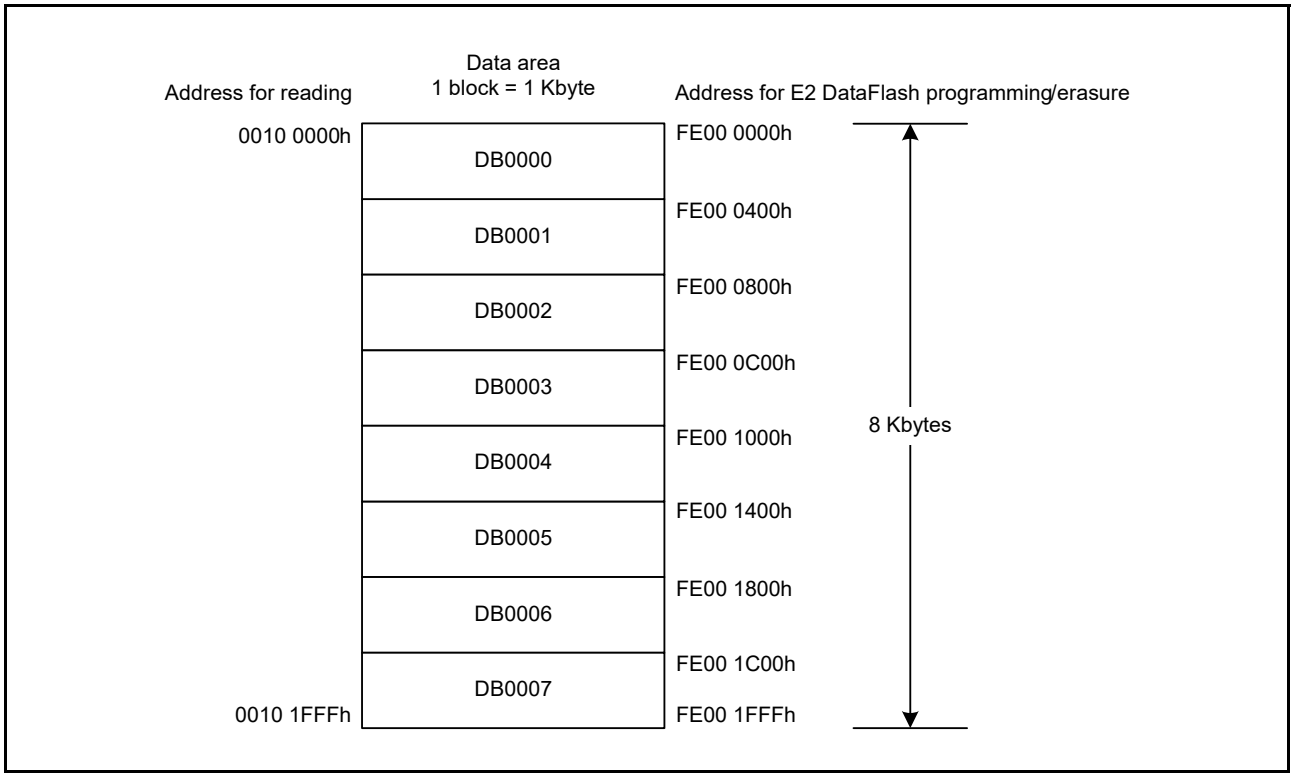


Figure 36.2 E2 DataFlash Area and Block Configuration

36.4 Register Descriptions

36.4.1 E2 DataFlash Control Register (DFLCTL)

Address(es): 007F C090h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DFLEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DFLEN	E2 DataFlash Access Enable	0: Access to E2 DataFlash and access to the extra area in P/E mode*1 disabled 1: Access to E2 DataFlash and access to the extra area in P/E mode*1 enabled	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Start-up area information programming and access window information program

The DFLCTL register is used to enable or disable access (read, program, and erase) to the E2 DataFlash and access (start-up area information programming, and access window information program) to the extra area in P/E mode. When reading, programming, and erasing the E2 DataFlash, set the DFLCTL.DFLEN bit to 1 and wait for the E2 DataFlash STOP recovery time (tDSTOP) to elapse before reading the E2 DataFlash and entering E2 DataFlash P/E mode. Do not read the E2 DataFlash or enter E2 DataFlash P/E mode until tDSTOP has elapsed.
Refer to section 36.7.1, Sequencer Modes for details on E2 DataFlash P/E mode. Refer to section 37, Electrical Characteristics for E2 DataFlash STOP recovery time (tDSTOP).

36.4.2 Flash P/E Mode Entry Register (FENTRYR)

Address(es): 007F FFB2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	FEKEY[7:0]								FENTRYD	—	—	—	—	—	—	FENTRY0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	FENTRY0	ROM P/E Mode Entry 0	0: ROM is in read mode. 1: ROM can be placed in P/E mode.	R/W
b6 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	FENTRYD	E2 DataFlash P/E Mode Entry	0: E2 DataFlash is in read mode. 1: E2 DataFlash can be placed in P/E mode.	R/W
b15 to b8	FEKEY[7:0]	Key Code	The FEKEY[7:0] bits are used to control rewriting of the FENTRYR register. When rewriting the value of the low-order 8 bits, set the FEKEY[7:0] bits to AAh at the same time (write this register in 16 bits). The FEKEY[7:0] bits are read as 00h.	R/W

To rewrite the ROM or E2 DataFlash, the FENTRYD or FENTRY0 bit must be set to 1 to place the ROM or E2 DataFlash in P/E mode.
When returning to read mode, set the FENTRYR register and confirm that its value has been rewritten before reading the ROM or E2 DataFlash.
Refer to section 36.7.1, Sequencer Modes for details on P/E mode and read mode.

FENTRY0 Bit (ROM P/E Mode Entry 0)

This bit is used to place the ROM in P/E mode.
[Setting condition]

- AA01h is written to the FENTRYR register when the FENTRYR register is 0000h.

Note: When entering ROM P/E mode, the instruction fetch address must be transferred to an area other than the ROM so that instruction fetching is not executed to the ROM. Copy necessary instruction code to the internal RAM and jump to the RAM. Note that E2 DataFlash can be rewritten by a program in the ROM.

[Clearing condition]

- AA00h is written to the FENTRYR register.

FENTRYD Bit (E2 DataFlash P/E Mode Entry)

This bit is used to place the E2 DataFlash in P/E mode.
[Setting condition]

- AA80h is written to the FENTRYR register when the FENTRYR register is 0000h.

[Clearing condition]

- AA00h is written to the FENTRYR register.

36.4.3 Protection Unlock Register (FPR)

Address(es): 007F C180h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

This write-only register is used to protect the FPMCR register from being rewritten inadvertently when the CPU runs out of control. Writing to the FPMCR register is enabled only when the following procedure is used to access the register.

Procedure to unlock protection

(1) Write A5h to the FPR register.
(2) Write a set value to the FPMCR register.
(3) Write the inverted set value to the FPMCR register.
(4) Write a set value to the FPMCR register again.

When a procedure other than the above is used to write data, the FPSR.PERR flag is set to 1.

36.4.4 Protection Unlock Status Register (FPSR)

Address(es): 007F C184h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	PERR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	PERR	Protect Error Flag	0: No error 1: An error occurs.	R
b7 to b1	—	Reserved	These bits are read as 0.	R

PERR Flag (Protect Error Flag)

When the FPMCR register is not accessed as described in the procedure to unlock protection, data is not written to the register and this flag is set to 1.

[Setting condition]

- The FPMCR register is not accessed as described in the procedure to unlock protection.

[Clearing condition]

- The FPMCR register is accessed according to the procedure to unlock protection described in section 36.4.3, Protection Unlock Register (FPR).

36.4.5 Flash P/E Mode Control Register (FPMCR)

Address(es): 007F C100h

	b7	b6	b5	b4	b3	b2	b1	b0
	FMS2	LVPE	—	FMS1	RPDIS	—	FMS0	—
Value after reset:	0	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b1	FMS0	Flash Operating Mode Select 0	FMS2 FMS1 FMS0 0 0 0: ROM/E2 DataFlash read mode 0 1 0: E2 DataFlash P/E mode 0 1 1: Discharge mode 1 1 0 1: ROM P/E mode 1 1 1: Discharge mode 2 Settings other than above are prohibited.	R/W
b2	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b3	RPDIS	ROM P/E Disable	0: ROM programming/erasure enabled 1: ROM programming/erasure disabled	R/W
b4	FMS1	Flash Operating Mode Select 1	See the FMS0 bit.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	LVPE	Low-Voltage P/E Mode Enable	0: Low-voltage P/E mode disabled 1: Low-voltage P/E mode enabled	R/W
b7	FMS2	Flash Operating Mode Select 2	See the FMS0 bit.	R/W

The FPMCR register is used to set the operating mode of the flash memory.
This register is protected. Set its value using the procedure to unlock protection. For details, refer to section 36.4.3, Protection Unlock Register (FPR).
When entering discharge mode 2 or ROM P/E mode, or during either of these modes, an instruction must be executed on the RAM.

FMS0, FMS1, and FMS2 Bits (Flash Operating Mode Select 0 to Flash Operating Mode Select 2)

These bits are used to set the operating mode of the flash memory.
[Transition from read mode to ROM P/E mode]
Set the FMS2 bit = 0, the FMS1 bit = 1, the FMS0 bit = 1, and the RPDIS bit = 0.
Wait for ROM mode transition wait time 1 (tDIS, refer to section 37, Electrical Characteristics).
Set the FMS2 bit = 1, the FMS1 bit = 1, the FMS0 bit = 1, and the RPDIS bit = 0.
Set the FMS2 bit = 1, the FMS1 bit = 0, the FMS0 bit = 1, and the RPDIS bit = 0.
Wait for ROM mode transition wait time 2 (tMS, refer to section 37, Electrical Characteristics).
[Transition from ROM P/E mode to read mode]
Set the FMS2 bit = 1, the FMS1 bit = 1, the FMS0 bit = 1, and the RPDIS bit = 0.
Wait for ROM mode transition wait time 1 (tDIS, refer to section 37, Electrical Characteristics).
Set the FMS2 bit = 0, the FMS1 bit = 1, the FMS0 bit = 1, and the RPDIS bit = 0.
Set the FMS2 bit = 0, the FMS1 bit = 0, the FMS0 bit = 0, and the RPDIS bit = 1.
Wait for ROM mode transition wait time 2 (tMS, refer to section 37, Electrical Characteristics).
[Transition from read mode to E2 DataFlash P/E mode]
Set the FMS2 bit = 0, the FMS1 bit = 1, the FMS0 bit = 0, and the RPDIS bit = 0.
[Transition from E2 DataFlash P/E mode to read mode]
Set the FMS2 bit = 0, the FMS1 bit = 0, the FMS0 bit = 0, and the RPDIS bit = 1.

Wait for ROM mode transition wait time 2 (tMS, refer to section 37, Electrical Characteristics).

RPDIS Bit (ROM P/E Disable)

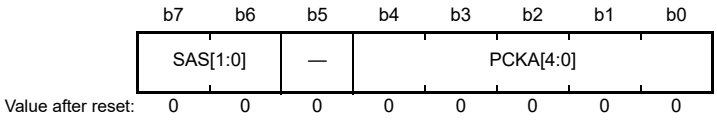
This bit is used to disable the execution of ROM programming/erasure with software.

LVPE Bit (Low-Voltage P/E Mode Enable)

Set this bit to 0 for programming/erasure in high-speed mode, and set this bit to 1 for programming/erasure in middle-speed mode.

36.4.6 Flash Initial Setting Register (FISR)

Address(es): 007F C1D8h



Bit	Symbol	Bit Name	Description	R/W
b4 to b0	PCKA[4:0]	Peripheral Clock Notification	These bits are used to set the frequency of the FlashIF clock (FCLK).	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7, b6	SAS[1:0]	Start-Up Area Select	b7 b6 0 x: The start-up area is selected according to the start-up area settings of the extra area. 1 0: The start-up area is switched to the default area temporarily. 1 1: The start-up area is switched to the alternate area temporarily.	R/W

x: Don't care

Data can be written to the FISR register in ROM P/E mode or E2 DataFlash P/E mode.

PCKA[4:0] Bits (Peripheral Clock Notification)

These bits are used to set the frequency of the FlashIF clock (FCLK) when programming/erasing the ROM/E2 DataFlash.

Set the FCLK frequency in the PCKA[4:0] bits before programming/erasure. Do not change the frequency during programming/erasure of the ROM/E2 DataFlash.

[When FCLK is higher than 4 MHz]

Set a rounded-up value for a non-integer frequency.

For example, set 32 MHz (PCKA[4:0] bits = 11111b) when the frequency is 31.5 MHz.

[When FCLK is 4 MH or lower]

Do not use a non-integer frequency.

Use the FCLK at a frequency of 1, 2, 3, or 4 MHz.

Note: When the PCKA[4:0] bits are set to a frequency different from the FCLK, the data in the ROM/E2 DataFlash may be damaged.

Table 36.3 Example of FlashIF Clock Frequency Settings

FlashIF Clock Frequency [MHz]	PCKA[4:0] Bit Setting	FlashIF Clock Frequency [MHz]	PCKA[4:0] Bit Setting	FlashIF Clock Frequency [MHz]	PCKA[4:0] Bit Setting
32	11111b	31	11110b	30	11101b
29	11100b	28	11011b	27	11010b
26	11001b	25	11000b	24	10111b
23	10110b	22	10101b	21	10100b
20	10011b	19	10010b	18	10001b
17	10000b	16	01111b	15	01110b
14	01101b	13	01100b	12	01011b
11	01010b	10	01001b	9	01000b
8	00111b	7	00110b	6	00101b
5	00100b	4	00011b	3	00010b
2	00001b	1	00000b	—	—

SAS[1:0] Bits (Start-Up Area Select)

These bits are used to select the start-up area. To change the start-up area, the following three methods can be used.

(1) When selecting the start-up area according to the start-up area settings of the extra area

With the SAS[1:0] bits set to 00b or 01b, the start-up area is selected according to the start-up area settings of the extra area. The settings are enabled after a reset is released.

(2) When switching the start-up area to the default area temporarily

When 10b is written to the SAS[1:0] bits, the start-up area is switched to the default area immediately after data is written to the register, regardless of the start-up area settings of the extra area.
When a reset is generated after this, the area is selected according to the start-up area settings of the extra area.

(3) When switching the start-up area to the alternative area temporarily

When 11b is written to the SAS[1:0] bits, the start-up area is switched to the alternative area, regardless of the start-up area settings of the extra area.
When a reset is generated after this, the area is selected according to the start-up area settings of the extra area.

36.4.7 Flash Reset Register (FRESETR)

Address(es): 007F C124h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	FRESET
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	FRESET	Flash Reset	0: Flash control circuit reset is released. 1: Flash control circuit is reset.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

FRESET Bit (Flash Reset)

When this bit is set to 1, registers FASR, FSARH, FSARL, FEARH, FEARL, FWB0, FWB1, FWB2, FWB3, FCR, and FEXCR are reset. Also, the values of registers FEAMH and FEAML are undefined. Do not access these registers during a reset. To release the reset, set this bit to 0.

Do not write to this register while executing a software command or rewriting the extra area.

36.4.8 Flash Area Select Register (FASR)

Address(es): 007F C104h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	EXS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	EXS	Extra Area Select	0: User area or data area 1: Extra area	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Data can be written to the FASR register in ROM P/E mode or E2 DataFlash P/E mode.

This register is initialized by a reset or setting the FRESETR.FRESET bit to 1.

Data cannot be written to this register while the FRESETR.FRESET bit is 1.

EXS Bit (Extra Area Select)

Set this bit to 1 before issuing a software command (start-up area information program or access window information program) for the extra area. Set this bit to 0 before issuing a software command (program, blank check, block erase, or all-block erase) for the user area.

After issuing a software command, do not change the value until changing it for issuing the next software command.

36.4.9 Flash Control Register (FCR)

Address(es): 007F C114h

	b7	b6	b5	b4	b3	b2	b1	b0
	OPST	STOP	—	—	CMD[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	CMD[3:0]	Software Command Setting	b3 b0 0 0 0 1: Program 0 0 1 1: Blank check 0 1 0 0: Block erase 0 1 1 0: All-block erase Settings other than above are prohibited.*1	R/W
b5, b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	STOP	Forced Processing Stop	When this bit is set to 1, the processing being executed can be forcibly stopped.	R/W
b7	OPST	Processing Start	0: Processing stops. 1: Processing starts.	R/W

Note 1. This does not include set the FCR register to 00h when the FSTATR1.FRDY flag is 1.

Data can be written to the FCR register when in ROM P/E mode and the ROM can be programmed/erased or in E2 DataFlash P/E mode.
This register is initialized by a reset or setting the FRESETR.FRESET bit to 1. Data cannot be written to this register while the FRESETR.FRESET bit is 1.
Note that this register cannot be initialized by the FRESETR.FRESET bit while a software command is being executed.

CMD[3:0] Bits (Software Command Setting)

These bits are used to set a software command (program, blank check, block erase, or all-block erase).
The function of each command is described below.
[Program]

- Write the value set in registers FWB0, FWB1, FWB2, and FWB3 to the address set in registers FSARH and FSARL.

[Blank check]

- Check whether there is data in the area from the address set in registers FSARH and FSARL to the address set in registers FEARH and FEARL. Confirm that data is not programmed in the area. This command does not guarantee whether the area remains erased.

[Block erase]

- Erase consecutive areas specified in the flash memory by the blocks. Set the beginning address of the block in registers FSARH and FSARL and the end address in registers FEARH and FEARL.

[All-block erase]

- Erase all blocks in the ROM or E2 DataFlash.
  All-block erase requires less time to erase the memory compared to block erase. When erasing the whole of the ROM area, set the beginning address of the ROM area in registers FSARH and FSARL, and the end address in registers FEARH and FEARL. Table 36.4 lists the setting address for all-block erase.

Table 36.4 Setting Address for All-Block Erase

Target	Memory Size	FSARH/FSARL	FEARH/FEARL
ROM	512 Kbytes	FC180000h	FC1FFFFFh
	384 Kbytes	FC1A0000h	FC1FFFFFh
	256 Kbytes	FC1C0000h	FC1FFFFFh
E2 DataFlash	8 Kbytes	FE000000h	FE001FFFh

STOP Bit (Forced Processing Stop)

This bit is used to forcibly stop the processing (blank check, block erase, or all-block erase) being executed.
After setting this bit to 1, wait until the FSTATR1.FRDY flag is 1 (processing completed) before setting the OPST bit to 0.

OPST Bit (Processing Start)

This bit is used to execute the command set in the CMD[2:0] bits.
This bit is not set to 0 again even when the processing is completed. Confirm that the FSTATR1.FRDY flag is 1 (processing completed) before setting the OPST bit to 0 again. After that, confirm that the FRDY flag is 0 before executing the next processing.

36.4.10 Flash Extra Area Control Register (FEXCR)

Address(es): 007F C1DCh

	b7	b6	b5	b4	b3	b2	b1	b0
	OPST	—	—	—	—	CMD[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	CMD[2:0]	Software Command Setting	b2 b0 0 0 1: Start-up area information program 0 1 0: Access window information program Settings other than above are prohibited.*1	R/W
b6 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	OPST	Processing Start	0: Processing stops. 1: Processing starts.	R/W

Note 1. This does not include set the FEXCR register to 00h when the FSTATR1.EXRDY flag is 1.

Data can be written to the FEXCR register when in ROM P/E mode and the ROM can be programmed/erased.
This register is initialized by a reset or setting the FRESETR.FRESET bit to 1. Data cannot be written to this register while the FRESETR.FRESET bit is 1.
Note that this register cannot be initialized by the FRESETR.FRESET bit while a software command is being executed.

CMD[2:0] Bits (Software Command Setting)

These bits are used to set a software command (start-up area information program or access window information program).
The details of each command are described below.
[Start-up area information program]

This command is used to switch the start-up area used for start-up program protection.

- When setting the start-up area to the default area
  Set registers FWB0, FWB1, FWB2, and FWB3 to FFFFh, and execute this command.
- When setting the start-up area to the alternative area
  Set the FWB0 register to FEFFh, set the FWB1 register to FFFFh, set registers FWB2 and FWB3 to FFFFh, and execute this command.

When registers FWB0, FWB1, FWB2, and FWB3 are set to values other than the above, do not execute the start-up area information program.

[Access window information program]

This command is used to set the access window used for area protection.

Set the access window in block units.

Specify the access window start address, which is the beginning address of the access window in the FWB0 register, specify the access window end address, which is the next address of the last address of the access window in the FWB1 register, and issue this command. Set bit 21 to bit 10 of the address for programming/erasure in each register.

If the same value is set as the start address and end address, all areas can be accessed. Do not set the start address to a value larger than the value of the end address.

OPST Bit (Processing Start)

This bit is used to execute the command set in the CMD[2:0] bits.

This bit is not set to 0 again even when the processing is completed. Confirm that the FSTATR1.EXRDY flag is 1 (processing completed) before setting the OPST bit to 0 again. After that, confirm that the FSTATR1.EXRDY flag is 0 before executing the next processing.

Writing to the extra area is started by writing 1 to the OPST bit. Do not write to the CMD[2:0] bits while a software command is being executed.

36.4.11 Flash Processing Start Address Register H (FSARH)

Address(es): 007F C110h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
								—	—	—	—					
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The FSARH register is used to set the target processing address or the start address of the target processing range in the flash memory when a software command is executed.
Set bit 31 to bit 25 and bit 20 to bit 16 of the flash memory address for programming/erasure in this register.
Data can be written to this register in ROM P/E mode or E2 DataFlash P/E mode.
This register is initialized by a reset or setting the FRESETR.FRESET bit to 1. Data cannot be written to this register while the FRESETR.FRESET bit is 1.
If this register is read while executing a software command set by the FEXCR register, an undefined value is read.
Refer to Figure 36.1 and Figure 36.2 for details on the addresses of the flash memory.

36.4.12 Flash Processing Start Address Register L (FSARL)

Address(es): 007F C108h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The FSARL register is used to set the target processing address or the start address of the target processing range in the flash memory when a software command is executed.
Set bit 15 to bit 0 of the flash memory address for programming/erasure in this register.
To set the ROM area, set bit 2 to bit 0 to 000b.
Data can be written to this register in ROM P/E mode or E2 DataFlash P/E mode.
This register is initialized by a reset or setting the FRESETR.FRESET bit to 1. Data cannot be written to this register while the FRESETR.FRESET bit is 1.
This register is incremented by 8h if the code flash memory is specified and 1h if the data flash area is specified after a program command is executed. Therefore, it is not necessary to set the target address to be written to this register when executing a program command sequentially.
If this register is read while executing a software command set by the FEXCR register, an undefined value is read.
Refer to Figure 36.1 and Figure 36.2 for details on the addresses of the flash memory.

36.4.13 Flash Processing End Address Register H (FEARH)

Address(es): 007F C120h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
								—	—	—	—					
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The FEARH register is used to set the end address of the target processing range in the flash memory when a software command is executed.
Set bit 31 to bit 25 and bit 20 to bit 16 of the flash memory address for programming/erasure in this register.
Data can be written to this register in ROM P/E mode or E2 DataFlash P/E mode.
This register is initialized by a reset or setting the FRESETR.FRESET bit to 1. Data cannot be written to this register while the FRESETR.FRESET bit is 1.
If this register is read while executing a software command set by the FEXCR register, an undefined value is read.
Refer to Figure 36.1 and Figure 36.2 for details on the addresses of the flash memory.

36.4.14 Flash Processing End Address Register L (FEARL)

Address(es): 007F C118h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The FEARH register is used to set the end address of the target range for processing when a software command is executed.
Set bit 15 to bit 0 of the flash memory address for programming/erasure in this register.
When setting the ROM area, set bit 2 to bit 0 to 000b.
Data can be written to this register in ROM P/E mode or E2 DataFlash P/E mode.
This register is initialized by a reset or setting the FRESETR.FRESET bit to 1. Data cannot be written to this register while the FRESETR.FRESET bit is 1.
If this register is read while executing a software command set by the FEXCR register, an undefined value is read.
Refer to Figure 36.1 and Figure 36.2 for details on the addresses of the flash memory.

36.4.15 Flash Write Buffer n Register (FWBn) (n = 0 to 3)

Address(es): FWB0 007F C130h, FWB1 007F C138h, FWB2 007F C140h, FWB3 007F C144h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This register is used to set the data for programming the ROM, E2 DataFlash, or extra area. The data can be written in ROM P/E mode or E2 DataFlash P/E mode.
This register is initialized by a reset or setting the FRESETR.FRESET bit to 1. Data cannot be written to this register

while the FRESETR.FRESET bit is 1.
The read value of this register is undefined while executing a software command set by the FCR register or the FEXCR register.
When programming the extra area, set the 4-byte data for programming in registers FWB0 and FWB1.
When programming the E2 DataFlash, set the data for programming in the low-order 8 bits in the FWB0 register.
When programming the ROM, set the 8-byte data for programming in registers FWB0 to FWB3. Figure 36.3 shows the relationship between the addresses indicated by registers FSARH and FSARL and the data set in the FWBn register.

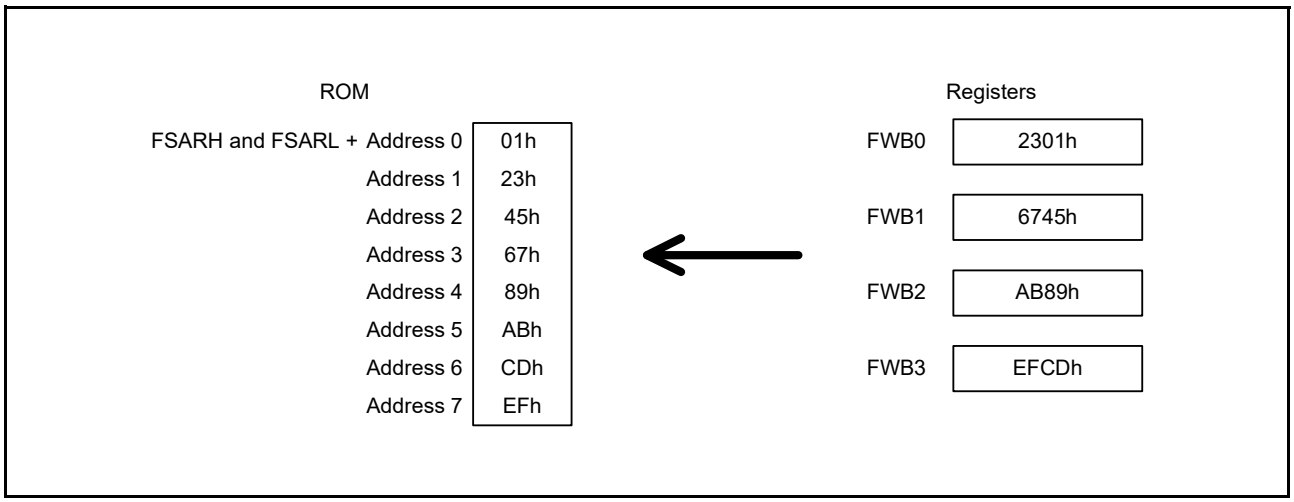


Figure 36.3 FWBn Register Setting Values and Data Allocation in the ROM

36.4.16 Flash Status Register 0 (FSTATR0)

Address(es): 007F C1F0h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	EILGLERR	ILGLERR	BCERR	—	PRGERR	ERERR
Value after reset:	x	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ERERR	Erase Error Flag	0: Erasure terminates normally. 1: An error occurs during erasure.	R
b1	PRGERR	Program Error Flag	0: Programming terminates normally. 1: An error occurs during programming.	R
b2	—	Reserved	The read value is undefined.	R
b3	BCERR	Blank Check Error Flag	0: Blank checking terminates normally. 1: An error occurs during blank checking.	R
b4	ILGLERR	Illegal Command Error Flag	0: No illegal software command or illegal access is detected. 1: An illegal command or illegal access is detected.	R
b5	EILGLERR	Extra Area Illegal Command Error Flag	0: No illegal command or illegal access to the extra area is detected. 1: An illegal command or illegal access to the extra area is detected.	R
b7, b6	—	Reserved	The read value is undefined.	R

This register is a status register used to confirm the result of executing a software command. Each error flag is set to 0 when the next software command is executed.

ERERR Flag (Erase Error Flag)

This flag indicates the result of the erase processing for the ROM/E2 DataFlash.
[Setting condition]

- An error occurs during erasure.

[Clearing condition]

- The next software command is executed.
  The value read from this flag is undefined when the FCR.STOP bit is set to 1 (processing is forcibly stopped) during erasure.

PRGERR Flag (Program Error Flag)

This flag indicates the result of the program processing for the ROM/E2 DataFlash.
[Setting condition]

- An error occurs during programming.

[Clearing condition]

- The next software command is executed.

BCERR Flag (Blank Check Error Flag)

This flag indicates the result of the blank check processing for the ROM/E2 DataFlash.
[Setting condition]

- An error occurs during blank checking.

[Clearing condition]

- The next software command is executed.
  The value read from this flag is undefined when the FCR.STOP bit is set to 1 (processing is forcibly stopped) during blank checking.

ILGLERR Flag (Illegal Command Error Flag)

This flag indicates the result of executing a software command.

[Setting conditions]

- Programming/erasure is executed to an area other than the access window range.
- A blank check or block erase command is executed when the set value of registers FSARH and FSARL is larger than the set value of registers FEARH and FEARL.
- Program and block erase commands are executed when the FASR.EXS bit is 1.
- An all-block erase command is executed while the access window is set.
- An all-block erase command is executed without setting registers FSARH and FSARL and registers FEARH and FEARL properly.
- The E2 DataFlash address is set in registers FSARH and FSARL and a software command is executed when the ROM is in P/E mode.
- The ROM address is set in registers FSARH and FSARL and a software command is executed when the E2 DataFlash is in P/E mode.
- The ROM and E2 DataFlash are set to P/E mode and a software command is executed.

[Clearing condition]

- The next software command is executed.

EILGLERR Flag (Extra Area Illegal Command Error Flag)

This flag indicates the result of executing a software command for the extra area.

[Setting condition]

- A software command for the extra area is executed when the FASR.EXS bit is 0.

[Clearing condition]

- The next software command is executed.

36.4.17 Flash Status Register 1 (FSTATR1)

Address(es): 007F C12Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	EXRDY	FRDY	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	1	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0.	R
b2	—	Reserved	This bit is read as 1.	R
b5 to b3	—	Reserved	These bits are read as 0.	R
b6	FRDY	Flash Ready Flag	0: Other than below 1: 00h can be written to the FCR register (processing to complete the software command).	R
b7	EXRDY	Extra Area Ready Flag	0: Other than below 1: 00h can be written to the FEXCR register (processing to complete the software command).	R

This register is a status register used to confirm the result of executing a software command. Each flag is set to 0 when the next software command is executed.

FRDY Flag (Flash Ready Flag)

This flag is used to confirm whether a software command is executed.
This flag becomes 1 when processing of the executed software command or the forced stop processing is completed, and this flag becomes 0 when setting the FCR.OPST bit to 0.
Also, an interrupt (FRDYI) is generated when this flag becomes 1.

EXRDY Flag (Extra Area Ready Flag)

This flag is used to confirm whether a software command for the extra area is executed.
This flag is set to 1 when processing of the executed software command is completed, and 0 when the FEXCR.OPST bit is set to 0.
Also, an interrupt (FRDYI) is generated when this flag becomes 1.

36.4.18 Flash Error Address Monitor Register H (FEAMH)

Address(es): 007F C1E8h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
								—	—	—	—					
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This register is used to check the address where the error has occurred if an error occurs during processing of a software command. This register stores bit 31 to bit 25 and bit 20 to bit 16 of the address where the error has occurred for the program command or blank check command, or it stores bit 31 to bit 25 and bit 20 to bit 16 of the beginning address of the area where the error has occurred for the block erase command or all-block erase command.
Since this register value becomes undefined if setting the FRESETR.FRESET bit to 1, read the value before error processing.
If the software command terminates normally, this register stores bit 31 to bit 25 and bit 20 to bit 16 of the end address at execution of the command.
Refer to Figure 36.1 and Figure 36.2 for details on the addresses of the flash memory.

36.4.19 Flash Error Address Monitor Register L (FEAML)

Address(es): 007F C1E0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This register is used to check the address where the error has occurred if an error occurs during processing of a software command. This register stores bit 15 to bit 0 of the address where the error has occurred for the program command or blank check command, or it stores bit 15 to bit 0 of the beginning address of the area where the error has occurred for the block erase command or all-block erase command.
Since this register value becomes undefined if setting the FRESETR.FRESET bit to 1, read the value before error processing.
When the software command is normally completed, this register stores bit 15 to bit 0 of the last address at execution of the command.
When executing a software command for the ROM, low-order 2 bits become 00b.
Refer to Figure 36.1 and Figure 36.2 for details on the addresses of the flash memory.

36.4.20 Flash Start-Up Setting Monitor Register (FSCMR)

Address(es): 007F C1C0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	SASMF	—	—	—	—	—	—	—	—
Value after reset:	0	1	1	1	0	1	1	Value set by user*1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	—	Reserved	These bits are read as 0.	R
b8	SASMF	Start-Up Area Setting Monitor Flag	0: Setting to start up using the alternative area 1: Setting to start up using the default area	R
b10, b9	—	Reserved	These bits are read as 1. Writing to these bits has no effect.	R
b11	—	Reserved	This bit is read as 0. Writing to this bit has no effect.	R
b14 to b12	—	Reserved	These bits are read as 1. Writing to these bits has no effect.	R
b15	—	Reserved	This bit is read as 0. Writing to this bit has no effect.	R

Note 1. The value of the blank product is 1. It is set to the same value set in bit 8 in the FWB1 register after the start-up area information program command is executed.

SASMF Flag (Start-Up Area Setting Monitor Flag)

This flag is used to confirm the settings of the start-up area.

When this flag is 0, the user program is set to start up using the alternative area.

When this flag is 1, the user program is set to start up using the default area.

36.4.21 Flash Access Window Start Address Monitor Register (FAWSMR)

Address(es): 007F C1C8h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—												
Value after reset:	0	0	0	0	The value set by the user*1											

Note 1. The value of the blank product is 1. It is set to the same value set in bit 11 to bit 0 the FWB0 register after the access window information program command is executed.

This register is used to confirm the set value of the access window start address used for area protection.

36.4.22 Flash Access Window End Address Monitor Register (FAWEMR)

Address(es): 007F C1D0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	The value set by the user*1											
Value after reset:	0	0	0	0												

Note 1. The value of the blank product is 1. It is set to the same value set in bit 11 to bit 0 in the FWB1 register after the access window information program command is executed.

This register is used to confirm the set value of the access window end address used for area protection.

36.4.23 Unique ID Register n (UIDRn) (n = 0 to 3)

Address(es): UIDR0 007F C350h, UIDR1 007F C354h, UIDR2 007F C358h, UIDR3 007F C35Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	Unique value for each chip															

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	Unique value for each chip															

The UIDRn register stores a 16-byte ID code (unique ID) for identifying the individual MCU.
The unique ID is stored in the extra area of the flash memory and cannot be rewritten by the user.

36.4.24 ROM Cache Enable Register (ROMCE)

Address(es): 0008 1000h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ROMCEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ROMCEN	ROM Cache Operation Enable	0: ROM cache operation disabled. 1: ROM cache operation enabled.	R/W
b15 to b1	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R

ROMCEN Bit (ROM Cache Operation Enable)

When setting the ROMCEN bit to 1, the ROM cache starts operation. While ROM cache is enabled, the data is served from the cache when a cache hit occurs.
When rewriting the ROM, set the ROMCEN bit to 0 in advance. After rewriting the ROM, write 1 to the ROMCIV.ROMCIV bit to invalidate the cache line.
When setting the ROMCEN bit to 1, perform the following settings.

(1) Write 1 to the ROMCIV.ROMCIV bit.
(2) Wait for the ROMCIV.ROMCIV bit to become 0.
(3) Set the ROMCE.ROMCEN bit to 1.
(4) Confirm that the ROMCE.ROMCEN bit is 1.

36.4.25 ROM Cache Invalidate Register (ROMCIV)

Address(es): 0008 1004h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ROMCIV
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ROMCIV	ROM Cache Invalidate	When reading 0: Invalidation is not started/Invalidation is completed. 1: Invalidation is in progress. When writing 0: Has no effects. 1: Start invalidation.	R/W
b15 to b1	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R

ROMCIV Bit (ROM Cache Invalidate)

When writing 1 to the ROMCIV bit, the ROM cache invalidation is performed.
Set the ROMCIV bit to 1 while the ROMCE.ROMCEN bit is 0.

36.5 Start-Up Program Protection

When rewriting the start-up program*1 by self-programming, if the rewrite operation is interrupted due to temporary blackout, the start-up program may not be successfully programmed and the user program may not start properly. This problem can be avoided by rewriting the start-up program without erasing the existing start-up program using the start-up program protection. This function is available in products with a 32-Kbyte or larger ROM.
Figure 36.4 shows the Overview of the Start-Up Program Protection. In this figure, the default area indicates block 0 to block 7, and the alternate area indicates block 8 to block 15.

Note 1. Program to perform operation to start the user program. It includes the fixed vector table.

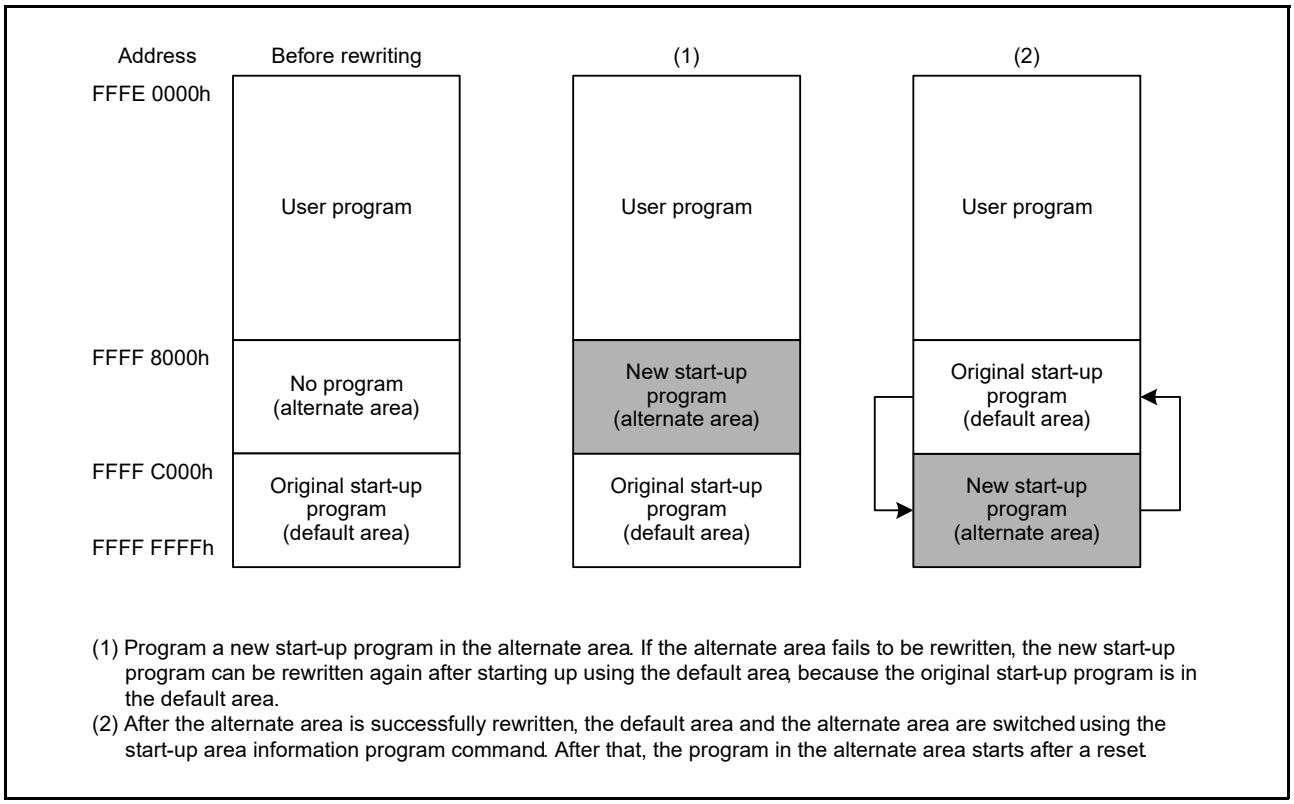


Figure 36.4 Overview of the Start-Up Program Protection

36.6 Area Protection

Area protection enables rewriting only the selected blocks (access window) in the user area and disables rewriting the other blocks during self-programming. The access window cannot be set in the data area.
Specify the start address and end address to set the access window. While the access window can be set in boot mode or by self-programming, area protection is enabled only during self-programming in single-chip mode.
Figure 36.5 shows the Area Protection Overview (When Blocks 4 to 6 are Set as the Access Window in Products with 128-Kbyte ROM).

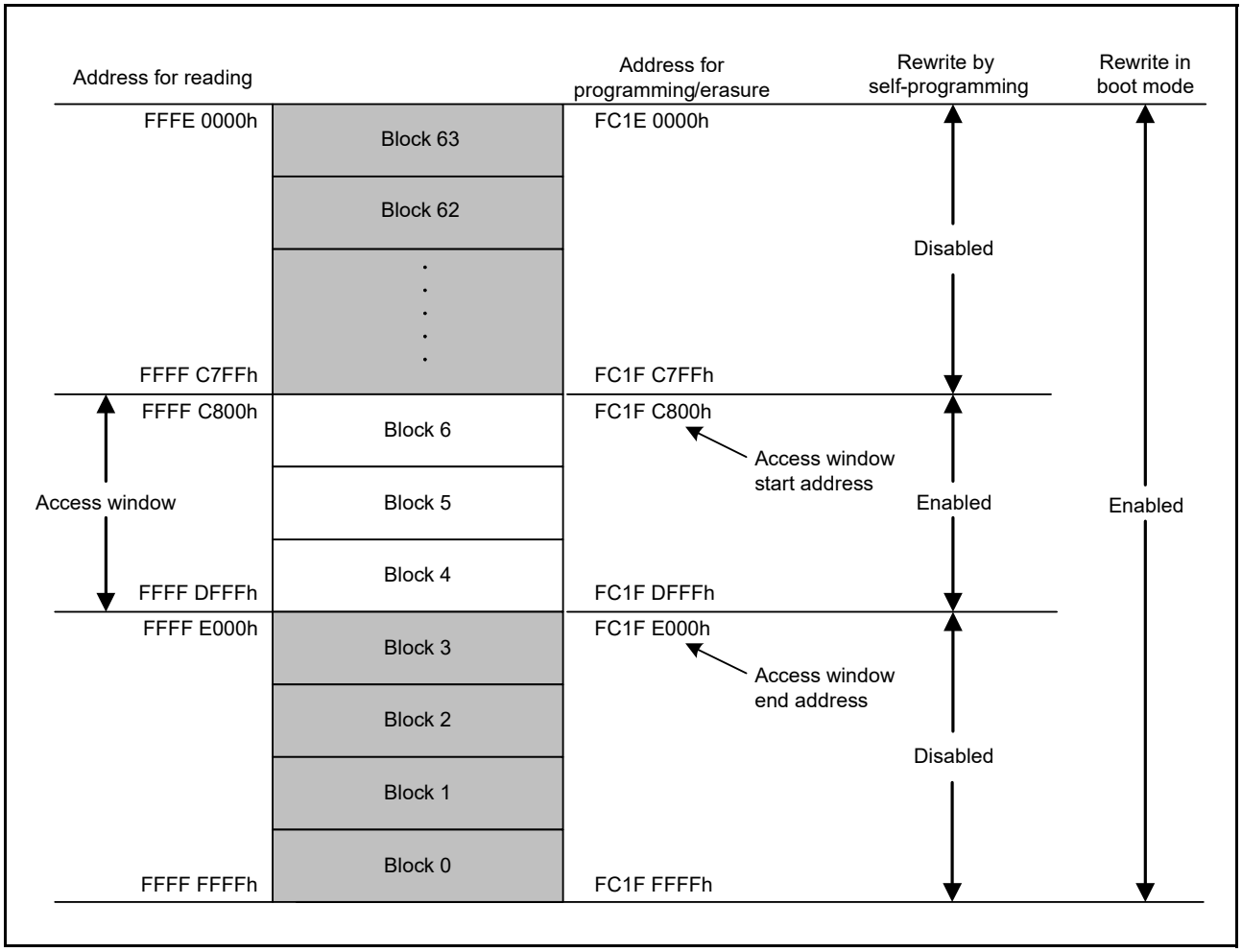


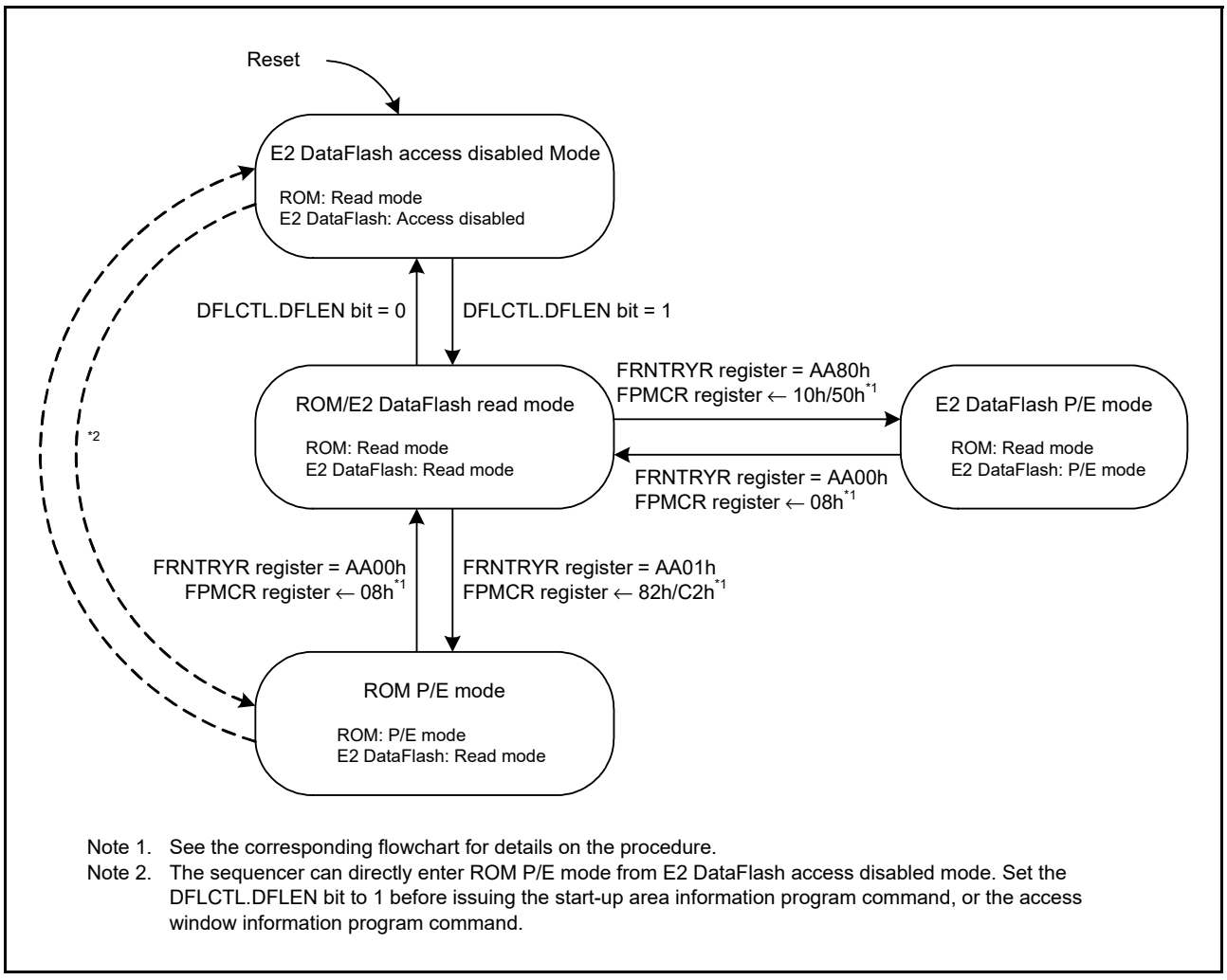
Figure 36.5 Area Protection Overview (When Blocks 4 to 6 are Set as the Access Window in Products with 128-Kbyte ROM)

36.7 Programming and Erasure

The ROM and E2 DataFlash can be programmed and erased by changing the mode of the dedicated sequencer for programming and erasure, and by issuing commands for programming and erasure.
The mode transitions and commands required to program or erase the ROM and E2 DataFlash are described below. The descriptions apply in common to boot mode and single-chip mode.

36.7.1 Sequencer Modes

The sequencer has four modes. Transitions between modes are caused by writing to the DFLCTL and FENTRYR registers and setting the FPMCR register. Figure 36.6 is a diagram of mode transitions of the flash memory.



Note 1. See the corresponding flowchart for details on the procedure.
Note 2. The sequencer can directly enter ROM P/E mode from E2 DataFlash access disabled mode. Set the DFLCTL.DFLEN bit to 1 before issuing the start-up area information program command, or the access window information program command.

Figure 36.6 Mode Transitions of the Flash Memory

36.7.1.1 E2 DataFlash Access Disabled Mode

In E2 DataFlash access disabled mode, access to the E2 DataFlash is disabled. After a reset, the sequencer enters this mode.
When setting the DFLCTL.DFLEN bit to 1, the E2 DataFlash is placed in read mode.

36.7.1.2 Read Mode

Read mode is for high-speed reading of the ROM/E2 DataFlash. Reading from a ROM address for reading can be accomplished in one ICLK clock.

(1) ROM/E2 DataFlash Read Mode

In this mode, both the ROM and E2 DataFlash are in read mode. The sequencer enters this mode from P/E mode when setting the FPMCR register to 08h, setting the FENTRYR.FENTRYD bit to 0, and setting the FENTRYR.FENTRY0 bit to 0.

36.7.1.3 P/E Modes

The P/E mode is for programming and erasure of the ROM/E2 DataFlash.

(1) ROM P/E Mode

In this mode, the ROM is in P/E mode, and the E2 DataFlash is in read mode. The sequencer enters this mode when setting the FENTRYR.FENTRYD to 0, setting the FENTRYR.FENTRY0 bit to 1, and setting the FPMCR register 82h or C2h.

(2) E2 DataFlash P/E Mode

In this mode, the ROM is in read mode, and the E2 DataFlash is in P/E mode. The sequencer enters this mode when the setting the FENTRYR.FENTRYD to 1, setting the FENTRYR.FENTRY0 bit to 0, and setting the FPMCR register 10h or 50h.

36.7.2 Mode Transitions

36.7.2.1 Transition from E2 DataFlash Access Disable Mode to Read Mode

Reading of the E2 DataFlash requires switching from E2 DataFlash access disabled mode to ROM/E2 DataFlash read mode.

Set the DFLCTL.DFLEN bit to 1 to switch to ROM/E2 DataFlash read mode.

Figure 36.7 shows the Procedure for Transition from E2 DataFlash Access Disabled Mode to ROM/E2 DataFlash Read Mode.

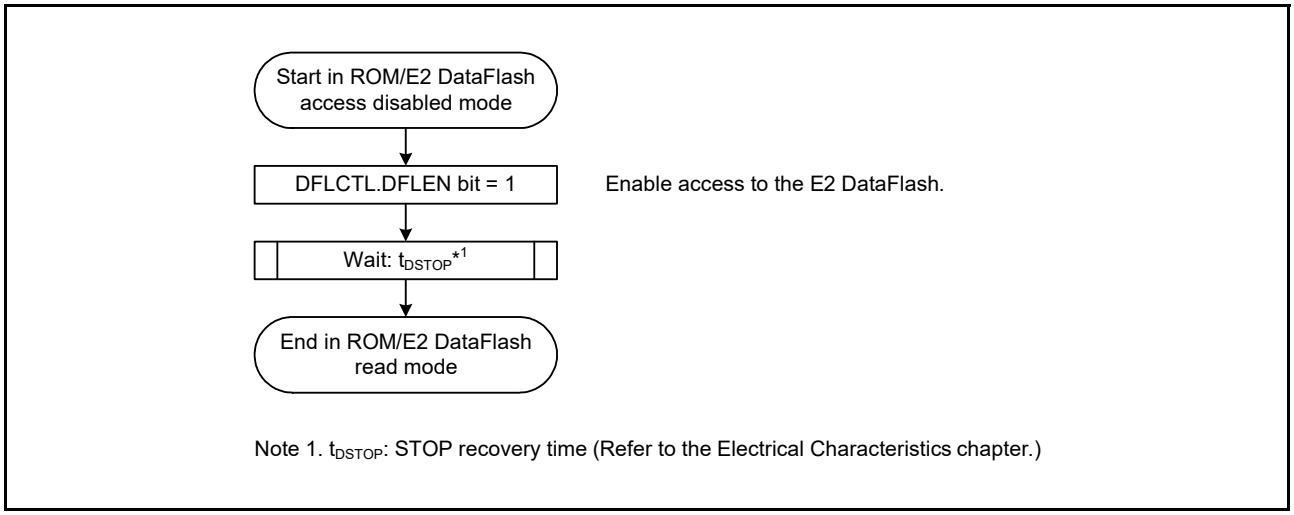
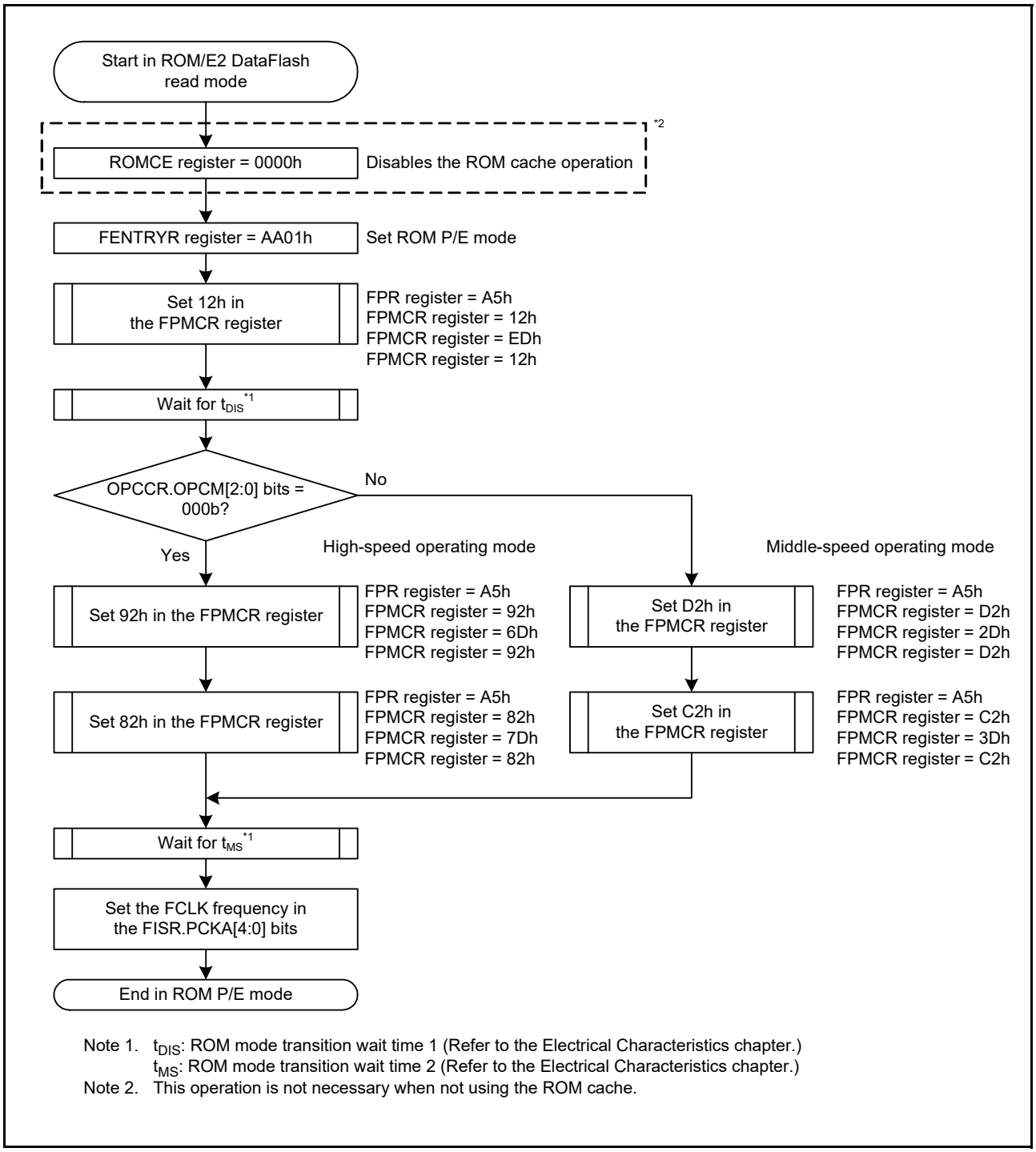


Figure 36.7 Procedure for Transition from E2 DataFlash Access Disabled Mode to ROM/E2 DataFlash Read Mode

36.7.2.2 Transition from Read Mode to P/E Mode

Switching to ROM P/E mode is required before executing a software command for the ROM.
Figure 36.8 shows the Procedure for Transition from ROM/E2 DataFlash Read Mode to ROM P/E Mode. Figure 36.9 shows the Procedure for Transition from ROM/E2 DataFlash Read Mode to E2 DataFlash P/E Mode.



Note 1. t_{DIS}: ROM mode transition wait time 1 (Refer to the Electrical Characteristics chapter.)
t_{MS}: ROM mode transition wait time 2 (Refer to the Electrical Characteristics chapter.)
Note 2. This operation is not necessary when not using the ROM cache.

Figure 36.8 Procedure for Transition from ROM/E2 DataFlash Read Mode to ROM P/E Mode

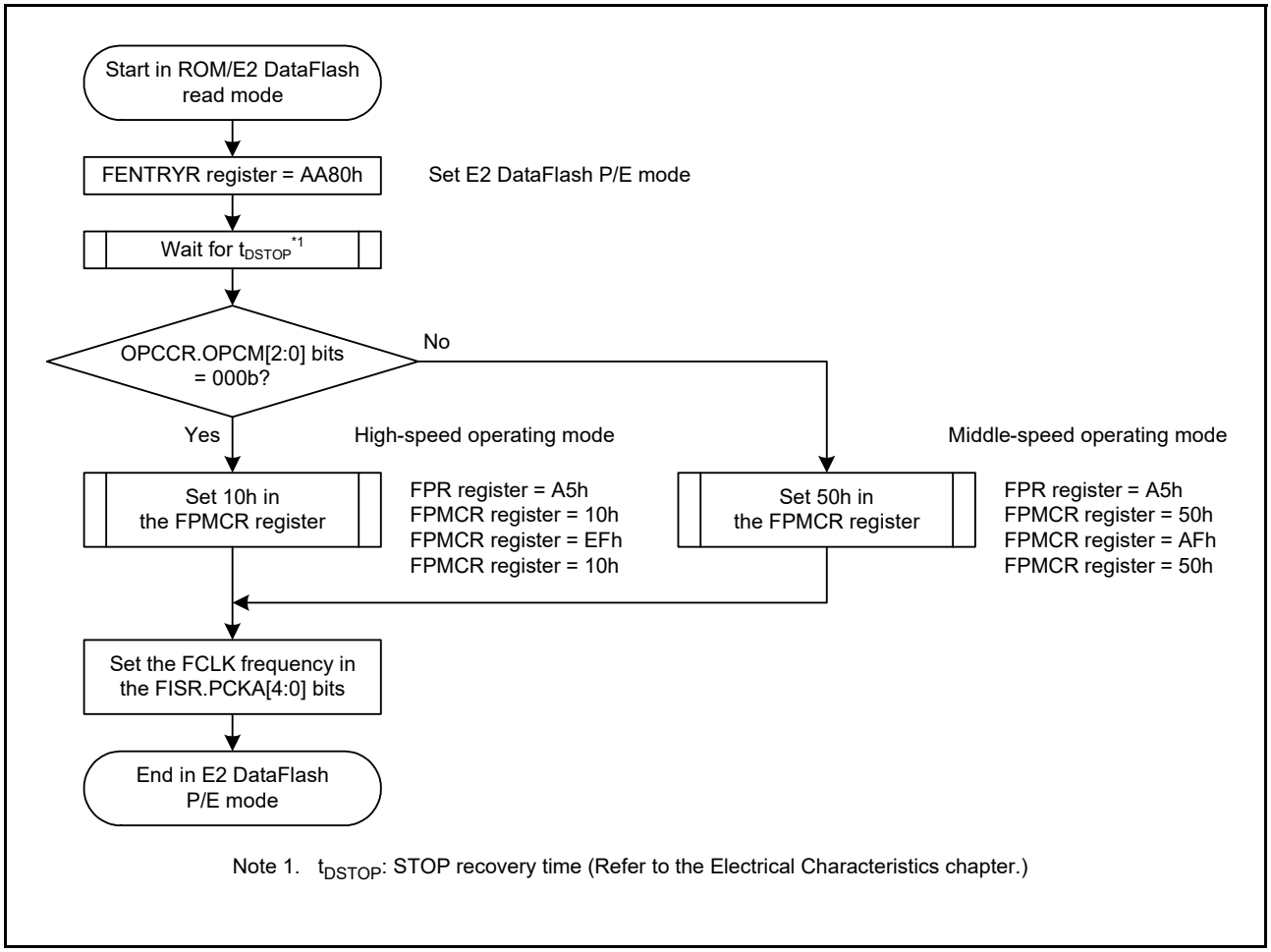
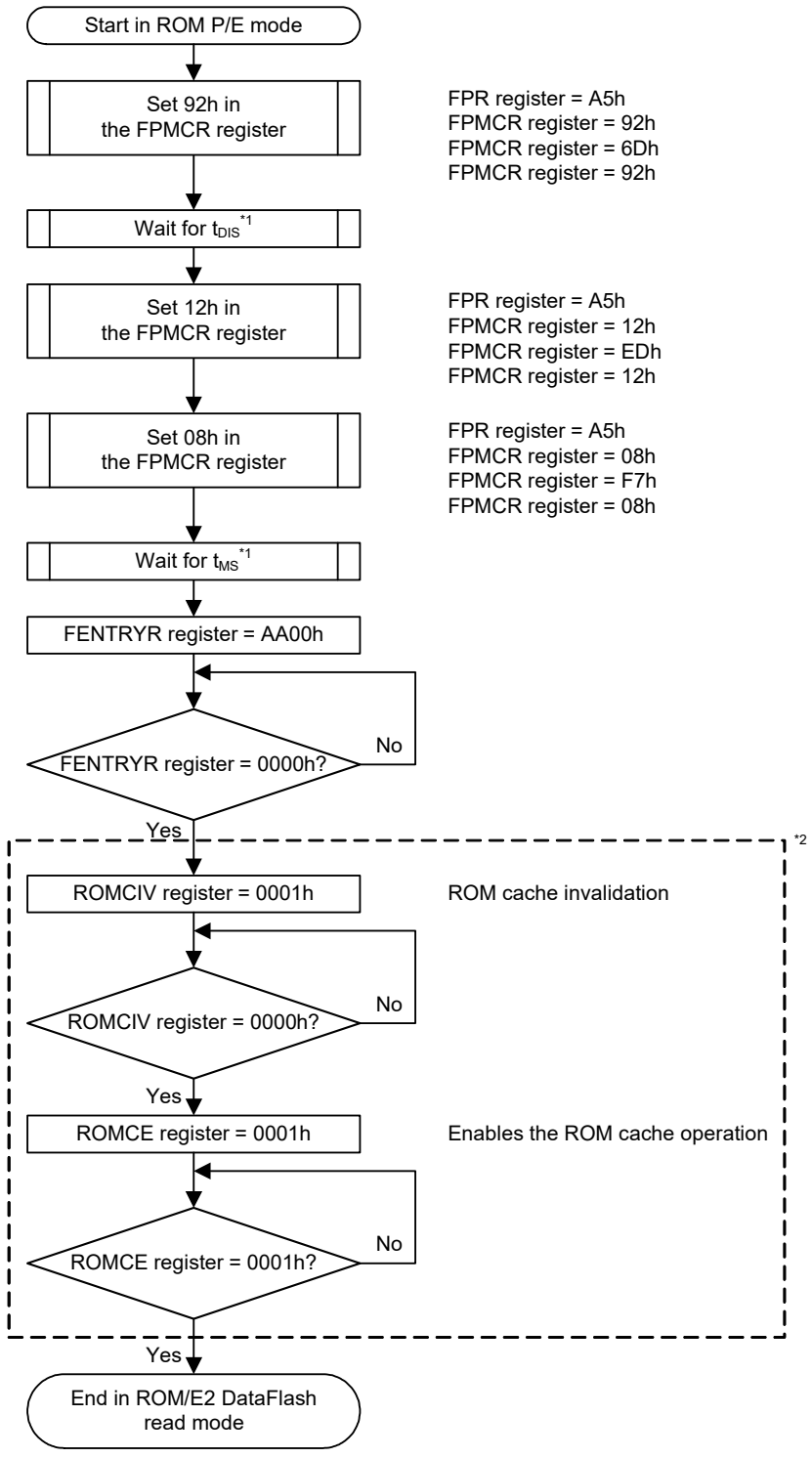


Figure 36.9 Procedure for Transition from ROM/E2 DataFlash Read Mode to E2 DataFlash P/E Mode

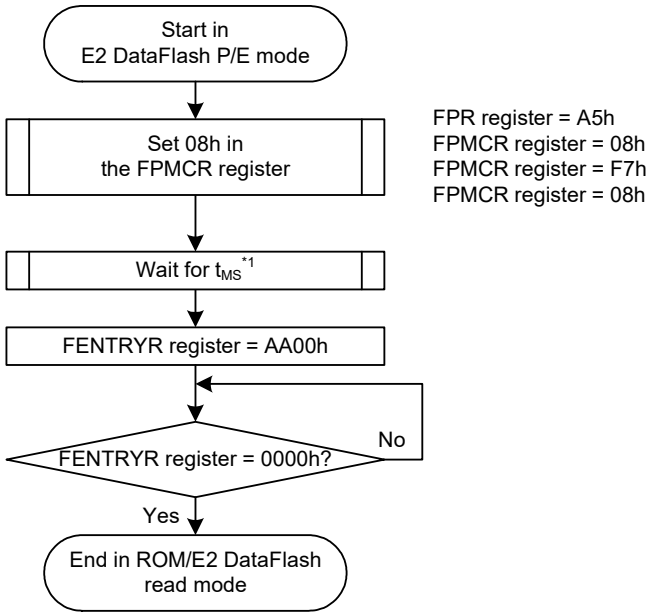
36.7.2.3 Transition from P/E Mode to Read Mode

High-speed reading of the ROM requires switching to ROM/E2 DataFlash read mode.
Figure 36.10 shows the Procedure for Transition from ROM P/E Mode to ROM/E2 DataFlash Read Mode. Figure 36.11 shows the Procedure for Transition from E2 DataFlash P/E Mode to ROM/E2 DataFlash Read Mode.



Note 1. t_{DIS}: ROM mode transition wait time 1 (Refer to the Electrical Characteristics chapter.)
t_{MS}: ROM mode transition wait time 2 (Refer to the Electrical Characteristics chapter.)
Note 2. These operations are not necessary when not using the ROM cache.

Figure 36.10 Procedure for Transition from ROM P/E Mode to ROM/E2 DataFlash Read Mode



Note 1. t_{MS}: ROM mode transition wait time 2 (Refer to the Electrical Characteristics chapter.)

Figure 36.11 Procedure for Transition from E2 DataFlash P/E Mode to ROM/E2 DataFlash Read Mode

36.7.3 Software Commands

Software commands consist of commands for programming and erasure and commands for programming start-up program area information and access window information. Table 36.5 lists the software commands for use with the flash memory.

Table 36.5 Software Commands

Command	Function
Program	• ROM programming (8 bytes) • E2 DataFlash programming (1 byte)
Block erase	ROM/E2 DataFlash erasure
All-block erase	Erasure of all blocks in the ROM/E2 DataFlash
Blank check	Check whether the specified area is blank. Confirm that data is not programmed in the area. This command does not guarantee whether the area remains erased.
Start-up area information program	Rewrite the start-up area switching information used for start-up program protection.
Access window information program	Set the access window used for area protection.

36.7.4 Software Command Usage

This section describes how to use each software command, using flowcharts.

36.7.4.1 Program

Figure 36.12 and Figure 36.13 show the procedure to issue the program command.

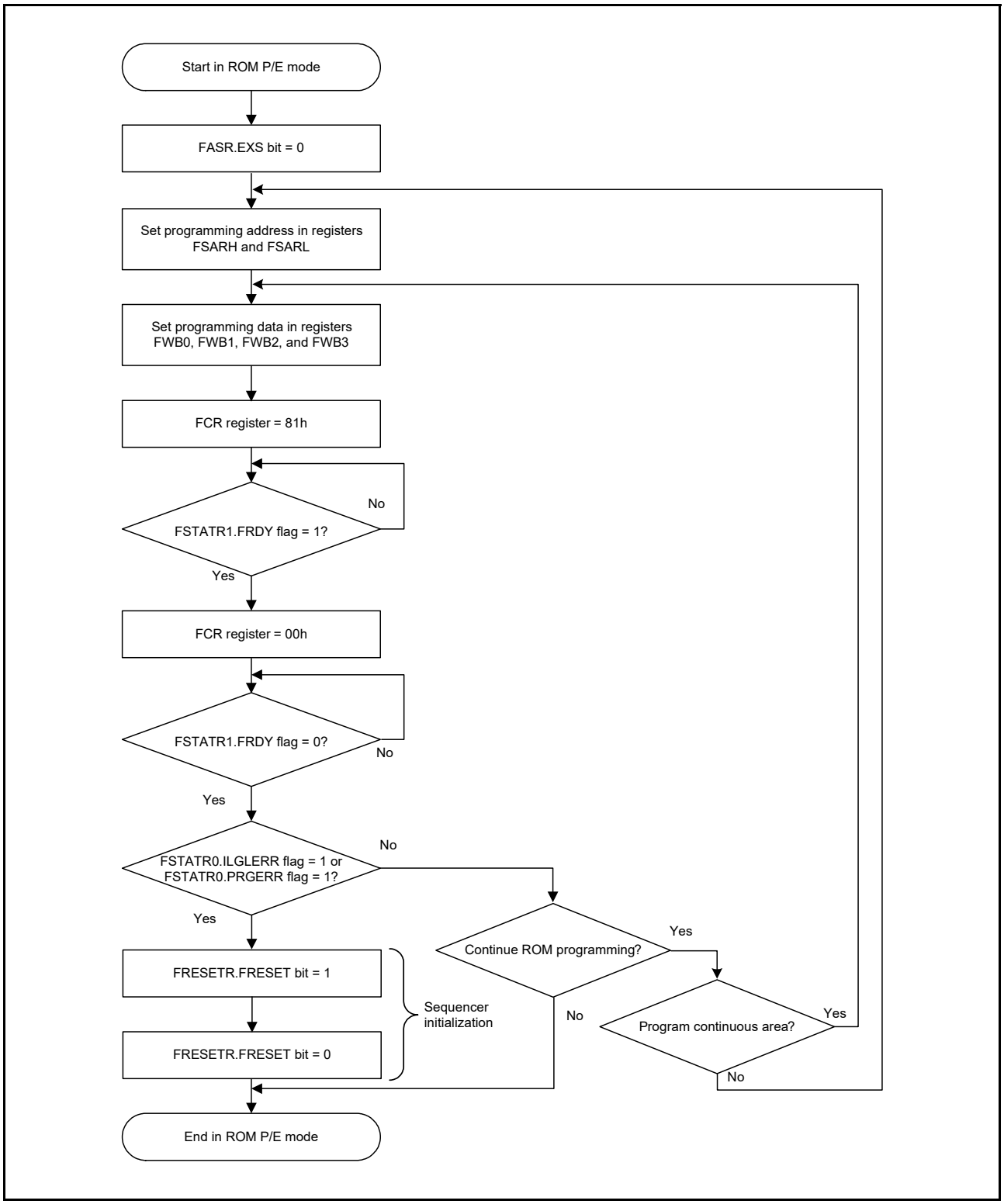


Figure 36.12 Procedure to Issue the Program Command for the ROM

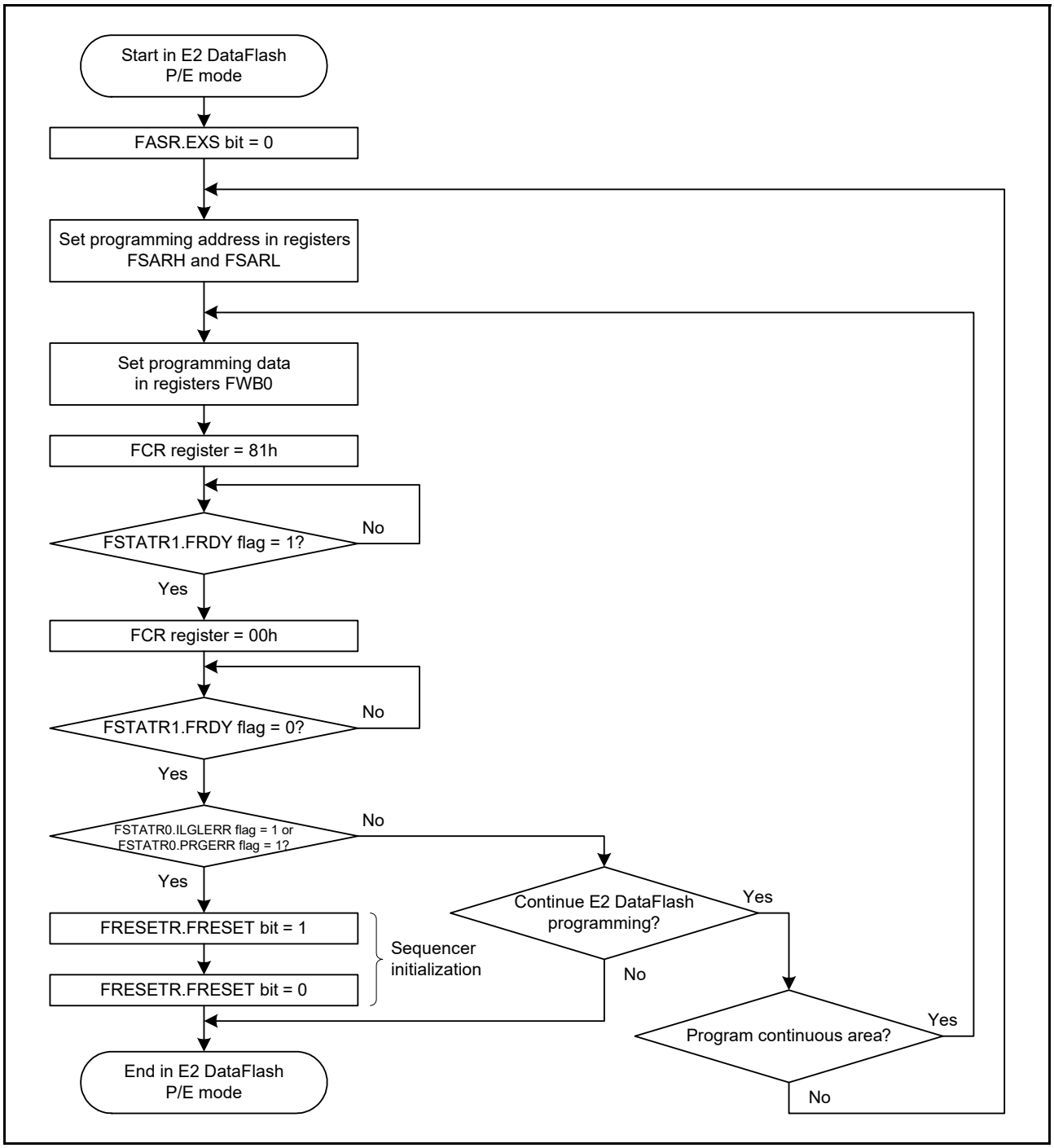


Figure 36.13 Procedure to Issue the Program Command for the E2 DataFlash

36.7.4.2 Block Erase

Figure 36.14 and Figure 36.15 show the procedure to issue the block erase command.

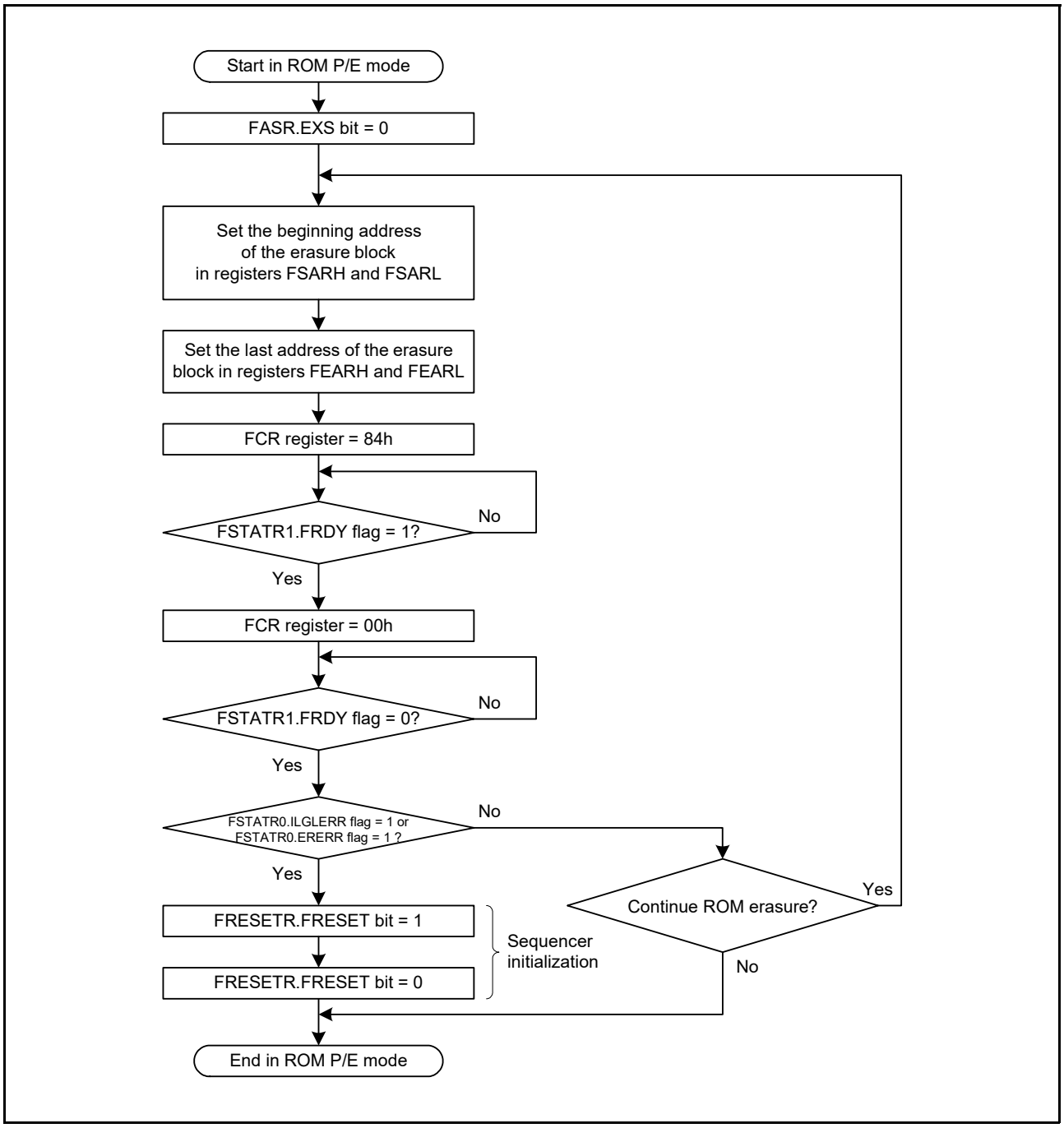


Figure 36.14 Procedure to Issue the Block Erase Command for the ROM

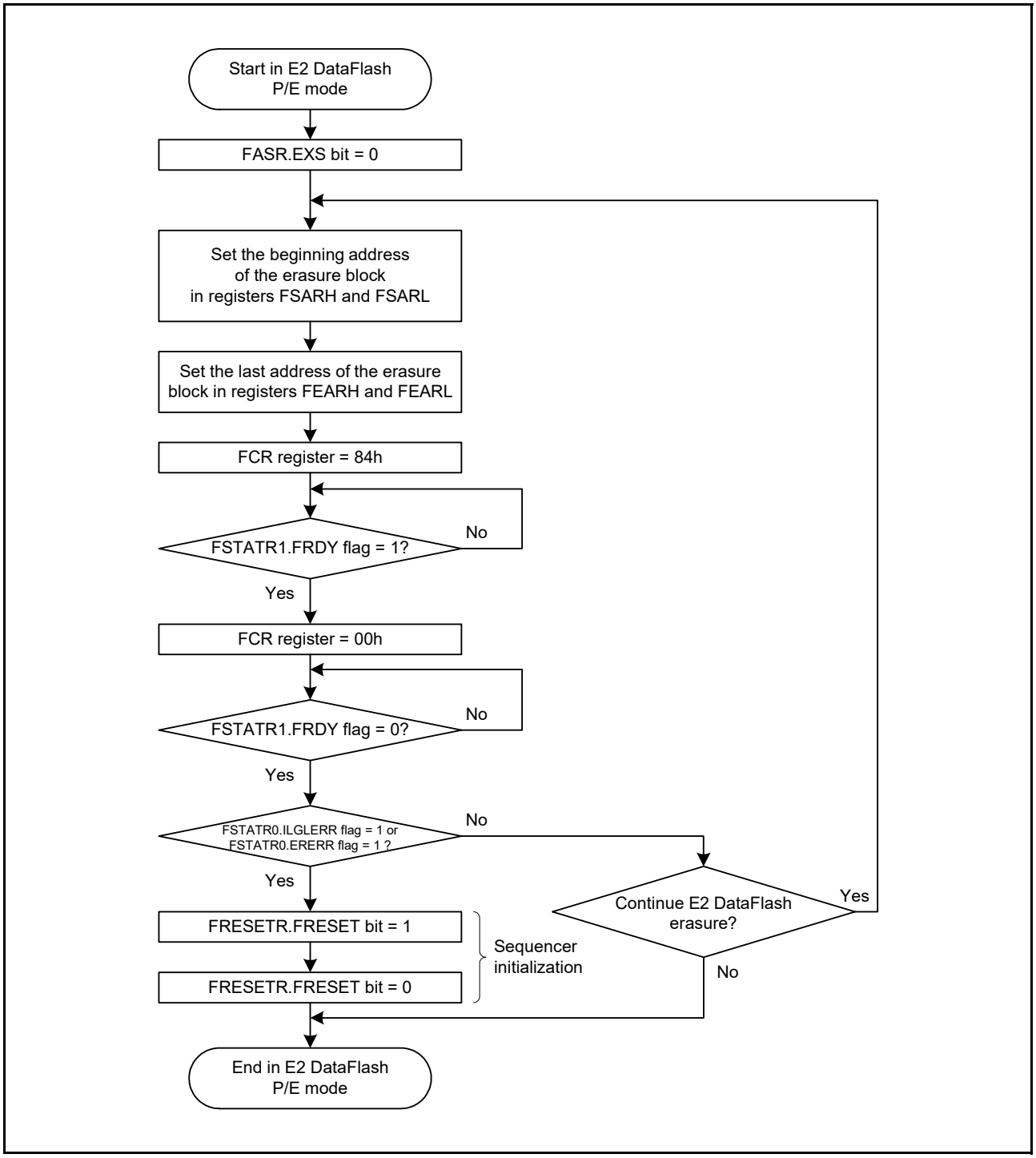


Figure 36.15 Procedure to Issue the Block Erase Command for the E2 DataFlash

36.7.4.3 All-Block Erase

Figure 36.16 and Figure 36.17 show the procedure to issue the all-block erase command.

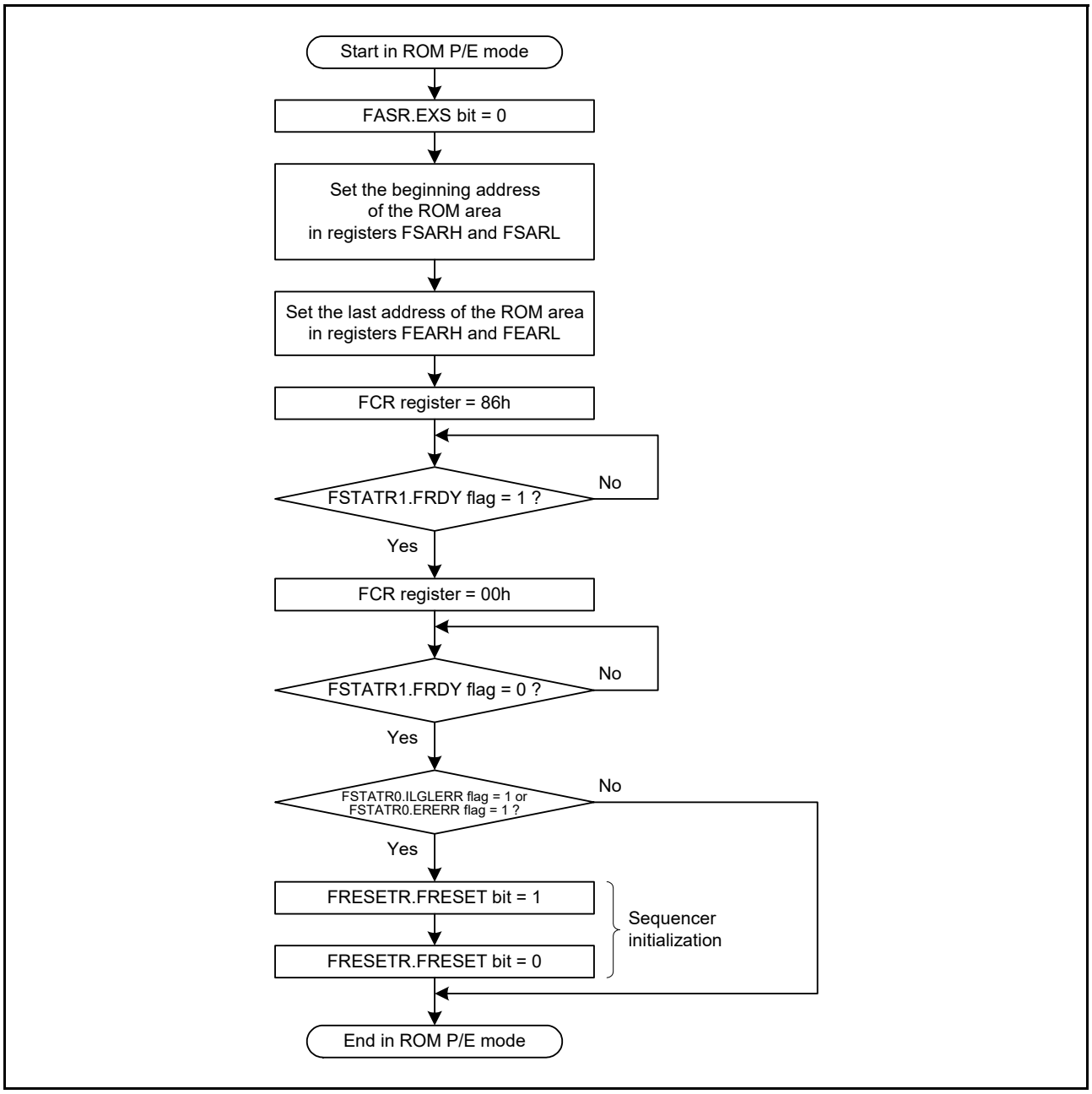


Figure 36.16 Procedure to Issue the All-Block Erase Command for the ROM

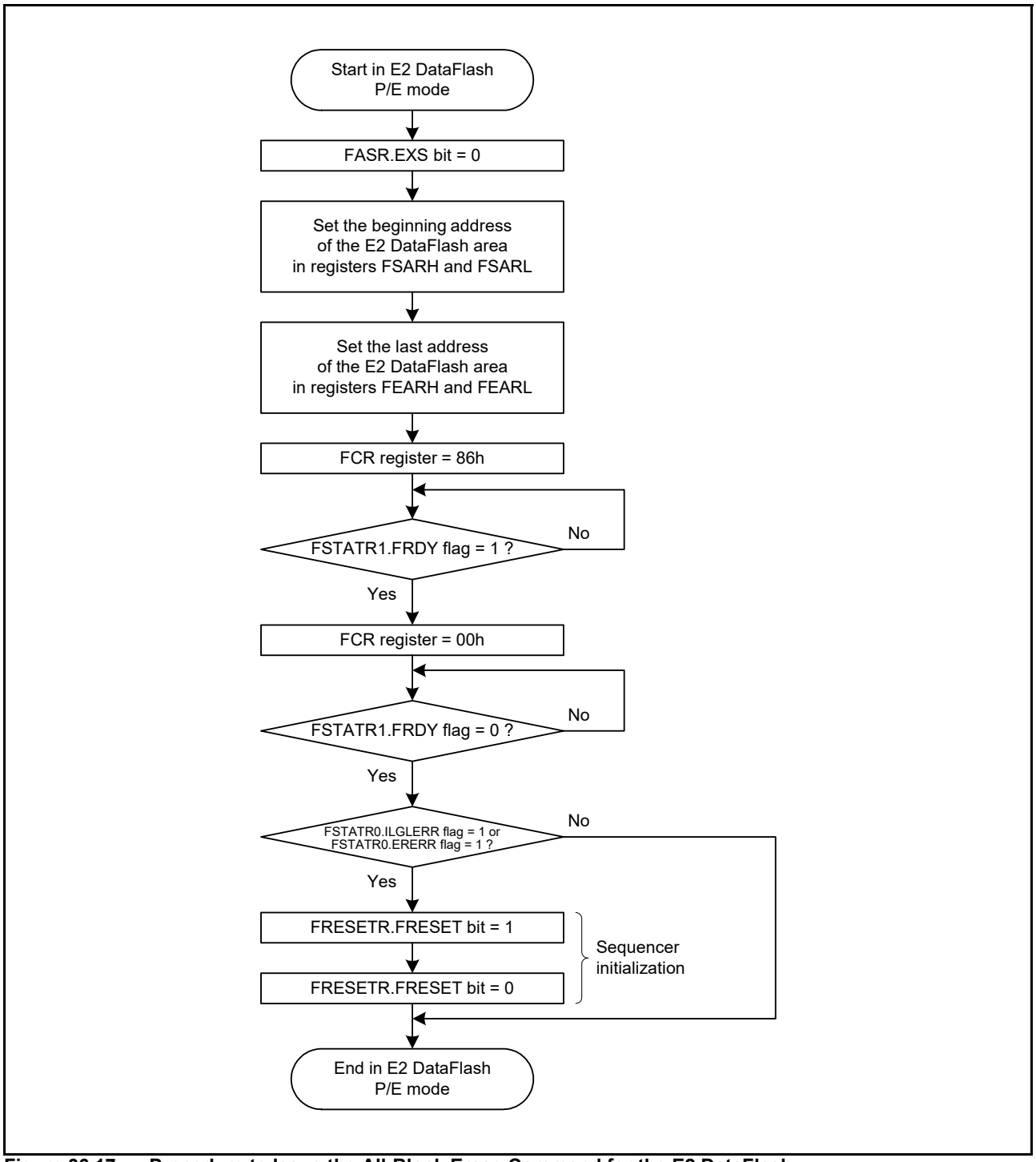


Figure 36.17 Procedure to Issue the All-Block Erase Command for the E2 DataFlash

36.7.4.4 Blank Check

Figure 36.18 and Figure 36.19 show the procedure to issue the blank check command.

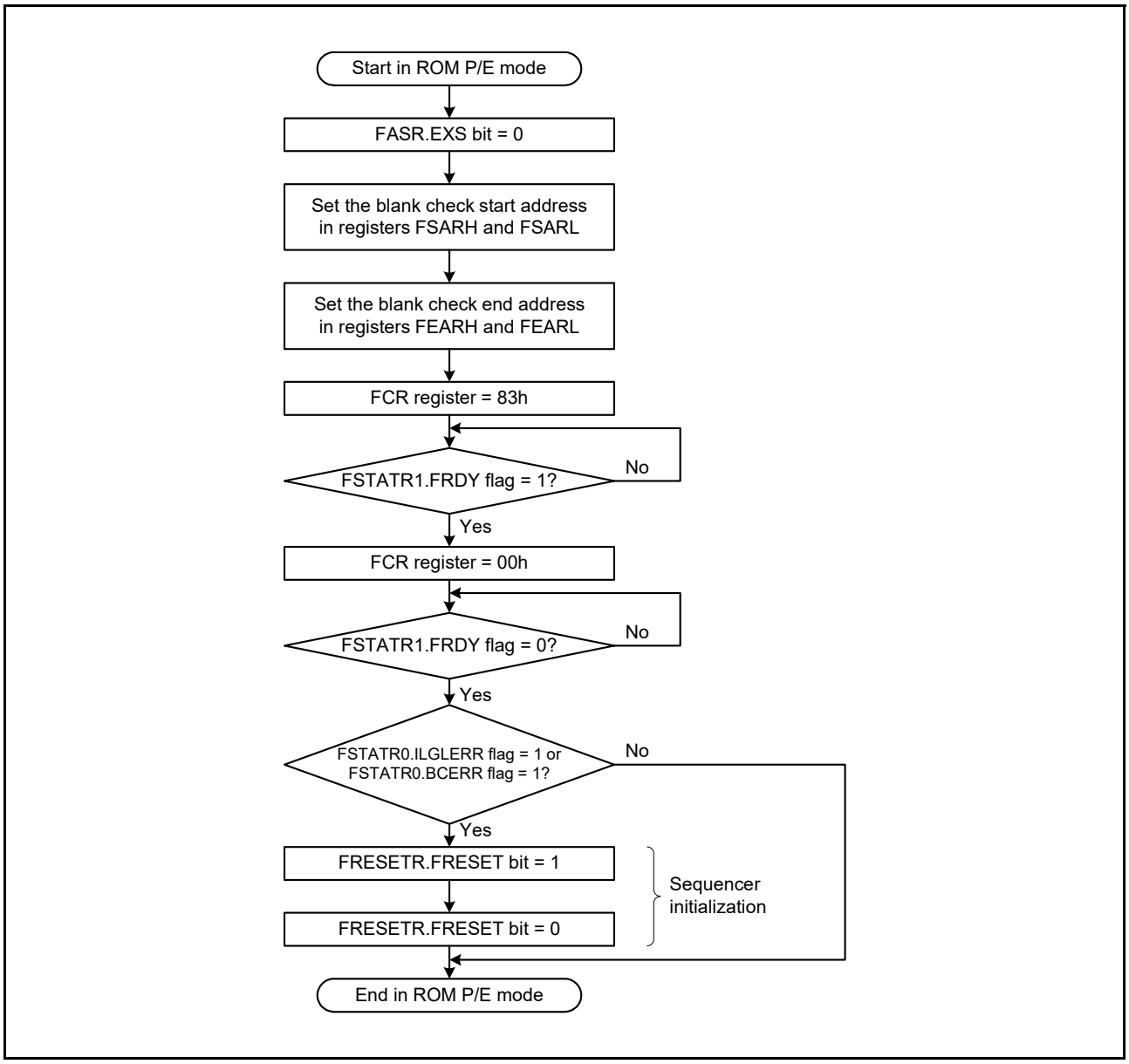


Figure 36.18 Procedure to Issue the Blank Check Command for the ROM

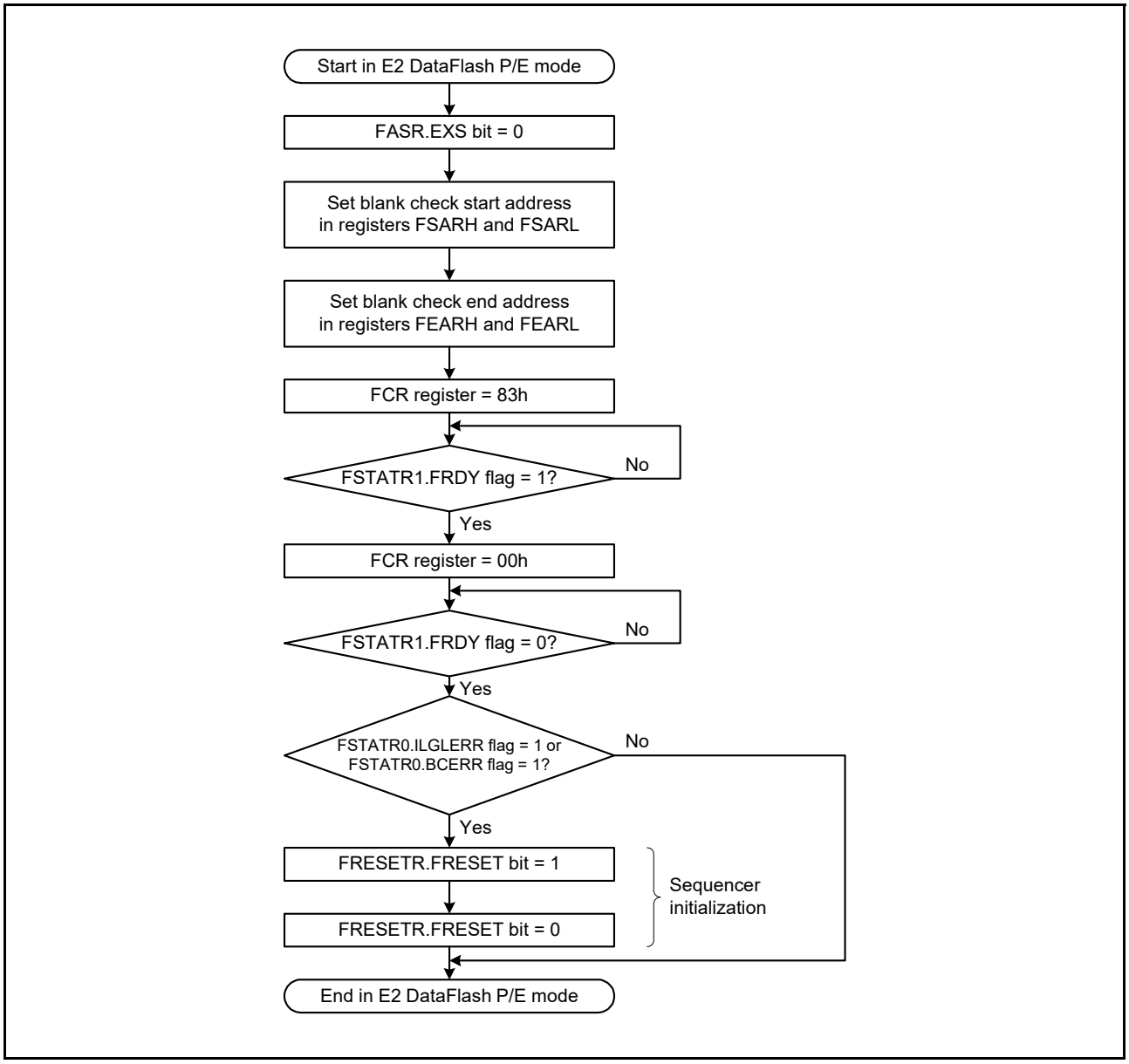


Figure 36.19 Procedure to Issue the Blank Check Command for the E2 DataFlash

36.7.4.5 Start-Up Area Information Program/Access Window Information Program

Figure 36.20 shows the procedure to issue the start-up area information program command and access window information program command.

When the sequencer has directly entered ROM/PE mode from E2 DataFlash access disabled mode, set the DFLCTL.DFLEN bit to 1 at the beginning of the procedure.

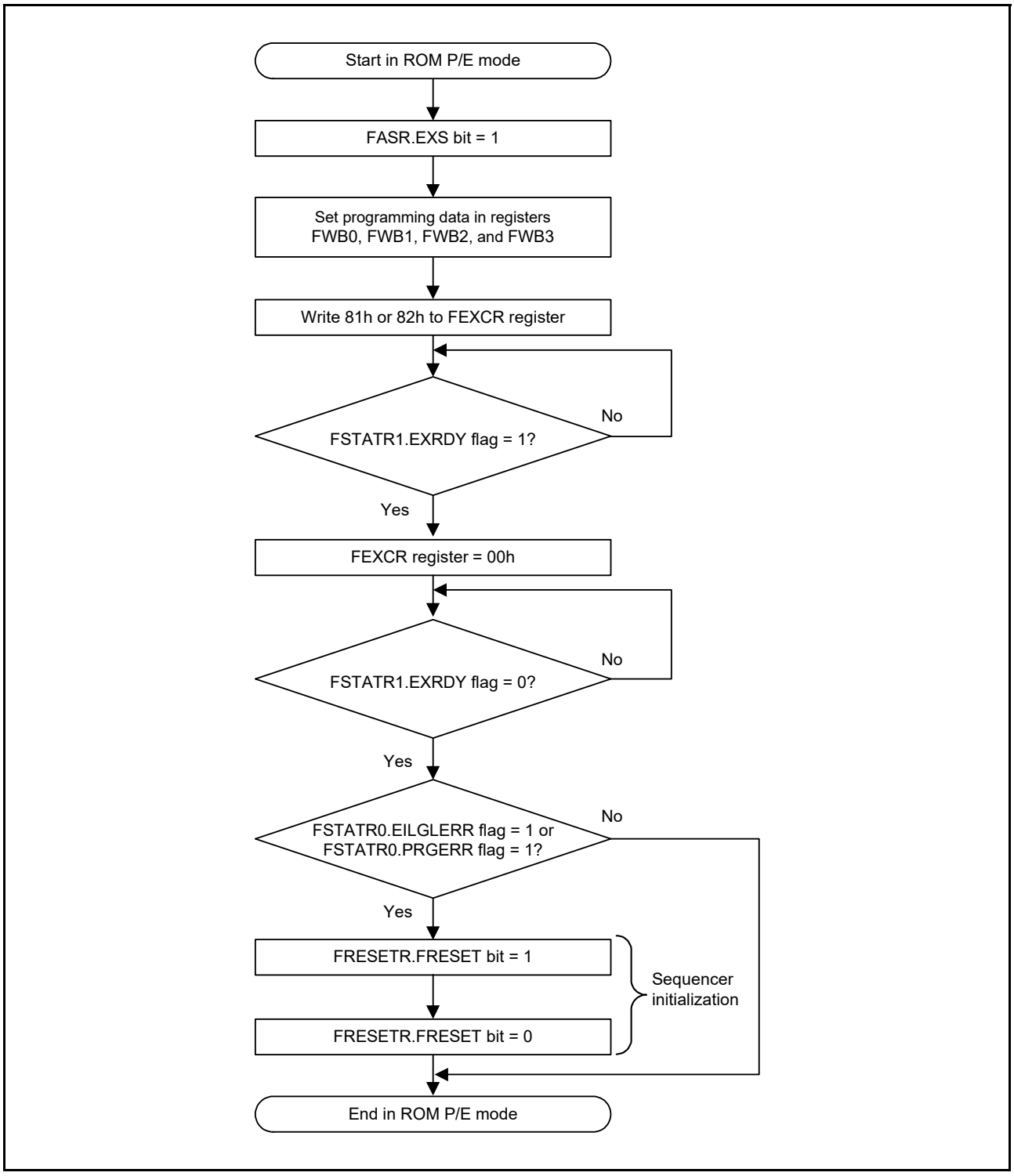


Figure 36.20 Procedure to Issue the Start-Up Area Information Program Command/Access Window Information Program Command

36.7.4.6 Forced Stop of Software Commands

Perform the procedure shown in Figure 36.21 to forcibly stop the blank check command or block erase command. When the command processing is forcibly stopped, registers FEAMH and FEAML store the address at the time of the forced stop. For blank check, the stopped processing can be continued by copying the FEAMH and FEAML register values to registers FSARH and FSARL.

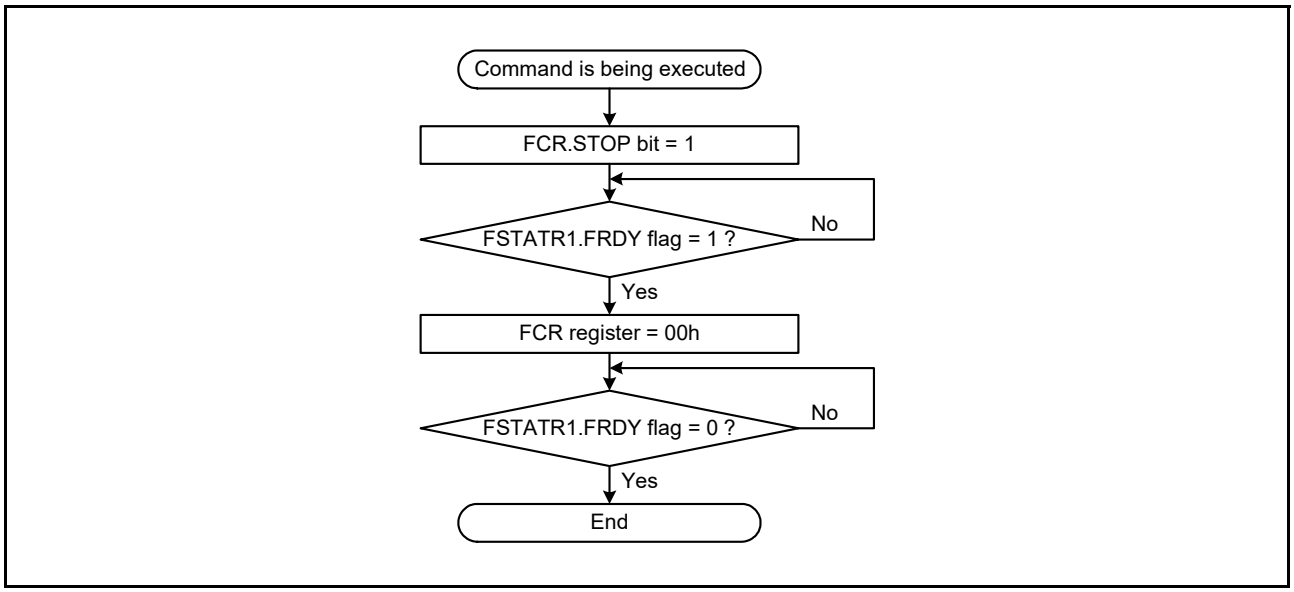


Figure 36.21 Procedure for Forced Stop of Software Commands

36.7.5 Interrupt

When software command processing or forced stop processing is completed, an interrupt (FRDYI) is generated.
When the FSTATR1.FRDY flag becomes 0 by setting the FCR.OPST bit to 0 and the FSTATR1.EXRDY flag becomes 0 by setting the FEXCR.OPST bit to 0, the next interrupt (FRDYI) can be accepted.
Clear the IRn.IR flag before setting the IERm.IEN bit of the ICU corresponding to this interrupt.

36.8 Boot Mode

The SCI or FINE interface is used in boot mode.

Table 36.6 lists the Programmable and Erasable Areas and Peripheral Modules Used in Boot Mode. Table 36.7 lists the I/O Pins Used in Boot Mode.

Table 36.6 Programmable and Erasable Areas and Peripheral Modules Used in Boot Mode

	Boot Mode	
Item	**SCI Interface**	**FINE Interface**
Programmable and erasable areas	User area Data area	User area Data area
Peripheral module	SCI1 (asynchronous serial communication)	FINE

Table 36.7 I/O Pins Used in Boot Mode

Pin Name	I/O	Mode	Description
MD	Input	Boot mode	Select operating mode (refer to section 3, Operating Modes).
MD/FINED	I/O	Boot mode (FINE interface)	Select operating mode, FINE data I/O
PD5/RXD1	Input	Boot mode (SCI)	Receive data*1
PD3/TXD1	Output		Transmit data*1

Note 1. Connect (pull up) this pin to VCC via a resistor.

36.8.1 Boot Mode (SCI)

The flash memory can be programmed and erased using asynchronous serial communication in boot mode (SCI). The user area and data area can be rewritten.
When a reset is released while the MD pin is low, the MCU starts in boot mode (SCI).
Contact the manufacturer for details on the serial programmer.

36.8.1.1 Operating Conditions in Boot Mode (SCI)

SCI1 is used to communicate with the serial programmer in boot mode (SCI).
Figure 36.22 shows an Example of Pin Connections in Boot Mode (SCI). Table 36.8 lists Pin Handling in Boot Mode (SCI).
The examples of pin connections shown in Figure 36.22 are simplified circuits. Operations are not guaranteed in all systems.

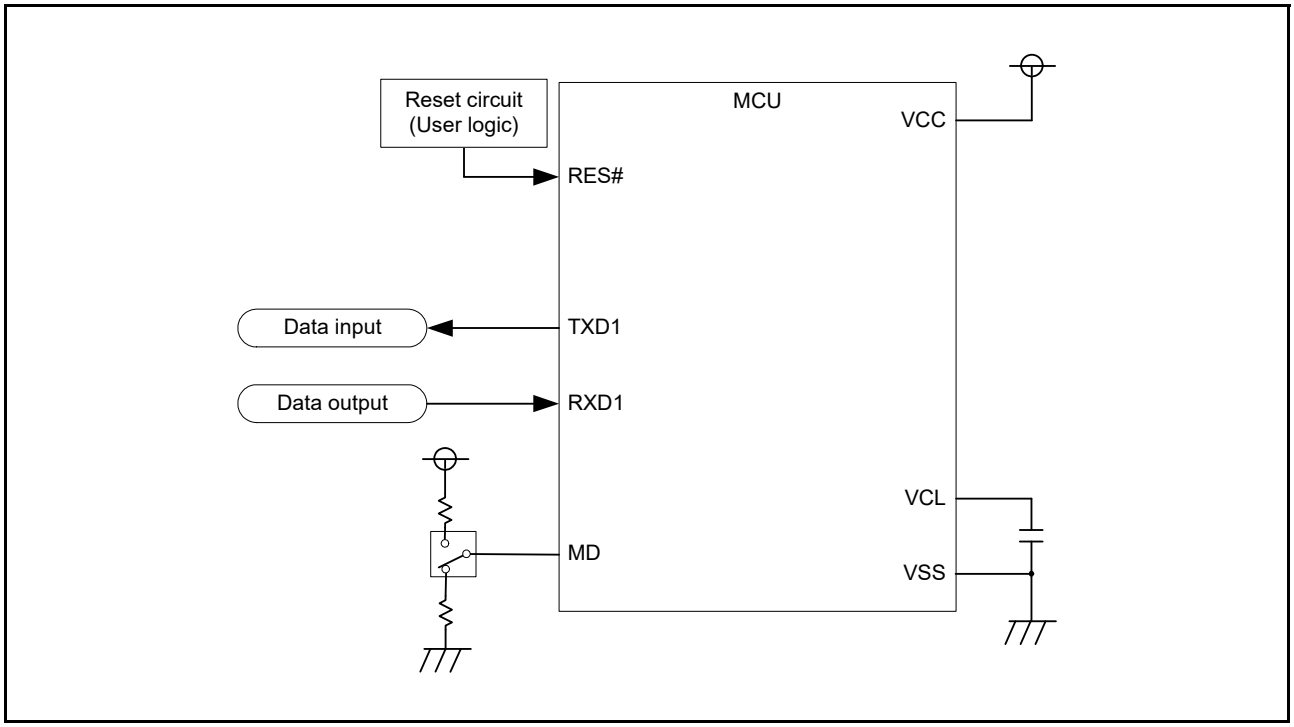


Figure 36.22 Example of Pin Connections in Boot Mode (SCI)

Table 36.8 Pin Handling in Boot Mode (SCI)

Pin Name	Name	I/O	Function
VCC, VSS	Power supply	—	Input 2.7 V or higher to the VCC pin. Input 0 V to the VSS pin.
VCL	Decoupling capacitor connect pin	—	Connect to the VSS pin via a decoupling capacitor for stabilizing the internal voltage.
MD	Operating mode control	Input	Input low.
RES#	Reset input	Input	Reset pin. Connect to the reset circuit.
PD5/RXD1	Data input RXD	Input	Input pin for serial data
PD3/TXD1	Data output TXD	Output	Output pin for serial data

As shown in Figure 36.23, set the format to 8-bit data, 1 stop bit, no parity, and LSB first to communicate with the serial programmer.

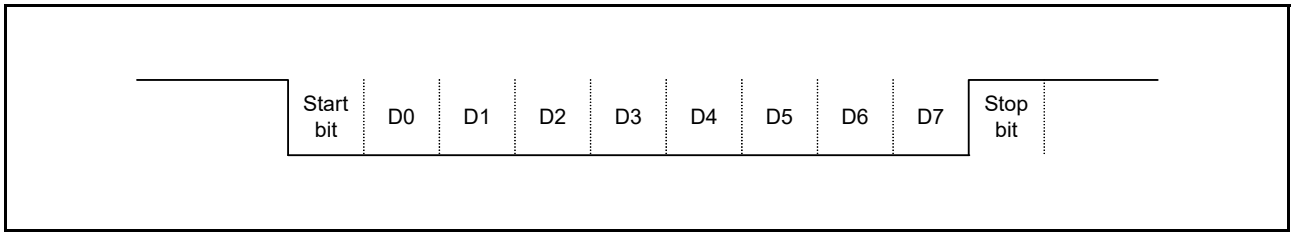


Figure 36.23 Communication Format

Initial communication with the programmer is performed at 9,600 or 19,200 bps. The communication bit rate can be changed after the MCU is connected with the programmer.
Table 36.9 lists the maximum communication bit rates for communication in boot mode (SCI).

Table 36.9 Conditions for Communication

Operating Voltage	Maximum Communication Bit Rate
2.7 V or higher, and lower than 3.0 V	500 kbps
3.0 V or higher, and 5.5 V or lower	2 Mbps

36.8.1.2 Starting Up in Boot Mode (SCI)

To start up in boot mode (SCI), release the reset (drive the RES# pin high from low) while the MD pin is low. After starting up in boot mode (SCI), wait at least 400 ms until communication is enabled in boot mode (SCI).
As shown in Figure 36.24, keep the signal of each pin unchanged for 400 ms after the reset is released. Use resets according to the range described in section 37.3.2, Reset Timing.

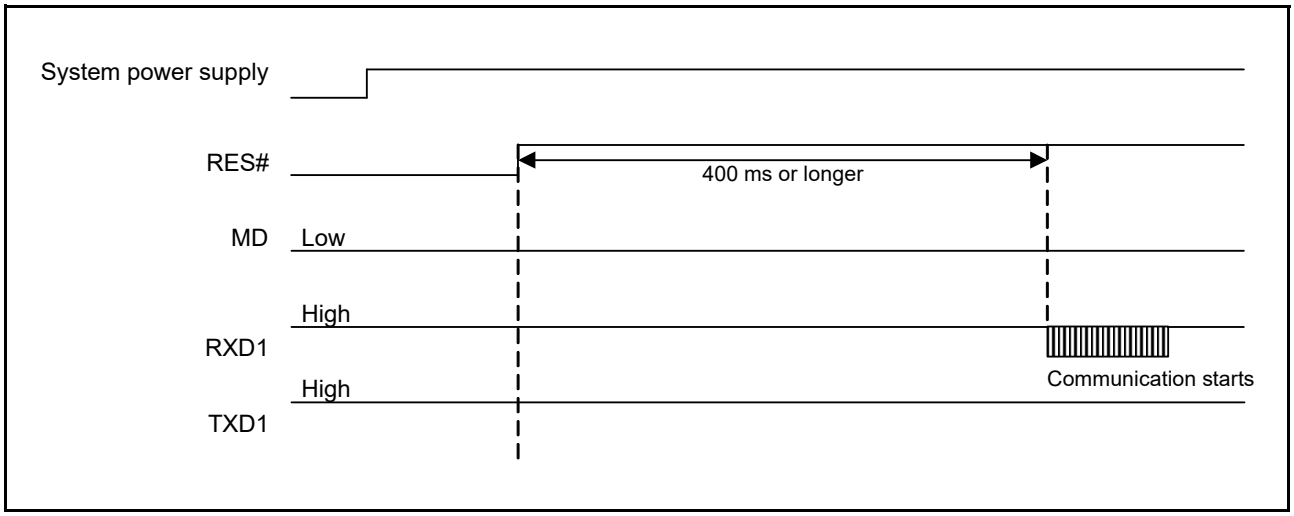


Figure 36.24 Wait Time until Communication Becomes Possible in Boot Mode (SCI)

36.8.2 Boot Mode (FINE Interface)

The flash memory can be programmed and erased using the FINE in boot mode (FINE interface). The user area and data area can be rewritten.
Contact the manufacturer for details on the serial programmer.

36.8.2.1 Operating Conditions in Boot Mode (FINE Interface)

FINE is used to communicate with the serial programmer in boot mode (FINE Interface).
Figure 36.25 shows an Example of Pin Connections in Boot Mode (FINE Interface). Table 36.10 lists Pin Handling in Boot Mode (FINE Interface).
The example of pin connections shown in Figure 36.25 is a simplified circuit. Operations are not guaranteed in all systems.

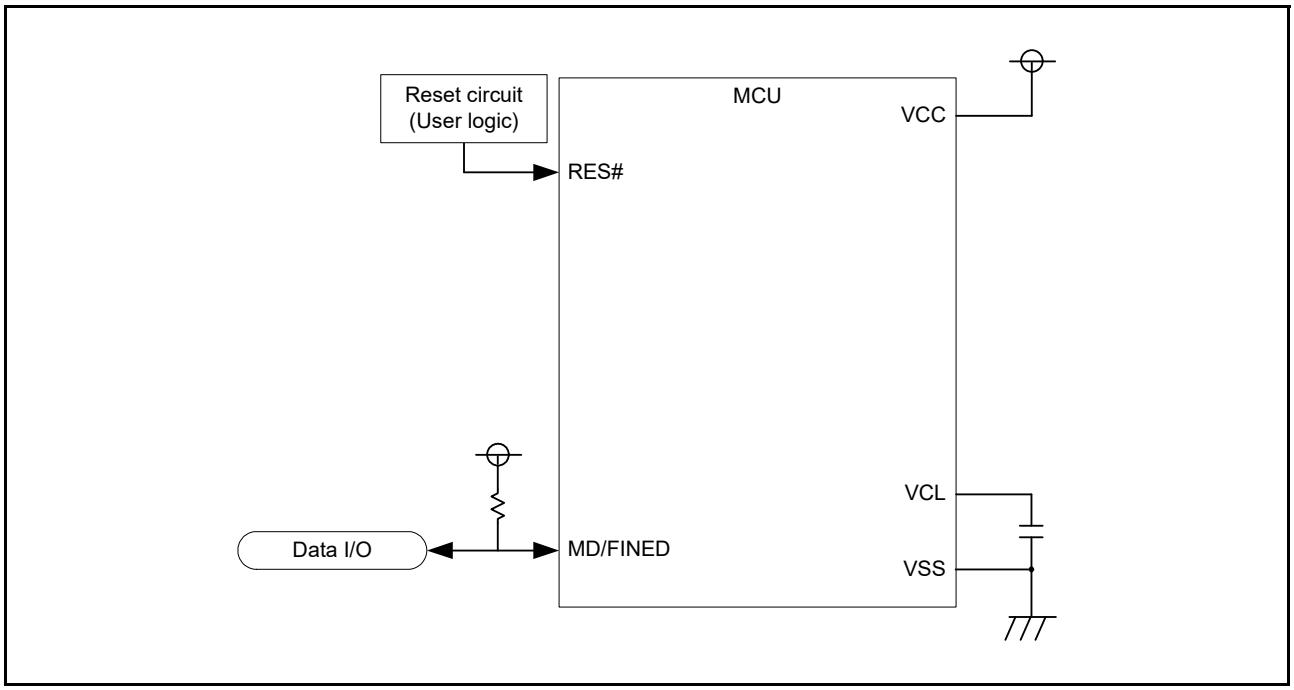


Figure 36.25 Example of Pin Connections in Boot Mode (FINE Interface)

Table 36.10 Pin Handling in Boot Mode (FINE Interface)

Pin Name	Name	I/O	Function
VCC, VSS	Power supply	—	Input 2.7 V or higher to the VCC pin. Input 0 V to the VSS pin.
VCL	Decoupling capacitor connect pin	—	Connect to the VSS pin via a decoupling capacitor for stabilizing the internal voltage.
MD/FINED	Operating mode control/data I/O	I/O	Connect the VSS pin via a resistor (pull up).
RES#	Reset input	Input	Reset pin. Connect to the reset circuit.

36.9 Flash Memory Protection

Flash memory protection prevents the flash memory from being read or rewritten by the third party.
Boot mode ID code protection is for connecting the serial programmer, and on-chip debugging emulator ID code protection is for connecting the on-chip debugging emulator. ROM code protection is for connecting the parallel programmer.

36.9.1 ID Code Protection

There are two types of ID code protection: Boot mode ID code protection for connecting the serial programmer and on-chip debugging emulator ID code protection is for connecting the on-chip debugging emulator. The same ID codes are used for both functions, but operations differ.
ID codes consist of the control code and ID code 1 to ID code 15. Set ID codes to four 32-bit data in 32-bit units. Figure 36.26 shows the ID Code Configuration.

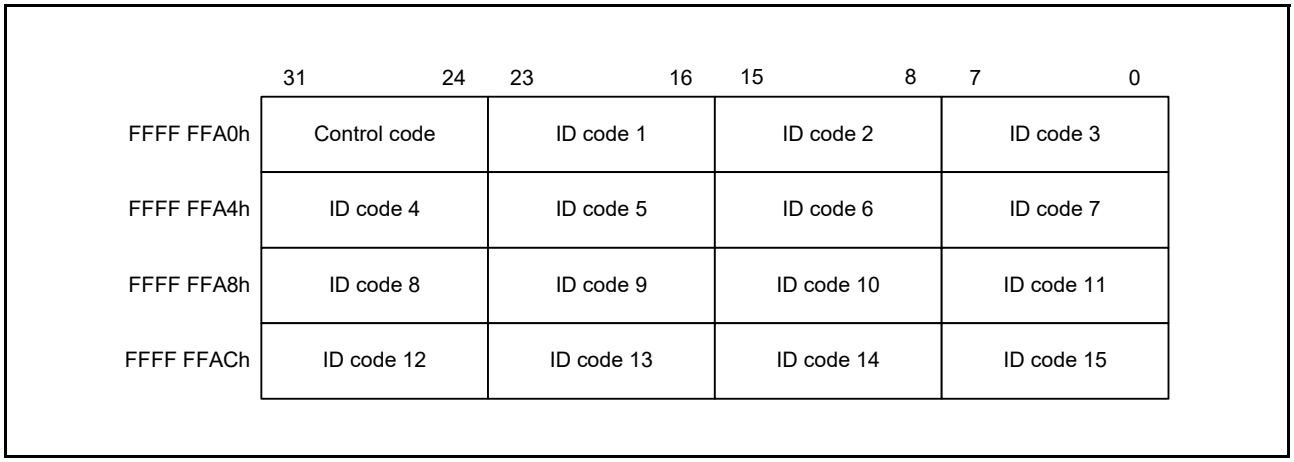


Figure 36.26 ID Code Configuration

The following shows a program example for setting ID codes.
This is an example when setting the control code to 45h and setting ID codes to 01h, 02h, 03h, 04h, 05h, 06h, 07h, 08h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, and 0Fh (from the ID code 1 field to the ID code 15 field).

C language:

```
#pragma address ID_CODE = 0xFFFFFFA0
const unsigned long ID_CODE [4] = {0x45010203, 0x04050607,0x08090A0B, 0x0C0D0E0F};
```

Assembly language:

```
.SECTION ID_CODE,CODE
.ORG 0FFFFFFA0h
.LWORD 45010203h
.LWORD 04050607h
.LWORD 08090A0Bh
.LWORD 0C0D0E0Fh
```

36.9.1.1 Boot Mode ID Code Protection

Boot mode ID code protection disables reading and programming of the user area and data area when the serial programmer is connected by the third party.
When the control code indicates 45h or 52h (boot mode ID code protection is enabled), the MCU compares 16-byte ID code sent from the serial programmer with the ID code in the user area. According to the comparison result, reading and programming the user area and data area is enabled.
When the control code indicates a value other than 45h and 52h (boot mode ID code protection is disabled), all blocks in the user area and data area are erased, and reading and programming the user area and data area are enabled.

The control code is used to enable or disable protection. Table 36.11 lists the specifications of boot mode ID code protection, and Figure 36.27 shows the authentication flow of boot mode ID code protection.
ID code 1 to ID code 15 can be set to any desired value.
However, only when disabling connection with the serial programmer, the ID codes must be set to 50h, 72h, 6Fh, 74h, 65h, 63h, 74h, FFh, FFh, FFh, FFh, FFh, FFh, FFh, and FFh (from the ID code 1 field to the ID code 15 field).

Table 36.11 Boot Mode ID Code Protection Specifications

ID Code				
Control Code	**ID Code 1 to ID Code 15**	**Protection**	**ID Code Matching Result**	**Operation**
45h	Any desired value	Enabled	Matched	Exit the boot mode ID code authentication state and enter the program/erase host command wait state.
			Not matched	Continue the boot mode ID code authentication state.
			Not matched three times consecutively	Erase all blocks in the user area and data area, and continue boot mode ID code authentication state.
52h	50h, 72h, 6Fh, 74h, 65h, 63h, 74h, FFh, ..., and FFh (8 bytes are all FFh)	Enabled	N/A	Disable reading or rewriting of the flash memory, regardless of the codes sent from the serial programmer.
	Other than above		Matched	Exit the boot mode ID code authentication state and enter the program/erase state.
			Not matched	Continue the boot mode ID code authentication state.
Other than above	Any desired value	Disabled	N/A	Erase all blocks in the user area and data area.

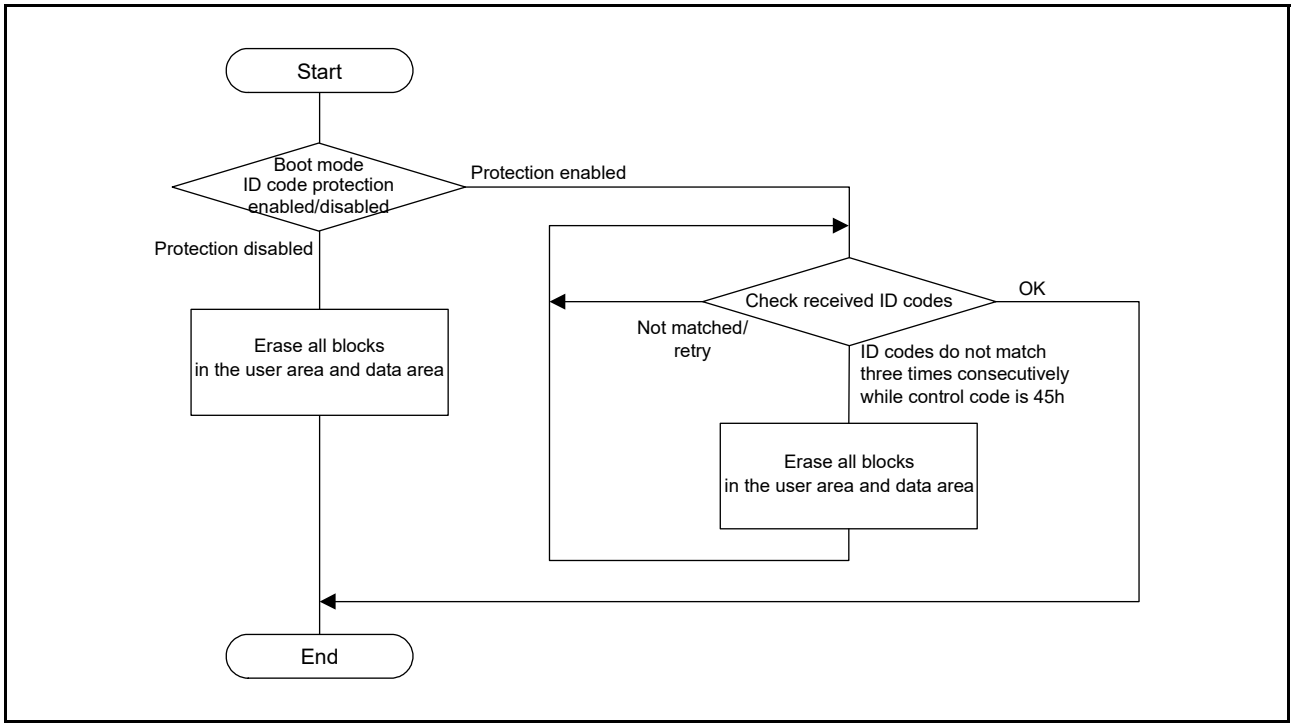


Figure 36.27 Authentication for Boot Mode ID Code Protection

36.9.1.2 On-Chip Debugging Emulator ID Code Protection

On-chip debugging emulator ID code protection enables or disables connection with the on-chip debugging emulator. When the on-chip debugging emulator ID code protection is disabled, connection with the on-chip debugging emulator is enabled. When 16-byte ID codes sent from the on-chip debugging emulator and ID codes in the user area match while on-chip debugging emulator ID code protection is enabled, connection with the on-chip debugging emulator is also enabled.

Table 36.12 lists the specifications of on-chip debugging emulator ID code protection.

Table 36.12 On-Chip Debugging Emulator ID Code Protection Specifications

ID Code				
Control Code	ID Code 1 to ID Code 15	Protection	ID Code Matching Result	Operation
FFh	FFh,…, and FFh (15 bytes are all FFh)	Disabled	N/A	Enable connection with the on-chip debugging emulator.
52h	50h, 72h, 6Fh, 74h, 65h, 63h, and 74h + any 8 bytes	Enabled	N/A	Disable connection with the on-chip debugging emulator, regardless of the codes sent from the on-chip debugging emulator.
Other than above	Other than above	Enabled	Matched	Enable connection with the on-chip debugging emulator.
			Not matched	Continue the ID code wait state.

36.9.2 ROM Code Protection

ROM code protection prevents the flash memory from being read or rewritten by the third party when the parallel programmer is used. Table 36.13 lists the specifications of ROM code protection.
The ROM code in the flash memory is 32-bit data that is allocated in block 0 of the user area.
Figure 36.28 shows the ROM code configuration. Set ROM code in 32-bit units.
When unlocking ROM code protection, erase block 0 of the user area in boot mode or by self-programming.

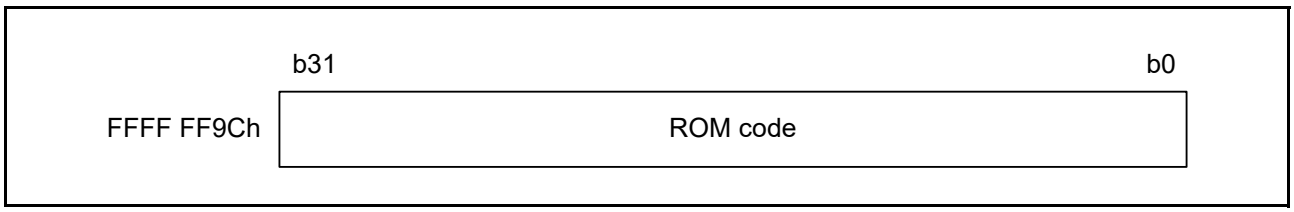


Figure 36.28 ROM Code Configuration

Table 36.13 ROM Code Protection Specification

ROM Code	Protection	Operation When Parallel Programmer is Connected
0000 0000h	Enabled	Disable reading and rewriting of the user area and data area.
0000 0001h	Enabled	Disable reading of the user area and data area.
Other than above	Disabled	Enable reading and rewriting of the user area and data area.

36.10 Communication Protocol

This section describes the protocol used in boot mode. When developing a serial programmer, control with this communication protocol.

36.10.1 State Transition in Boot Mode (SCI)

Figure 36.29 shows the Boot Mode (SCI) State Transition.

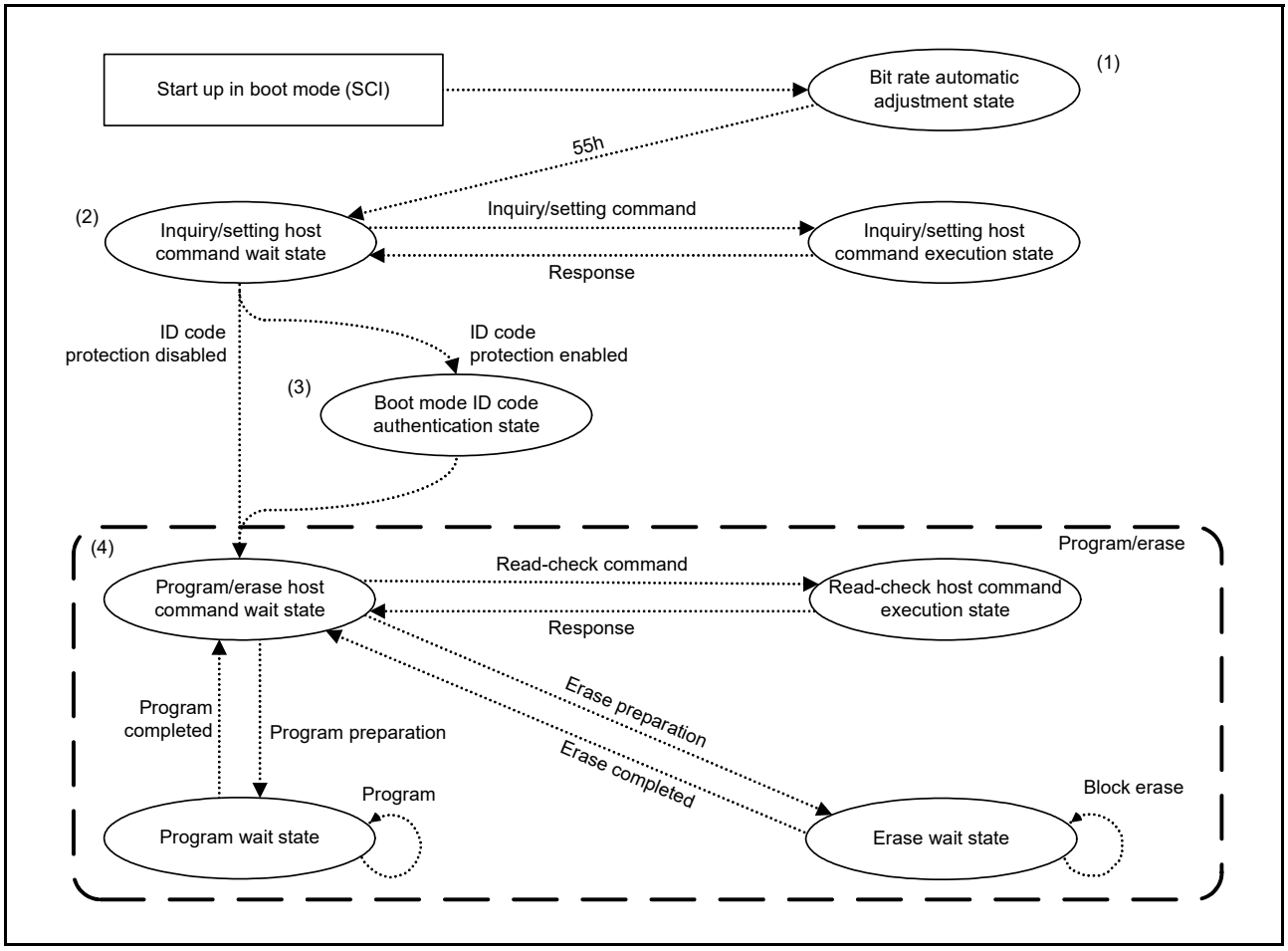


Figure 36.29 Boot Mode (SCI) State Transition

(1) Bit rate automatic adjustment state

In this state, the bit rate is automatically adjusted to 9,600 or 19,200 bps for communication with the host.

When the bit rate adjustment is completed, the MCU sends 00h to the host. After that, when the MCU receives 55h sent from the host, the MCU sends E6h to the host, and enters the inquiry/setting host command wait state.

The host must not send data until 400 ms elapse after a reset of the MCU is released.

(2) Inquiry/setting host command wait state

In this state, the host can make inquiries for the MCU information including block configuration, size, and addresses where the user area and data area are allocated, and select the endian of data and a bit rate.

When the MCU receives the program/erase host state transition command from the host, it determines whether boot mode ID code protection is enabled or disabled. If boot mode ID code protection is disabled, the MCU enters the inquiry/setting host command wait state. If boot mode ID code protection is enabled, the MCU enters the boot mode ID code authentication state.

Refer to section 36.10.5, Inquiry Commands and section 36.10.6, Setting Commands for details on inquiry/setting commands.

(3) Boot mode ID code authentication state
In this state, the MCU accepts the ID code authentication command.
If boot mode ID codes do not match, the MCU remains in the boot mode ID code authentication state.
Refer to section 36.9.1.1, Boot Mode ID Code Protection for details on boot mode ID code protection. Refer to section 36.10.7, ID Code Authentication Command for details on the ID code authentication command.

(4) Program/erase state
In this state, the MCU executes program/erase or read-check commands according to commands sent from the host.
Refer to section 36.10.8, Program/Erase Commands for details on program/erase commands. Refer to section 36.10.9, Read-Check Commands for details on read-check commands.

36.10.2 Command and Response Configuration

The communication protocol is composed of a “Command” sent from the host to the MCU and a “Response” sent from the MCU to the host. Commands include 1-byte commands and multiple-byte commands. Responses include 1-byte responses, multiple-byte responses, and error responses.
A multiple-byte command and multiple-byte response have “Size” for informing the number of transmit/receive data bytes and “SUM” for detecting communication errors.
“Size” indicates the number of transmit/receive data bytes excluding Command code (the first byte), Size, and SUM.
“SUM” indicates byte data that is calculated so the total bytes of Command or Response becomes 00h.
The flash memory addresses for reading are used as the following addresses: the program address specified in the program command, the block start address specified in the block erase command, and the AW start and end addresses specified in the access window information program command, and the AW start and end addresses received in the access window read command.

36.10.3 Response to Undefined Commands

When the MCU receives an undefined command, it sends a command error as a response. The contents of the response are shown below. “Command code” in the error response stores the first byte of the command sent from the MCU.

Error response	80h	Command code

36.10.4 Boot Mode Status Inquiry

This command is used to check the current state and the previous error of the boot program.
The MCU returns a code from Table 36.14 and Table 36.15 as the current state and the previous error.
The boot mode status inquiry command can be used in the inquiry/setting host command wait state and program/erase state.

Command	4Fh				
Response	5Fh	Size	State	Error	SUM

Size (1 byte): Total bytes of “State” and “Error” (the value is always 02h)
State (1 byte): MCU's current state (see Table 36.14)
Error (1 byte): Information about the error occurred in the MCU (see Table 36.15)
SUM (1 byte): Value that is calculated so the sum of response data is 00h

Table 36.14 Information Regarding the States

Code	State*1	Description
11h	Inquiry/setting host command wait state	Device selection wait state
12h/13h		Operating frequency selection wait state
1Fh		Program/erase state transition command wait state
31h	Boot mode ID code authentication state	The user area and data area are being erased
3Fh	Program/erase host command wait state	Program/erase command wait state
4Fh		Program data reception wait state
5Fh		Block erase specification wait state

Note 1. Refer to Figure 36.29 for details on the state transitions.

Table 36.15 Error Information

Code	Description
00h	No error
11h	SUM error
21h	Device code error
24h	Bit rate selection error
29h	Block start address error
2Ah	Address error
2Bh	Data length error
51h	Erase error
52h	Not blank (blank check error)
53h	Program error
61h	ID code do not match
63h	ID code do not match and erase error
80h	Command error
FFh	Bit rate automatic adjustment error

36.10.5 Inquiry Commands

Inquiry commands are used to obtain necessary information for sending setting commands, program/erase commands, and read-check commands. Table 36.16 lists the inquiry commands. These commands can only be used in the inquiry/setting host command wait state.

Table 36.16 Inquiry Commands

Command	Description
Supported device inquiry	Inquiry for the device code and series name
Data area availability inquiry	Inquiry for the availability of the data area
User area information inquiry	Inquiry for the number of user areas, and the start and end addresses of the user area
Data area information inquiry	Inquiry for the number of data areas, and the start and end addresses of the data area
Block information inquiry	Inquiry for the start and end addresses of the user areas and data areas, the block size, and the number of blocks

36.10.5.1 Supported Device Inquiry

This command is used to obtain the device information for identifying the endian of developed software.
After the MCU receives this command, it sends the device information when developed software uses little endian data and the device information when developed software uses big endian data in this order.

Command	20h			
Response	30h	Size	Number of devices	
	Number of characters	Device code for little endian		Series name for little endian
	Number of characters	Device code for big endian		Series name for big endian
	SUM			

Size (1 byte): Total bytes of Number of Devices, Characters, Device code, and Series name
Number of devices (1 byte): Number of endian types of program data (the value is always 02h)
Number of characters (1 byte): Number of characters for the device code and device name
Device code (4 bytes): Identification code indicating the endian of developed software
Series name (n bytes): Little endian/big endian (ASCII code) of the series name of the MCU
SUM (1 byte): Value that is calculated so the sum of response data is 00h

36.10.5.2 Data Area Availability Inquiry

When the MCU receives this command, it sends the result indicating the data area is available, area protection can be used, and data area program command is available.

Command	2Ah			
Response	3Ah	Size	Availability	SUM

Size (1 byte): Number of characters of Availability (the value is always 01h)
Availability (1 byte): Availability of the data area (the value is always 1Dh)
1Dh represents the data area is available, area protection can be used, data area program command is available.
SUM (1 byte): Value that is calculated so the sum of response data is 00h (the value is always A8h)

36.10.5.3 User Area Information Inquiry

When the MCU receives this command, it sends the number of user areas and addresses.

Command	25h		
Response	35h	Size	Number of areas
	Area start address		
	Area end address		
	SUM		

Size (1 byte): Total bytes of Number of areas, Area start address, and Area end address (the value is always 09h)
Number of areas (1 byte): Number of user areas (the value is always 01h)
Area start address (4 bytes): Start address of the user area
Area end address (4 bytes): End address of the user area
SUM (1 byte): Value that is calculated so the sum of the response data is 00h

36.10.5.4 Data Area Information Inquiry

When the MCU receives this command, it sends the number of data areas and addresses.

Command	2Bh		
Response	3Bh	Size	Number of areas
	Area start address		
	Area end address		
	SUM		

Size (1 byte): Total bytes of data of Number of areas, Area start address, and Area end address (the value is always 09h)
Number of areas (1 byte): Number of areas in the data area (the value is always 01h)
Area start address (4 bytes): Start address of the data area (the value is always 0010 0000h)
Area end address (4 bytes): End address of the data area (the value is always 0010 1FFFh)
SUM (1 byte): Value that is calculated so the sum of the response data is 00h (the value is always 7Dh)

36.10.5.5 Block Information Inquiry

When the MCU receives this command, it sends the start address, the size of one block, and the number of blocks in the user area and data area.

Command	26h		
Response	36h	Size	DDh
	Start address of the user area		
	Block size of one block for the user area		
	Number of blocks of the user area		
	Start address of the data area		
	Block size of one block for the data area		
	Number of blocks of the data area		
	SUM		

Size (2 bytes): Total bytes of data from DDh to Number of blocks of the data area (the value is always 00 19h)
Start address of the user area (4 bytes): Start address of the user area
Block size of one block for the user area (4 bytes): Memory size of one block (the value is always 00 00 08 00h)
Number of blocks of the user area (4 bytes): Number of blocks in the user area
Start address of the data area (4 bytes): Start address of the data area (the value is always 00 10 00 00h)
Block size of one block for the data area (4 bytes): Memory size of one block (the value is always 00 00 04 00h)
Number of blocks of the data area (4 bytes): Number of blocks in the data area (the value is always 00 00 00 08h)
SUM (1 byte): Value that is calculated so the sum of response data is 00h

36.10.6 Setting Commands

Setting commands are used to configure the settings necessary to execute program/erase commands in the MCU.
Table 36.17 lists Setting Commands. These commands can be used only in the inquiry/setting host command wait state.

Table 36.17 Setting Commands

Command	Function
Device select	Select a device code.
Operating frequency select	Change the bit rate for communication.
Program/erase host command wait state transition	Enter the program/erase host command wait state or boot mode ID code authentication state.

36.10.6.1 Device Select

This command is used to specify the endian of developed software. Select a device code from among the device codes obtained in the response to the support device inquiry command.
If the received device code matches the supported device, the MCU sends a response (46h).
If the device is not supported or the SUM of the received command does not match, the MCU sends an error response.

Command	10h	Size	Device code	SUM

Size (1 byte): Number of characters of the device code (the value is always 04h)
Device code (4 bytes): Identification code indicating the device
(code in the response to the support device inquiry command)
SUM (1 byte): Value that is calculated so the sum of command data is 00h

Response	46h

Error response	90h	Error

Error (1 byte): Error code
11h: SUM error
21h: Device code error

36.10.6.2 Operating Frequency Select

This command is used to specify the operating frequency of the MCU and a bit rate for communication with the flash memory programmer. The bit rate selected in this command should be set to a value with error of less than 4% compared to the bit rate obtained by dividing 32 or 8 MHz that corresponds to the operating voltage.
If the specified settings can be supported, the MCU sends a response (06h). If the bit rate error is 4% or more or the SUM of the received command does not match, the MCU sends an error response.

After the host receives a response, wait for at least a 1-bit period at the old bit rate, and send communication confirmation data at the new bit rate.
If the MCU successfully receives communication confirmation data, the MCU sends a response (06h). If the MCU fails to receive the communication confirmation data, the MCU sends an error response.

Command	3Fh	Size	Bit rate	Dummy data
	Number of clocks	Multiplier 1	Multiplier 2	
	SUM			

Size (1 byte): Total bytes of data of Bit rate, Dummy data, Number of clocks, and Multiplier (the value is always 07h)
Bit rate (2 bytes): New bit rate
The value is calculated by dividing the bit rate by 100 (Example: Set 00C0h for 19200 bps)
Dummy data (2 bytes): The value should always be set to 0000h
Number of clocks (1 byte): Types of clocks for multiplier setting (the value is always 02h)
Multiplier 1 (1 byte): Multiplier of the system clock (ICLK) (the value is always 01h)
Multiplier 2 (1 byte): Multiplier of the peripheral module clock (PCLK) (the value is always 01h)
SUM (1 byte): Value that is calculated so the sum of command data is 00h

Response	06h	

Error response	BFh	Error

Error (1 byte): Error code
11h: SUM error
24h: Bit rate selection error

Communication confirmation	06h

Response	06h

Error response	FFh

- Bit rate selection error
  A bit rate selection error occurs when the bit rate specified with the operating frequency select command cannot be set to a value with error of less than 4%. When the new bit rate specified with the operating frequency select command is B, and 32 (MHz) or 8 (MHz) corresponding to the operating voltage is Pφ, the bit rate error is calculated by the following formula:

$$\text{Error}\,[\%] = \left(\frac{P\varphi \times 10^6}{B \times 32 \times N} - 1\right) \times 100$$

$$N = \text{INT}\left(\frac{P\varphi \times 10^6}{B \times 32}\right)$$

Pφ: 32 (MHz) when the operating voltage is 3.0 V or above
8 (MHz) when the operating voltage is below 3.0 V
B: New bit rate (bps)
N: Ratio between Pφ and the new bit rate multiplied by 32 (however, $1 \leq N \leq 256$)

36.10.6.3 Program/Erase Host Command Wait State Transition

This command is used for the transition from the inquiry/setting host command wait state to the program/erase host command wait state.
When the MCU receives this command, it determines whether boot mode ID code protection is enabled or disabled.

When boot mode ID code protection is disabled, all blocks in the user area and data area are erased.
When all blocks are successfully erased, the MCU sends a response (06h) and enters the program/erase host command wait state. If not all blocks are successfully erased, the MCU sends an error response.
When boot mode ID code protection is enabled, the MCU sends a response (16h) and enters boot mode ID code authentication state.

Command	40h

Response	ACK

ACK (1 byte): ACK code
06h: ID code protection is disabled.
16h: ID code protection is enabled.

Error response	C0h	Error

Error (1 byte): Error code
51h: Erase error

36.10.7 ID Code Authentication Command

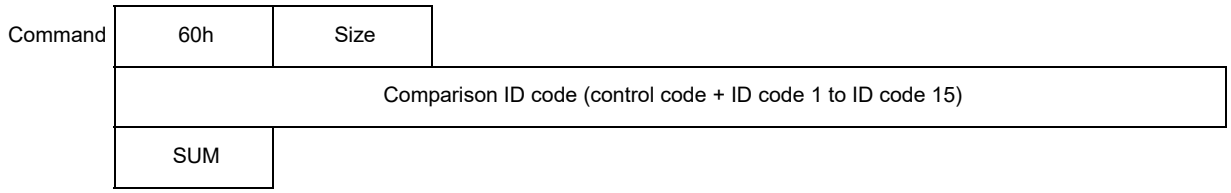
This command is used for ID code authentication when boot mode ID code protection is enabled.
Table 36.18 lists ID code authentication command. This command can be used only in the boot mode ID code authentication state.

Table 36.18 ID Code Authentication Command

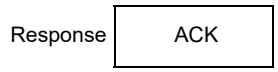
Command	Function
ID code check	Compare the 16-byte code sent from the host and ID code.

36.10.7.1 ID Code Check

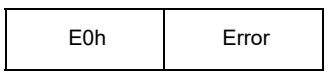
This command is used to unlock boot mode ID code protection.
The comparison ID code specified with the command should be set to the same value as the control code and ID code 1 to ID code 15.
If the comparison ID code sent from the host matches the ID code programmed in the user area, the MCU sends a response (06h) and enters program/erase host command wait state.
If the codes do not match or the SUM of the received command does not match, the MCU sends an error response.
When the ID codes do not match three times consecutively while the control code is 45h, all blocks in the user area and data area are erased. If an error occurs during erasure, the MCU sends an error response.
Also, even if all blocks are successfully erased, the MCU sends an error response and continues the boot mode ID code state. Reset the MCU to enter the program/erase host command wait state.



Size (1 byte): Number of bytes of ID codes (the value is always 10h)
ID code (16 bytes): Control code (1 byte) + ID code 1 to ID code 15 (15 bytes)
SUM (1 byte): Value that is calculated so the sum of the command data is 00h



ACK (1 byte): ACK code
06h: The MCU enters the program/erase host command wait state.



Error (1 byte): Error code
11h: SUM error
61h: ID codes do not match
63h: ID codes do not match and erase error

36.10.8 Program/Erase Commands

Program/erase commands are used to program or erase the user area or data area based on the response to inquiry commands. Table 36.19 lists commands used in the program/erase command wait state, program wait state, and erase wait state. Table 36.20 lists commands that can be accepted in each state.
When a command that cannot be accepted is received in the state listed in Table 36.20, the MCU sends a command error response.

Table 36.19 Program/Erase Commands

Command	Function
User/data area program preparation	Select the user area or data area to program, and enter the program wait state.
Program	Program the specified data to the selected area in the user area or data area. Or enter the program/erase host command wait state (end of program).
Data area program	Program the specified-size data to the selected area in the data area. Or enter the program/erase host command wait state (end of program).
Erase preparation	Enter the erase wait state.
Block erase	Erase the selected block, or enter the program/erase host command wait state (end of erase).

Table 36.20 Acceptable Commands for Each State

State	Acceptable Command
Program/erase host command wait state	User/data area program preparation command, erase preparation command
Program wait state	Program command, data area program command
Erase wait state	Block erase command

36.10.8.1 User/Data Area Program Preparation

This command is used to prepare for accepting the program command and the data area program command.
When the MCU receives this command, it recognizes that an instruction to prepare for the program command is issued from the host. Then, the MCU enters the program wait state, where only the program command to the user area or data area can be accepted, and sends a response (06h).

Command	43h
Response	06h

36.10.8.2 Program

This command is used to program the specified data to the user area or data area. Set the low-order 8 bits to 0 for the program address selected in this command. When the data length is shorter than 256 bytes, the data cannot be programmed. Fill the gaps with FFh.
When the program from the selected address is successfully completed, the MCU sends a response (06h). If the SUM of the received command does not match or an error occurs during a program operation, the MCU sends an error response.

To enter the program/erase host command wait state after the program operation ends, send 50h FFh FFh FFh FFh B4h from the host. The MCU sends a response (06h), and enters the program/erase host command wait state.

Command	50h	Program address	
	Program data		
	SUM		

Program address (4 bytes): Address for program destination
Set the low-order 8 bits to 0
Set FFFF FFFFh for end of program
Program data (n bytes): Program data (n = 256 in boot mode, 0 for end of program)
When the program is less than n bytes, set FFh for the missing data.
No program data for the end of program
SUM (1 byte): Value that is calculated so the sum of command data is 00h

Response	06h	

Error response	D0h	Error

Error (1 byte): Error code
11h: SUM error
2Ah: Address error (the address is not in the selected area.)
53h: Program error (the data or program data cannot be programmed.)

36.10.8.3 Data Area Program

This command is used to program the specified data to the data area. Set the low-order 2 bits to 0 for the program address selected in this command. When the data length is shorter than 4 bytes, the data cannot be programmed. Fill the gaps with FFh.
When the program from the selected address is successfully completed, the MCU sends a response (06h). If the SUM of the received command does not match or an error occurs during a program operation, the MCU sends an error response.

To enter the program/erase host command wait state after the program operation ends, send 51h FFh FFh FFh FFh B4h from the host. The MCU sends a response (06h), and enters the program/erase host command wait state.

Command	51h	Program address	Program data length
	Program data		
	SUM		

Program address (4 bytes): Address for program destination
Set the low-order 2 bits of the selected address to 0

Set FFFF FFFFh for end of data area program

Program data length (1 byte): Size of program data
Set 4-byte data
Set 00h for end of data area program

Program data (n bytes): Program data for the data area (n = program data length, 0 for end of program)
Set data of the program data length
When the program is less than n bytes, set FFh for the missing data.
No program data for the end of data area program

SUM (1 byte): Value that is calculated so the sum of command data is 00h

Response	06h

Error response	D1h	Error

Error (1 byte): Error code
11h: SUM error
2Ah: Address error (the address is not in the selected area.)
2Bh: Program data length error
53h: Program error (the data or program data cannot be programmed.)

36.10.8.4 Erase Preparation

This command is used to prepare for accepting the block erase command. When the MCU receives this command, it recognizes that an instruction to prepare for the erase command is issued from the host. Then, the MCU enters the erase wait state, where only the block erase command can be accepted, and sends a response (06h).

Command	48h
Response	06h

36.10.8.5 Block Erase

This command is used to erase the selected block in the user area or data area. Specify the block start address selected in the command by calculating the address based on the response to the block information inquiry command.
When the selected block in the block start address is successfully erased, the MCU sends an error response (06h). If the SUM of the received command does not match or an error occurs during an erase operation, the MCU sends an error response.

To enter the program/erase host command wait state after the erase operation ends, send 59h 04h FFh FFh FFh FFh A7h from the host. The MCU enters the program/erase host command wait state and sends a response (06h).

Command	59h	Size
	Block start address	
Response	SUM	

Size (1 byte): Total bytes of Block start address (the value is always 04h)
Block start address (4 bytes): Start address of the block that is erased
Set FFFF FFFFh for end of erase
SUM (1 byte): Value that is calculated so the sum of response data is 00h

Response	06h	
Error response	D9h	Error

Error (1 byte): Error code
11h: SUM error
29h: Block start address error
51h: Erase error (the selected block cannot be erased)

36.10.9 Read-Check Commands

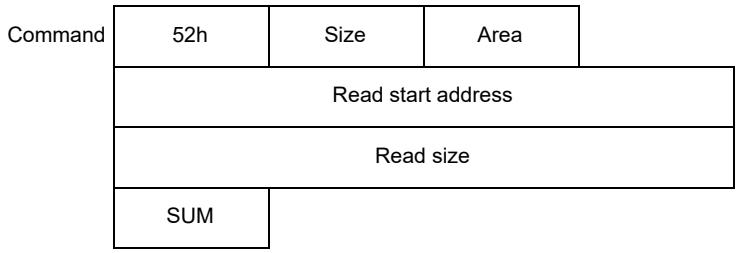
Read-check commands are used to read data or check whether data is programmed in the user area or data area in the MCU based on the response to inquiry commands.
Table 36.21 lists read-check commands used in the program/erase host command wait state.

Table 36.21 Read-Check Commands

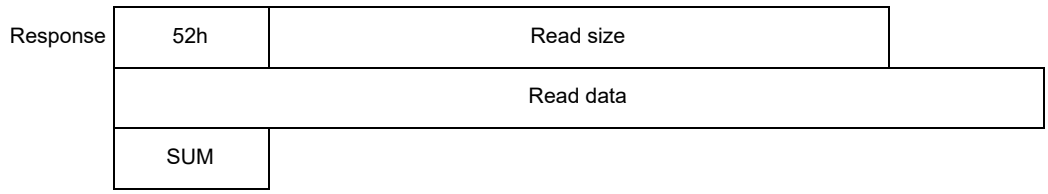
Command	Function
Memory read	Read data from the user area or data area.
User area checksum	Obtain the checksum of the entire user area.
Data area checksum	Obtain the checksum of the entire data area.
User area blank check	Check whether data is programmed in the user area.
Data area blank check	Check whether data is programmed in the data area.
Access window information program	Set the access window.
Access window read	Read the settings of the access window.

36.10.9.1 Memory Read

This command is used to read data programmed in the user area or data area. For a read start address selected in the command, set a value within the range from the area start address to the area end address received in the response to the user area information inquiry command or data area information inquiry command.
For a read size selected in the command, set a value so the sum of the read start address and the read size is within the range from the area start address to the area end address received in the response to the user area information inquiry command or the data area information inquiry command.
When the MCU performs a read successfully, it sends data of the specified range. If the SUM of the received command does not match or the MCU fails to perform a read successfully, it sends an error response.



Size (1 byte): Total bytes for Read start address and Read size
Area (1 byte): Area that is read
01h: User area or data area
Read start address (4 bytes): Start address of the area that is read
Read size (4 bytes): Size of data that is read (in bytes)
SUM (1 byte): Value that is calculated so the sum of response data is 00h



Read size (4 bytes): Size of Data that is read (in bytes)
Read data (n bytes): Data read from the selected address (n = read size)
SUM (1 byte): Value that is calculated so the sum of response data is 00h

Error response	D2h	Error

Error (1 byte): Error code
- 11h: SUM error
- 2Ah: Address error
  - A value other than 01h is set for the “Area” field.
  - The read start address is not in the selected area.
- 2Bh: Size error
  - The read size is set to 0000 0000h.
  - The read size exceeds the area size.
  - The address calculated from the read start address and read size is not in the selected area.

36.10.9.2 User Area Checksum

This command used to obtain the checksum of the entire user area. When the MCU receives this command, it adds data from the start address to the end address in bytes, and sends the calculated result (checksum) as a response.

Command	4Bh	

Response	5Bh	Size
	User area checksum	
	SUM	

Size (1 byte): Number of bytes for checksum of the user area (the value is always 04h)
User area checksum (4 bytes): Calculated result of the data in the user area in bytes
SUM (1 byte): Value that is calculated so the sum of response data is 00h

36.10.9.3 Data Area Checksum

This command used to obtain the checksum of the entire data area. When the MCU receives this command, it adds data from the start address to the end address in bytes, and sends the calculated result (checksum) as a response.

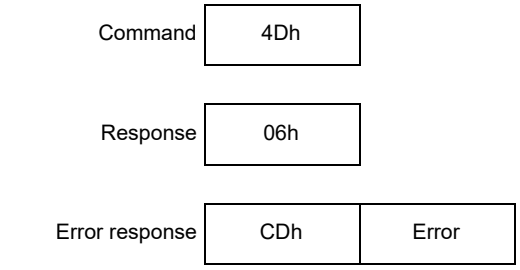
Command	61h	

Response	71h	Size
	Data area checksum	
	SUM	

Size (1 byte): Number of bytes for checksum of the data area (the value is always 04h)
Data area checksum (4 bytes): Calculated result of the data in the data area in bytes
SUM (1 byte): Value that is calculated so the sum of response data is 00h

36.10.9.4 User Area Blank Check

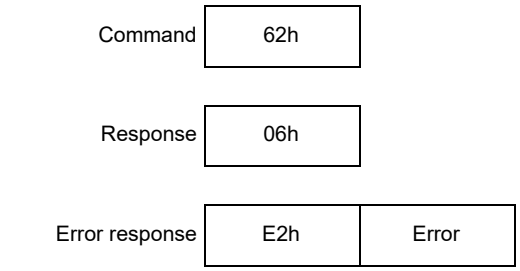
This command is used to check whether data is programmed in the user area.
When the MCU receives this command, it checks whether there is data in the entire user area. If there is no programmed data, the MCU sends a response (06h). If there is at least 1 byte of data, the MCU sends an error response.



Error (1 byte): Error code
52h: Not blank

36.10.9.5 Data Area Blank Check

This command is used to check whether data is programmed in the user area.
When the MCU receives this command, it checks whether there is programmed data in the entire user area. If there is no programmed data, the MCU sends a response (06h). If there is at least 1 byte of programmed data, the MCU sends an error response.



Error (1 byte): Error code
52h: Not blank

36.10.9.6 Access Window Information Program

This command is used to set the access window used for area protection. For the access window start address selected in the command, set the start address of the start block. For the access window end address, set the end address of the end block.

When the specified access window settings are successfully completed, the MCU sends a response (06h). If the SUM of the received command does not match or an error occurs during the access window settings, the MCU sends an error response.

For details on the access window, see section 36.6, Area Protection.

Command	74h	05h	Access window	
	Access window start address LH	Access window start address HL	Access window end address LH	Access window end address HL
	SUM			

Access window (1 byte): Select the access window or clear the access window settings
Set 00h to select the access window
Set FFh to clear the access window settings

Access window start address LH (1 byte): Start address of the access window (A15 to A8)
Set A15 to A8 of the block start address.
Set FFh to clear the access window settings

Access window start address HL (1 byte): Start address of the access window (A23 to A16)
Set A23 to A16 of the block start address.
Set FFh to clear the access window settings

Access window end address LH (1 byte): End address of the access window (A15 to A8)
Set A15 to A8 of the block end address.
Set FFh to clear the access window settings

Access window end address HL (1 byte): End address of the access window (A23 to A16)
Set A23 to A16 of the block end address.
Set FFh to clear the access window settings

SUM (1 byte): Value that is calculated so the sum of response data is 00h

Response	06h

Error response	F4h	Error

Error (1 byte): Error code
11h: SUM error
2Ah: Address error (address is not in the selected area)
53h: Program error (access window cannot be set)

36.10.9.7 Access Window Read

This command is used to check the set range of the access window.
When the MCU successfully obtains the access window range, the MCU sends the access window start address and end address that it read. If the SUM of the received command does not match, the MCU sends an error response.

Command	73h	01h	FFh	8Dh

Response	73h	05h		
	Access window start address LH	Access window start address HL	Access window end address LH	Access window end address HL
	FFh			
	SUM			

Access window start address LH (1 byte): Start address of the access window range (A15 to A8)
Access window start address HL (1 byte): Start address of the access window range (A23 to A16)
Access window end address LH (1 byte): End address of the access window range (A15 to A8)
Access window end address HL (1 byte): End address of the access window range (A23 to A16)
SUM (1 byte): Value that is calculated so the sum of response data is 00h

Error response	F3h	Error

Error (1 byte): Error code
11h: SUM error

36.11 Serial Programmer Operation in Boot Mode (SCI)

The following describes the procedure for the serial programmer to program/erase the user area and data area in boot mode (SCI).

1. Automatically adjust the bit rate
2. Receive the MCU information*1
3. Select the device and change the bit rate
4. Enter the program/erase host command wait state
5. Unlock boot mode ID code protection
6. Erase the user area and data area*2, *3
7. Program the user area and data area*2, *3
8. Check data in the user area*2
9. Check data in the data area*2
10. Set the access window in the user area
11. Reset the MCU

Note 1. If the necessary information has been already received, step 2 can be skipped.
Note 2. Any step from 6 to 10 can be skipped, and their order can be changed.
Note 3. When a timeout occurs or invalid response data is received, stop the operation and perform step 11 (reset the MCU).

Refer to section 36.10.5, Inquiry Commands, section 36.10.6, Setting Commands, section 36.10.7, ID Code Authentication Command, section 36.10.8, Program/Erase Commands, and section 36.10.9, Read-Check Commands for details on the commands used in the above steps 2 to 10.

36.11.1 Bit Rate Automatic Adjustment Procedure

The MCU measures the low width of data 00h that is sent from the serial programmer at 9,600 or 19,200 bps to automatically adjust the bit rate.

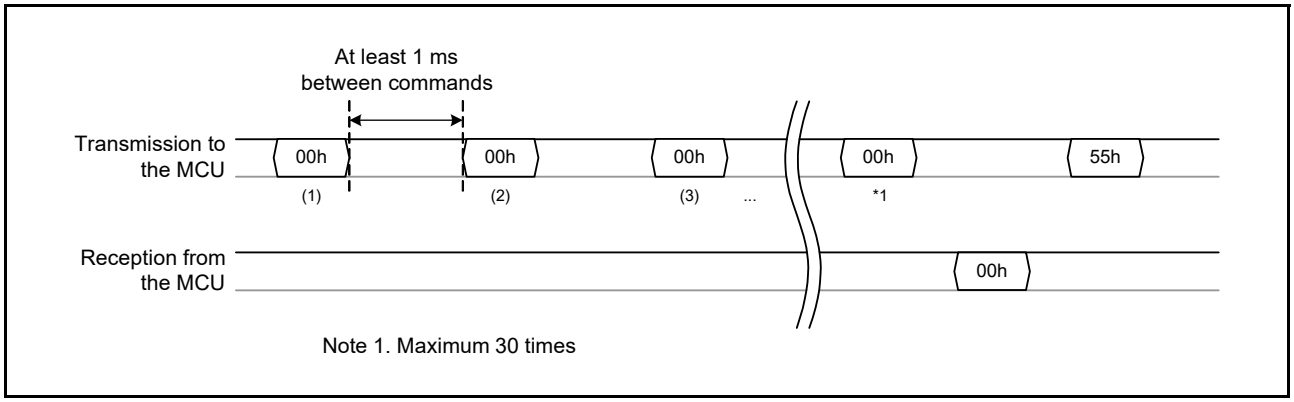


Figure 36.30 Transmit/Receive Data for Bit Rate Automatic Adjustment

After starting up in boot mode, wait for at least 400 ms and then send 00h to the MCU from the serial programmer. When the bit rate adjustment is completed, the MCU sends 00h to the programmer. When the programmer receives 00h, send 55h to the MCU from the programmer. When the programmer can not receive 00h, wait for at least 1 ms and send 00h to the MCU again. When the programmer fails to receive 00h even if it send 00h 30 times, restart the MCU in boot mode and adjust the bit rate again.

When the MCU receives 55h, the MCU sends E6h and enters the inquiry/setting command wait state. If the MCU fails to receive 55h, the MCU sends FFh. When the programmer receives FFh, restart the MCU in boot mode, and adjust the bit rate again.

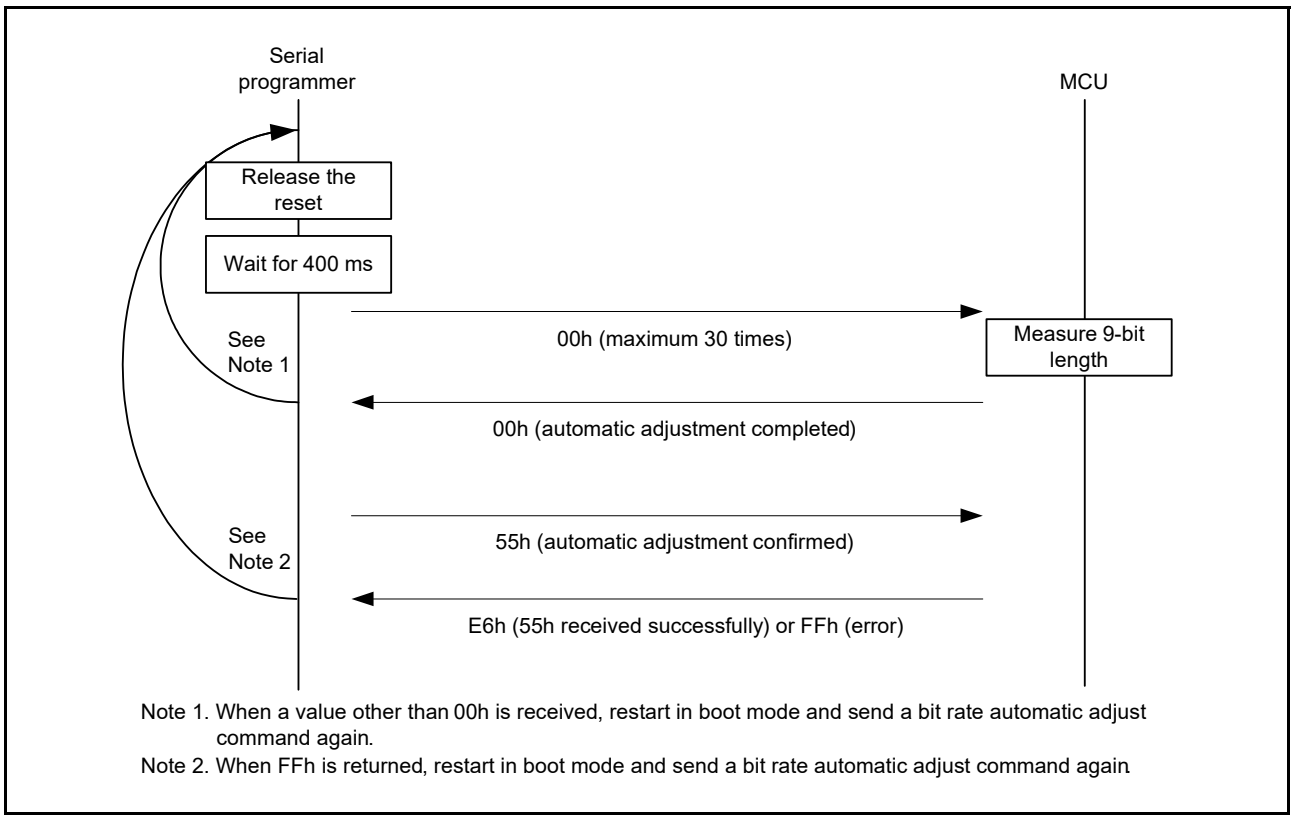


Figure 36.31 Bit Rate Automatic Adjustment Procedure

36.11.2 Procedure to Receive the MCU Information

Send inquiry commands, and receive the information necessary to send setting commands, program/erase commands, and read-check commands.

(1) Send a support device inquiry command (20h) to check which device to connect. The MCU returns the device code and series name.
(2) Send a user area information inquiry command (25h) to check the start and end addresses of the user area. The MCU returns the start and end addresses of the user area.
(3) Send a block information inquiry command (26h) to check the block configuration. The MCU returns the start address, the size of one block, and the number of blocks for the user area and data area.
(4) Send a data area information inquiry command (2Bh) to check the start and end addresses of the data area. The MCU returns the start and end addresses of the data area.

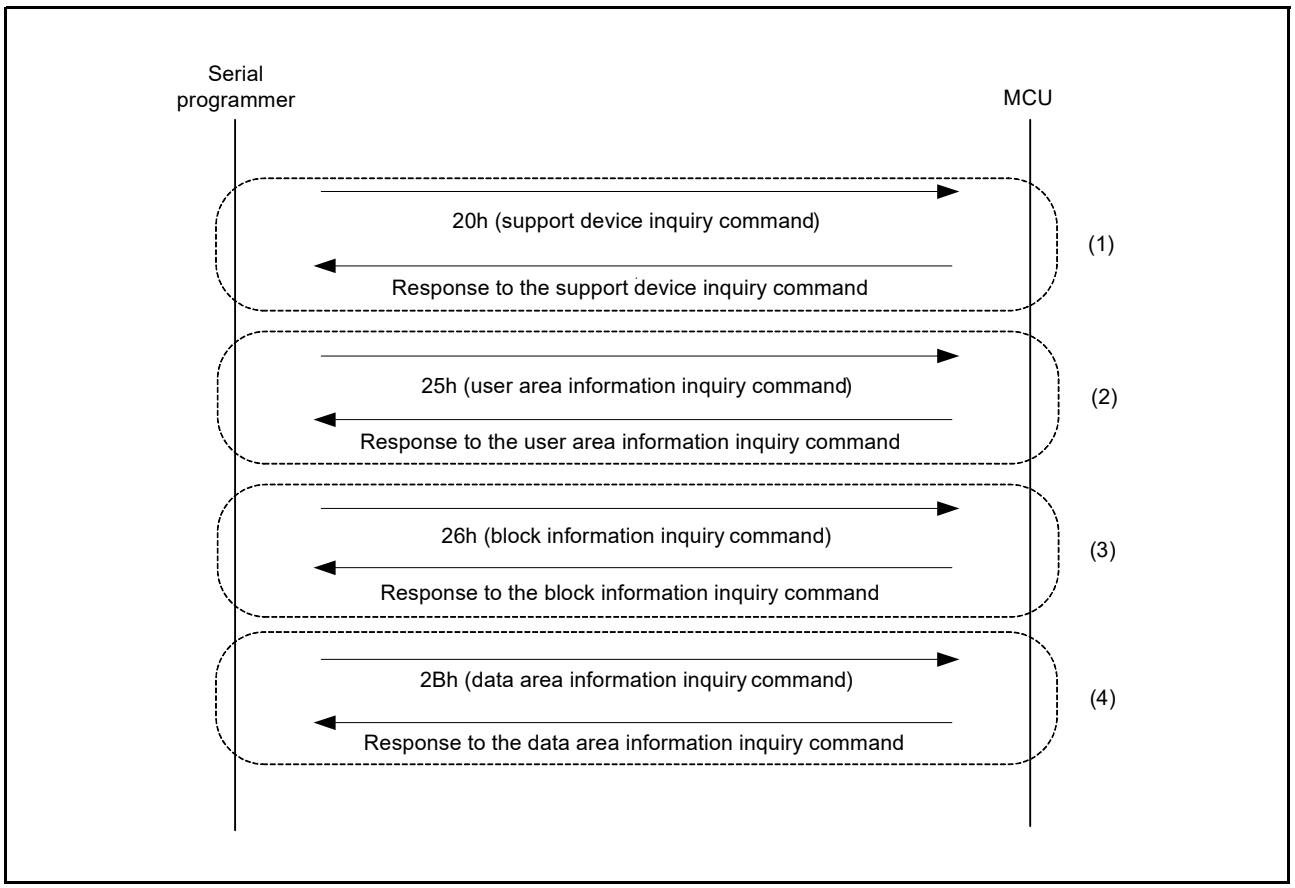


Figure 36.32 Procedure to Receive the MCU Information

36.11.3 Procedure to Select the Device and Change the Bit Rate

Select the device to connect with the serial programmer and change the bit rate for communication.

(1) Send the device select command (10h). Select the device code according to the endian of developed software.
(2) Send the operating frequency select command (3Fh) to change the communication bit rate from 9,600 or 19,200 bps.

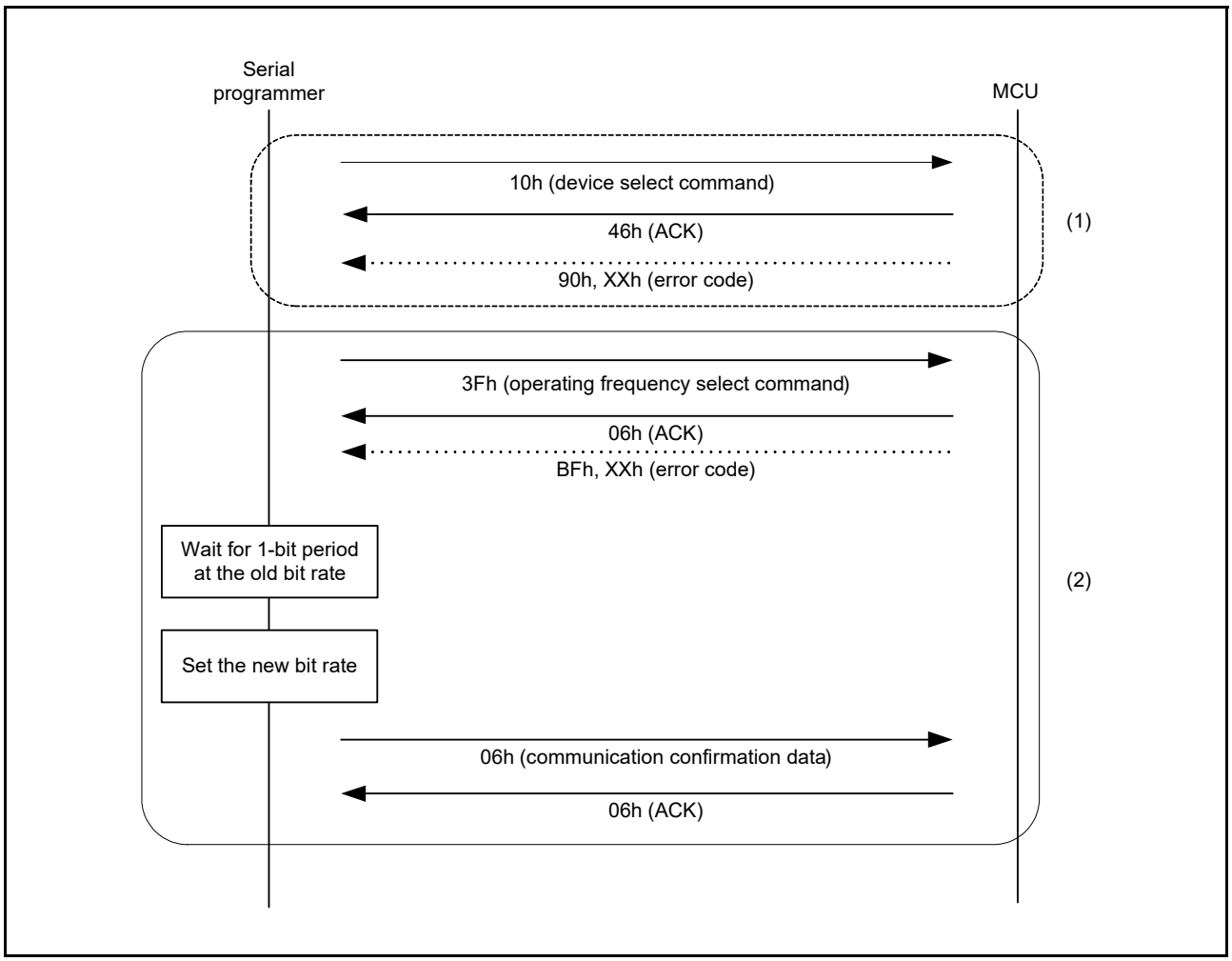


Figure 36.33 Procedure to Select the Device and Change the Bit Rate

36.11.4 Transition to the Program/Erase Host Command Wait State

Send the program/erase host command wait state transition command to perform program/erase operations. The MCU sends a response according to whether boot mode ID code protection is enabled or disabled.

(1) When boot mode ID code protection is disabled, the MCU sends a response (06h), and enters the program/erase host command wait state. Use the serial programmer to start from the operation described in section 36.11.6, Erase the User Area and Data Area.

(2) When the boot mode ID code protection is enabled, the MCU sends a response (16h), and enters the ID code authentication wait state. Use the serial programmer to start from the operation described in section 36.11.5, Unlock Boot Mode ID Code Protection.

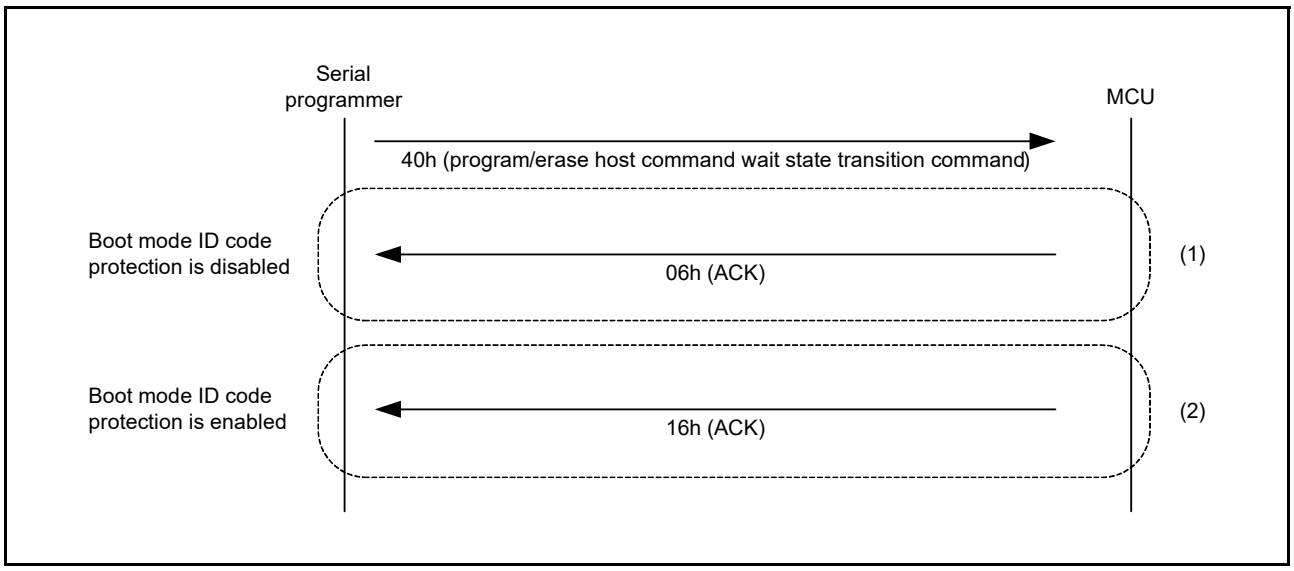


Figure 36.34 Procedure to Enter the Program/Erase Host Command Wait State

36.11.5 Unlock Boot Mode ID Code Protection

Send the ID code check command to unlock boot mode ID code protection.

(1) When ID codes match, the MCU enters the program/erase host command wait state. Data in the user area and data area is not erased. Use the serial programmer to start from the operation described in section 36.11.6, Erase the User Area and Data Area.

(2) If ID codes do not match consecutively, the MCU remains in the boot mode ID code authentication state. Reset the MCU, and then use the serial programmer to start again from section 36.11.1, Bit Rate Automatic Adjustment Procedure.

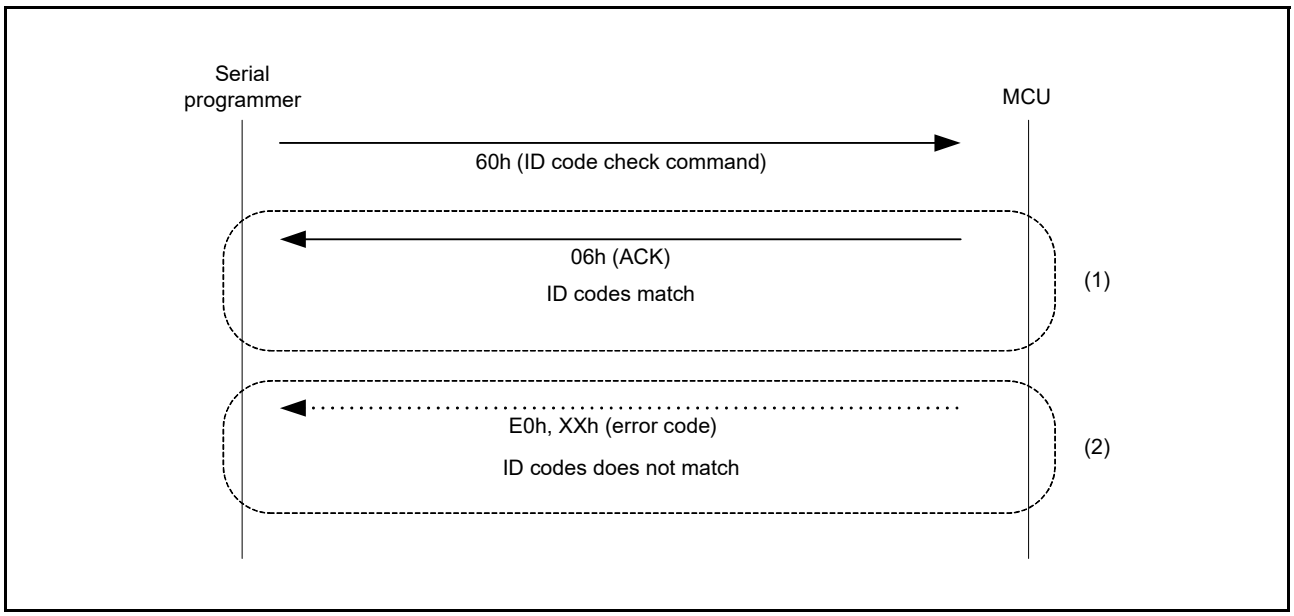


Figure 36.35 Procedure to Unlock ID Code Protection

36.11.6 Erase the User Area and Data Area

Erase blocks that are programmed in the user area and data area to program a user program.

(1) Send an erase preparation command (48h).
(2) Send a block erase command (59h).
(3) To place the MCU in the program/erase host command wait state, send a block erase command for end of erase (59h 04h FFh FFh FFh FFh A7h).

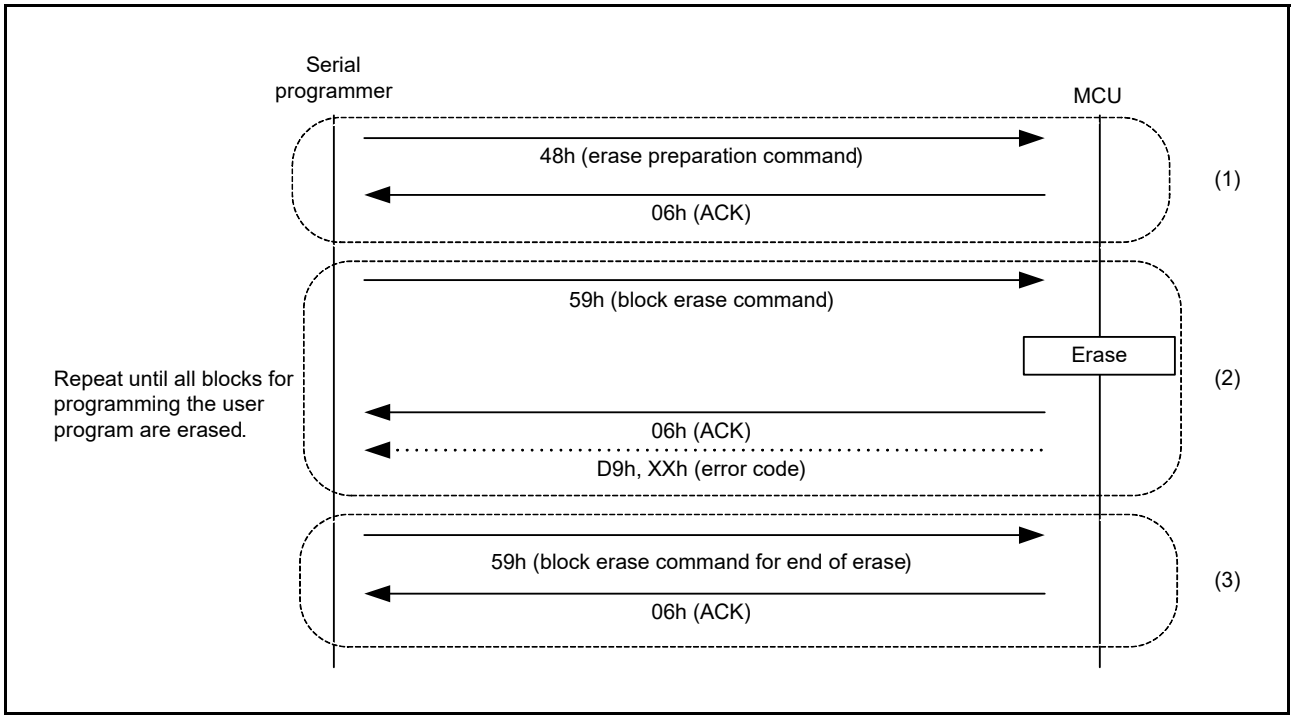


Figure 36.36 Procedure to Erase the User Area and Data Area

36.11.7 Program the User Area and Data Area

Program a user program in the user area and data area.

(1) Send the user/data area program preparation command (43h).
(2) Send the program command (50h) or data area program (51h).
(3) To place the MCU in the program/erase host command wait state, send the program command (50h FFh FFh FFh FFh B4h) or data area program command (51h FFh FFh FFh FFh 00h B3h) for end of program.

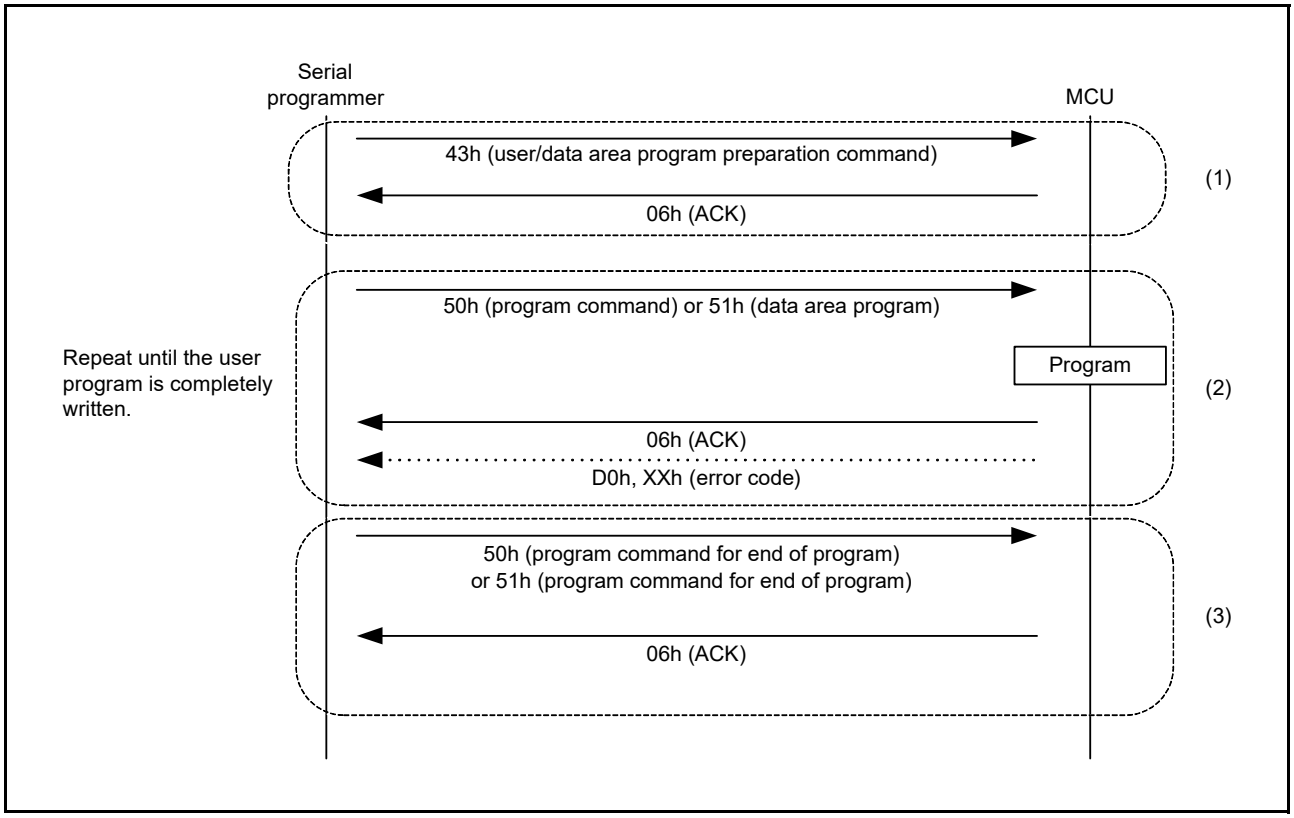


Figure 36.37 Procedure to Program the User Area and Data Area

36.11.8 Check Data in the User Area

Read and check, checksum, and blank check the user area to check the programmed data in the user area.

(1) The read and check operation is used to read data in the user area and compare the read data with the programmed data to check if the program operation is performed successfully. Send a memory read command (52h) to read data in the user area.
(2) Send the user area checksum command (4Bh) to check program data using the checksum of user area.
(3) Send a user area blank check command (4Dh) to check if the user area has data.

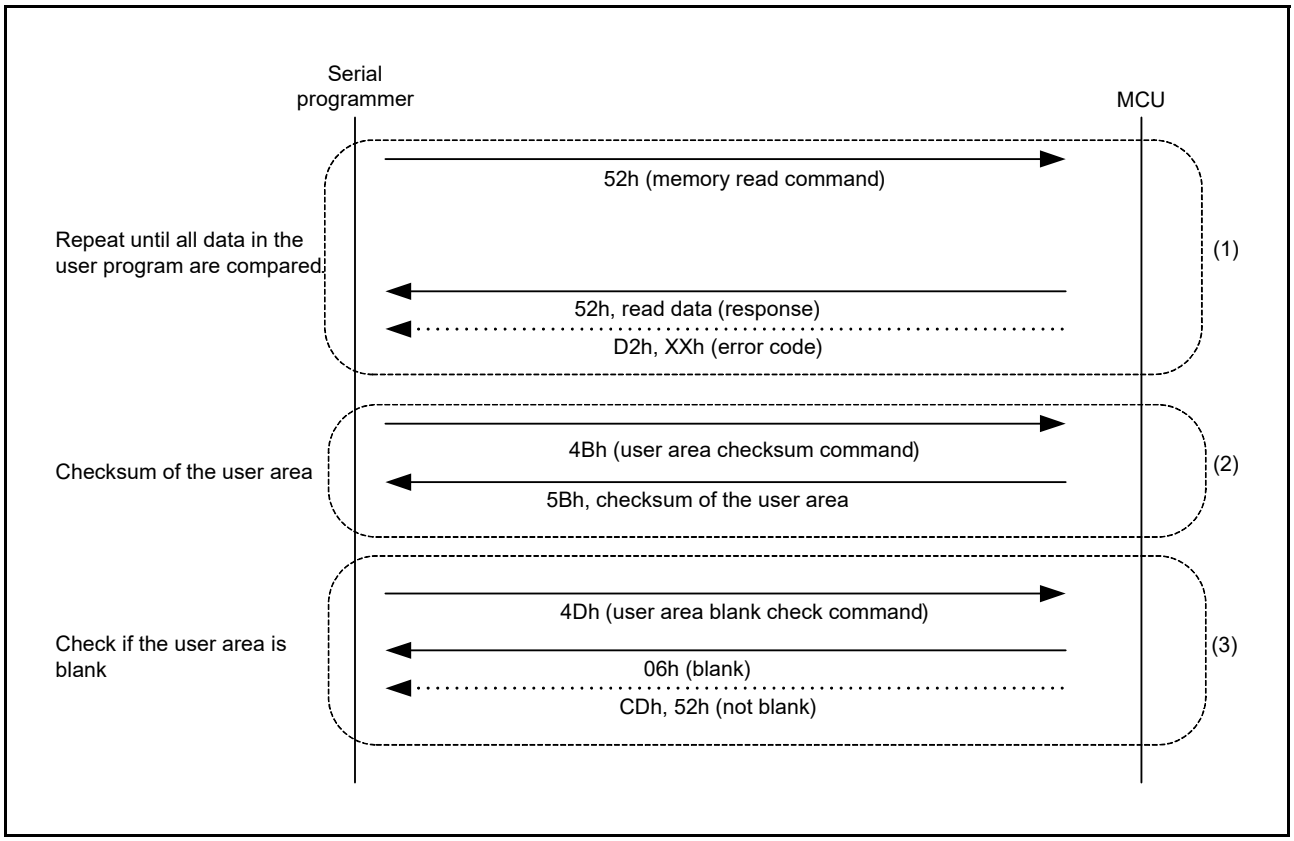


Figure 36.38 Procedure to Check Data in the User Area

36.11.9 Check Data in the Data Area

Read and check, checksum, and blank check the user area to check the programmed data in the data area.

(1) The read and check operation is used to read data in the data area and compare the read data with the programmed data to check if the program operation is performed successfully. Send a memory read command (52h) to read data in the data area.
(2) Send the data area checksum command (61h) to check program data using the checksum of data area.
(3) Send the data area blank check command (62h) to check if the data area has data.

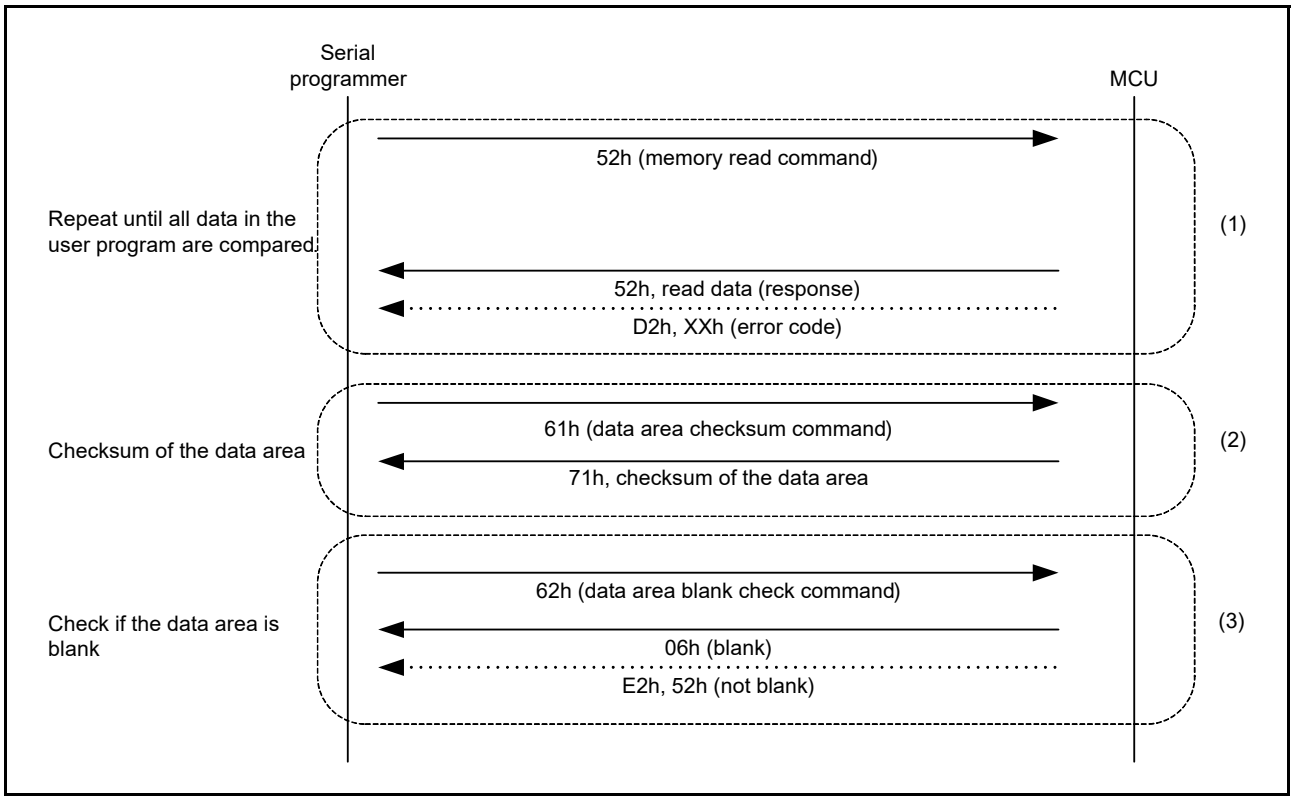


Figure 36.39 Procedure to Check Data in the Data Area

36.11.10 Set the Access Window in the User Area

Set the access window to avoid unintentionally rewriting the user area during the self-programming.

(1) Send the access window program command (74h) to set the access window settings.
(2) Send the access window read command (73h) to confirm the access window settings.

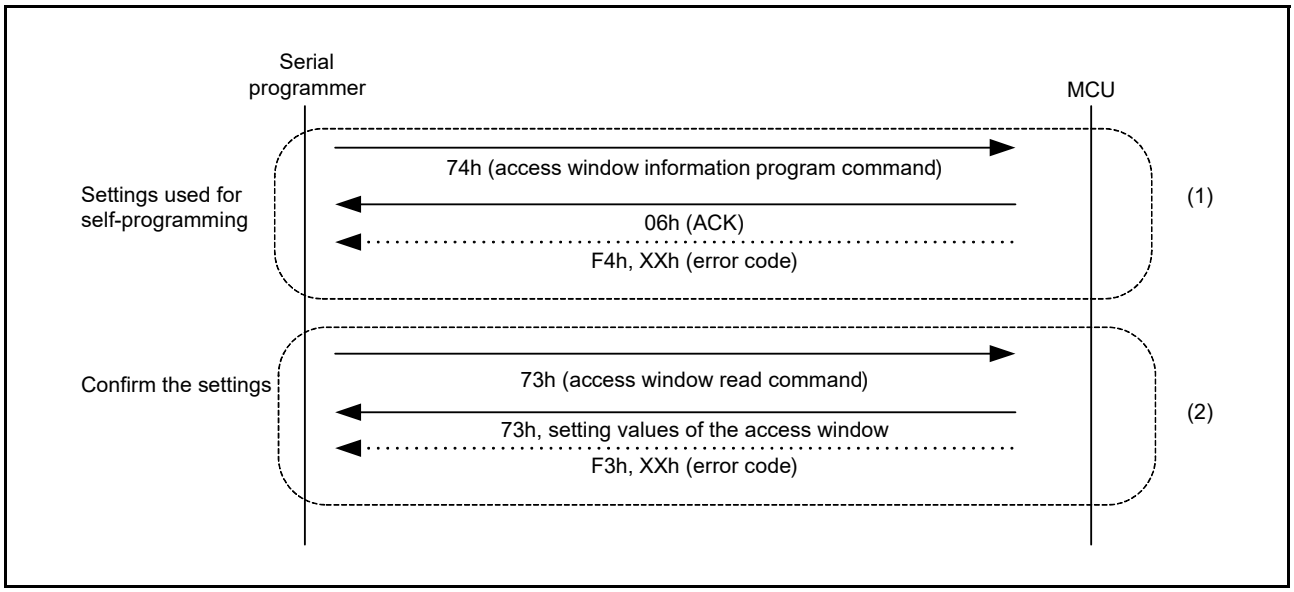


Figure 36.40 Procedure to Set the Access Window in the User Area

36.12 Rewriting by Self-Programming

36.12.1 Overview

The MCU supports rewriting of the flash memory by the user program. The ROM and E2 DataFlash can be rewritten by preparing a routine to rewrite the flash memory (flash rewrite routine) in the user program.
When rewriting the E2 DataFlash, the BGO can be used to execute the flash rewrite routine on the ROM. The E2 DataFlash can also be rewritten by executing the flash rewrite routine that is transferred on the RAM in advance.

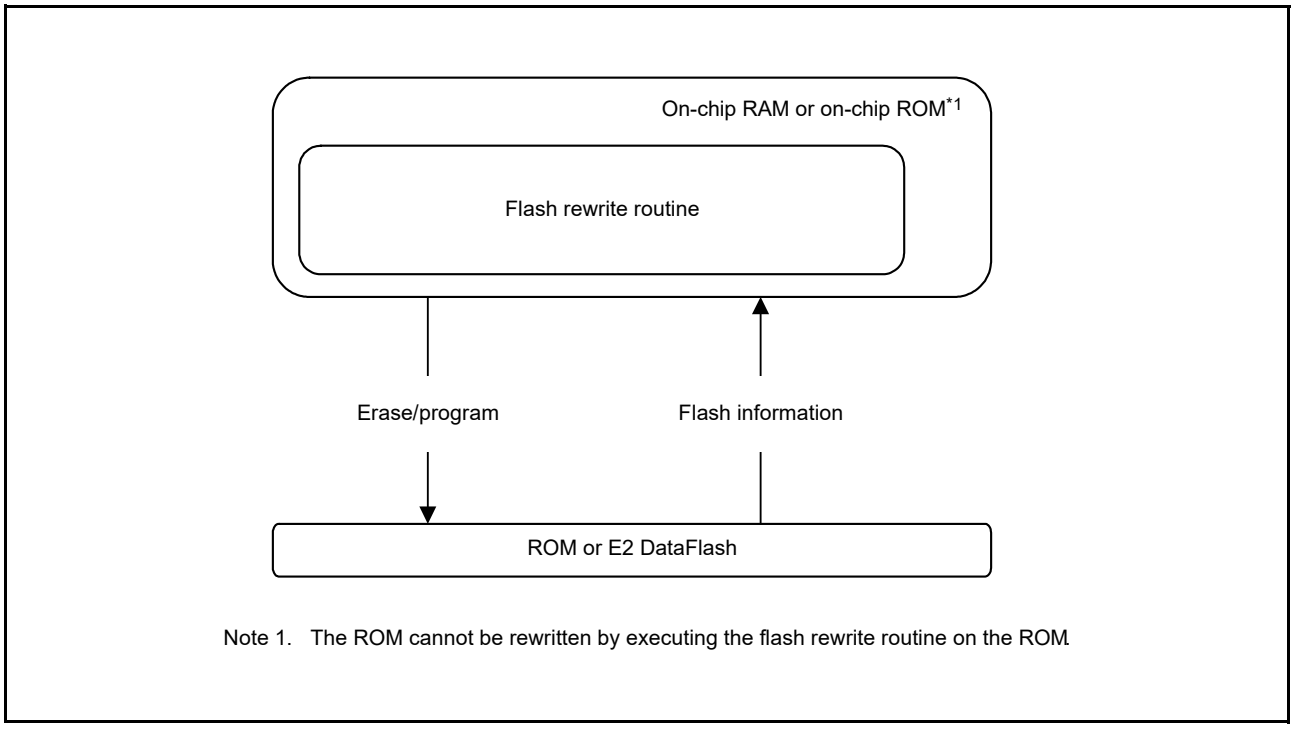


Figure 36.41 Self-Programming Overview

36.13 Usage Notes

(1) Access the Block Where Erase Operation is Forcibly Stopped
When forcibly stopping an erase operation, data in the block where the erase operation is aborted is undefined. To avoid malfunctions caused by reading undefined data, do not execute instructions or read data in the block where an erase operation is forcibly stopped.

(2) Processing After Forced Stop of Erase Operation
When an erase operation is forcibly stopped, issue a block erase command again to the same block.

(3) Additional Programming Disabled
The same address cannot be programmed more than once. When programming an area that has been already programmed, erase the area first.

(4) Reset during Program/Erase
If inputting a reset from the RES# pin, release the reset after reset input time of at least tRESW (refer to section 37, Electrical Characteristics) within the range of the operating voltage defined in the electrical characteristics.
The IWDT reset and software reset can be used regardless of tRESW.

(5) Location of Interrupt Vectors and Exception Vectors during Program/Erase Operation
When an interrupt or an exception occurs during a program/erase operation, the vector may be fetched from the ROM. To avoid fetching the vector from the ROM, allocate the interrupt vector table and exception vector table to the area other than the ROM with the INTB and EXTB registers in the CPU.

(6) Abnormal Termination during Program/Erase
When the voltage exceeds the range of the operating voltage during a program/erase operation or when a program/erase operation is not completed successfully due to a reset or prohibited actions described in (7), erase the area again.

(7) Actions Prohibited during Program/Erase
To prevent the damage to the flash memory, comply with the following instructions.

- Do not use the MCU power supply that is outside the operating voltage range.
- Do not update the value of the OPCCR.OPCM[2:0] bits.
- Do not change the clock source select bit in the SCKCR3 register.
- Do not change the division ratio of the flash interface clock (FCLK).
- Do not place the MCU in deep sleep mode or software standby mode.
- Do not access the E2 DataFlash during a program/erase operation to the ROM.
- Do not change the DFLCTL.DFLEN bit value during a program/erase operation to the E2 DataFlash.

(8) FCLK during Program/Erase
For programming/erasure by self-programming, set the frequency of the FlashIF clock (FCLK), and specify an integer FCLK frequency (MHz) in FISR.PCKA[4:0] bits. Note that when the FCLK is 4 to 32 MHz, a rounded-up value should be set for a non-integer frequency such as 12.5 MHz (i.e. 12.5 MHz should be set rounded up to 13 MHz). If the FCLK is equal to or less than 4 MHz, only 1, 2, 3, or 4 MHz can be used.

36.14 Usage Notes in Boot Mode

(1) Notes on Communication Errors in Boot Mode
When communication with the MCU cannot be performed properly, reset and start up in boot mode again.

(2) Notes on Power Supply Voltage in Boot Mode (SCI)
When the bit rate exceeds 500 kbps in boot mode (SCI), use a voltage that is 3.0 V or higher.

(3) Notes on Option-Setting Memory in Boot Mode
The settings of option function select register 0 (OFS0), option function select register 1 (OFS1), and endian select register (MDE) are disabled in boot mode.

(4) Notes on Switching the Start-Up Area
Switch the start-up area by self-programming.

37. Electrical Characteristics

37.1 Absolute Maximum Ratings

Table 37.1 Absolute Maximum Ratings

Conditions: VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V

Item		Symbol	Value	Unit
Power supply voltage		VCC	–0.3 to +6.5	V
Input voltage	Port 4, port 5, port 6	V_{in}	–0.3 to AVCC2 + 0.3	V
	Except for port 4, port 5, port 6 and ports for 5 V tolerant*1		–0.3 to VCC + 0.3	V
	Ports for 5 V tolerant*1		–0.3 to +6.5	V
Reference power supply voltage		VREFH0	–0.3 to AVCC0 + 0.3	V
		VREFH1	–0.3 to AVCC1 + 0.3	V
		VREFH2	–0.3 to AVCC2 + 0.3	V
Analog power supply voltage		AVCC0, AVCC1, AVCC2	–0.3 to +6.5	V
Analog input voltage	When AN000 to AN003, AN100 to AN103, AN200 to AN211 used	V_{AN}	–0.3 to AVCC2 + 0.3	V
	When AN016, AN116 used		–0.3 to VCC + 0.3	
Reference ground for PGA gain setting resistor		PGAVSS0	–0.3 to AVCC0 + 0.3	V
		PGAVSS1	–0.3 to AVCC1 + 0.3	V
Operating temperature		T_{opr}	–40 to +85	°C
Storage temperature		T_{stg}	–55 to +125	°C

Caution: Permanent damage to the MCU may result if absolute maximum ratings are exceeded.
To preclude any malfunctions due to noise interference, insert capacitors of high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, between the AVCC1 and AVSS1 pins, between the AVCC2 and AVSS2 pins, between the VREFH0 and VREFL0 pins, between the VREFH1 and VREFL1 pins, and between the VREFH2 and VREFL2 pins. Place capacitors of about 0.1 µF as close as possible to every power supply pin and use the shortest and heaviest possible traces.
Connect the VCL pin to a VSS pin via a 4.7 µF capacitor. The capacitor must be placed close to the pin.
Do not input signals or an I/O pull-up power supply to ports other than 5 V tolerant ports while the device is not powered.
The current injection that results from input of such a signal or I/O pull-up may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.
Even if –0.3 to +6.5 V is input to 5 V tolerant ports, it will not cause problems such as damage to the MCU.
Note 1. Ports B1 and B2 are 5 V tolerant.

Table 37.2 Recommended Operating Voltage Conditions

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltages	VCC*1, *2		2.7	—	5.5	V
	VSS		—	0	—	
Analog power supply voltages	AVCC0, AVCC1, AVCC2*1, *2, VREFH0, VREFH1, VREFH2		VCC	—	5.5	V
	AVSS0, AVSS1, AVSS2, VREFL0, VREFL1, VREFL2		—	0	—	

Note 1. AVCC0/AVCC1/AVCC2/VREFH0/VREFH1/VREFH2 and VCC can be set individually within the operating range.
Note 2. When powering on the VCC and AVCC0/AVCC1/AVCC2/VREFH0/VREFH1/VREFH2 pins, power them on at the same time or the VCC pin first and then the AVCC0/AVCC1/AVCC2/VREFH0/VREFH1/VREFH2 pin.

37.2 DC Characteristics

Table 37.3 DC Characteristics (1)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	RIIC input pin (except for SMBus, 5 V tolerant)	V_{IH}	VCC × 0.7	—	5.8	V	
	Ports B1, B2 (5 V tolerant)		VCC × 0.8	—	5.8		
	Ports 00 to 02, ports 10 to 17, ports 20 to 27, ports 30 to 37, ports 70 to 76, ports 80 to 84, ports 90 to 96, ports A0 to A7, ports B0, B3 to B7, ports C0 to C6, ports D0 to D7, ports E0 to E6, ports F0 to F3, ports G0 to G2, RES#		VCC × 0.8	—	VCC + 0.3		
	Ports 40 to 47, ports 50 to 55, ports 60 to 65		AVCC2 × 0.8	—	AVCC2 + 0.3		
	RIIC input pin (except for SMBus)	V_{IL}	–0.3	—	VCC × 0.3		
	Ports 40 to 47, ports 50 to 55, ports 60 to 65		–0.3	—	AVCC2 × 0.2		
	Other than RIIC input pin, Other than ports 40 to 47, ports 50 to 55, or ports 60 to 65		–0.3	—	VCC × 0.2		
	RIIC input pin (except for SMBus)	ΔV_T	VCC × 0.05	—	—		
	Ports 40 to 47, ports 50 to 55, ports 60 to 65		AVCC2 × 0.1	—	—		
	Other than RIIC input pin, Other than ports 40 to 47, ports 50 to 55, or ports 60 to 65		VCC × 0.1	—	—		
Input level voltage (except for Schmitt trigger input pins)	MD	V_{IH}	VCC × 0.9	—	VCC + 0.3	V	
	EXTAL (external clock input)		VCC × 0.8	—	VCC + 0.3		
	RIIC input pin (SMBus)		2.1	—	VCC + 0.3		VCC ≤ 5.2 V
	MD	V_{IL}	–0.3	—	VCC × 0.1		
	EXTAL (external clock input)		–0.3	—	VCC × 0.2		
	RIIC input pin (SMBus)		–0.3	—	0.8		VCC ≤ 5.2 V

Table 37.4 DC Characteristics (2)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input leakage current	RES#, MD, port E2	$\lvert I_{in} \rvert$	—	—	1.0	μA	V_{in} = 0 V, VCC
Three-state leakage current (off-state)	Port 4, port 5, port 6	$\lvert I_{TSI} \rvert$	—	—	1.0	μA	V_{in} = 0 V, AVCC2
	Ports except for 5 V tolerant ports and port 4, port 5, port 6		—	—	0.2		V_{in} = 0 V, VCC
	Ports for 5 V tolerant		—	—	1.0		V_{in} = 0 V, 5.8 V
Input capacitance	All input pins	C_{in}	—	4	15	pF	V_{in} = 0 mV, f = 1 MHz, T_a = 25°C
Input pull-up resistor	All ports (except for port E2)	R_U	10	20	50	kΩ	V_{in} = 0 V

Table 37.5 DC Characteristics (3)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item					Symbol	Typ. *7	Max.	Unit	Test Conditions
Supply current *1	High-speed operating mode	Normal operating mode	No peripheral operation*2	ICLK = 80 MHz	I_{CC}	26.0	—	mA	
				ICLK = 64 MHz		20.7	—		
				ICLK = 32 MHz		11.8	—		
				ICLK = 16 MHz		7.0	—		
				ICLK = 8 MHz		4.7	—		
			All peripheral operation: Normal	ICLK = 80 MHz*3		40.5	—		
				ICLK = 64 MHz*4		32.5	—		
				ICLK = 32 MHz*5		20.9	—		
				ICLK = 16 MHz*5		11.7	—		
				ICLK = 8 MHz*5		7.0	—		
			All peripheral operation: Max.	ICLK = 80 MHz*3		—	80.0		
				ICLK = 64 MHz*4		—	70.0		
				ICLK = 32 MHz*5		—	45.0		
		Sleep mode	No peripheral operation*2	ICLK = 80 MHz		7.2	—		
				ICLK = 64 MHz		6.1	—		
				ICLK = 32 MHz		4.4	—		
				ICLK = 16 MHz		3.4	—		
				ICLK = 8 MHz		2.9	—		
			All peripheral operation: Normal	ICLK = 80 MHz*3		26.9	—		
				ICLK = 64 MHz*4		21.9	—		
				ICLK = 32 MHz*5		15.5	—		
				ICLK = 16 MHz*5		9.0	—		
				ICLK = 8 MHz*5		5.7	—		

Item					Symbol	Typ. *7	Max.	Unit	Test Conditions
Supply current *1	High-speed operating mode	Deep sleep mode	No peripheral operation*2	ICLK = 80 MHz	I_{CC}	3.4	—	mA	
				ICLK = 64 MHz		2.9	—		
				ICLK = 32 MHz		2.5	—		
				ICLK = 16 MHz		2.3	—		
				ICLK = 8 MHz		2.2	—		
			All peripheral operation: Normal	ICLK = 80 MHz*3		22.2	—		
				ICLK = 64 MHz*4		17.9	—		
				ICLK = 32 MHz*5		12.9	—		
				ICLK = 16 MHz*5		7.6	—		
				ICLK = 8 MHz*5		4.8	—		
		Increase during BGO operation*6				2.5	—		
	Middle-speed operating modes	Normal operating mode	No peripheral operation*8	ICLK = 12 MHz*10	I_{CC}	5.3	—	mA	
				ICLK = 8 MHz		4.5	—		
				ICLK = 1 MHz		2.5	—		
			All peripheral operation: Normal*9	ICLK = 12 MHz*10		8.7	—		
				ICLK = 8 MHz		6.9	—		
				ICLK = 1 MHz		2.7	—		
			All peripheral operation: Max.*9	ICLK = 12 MHz*10		—	18.0		
		Sleep mode	No peripheral operation*8	ICLK = 12 MHz*10		2.6	—		
				ICLK = 8 MHz		2.7	—		
				ICLK = 1 MHz		2.2	—		
			All peripheral operation: Normal*9	ICLK = 12 MHz*10		6.7	—		
				ICLK = 8 MHz		5.6	—		
				ICLK = 1 MHz		2.5	—		
		Deep sleep mode	No peripheral operation*8	ICLK = 12 MHz*10		1.8	—		
				ICLK = 8 MHz		2.1	—		
				ICLK = 1 MHz		2.1	—		
			All peripheral operation: Normal*9	ICLK = 12 MHz*10		5.7	—		
				ICLK = 8 MHz		4.8	—		
				ICLK = 1 MHz		2.3	—		
		Increase during BGO operation*6				2.5	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. Supply of the clock signal to peripheral modules is stopped in this state. The clock source is PLL. FCLK, PCLKA, PCLKB, and PCLKD are set to divided by 64.
Note 3. The clock signal to peripheral modules is supplied in this state. The clock source is PLL. FCLK is set to divided by 4. PCLKA is set to divided by 1. PCLKB and PCLKD are set to divided by 2.
Note 4. The clock signal to peripheral modules is supplied in this state. The clock source is PLL. PCLKA is set to divided by 1. FCLK, PCLKB, and PCLKD are set to divided by 2.
Note 5. The clock signal to peripheral modules is supplied in this state. The clock source is PLL. The frequencies of FCLK, PCLKA, PCLKB, and PCLKD are same as ICLK.
Note 6. This is the increase when data is programmed to or erased from the ROM or E2 DataFlash during program execution.
Note 7. Values when VCC = 5 V.
Note 8. Supply of the clock signal to peripheral modules is stopped in this state. The clock source is PLL. FCLK, PCLKA, PCLKB, and PCLKD are set to divided by 64.
Note 9. Supply of the clock signal to peripheral modules is stopped in this state. The clock source is PLL. The frequencies of FCLK, PCLKA, PCLKB, and PCLKD are same as ICLK.
Note 10. When the frequency of PLL is 48 MHz.

Table 37.6 DC Characteristics (4)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item			Symbol	Typ.*3	Max.	Unit	Test Conditions
Supply current*1	Software standby mode*2	T_a = 25°C	I_{CC}	1.5	15.0	µA	
		T_a = 55°C		3.0	38.0		
		T_a = 85°C		13.0	135.0		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. The IWDT and LVD are stopped.
Note 3. VCC = 5 V.

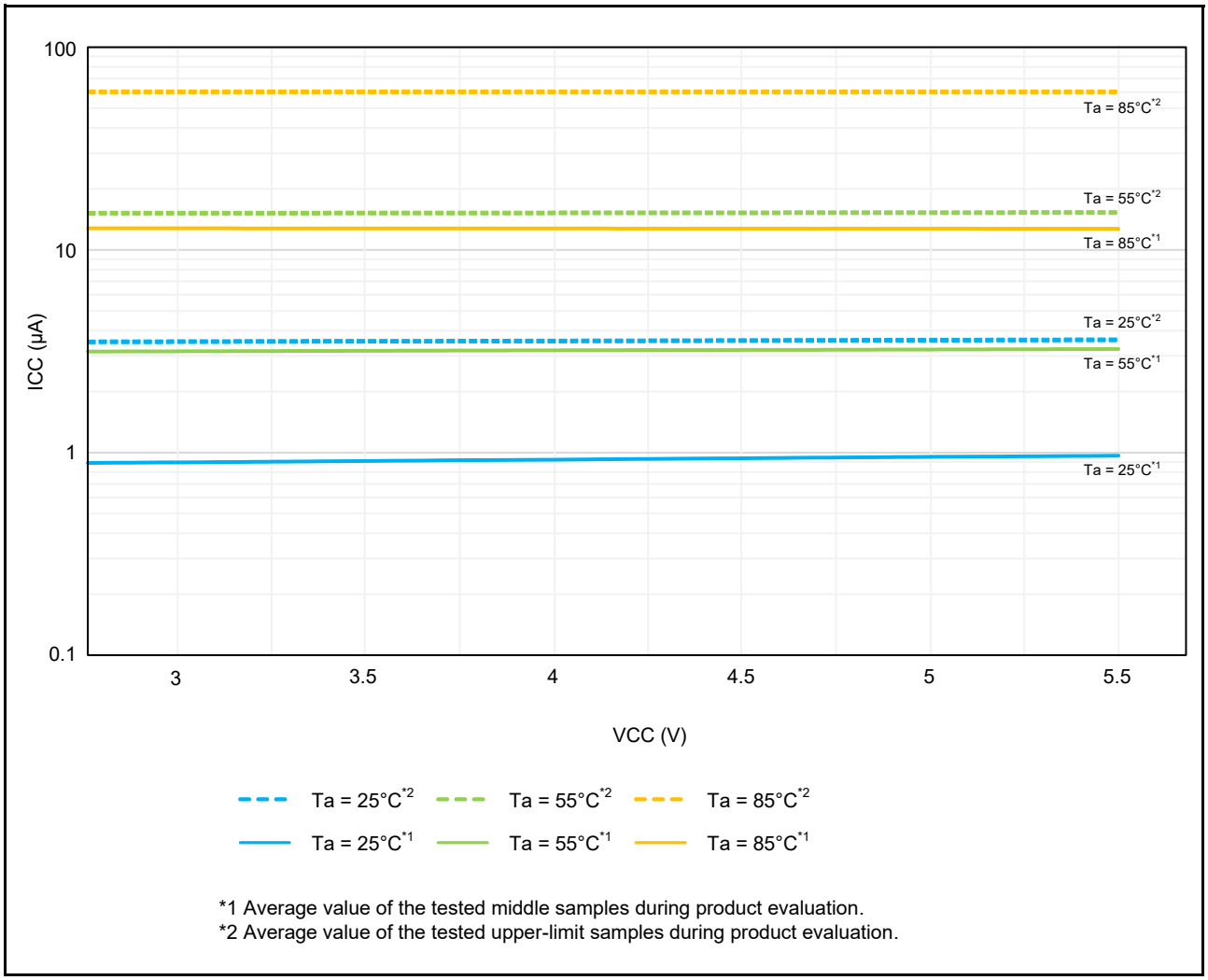


Figure 37.1 Voltage Dependency in Software Standby Mode (Reference Data)

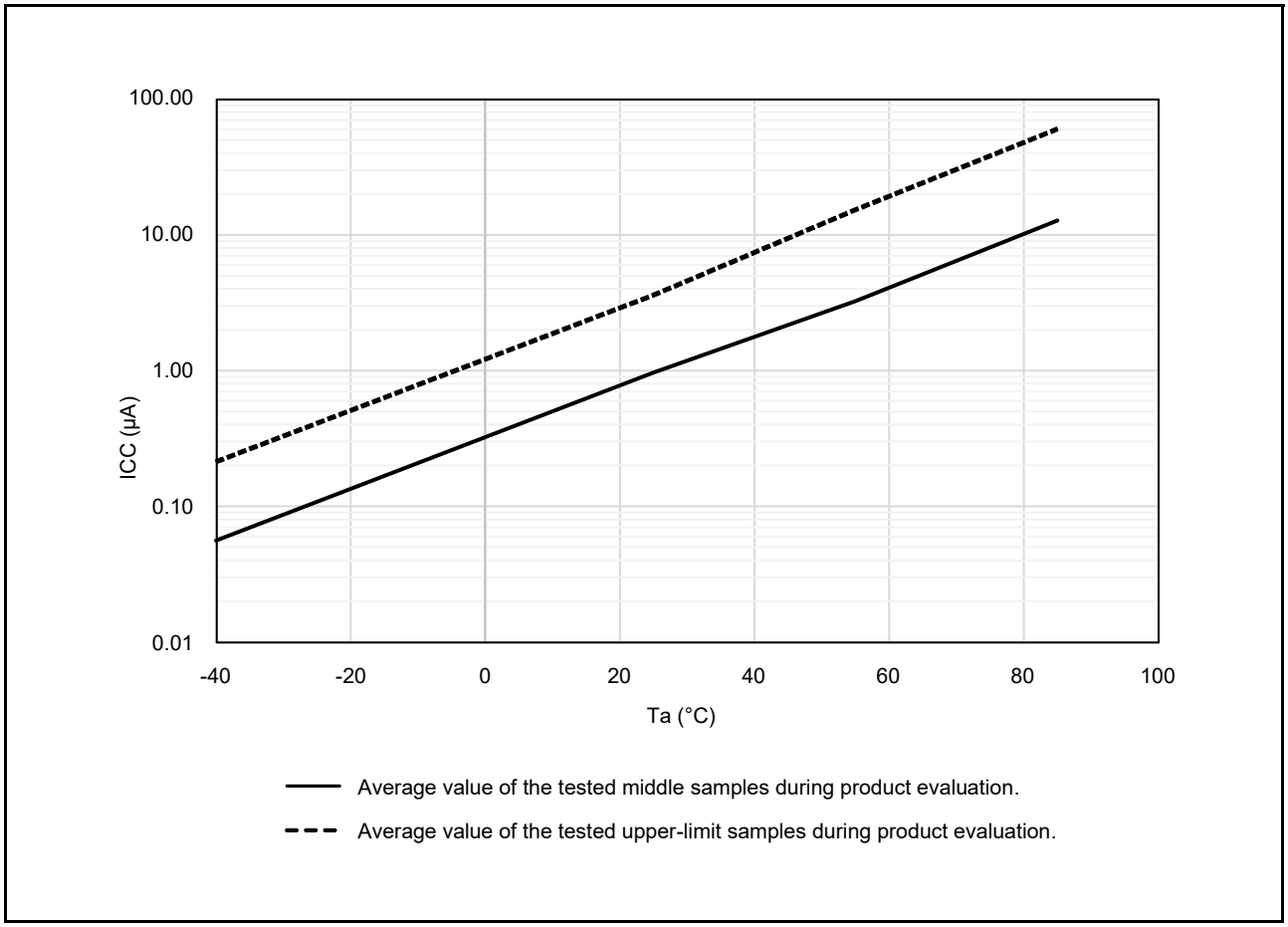


Figure 37.2 Temperature Dependency in Software Standby Mode (Reference Data)

Table 37.7 DC Characteristics (5)

Conditions: VCC = 2.7V to 5.5V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0V, T_a = –40 to +85°C

Item	Symbol	Typ.	Max.	Unit	Test Conditions
Permissible total consumption power*1	Pd	—	570	mW	

Note 1. Total power dissipated by the entire chip (including output currents)

Table 37.8 DC Characteristics (6)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0V, T_a = –40 to +85°C

Item			Symbol	Min.	Typ.*2	Max.	Unit	Test Conditions
Analog power supply current	A/D unit 0	During A/D conversion (programmable gain amplifier in use)	I_{AVCC}	—	1.5	2.5	mA	
		During A/D conversion (programmable gain amplifier not in use)		—	1.0	1.8		
	A/D unit 1	During A/D conversion (sample-and-hold circuits in use, programmable gain amplifier in use)		—	4.6	6.9		
		During A/D conversion (sample-and-hold circuits in use, programmable gain amplifier not in use)		—	3.1	4.8		
		During A/D conversion (sample-and-hold circuits not in use, programmable gain amplifier in use)		—	2.5	3.9		
		During A/D conversion (sample-and-hold circuits not in use, programmable gain amplifier not in use)		—	1.0	1.8		
	A/D unit 2			—	1.0	1.8		
	During D/A conversion (per 1 channel)*1			—	0.7	1.0		
	Waiting for A/D or D/A conversion (all units)			—	—	2.2	μA	
Reference power supply current	During A/D conversion (at high-speed conversion per 1 unit)		I_{REFH}	—	10.0	20.0	μA	
	Waiting for A/D conversion (all units)			—	—	180.0	nA	
Comparator C operating current*3	Comparator enabled		I_{CMP}	—	40.0	60.0	μA	

Note 1. The value of the D/A converter is the value of the power supply current including the reference current.
Note 2. When VCC =AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = 5 V.
Note 3. Current consumed only by the comparator C module.

Table 37.9 DC Characteristics (7)

Conditions: VCC = 0 V to AVCC0, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = 0 V to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Power-on VCC rising gradient	At normal startup	SrVCC	0.02	—	20	ms/V	
	Voltage monitoring 0 reset enabled at startup*1, *2		0.02	—	—		

Note 1. When OFS1.LVDAS = 0.
Note 2. Turn on the power supply voltage according to the normal startup rising gradient because the register settings set by OFS1 are not read in boot mode.

Table 37.10 DC Characteristics (8)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

The ripple voltage must meet the allowable ripple frequency $f_{r\,(VCC)}$ within the range between the VCC upper limit (5.5 V) and lower limit (2.7 V). When VCC change exceeds VCC ±10%, the allowable voltage change rising/falling gradient dt/dVCC must be met.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Allowable ripple frequency	$f_{r\,(VCC)}$	—	—	10	kHz	Figure 37.3 $V_{r\,(VCC)} \leq VCC \times 0.2$
		—	—	1	MHz	Figure 37.3 $V_{r\,(VCC)} \leq VCC \times 0.08$
		—	—	10	MHz	Figure 37.3 $V_{r\,(VCC)} \leq VCC \times 0.06$
Allowable voltage change rising/falling gradient	dt/dVCC	1.0	—	—	ms/V	When VCC change exceeds VCC ±10%

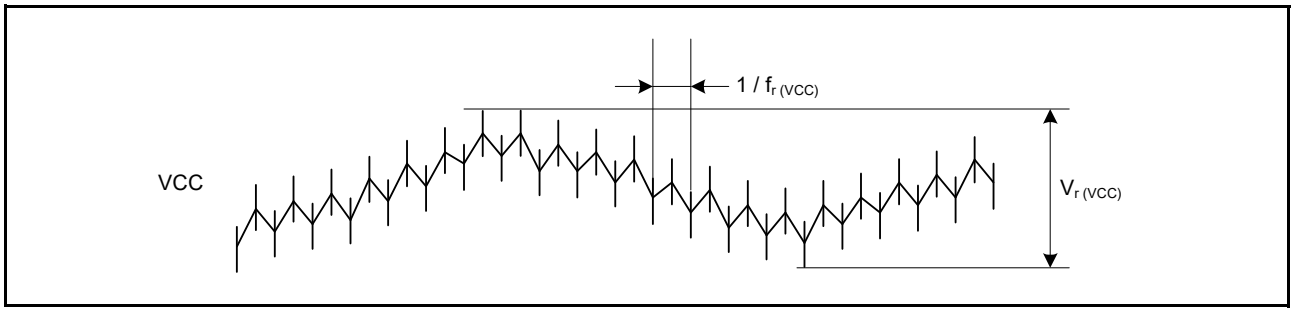


Figure 37.3 Ripple Waveform

Table 37.11 DC Characteristics (9)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Permissible error of VCL pin external capacitance	C_{VCL}	3.3	4.7	6.1	µF	

Note: The recommended capacitance is 4.7 µF. Variations in connected capacitors should be within the above range.

Table 37.12 Permissible Output Currents

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item			Symbol	Max.	Unit
Permissible output low current	Ports 71 to 76, port 81, ports 90 to 95, port B5, port D3		I_{OL}	10.0	mA
	RIIC pins			6.0	
	Ports other than above	Normal output mode		4.0	
		High-drive output mode		8.0	
Permissible output low current	Total of all output pins		ΣI_{OL}	110.0	
	Total of ports 40 to 47, ports 50 to 55, ports 60 to 65			50.0	
	Total of port 02, ports E5 and E6, ports 10 to 17, ports 80 to 84			50.0	
	Total of ports B4 to B7, ports F0 to F3, ports D0 to D7, ports E0 and E1			55.0	
	Total of port 96, ports 34 and 35, ports A0 to A7, ports B0 to B3, ports C0 to C2, ports C5 and C6			90.0	
	Total of ports 71 to 76			30.0	
	Total of ports 90 to 95			30.0	
	Total of ports 31 to 33, ports G0 to G2, port 70			32.0	
	Total of ports 20 to 27, port 30, ports C3 and C4			50.0	
Permissible output high current	Ports 71 to 76, port 81, ports 90 to 95, port B5, port D3		I_{OH}	–5.0	
	Ports other than above	Normal output mode		–4.0	
		High-drive output mode		–8.0	
Permissible output high current	Total of all output pins		ΣI_{OH}	–35.0	
	Total of ports 40 to 47, ports 50 to 55, ports 60 to 65			–25.0	

Note: Do not exceed the permissible total supply current.

Table 37.13 Output Values of Voltage

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Output low	Ports 71 to 76, port 81, ports 90 to 95, port B5, port D3		V_{OL}	—	0.8	V	I_{OL} = 10.0 mA
	RIIC pins	Standard mode		—	0.4		I_{OL} = 3.0 mA
		Fast mode		—	0.6		I_{OL} = 6.0 mA
	Ports other than above	Normal output mode		—	0.8		I_{OL} = 1.0 mA
		High-drive output mode		—	0.8		I_{OL} = 2.0 mA
Output high	Ports 71 to 76, port 81, ports 90 to 95, port B5, port D3		V_{OH}	VCC – 0.8	—	V	I_{OH} = –5.0 mA
	Ports 40 to 47, ports 50 to 55, ports 60 to 65			AVCC2 – 0.8	—		I_{OH} = –2.0 mA
	Ports other than above	Normal output mode		VCC – 0.8	—		I_{OH} = –2.0 mA
		High-drive output mode		VCC – 0.8	—		I_{OH} = –4.0 mA

37.2.1 Normal I/O Pin Output Characteristics (1)

Figure 37.4 to Figure 37.7 show the characteristics when normal output is selected by the drive capacity control register.

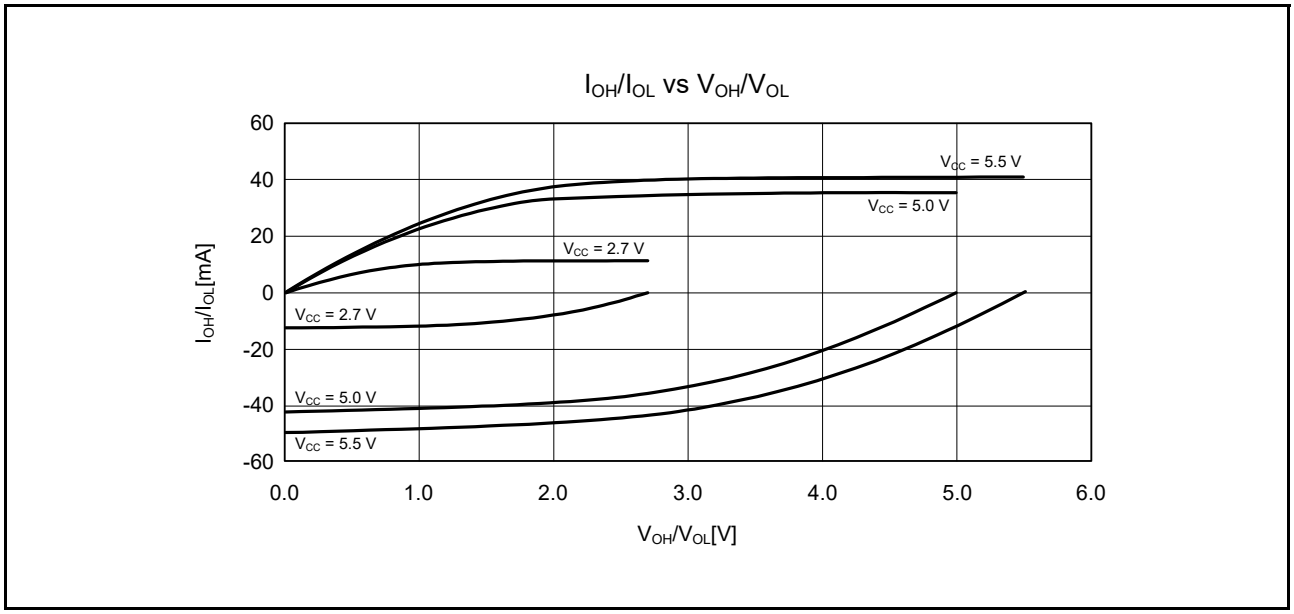


Figure 37.4 V_{OH}/V_{OL} and I_{OH}/I_{OL} Voltage Characteristics at T_a = 25°C When Normal Output is Selected (Reference Data)

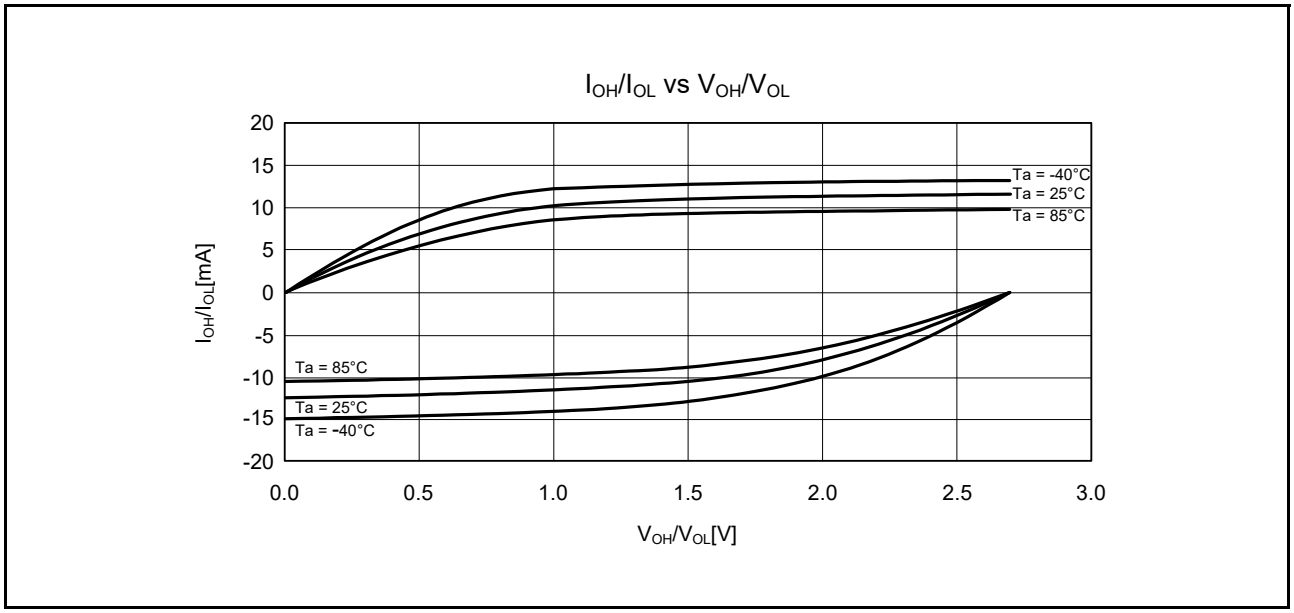


Figure 37.5 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 2.7 V when Normal Output is Selected (Reference Data)

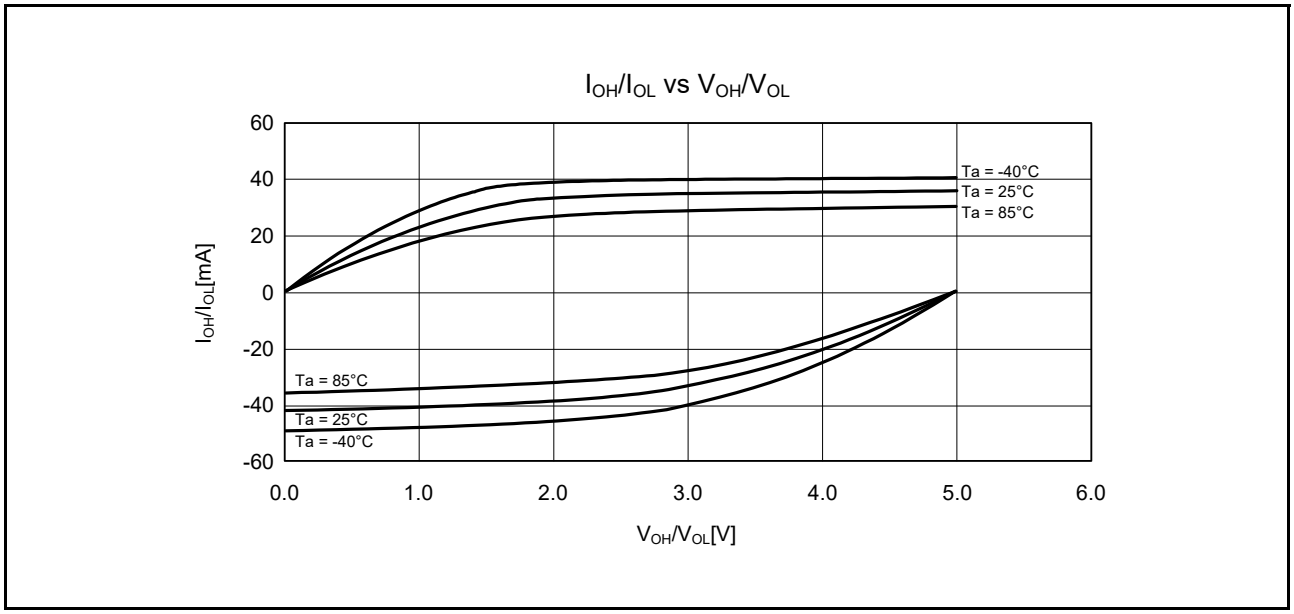


Figure 37.6 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 5.0 V when Normal Output is Selected (Reference Data)

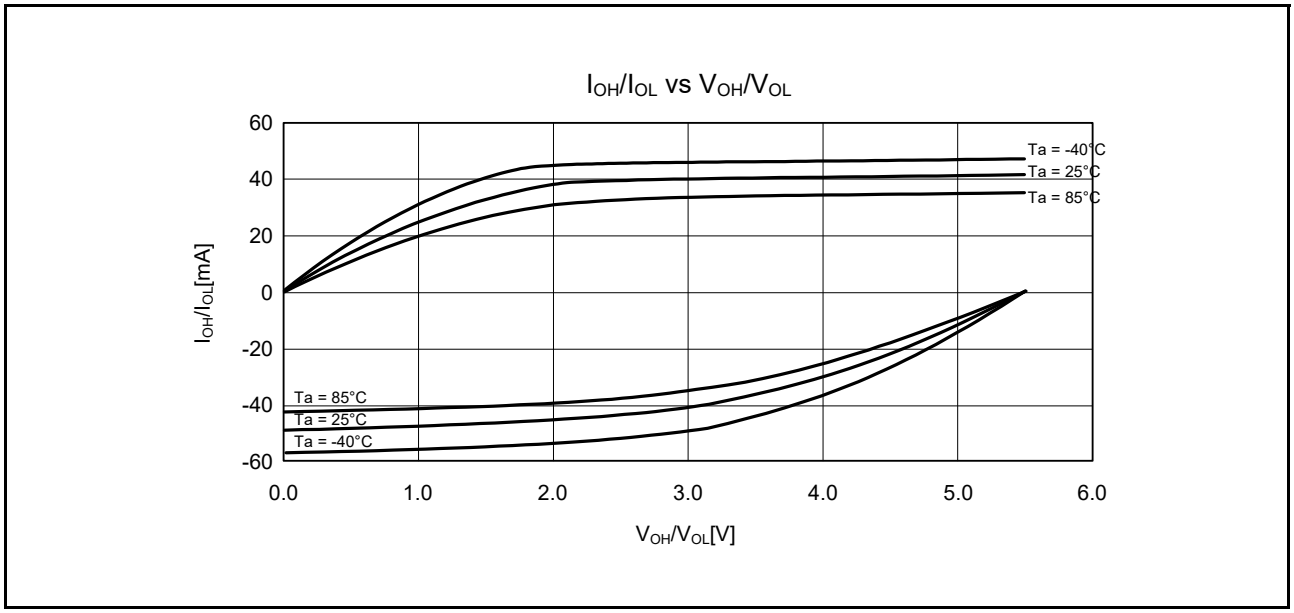


Figure 37.7 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 5.5 V when Normal Output is Selected (Reference Data)

37.2.2 Standard I/O Pin Output Characteristics (2)

Figure 37.8 to Figure 37.11 show the characteristics when high-drive output is selected by the drive capacity control register.

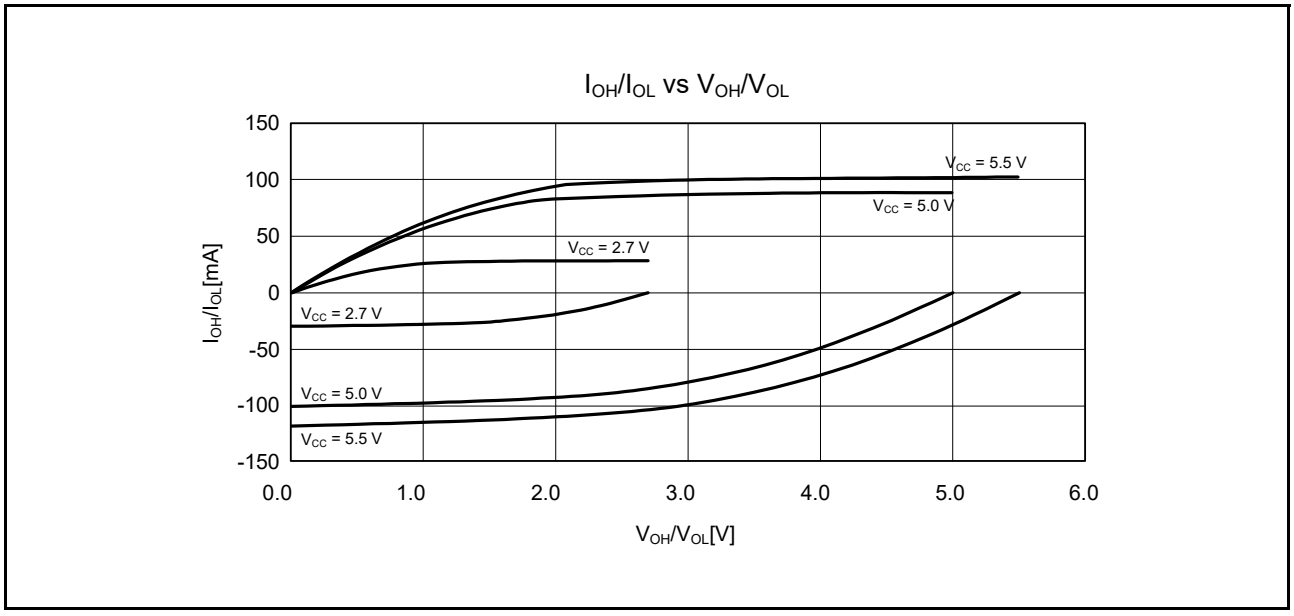


Figure 37.8 V_{OH}/V_{OL} and I_{OH}/I_{OL} Voltage Characteristics at T_a = 25°C When Normal Output is Selected (Reference Data)

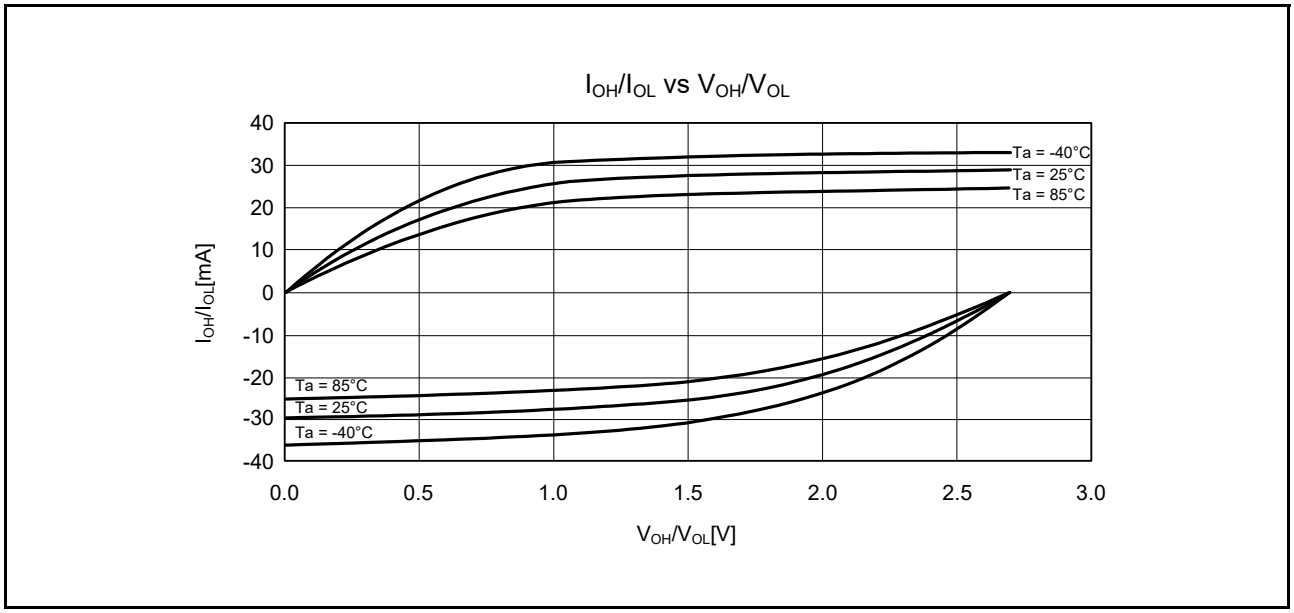


Figure 37.9 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 2.7 V when Normal Output is Selected (Reference Data)

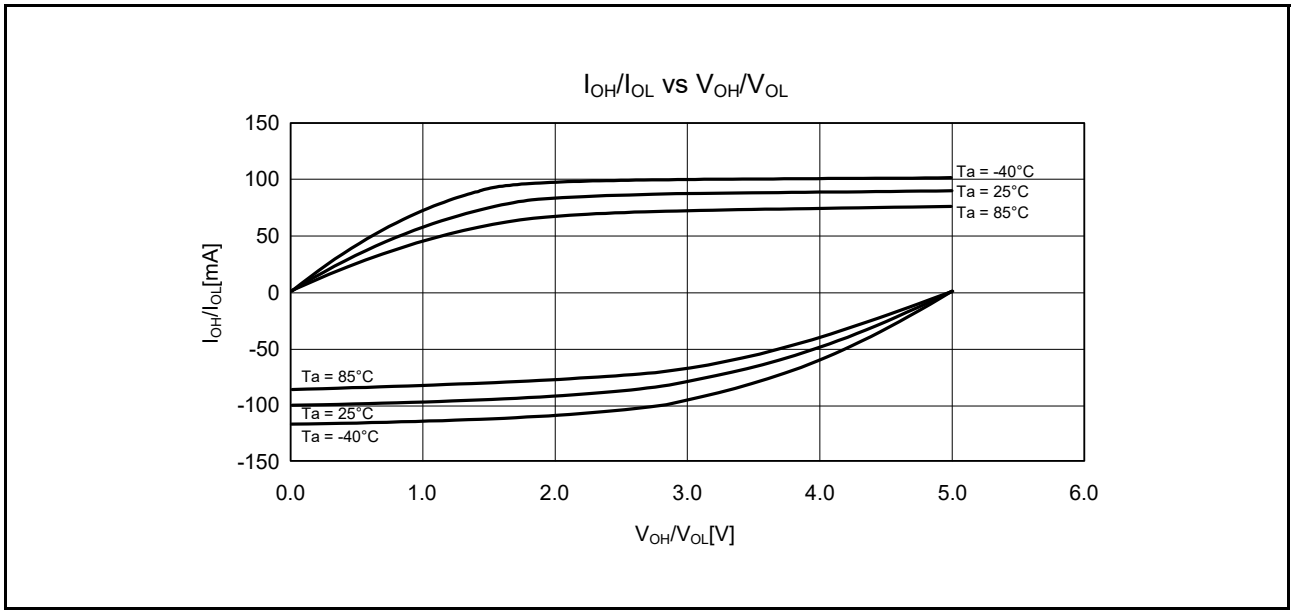


Figure 37.10 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 5.0 V when Normal Output is Selected (Reference Data)

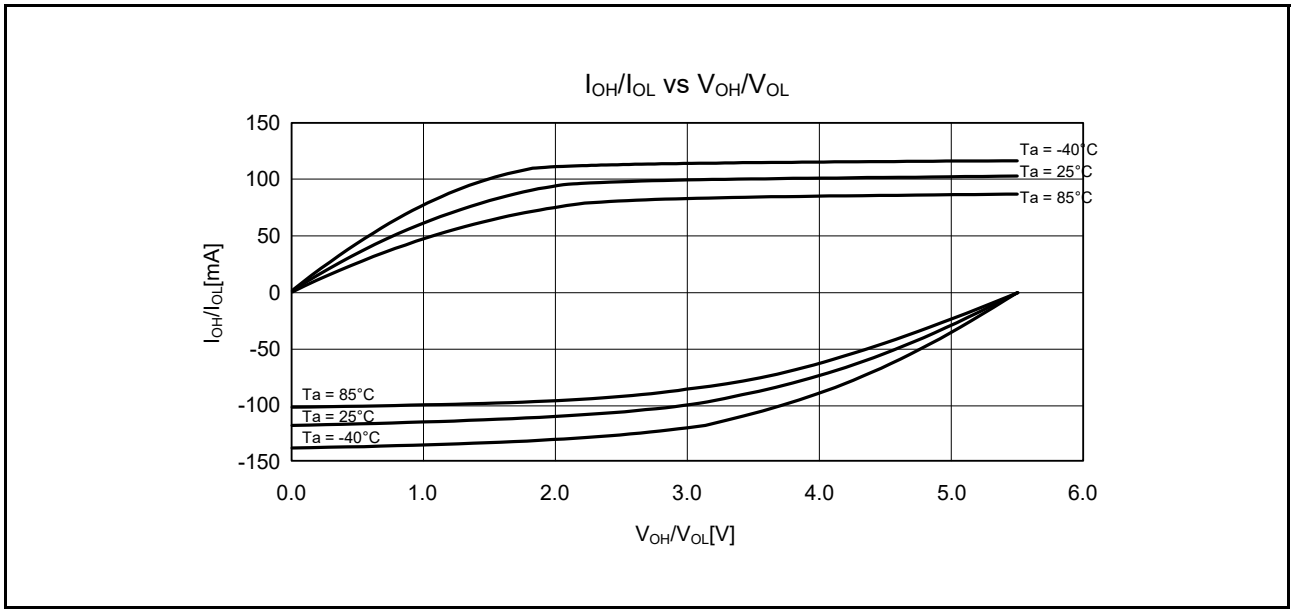


Figure 37.11 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 5.5 V when Normal Output is Selected (Reference Data)

37.2.3 Standard I/O Pin Output Characteristics (3)

Figure 37.12 to Figure 37.15 show the output characteristics of the large current ports.

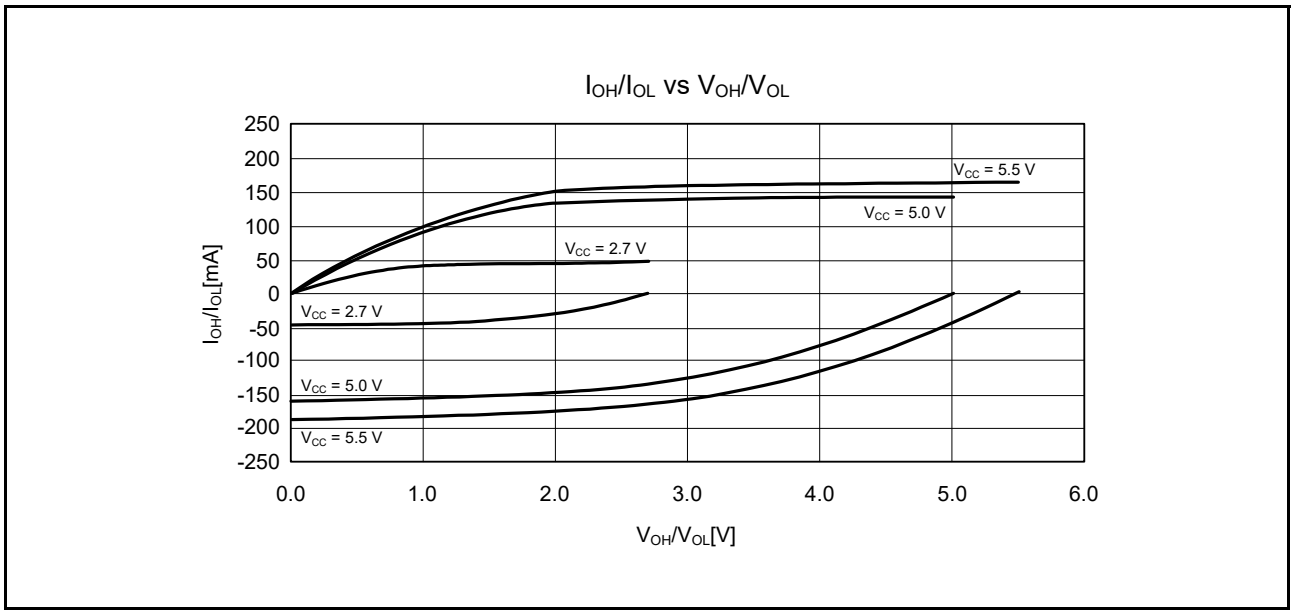


Figure 37.12 V_{OH}/V_{OL} and I_{OH}/I_{OL} Voltage Characteristics of Large Current Ports at T_a = 25°C (Reference Data)

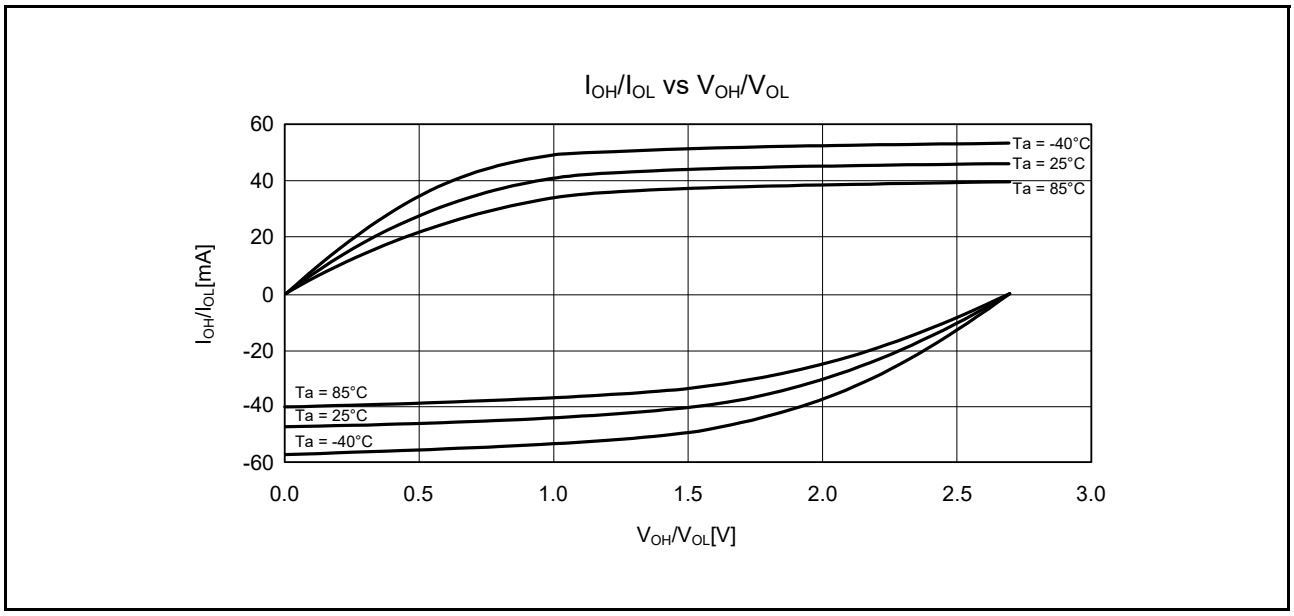


Figure 37.13 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics of Large Current Ports at VCC = 2.7 V (Reference Data)

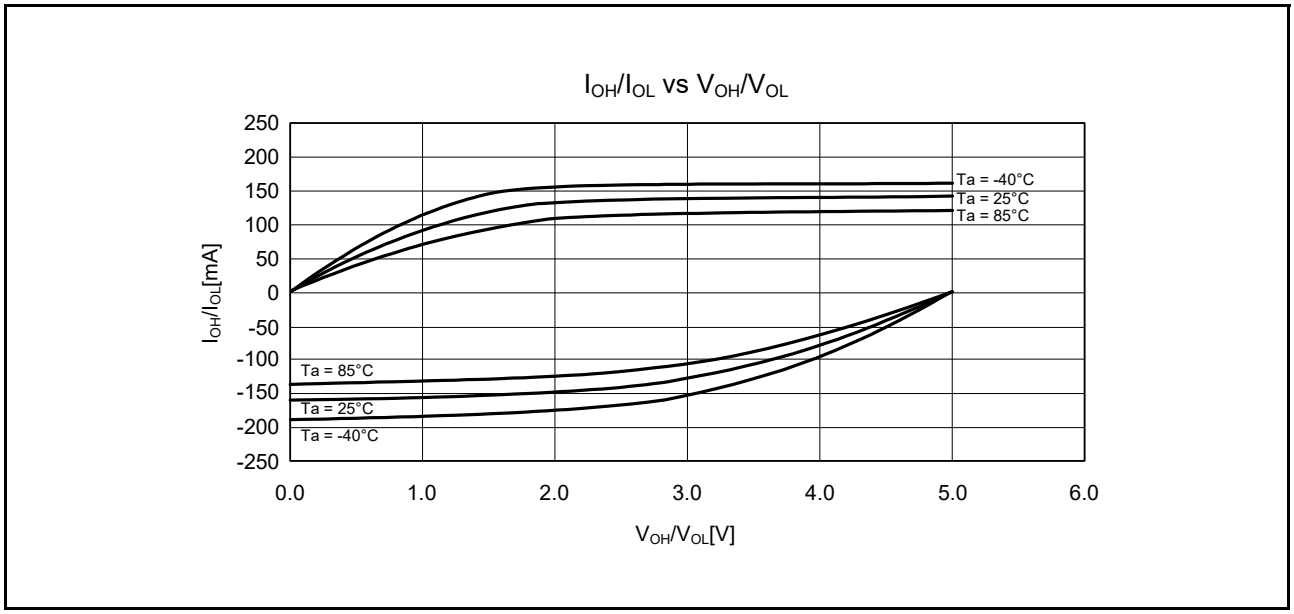


Figure 37.14 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics of Large Current Ports at VCC = 5.0 V (Reference Data)

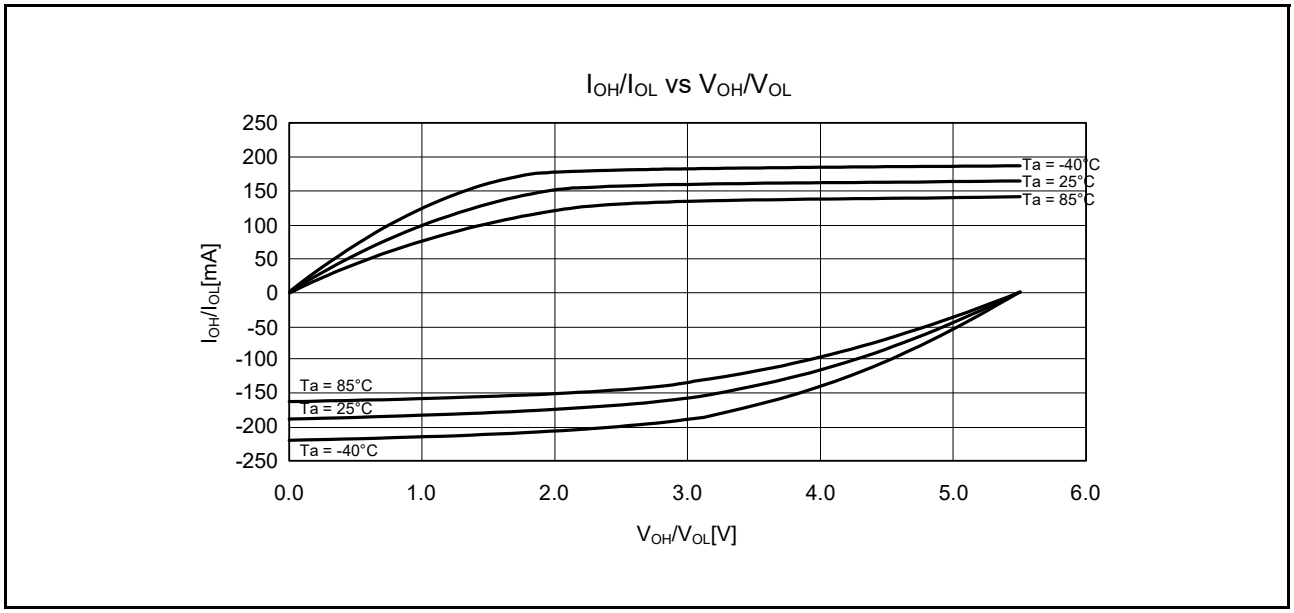


Figure 37.15 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics of Large Current Ports at VCC = 5.5 V (Reference Data)

37.2.4 RIIC Pin Output Characteristics

Figure 37.16 to Figure 37.19 show the output characteristics of the RIIC pin.

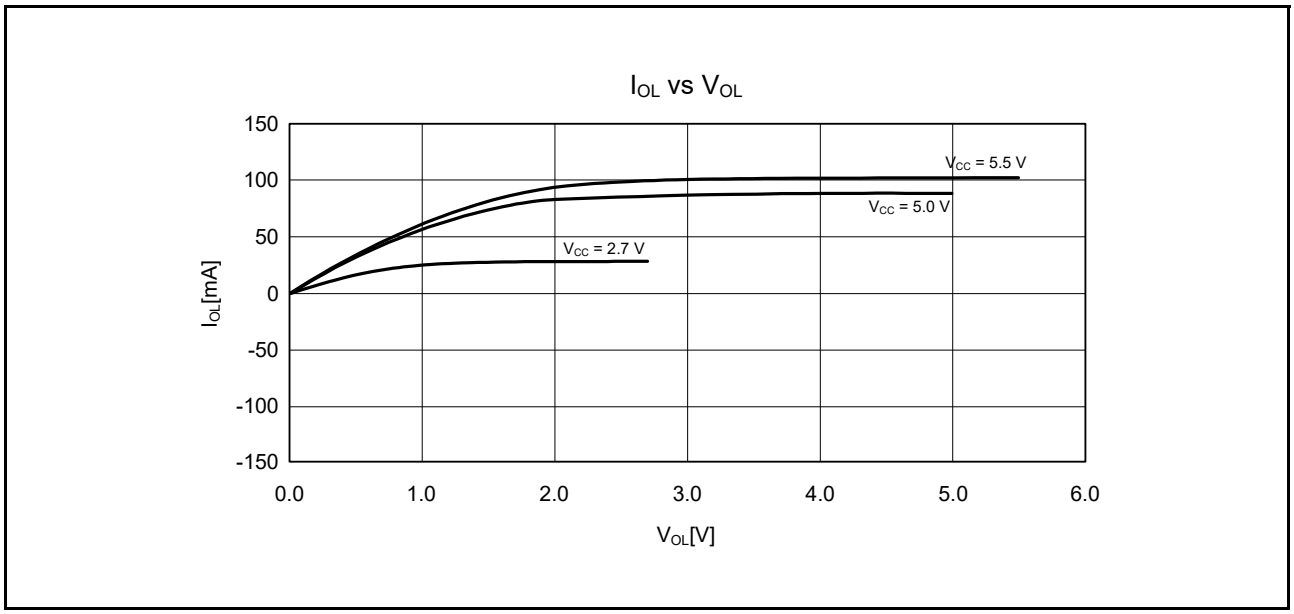


Figure 37.16 V_{OL} and I_{OL} Voltage Characteristics of RIIC Output Pin at T_a = 25°C (Reference Data)

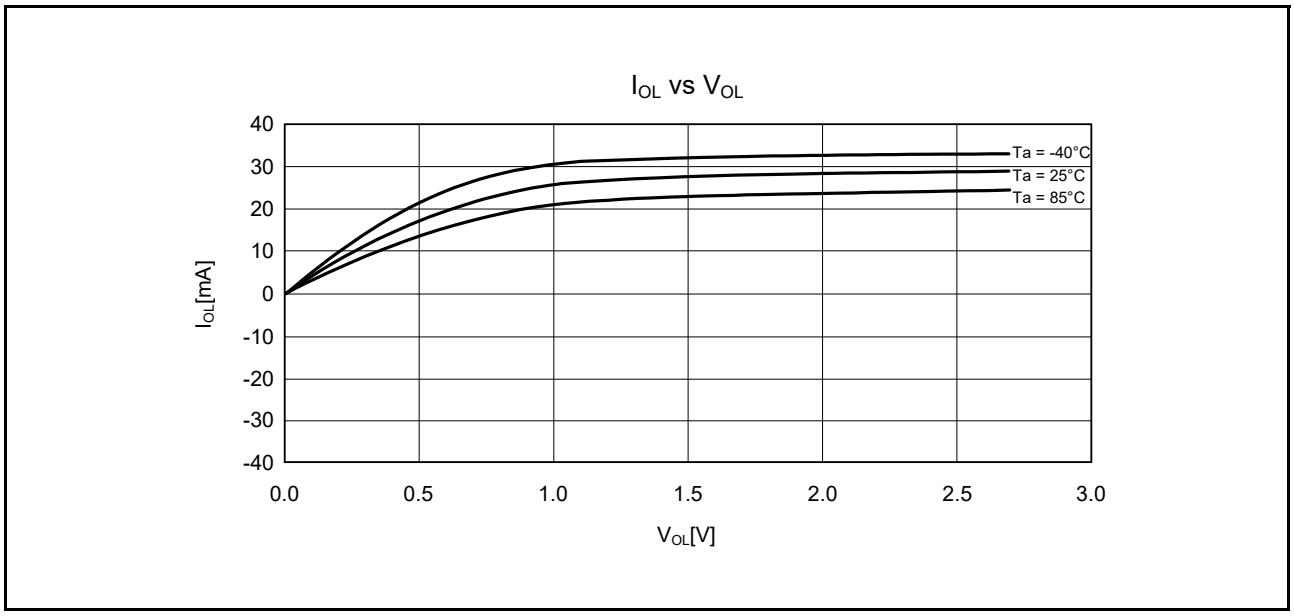


Figure 37.17 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at VCC = 2.7 V (Reference Data)

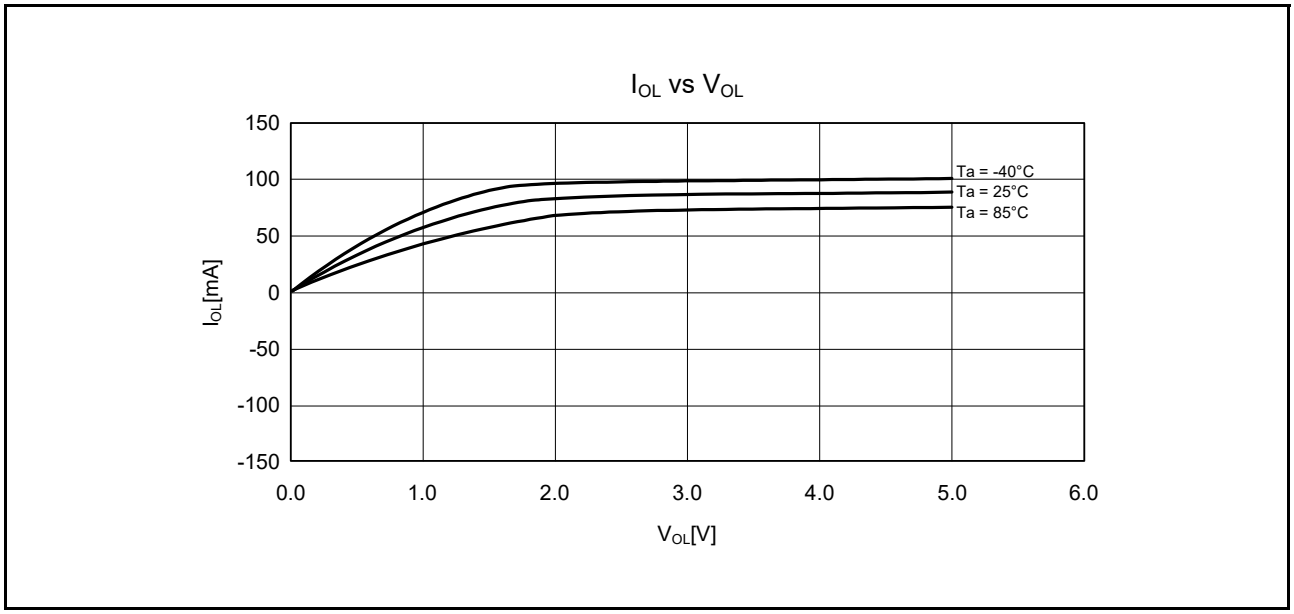


Figure 37.18 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at VCC = 5.0 V (Reference Data)

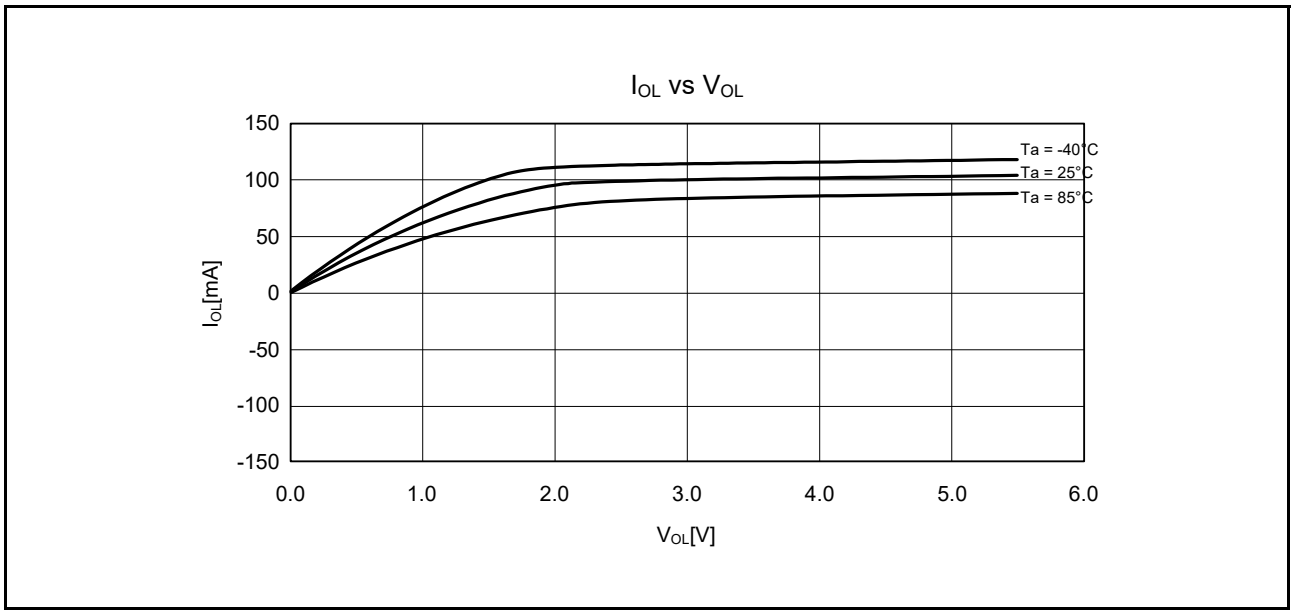


Figure 37.19 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at VCC = 5.5 V (Reference Data)

37.3 AC Characteristics

37.3.1 Clock Timing

Table 37.14 Operating Frequency Value (High-Speed Operating Mode)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item		Symbol	min.	typ.	max.	Unit
Operating frequency	System clock (ICLK)	f_{max}	—	—	80	MHz
	FlashIF clock (FCLK)*1, *2		—	—	32	
	Peripheral module clock (PCLKA)		—	—	80	
	Peripheral module clock (PCLKB)		—	—	40	
	Peripheral module clock (PCLKD)		—	—	40	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK should be ±3.5%.

Table 37.15 Operating Frequency Value (Middle-Speed Operating Mode)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item		Symbol	min.	typ.	max.	Unit
Operating frequency	System clock (ICLK)	f_{max}	—	—	12	MHz
	FlashIF clock (FCLK)*1, *2		—	—	12	
	Peripheral module clock (PCLKA)		—	—	12	
	Peripheral module clock (PCLKB)		—	—	12	
	Peripheral module clock (PCLKD)		—	—	12	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK should be ±3.5%.

Table 37.16 Clock Timing

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time	t_{Xcyc}	50	—	—	ns	Figure 37.20
EXTAL external clock input high pulse width	t_{XH}	20	—	—	ns	
EXTAL external clock input low pulse width	t_{XL}	20	—	—	ns	
EXTAL external clock rise time	t_{Xr}	—	—	5	ns	
EXTAL external clock fall time	t_{Xf}	—	—	5	ns	
EXTAL external clock input wait time*1	t_{XWT}	0.5	—	—	μs	
Main clock oscillator oscillation frequency	f_{MAIN}	1	—	20	MHz	
Main clock oscillation stabilization time (crystal)*2	$t_{MAINOSC}$	—	3	—	ms	Figure 37.21
Main clock oscillation stabilization time (ceramic resonator)*2	$t_{MAINOSC}$	—	50	—	μs	
LOCO clock oscillation frequency	f_{LOCO}	3.44	4.0	4.56	MHz	
LOCO clock oscillation stabilization time	t_{LOCO}	—	—	0.5	μs	Figure 37.22
HOCO clock oscillation frequency	f_{HOCO} (32 MHz)	31.52	32	32.48	MHz	T_a = –40 to –20°C
		31.68	32	32.32	MHz	T_a = –20 to +75°C
		31.52	32	32.48	MHz	T_a = +75 to +85°C
	f_{HOCO} (64 MHz)	63.04	64	64.96	MHz	T_a = –40 to –20°C
		63.36	64	64.64	MHz	T_a = –20 to +75°C
		63.04	64	64.96	MHz	T_a = +75 to +85°C
HOCO clock oscillation stabilization time	t_{HOCO} (32 MHz)	—	—	37.1	μs	Figure 37.24
	t_{HOCO} (64 MHz)	—	—	80.6	μs	Figure 37.24
IWDT-dedicated clock oscillation frequency	f_{ILOCO}	12.75	15	17.25	kHz	
IWDT-dedicated clock oscillation stabilization time	t_{ILOCO}	—	—	50	μs	Figure 37.25
PLL circuit oscillation frequency	f_{PLL}	40	—	80	MHz	
PLL clock oscillation stabilization time	t_{PLL}	—	—	50	μs	Figure 37.26
PLL free-running oscillation frequency	f_{PLLFR}	—	8	—	MHz	

Note 1. Time until the clock can be used after the main clock oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating) when the external clock is stable.

Note 2. Reference values when an 8 MHz resonator is used.
When specifying the main clock oscillator stabilization time, set the MOSCWTCR register with a stabilization time value that is equal to or greater than the resonator-manufacturer-recommended value.
After changing the setting of the MOSCCR.MOSTP bit so that the main clock oscillator operates, read the OSCOVFSR.MOOVF flag to confirm that is has become 1, and then start using the main clock.

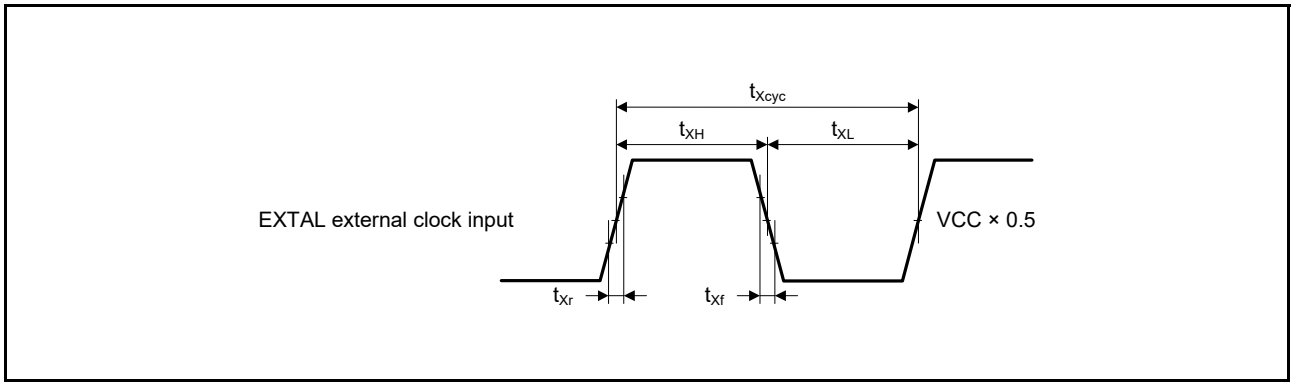


Figure 37.20 EXTAL External Clock Input Timing

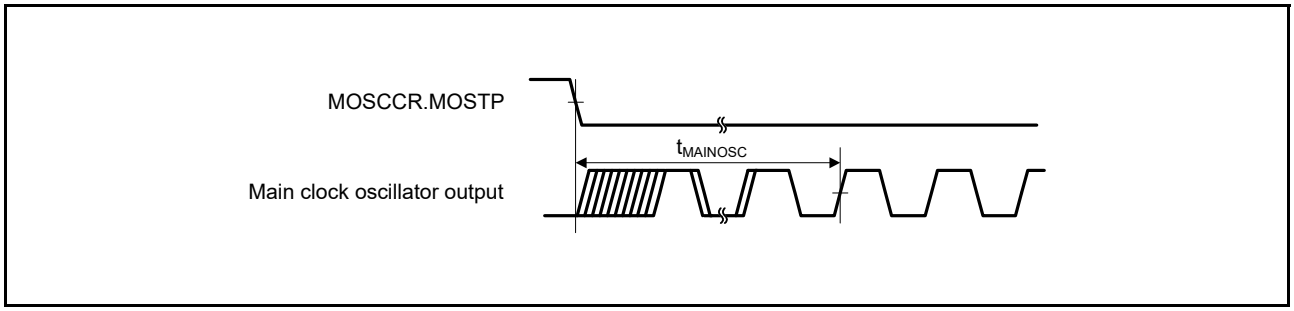


Figure 37.21 Main Clock Oscillation Start Timing

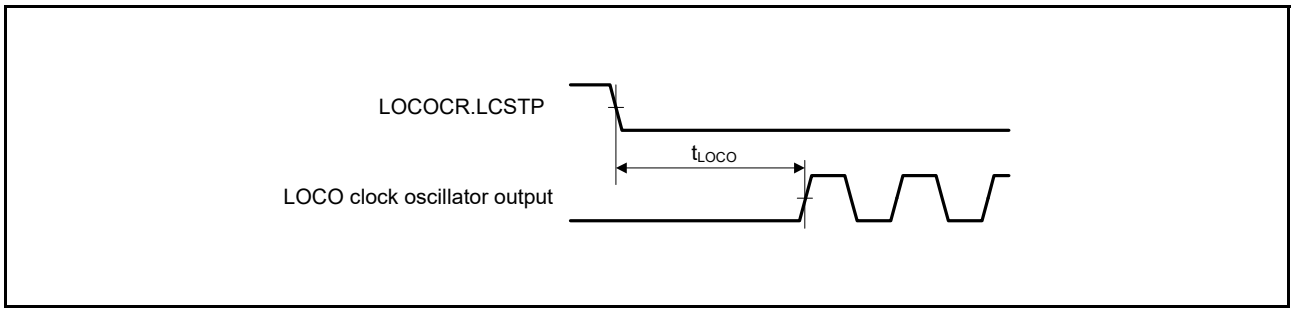


Figure 37.22 LOCO Clock Oscillation Start Timing

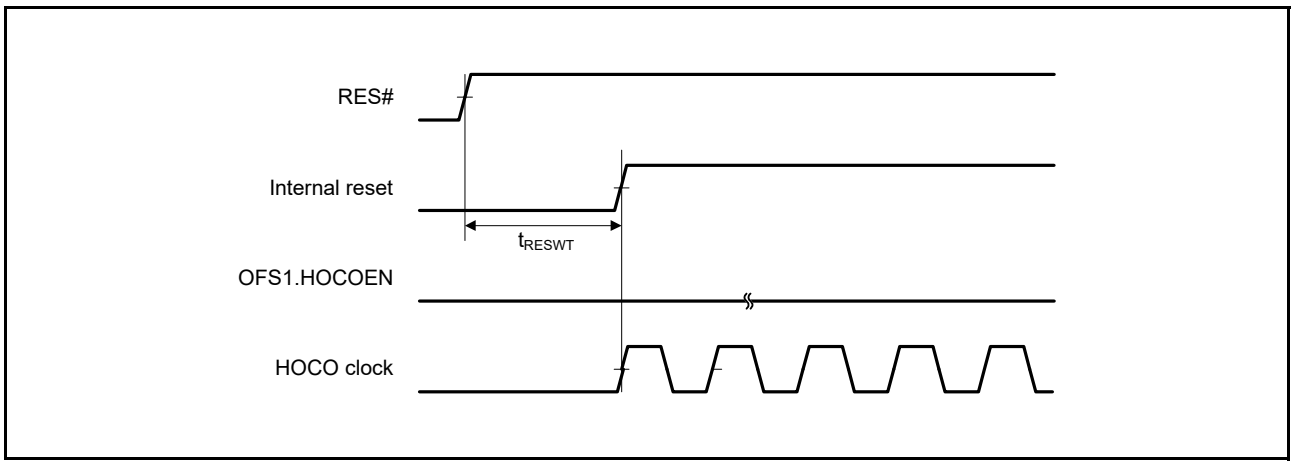


Figure 37.23 HOCO Clock Oscillation Start Timing (After Reset is Canceled by Setting OFS1.HOCOEN Bit to 0)

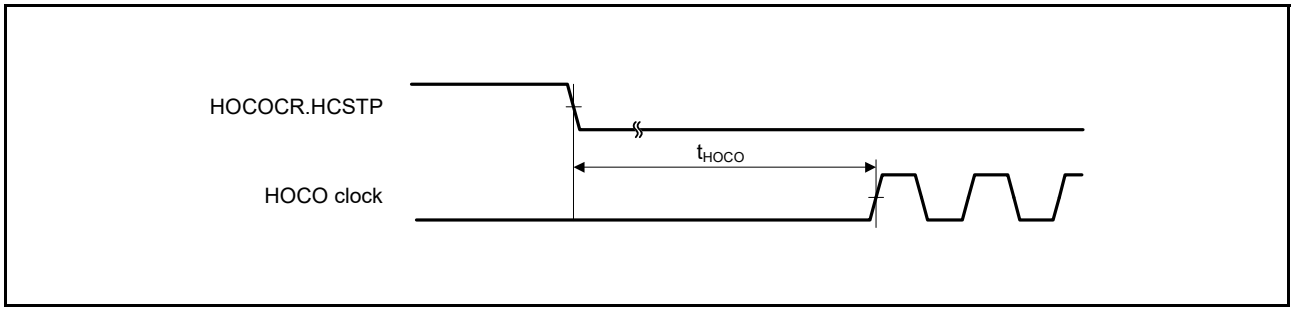


Figure 37.24 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting HOCOCR.HCSTP Bit)

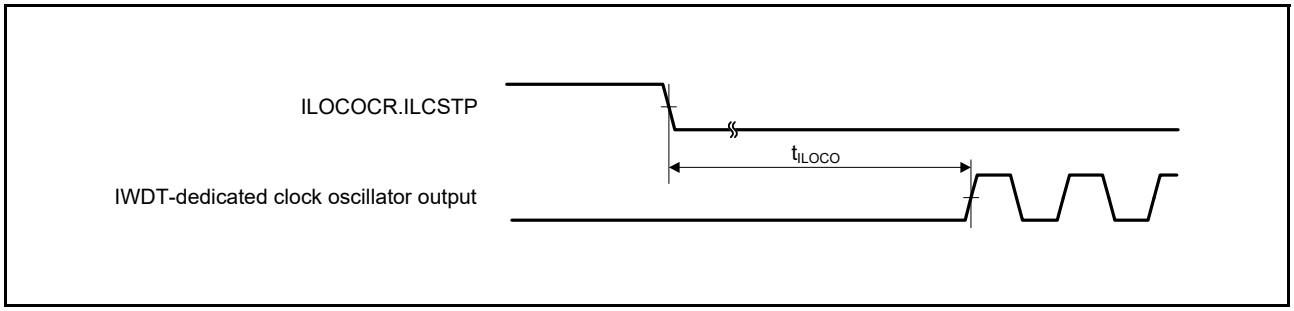


Figure 37.25 IWDT-Dedicated Clock Oscillation Start Timing

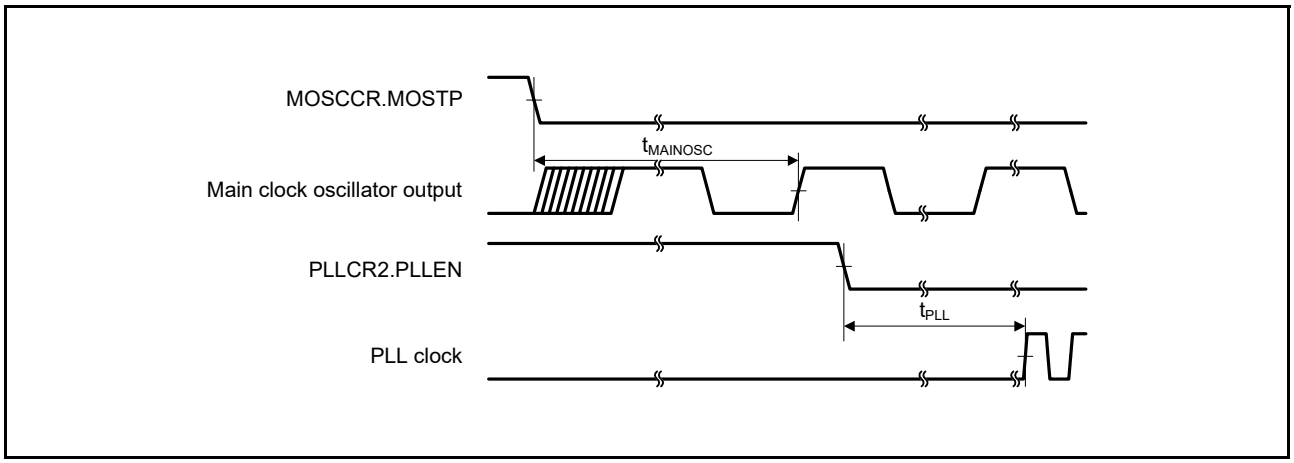


Figure 37.26 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Settled)

37.3.2 Reset Timing

Table 37.17 Reset Timing

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RES# pulse width	At power-on	t_{RESWP}	3	—	—	ms	Figure 37.27
	Other than above	t_{RESW}	30	—	—	µs	Figure 37.28
Wait time after RES# cancellation (at power-on)		t_{RESWT}	—	27.5	—	ms	Figure 37.27
Wait time after RES# cancellation (during powered-on state)		t_{RESWT}	—	114	—	µs	Figure 37.28
Independent watchdog timer reset period		t_{RESWIW}	—	1	—	IWDT clock cycle	Figure 37.29
Software reset period		t_{RESWSW}	—	1	—	ICLK cycle	
Wait time after independent watchdog timer reset cancellation*1		t_{RESW2}	—	300	—	µs	
Wait time after software reset cancellation		t_{RESW2}	—	168	—	µs	

Note 1. When IWDTCR.CKS[3:0] = 0000b.

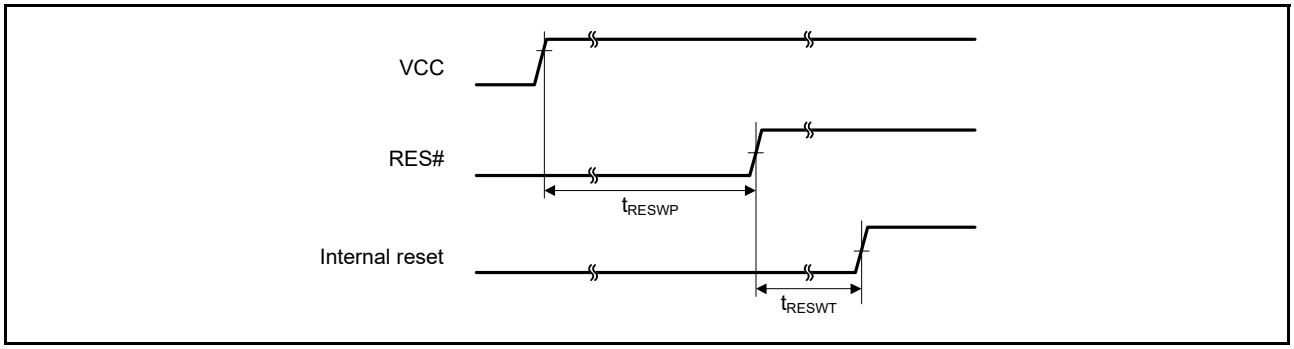


Figure 37.27 Reset Input Timing at Power-On

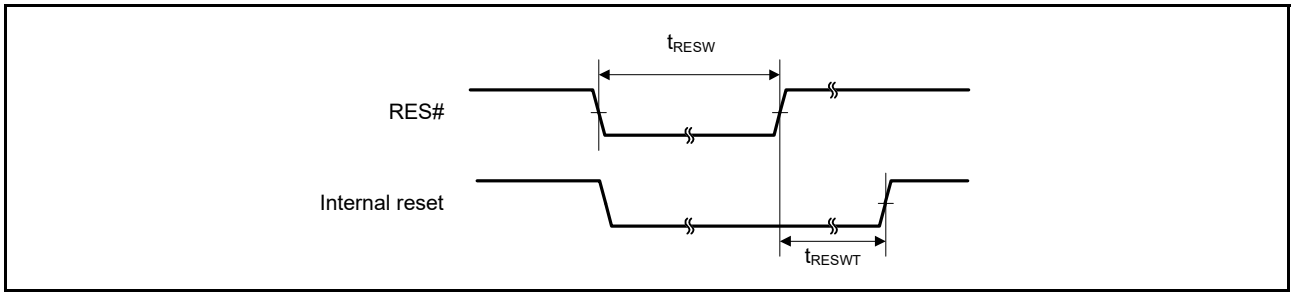


Figure 37.28 Reset Input Timing (1)

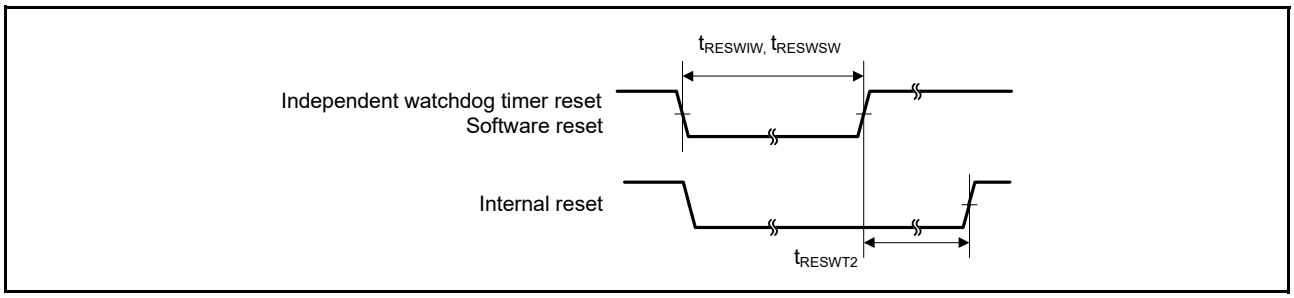


Figure 37.29 Reset Input Timing (2)

37.3.3 Timing of Recovery from Low Power Consumption Modes

Table 37.18 Timing of Recovery from Low Power Consumption Modes (1)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from software standby mode*1	High-speed mode	Crystal connected to main clock oscillator	Main clock oscillator operating*2	t_{SBYMC}	—	2	3	ms	Figure 37.30
			Main clock oscillator and PLL circuit operating*3	t_{SBYPC}	—	2	3	ms	
		External clock input to main clock oscillator	Main clock oscillator operating*4	t_{SBYEX}	—	35	50	µs	
			Main clock oscillator and PLL circuit operating*5	t_{SBYPE}	—	70	95	µs	
		HOCO clock operation	HOCO clock oscillator operation 1 *6	t_{SBYHO}	—	40	55	µs	
			HOCO clock oscillator operation 2 *7		—	75	90	µs	
			HOCO clock oscillator, PLL circuit operation*8	t_{SBYPH}	—	110	130	µs	
		LOCO clock oscillator operating*9		t_{SBYLO}	—	40	55	µs	

Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. The recovery time when multiple oscillators are operating varies depending on the operating state of the oscillators that are not selected as the system clock source. The above table applies when only the corresponding clock is operating.
Note 2. When the frequency of crystal is 20 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.
When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are not divided.
Note 3. When the frequency of PLL is 80 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.
When the frequencies of ICLK and PCLKA are set to 80 MHz, PCLKB and PCLKD are set to 40 MHz, and FCLK is set to 20 MHz.
Note 4. When the frequency of the external clock is 20 MHz.
When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are not divided.
Note 5. When the frequency of PLL is 80 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.
When the frequencies of ICLK and PCLKA are set to 80 MHz, PCLKB and PCLKD are set to 40 MHz, and FCLK is set to 20 MHz.
Note 6. When the frequency of the high-speed on-chip oscillator is 32 MHz. When the high-speed on-chip oscillator wait control register (HOCOWTCR) is set to 05h. When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are not divided.
Note 7. When the frequency of the high-speed on-chip oscillator is 64 MHz. Set the high-speed on-chip oscillator wait control register (HOCOWTCR) is set to 06h. When the frequencies of ICLK and PCLKA are set to 64 MHz, and the frequencies of PCLKB, PCLKD, and FCLK are set to 32 MHz.
Note 8. When the frequency of the high-speed on-chip oscillator is 32 MHz, and the frequency of PLL is 80 MHz. When the high-speed on-chip oscillator wait control register (HOCOWTCR) is set to 05h. When the frequencies of ICLK and PCLKA are set to 80 MHz, the frequencies of PCLKB and PCLKD are set to 40 MHz, and the frequency of FCLK is set to 20MHz.
Note 9. When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are not divided.

Table 37.19 Timing of Recovery from Low Power Consumption Modes (2)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from software standby mode*1	Middle-speed mode	Crystal connected to main clock oscillator	Main clock oscillator operating*2	t_{SBYMC}	—	2	3	ms	Figure 37.30
			Main clock oscillator and PLL circuit operating*3	t_{SBYPC}	—	2	3	ms	
		External clock input to main clock oscillator	Main clock oscillator operating*4	t_{SBYEX}	—	3	4	µs	
			Main clock oscillator and PLL circuit operating*5	t_{SBYPE}	—	65	85	µs	
		HOCO clock oscillator operating	HOCO clock oscillator operating 1 *6	t_{SBYHO}	—	40	50	µs	
			HOCO clock oscillator operating 2 *7		—	75	85	µs	
			HOCO clock oscillator and PLL circuit operating*8	t_{SBYPH}	—	110	125	µs	
		LOCO clock oscillator operating*9		t_{SBYLO}	—	5	7	µs	

Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. The recovery time when multiple oscillators are operating varies depending on the operating state of the oscillators that are not selected as the system clock source. The above table applies when only the corresponding clock is operating.

Note 2. When the frequency of the crystal is 12 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.
When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are not divided.

Note 3. When the frequency of PLL is 48 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.
When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are set to 12 MHz.

Note 4. When the frequency of the external clock is 12 MHz.
When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are not divided.

Note 5. When the frequency of PLL is 48 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.
When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are set to 12 MHz.

Note 6. When the frequency of the high-speed on-chip oscillator is 32 MHz. When the high-speed on-chip oscillator wait control register (HOCOWTCR) is set to 05h. When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are set to 8 MHz.

Note 7. When the frequency of the high-speed on-chip oscillator is 64 MHz. Set the high-speed on-chip oscillator wait control register (HOCOWTCR) is set to 06h. When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are set to 8 MHz.

Note 8. When the frequency of the high-speed on-chip oscillator is 32 MHz, and the frequency of PLL is 80 MHz. When the high-speed on-chip oscillator wait control register (HOCOWTCR) is set to 05h. When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are set to 10 MHz.

Note 9. When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are not divided.

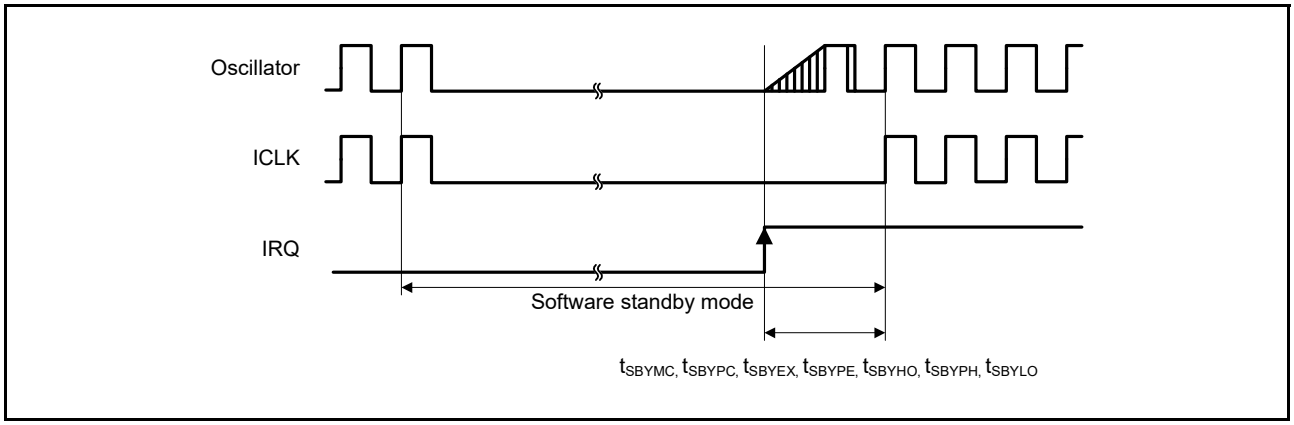


Figure 37.30 Software Standby Mode Recovery Timing

Table 37.20 Timing of Recovery from Low Power Consumption Modes (3)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from deep sleep mode*1	High-speed mode*2	t_{DSLP}	—	2	3.5	µs	Figure 37.31
	Middle-speed mode*3	t_{DSLP}	—	3	4	µs	

Note 1. Oscillators continue oscillating in deep sleep mode.
Note 2. When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are 32 MHz.
Note 3. When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are 12 MHz.

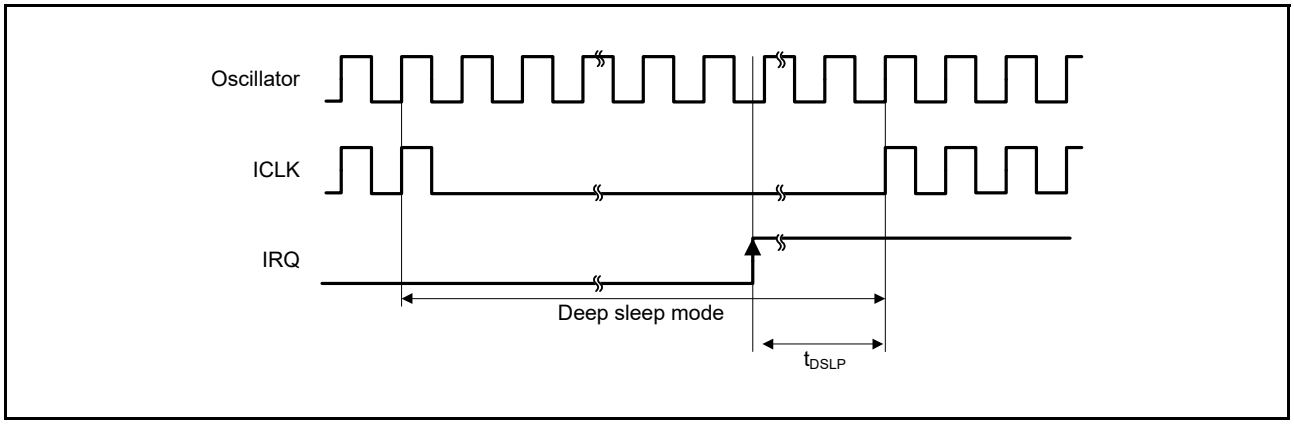


Figure 37.31 Deep Sleep Mode Recovery Timing

Table 37.21 Operating Mode Transition Time

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Mode before Transition	Mode after Transition	ICLK Frequency	Transition Time			Unit
			Min.	Typ.	Max.	
High-speed operating mode	Middle-speed operating modes	8 MHz	—	10	—	µs
Middle-speed operating modes	High-speed operating mode	8 MHz	—	37.5	—	µs

Note: Values when the frequencies of PCLKA, PCLKB, PCLKD, and FCLK are not divided.

37.3.4 Control Signal Timing

Table 37.22 Control Signal Timing

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter disabled (NMIFLTE.NFLTEN = 0)	$t_{Pcyc} \times 2 \le 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		NMI digital filter enabled (NMIFLTE.NFLTEN = 1)	$t_{NMICK} \times 3 \le 200$ ns
		$t_{NMICK} \times 3.5$*2	—	—			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter disabled (IRQFLTE0.FLTENi = 0)	$t_{Pcyc} \times 2 \le 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		IRQ digital filter enabled (IRQFLTE0.FLTENi = 1)	$t_{IRQCK} \times 3 \le 200$ ns
		$t_{IRQCK} \times 3.5$*3	—	—			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in software standby mode.
Note 1. t_{Pcyc} indicates the cycle of PCLKB.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).

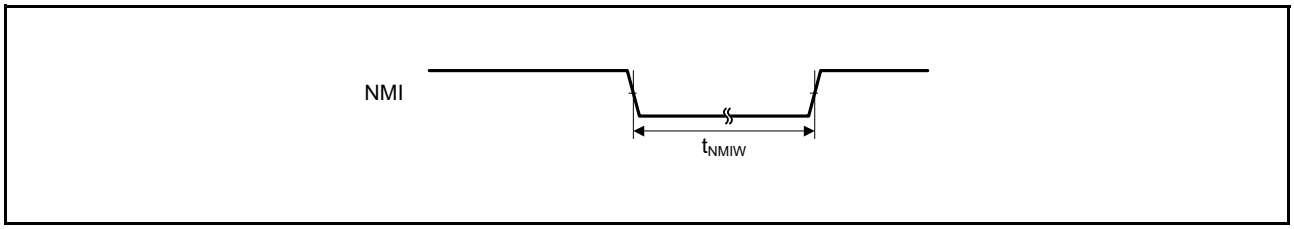


Figure 37.32 NMI Interrupt Input Timing

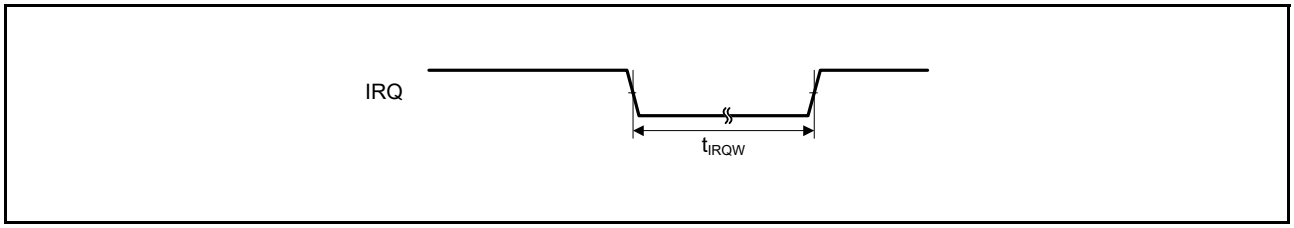


Figure 37.33 IRQ Interrupt Input Timing

37.3.5 Timing of On-Chip Peripheral Modules

Table 37.23 Timing of On-Chip Peripheral Modules (1)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item				Symbol	Min.	Max.	Unit *1	Test Conditions
I/O ports	Input data pulse width			t_{PRW}	1.5	—	t_{Pcyc}	Figure 37.34
MTU3	Input capture input pulse width		Single-edge setting	t_{TICW}	1.5	—	t_{PAcyc}	Figure 37.35
			Both-edge setting		2.5	—		
	Timer clock pulse width		Single-edge setting	t_{TCKWH}, t_{TCKWL}	1.5	—	t_{PAcyc}	Figure 37.36
			Both-edge setting		2.5	—		
			Phase counting mode		2.5	—		
POE3	POE# input pulse width			t_{POEW}	1.5	—	t_{Pcyc}	Figure 37.37
GPT	Input capture input pulse width		Single-edge setting	t_{GTICW}	1.5	—	t_{PAcyc}	Figure 37.38
			Both-edge setting		2.5	—		
	External trigger input pulse width		Single-edge setting	t_{GTETW}	1.5	—	t_{PAcyc}	Figure 37.39
			Both-edge setting		2.5	—		
	Timer clock pulse width			t_{GTCKWH}	1.5	—	t_{PAcyc}	Figure 37.40
				t_{GTCKWL}				
TMR	Timer clock pulse width		Single-edge setting	t_{TMCWH}, t_{TMCWL}	1.5	—	t_{Pcyc}	Figure 37.41
			Both-edge setting		2.5	—		
SCI1, SCI5, SCI6, SCI8, SCI9	Input clock cycle		Asynchronous	t_{Scyc}	4	—	t_{Pcyc}	Figure 37.42
			Clock synchronous		6	—		
	Input clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time			t_{SCKr}	—	20	ns	
	Input clock fall time			t_{SCKf}	—	20	ns	
	Output clock cycle		Asynchronous	t_{Scyc}	16	—	t_{Pcyc}	Figure 37.43
			Clock synchronous		4	—		
	Output clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time			t_{SCKr}	—	20	ns	
	Output clock fall time			t_{SCKf}	—	20	ns	
	Transmit data delay time (master)	Clock synchronous		t_{TXD}	—	40	ns	
	Transmit data delay time (slave)	Clock synchronous	VCC = 4.0 V or above		—	40	ns	
			VCC = 2.7 V or above		—	65	ns	
	Receive data setup time (master)	Clock synchronous	VCC = 4.0 V or above	t_{RXS}	40	—	ns	
			VCC = 2.7 V or above		65	—	ns	
	Receive data setup time (slave)	Clock synchronous			40	—	ns	
	Receive data hold time	Clock synchronous		t_{RXH}	40	—	ns	
A/D converter	Trigger input pulse width			t_{TRGW}	1.5	—	t_{Pcyc}	Figure 37.44
CAC	CACREF input pulse width		$t_{Pcyc} \le t_{cac}$ *2	t_{CACREF}	4.5 t_{cac} + 3 t_{Pcyc}	—	ns	
			$t_{Pcyc} > t_{cac}$ *2		5 t_{cac} + 6.5 t_{Pcyc}			

Note 1. t_{Pcyc}: PCLK cycle, t_{PAcyc}: PCLKA cycle
Note 2. t_{cac}: CAC count clock source cycle

Table 37.24 Timing of On-Chip Peripheral Modules (2)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item				Symbol	Min.	Max.	Unit *1	Test Conditions
SCI11	Input clock cycle		Asynchronous	t_{Scyc}	4	—	t_{PAcyc}	Figure 37.42
			Clock synchronous		6	—		
	Input clock frequency		Asynchronous	t_{Scyc}	—	10	MHz	
			Clock synchronous		—	6.67		
	Input clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time			t_{SCKr}	—	20	ns	
	Input clock fall time			t_{SCKf}	—	20	ns	
	Output clock cycle		Asynchronous	t_{Scyc}	16	—	t_{PAcyc}	Figure 37.43
			Clock synchronous		4	—		
	Output clock frequency		Asynchronous	t_{Scyc}	—	5	MHz	
			Clock synchronous		—	10		
	Output clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time			t_{SCKr}	—	20	ns	
	Output clock fall time			t_{SCKf}	—	20	ns	
	Transmit data delay time (master)	Clock synchronous		t_{TXD}	—	40	ns	
	Transmit data delay time (slave)	Clock synchronous	VCC = 4.0 V or above		—	40	ns	
			VCC = 2.7 V or above		—	65	ns	
	Receive data setup time (master)	Clock synchronous	VCC = 4.0 V or above	t_{RXS}	40	—	ns	
			VCC = 2.7 V or above		65	—	ns	
	Receive data setup time (slave)	Clock synchronous			40	—	ns	
	Receive data hold time	Clock synchronous		t_{RXH}	40	—	ns	

Note 1. t_{Pcyc}: PCLK cycle, t_{PAcyc}: PCLKA cycle

Table 37.25 Timing of On-Chip Peripheral Modules (3)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 =AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C, C = 30 pF

Item				Symbol	Min.	Max.	Unit*1	Test Conditions
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{Pcyc}	Figure 37.45
		Slave			6	—		
	RSPCK clock high pulse width	Master	VCC = 4.0 V or above	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 5$	—	ns	
			VCC = 2.7 V or above		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 8$	—		
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock low pulse width	Master	VCC = 4.0 V or above	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 5$	—	ns	
			VCC = 2.7 V or above		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 8$	—		
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock rise/fall time	Output	VCC = 4.0 V or above	t_{SPCKr}, t_{SPCKf}	—	6	ns	
			VCC = 2.7 V or above		—	10		
		Input			—	0.1	μs/V	
	Data input setup time	Master	VCC = 4.0 V or above	t_{SU}	10	—	ns	Figure 37.46 to Figure 37.49
			VCC = 2.7 V or above		26	—		
		Slave			20	—		
	Data input hold time	Master	RSPCK set to a division ratio other than PCLKB divided by 2	t_H	t_{Pcyc}	—	ns	
			RSPCK set to PCLKB divided by 2	t_{HF}	0	—		
		Slave		t_H	0	—		
	SSL setup time	Master		t_{LEAD}	–30 + N*2 × t_{SPcyc}	—	ns	
		Slave			6	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	–30 + N*3 × t_{SPcyc}	—	ns	
		Slave			6	—	t_{Pcyc}	
	Data output delay time	Master	VCC = 4.0 V or above	t_{OD}	—	10	ns	
			VCC = 2.7 V or above		—	14		
		Slave			—	65		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave			$6 \times t_{Pcyc}$	—		
	MOSI and MISO rise/fall time	Output		t_{Dr}, t_{Df}	—	10	ns	
		Input			—	1	μs	
	SSL rise/fall time	Output		t_{SSLr}, t_{SSLf}	—	10	ns	
		Input			—	1	μs	
	Slave access time			t_{SA}	—	6	t_{Pcyc}	Figure 37.48, Figure 37.49
	Slave output release time			t_{REL}	—	5	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle
Note 2. N: An integer from 1 to 8 that can be set by the RSPI clock delay register (SPCKD)
Note 3. N: An integer from 1 to 8 that can be set by the RSPI slave select negation delay register (SSLND)

Table 37.26 Timing of On-Chip Peripheral Modules (4)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C, C = 30 pF

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI (SCI1, SCI5, SCI6, SCI8, SCI9)	SCK clock cycle output (master)		t_{SPcyc}	4	65536	t_{Pcyc}	Figure 37.45
	SCK clock cycle input (slave)			6	—	t_{Pcyc}	
	SCK clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time		t_{SPCKr}, t_{SPCKf}	—	20	ns	
	Data input setup time (master)	VCC = 4.0 V or above	t_{SU}	40	—	ns	Figure 37.46, Figure 37.47
		VCC = 2.7 V or above		65	—		
	Data input setup time (slave)			40	—		
	Data input hold time		t_H	40	—	ns	
	SS input setup time		t_{LEAD}	3	—	t_{SPcyc}	
	SS input hold time		t_{LAG}	3	—	t_{SPcyc}	
	Data output delay time (master)		t_{OD}	—	40	ns	
	Data output delay time (slave)	VCC = 4.0 V or above		—	40		
		VCC = 2.7 V or above		—	65		
	Data output hold time	Master	t_{OH}	–10	—	ns	
		Slave		–10	—		
	Data rise/fall time		t_{Dr}, t_{Df}	—	20	ns	
	SS input rise/fall time		t_{SSLr}, t_{SSLf}	—	20	ns	
	Slave access time		t_{SA}	—	6	t_{Pcyc}	Figure 37.48, Figure 37.49
	Slave output release time		t_{REL}	—	6	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle

Table 37.27 Timing of On-Chip Peripheral Modules (5)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C, C = 30 pF

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI (SCI11)	SCK clock cycle output (master)		t_{SPcyc}	4	65536	t_{Pcyc}	Figure 37.45
	SCK clock cycle input (slave)			6	—	t_{Pcyc}	
	SCK clock output frequency (master)		f_{SPcyc}	—	10	MHz	
	SCK clock input frequency (slave)			—	6.67	MHz	
	SCK clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time		t_{SPCKr}, t_{SPCKf}	—	20	ns	
	Data input setup time (master)	VCC = 4.0 V or above	t_{SU}	40	—	ns	Figure 37.46, Figure 37.47
		VCC = 2.7 V or above		65	—		
	Data input setup time (slave)			40	—		
	Data input hold time		t_H	40	—	ns	
	SS input setup time		t_{LEAD}	3	—	t_{SPcyc}	
	SS input hold time		t_{LAG}	3	—	t_{SPcyc}	
	Data output delay time (master)		t_{OD}	—	40	ns	
	Data output delay time (slave)	VCC = 4.0 V or above		—	40		
		VCC = 2.7 V or above		—	65		
	Data output hold time	Master	t_{OH}	–10	—	ns	
		Slave		–10	—		
	Data rise/fall time		t_{Dr}, t_{Df}	—	20	ns	
	SS input rise/fall time		t_{SSLr}, t_{SSLf}	—	20	ns	
	Slave access time	PCLKA ≤ 40MHz	t_{SA}	—	6	t_{PAcyc}	Figure 37.48, Figure 37.49
		PCLKA > 40MHz		—	12	t_{PAcyc}	
	Slave output release time	PCLKA ≤ 40MHz	t_{REL}	—	6	t_{PAcyc}	
		PCLKA > 40MHz		—	12	t_{PAcyc}	

Note 1. t_{Pcyc}: PCLK cycle, t_{PAcyc}: PCLKA cycle

Table 37.28 Timing of On-Chip Peripheral Modules (6)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.*1, *2	Max.	Unit	Test Conditions
RIIC (Standard mode, SMBus)	SCL cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 1300	—	ns	Figure 37.50
	SCL high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA rise time	t_{Sr}	—	1000	ns	
	SCL, SDA fall time	t_{Sf}	—	300	ns	
	SCL, SDA spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA bus free time	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	START condition hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Repeated START condition setup time	t_{STAS}	1000	—	ns	
	STOP condition setup time	t_{STOS}	1000	—	ns	
	Data setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast mode)	SCL cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 600	—	ns	Figure 37.50
	SCL high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA rise time	t_{Sr}	—	300	ns	
	SCL, SDA fall time	t_{Sf}	—	300	ns	
	SCL, SDA spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA bus free time	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	START condition hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Repeated START condition setup time	t_{STAS}	300	—	ns	
	STOP condition setup time	t_{STOS}	300	—	ns	
	Data setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note 1. t_{IICcyc}: RIIC internal reference count clock (IICφ) cycle

Note 2. The value in parentheses is used when the ICMR3.NF[1:0] bits are set to 11b while a digital filter is enabled with the ICFER.NFE bit is 1.

Table 37.29 Timing of On-Chip Peripheral Modules (7)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = 2.7 V to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Max.	Unit	Test Conditions
Simple I²C (Standard mode) (SCI1, SCI5, SCI6, SCI8, SCI9, SCI11)	SDA rise time	t_{Sr}	—	1000	ns	Figure 37.50
	SDA fall time	t_{Sf}	—	300	ns	
	SDA spike pulse removal time	t_{SP}	0	4 × t_{Pcyc}*1	ns	
	Data setup time	t_{SDAS}	250	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*2	—	400	pF	
Simple I²C (Fast mode) (SCI, SCI5, SCI6, SCI8, SCI9, SCI11)	SDA rise time	t_{Sr}	—	300	ns	Figure 37.50
	SDA fall time	t_{Sf}	—	300	ns	
	SDA spike pulse removal time	t_{SP}	0	4 × t_{Pcyc}*1	ns	
	Data setup time	t_{SDAS}	100	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*2	—	400	pF	

Note 1. t_{Pcyc}: PCLKB cycle
Note 2. C_b is the total capacitance of the bus lines.

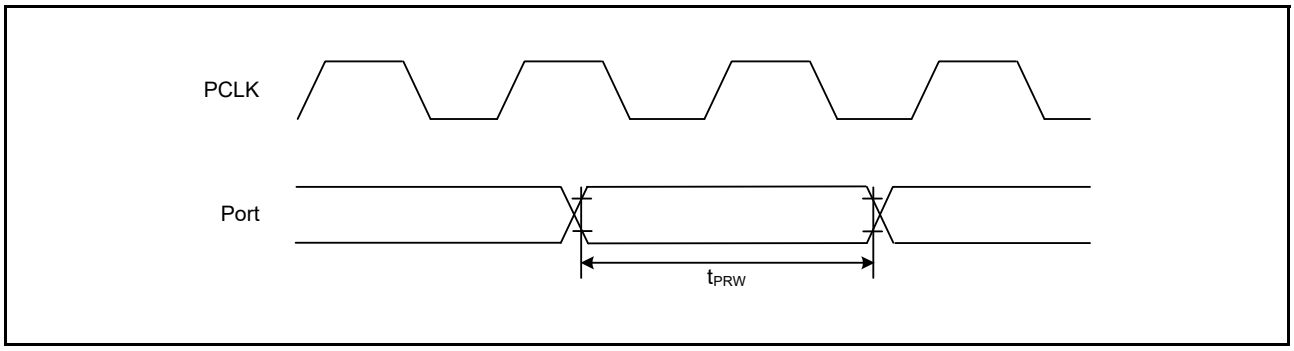


Figure 37.34 I/O Port Input Timing

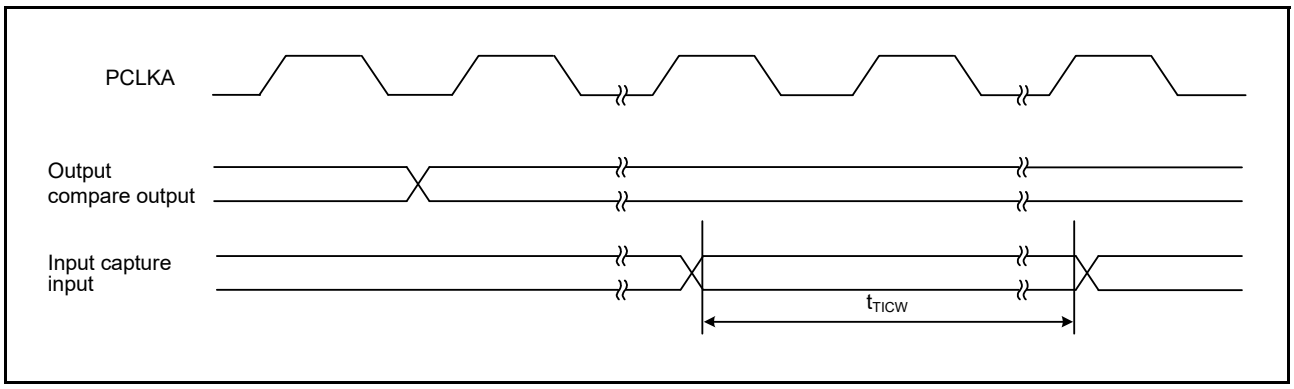


Figure 37.35 MTU3 Input/Output Timing

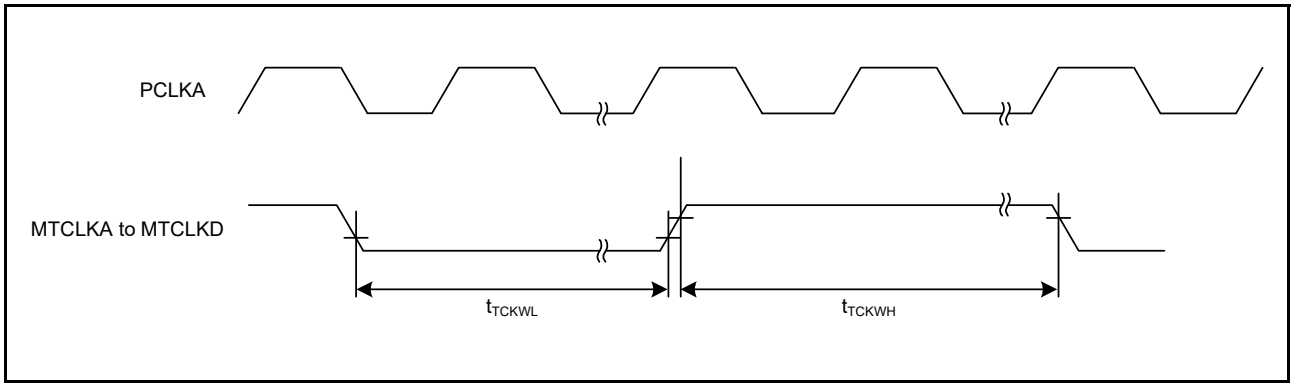


Figure 37.36 MTU3 Clock Input Timing

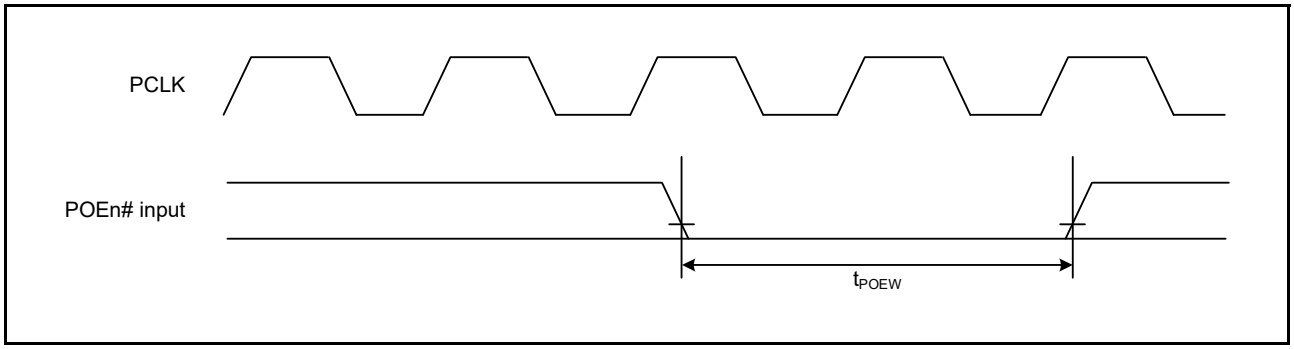


Figure 37.37 POE# Input Timing

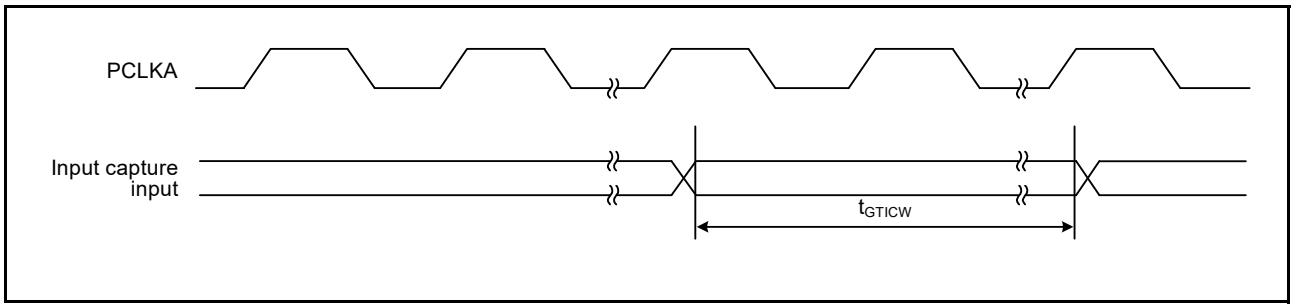


Figure 37.38 Input Timing of GPT Input Capture

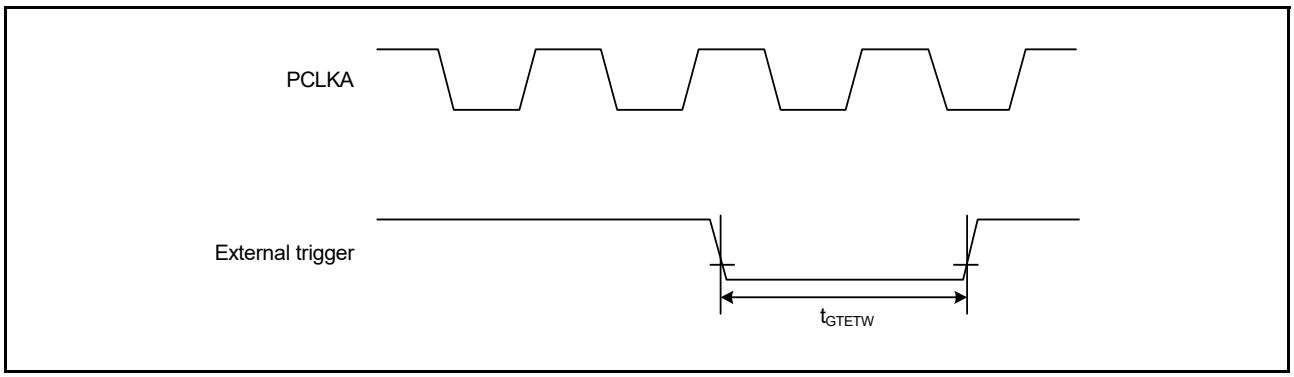


Figure 37.39 Timing of the GPT External Trigger Input

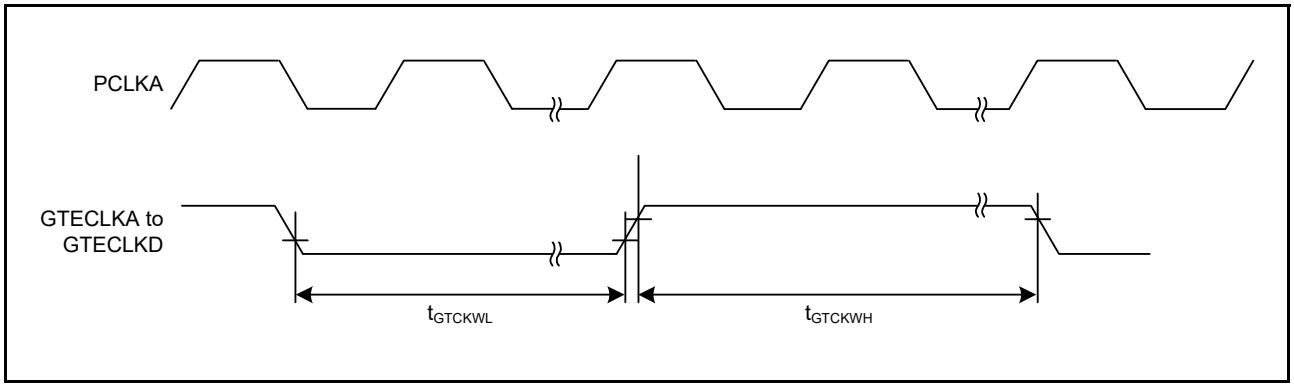


Figure 37.40 GPT Clock Input Timing

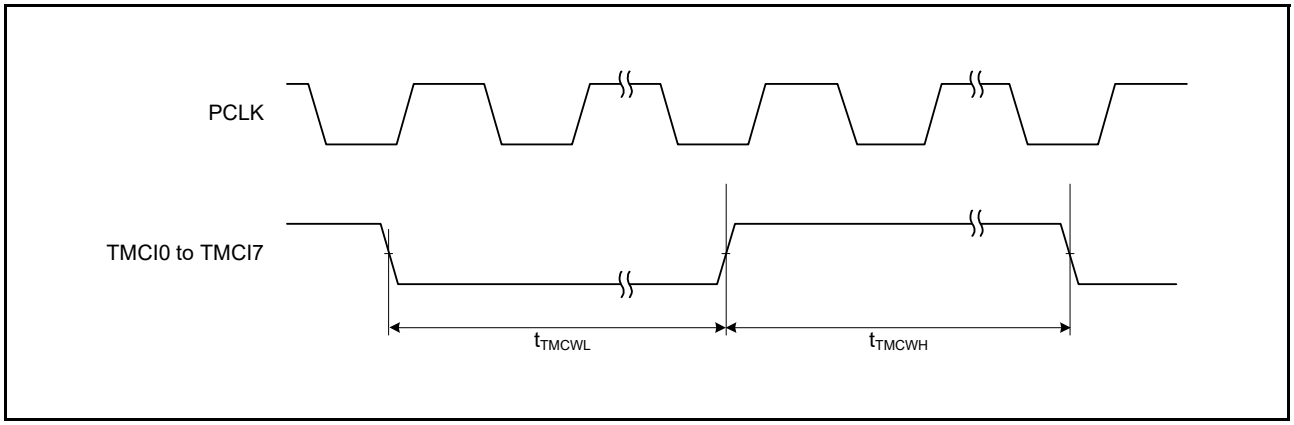


Figure 37.41 TMR Clock Input Timing

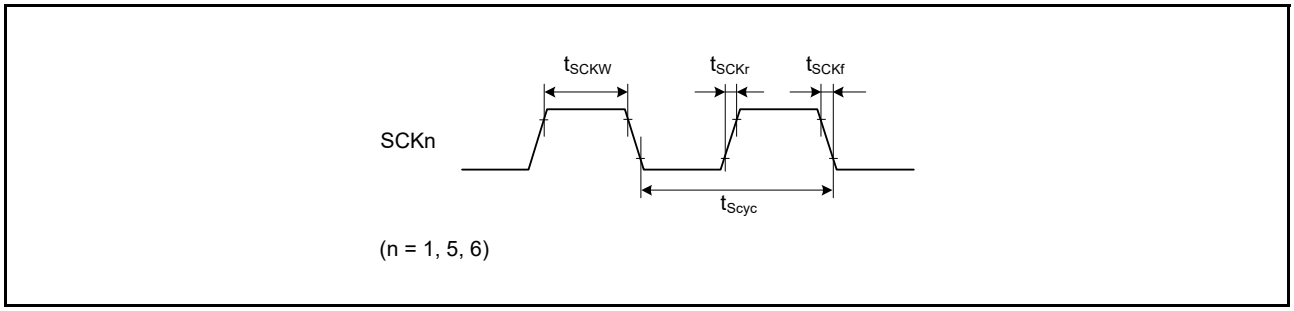


Figure 37.42 SCK Clock Input Timing

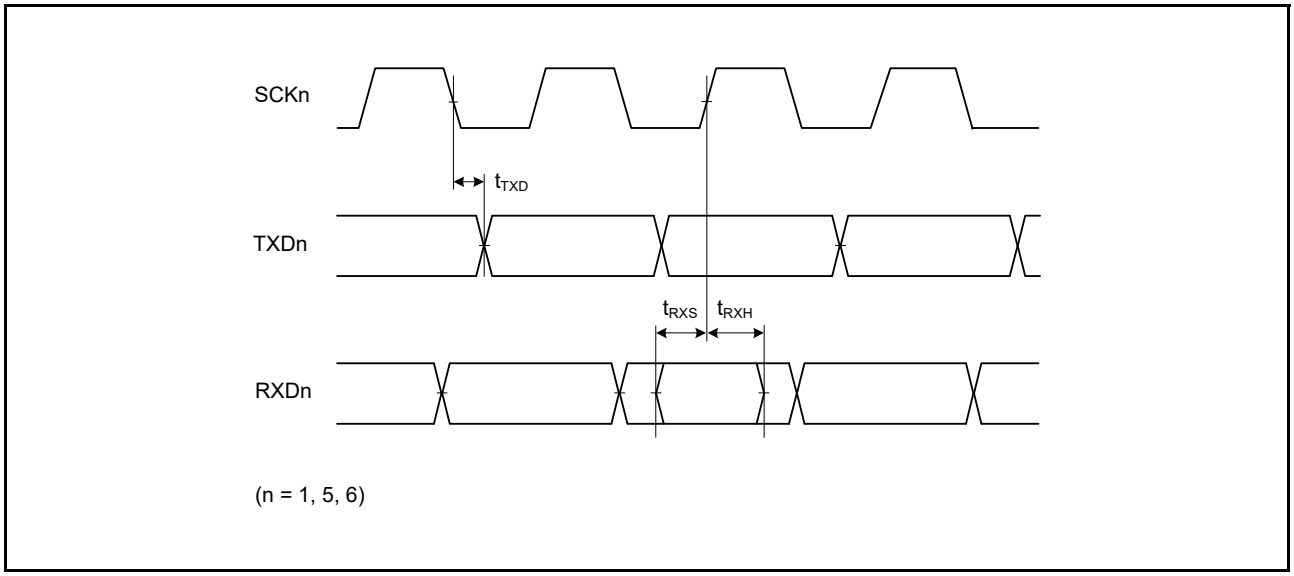


Figure 37.43 SCI Input/Output Timing: Clock Synchronous Mode

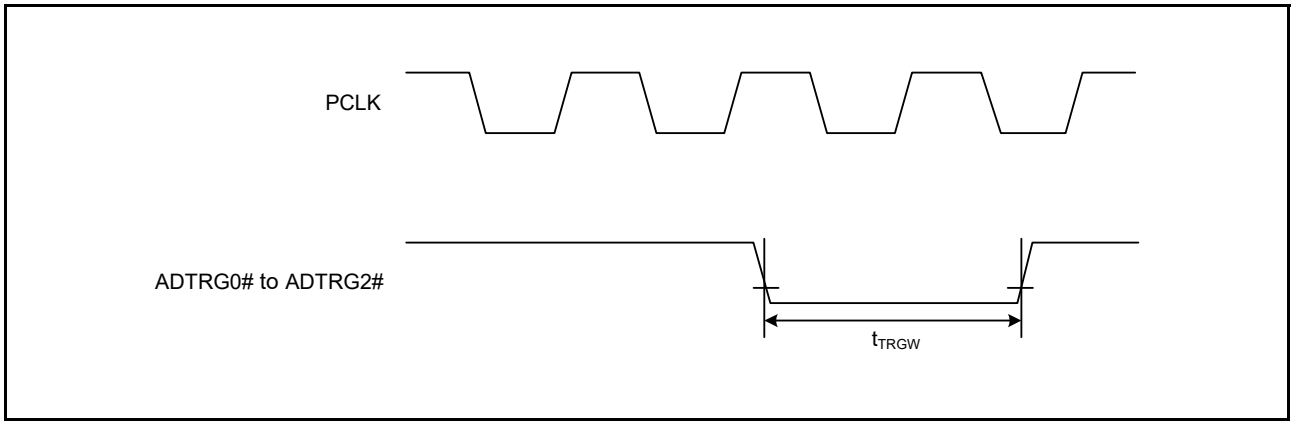


Figure 37.44 A/D Converter External Trigger Input Timing

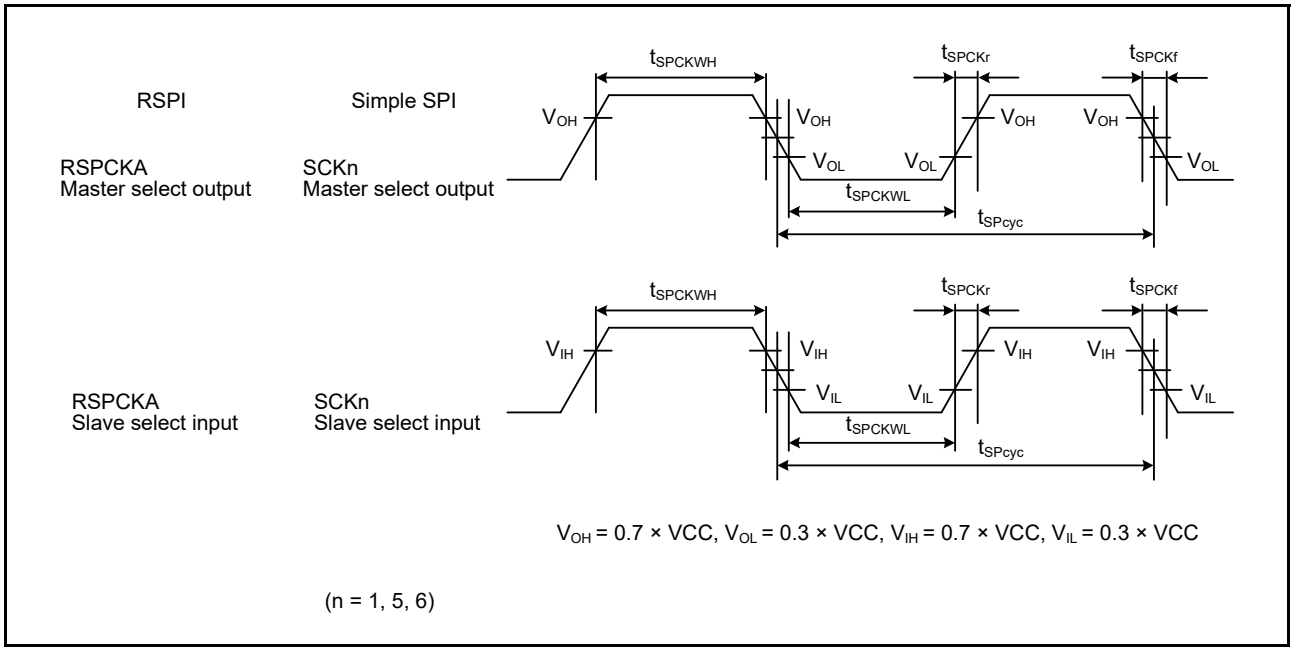


Figure 37.45 RSPI Clock Timing and Simple SPI Clock Timing

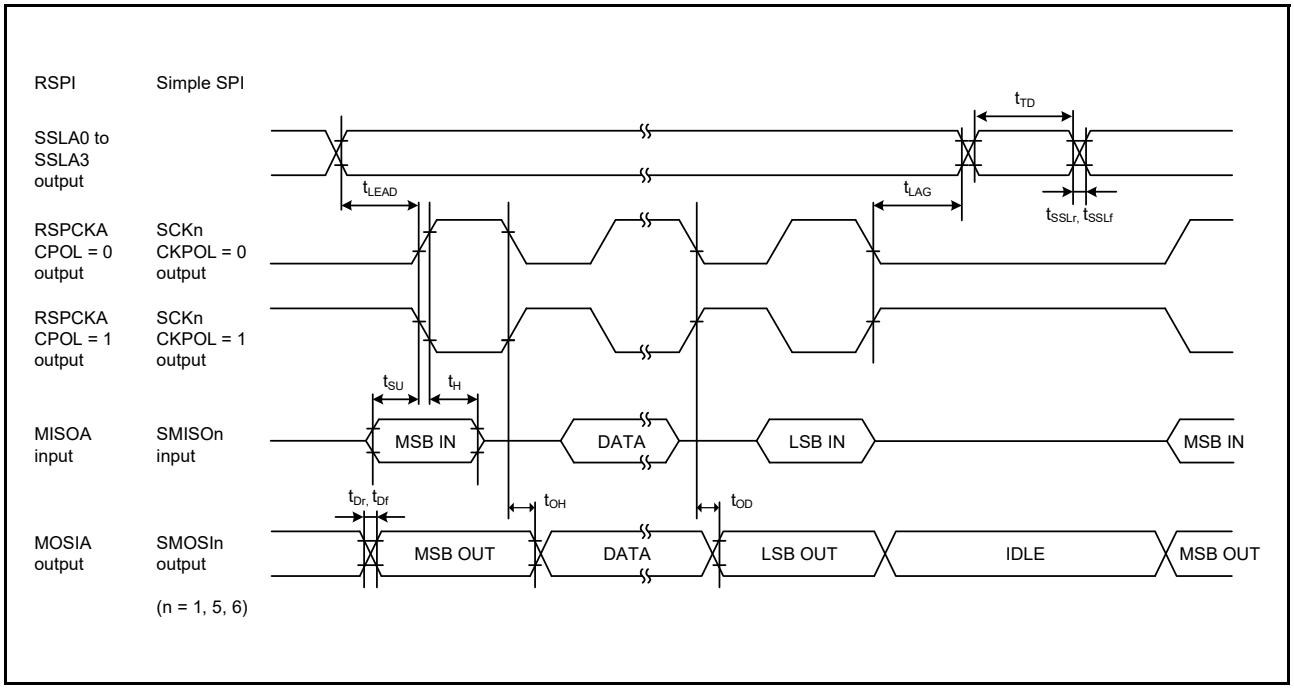


Figure 37.46 RSPI Timing (Master, CPHA = 0) and Simple SPI Clock Timing (Master, CKPH = 1)

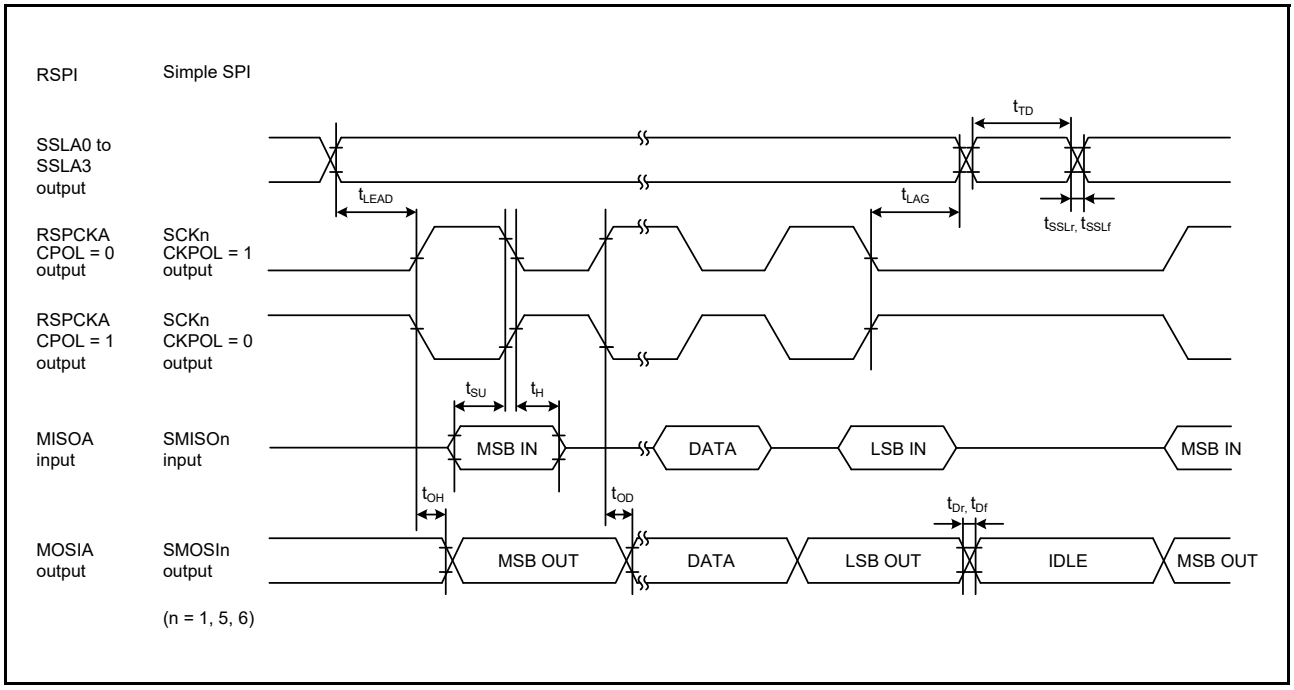


Figure 37.47 RSPI Timing (Master, CPHA = 1) and Simple SPI Clock Timing (Master, CKPH = 0)

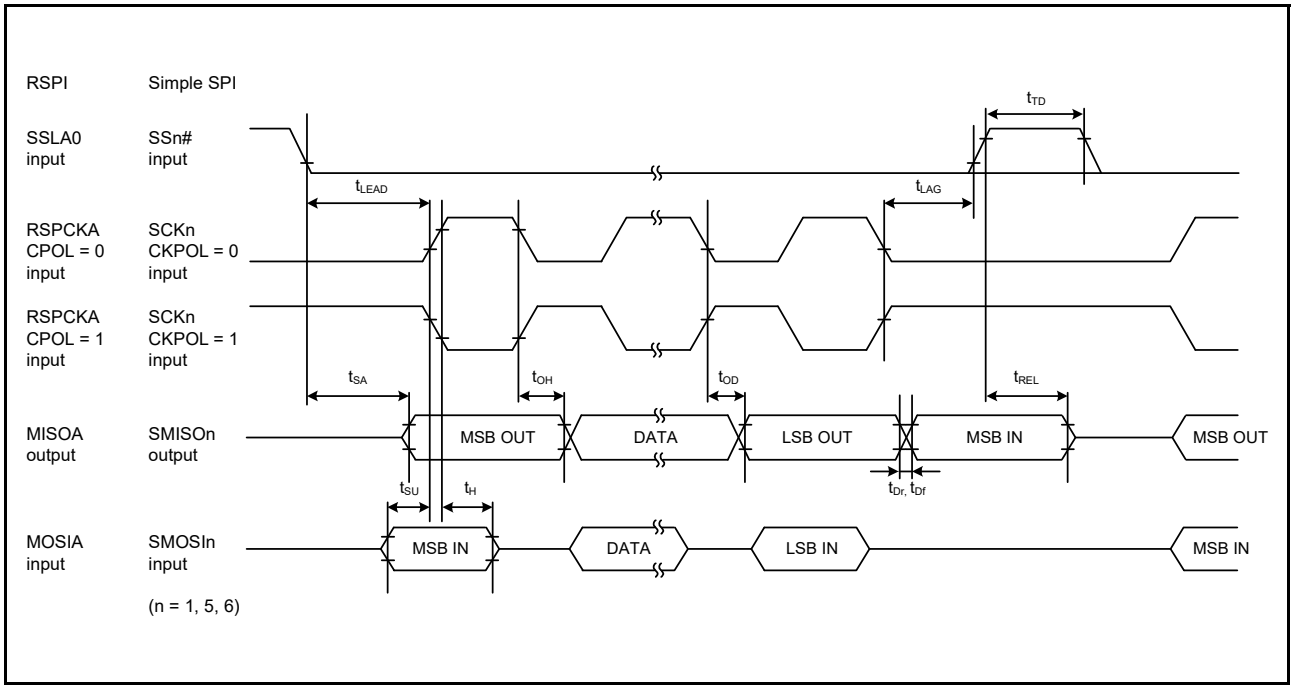


Figure 37.48 RSPI Timing (Slave, CPHA = 0) and Simple SPI Clock Timing (Slave, CKPH = 1)

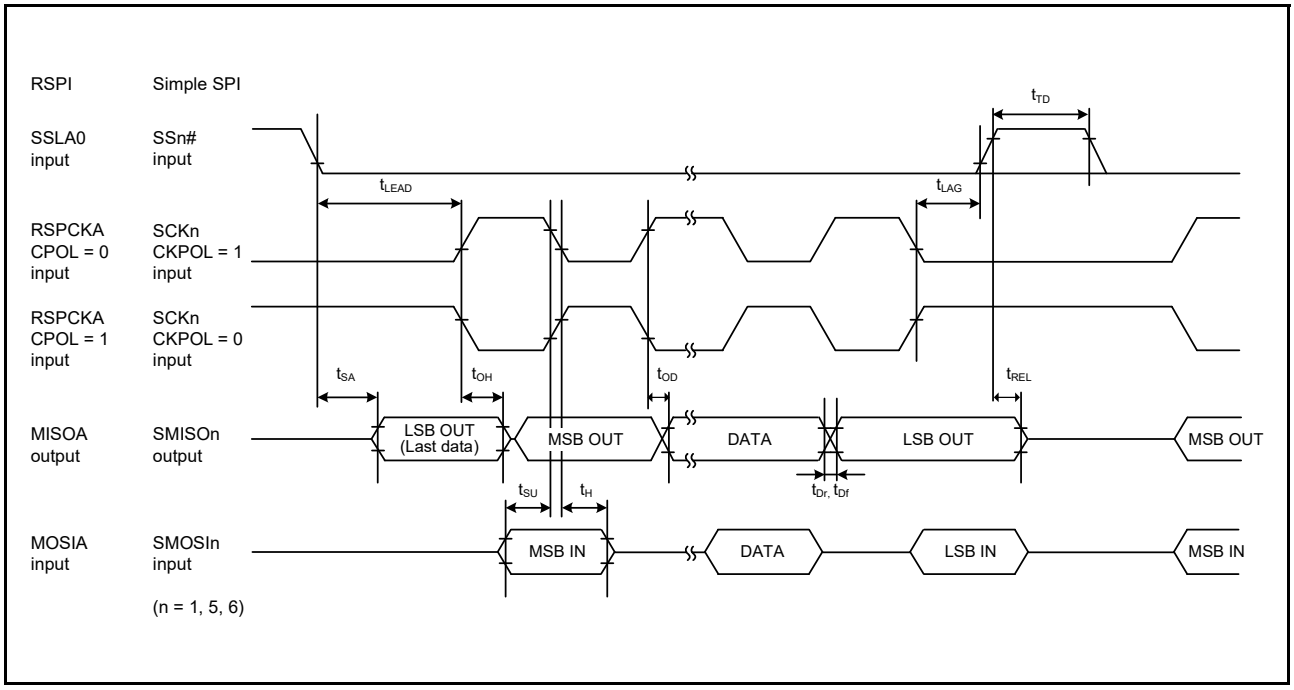
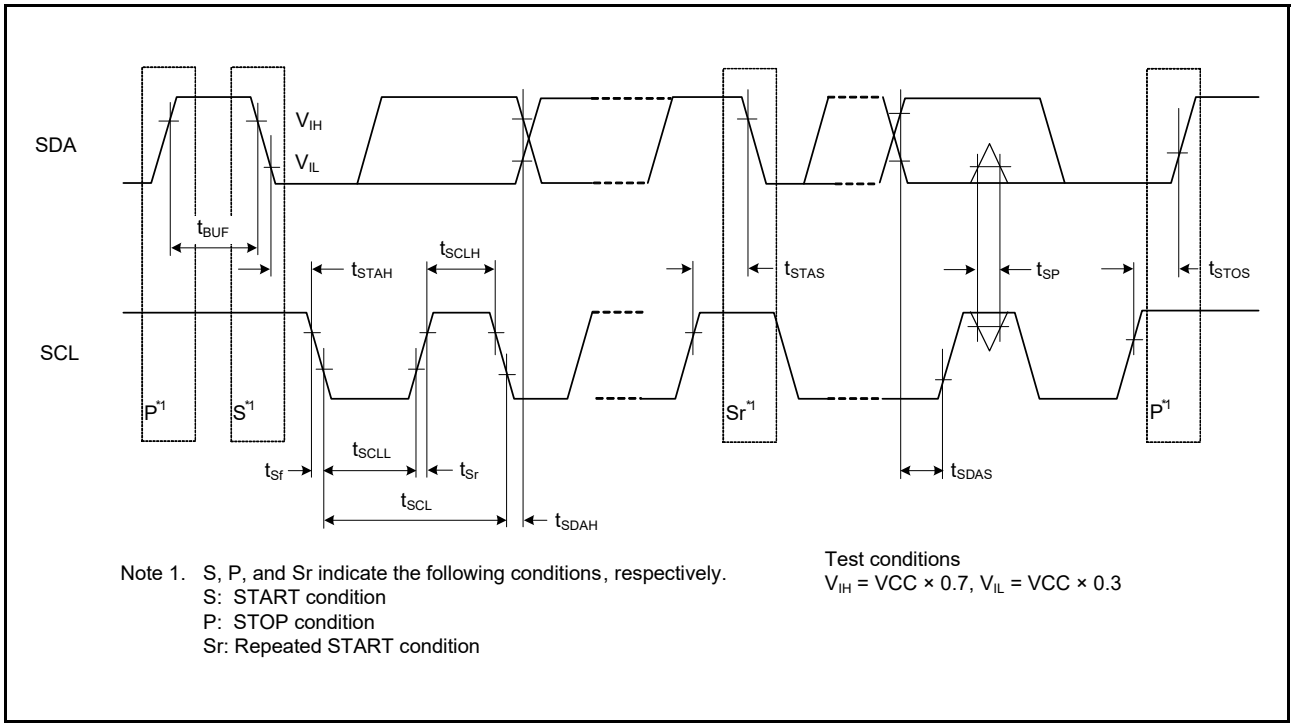


Figure 37.49 RSPI Timing (Slave, CPHA = 1) and Simple SPI Clock Timing (Slave, CKPH = 0)



Note 1. S, P, and Sr indicate the following conditions, respectively.
S: START condition
P: STOP condition
Sr: Repeated START condition

Test conditions
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3

Figure 37.50 RIIC Bus Interface Input/Output Timing and Simple I²C Bus Interface Input/Output Timing

37.4 A/D Conversion Characteristics

Table 37.30 A/D Conversion Characteristics (1)

Conditions: VCC = 4.5 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	40	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 40 MHz)	Permissible signal source impedance (Max.) = 1.0 kΩ Sample-and-hold circuit not in use	1.00	—	—	µs	High-precision channel ADSSTRn.SST[7:0] bits = 08h
		1.25	—	—	µs	Normal-precision channel ADSSTRn.SST[7:0] bits = 12h
	Permissible signal source impedance (Max.) = 1.0 kΩ Sample-and-hold circuit in use	1.65	—	—	µs	High-precision channel ADSSTRn.SST[7:0] bits = 08h ADSHCR.SSTSH[7:0] bits = 0Dh AN100 to 102 = 0.25 V to AVCC1 – 0.25 V
Analog input capacitance		—	—	12	pF	
Offset error		—	±2.0	±6.5	LSB	
Full-scale error		—	±2.0	±6.5	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy	Sample-and-hold circuit in use	—	±2.5	±8.0	LSB	AN100 to 102 = 0.25 V to AVCC1 – 0.25
	Sample-and-hold circuit not in use	—	±3.0	±8.0	LSB	
DNL differential nonlinearity error		—	±0.5	±1.5	LSB	
INL integral nonlinearity error		—	±1.5	±4.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 37.31 A/D Conversion Characteristics (2)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	40	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 40 MHz)	Permissible signal source impedance (Max.) = 1.0 kΩ Sample-and-hold circuit not in use	1.15	—	—	µs	High-precision channel ADSSTRn.SST[7:0] bits = 0Eh
		1.30	—	—	µs	Normal-precision channel ADSSTRn.SST[7:0] bits = 14h
	Permissible signal source impedance (Max.) = 1.0 kΩ Sample-and-hold circuit in use	1.90	—	—	µs	High-precision channel ADSSTRn.SST[7:0] bits = 0Eh ADSHCR.SSTSH[7:0] bits = 11h AN100 to 102 = 0.25 V to AVCC1 – 0.25 V
Analog input capacitance		—	—	12	pF	
Offset error		—	±2.0	±6.5	LSB	
Full-scale error		—	±2.0	±6.5	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±3.0	±8.0	LSB	
DNL differential nonlinearity error		—	±0.5	±1.5	LSB	
INL integral nonlinearity error		—	±1.5	±4.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 37.32 A/D Converter Channel Classification

Classification	Channel	Conditions	Remarks
High-precision channel	AN000 to AN003, AN100 to AN103, AN200 to AN211	AVCC0 = AVCC1 = AVCC2 = 2.7 to 5.5 V	
Normal-precision channel	AN016, AN116	VCC = AVCC0 = AVCC1 =AVCC2 = 2.7 to 5.5 V	
Internal reference voltage input channel	Internal reference voltage	AVCC0 = AVCC1 = AVCC2 = 2.7 to 5.5 V	

Table 37.33 A/D Internal Reference Voltage Characteristics

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item	Min.	Typ.	Max.	Unit	Test Conditions
Internal reference voltage input channel*1	1.35	1.43	1.50	V	

Note 1. The A/D internal reference voltage indicates the voltage when the internal reference voltage is input to the A/D converter.

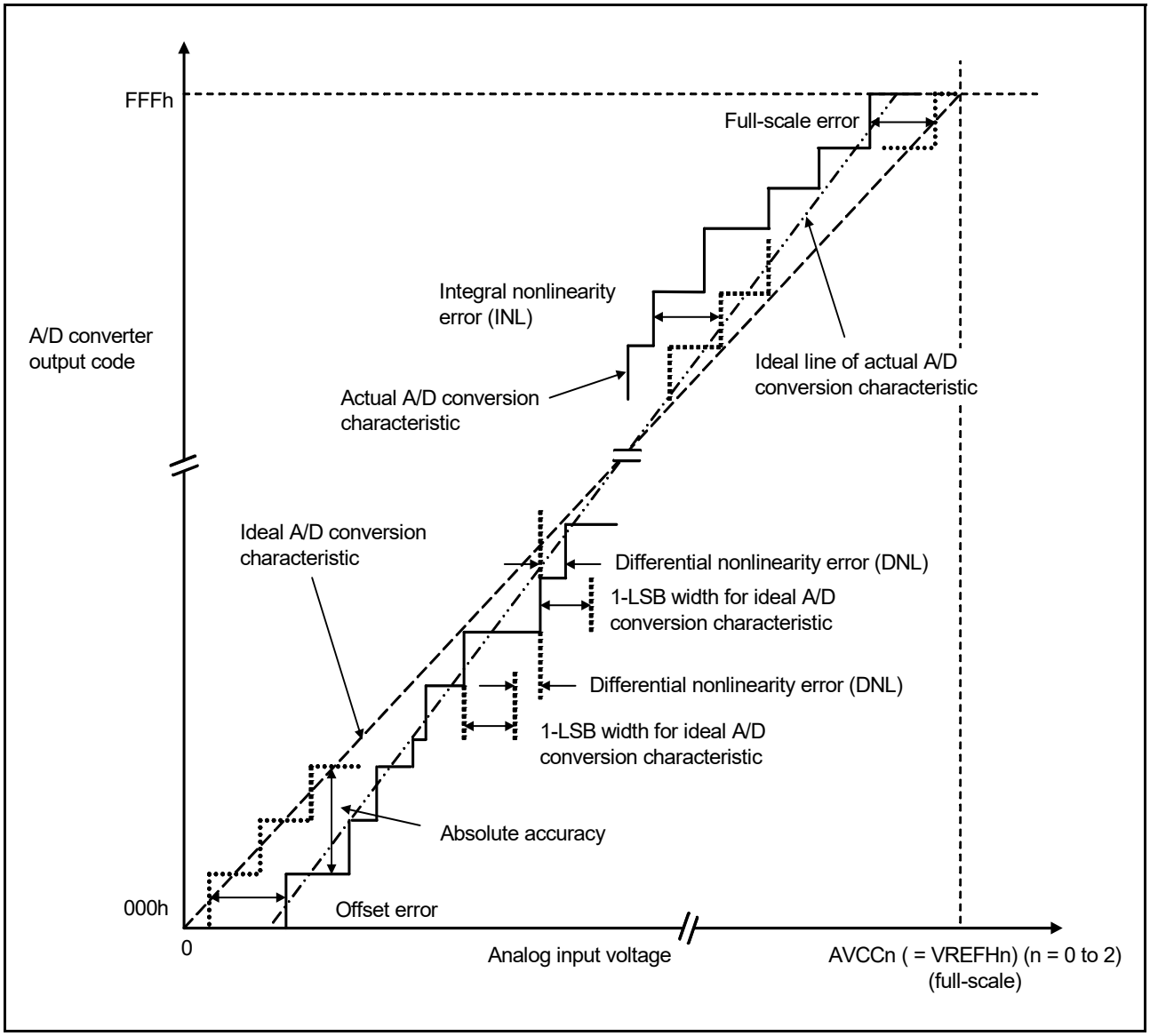


Figure 37.51 Illustration of A/D Converter Characteristic Terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of analog input voltage (1-LSB width), that can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and if reference voltage (AVCCn (= VREFHn) (n = 0 to 2)) is 3.072 V, then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, 1.5 mV, ... are used as analog input voltages.

If analog input voltage is 6 mV, absolute accuracy = ±5 LSB means that the actual A/D conversion result is in the range of 003h to 00Dh though an output code, 008h, can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

Offset error is the difference between a transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.

37.5 Programmable Gain Amplifier Characteristics

Table 37.34 Programmable Gain Amplifier Characteristics

Conditions: VCC = 2.7 V to AVCC0, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = 4.5 V to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input offset voltage		V_{poff}	—	—	8	mV	
Input voltage range		V_{pin}	(V_{pout} (min) – PGAVSSin)/G + PGAVSSin	—	(V_{pout} (max) – PGAVSSin)/G + PGAVSSin	V	
PGAVSS input voltage range		PGAVSSin	–0.3	—	0.3	V	
Output voltage range	G = 2.000, 2.500, 3.077, 3.636, 4.000, 4.444	V_{pout}	0.1 × AVCC	—	0.9 × AVCC	V	
	G = 5.000, 6.667, 8.000, 10.000, 13.333		0.15 × AVCC	—	0.85 × AVCC		
Gain		G	2.000	—	13.333		
Gain error	G = 2.000, 2.500, 3.077	G_{err}	—	±1.0	±2.0	%	0V ≤ PGAVSS ≤ +0.3V
	G = 3.636, 4.000, 4.444		—	±1.5	±3.0		
	G = 5.000, 6.667, 8.000, 10.000, 13.333		—	±2.0	±4.0		
	G = 2.000, 2.500, 3.077		—	±1.0	±3.0		–0.3V ≤ PGAVSS < 0V
	G = 3.636, 4.000, 4.444		—	±1.5	±4.0		
	G = 5.000, 6.667, 8.000, 10.000, 13.333		—	±2.0	±5.0		
Slew rate		SR	10	—	—	V/µs	
Operation stabilization wait time		t_{start}	—	—	5.0	µs	

37.6 Comparator Characteristics

Table 37.35 Comparator Characteristics

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Offset voltage	V_{cioff}	—	—	40	mV	
Response time	t_{cr}	—	—	200	ns	VOD = 100 mV CMPCTL.CDFS = 0
	t_{cf}	—	—	200	ns	
Stabilization wait time for input selection	t_{cwait}	300	—	—	ns	
Operation stabilization wait time	t_{cmp}		—	1	µs	

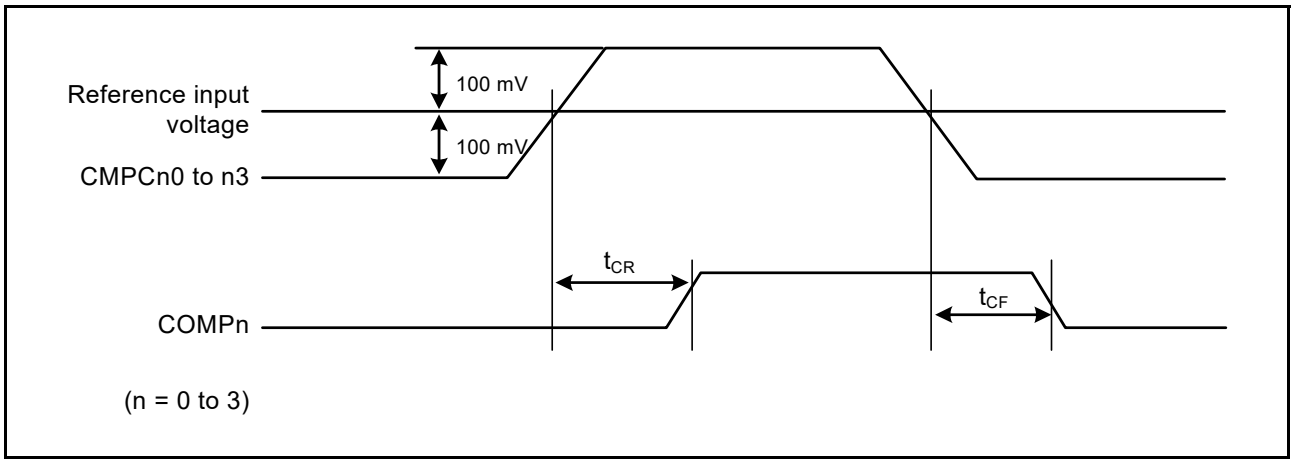


Figure 37.52 Comparator Response Time

37.7 D/A Conversion Characteristics

Table 37.36 D/A Conversion Characteristics

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	—	—	—	8	Bit	
Conversion time	t_{DCONV}	—	—	3.0	µs	
Absolute accuracy	—	—	—	±3.0	LSB	
Output load resistance	—	4	—	—	MΩ	
Output load capacity	—	—	—	35	pF	
Output resistance	—	—	9.0	—	kΩ	

Note: When using ports 23 and 24 as DA0 and DA1 outputs, make sure that VCC ≥ DA output voltage.

37.8 Power-On Reset Circuit and Voltage Detection Circuit Characteristics

Table 37.37 Power-On Reset Circuit and Voltage Detection Circuit Characteristics (1)

Conditions: VCC = 0 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	1.35	1.50	1.65	V	Figure 37.53, Figure 37.54
	Voltage detection circuit (LVD0)*1	V_{det0_0}	3.67	3.84	3.97	V	
		V_{det0_1}	2.70	2.82	3.00		
		V_{det0_2}	2.37	2.51	2.67		
	Voltage detection circuit (LVD1)*2	V_{det1_0}	4.12	4.29	4.42	V	Figure 37.56 At falling edge VCC
		V_{det1_1}	3.98	4.14	4.28		
		V_{det1_2}	3.86	4.02	4.16		
		V_{det1_3}	3.68	3.84	3.98		
		V_{det1_4}	2.99	3.10	3.29		
		V_{det1_5}	2.89	3.00	3.19		
		V_{det1_6}	2.79	2.90	3.09		
		V_{det1_7}	2.68	2.79	2.98		
		V_{det1_8}	2.57	2.68	2.87		
	Voltage detection circuit (LVD2)*3	V_{det2_0}	4.08	4.29	4.48		Figure 37.57 At falling edge VCC
		V_{det2_1}	3.95	4.14	4.35		
		V_{det2_2}	3.82	4.02	4.22		
		V_{det2_3}	3.62	3.84	4.02		

Note: These characteristics apply when noise is not superimposed on the power supply. When a setting is made so that the voltage detection level overlaps with that of the voltage detection circuit (LVD2), it cannot be specified which of LVD1 and LVD2 is used for voltage detection.

Note 1. n in the symbol V_{det0_n} denotes the value of the LVDS0[1:0] bits.

Note 2. n in the symbol V_{det1_n} denotes the value of the LVDLVLR.LVD1LVL[3:0] bits.

Note 3. n in the symbol V_{det2_n} denotes the value of the LVDLVLR.LVD2LVL[3:0] bits.

Table 37.38 Power-On Reset Circuit and Voltage Detection Circuit Characteristics (2)

Conditions: VCC = 0 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Wait time after power-on reset cancellation	At normal startup	t_{POR}	—	28.4	—	ms	Figure 37.54
Wait time after voltage monitoring 0 reset cancellation		t_{LVD0}	—	568	—	µs	Figure 37.55
Wait time after voltage monitoring 1 reset cancellation		t_{LVD1}	—	100	—	µs	Figure 37.56
Wait time after voltage monitoring 2 reset cancellation		t_{LVD2}	—	100	—	µs	Figure 37.57
Response delay time		t_{det}	—	—	350	µs	Figure 37.53
Minimum VCC down time*1		t_{VOFF}	350	—	—	µs	Figure 37.53, VCC = 1.0 V or above
Power-on reset enable time		$t_{W(POR)}$	1	—	—	ms	Figure 37.54, VCC = below 1.0 V
LVD operation stabilization time (after LVD is enabled)		$Td_{(E-A)}$	—	—	300	µs	Figure 37.56, Figure 37.57
Hysteresis width (LVD0, LVD1 and LVD2)		V_{LVH}	—	70	—	mV	Vdet1_0 to 4 selected
			—	60	—		Vdet0_0 to 2 selected Vdet1_5 to 8 selected LVD2 selected

Note: These characteristics apply when noise is not superimposed on the power supply. When a setting is made so that the voltage detection level overlaps with that of the voltage detection circuit (LVD1), it cannot be specified which of LVD1 and LVD2 is used for voltage detection.

Note 1. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{det2} for the POR/LVD.

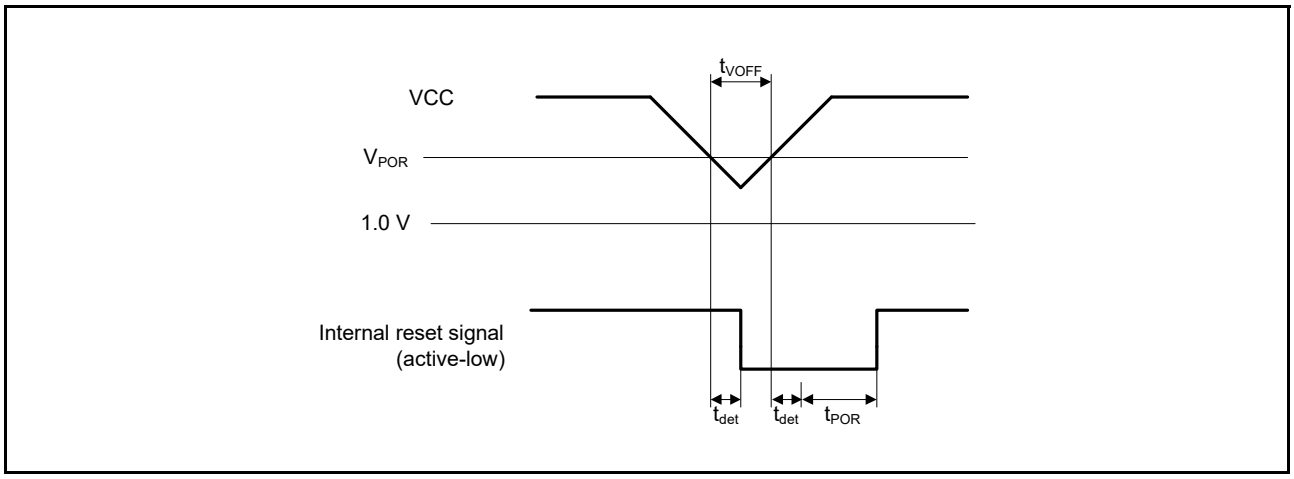
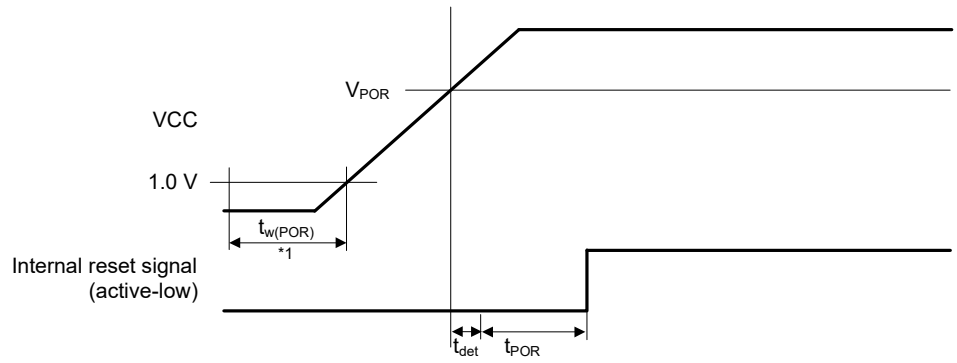


Figure 37.53 Voltage Detection Reset Timing



Note 1. $t_{w(POR)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (1.0 V).
When VCC turns on, maintain $t_{w(POR)}$ for 1.0 ms or more.

Figure 37.54 Power-On Reset Timing

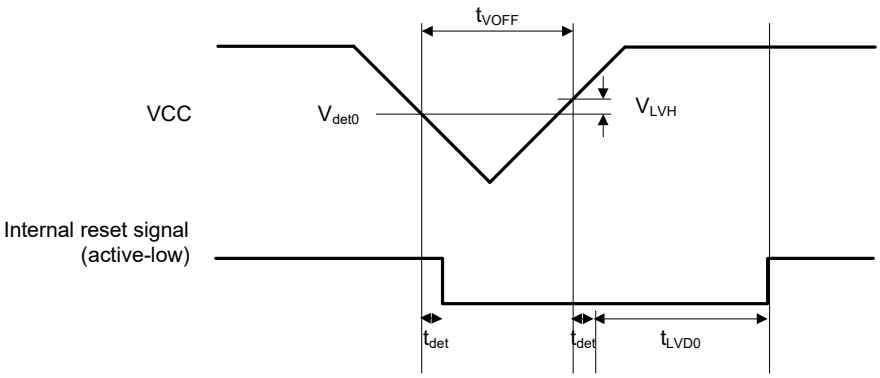


Figure 37.55 Voltage Detection Circuit Timing (V_{det0})

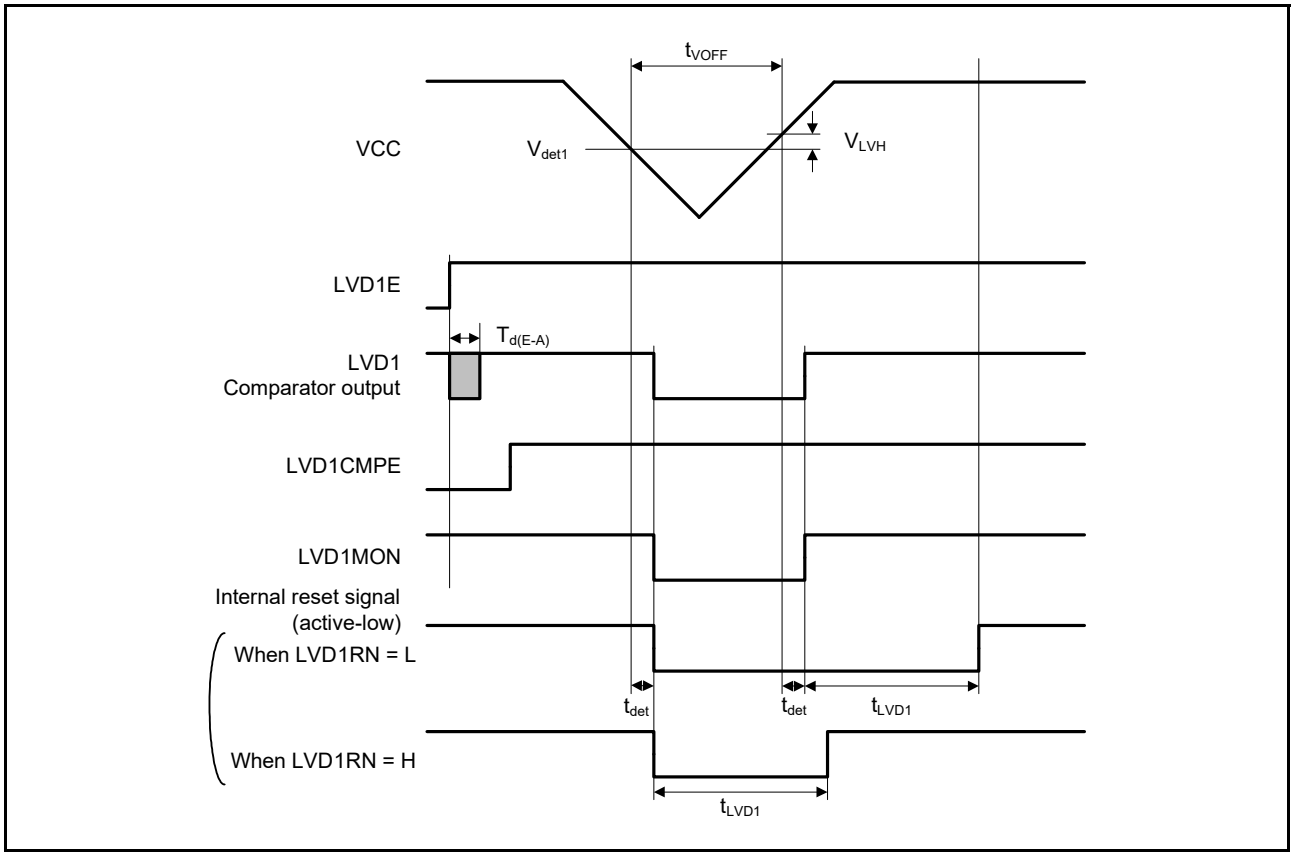


Figure 37.56 Voltage Detection Circuit Timing (V_{det1})

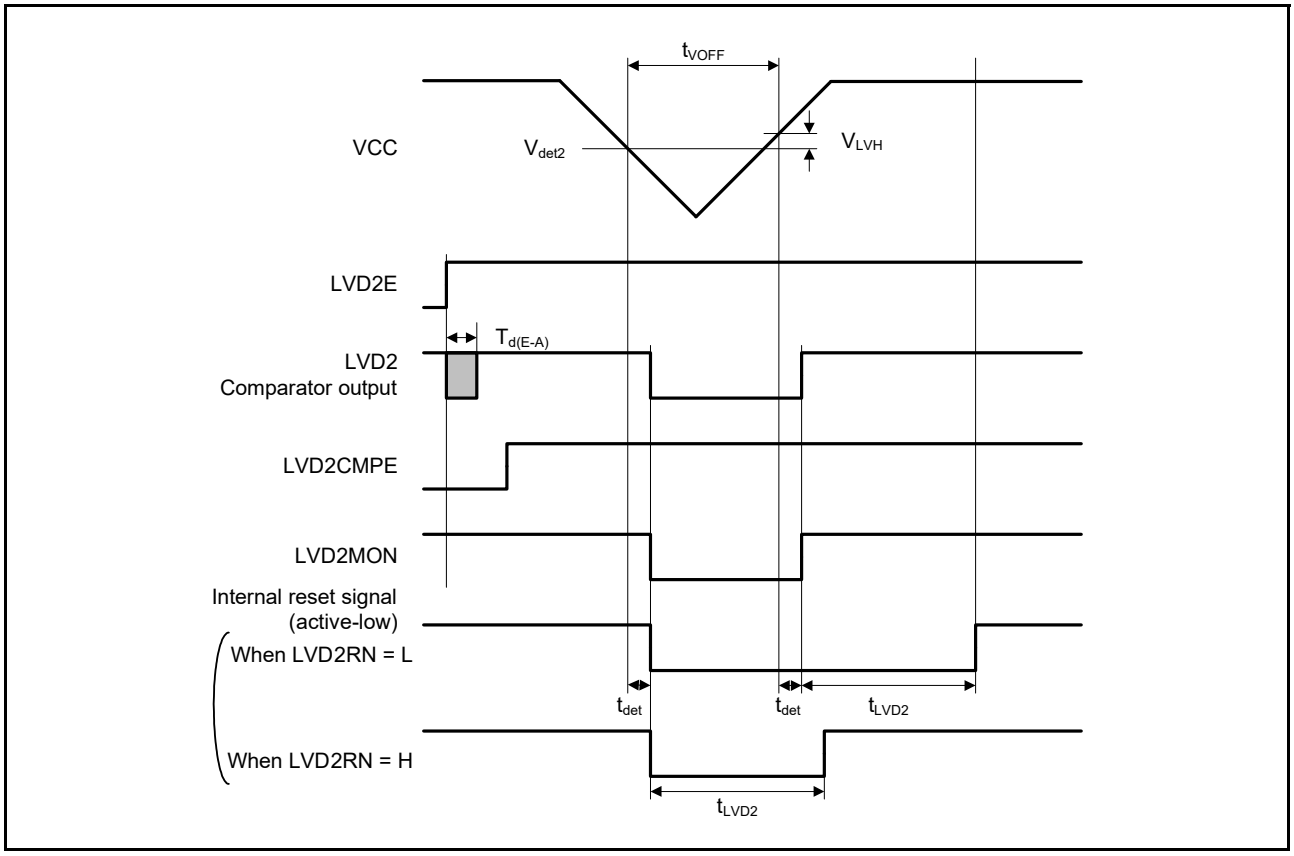


Figure 37.57 Voltage Detection Circuit Timing (V_{det2})

37.9 Oscillation Stop Detection Timing

Table 37.39 Oscillation Stop Detection Timing

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 =AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 37.58

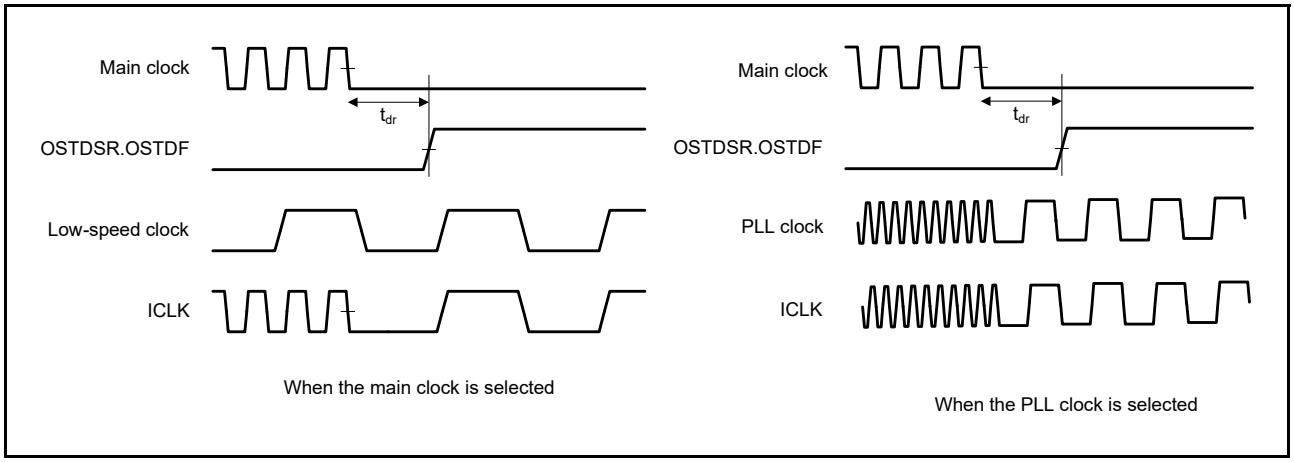


Figure 37.58 Oscillation Stop Detection Timing

37.10 ROM (Flash Memory for Code Storage) Characteristics

Table 37.40 ROM (Flash Memory for Code Storage) Characteristics (1)

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
Reprogramming/erasure cycle*1		N_{PEC}	1000	—	—	Times	
Data hold time	After 1000 times of N_{PEC}	t_{DRP}	20*2, *3	—	—	Year	T_a = +85°C

Note 1. Definition of reprogram/erase cycle: The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 4-byte programming is performed 256 times for different addresses in 1-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. Characteristic when using the flash memory programmer and the self-programming library provided from Renesas Electronics.
Note 3. This result is obtained from reliability testing.

Table 37.41 ROM (Flash Memory for Code Storage) Characteristics (2): High-Speed Operating Mode

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V

Temperature range for the programming/erasure operation: T_a = –40 to +85°C

Item		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	8-byte	t_{P8}	—	112.0	967.0	—	52.3	490.5	µs
Erasure time	2-Kbyte	t_{E2K}	—	8.7	278.1	—	5.5	214.6	ms
	512-Kbyte (when block erase command used)	t_{E512K}	—	927.8	19218.0	—	72.0	1678.9	ms
	512-Kbyte (when all-block erase command used)	t_{EA512K}	—	922.7	19013.4	—	66.7	1469.2	ms
Blank check time	8-byte	t_{BC8}	—	—	55.0	—	—	16.1	µs
	2-Kbyte	t_{BC2K}	—	—	1840.0	—	—	135.7	µs
Erase operation forcible stop time		t_{SED}	—	—	18.0	—	—	10.7	µs
Start-up area switching setting time		t_{SAS}	—	12.3	566.5	—	6.2	433.5	ms
Access window time		t_{AWS}	—	12.3	566.5	—	6.2	433.5	ms
ROM mode transition wait time 1		t_{DIS}	2.0	—	—	2.0	—	—	µs
ROM mode transition wait time 2		t_{MS}	5.0	—	—	5.0	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK should be ±3.5%.

Table 37.42 ROM (Flash Memory for Code Storage) Characteristics (3): Middle-Speed Operating Mode

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V

Temperature range for the programming/erasure operation: T_a = –40 to +85°C

Item		Symbol	FCLK = 1 MHz			FCLK = 8 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	8-byte	t_{P8}	—	152.0	1367.0	—	97.9	936.0	µs
Erasure time	2-Kbyte	t_{E2K}	—	8.8	279.7	—	5.9	220.8	ms
	512-Kbyte (when block erase command used)	t_{E512K}	—	928.0	19221.2	—	190.6	4107.3	ms
	512-Kbyte (when all-block erase command used)	t_{EA512K}	—	922.7	19015.0	—	185.4	3901.0	ms
Blank check time	8-byte	t_{BC8}	—	—	85.0	—	—	50.9	µs
	2-Kbyte	t_{BC2K}	—	—	1870.0	—	—	401.5	µs
Erase operation forcible stop time		t_{SED}	—	—	28.0	—	—	21.3	µs
Start-up area switching setting time		t_{SAS}	—	13.0	573.3	—	7.7	450.1	ms
Access window time		t_{AWS}	—	13.0	573.3	—	7.7	450.1	ms
ROM mode transition wait time 1		t_{DIS}	2.0	—	—	2.0	—	—	µs
ROM mode transition wait time 2		t_{MS}	3.0	—	—	3.0	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK should be ±3.5%.

37.11 E2 DataFlash Characteristics

Table 37.43 E2 DataFlash Characteristics (1)

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
Reprogramming/erasure cycle*1		N_{DPEC}	100000	1000000	—	Times	
Data hold time	After 10000 times of N_{DPEC}	t_{DDRP}	20*2, *3	—	—	Year	T_a = +85°C
	After 100000 times of N_{DPEC}		5*2, *3	—	—	Year	
	After 1000000 times of N_{DPEC}		—	1*2, *3	—	Year	T_a = +25°C

Note 1. Definition of reprogram/erase cycle: The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 100000), erasing can be performed n times for each block. For instance, when 1-byte programming is performed 1000 times for different addresses in 1-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. Characteristic when using the flash memory programmer and the self-programming library provided from Renesas Electronics.
Note 3. This result is obtained from reliability testing.

Table 37.44 E2 DataFlash Characteristics (2): High-Speed Operating Mode

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V,

Temperature range for the programming/erasure operation: T_a = –40 to +85°C

Item		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	1-byte	t_{Dp1}	—	95.0	797.0	—	40.8	375.5	µs
Erasure time	1-Kbyte	t_{DE1K}	—	19.5	498.5	—	6.2	229.4	ms
	8-Kbyte	t_{DE8K}	—	119.8	2555.7	—	12.9	367.2	ms
Blank check time	1-byte	t_{DBC1}	—	—	55.0	—	—	16.1	µs
	1-Kbyte	t_{DBC1K}	—	—	7216.0	—	—	495.7	µs
Erase operation forcible stop time		t_{DSED}	—	—	16.0	—	—	10.7	µs
Data flash-module stop release time		t_{DSTOP}	5.0	—	—	5.0	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK should be ±3.5%.

Table 37.45 E2 DataFlash Characteristics (3): Middle-Speed Operating Mode

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V,

Temperature range for the programming/erasure operation: T_a = –40 to +85°C

Item		Symbol	FCLK = 1 MHz			FCLK = 8 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	1-byte	t_{Dp1}	—	135.0	1197.0	—	86.5	822.5	µs
Erasure time	1-Kbyte	t_{DE1K}	—	19.6	500.1	—	8.0	264.1	ms
	8-Kbyte	t_{DE8K}	—	119.9	2557.4	—	27.7	668.2	ms
Blank check time	1-byte	t_{DBC1}	—	—	85.0	—	—	50.9	µs
	1-Kbyte	t_{DBC1K}	—	—	7246.0	—	—	1457.5	µs
Erase operation forcible stop time		t_{DSED}	—	—	28.0	—	—	21.3	µs
Data flash-module stop release time		t_{DSTOP}	0.72	—	—	0.72	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK should be ±3.5%.

37.12 Usage Notes

37.12.1 Connecting VCL Capacitor and Bypass Capacitors

This MCU integrates an internal voltage-down circuit, which is used for lowering the power supply voltage in the internal MCU to adjust automatically to the optimum level. A 4.7-µF capacitor needs to be connected between this internal voltage-down power supply (VCL pin) and VSS pin. Figure 37.59 and Figure 37.60 shows how to connect external capacitors. Place an external capacitor close to the pins. Do not apply the power supply voltage to the VCL pin. Insert a multilayer ceramic capacitor as a bypass capacitor between each pair of the power supply pins. Implement a bypass capacitor to the MCU power supply pins as close as possible. Use a recommended value of 0.1 µF as the capacitance of the capacitors. For the capacitors related to crystal oscillation, see section 9, Clock Generation Circuit. For the capacitors related to analog modules, also see section 31, 12-Bit A/D Converter (S12ADF).
For notes on designing the printed circuit board, see the descriptions of the application note “Hardware Design Guide” (R01AN1411EJ). The latest version can be downloaded from Renesas Electronics Website.

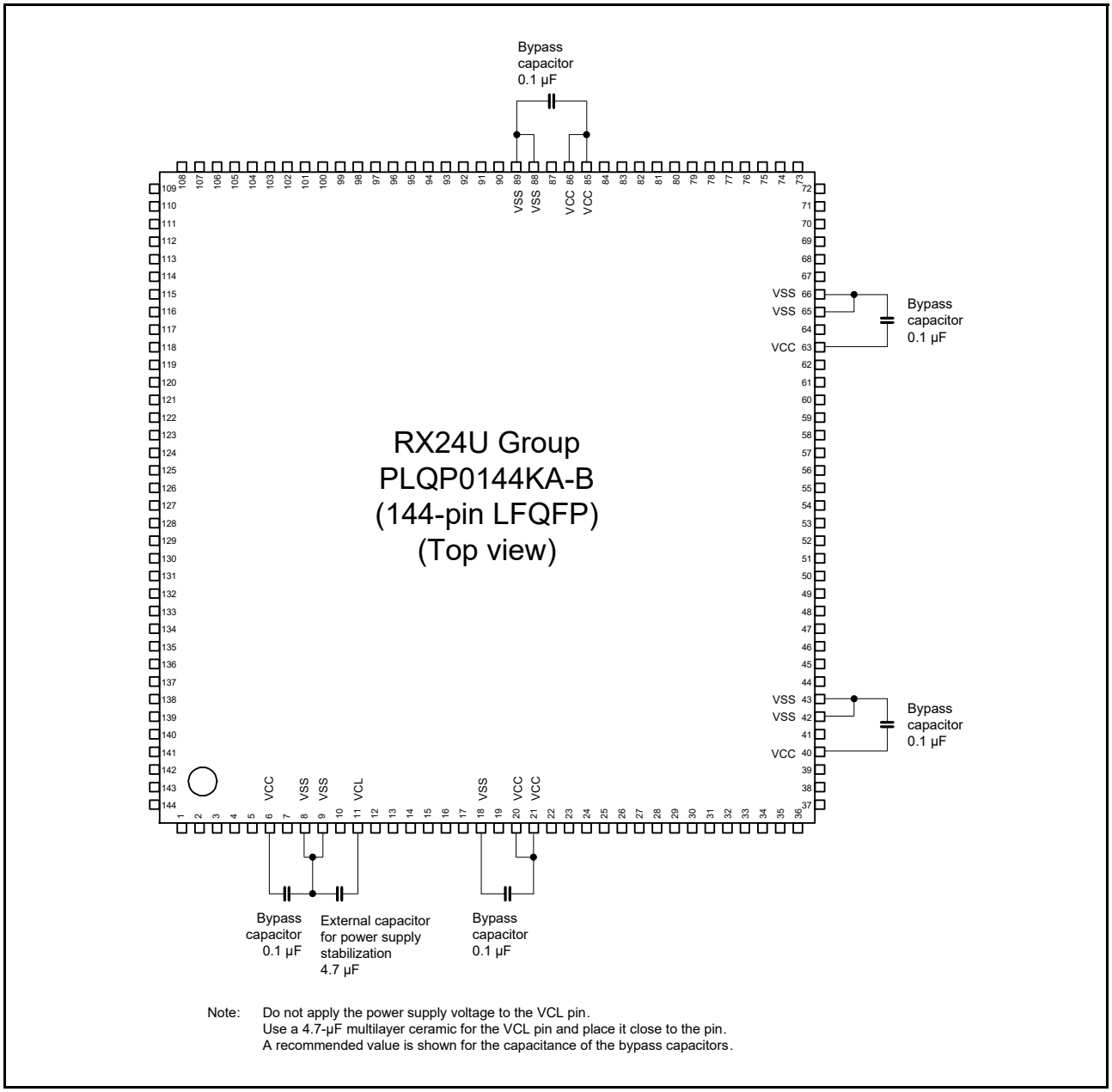
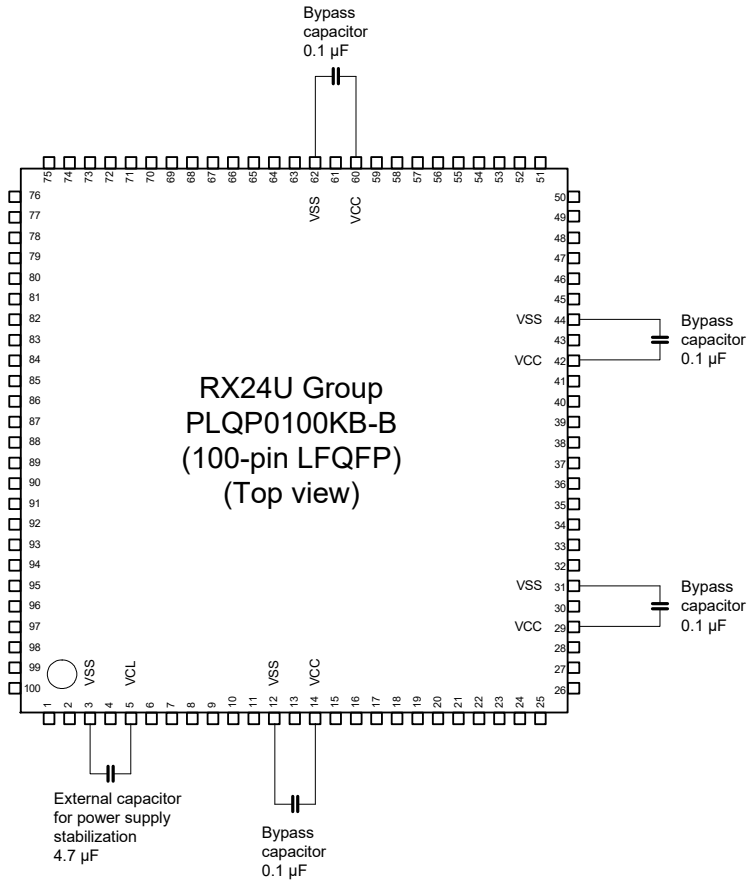


Figure 37.59 Connecting Capacitors (144 Pins)



Note: Do not apply the power supply voltage to the VCL pin.
Use a 4.7-µF multilayer ceramic for the VCL pin and place it close to the pin.
A recommended value is shown for the capacitance of the bypass capacitors.

Figure 37.60 Connecting Capacitors (100 Pins)

Appendix 1. Port States in Each Processing Mode

Table 1.1 Port States in Each Processing Mode

Port Name (Pin Name)	Operating Mode According to Registers Setting		Reset	Software Standby Mode
P00, P01, P02 (IRQ2, IRQ4, IRQ5)	All		Hi-Z	Keep-O*1
P10, P11 (IRQ0, IRQ1)	All		Hi-Z	Keep-O*1
P12 to P17	All		Hi-Z	Keep-O
P20, P21 (IRQ7, IRQ6)	All		Hi-Z	Keep-O*1
P22, P25, P26, P27	All		Hi-Z	Keep-O
P23 (DA1)	All	DA1 output	Hi-Z	DA1 output retained
		Other than the above	Hi-Z	Keep-O
P24 (DA0)	All	DA0 output	Hi-Z	DA0 output retained
		Other than the above	Hi-Z	Keep-O
P30, P31 (IRQ7, IRQ6)	All		Hi-Z	Keep-O*1
P32 to P37	All		Hi-Z	Keep-O
P40 to P47	All		Hi-Z	Keep-O
P50, P51	All		Hi-Z	Keep-O
P52, P53, P54, P55 (IRQ0, IRQ1, IRQ2, IRQ3)	All		Hi-Z	Keep-O*1
P60, P61, P62, P63 (IRQ4, IRQ5, IRQ6, IRQ7)	All		Hi-Z	Keep-O*1
P64, P65	All		Hi-Z	Keep-O
P70 (IRQ5)	All		Hi-Z	Keep-O*1
P71 to P76	All		Hi-Z	Keep-O
P80 to P84	All		Hi-Z	Keep-O
P90 to P95	All		Hi-Z	Keep-O
P96 (IRQ4)	All		Hi-Z	Keep-O*1
PA0 to PA4, PA6, PA7	All		Hi-Z	Keep-O
PA5 (IRQ1)	All		Hi-Z	Keep-O*1
PB0 to PB3, PB5, PB7	All		Hi-Z	Keep-O
PB4, PB6 (IRQ3, IRQ5)	All		Hi-Z	Keep-O*1
PC0 to PC6	All		Hi-Z	Keep-O
PD0 to PD3, PD7	All		Hi-Z	Keep-O
PD4, PD5, PD6 (IRQ2, IRQ3, IRQ5)	All		Hi-Z	Keep-O*1
PE0, PE1	All		Hi-Z	Keep-O
PE2, PE3, PE4, PE5, PE6 (NMI, IRQ2, IRQ1, IRQ0, IRQ3)	All		Hi-Z	Keep-O*1
PF0 to PF3	All		Hi-Z	Keep-O
PG0 to PG2	All		Hi-Z	Keep-O

Keep-O: Output pins retain their previous values, and input pins become high-impedance.
Hi-Z: High-impedance

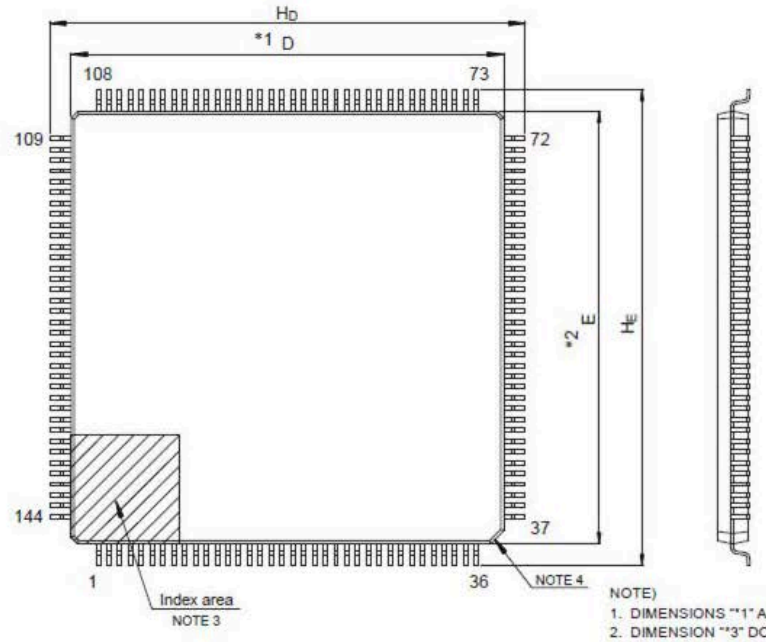
Note 1. Input is enabled if the pin is specified as the software standby mode canceling source while it is used as an external interrupt pin.

Appendix 2. Package Dimensions

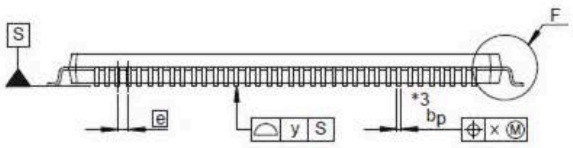
Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

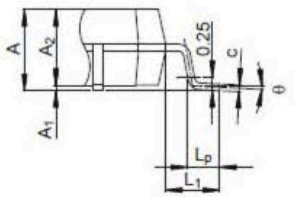
JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP144-20x20-0.50	PLQP0144KA-B	—	1.2

Unit: mm



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.





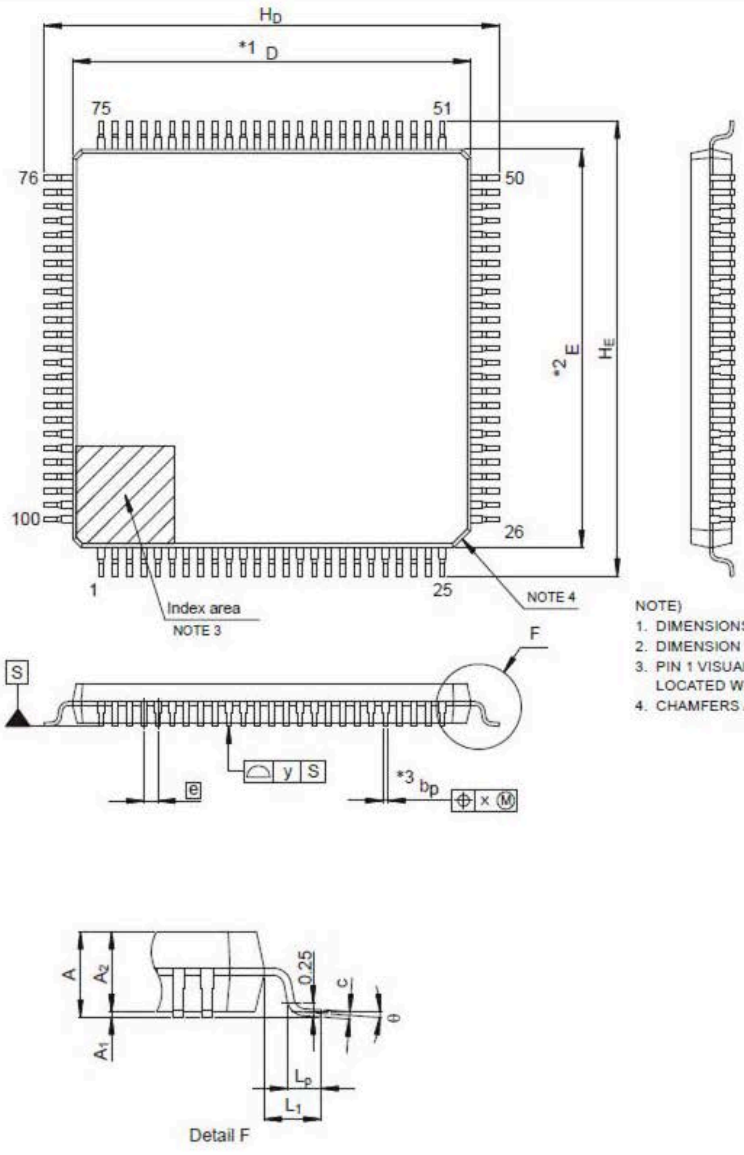
Detail F

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.17	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure A 144-Pin LFQFP (PLQP0144KA-B)

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6

Unit: mm



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure B 100-Pin LFQFP (PLQP0100KB-B)

REVISION HISTORY	RX24U Group User's Manual: Hardware

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
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