

μPC844, μPC4744

Single Power Supply, High Speed, Wide Band,

R03DS0137EJ0100 Rev.1.00 2019.1.17

Quad Operational Amplifier

DESCRIPTION

 μ PC324 realizing high-speed version of the single-power general-purpose operational amplifier μ PC451, μ PC324 realizing high-speed response and high stability. By adopting a high speed PNP transistor circuit, various characteristics such as slew rate and gain bandwidth are improved, as compared to μ PC451 and μ PC324, the load capacity stability is also improved, with no crossover distortion.

It can be used widely for various application circuits such as single power supply AC amplifier, active filter, line driver, amplifier for light receiving element, etc.

Depending on the usage and operating ambient temperature range, the μ PC844 is designed for extended temperature and suited for wide operating ambient temperature application, and μ PC4744 is design for general purposes. Along with this series of lineup, the dual type operational amplifier, μ PC842, μ PC4742 with the same circuit configuration are also available.

FEATURES

Slew Rate (A_V = 1)
 7 V/µs (TYP.) (V ⁺ = +5 V, V ⁻ = GND)

Gain Bandwidth Product (f = 100 kHz)
 Input Offset Voltage
 Input Offset Current
 ±2 mV (TYP.)
 ±6 nA (TYP.)

Operating Ambient Temperature

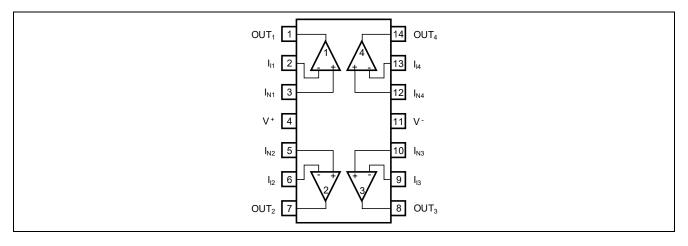
 μ PC844G2 : T_A = -40 ~ +85 °C, μ PC4744G2 : T_A = -20 ~ +80 °C, μ PC844GR-9LG : T_A = -40 ~ +125 °C, μ PC4744GR-9LG : T_A = -40 ~ +85 °C,

- Stability to capacitive load (Capacitive load, 1000 pF)
- Built-in phase correction circuit.
- Built-in output short-circuit protection circuit.
- Standard pin (pin compatible) configuration of a quad operational amplifier.

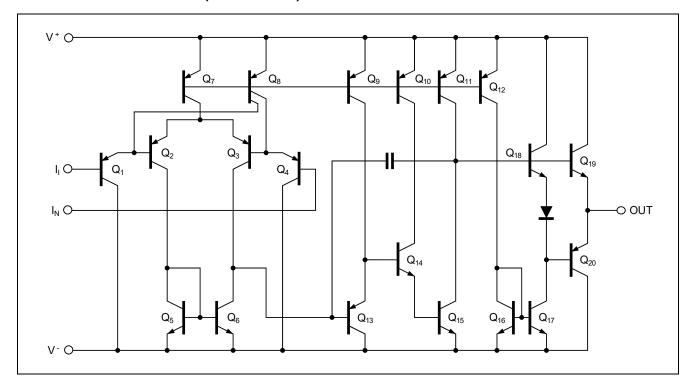
ORDERING INFORMATION

Order Name	Selected Grade	Package
μPC844G2-A	Standard	14-pin plastic SOP (5.72 mm (225))
μPC4744G2-A	Standard	14-pin plastic SOP (5.72 mm (225))
μPC844GR-9LG-A	Standard	14-pin plastic TSSOP (5.72 mm (225))
μPC4744GR-9LG-A	Standard	14-pin plastic TSSOP (5.72 mm (225))

PIN CONFIGURATION (Top View)



EQUIVALENT CIRCUIT (1/4CIRCUIT)



ABSOLUTE MAXIMUM RATINGS ($T_A = 25 \, ^{\circ}C$)

Parameter	Symbol	μPC844G2	μPC4744G2	μPC844GR- 9LG	μPC4744GR- 9LG	Unit
Power Supply Voltage Note 1	V + - V -	-0.3 ~ +36				V
Differential Input Voltage	V_{ID}		±36			
Input Voltage Note 2	Vı	V0.3 ~ V - +36			V	
Output Applied Voltage Note 3	Vo	V ⁻ -0.3 ~ V ⁺ +0.3			V	
Total Power Dissipation Note 4	PT	550				mW
Output Short Circuit Duration Note 5	ts	Indefinite			s	
Operating Ambient Temperature	TA	-40 ~ +85	-20 ~ +80	-40 ~ +125	-40 ~ +85	°C
Storage Temperature	T _{stg}	-55 ~ +125		-55 ~ +150	-55 ~ +125	°C

[Note] 1. Note that reverse connections of the power supply may damage the ICs.

2. The allowable input voltage range without damaging or destructing the device. Independent to power supply voltage range.

Do not apply voltage equivalent to V - (GND) - 0.3 V or less.

Note that the operational amplifier will operate normally when the input voltage applied is within the common mode input voltage range.

- 3. The input voltage range that can be applied to the output pin externally without deteriorating or damaging the device characteristic. The permitted input voltage that can be applied regardless of the power supply voltage. This specification also includes precaution during transition state such as ON/OFF, etc.
- 4. This is the value when the glass epoxy substrate (size: 100 mm x 100 mm, thickness: 1 mm, 15% of the substrate area where only one side is copper foiled is filling wired) is mounted.

Note that restrictions will be made to the following conditions for each product, and the de-rating ratio depending on the operating ambient temperature.

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\muPC844G2, 4744G2 : De-rate -5.5 mW/°C when T<sub>A</sub> > 25 °C
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(Junction – ambient thermal resistance R_{th(J-A)} = 182 °C/W)

 μ PC844GR-9LG : De-rate -7.0 mW/°C when T_A > 71 °C

(Junction - ambient thermal resistance Rth(J-A) = 144 °C/W)

 $\mu PC4744GR\text{-}9LG$: De-rate -7.0 mW/°C when $T_A\,>\,46\,\,^{\circ}C_{\circ}$

(Junction - ambient thermal resistance R_{th(J-A)} = 144 °C/W)

5. Please use the total loss and the de-rating factor of Note 4.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Power Supply Voltage (V - = GND)	V +	+3	+5 ~ +30	+32	V
Power Supply Voltage (Dual Supply)	V ±	±1.5		±16	٧
Output Current	lo			±10	mA
Capacitive Load (A _V = +1)	CL			1000 Note 6	pF

[Note] 6. This is the value when feedback resistor (R_f) = 0 Ω .

ELECTRICAL CHARACTERISTICS

 $(T_A = 25 \, {}^{\circ}C, V^{\pm} = \pm 15 \, V)$

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
Input Offset Voltage	Vio		±2	±6	mV	
Input Offset Current	I _{IO}		±6	±75	nA	
Input Bias Current Note 7	I _B		130	500	nA	
Large Signal Voltage Gain	Av	25000	300000			$R_L \ge 2 \text{ k}\Omega$, $V_O = \pm 10 \text{ V}$
Circuit Current Note 8	Icc		7.5	11	mA	I _O = 0 A
Common Mode Rejection Ratio	CMR	70	86		dB	
Supply Voltage Rejection Ratio	SVR	70	93		dB	
Output Voltage Swing	V _{Om1}	V _{Om1} ±13.7	+14		V	$R_L \ge 10 \text{ k}\Omega$
		±13.7	-14.3		V	
	V _{Om2}	±13.5			V	$R_L \ge 2 k\Omega$
Common Mode Input Voltage Range	V _{ICM}	V -		V + -1.8	٧	
Slew Rate	SR		8.5		V/µs	A _V = 1 (Rise edge)
Gain Bandwidth Product	GBW		3.5		MHz	f = 100 kHz
Channel Separation			120		dB	f = 20 Hz ~ 20 kHz

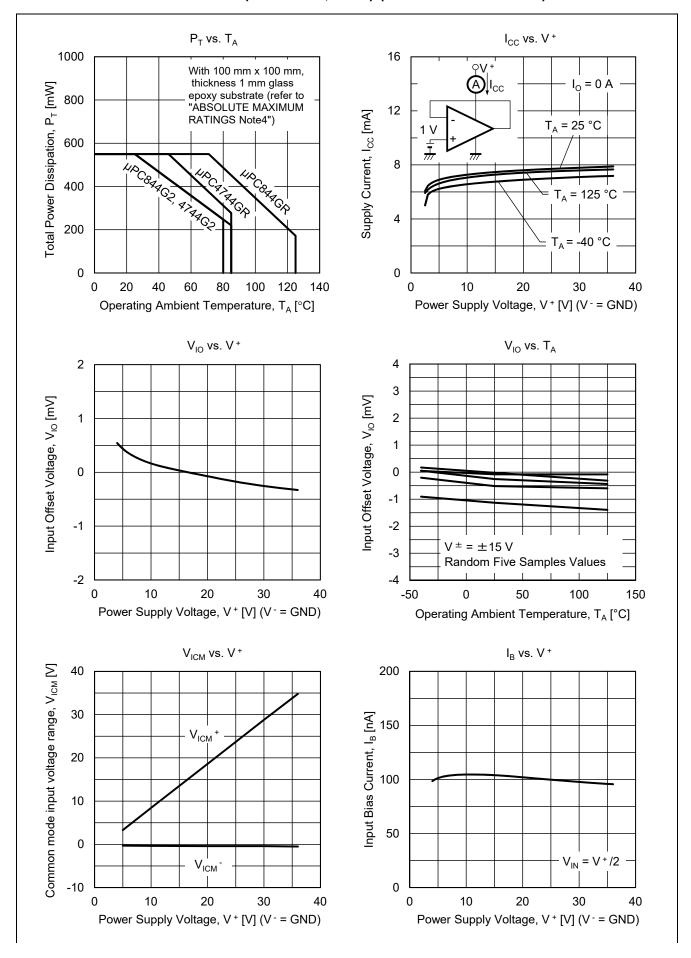
(T_A = 25 °C, V $^{+}$ = +5 V, V $^{-}$ = GND)

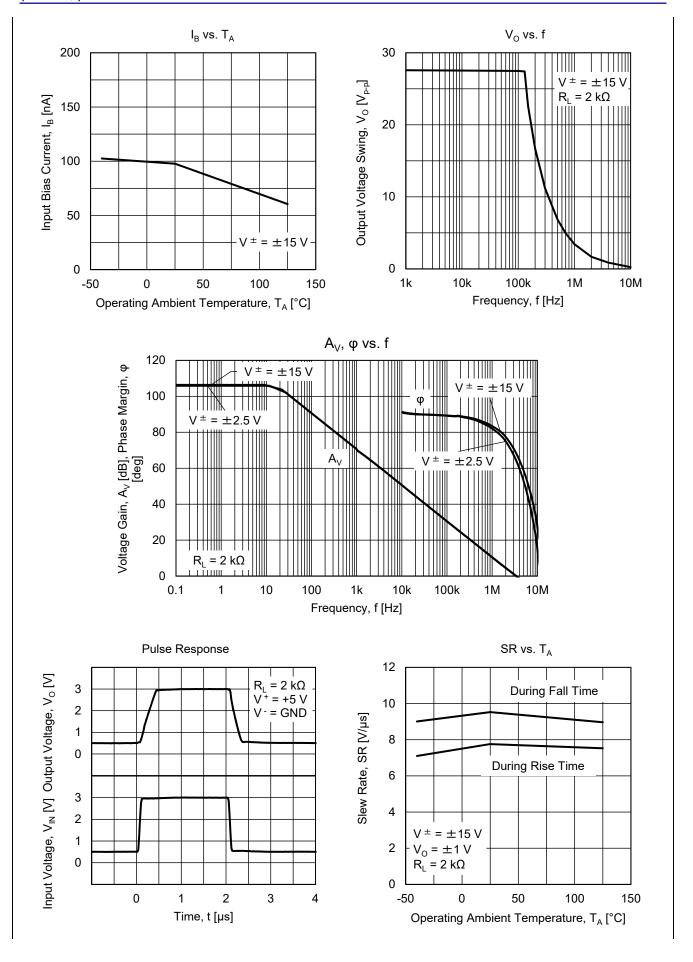
				('	Λ - 0 (5, V 10 V, V CITE,
Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
Input Offset Voltage	V _{IO}		±2	±5	mV	
Input Offset Current	lio		±6	±75	nA	
Input Bias Current Note 7	lΒ		150	500	nA	
Large Signal Voltage Gain	Av	25000	300000			$R_L \ge 2 k\Omega$
Circuit Current Note 8	Icc		6	9	mA	Io = 0 A
Common Mode Rejection Ratio	CMR	70	80		dB	
Supply Voltage Rejection Ratio	SVR	70	95		dB	
Output Voltage Swing	Vom	3.7	4		V	$R_L \ge 2 \ k\Omega$ (Connected to GND)
		0	0			
Common Mode Input Voltage Range	Vicm	0		V + -1.8	V	
Output Source Current	lo source	10	30		mA	V _{IN(+)} = +1 V, V _{IN(-)} = 0 V
Output Sink Current	I _{O SINK}	10	30		mA	V _{IN(+)} = 0 V, V _{IN(-)} = +1 V
Slew Rate	SR		7		V/µs	A _V = 1 (Rise)

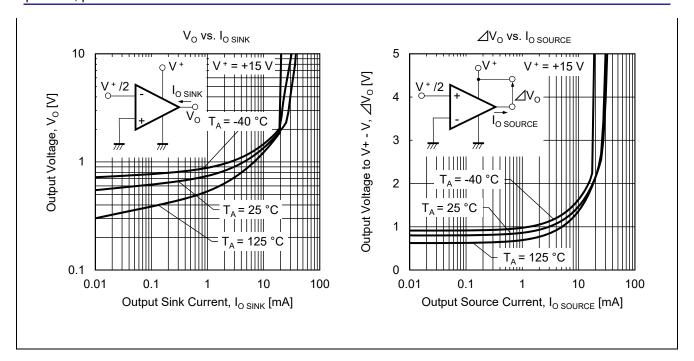
[Note] 7. The current flow direction of the input bias is out from the IC because the first stage of the IC composed of PNP transistor.

8. Current flowing through the internal circuit. This current flow regardless of the channel used.

CHARACTERISTICS CURVE (T_A = 25 °C, TYP.) (REFERENCE VALUE)





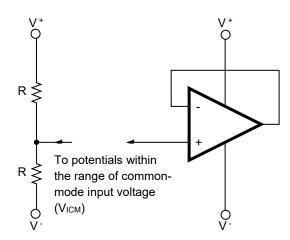


USE WITH PRECAUTIONS

· Managing unused circuits

If there is an unused circuit, the following connection is recommended.

Process example of unused circuits



Remark: In this example, an intermediate potential between V + and V - is applied.

• Ratings of input/output pin voltage

When the voltage of input/output pin exceeds the absolute maximum rating, the parasitic diode within the IC may conduct, causing characteristics degradation or damage. In addition, if the input pin is lower than V-, or the output pin exceeds the power supply voltage, it is recommended to make a clamping circuit using a diode with low forward voltage (e.g.: Schottky diode) as protection.

• Range of common-mode input voltage

When the supply voltage does not meet the condition of electrical characteristics, the range of common-mode input voltage is as follows.

$$V_{ICM}$$
 (TYP.) : $V^- \sim V^+ - 1.8$ [V] ($T_A = 25$ °C)

During designing, do include some tolerance by considering temperature characteristics etc.

Maximum Output Voltage

The TYP. value range of the maximum output voltage when the supply voltage does not meet the condition of electrical characteristics is as follows:

$$V_{Om}^+$$
 (TYP.) : V^+ -1 [V] (T_A = 25 °C), V_{Om}^- (TYP.) : V^- +0.7 [V] (T_A = 25 °C)

During designing, do include some tolerance by considering characteristics variation, temperature characteristics and so on. In addition, also note that the output voltage range $(V_{om}^+ - V_{om}^-)$ will become narrow when the output current increases.

Output Operation

This IC will not be able to sink output current when the output voltage is $V^- + 0.7$ V and below. In this case, the output voltage level can be improved to the V- side by connecting the load resistor between the output terminal and V^- to sink the current at the load resistor. (The effect will differ depending on the flow of current in the load resistance.)

Handling of ICs

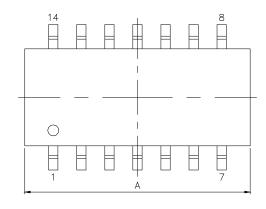
When stress is added to the ICs due to warpage or bending of a board, the characteristic may fluctuates due to piezoelectric effect. Therefore, pay attention to warpage or bending of a board.

PACKAGE DRAWINGS

14-PIN PLASTIC SOP

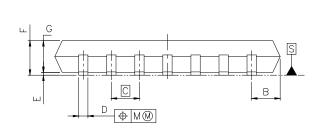
JEITA Package code	RENESAS code	Previous code	MASS (TYP.) [g]
P-SOP14-0225-1.27	PRSP0014DI-A	P14GR-50-225B	0.14

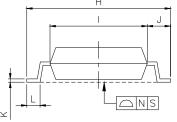
Unit: mm



detail of lead end







NOTE

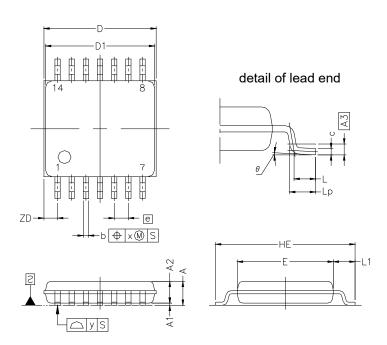
Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
Α	10.2 ±0.26
В	1.42 MAX
С	1.27 (T.P)
D	0.42 ^{+0.08} -0.07
Е	0.1 ±0.1
F	1.59 ^{+0.21} -0.2
G	1.49
Н	6.5 ±0.2
	4.4 ±0.1
J	1.1 ±0.16
K	0.17 ^{+0.08} _{-0.07}
L	0.6 ±0.2
М	0.1
N	0.10
Р	3° ^{+7°} -3°

14-PIN PLASTIC TSSOP

JEITA Package code	RENESAS code	Previous code	MASS(TYP.) [g]
P-TSSOP14-0225-0.65	PTSP0014JB-A	P14GR-65-9LG-1	_

Unit: mm



NOTE

Each lead centerline is located within 0.10 mm of its true position at maximum material condition.

ITEM	MILLIMETERS
D	5.15 ±0.15
D1	5.00 ±0.10
Е	4.40 ±0.10
HE	6.40 ±0.20
A	1.20 MAX.
A1	0.10 ±0.05
A2	1.00 ±0.05
A3	0.25
b	0.24 ^{+0.06} -0.05
С	0.145 ±0.055
L	0.5
Lp	0.60 ±0.15
L1	1.00 ±0.20
θ	3° +5° -3°
е	0.65
Х	0.10
у	0.10
ZD	0.625

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