

# SH74582

R01DS0240EJ0111

Rev.1.11

Feb 18, 2015

## RENESAS MCU

### 1. Overview

The SH7458 Group is a single-chip RISC (reduced instruction set computer) microcontroller based on a Renesas original RISC CPU core.

Basically the SH7458 Group is the same as the SH7456 Group. Please refer to SH7455 Group, SH7456 Group User's Manual: Hardware Rev.1.10 (Sep 22, 2011). Table 1.1 shows the differences between the SH7456 Group and the SH7458 Group.

\* Henceforth, the bold letter portion (shaped portion) shows a difference from SH7456 Group.

**Table 1.1 Products**

Group	Product	Model	CPU Frequency	Memory Capacity	Package	FlexRay	Operating temperature (Ta)
<b>SH7458</b>	<b>SH74582</b>	<b>R5F74582KBG</b>	160MHz	ROM: 1Mbytes IL memory: 8 Kbytes, OL memory: 16 Kbytes, and SHwyRAM: <b>512</b> Kbytes	PRBG0176GA-A	<b>Yes</b>	-40 to +125°C
SH7455	SH74552	R5F74552KBG	160MHz	ROM: 1Mbyte	PRBG0176GA-A	Yes	-40 to +125°C
SH7456	SH74562	R5F74562KBG	160MHz	IL memory: 8 Kbytes, OL memory: 16 Kbytes, and SHwyRAM: 256 Kbytes	PRBG0176GA-A	No	-40 to +125°C
SH7457	SH74572	R5F74572LBG	240MHz	ROM: 1Mbyte IL memory: 8 Kbytes, OL memory: 16 Kbytes, and SHwyRAM: 256 Kbytes	PRBG0176GA-A	Yes	-40 to +105°C
SH7459	SH74593	R5F74593LBG	240MHz	ROM: 1.5Mbytes IL memory: 8 Kbytes, OL memory: 16 Kbytes, and SHwyRAM: 512 Kbytes	PRBG0176GA-A	Yes	-40 to +105°C

### 2. Details

This section shows the details of the difference from SH7455 Group, SH7456 Group User's Manual: Hardware Rev.1.10 (Sep 22, 2011). Table 2.1 shows the difference between the SH74562 and the SH74582.

**Table 2.1 Difference between SH74562 and SH74582**

Page	Description						
1-1	<ul style="list-style-type: none"> <li>1.1 Features</li> </ul> <table border="1"> <thead> <tr> <th>Product</th> <th>SuperHyway RAM (SHwyRAM) Capacity</th> </tr> </thead> <tbody> <tr> <td>SH74562</td> <td>256 Kbytes</td> </tr> <tr> <td>SH74582</td> <td><b>512</b> Kbytes</td> </tr> </tbody> </table>	Product	SuperHyway RAM (SHwyRAM) Capacity	SH74562	256 Kbytes	SH74582	<b>512</b> Kbytes
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SH74562	256 Kbytes						
SH74582	<b>512</b> Kbytes						
1-4	<ul style="list-style-type: none"> <li>Table 1.1 Specifications Overview: Descriptions of RAM</li> </ul> <table border="1"> <thead> <tr> <th>Product</th> <th>RAM Capacity</th> </tr> </thead> <tbody> <tr> <td>SH74562</td> <td>256-Kbyte</td> </tr> <tr> <td>SH74582</td> <td><b>512</b>-Kbyte</td> </tr> </tbody> </table>	Product	RAM Capacity	SH74562	256-Kbyte	SH74582	<b>512</b> -Kbyte
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SH74562	None: SH7456 Group												
SH74582	<b>Two channels: SH7458</b> Group												
1-7	<ul style="list-style-type: none"> <li>Table 1.2 Products</li> </ul> <table border="1"> <thead> <tr> <th>Product</th> <th>Model</th> <th>SHwyRAM Capacity</th> <th>FlexRay</th> </tr> </thead> <tbody> <tr> <td>SH74562</td> <td>R5F74562KBG</td> <td>256 Kbytes</td> <td>No</td> </tr> <tr> <td>SH74582</td> <td><b>R5F74582KBG</b></td> <td><b>512</b> Kbytes</td> <td><b>Yes</b></td> </tr> </tbody> </table> <p>Please refer to Appendix A.</p>	Product	Model	SHwyRAM Capacity	FlexRay	SH74562	R5F74562KBG	256 Kbytes	No	SH74582	<b>R5F74582KBG</b>	<b>512</b> Kbytes	<b>Yes</b>
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SH74562	R5F74562KBG	256 Kbytes	No										
SH74582	<b>R5F74582KBG</b>	<b>512</b> Kbytes	<b>Yes</b>										
1-8	<ul style="list-style-type: none"> <li>Figure 1.1 Block Diagram</li> </ul> <table border="1"> <thead> <tr> <th>Product</th> <th>SHwyRAM Capacity</th> </tr> </thead> <tbody> <tr> <td>SH74562</td> <td>SHwyRAM (256 Kbytes)</td> </tr> <tr> <td>SH74582</td> <td>SHwyRAM (<b>512</b> Kbytes)</td> </tr> </tbody> </table>	Product	SHwyRAM Capacity	SH74562	SHwyRAM (256 Kbytes)	SH74582	SHwyRAM ( <b>512</b> Kbytes)						
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28-47	<ul style="list-style-type: none"> <li>28.3.24 DRli Address Counters 0 and 1 (DRliADR0CT and DRliADR1CT) : Description of DRIADn bit</li> </ul> <table border="1"> <thead> <tr> <th>Product</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>SH74562</td> <td>Destination Address Bits 18 to 2 (256-Kbyte area)</td> </tr> <tr> <td>SH74582</td> <td>Destination Address Bits 18 to 2 (<b>512</b>-Kbyte area)</td> </tr> </tbody> </table> <p>Please refer to Appendix D.3.</p>	Product	Description	SH74562	Destination Address Bits 18 to 2 (256-Kbyte area)	SH74582	Destination Address Bits 18 to 2 ( <b>512</b> -Kbyte area)																
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Product	Access area																						
SH74562	SHwyRAM area (256 Kbytes)																						
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## Appendix A

### Section 1 Overview

#### 1.2 Product Line Overview

Table 1.2 lists the products.

**Table 1.2 Products**

Product	Model	ROM Capacity	RAM Capacity	Package	FlexRay
SH74552	R5F74552KBG	1 Mbyte	IL memory: 8 Kbytes,	PRBG0176GA-A	Yes
SH74562	R5F74562KBG		OL memory: 16 Kbytes, and		No
SH74572	R5F74572LBG		SHwyRAM: 256 Kbytes		Yes
<b>SH74582</b>	<b>R5F74582KBG</b>		IL memory: 8 Kbytes,		<b>Yes</b>
			OL memory: 16 Kbytes, and		
			SHwyRAM: <b>512</b> Kbytes		
SH74593	R5F74593LBG	1.5 Mbytes	IL memory: 8 Kbytes,		Yes
			OL memory: 16 Kbytes, and		
			SHwyRAM: 512 Kbytes		

Appendix B

Appendix B.1

Section 11 Address Space

For details on the P0/U0 area to the P4 area, see figures 11.2 to 11.6.

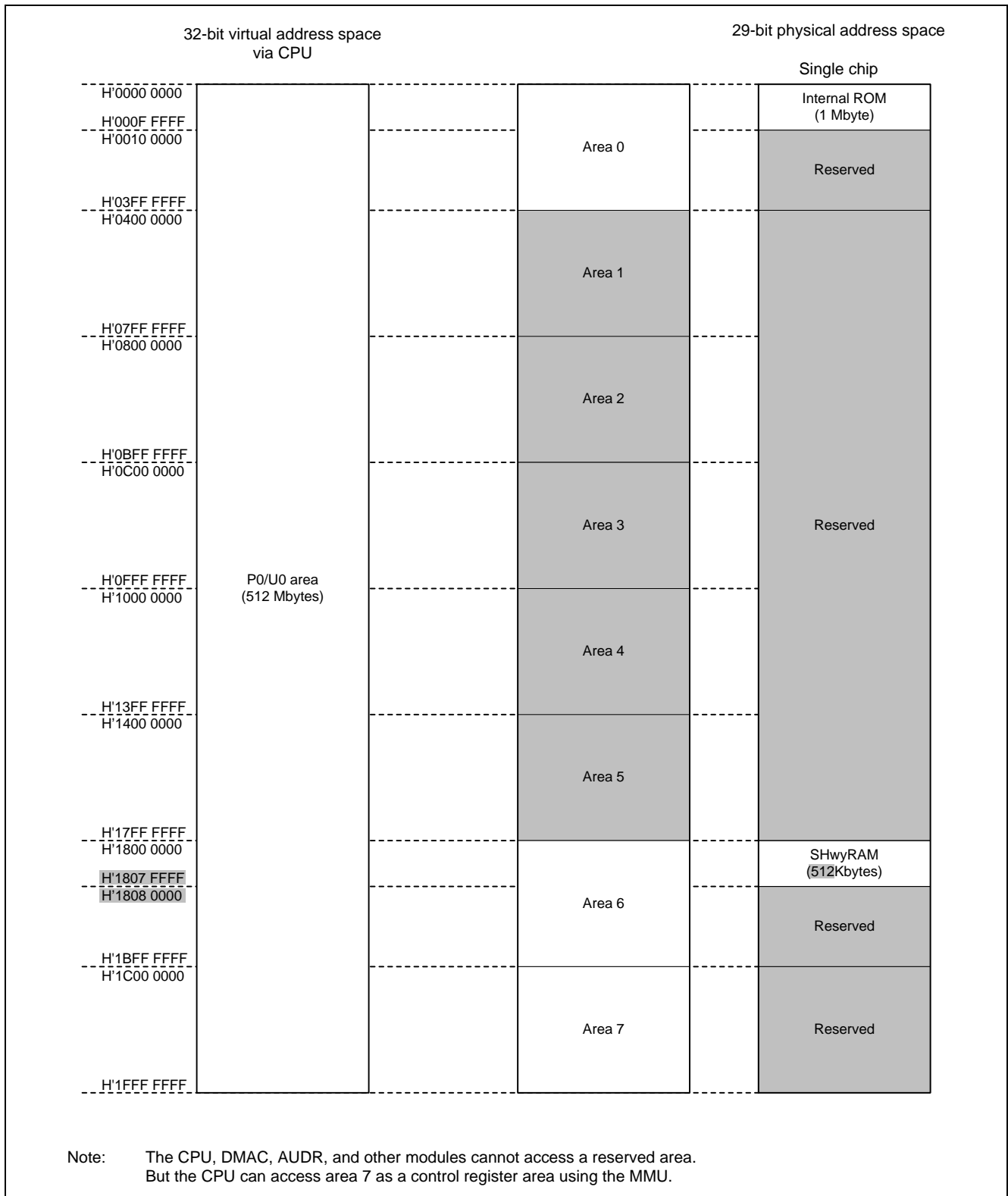


Figure 11.2 Address Space (P0/U0 Area)

Appendix B.2

Section 11 Address Space

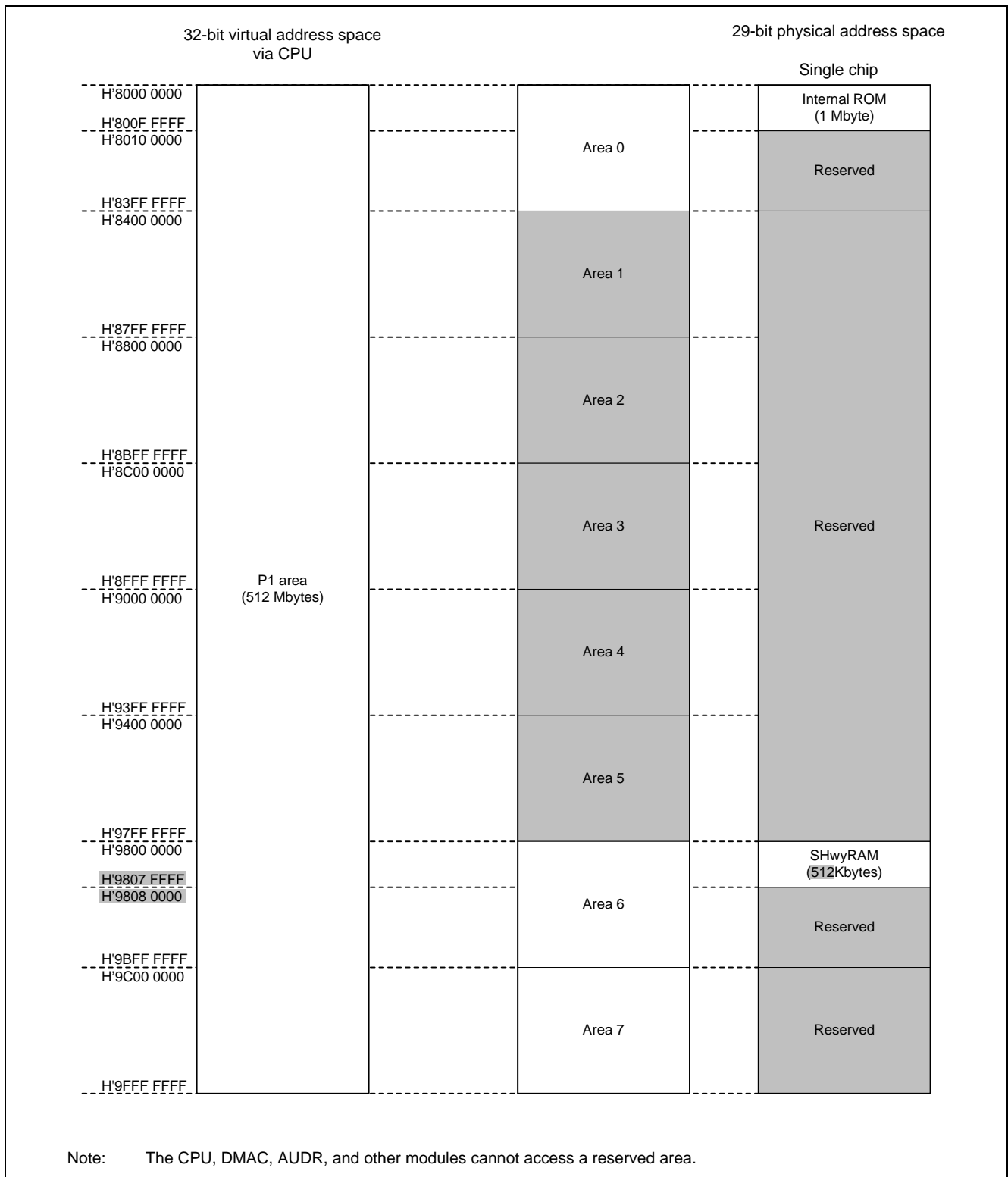


Figure 11.3 Address Space (P1 Area)

Appendix B.3

Section 11 Address Space

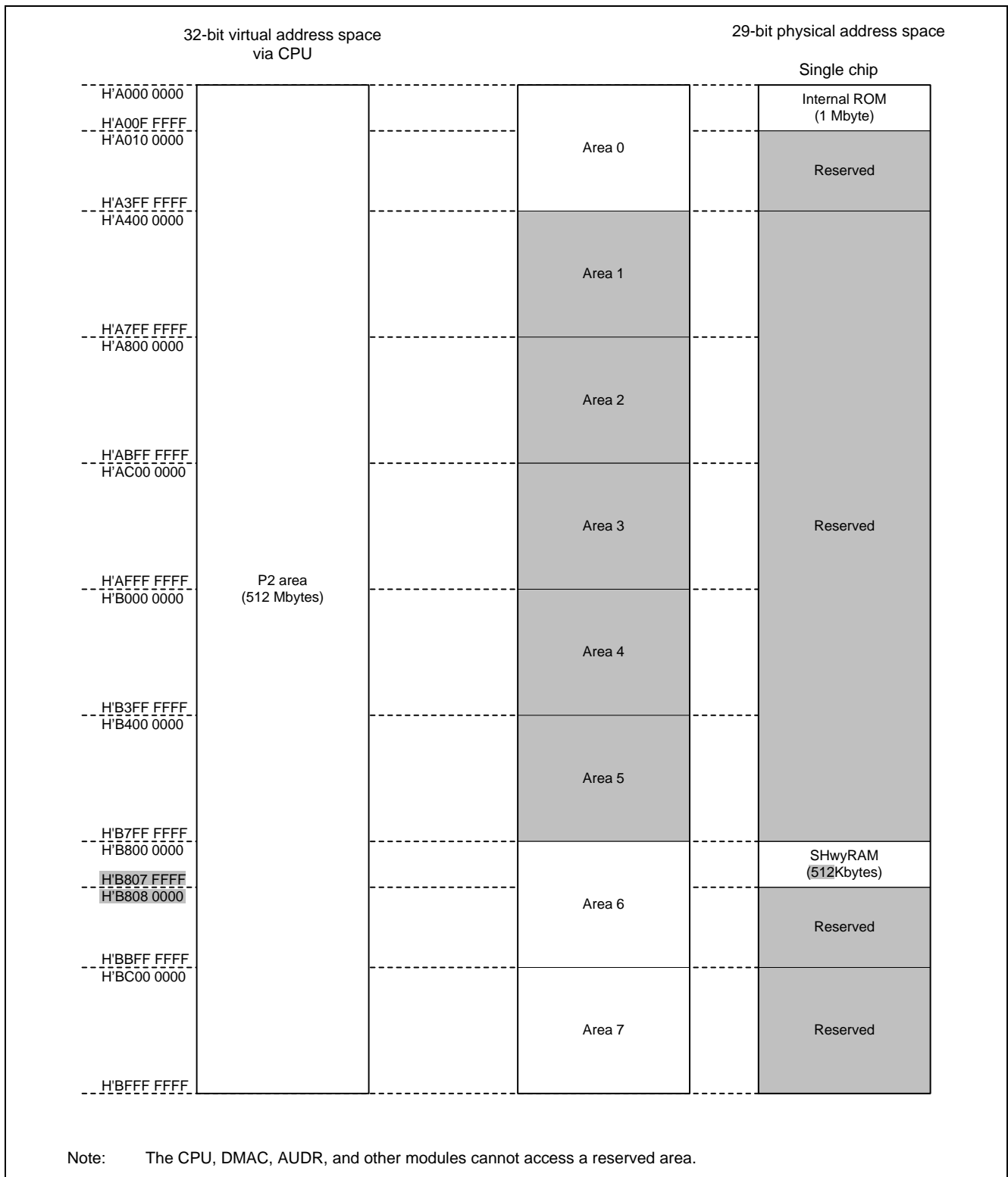


Figure 11.4 Address Space (P2 Area)

Appendix B.4

Section 11 Address Space

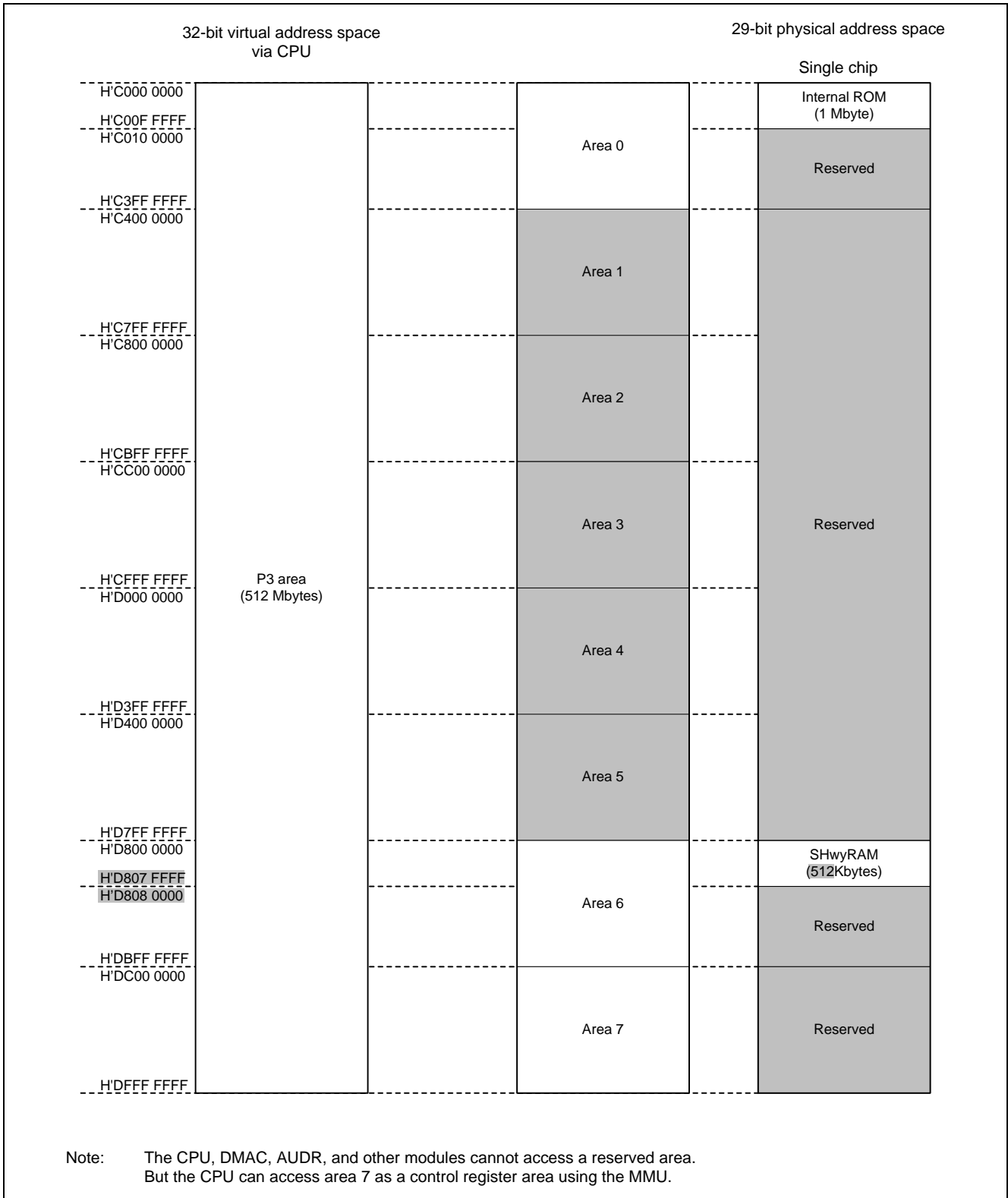


Figure 11.5 Address Space (P3 Area)



## Appendix C

### Section 13 SuperHyway RAM (SHwyRAM)

#### 13.1 Overview

As shown in figure 13.2, the SHwyRAM is allocated to the upper **512 Kbytes** of area 6 (H'1800 0000 to **H'1807 FFFF** in the 29-bit physical address space).

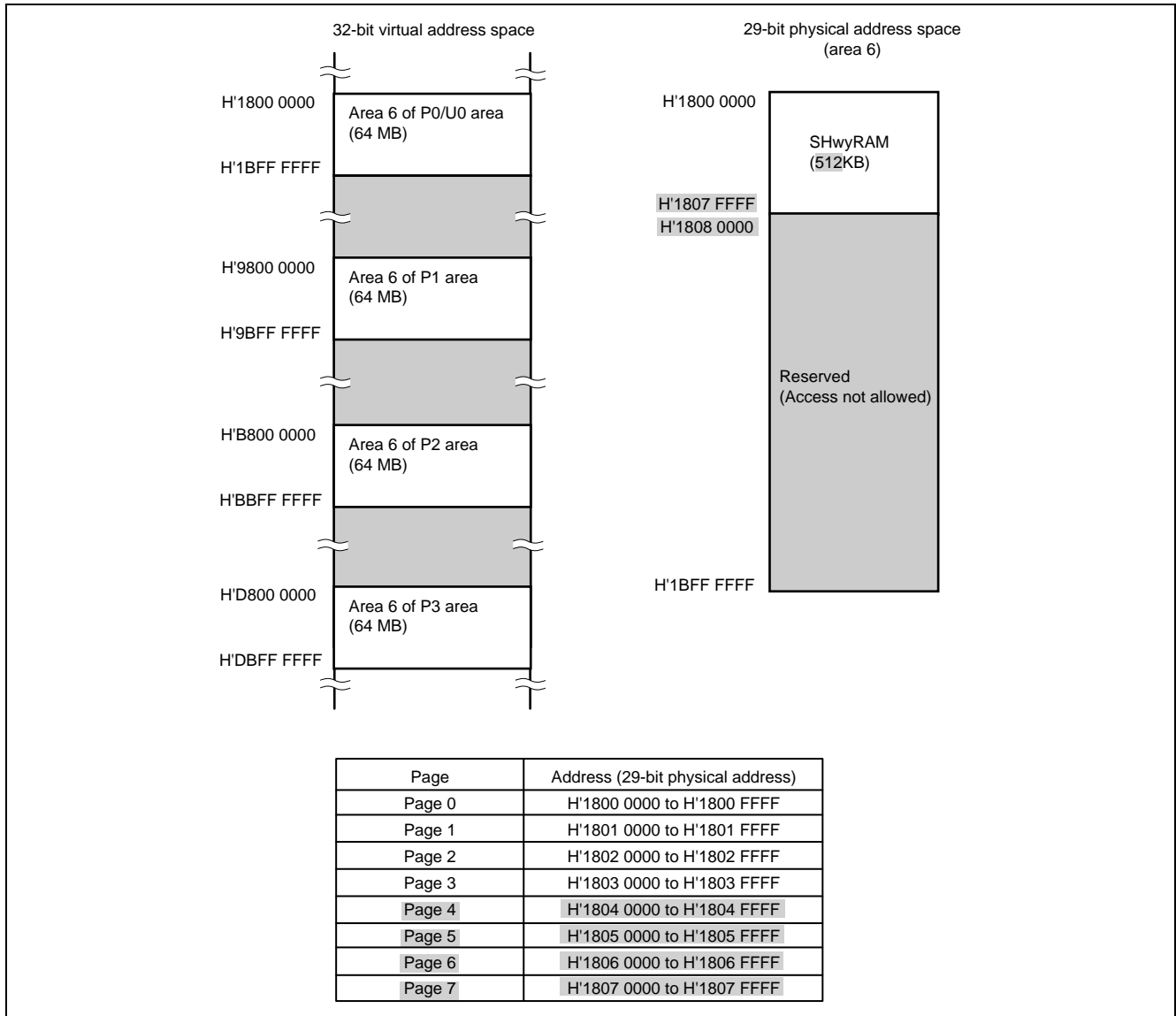


Figure 13.2 Address Space

## Appendix D

### Section 28 Direct RAM Input Interface (DRI)

#### Appendix D.1

#### 28.1 Overview

Table 28.1 lists the overview of the DRI modules.

**Table 28.1 DRI Overview**

Item	Description
Number of channels	3 channels
Operating frequency	80 MHz (when P <sub>ACK</sub> = 80 MHz)
Transfer method	Clock synchronous parallel input
Access areas	All SHwyRAM areas (up to <b>512</b> Kbytes)
Maximum transfer rate	80 Mbytes/second (when the DRI operating frequency is 80 MHz)
Minimum data acquisition period	The following are the minimum periods when the DRI operating frequency is 80 MHz. 43.75 ns (special mode disabled and the input data bus width is 8 or 16 bits) 25 ns (special mode enabled)
Data acquisition bus width	8 or 16 bits
Event counter	16 bits × 6 counters (DEC5 to DEC0)
Bank switching function	Two banks can be specified as the data storage destination in SHwyRAM
Data acquisition edges	Either rising edges, falling edges, or both edges can be selected
Acquisition timing adjustment function	Sets the time between detection of the data acquisition edge and the acquisition operation
Decimation control function	Data can be acquired selectively using an event counter (DEC5 to DEC0)

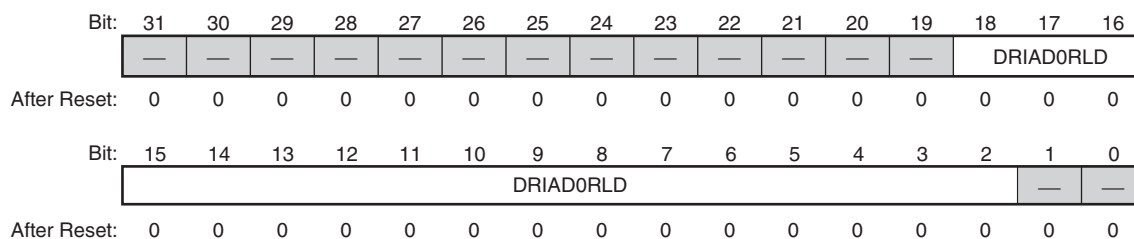
## Appendix D.2

### 28.3.23 DRi Address Reload Registers 0 and 1 (DRiADR0RLD and DRiADR1RLD)

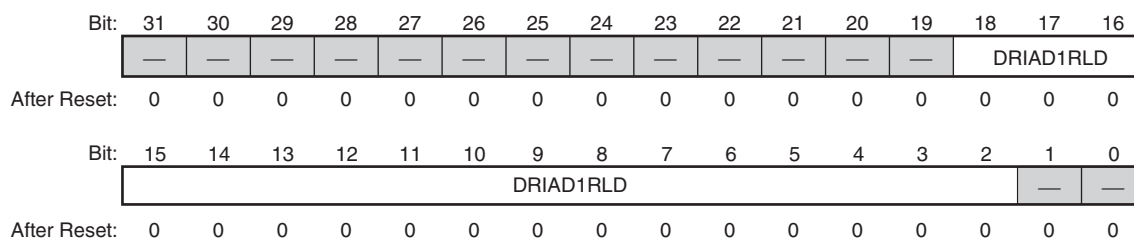
DRiADR0CT and DRiADR1CT are registers that hold counter reload values. When reload mode is selected with the DRi transfer control register (DRiTRMCNT) ADMD (address counter operating mode selection) bit, the corresponding DRi address counters are reloaded with the values set in these registers when the DRi data acquisition control register (DRiDCAPCNT) DCPEN (acquisition enable) bit changes from "0" to "1".

Note: • These registers may only be rewritten when the DRi data acquisition control register (DRiDCAPCNT) DCPEN (acquisition enable) bit is in the "0" state.

DRi0 Address Reload Register 0 (DRi0ADR0RLD) <P4 address: location H'FFBF C024>  
 DRi1 Address Reload Register 0 (DRi1ADR0RLD) <P4 address: location H'FFBF D024>  
 DRi2 Address Reload Register 0 (DRi2ADR0RLD) <P4 address: location H'FFBF E024>



DRi0 Address Reload Register 1 (DRi0ADR1RLD) <P4 address: location H'FFBF C02C>  
 DRi1 Address Reload Register 1 (DRi1ADR1RLD) <P4 address: location H'FFBF D02C>  
 DRi2 Address Reload Register 1 (DRi2ADR1RLD) <P4 address: location H'FFBF E02C>



<After Reset: H'0000 0000>

Bit	Abbreviation	After Reset	R	W	Description
31 to 19	—	All 0	0	0	Reserved Bits These bits are always read as "0". The write value should always be "0".
18 to 2	DRiADmRLD	All 0	R	W	Address Bits 18 to 2 Reload Value ( <b>512</b> -Kbyte area)
1, 0	—	All 0	0	0	Reserved Bits These bits are always read as "0". The write value should always be "0".

Legend: m = 0 or 1

## Appendix D.3

### 28.3.24 DRi Address Counters 0 and 1 (DRiADR0CT and DRiADR1CT)

The DRiADR0CT and DRiADR1CT counters are provided to specify bits A18 to A2 of the address in SHwyRAM that is the DRi module transfer destination. Bits A31 to A19 are fixed at "0". These counters are incremented by "4" each time a DRi transfer completes. There are two DRi address counter operating modes, and applications can select the mode with the DRi transfer control register (DRiTRMCNT) ADMD bit. See the documentation of the DRi transfer control register (DRiTRMCNT) for details.

- Notes:
- If a DRi address counter value is a value other than an area in which SHwyRAM is located, the DRi module will behave as though the DRi transfers complete, but no writes of the acquired data will be performed whatsoever.
  - A DRi address counter is incremented by "4" when a DRi transfer completed. This is performed for the one that is active at that time according to the setting of the DRi transfer control register (DRiTRMCNT) ADSL (address counter selection) bit.
  - These registers must only be rewritten in the state where a DRi transfer counter (DRiTRMCT) underflow has occurred (the counter is stopped at the value H'0000 0000).

DRi0 Address Counters 0 (DRi0ADR0CT)

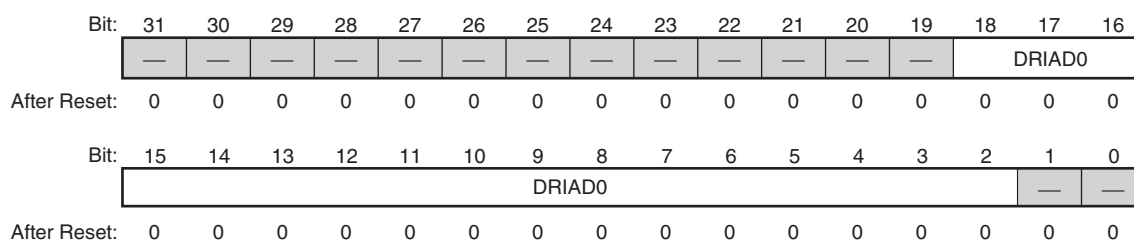
<P4 address: location H'FFBF C028>

DRi1 Address Counters 0 (DRi1ADR0CT)

<P4 address: location H'FFBF D028>

DRi2 Address Counters 0 (DRi2ADR0CT)

<P4 address: location H'FFBF E028>



DRi0 Address Counters 1 (DRi0ADR1CT)

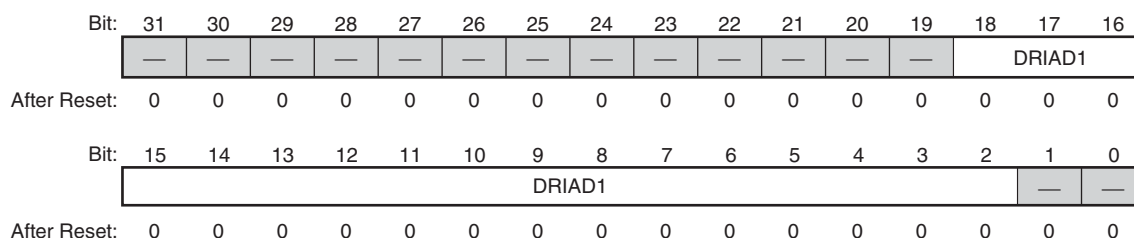
<P4 address: location H'FFBF C030>

DRi1 Address Counters 1 (DRi1ADR1CT)

<P4 address: location H'FFBF D030>

DRi2 Address Counters 1 (DRi2ADR1CT)

<P4 address: location H'FFBF E030>



<After Reset: H'0000 0000>

Bit	Abbreviation	After Reset	R	W	Description
31 to 19	—	All 0	0	0	Reserved Bits These bits are always read as "0". The write value should always be "0".
18 to 2	DRIADn	All 0	R	W	Destination Address Bits 18 to 2 (512-Kbyte area)
1, 0	—	All 0	0	0	Reserved Bits These bits are always read as "0". The write value should always be "0".

Legend: n = 0 or 1

## Appendix E

### Section 29 Direct RAM Output Interface (DRO)

#### 29.1 Overview

Table 29.1 lists the overview of the DRO module.

**Table 29.1 DRO Module Overview**

Item	Description
Transfer method	Parallel strobed output
Access area	SHwyRAM area ( <b>512</b> Kbytes)
Output data width	Either 8-bits or 16-bits
Maximum transfer clock	10 MHz
Maximum transfer rate	20 Mbytes/s (when 16 bits is selected, Pck = 40MHz)
Strobe polarity	Either "H" active or "L" active may be selected.
Timing adjustment function	The setup and hold times can be programmed in 1Pck units relative to the strobe signal edge.
Interrupt request	An interrupt request is generated after a prespecified number of data items have been output.

<b>REVISION HISTORY</b>	<b>SH74582 Datasheet</b>
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Rev.	Date	Description	
		Page	Summary
1.10	Oct 20, 2014	-	First edition issued
1.11	Feb 18, 2015	1	Corrected SHwyRAM capacity of R5F74572LBG. (Error) 512K -> (Correct) 256K

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