RAA730300
Monolithic Programmable Analog IC

R02DS0011EJ0110
Rev.1.10
May. 31, 2014

Overview

The RAA730300 is a monolithic programmable analog IC that supports low voltages and features a range of on-chip circuits such as configurable amplifiers, general-purpose operational amplifiers, D/A converters, and a temperature sensor, allowing the RAA730300 to be used as an analog front-end device for processing minute sensor signals. The RAA730300 uses a Serial Peripheral Interface (SPI) to allow external devices to control each on-chip circuit, enabling a more compact package and a reduction in the number of control pins. The compact package used by the RAA730300—a 48-pin LQFP—in turns enables a more compact set design.

Features

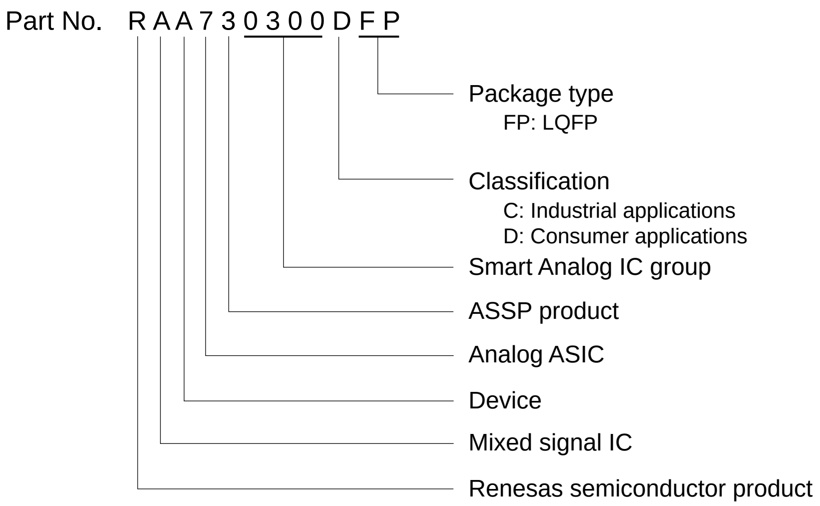
- On-chip configurable amplifier × 3 ch
- On-chip general-purpose operational amplifier × 2 ch
- On-chip low-pass filter × 1 ch
- On-chip high-pass filter × 1 ch
- On-chip D/A converter × 7 ch
- On-chip variable output voltage regulator × 1 ch
- On-chip temperature sensor × 1 ch
- On-chip SPI × 1 ch
- Includes a low-current mode.
- Operating voltage range: 2.2 V ≤ V_{DD} ≤ 3.6 V
- Operating temperature range: –40°C ≤ T_A ≤ 105°C
- Package: 48-pin plastic LQFP (fine pitch) (7 × 7)

Applications

- Home appliances
- Industrial equipment
- Healthcare equipment

Ordering Information

Pin count	Package	Part Number
48 pins	48-pin plastic LQFP (fine pitch) (7 × 7)	RAA730300CFP, RAA730300DFP



How to Read This Manual

It is assumed that the readers of this manual have general knowledge of electrical engineering, electronic circuits.

- To gain a general understanding of functions:
  →Read this manual in the order of the CONTENTS.
- To check the revised points :
  →The mark <R> shows major revised points. The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what: " field.

Conventions

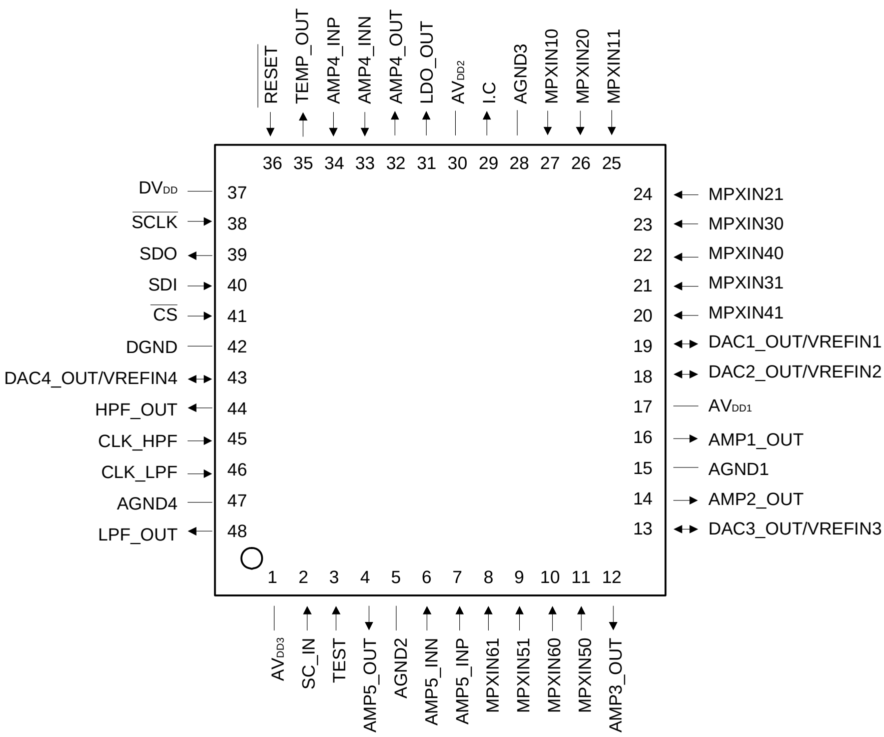
Data significance	: Higher digits on the left and lower digits on the right
Active low representations	: $\overline{xxx}$ (overscore over pin and signal name)
Note	: Footnote for item marked with Note in the text
Caution	: Information requiring particular attention
Remark	: Supplementary information
Numerical representations	: Binary ...xxxx or xxxxB Decimal ...xxxx Hexadecimal ...xxxxH

Contents

1. Pin Configuration

1.1 Pin Layout

48-pin plastic LQFP (fine pitch) (7 × 7)



Cautions 1. Make the potential of AGND1, AGND2, AGND3, AGND4, and DGND the same.

2. Make the potential of AV_{DD1}, AV_{DD2}, AV_{DD3}, and DV_{DD} the same.

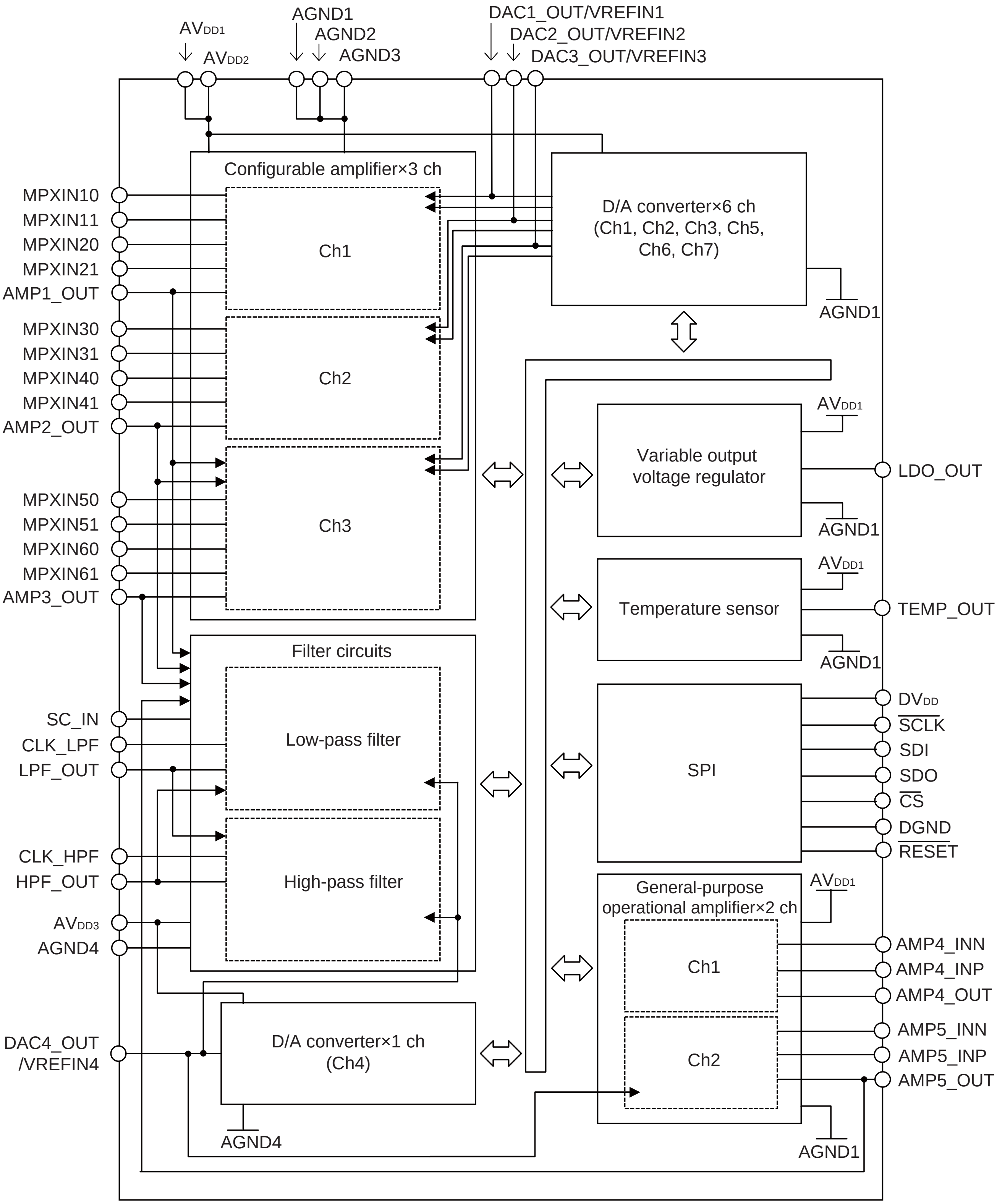
3. Connect the LDO_OUT pin to AGND3 via a capacitor (1.0 μF: recommended).

4. Connect the DAC4_OUT/VREFIN4 pin to AGND4 via a capacitor (470 pF: recommended).

5. Connect the I.C pin to AGND3.

6. Connect the TEST pin to AGND4.

1.2 Block Diagram



1.3 Pin Functions

Table 1-1. Pin Functions (1/2)

Pin No.	Pin Name	I/O	Pin Functions
1	AV_{DD3}	–	Power supply pin for low-pass filter, high-pass filter and D/A converter Ch4
2	SC_IN	Input	Input pin for filter signal processing
3	TEST	–	TEST pin
4	AMP5_OUT	Output	General-purpose operational amplifier Ch2 output pin
5	AGND2	–	GND pin for configurable amplifier channels Ch1 to Ch3,general-purpose operational amplifiers channels Ch1 to Ch2, D/A converter channels Ch1 to Ch3, Ch5 to Ch7, variable output voltage regulator and temperature sensor
6	AMP5_INN	Input	Pin for inputting inverted signal to general-purpose operational amplifier Ch2
7	AMP5_INP	Input	Pin for inputting non-inverted signal to general-purpose operational amplifier Ch2
8	MPXIN61	Input	Multiplexer 6 input pin 1
9	MPXIN51	Input	Multiplexer 5 input pin 1
10	MPXIN60	Input	Multiplexer 6 input pin 0
11	MPXIN50	Input	Multiplexer 5 input pin 0
12	AMP3_OUT	Output	Configurable amplifier Ch3 output pin
13	DAC3_OUT/ VREFIN3	Output/ input	D/A converter Ch3 output pin/ configurable amplifier Ch3 reference voltage input pin
14	AMP2_OUT	Output	Configurable amplifier Ch2 output pin
15	AGND1	–	GND pin for configurable amplifier channels Ch1 to Ch3, general-purpose operational amplifiers channels Ch1 to Ch2, D/A converter channels Ch1 to Ch3, Ch5 to Ch7, variable output voltage regulator and temperature sensor
16	AMP1_OUT	Output	Configurable amplifier Ch1 output pin
17	AV_{DD1}	–	Power supply pin for configurable amplifier channels Ch1 to Ch3, general-purpose operational amplifiers channels Ch1 to Ch2, D/A converter channels Ch1 to Ch3, Ch5 to Ch7, variable output voltage regulator and temperature sensor.
18	DAC2_OUT/ VREFIN2	Output/ input	D/A converter Ch2 output pin/ configurable amplifier Ch2 reference voltage input pin
19	DAC1_OUT/ VREFIN1	Output/ input	D/A converter Ch1 output pin/ configurable amplifier Ch1 reference voltage input pin
20	MPXIN41	Input	Multiplexer 4 input pin 1
21	MPXIN31	Input	Multiplexer 3 input pin 1
22	MPXIN40	Input	Multiplexer 4 input pin 0
23	MPXIN30	Input	Multiplexer 3 input pin 0
24	MPXIN21	Input	Multiplexer 2 input pin 1
25	MPXIN11	Input	Multiplexer 1 input pin 1
26	MPXIN20	Input	Multiplexer 2 input pin 0
27	MPXIN10	Input	Multiplexer 1 input pin 0
28	AGND3	–	GND pin for configurable amplifier channels Ch1 to Ch3, general-purpose operational amplifiers channels Ch1 to Ch2, D/A converter channels Ch1 to Ch3, Ch5 to Ch7, variable output voltage regulator and temperature sensor
29	I.C	–	–
30	AV_{DD2}	–	Power supply pin for configurable amplifier channels Ch1 to Ch3, general-purpose operational amplifiers channels Ch1 to Ch2, D/A converter channels Ch1 to Ch3, Ch5 to Ch7, variable output voltage regulator and temperature sensor

Table 1-1. Pin Functions (2/2)

Pin No.	Pin Name	I/O	Pin Functions
31	LDO_OUT	Output	Variable output voltage regulator output pin
32	AMP4_OUT	Output	General-purpose operational amplifier Ch1 output pin
33	AMP4_INN	Input	Pin for inputting inverted signal to general-purpose operational amplifier Ch1
34	AMP4_INP	Input	Pin for inputting non-inverted signal to general-purpose operational amplifier Ch1
35	TEMP_OUT	Output	Temperature sensor output pin
36	$\overline{\text{RESET}}$	Input	External reset input pin
37	DV_{DD}	–	Power supply pin for SPI
38	$\overline{\text{SCLK}}$	Input	Serial clock input pin for SPI
39	SDO	Output	Serial data output pin for SPI
40	SDI	Input	Serial data input pin for SPI
41	$\overline{\text{CS}}$	Input	Chip select input pin for SPI
42	DGND	–	GND pin for SPI
43	DAC4_OUT/ VREFIN4	Output/ input	D/A converter Ch4 output pin and pin for inputting reference voltage to low-pass filter, high-pass filter, and general-purpose operational amplifier Ch2
44	HPF_OUT	Output	High-pass filter output pin
45	CLK_HPF	Input	Pin for inputting high-pass filter control clock
46	CLK_LPF	Input	Pin for inputting low-pass filter control clock
47	AGND4	–	GND pin for low-pass filter, high-pass filter and D/A converter Ch4
48	LPF_OUT	Output	Low-pass filter output pin

1.4 Connection of Unused Pins

Table 1-2. Connection of Unused Pins

Pin Name	I/O	Recommended Connection of Unused Pins
SC_IN	Input	Directly connect to AGND4.
AMP5_OUT	Output	Leave open.
AMP5_INN	Input	Directly connect to AGND1.
AMP5_INP	Input	
MPXIN61	Input	
MPXIN51	Input	
MPXIN60	Input	
MPXIN50	Input	
AMP3_OUT	Output	Leave open.
DAC3_OUT/VREFIN3	Output/input	
AMP2_OUT	Output	
AMP1_OUT	Output	
DAC2_OUT/VREFIN2	Output/input	
DAC1_OUT/VREFIN1	Output/input	
MPXIN41	Input	Directly connect to AGND1.
MPXIN31	Input	
MPXIN40	Input	
MPXIN30	Input	
MPXIN21	Input	
MPXIN11	Input	
MPXIN20	Input	
MPXIN10	Input	
AMP4_OUT	Output	Leave open.
AMP4_INN	Input	Directly connect to AGND1.
AMP4_INP	Input	
TEMP_OUT	Output	Leave open.
$\overline{\text{SCLK}}$	Input	Connect to Ground.Note
SDO	Output	Leave open.
SDI	Input	Connect to Ground.Note
$\overline{\text{CS}}$	Input	
DAC4_OUT/VREFIN4	Output/input	Leave open.
HPF_OUT	Output	
CLK_HPF	Input	
CLK_LPF	Input	
LPF_OUT	Output	
LDO_OUT	Output	
$\overline{\text{RESET}}$	Input	Connect to DV$_{DD}$ directly or via a resistor.

Note Ground means the same electrical potential as AGND1, AGND2, AGND3, AGND4 and DGND.

1.5 Pin I/O Circuits

Figure 1-1. Pin I/O Circuit Type (1/4)

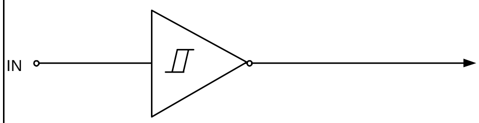
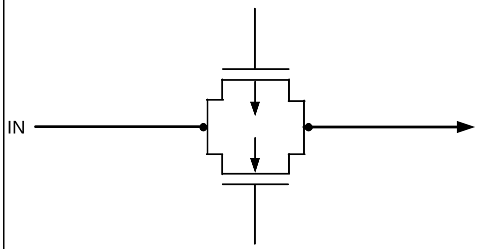
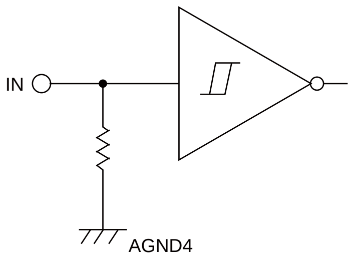
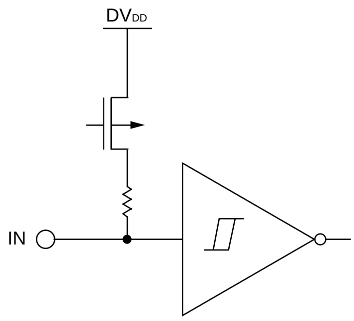
Pin Name	Equivalent Circuit	Pin Name	Equivalent Circuit
$\overline{\text{RESET}}$	 Schmitt-triggered input with hysteresis characteristics	MPXIN10 MPXIN11 MPXIN20 MPXIN21 MPXIN30 MPXIN31 MPXIN40 MPXIN41 MPXIN50 MPXIN51 MPXIN60 MPXIN61 SC_IN	
CLK_LPF CLK_HPF	Schmitt-triggered input with hysteresis characteristics 	$\overline{\text{SCLK}}$ SDI $\overline{\text{CS}}$	 Schmitt-triggered input with hysteresis characteristics

Figure 1-1. Pin I/O Circuit Type (2/4)

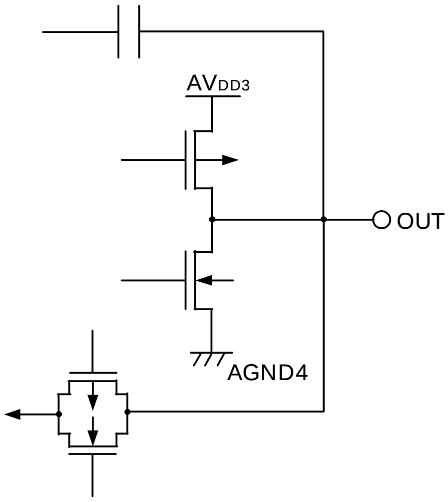
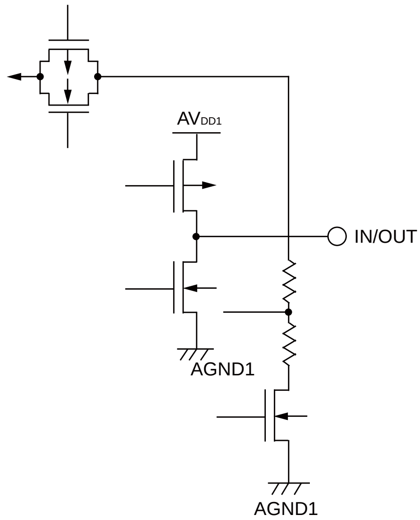
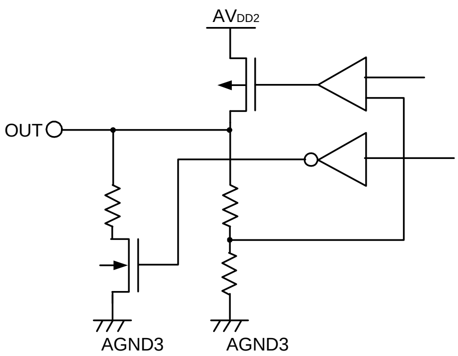
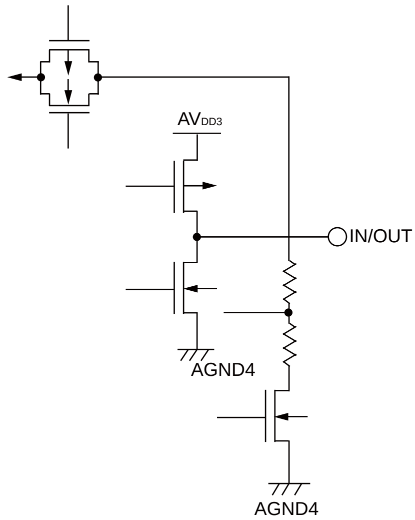
Pin Name	Equivalent Circuit	Pin Name	Equivalent Circuit
LPF_OUT HPF_OUT		DAC1_OUT/ VREFIN1 DAC2_OUT/ VREFIN2 DAC3_OUT/ VREFIN3	
LDO_OUT		DAC4_OUT/ VREFIN4	

Figure 1-1. Pin I/O Circuit Type (3/4)

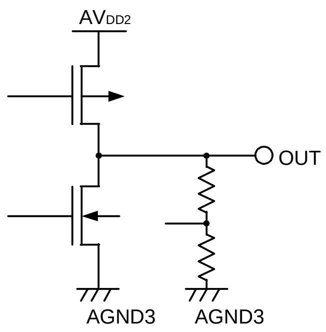
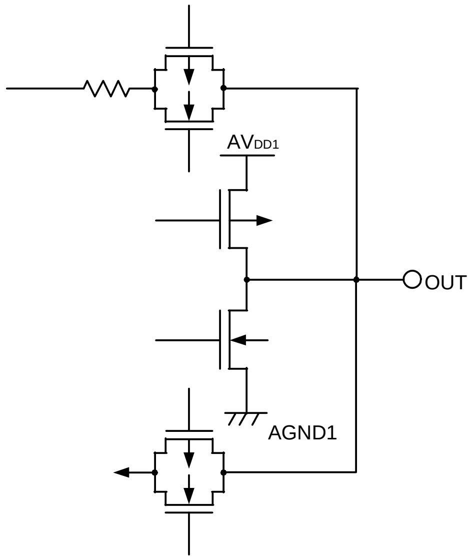
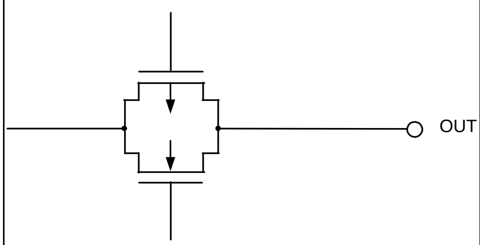
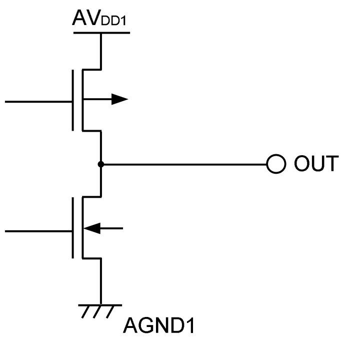
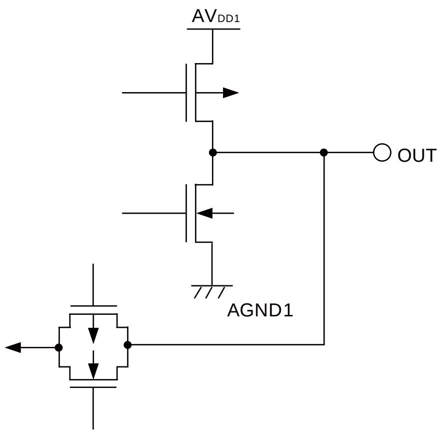
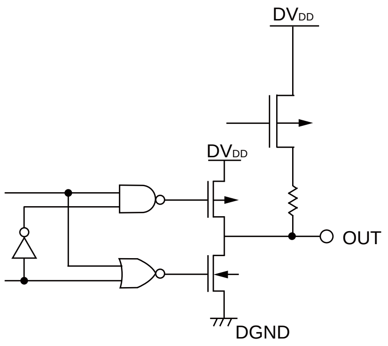
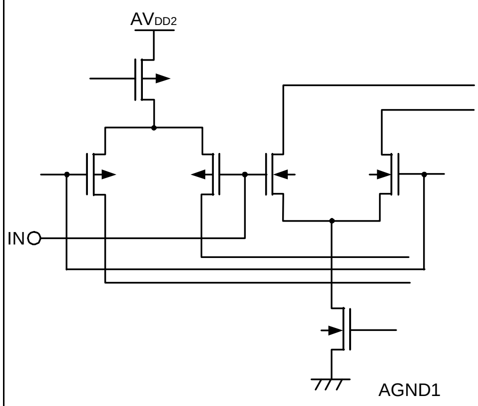
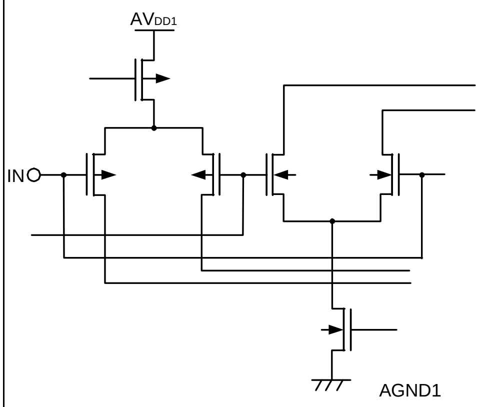
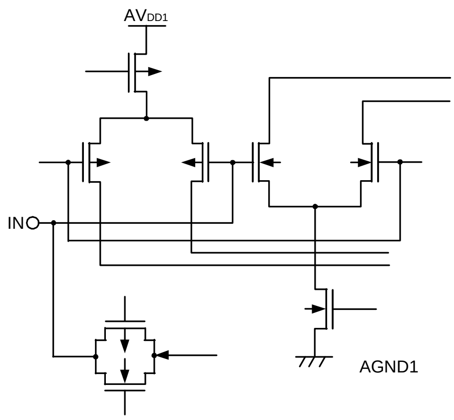
<table>
<tr><th>Pin Name</th><th>Equivalent Circuit</th><th>Pin Name</th><th>Equivalent Circuit</th></tr>
<tr><td>TEMP_OUT</td><td>
</td><td>AMP3_OUT</td><td>
</td></tr>
<tr><td>AMP1_OUT
AMP2_OUT</td><td>
</td><td>AMP4_OUT</td><td>
</td></tr>
<tr><td></td><td></td><td>AMP5_OUT</td><td>
</td></tr>
</table>

Figure 1-1. Pin I/O Circuit Type (4/4)

Pin Name	Equivalent Circuit	Pin Name	Equivalent Circuit
SDO		AMP4_INP	
AMP4_INN AMP5_INN		AMP5_INP	

2. Configurable Amplifiers

The RAA730300 has three on-chip configurable amplifier channels.

2.1 Overview of Configurable Amplifier Features

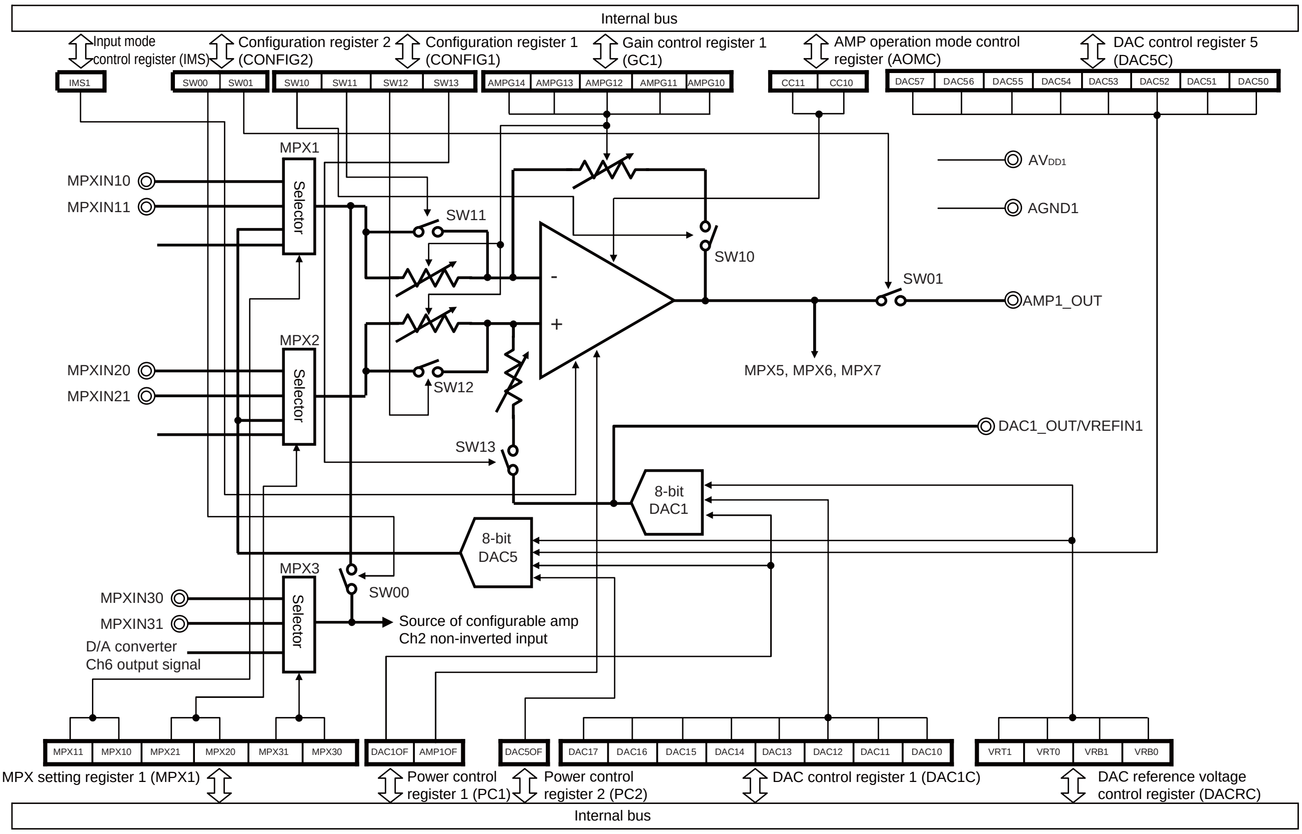
By specifying settings in the SPI control registers, the configurable amplifiers can be used to realize the following features:

- Single-channel operation
  - Non-inverting amplifier
    - The gain can be specified between 9.5 dB and 40.1 dB in 18 steps
    - Four operating modes are available
    - Includes an input mode switching function
    - Includes a power-off function
  - Inverting amplifier
    - The gain can be specified between 6 dB and 40 dB in 18 steps
    - Four operating modes are available
    - Includes an input mode switching function
    - Includes a power-off function
  - Differential amplifier
    - The gain can be specified between 6 dB and 40 dB in 18 steps
    - Four operating modes are available
    - Includes an input mode switching function
    - Includes a power-off function
  - Transimpedance amplifier
    - The feedback resistance can be specified between 20 kΩ and 640 kΩ in 6 steps
    - Four operating modes are available
    - Includes an input mode switching function
    - Includes a power-off function
  - General-purpose operational amplifier
    - Four operating modes are available
    - Includes an input mode switching function
    - Includes a power-off function
- Multiple-channel operation
  - Instrumentation amplifier
    - The gain can be specified between 15.5 dB and 33.5 dB in 10 steps
    - Four operating modes are available
    - Includes an input mode switching function
    - Includes a power-off function

<R> And also, the output signal from D/A converter Ch n (n = 1 to 3, 5 to 7) can be used as the reference voltage for each configurable amplifier. If D/A converters are powered off, the external reference voltage is to be input to DACn_OUT/VREFINn (n = 1 to 3) pin. For details about use of D/A converter, see **4. D/A Converter**.

2.2 Block Diagram

Figure 2-1. Block Diagram of Configurable Amplifier Ch1



<R> **Figure 2-2. Block Diagram of Configurable Amplifier Ch2**

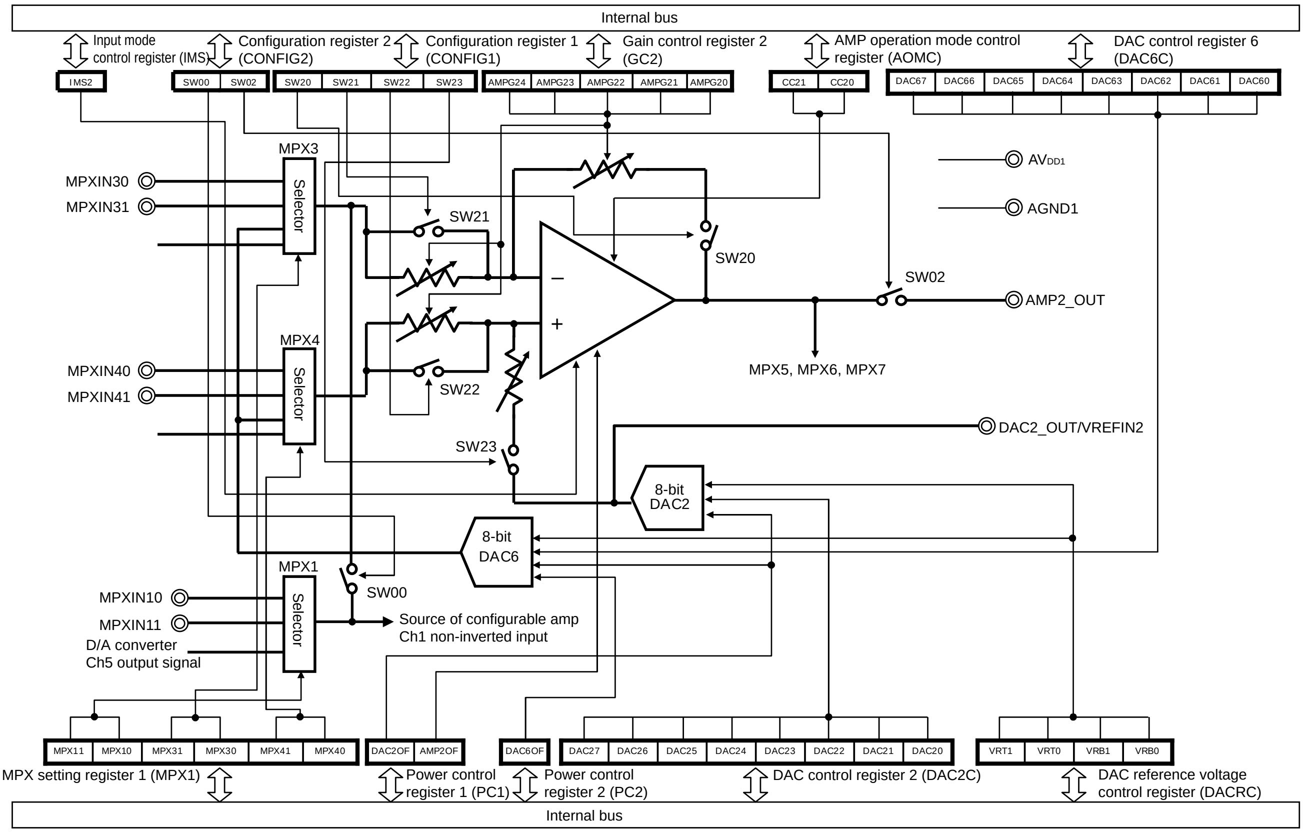
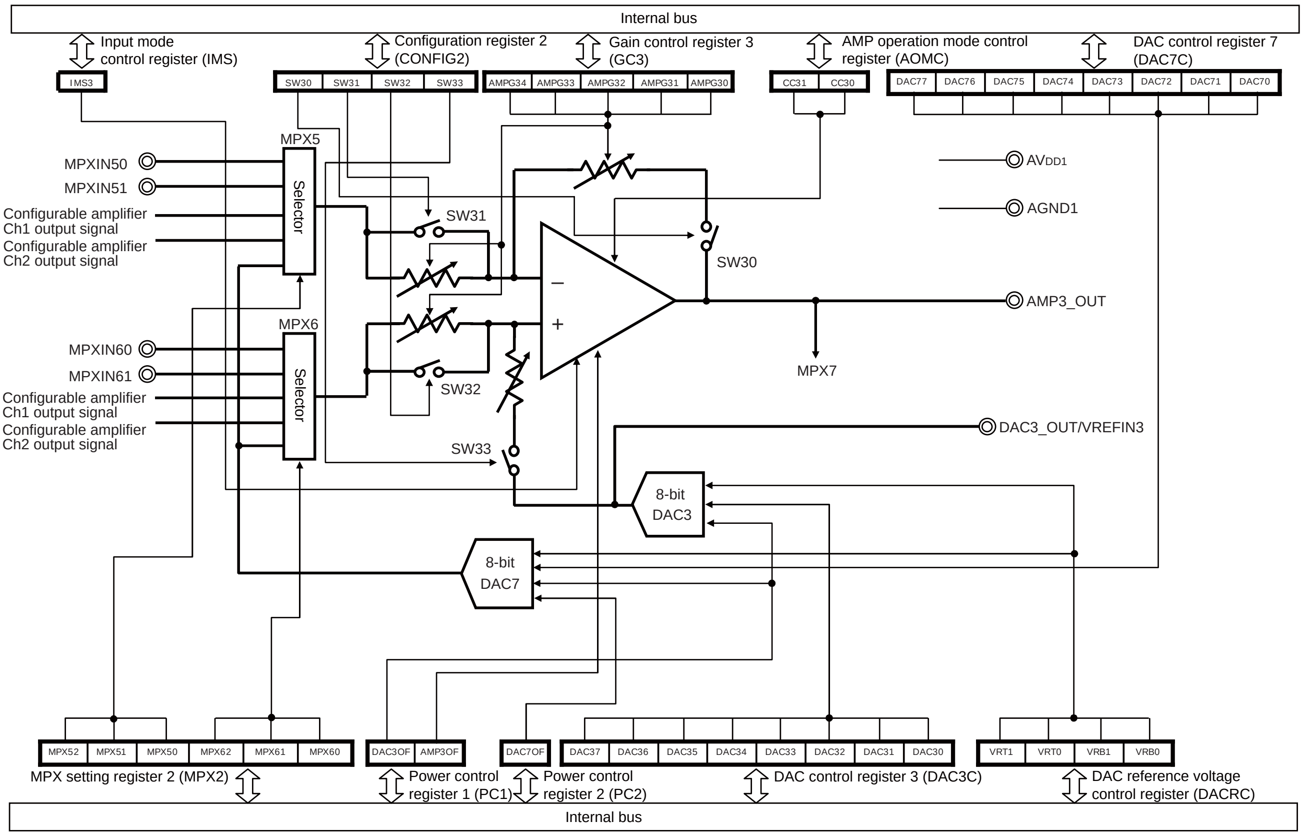


Figure 2-3. Block Diagram of Configurable Amplifier Ch3



2.3 Registers Controlling the Configurable Amplifiers

The configurable amplifiers are controlled by the following 10 registers:

- Configuration register 1 (CONFIG1)
- Configuration register 2 (CONFIG2)
- MPX setting register 1 (MPX1)
- MPX setting register 2 (MPX2)
- Gain control register 1 (GC1)
- Gain control register 2 (GC2)
- Gain control register 3 (GC3)
- AMP operation mode control register (AOMC)
- Power control register 1 (PC1)
- Input mode control register (IMS)

(1) Configuration register 1 (CONFIG1)

This register is used to turn on or off each switch of configurable amplifier channels Ch1 and Ch2.
Reset signal input sets this register to 88H.

Address: 00H After reset: 88H R/W

	7	6	5	4	3	2	1	0
CONFIG1	SW10	SW11	SW12	SW13	SW20	SW21	SW22	SW23

SW10	Control of SW10
0	Turn off SW10.
1	Turn on SW10.

SW11	Control of SW11
0	Turn off SW11.
1	Turn on SW11.

SW12	Control of SW12
0	Turn off SW12.
1	Turn on SW12.

SW13	Control of SW13
0	Turn off SW13.
1	Turn on SW13.

SW20	Control of SW20
0	Turn off SW20.
1	Turn on SW20.

SW21	Control of SW21
0	Turn off SW21.
1	Turn on SW21.

SW22	Control of SW22
0	Turn off SW22.
1	Turn on SW22.

SW23	Control of SW23
0	Turn off SW23.
1	Turn on SW23.

(2) Configuration register 2 (CONFIG2)

This register is used to turn on or off each switch of configurable amplifier channels Ch1 to Ch3.
Reset signal input sets this register to 80H.

Address: 01H After reset: 80H R/W

	7	6	5	4	3	2	1	0
CONFIG2	SW30	SW31	SW32	SW33	0	SW02	SW01	SW00

SW30	Control of SW30
0	Turn off SW30.
1	Turn on SW30.

SW31	Control of SW31
0	Turn off SW31.
1	Turn on SW31.

SW32	Control of SW32
0	Turn off SW32.
1	Turn on SW32.

SW33	Control of SW33
0	Turn off SW33.
1	Turn on SW33.

SW02	Control of SW02
0	Turn off SW02.
1	Turn on SW02.

SW01	Control of SW01
0	Turn off SW01.
1	Turn on SW01.

SW00	Control of SW00
0	Turn off SW00.
1	Turn on SW00.

Remark Bit 3 can be set to 1, but this has no effect on the function.

(3) MPX setting register 1 (MPX1)

This register is used to control MPX1, MPX2, MPX3, and MPX4.
This register is used to select the signal input to configurable amplifier channels Ch1 and Ch2.
Reset signal input clears this register to 00H.

Address: 03H After reset: 00H R/W

	7	6	5	4	3	2	1	0
MPX1	MPX11	MPX10	MPX21	MPX20	MPX31	MPX30	MPX41	MPX40

MPX11	MPX10	Source of configurable amplifier Ch1 inverted input
0	0	MPXIN10 pin
0	1	MPXIN11 pin
1	0	D/A converter Ch5 output signal
1	1	Open pin

MPX21	MPX20	Source of configurable amplifier Ch1 non-inverted input
0	0	MPXIN20 pin
0	1	MPXIN21 pin
1	0	D/A converter Ch5 output signal
1	1	Open pin

MPX31	MPX30	Source of configurable amplifier Ch2 inverted input
0	0	MPXIN30 pin
0	1	MPXIN31 pin
1	0	D/A converter Ch6 output signal
1	1	Open pin

MPX41	MPX40	Source of configurable amplifier Ch2 non-inverted input
0	0	MPXIN40 pin
0	1	MPXIN41 pin
1	0	D/A converter Ch6 output signal
1	1	Open pin

(4) MPX setting register 2 (MPX2)

This register is used to control MPX5 and MPX6.
This register is used to select the signal input to configurable amplifier Ch3.
Reset signal input clears this register to 00H.

Address: 04H After reset: 00H R/W

	7	6	5	4	3	2	1	0
MPX2	0	MPX52	MPX51	MPX50	0	MPX62	MPX61	MPX60

MPX52	MPX51	MPX50	Source of configurable amplifier Ch3 inverted input
0	0	0	MPXIN50 pin
0	0	1	MPXIN51 pin
0	1	0	Configurable amplifier Ch1 output signal
0	1	1	Configurable amplifier Ch2 output signal
1	0	0	D/A converter Ch7 output signal
Other than above			Setting prohibited

MPX62	MPX61	MPX60	Source of configurable amplifier Ch3 non-inverted input
0	0	0	MPXIN60 pin
0	0	1	MPXIN61 pin
0	1	0	Output signal of configurable amplifier Ch1
0	1	1	Configurable amplifier Ch2 output signal
1	0	0	D/A converter Ch7 output signal
Other than above			Setting prohibited

Remark Bits 7 and 3 can be set to 1, but this has no effect on the function.

(5) Gain control register 1 (GC1)

This register is used to specify the gain and feedback resistance of configurable amplifier Ch1.
The value to specify depends on the configuration of configurable amplifier Ch1.
When using configurable amplifier channels Ch1 to Ch3 together as an instrumentation amplifier, be sure to set gain control register 1 (GC1) to 00H.
Reset signal input clears this register to 00H.

Address: 06H After reset: 00H R/W

	7	6	5	4	3	2	1	0
GC1	0	0	0	AMPG14	AMPG13	AMPG12	AMPG11	AMPG10

Table 2-1. Gain of Configurable Amplifier Ch1 (Non-Inverting Amplifier)

AMPG14	AMPG13	AMPG12	AMPG11	AMPG10	Gain of Configurable Amplifier Ch1 (Typ.)
0	0	0	0	0	9.5 dB
0	0	0	0	1	10.9 dB
0	0	0	1	0	12.4 dB
0	0	0	1	1	14.0 dB
0	0	1	0	0	15.6 dB
0	0	1	0	1	17.3 dB
0	0	1	1	0	19.0 dB
0	0	1	1	1	20.8 dB
0	1	0	0	0	22.7 dB
0	1	0	0	1	24.5 dB
0	1	0	1	0	26.4 dB
0	1	0	1	1	28.3 dB
0	1	1	0	0	30.3 dB
0	1	1	0	1	32.2 dB
0	1	1	1	0	34.2 dB
0	1	1	1	1	36.1 dB
1	0	0	0	0	38.1 dB
1	0	0	0	1	40.1 dB
Other than above					Setting prohibited

Remark Bits 7 to 5 can be set to 1, but this has no effect on the function.

Table 2-2. Gain of Configurable Amplifier Ch1 (Inverting Amplifier and Differential Amplifier)

AMPG14	AMPG13	AMPG12	AMPG11	AMPG10	Gain of Configurable Amplifier Ch1 (Typ.)
0	0	0	0	0	6 dB
0	0	0	0	1	8 dB
0	0	0	1	0	10 dB
0	0	0	1	1	12 dB
0	0	1	0	0	14 dB
0	0	1	0	1	16 dB
0	0	1	1	0	18 dB
0	0	1	1	1	20 dB
0	1	0	0	0	22 dB
0	1	0	0	1	24 dB
0	1	0	1	0	26 dB
0	1	0	1	1	28 dB
0	1	1	0	0	30 dB
0	1	1	0	1	32 dB
0	1	1	1	0	34 dB
0	1	1	1	1	36 dB
1	0	0	0	0	38 dB
1	0	0	0	1	40 dB
Other than above					Setting prohibited

Table 2-3. Feedback Resistance of Configurable Amplifier Ch1 (Transimpedance Amplifier)

AMPG14	AMPG13	AMPG12	AMPG11	AMPG10	Feedback Resistance of Configurable Amplifier Ch1 (Typ.)
0	0	0	0	0	20 kΩ
0	0	0	0	1	
0	0	0	1	0	
0	0	0	1	1	40 kΩ
0	0	1	0	0	
0	0	1	0	1	
0	0	1	1	0	80 kΩ
0	0	1	1	1	
0	1	0	0	0	
0	1	0	0	1	160 kΩ
0	1	0	1	0	
0	1	0	1	1	
0	1	1	0	0	320 kΩ
0	1	1	0	1	
0	1	1	1	0	
0	1	1	1	1	640 kΩ
1	0	0	0	0	
1	0	0	0	1	
Other than above					Setting prohibited

(6) Gain control register 2 (GC2)

This register is used to specify the gain and feedback resistance of configurable amplifier Ch2.
The value to specify depends on the configuration of configurable amplifier Ch2.
When using configurable amplifier channels Ch1 to Ch3 together as an instrumentation amplifier, be sure to set gain control register 2 (GC2) to 00H.
Reset signal input clears this register to 00H.

Address: 07H After reset: 00H R/W

	7	6	5	4	3	2	1	0
GC2	0	0	0	AMPG24	AMPG23	AMPG22	AMPG21	AMPG20

Table 2-4. Gain of Configurable Amplifier Ch2 (Non-Inverting Amplifier)

AMPG24	AMPG23	AMPG22	AMPG21	AMPG20	Gain of Configurable Amplifier Ch2 (Typ.)
0	0	0	0	0	9.5 dB
0	0	0	0	1	10.9 dB
0	0	0	1	0	12.4 dB
0	0	0	1	1	14.0 dB
0	0	1	0	0	15.6 dB
0	0	1	0	1	17.3 dB
0	0	1	1	0	19.0 dB
0	0	1	1	1	20.8 dB
0	1	0	0	0	22.7 dB
0	1	0	0	1	24.5 dB
0	1	0	1	0	26.4 dB
0	1	0	1	1	28.3 dB
0	1	1	0	0	30.3 dB
0	1	1	0	1	32.2 dB
0	1	1	1	0	34.2 dB
0	1	1	1	1	36.1 dB
1	0	0	0	0	38.1 dB
1	0	0	0	1	40.1 dB
Other than above					Setting prohibited

Remark Bits 7 to 5 can be set to 1, but this has no effect on the function.

Table 2-5. Gain of Configurable Amplifier Ch2 (Inverting Amplifier and Differential Amplifier)

AMPG24	AMPG23	AMPG22	AMPG21	AMPG20	Gain of Configurable Amplifier Ch2 (Typ.)
0	0	0	0	0	6 dB
0	0	0	0	1	8 dB
0	0	0	1	0	10 dB
0	0	0	1	1	12 dB
0	0	1	0	0	14 dB
0	0	1	0	1	16 dB
0	0	1	1	0	18 dB
0	0	1	1	1	20 dB
0	1	0	0	0	22 dB
0	1	0	0	1	24 dB
0	1	0	1	0	26 dB
0	1	0	1	1	28 dB
0	1	1	0	0	30 dB
0	1	1	0	1	32 dB
0	1	1	1	0	34 dB
0	1	1	1	1	36 dB
1	0	0	0	0	38 dB
1	0	0	0	1	40 dB
Other than above					Setting prohibited

Table 2-6. Feedback Resistance of Configurable Amplifier Ch2 (Transimpedance Amplifier)

AMPG24	AMPG23	AMPG22	AMPG21	AMPG20	Feedback Resistance of Configurable Amplifier Ch2 (Typ.)
0	0	0	0	0	20 kΩ
0	0	0	0	1	
0	0	0	1	0	
0	0	0	1	1	40 kΩ
0	0	1	0	0	
0	0	1	0	1	
0	0	1	1	0	80 kΩ
0	0	1	1	1	
0	1	0	0	0	
0	1	0	0	1	160 kΩ
0	1	0	1	0	
0	1	0	1	1	
0	1	1	0	0	320 kΩ
0	1	1	0	1	
0	1	1	1	0	
0	1	1	1	1	640 kΩ
1	0	0	0	0	
1	0	0	0	1	
Other than above					Setting prohibited

(7) Gain control register 3 (GC3)

This register is used to specify the gain and feedback resistance of configurable amplifier Ch3.
The value to specify depends on the configuration of configurable amplifier Ch3.
When using configurable amplifier channels Ch1 to Ch3 together as an instrumentation amplifier, be sure to set gain control register 1 (GC1) and gain control register 2 (GC2) to 00H, respectively.
Reset signal input clears this register to 00H.

Address: 08H After reset: 00H R/W

	7	6	5	4	3	2	1	0
GC3	0	0	0	AMPG34	AMPG33	AMPG32	AMPG31	AMPG30

Table 2-7. Gain of Configurable Amplifier Ch3 (Non-Inverting Amplifier)

AMPG34	AMPG33	AMPG32	AMPG31	AMPG30	Gain of Configurable Amplifier Ch3 (Typ.)
0	0	0	0	0	9.5 dB
0	0	0	0	1	10.9 dB
0	0	0	1	0	12.4 dB
0	0	0	1	1	14.0 dB
0	0	1	0	0	15.6 dB
0	0	1	0	1	17.3 dB
0	0	1	1	0	19.0 dB
0	0	1	1	1	20.8 dB
0	1	0	0	0	22.7 dB
0	1	0	0	1	24.5 dB
0	1	0	1	0	26.4 dB
0	1	0	1	1	28.3 dB
0	1	1	0	0	30.3 dB
0	1	1	0	1	32.2 dB
0	1	1	1	0	34.2 dB
0	1	1	1	1	36.1 dB
1	0	0	0	0	38.1 dB
1	0	0	0	1	40.1 dB
Other than above					Setting prohibited

Remark Bits 7 to 5 can be set to 1, but this has no effect on the function.

Table 2-8. Gain of Configurable Amplifier Ch3 (Inverting Amplifier and Differential Amplifier)

AMPG34	AMPG33	AMPG32	AMPG31	AMPG30	Gain of Configurable Amplifier Ch3 (Typ.)
0	0	0	0	0	6 dB
0	0	0	0	1	8 dB
0	0	0	1	0	10 dB
0	0	0	1	1	12 dB
0	0	1	0	0	14 dB
0	0	1	0	1	16 dB
0	0	1	1	0	18 dB
0	0	1	1	1	20 dB
0	1	0	0	0	22 dB
0	1	0	0	1	24 dB
0	1	0	1	0	26 dB
0	1	0	1	1	28 dB
0	1	1	0	0	30 dB
0	1	1	0	1	32 dB
0	1	1	1	0	34 dB
0	1	1	1	1	36 dB
1	0	0	0	0	38 dB
1	0	0	0	1	40 dB
Other than above					Setting prohibited

Table 2-9. Feedback Resistance of Configurable Amplifier Ch3 (Transimpedance Amplifier)

AMPG34	AMPG33	AMPG32	AMPG31	AMPG30	Feedback Resistance of Configurable Amplifier Ch3 (Typ.)
0	0	0	0	0	20 kΩ
0	0	0	0	1	
0	0	0	1	0	
0	0	0	1	1	40 kΩ
0	0	1	0	0	
0	0	1	0	1	
0	0	1	1	0	80 kΩ
0	0	1	1	1	
0	1	0	0	0	
0	1	0	0	1	160 kΩ
0	1	0	1	0	
0	1	0	1	1	
0	1	1	0	0	320 kΩ
0	1	1	0	1	
0	1	1	1	0	
0	1	1	1	1	640 kΩ
1	0	0	0	0	
1	0	0	0	1	
Other than above					Setting prohibited

Table 2-10. Gain of Configurable Amplifier Ch3 (Instrumentation Amplifier)

AMPG34	AMPG33	AMPG32	AMPG31	AMPG30	Gain of Configurable Amplifier Ch3 (Typ.)
0	0	0	0	0	15.5 dB
0	0	0	0	1	17.5 dB
0	0	0	1	0	19.5 dB
0	0	0	1	1	21.5 dB
0	0	1	0	0	23.5 dB
0	0	1	0	1	25.5 dB
0	0	1	1	0	27.5 dB
0	0	1	1	1	29.5 dB
0	1	0	0	0	31.5 dB
0	1	0	0	1	33.5 dB
Other than above					Setting prohibited

(8) AMP operation mode control register (AOMC)

This register is used to specify the operating mode of configurable amplifiers Ch1 to Ch3.
Reset signal input clears this register to 00H.

Address: 09H After reset: 00H R/W

	7	6	5	4	3	2	1	0
AOMC	0	0	CC31	CC30	CC21	CC20	CC11	CC10

CC31	CC30	Operating mode of configurable amplifier Ch3
0	0	High-speed mode
0	1	Mid-speed mode 2
1	0	Mid-speed mode 1
1	1	Low-speed mode

CC21	CC20	Operating mode of configurable amplifier Ch2
0	0	High-speed mode
0	1	Mid-speed mode 2
1	0	Mid-speed mode 1
1	1	Low-speed mode

CC11	CC10	Operating mode of configurable amplifier Ch1
0	0	High-speed mode
0	1	Mid-speed mode 2
1	0	Mid-speed mode 1
1	1	Low-speed mode

Remark Bits 7 and 6 can be set to 1, but this has no effect on the function.

<R> **(9) Power control register 1 (PC1)**

This register is used to enable or disable operation of the configurable amplifiers, general-purpose operational amplifiers, and the D/A converters.
Use this register to stop unused functions to reduce power consumption and noise.
When using one of configurable amplifier channels Ch1 to Ch3, be sure to set the control bit that corresponds to the channel (bits 2 to 0) to 1.
Reset signal input clears this register to 00H.

Address: 11H After reset: 00H R/W

	7	6	5	4	3	2	1	0
PC1	DAC4OF	DAC3OF	DAC2OF	DAC1OF	AMP4OF	AMP3OF	AMP2OF	AMP1OF

AMP3OF	Operation of configurable amplifier Ch3
0	Stop operation of configurable amplifier Ch3.
1	Enable operation of configurable amplifier Ch3.

AMP2OF	Operation of configurable amplifier Ch2
0	Stop operation of configurable amplifier Ch2.
1	Enable operation of configurable amplifier Ch2.

AMP1OF	Operation of configurable amplifier Ch1
0	Stop operation of configurable amplifier Ch1.
1	Enable operation of configurable amplifier Ch1.

(10) Input mode control register (IMS)

This register is used to specify the input mode of the configurable amplifiers, general-purpose operational amplifiers, the low-pass filter, and high-pass filter.
When using one of configurable amplifier channels Ch1 to Ch3, be sure to set the control bit that corresponds to the channel (bits 2 to 0).

Address: 14H After reset: 00H R/W

	7	6	5	4	3	2	1	0
IMS	0	0	IMS6	IMS5	IMS4	IMS3	IMS2	IMS1

IMS3	Input mode of configurable amplifier Ch3
0	Rail-to-rail input mode
1	P-ch single-ended input mode

IMS2	Input mode of configurable amplifier Ch2
0	Rail-to-rail input mode
1	P-ch single-ended input mode

IMS1	Input mode of configurable amplifier Ch1
0	Rail-to-rail input mode
1	P-ch single-ended input mode

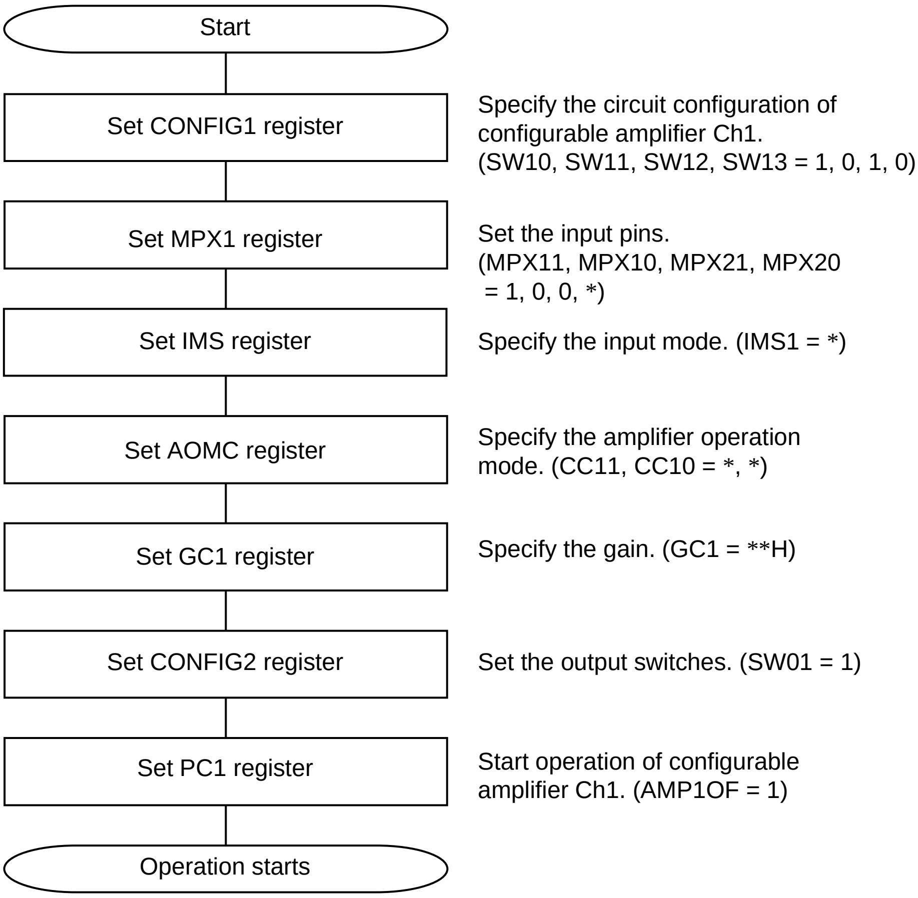
Remark Bits 7 and 6 can be set to 1, but this has no effect on the function.

2.4 Procedure for Operating the Configurable Amplifiers

(1) Procedure when using the amplifiers as non-inverting amplifiers

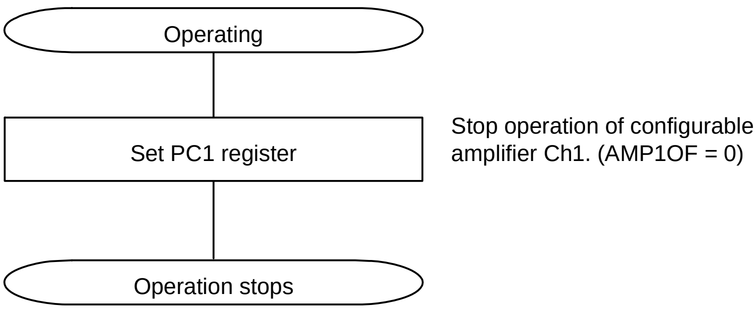
When using the configurable amplifiers as non-inverting amplifiers, follow the procedures below to start and stop the amplifiers.

Example of procedure for starting configurable amplifier Ch1 (non-inverting amplifier)

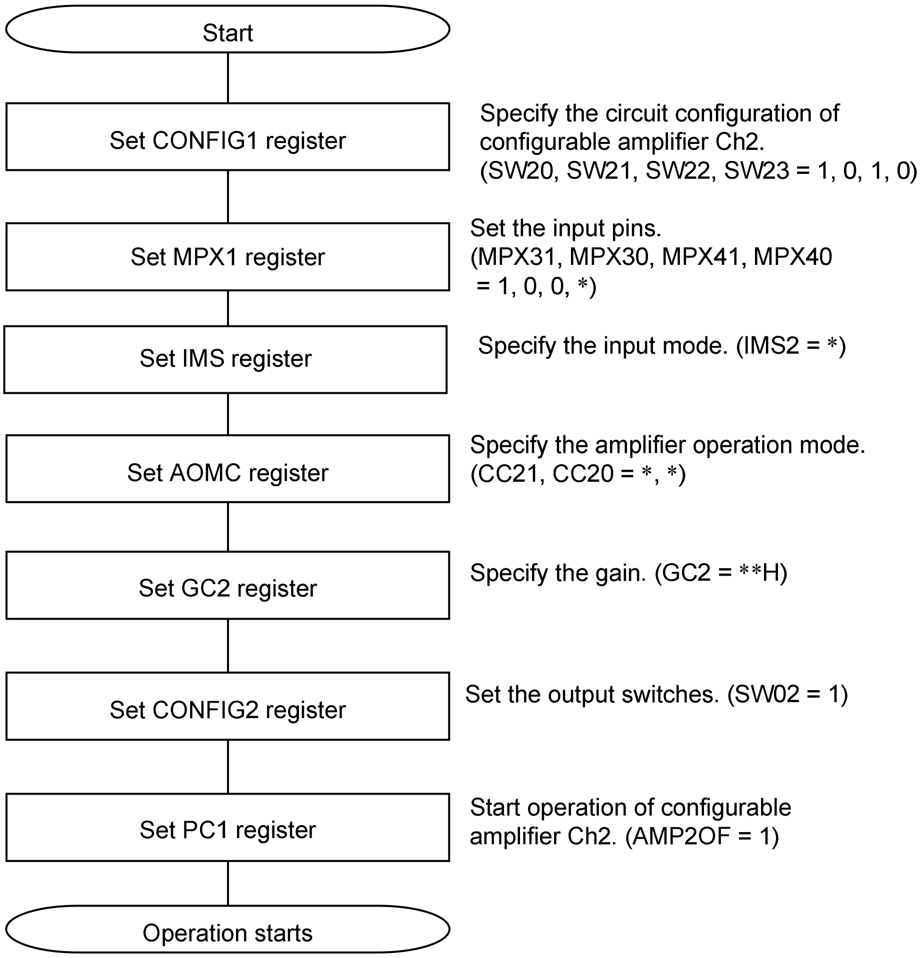


Remark *: don't care

Example of procedure for stopping configurable amplifier Ch1 (non-inverting amplifier)

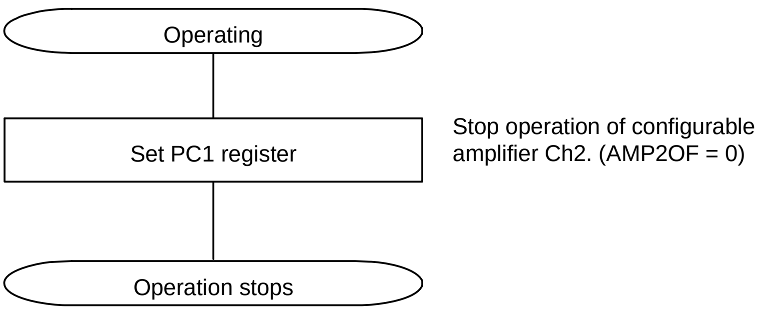


Example of procedure for starting configurable amplifier Ch2 (non-inverting amplifier)

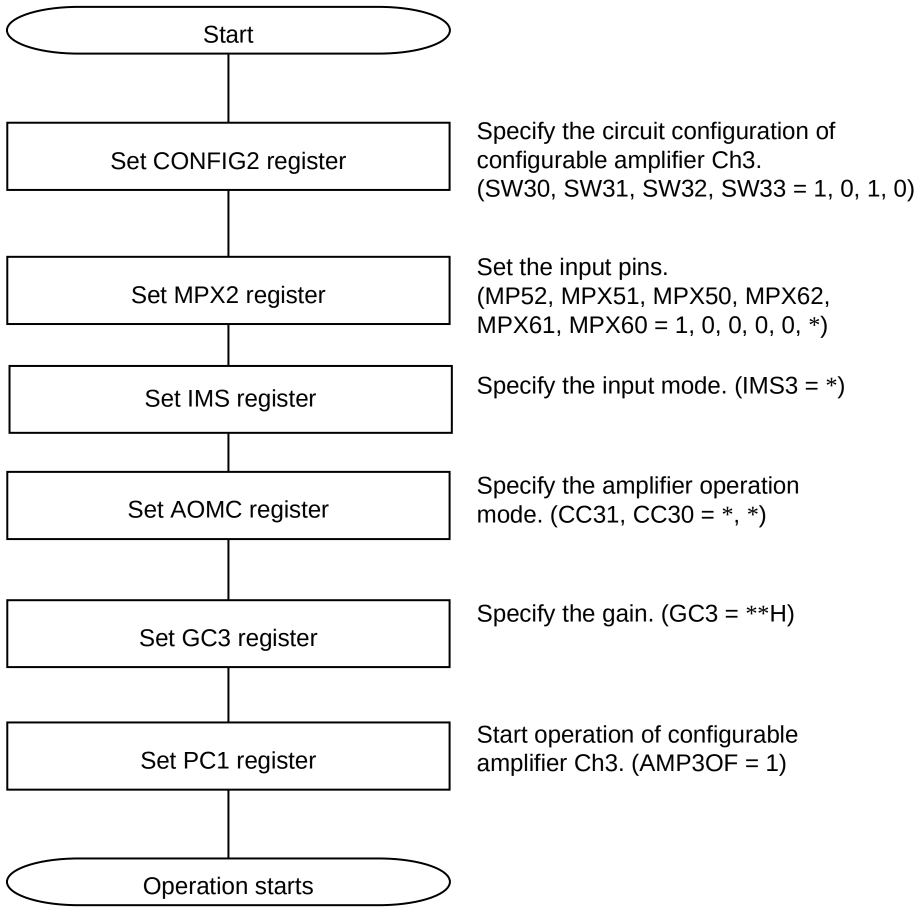


Remark *: don't care

Example of procedure for stopping configurable amplifier Ch2 (non-inverting amplifier)

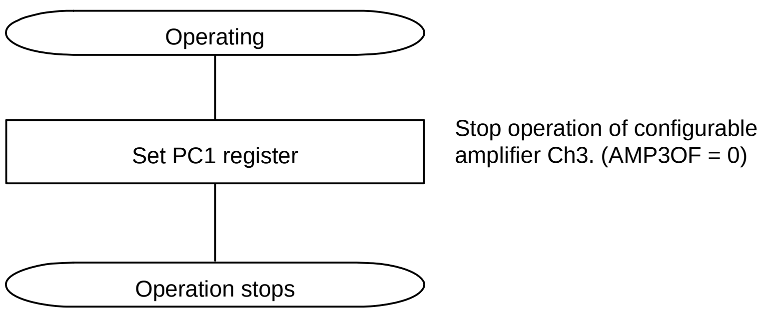


Example of procedure for starting configurable amplifier Ch3 (non-inverting amplifier)



Remark *: don't care

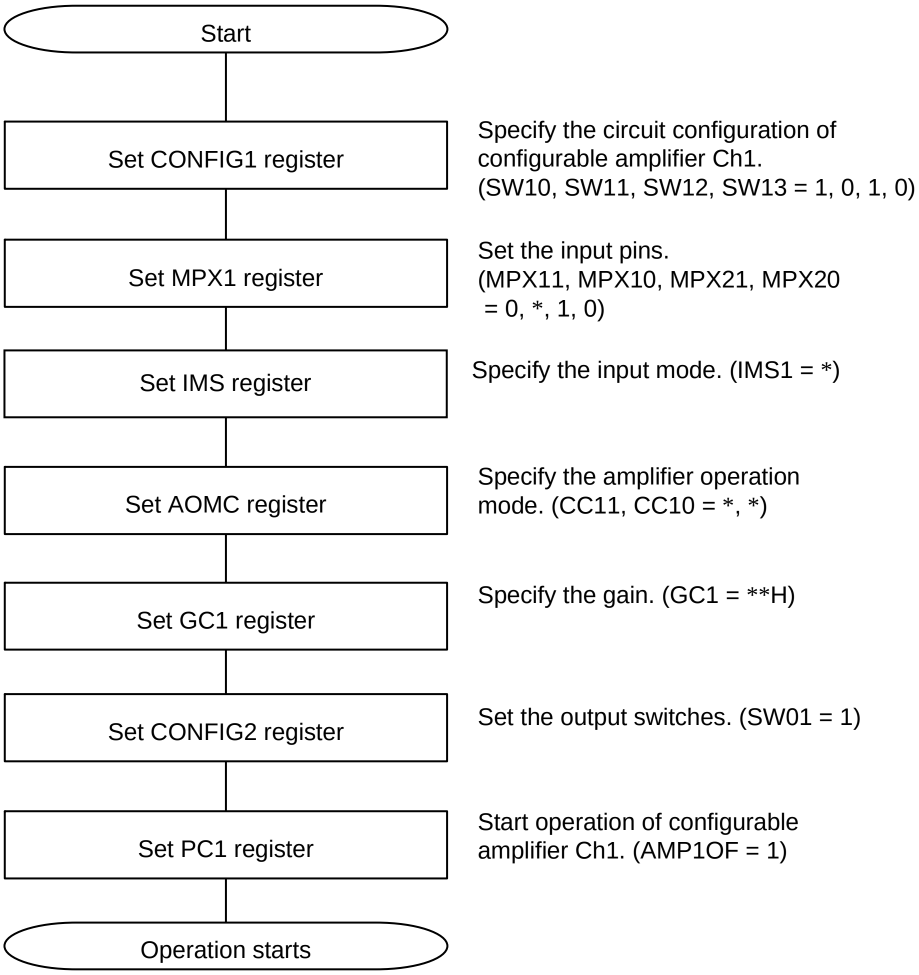
Example of procedure for stopping configurable amplifier Ch3 (non-inverting amplifier)



(2) Procedure when using the amplifiers as inverting amplifiers

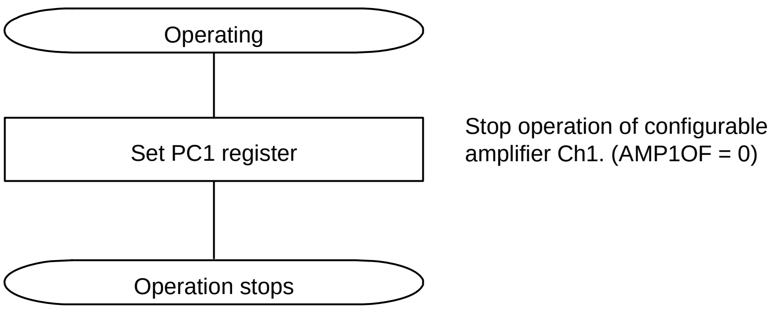
When using the configurable amplifiers as inverting amplifiers, follow the procedures below to start and stop the amplifiers.

Example of procedure for starting configurable amplifier Ch1 (inverting amplifier)

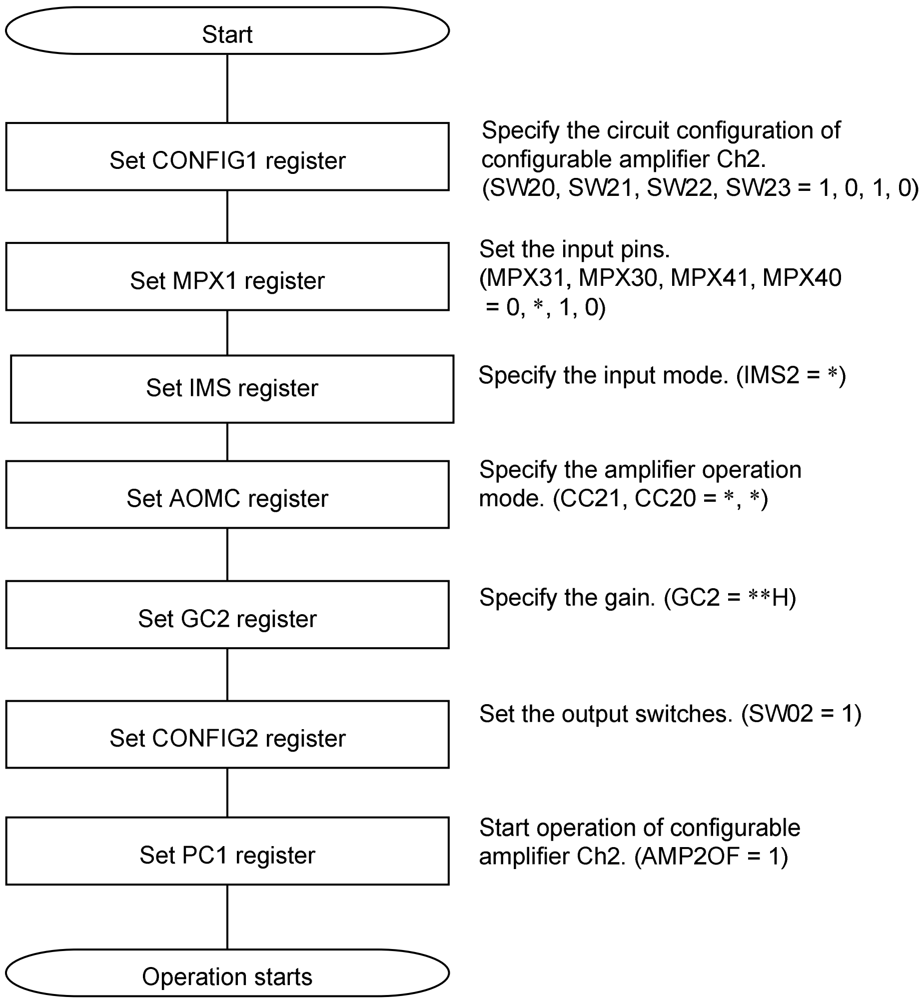


Remark *: don't care

Example of procedure for stopping configurable amplifier Ch1 (inverting amplifier)

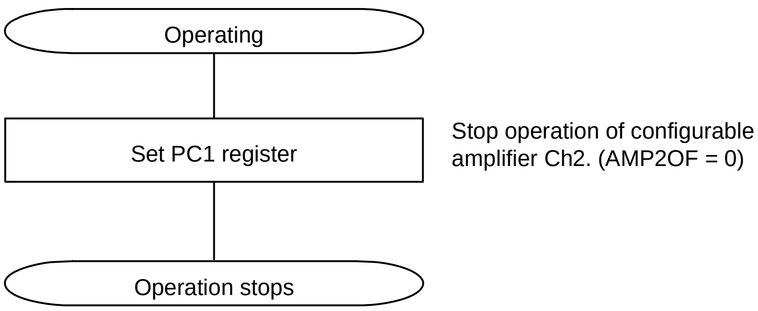


Example of procedure for starting configurable amplifier Ch2 (inverting amplifier)

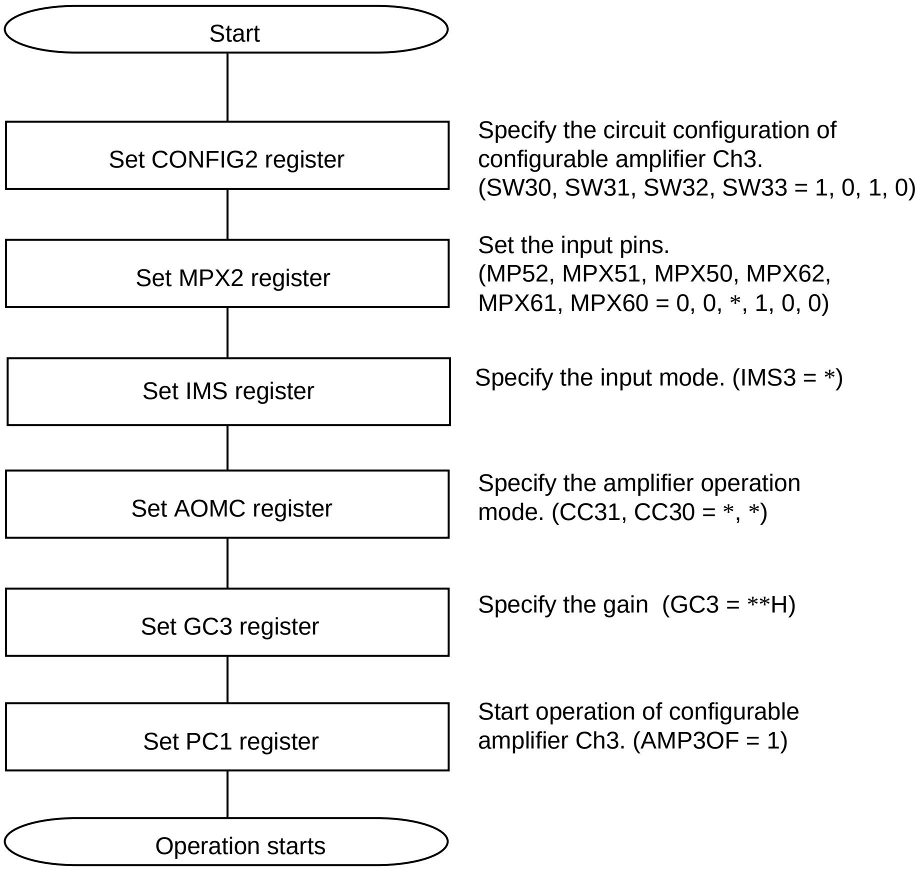


Remark *: don't care

Example of procedure for stopping configurable amplifier Ch2 (inverting amplifier)

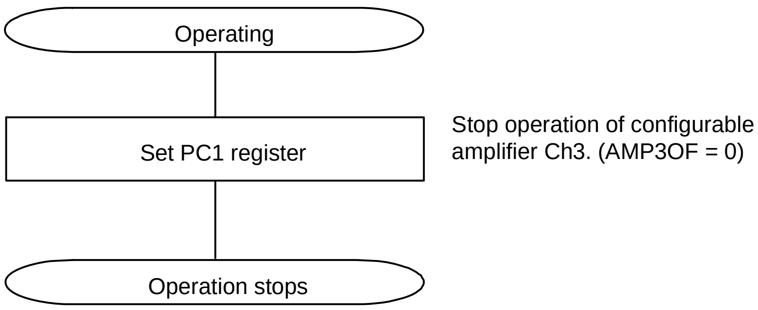


Example of procedure for starting configurable amplifier Ch3 (inverting amplifier)



Remark *: don't care

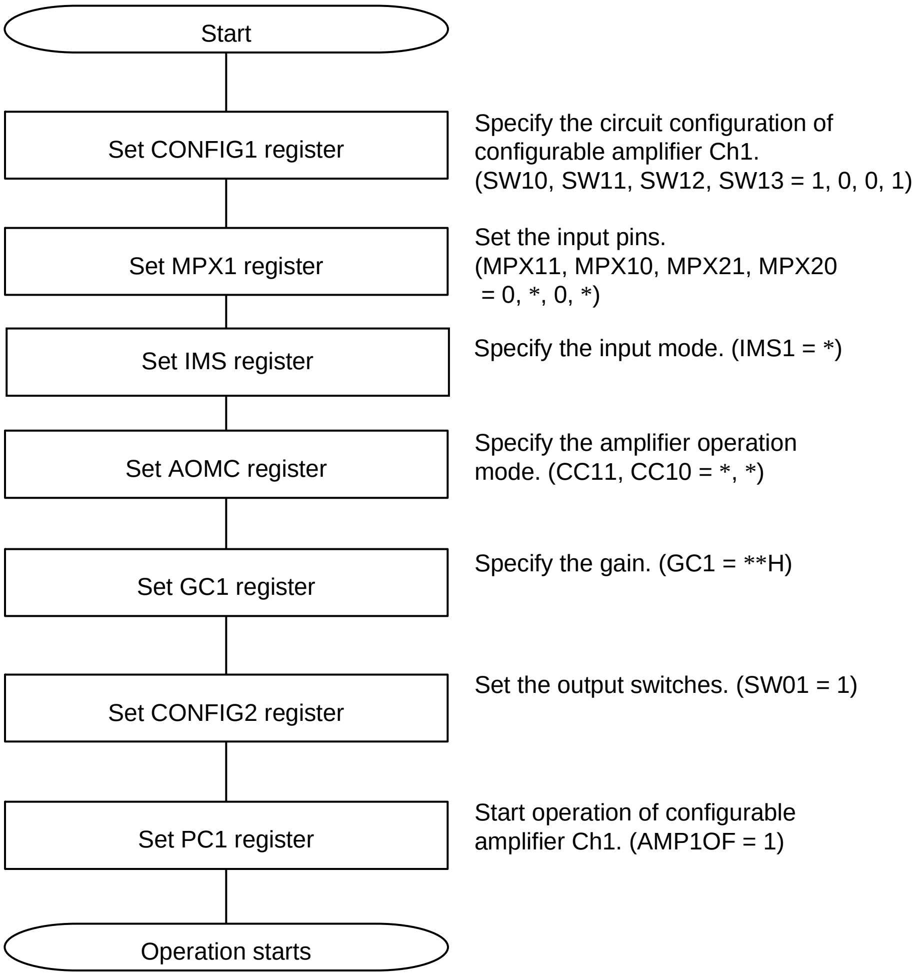
Example of procedure for stopping configurable amplifier Ch3 (inverting amplifier)



(3) Procedure when using the amplifiers as differential amplifiers

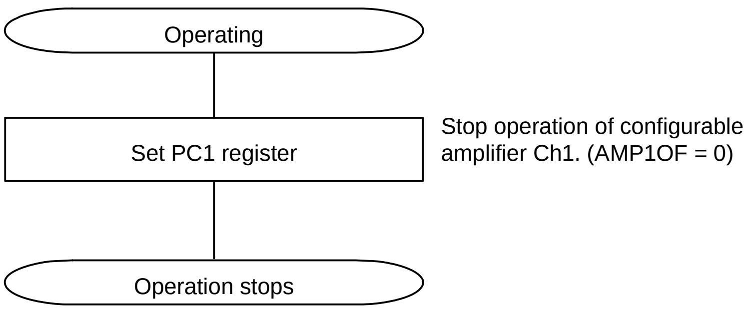
When using the configurable amplifiers together as a differential amplifier, follow the procedures below to start and stop the amplifier.

Example of procedure for starting configurable amplifier Ch1 (differential amplifier)

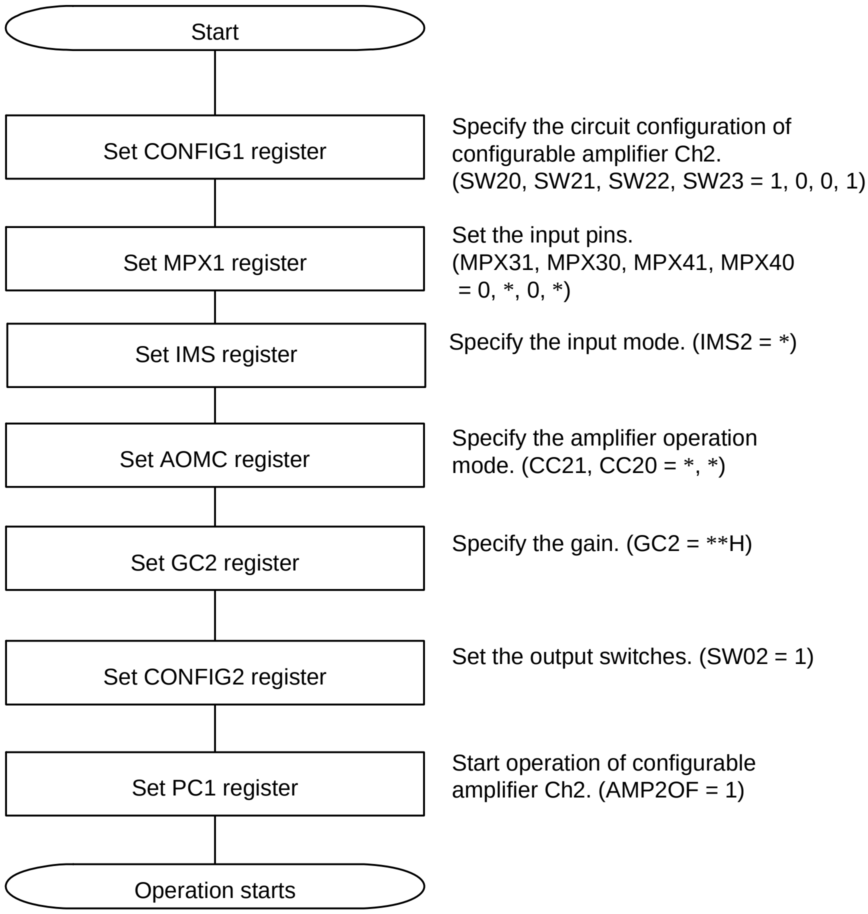


Remark *: don't care

Example of procedure for stopping configurable amplifier Ch1 (differential amplifier)

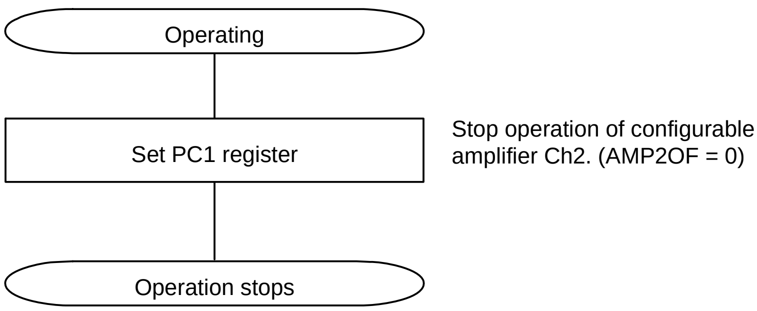


Example of procedure for starting configurable amplifier Ch2 (differential amplifier)

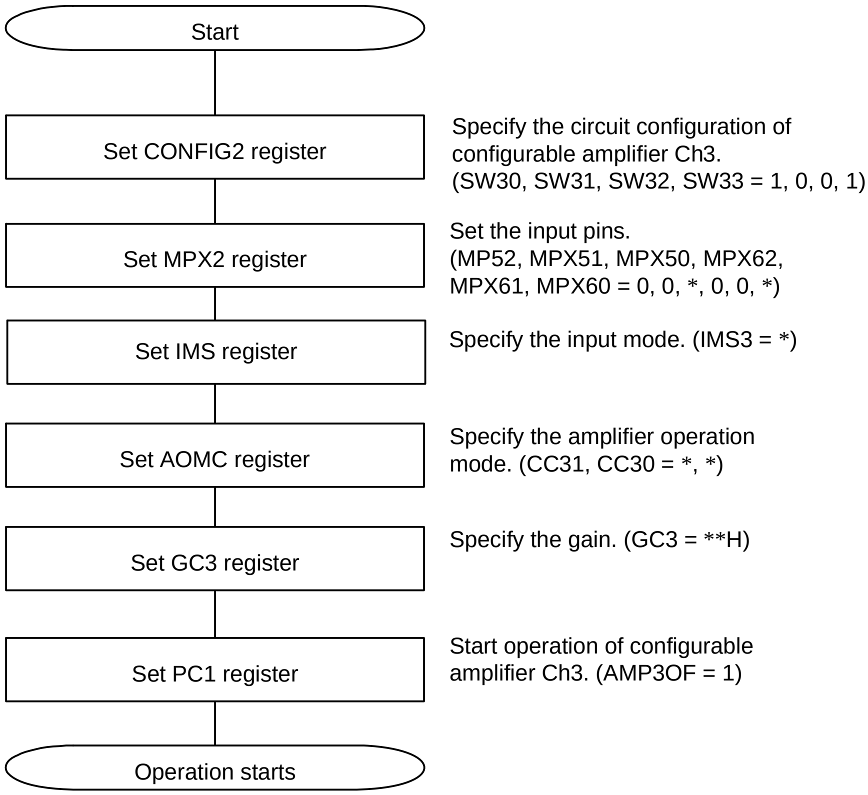


Remark *: don't care

Example of procedure for stopping configurable amplifier Ch2 (differential amplifier)

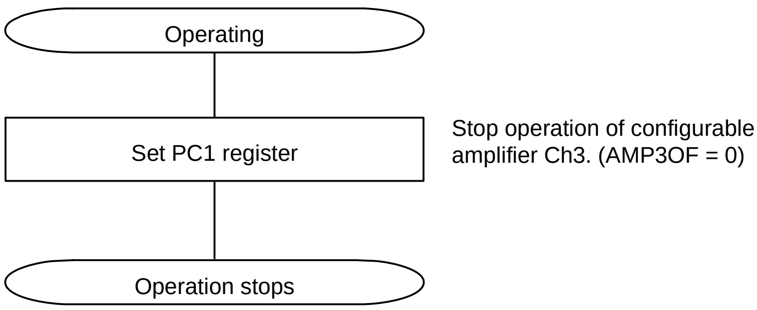


Example of procedure for starting configurable amplifier Ch3 (differential amplifier)



Remark *: don't care

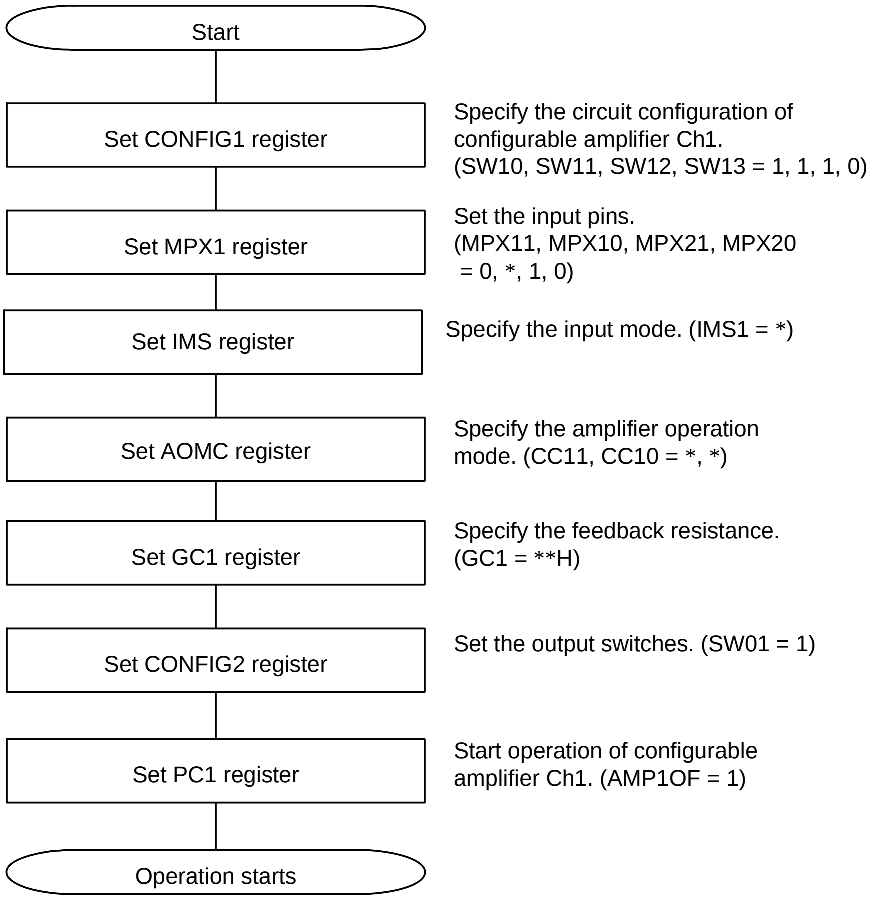
Example of procedure for stopping configurable amplifier Ch3 (differential amplifier)



(4) Procedure when using the amplifiers as a transimpedance amplifier

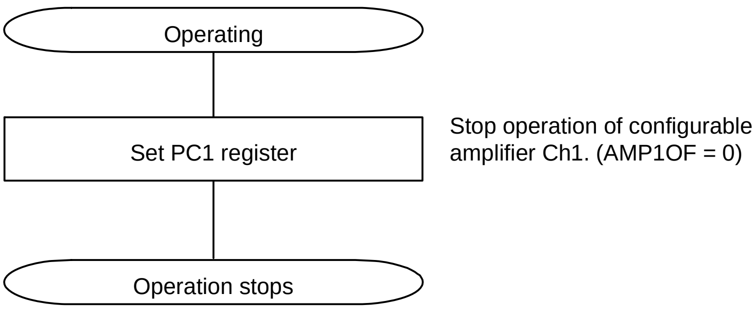
When using the configurable amplifiers as transimpedance amplifiers, follow the procedures below to start and stop the amplifiers.

Example of procedure for starting configurable amplifier Ch1 (transimpedance amplifier)

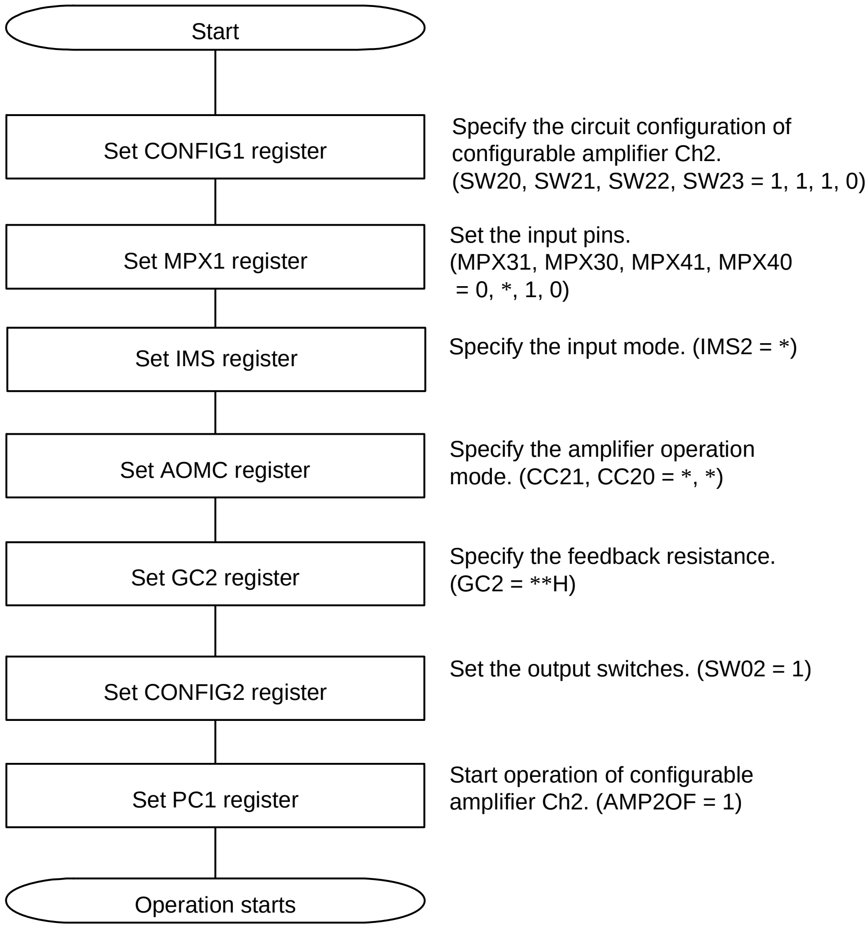


Remark *: don't care

Example of procedure for stopping configurable amplifier Ch1 (transimpedance amplifier)

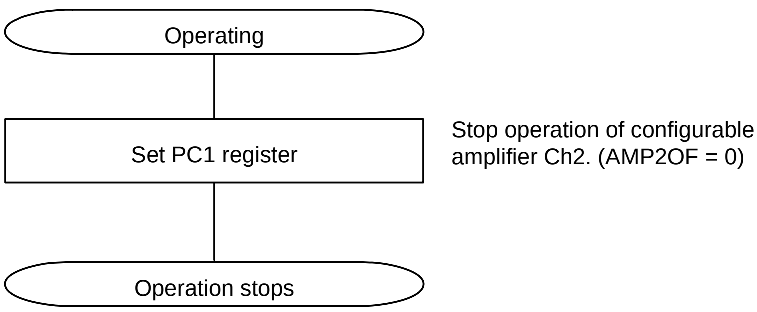


Example of procedure for starting configurable amplifier Ch2 (transimpedance amplifier)

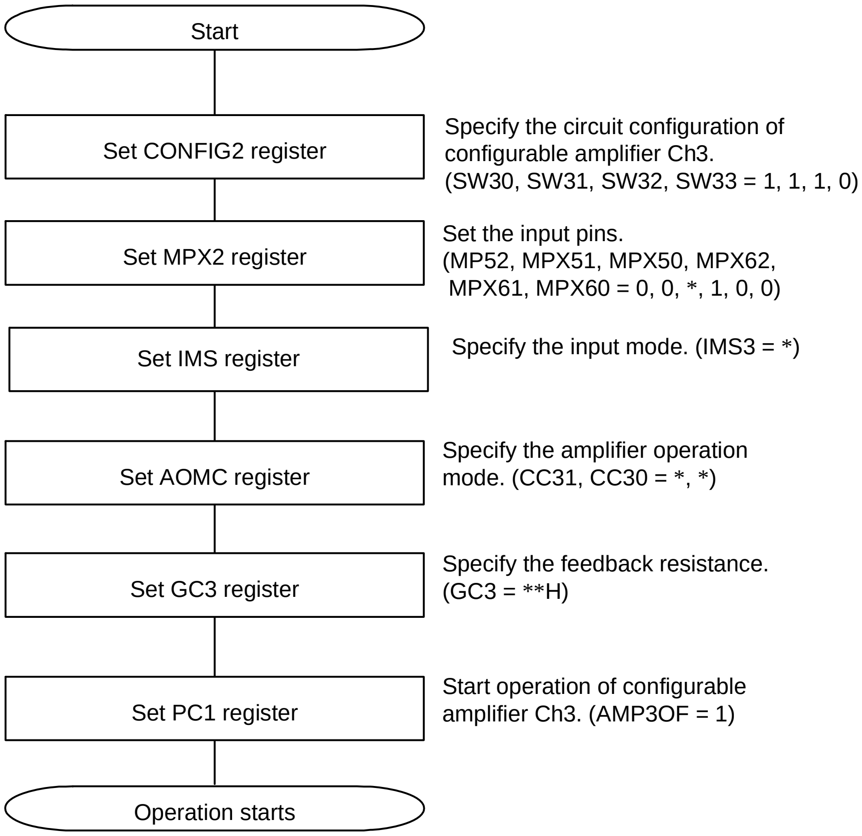


Remark *: don't care

Example of procedure for stopping configurable amplifier Ch2 (transimpedance amplifier)

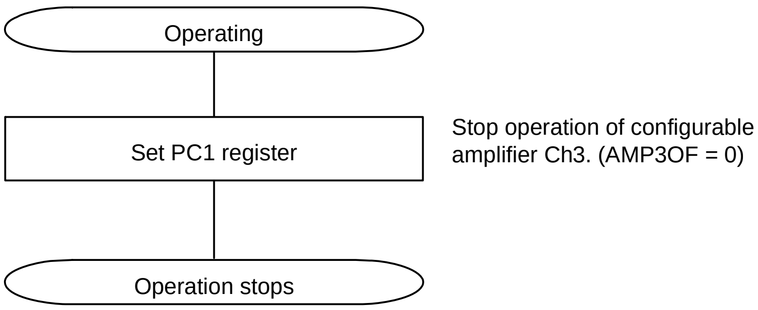


Example of procedure for starting configurable amplifier Ch3 (transimpedance amplifier)



Remark *: don't care

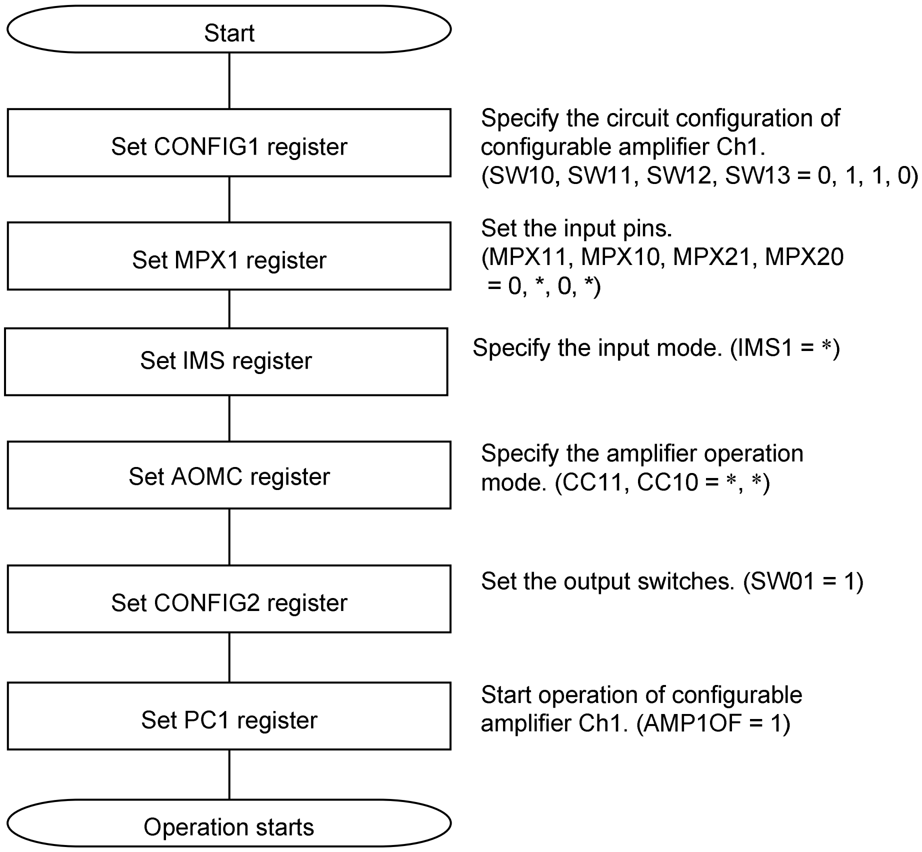
Example of procedure for stopping configurable amplifier Ch3 (transimpedance amplifier)



(5) Procedure when using the amplifiers as a general-purpose operational amplifier

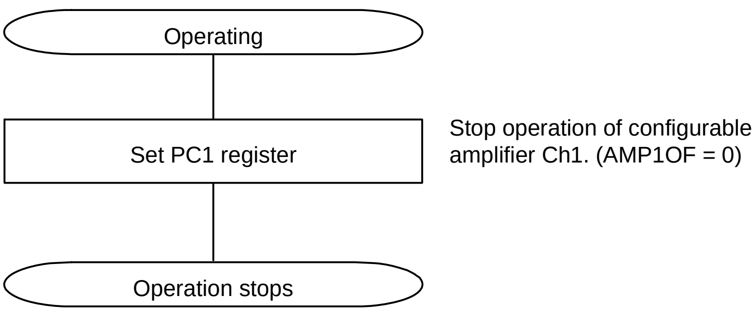
When using the configurable amplifiers as general-purpose operational amplifiers, follow the procedures below to start and stop the amplifiers.

Example of procedure for starting configurable amplifier Ch1 (general-purpose operational amplifier)

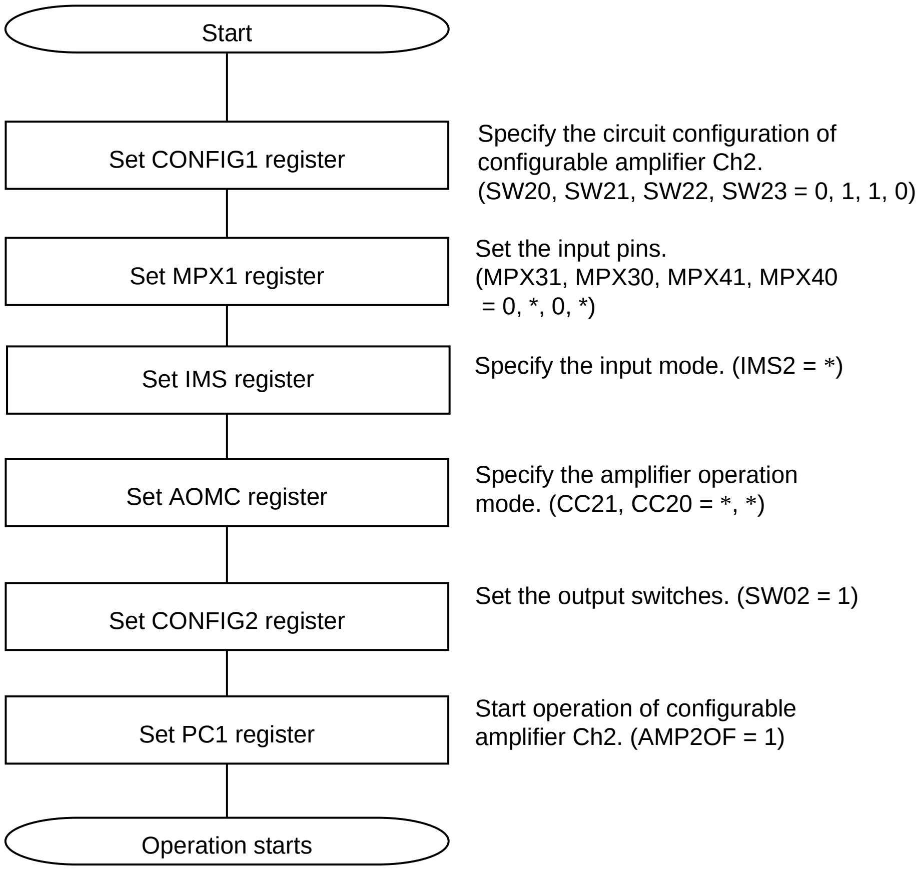


Remark *: don't care

Example of procedure for stopping configurable amplifier Ch1 (general-purpose operational amplifier)

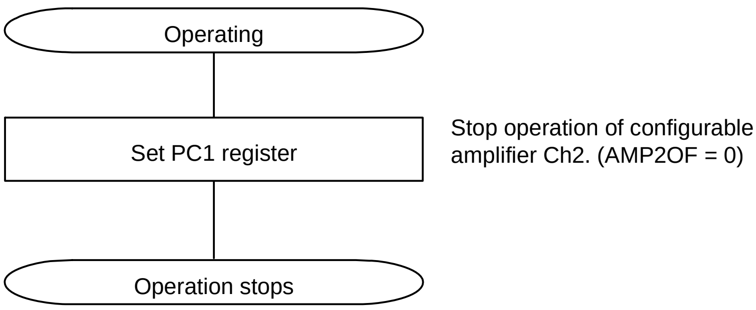


Example of procedure for starting configurable amplifier Ch2 (general-purpose operational amplifier)

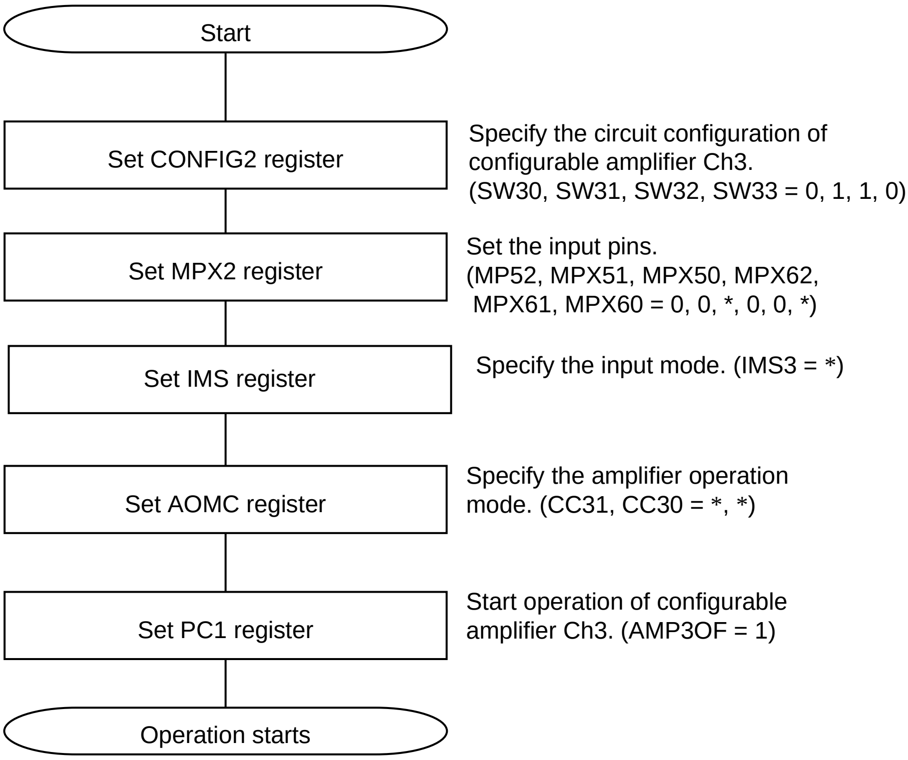


Remark *: don't care

Example of procedure for stopping configurable amplifier Ch2 (general-purpose operational amplifier)

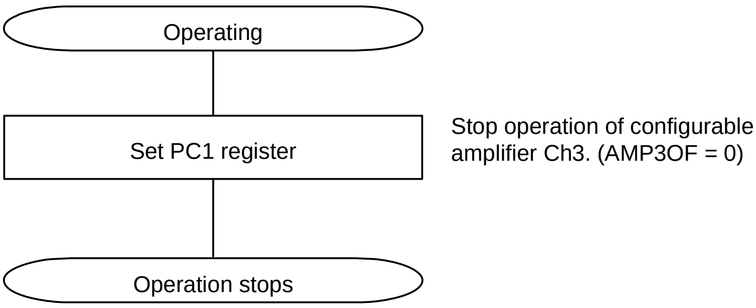


Example of procedure for starting configurable amplifier Ch3 (general-purpose operational amplifier)



Remark *: don't care

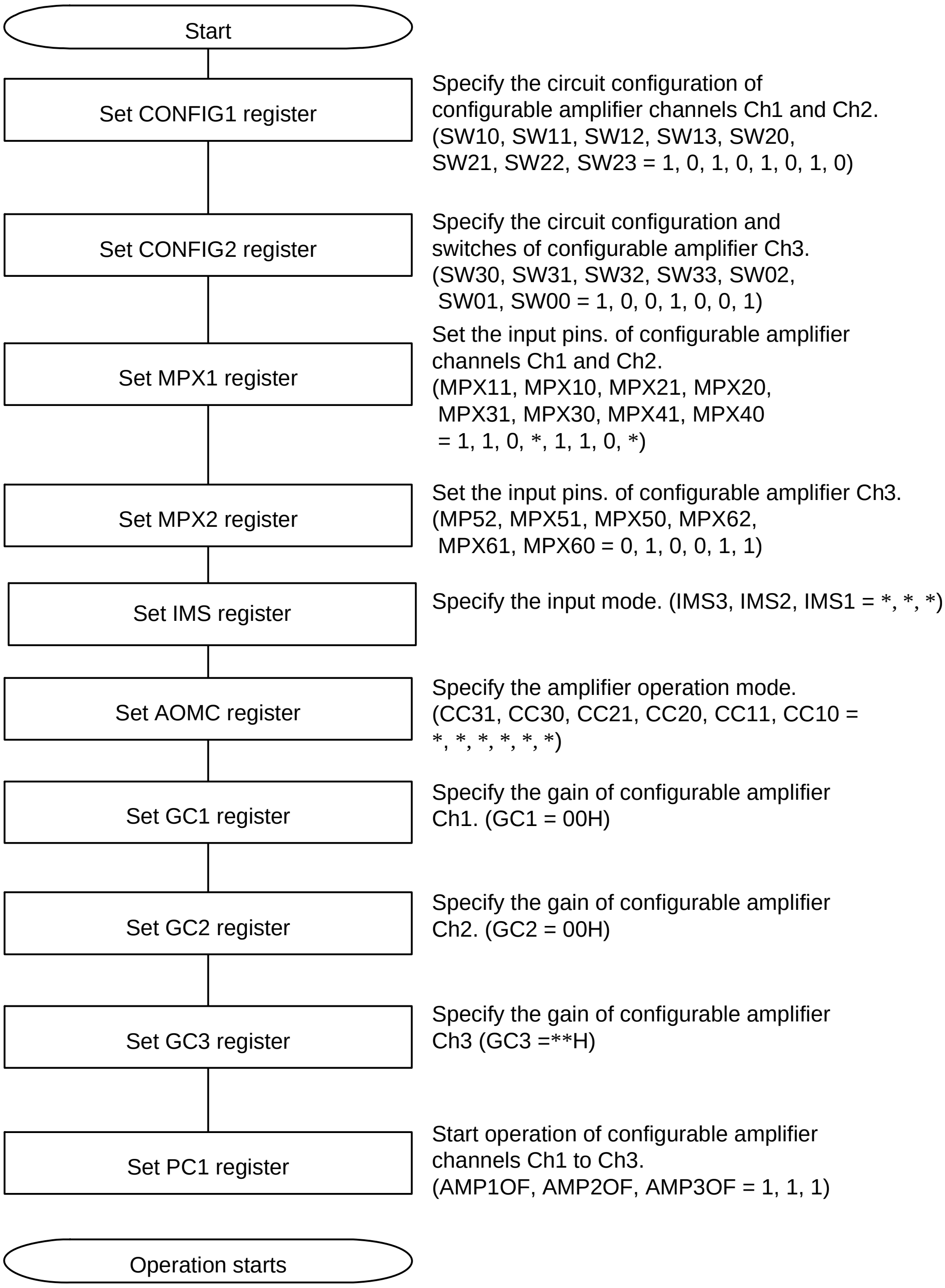
Example of procedure for stopping configurable amplifier Ch3 (general-purpose operational amplifier)



(6) Procedure when using the amplifiers as an instrumentation amplifier

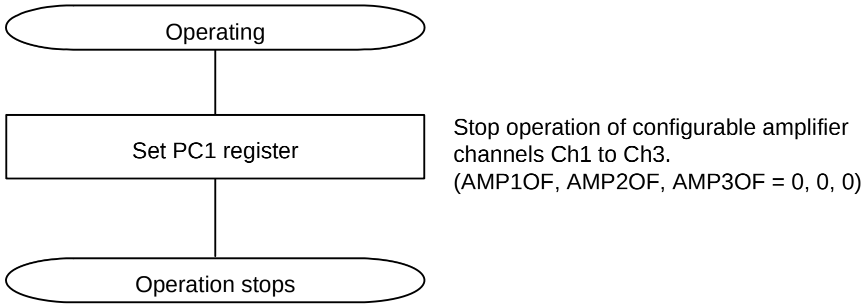
When using the configurable amplifiers together as an instrumentation amplifier, follow the procedures below to start and stop the amplifier.

Example of procedure for starting configurable amplifiers (instrumentation amplifier)



Remark *: don't care

Example of procedure for stopping configurable amplifiers (instrumentation amplifier)



3. General-Purpose Operational Amplifier

The RAA730300 has two on-chip general-purpose operational amplifier channels.

<R> 3.1 Overview of General-Purpose Operational Amplifier Features

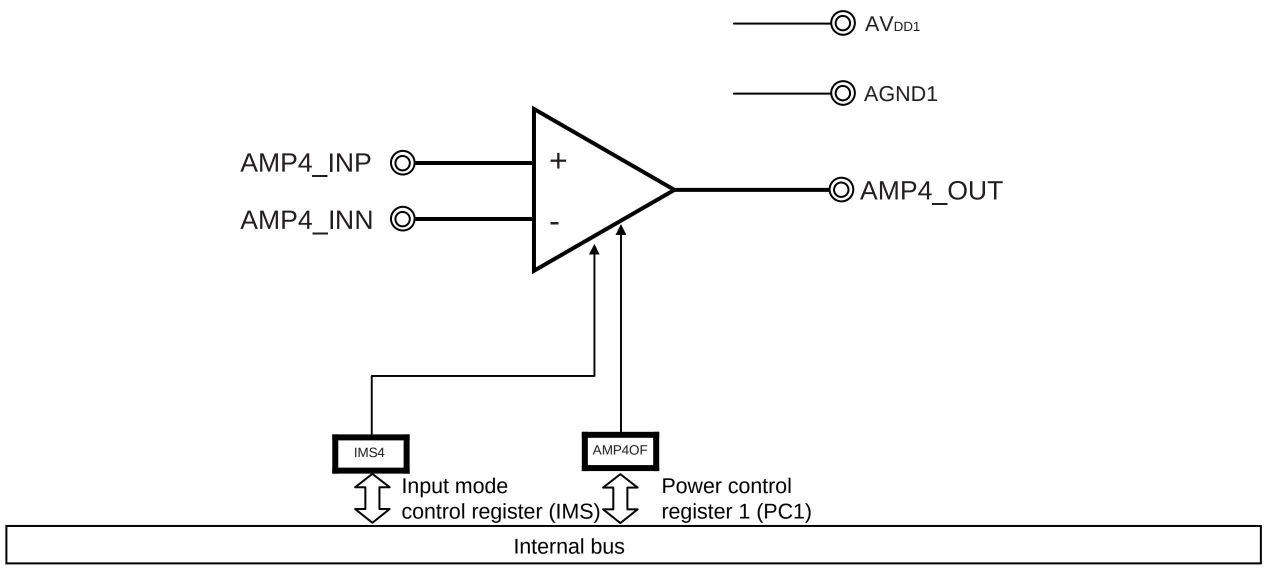
The general-purpose operational amplifiers have the following features:

- Includes an input mode switching function
- Includes a power-off function.

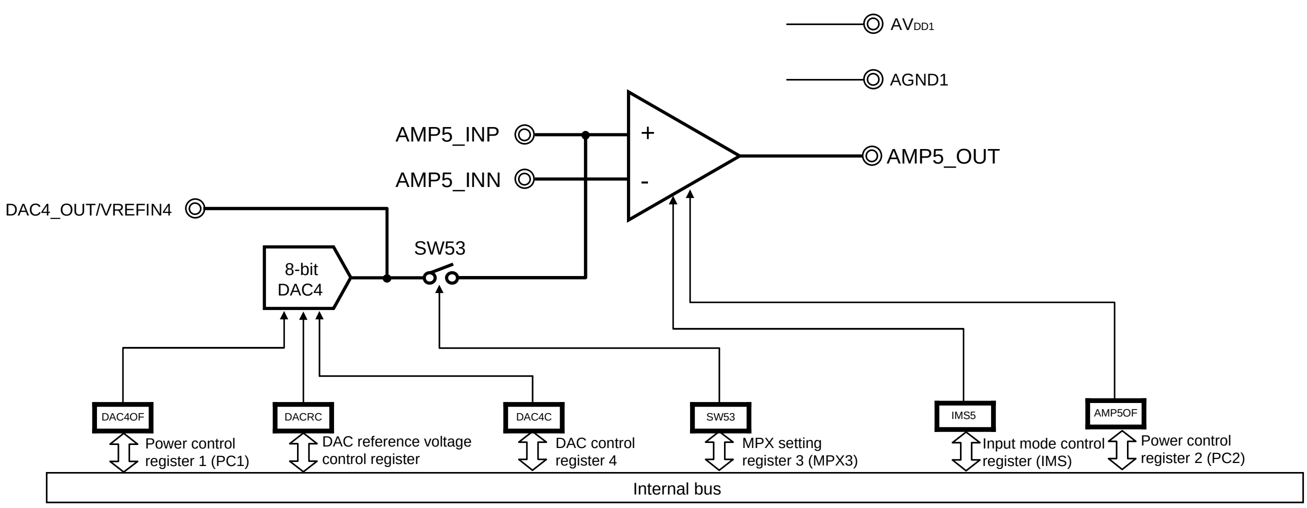
And also, the output signal from D/A converter Ch4 can be used as the reference voltage for a general-purpose operational amplifier Ch2. If D/A converter Ch4 is powered off, the external reference voltage is to be input to DAC4_OUT/VREFIN4 pin. For details about use of D/A converter, see **4. D/A Converter**.

3.2 Block Diagram

Figure 3-1. Block Diagram of General-Purpose Operational Amplifier Ch1



<R> **Figure 3-2. Block Diagram of General-Purpose Operational Amplifier Ch2**



<R> 3.3 Registers Controlling the General-Purpose Operational Amplifier

The general-purpose operational amplifier is controlled by the following 4 registers:

- Power control register 1 (PC1)
- Power control register 2 (PC2)
- MPX setting register 3 (MPX3)
- Input mode control register (IMS)

(1) Power control register 1 (PC1)

This register is used to enable or disable operation of the configurable amplifiers, general-purpose operational amplifiers, and D/A converters. Use this register to stop unused functions to reduce power consumption and noise.
When using a general-purpose operational amplifier Ch1, be sure to set the control bit that corresponds to the channel (bit 3) to 1.
Reset signal input clears this register to 00H.

Address: 11H After reset: 00H R/W

	7	6	5	4	3	2	1	0
PC1	DAC4OF	DAC3OF	DAC2OF	DAC1OF	AMP4OF	AMP3OF	AMP2OF	AMP1OF

AMP4OF	Operation of general-purpose operational amplifier Ch1
0	Stop operation of general-purpose operational amplifier Ch1.
1	Enable operation of general-purpose operational amplifier Ch1.

(2) Power control register 2 (PC2)

This register is used to enable or disable operation of the D/A converters, general-purpose operational amplifiers, the low-pass filter, high-pass filter, variable output voltage regulator, and temperature sensor.
Use this register to stop unused functions to reduce power consumption and noise.
When using general-purpose operational amplifier Ch2, be sure to set the control bit that corresponds to the channel (bit 4) to 1.
Reset signal input clears this register to 00H.

Address: 12H After reset: 00H R/W

	7	6	5	4	3	2	1	0
PC2	DAC7OF	DAC6OF	DAC5OF	AMP5OF	LPFOF	HPFOF	LDOOF	TEMPOF

AMP5OF	Operation of general-purpose operational amplifier Ch2
0	Stop operation of general-purpose operational amplifier Ch2.
1	Enable operation of general-purpose operational amplifier Ch2.

(3) MPX setting register 3 (MPX3)

This register is used to control MPX7, MPX8, MPX9, and MPX10.
This register is used to turn on or off the reference voltage input to general-purpose operational amplifier Ch2.
Reset signal input clears this register to 00H.

Address: 05H After reset: 00H R/W

	7	6	5	4	3	2	1	0
MPX3	0	0	SCF2	SCF1	SCF0	SW53	MPX71	MPX70

SW53	Control of SW53
0	Turn off SW53.
1	Turn on SW53.

Remark Bits 7 and 6 can be set to 1, but this has no effect on the function.

(4) Input mode control register (IMS)

This register is used to specify the input mode of the configurable amplifiers, general-purpose operational amplifiers, the low-pass filter, and high-pass filter.
When using one of general-purpose operational amplifier channels Ch1 and Ch2, be sure to set the control bit that corresponds to the channel (bits 4 and 3).

Address: 14H After reset: 00H R/W

	7	6	5	4	3	2	1	0
IMS	0	0	IMS6	IMS5	IMS4	IMS3	IMS2	IMS1

IMS5	Input mode of general-purpose operational amplifier Ch2
0	Rail-to-rail input mode
1	P-ch single-ended input mode

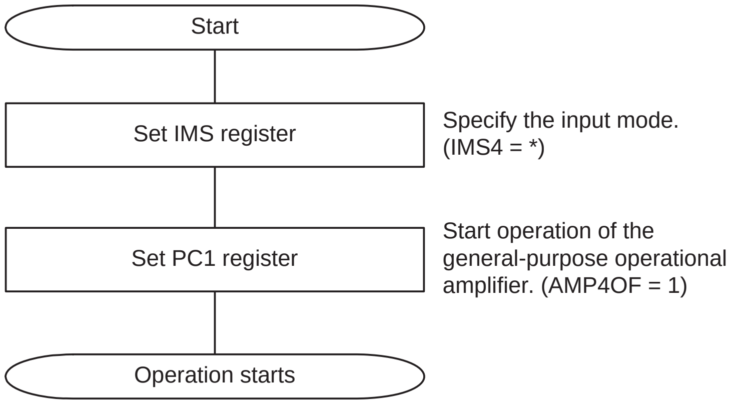
IMS4	Input mode of general-purpose operational amplifier Ch1
0	Rail-to-rail input mode
1	P-ch single-ended input mode

Remark Bits 7 and 6 can be set to 1, but this has no effect on the function.

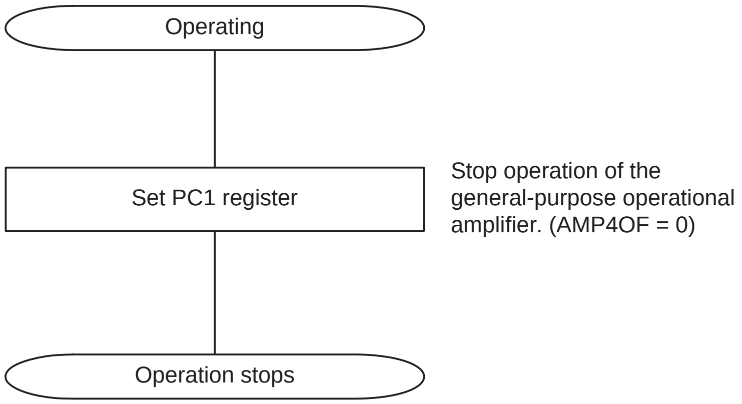
3.4 Procedure for Operating the General-Purpose Operational Amplifier

Follow the procedures below to start and stop the general-purpose operational amplifier.

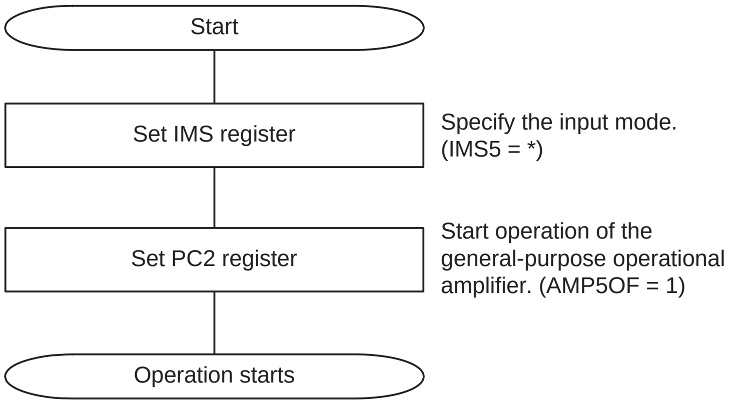
Example of procedure for starting the general-purpose operational amplifier Ch1



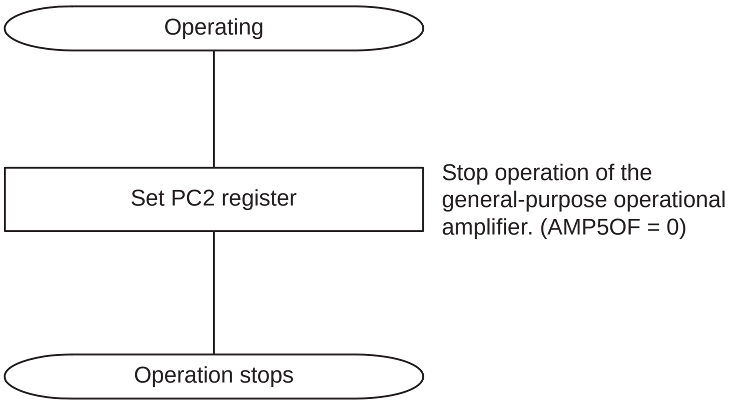
Example of procedure for stopping the general-purpose operational amplifier Ch1



Example of procedure for starting the general-purpose operational amplifier Ch2



Example of procedure for stopping the general-purpose operational amplifier Ch2



4. D/A Converters

The RAA730300 has seven on-chip D/A converter channels.

Channel	D/A Converter Output Pins
1 to 4	Provided
5 to 7	Not provided [Note]

Note Output pins are not provided although the channels are incorporated.

<R> 4.1 Overview of D/A Converter Features

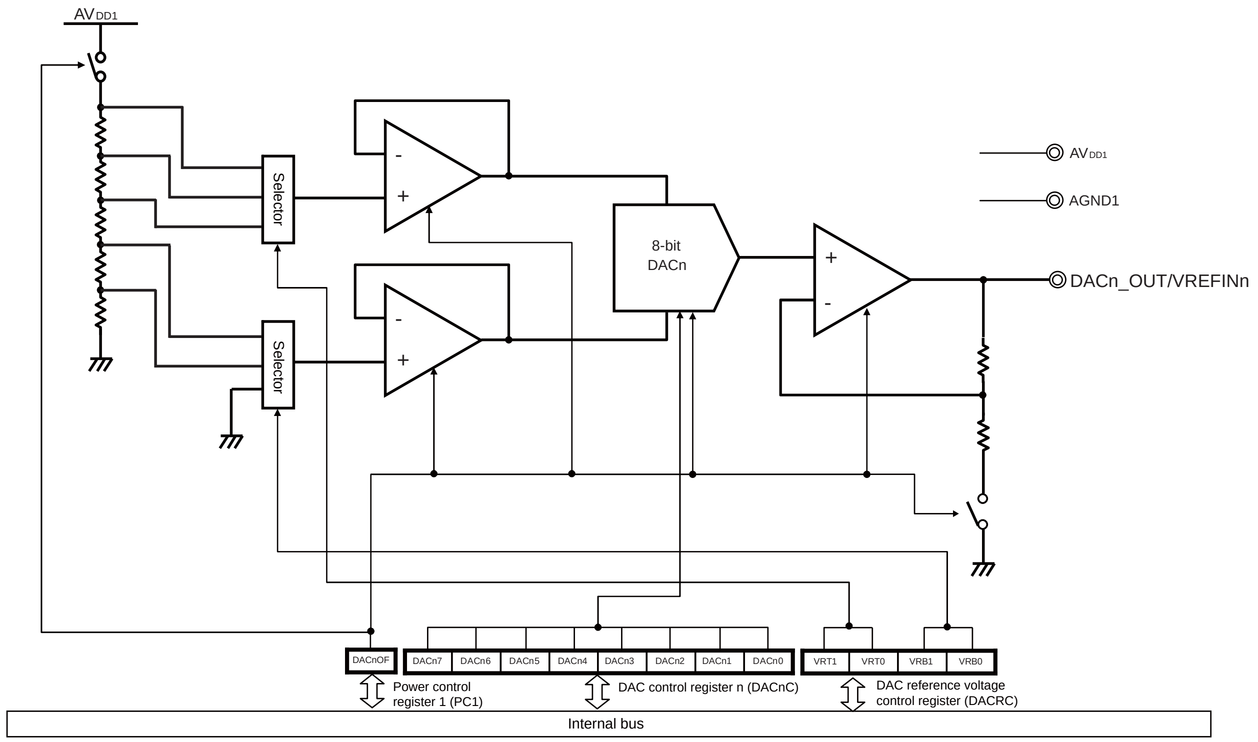
The D/A converters are 8-bit resolution converters that convert digital input signals into analog signals.
The D/A converters have the following features:

- 8-bit resolution (× 7 ch: Ch1 to Ch7)
- R-2R ladder method
- Analog output voltage: Output voltage can be calculated with the equation shown below.
  Output voltage = {(Reference voltage upper limit – Reference voltage lower limit) × m/256}
  + Reference voltage lower limit (m = 0 to 255: Value set to DACnC register)
- Controls the reference voltage for the configurable amplifier channels, general-purpose operational amplifier Ch2, low-pass filter, and high-pass filter
- Includes a power-off function.

Remark n = 1 to 7

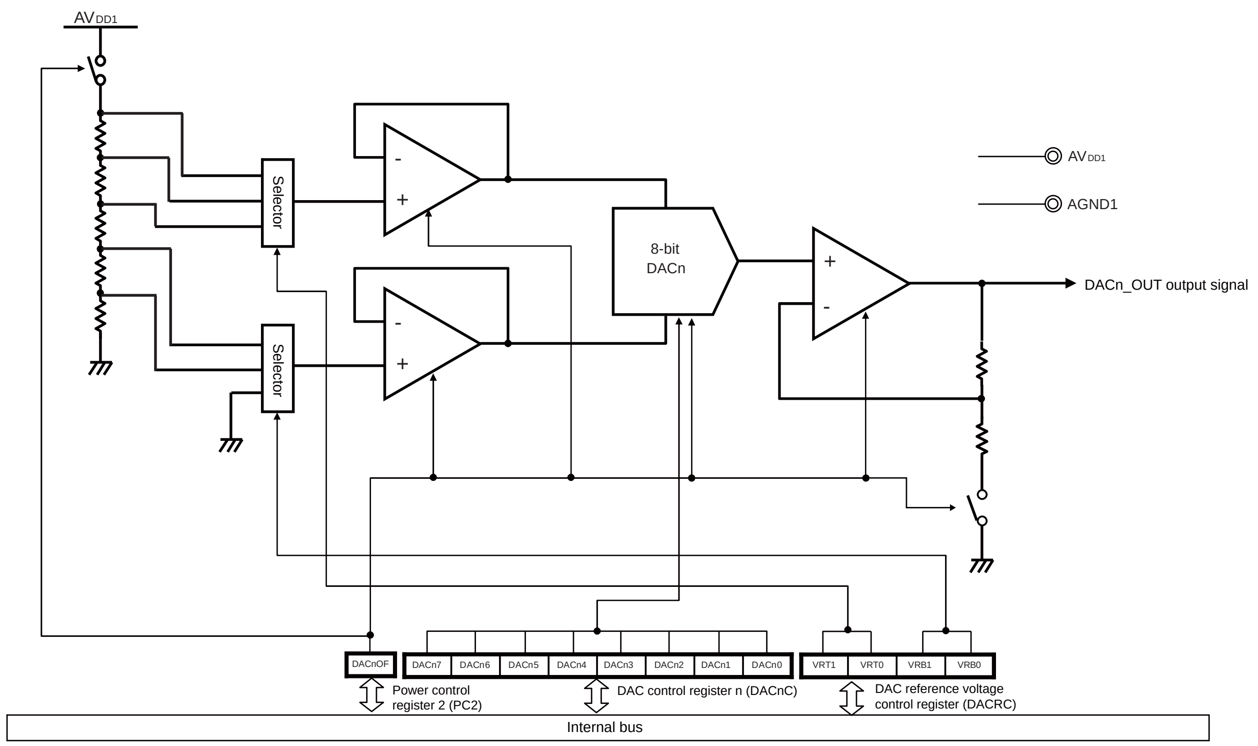
4.2 Block Diagram

Figure 4-1. Block Diagram of D/A Converter Channels Ch1 to Ch4



Remark n = 1 to 4

Figure 4-2. Block Diagram of D/A Converter Channels Ch5 to Ch7



Remark n = 5 to 7

4.3 Registers Controlling the D/A Converters

The D/A converters are controlled by the following 4 registers:

- DAC reference voltage control register (DACRC)
- DAC control registers 1, 2, 3, 4, 5, 6, 7 (DAC1C, DAC2C, DAC3C, DAC4C, DAC5C, DAC6C, DAC7C)
- Power control register 1 (PC1)
- Power control register 2 (PC2)

<R> **(1) DAC reference voltage control register (DACRC)**

This register is used to specify the upper (VRT) and lower (VRB) limits of the reference voltage for D/A converter channels Ch1 to Ch7.
When selecting the upper limit of the reference voltage, use bits 3 and 2.
When selecting the lower limit of the reference voltage, use bits 1 and 0.
Reset signal input clears this register to 00H.

Address: 0CH After reset: 00H R/W

	7	6	5	4	3	2	1	0
DACRC	0	0	0	0	VRT1	VRT0	VRB1	VRB0

VRT1	VRT0	Reference voltage upper limit (Typ.)
0	0	AV_{DD1}
0	1	$AV_{DD1} \times 4/5$
1	0	$AV_{DD1} \times 3/5$
1	1	AV_{DD1}

VRB1	VRB0	Reference voltage lower limit (Typ.)
0	0	AGND1
0	1	$AV_{DD1} \times 1/5$
1	0	$AV_{DD1} \times 2/5$
1	1	AGND1

Remark Bits 7 to 4 can be set to 1, but this has no effect on the function.

(2) DAC control registers 1, 2, 3, 4, 5, 6, 7 (DAC1C, DAC2C, DAC3C, DAC4C, DAC5C, DAC6C, DAC7C)

This register is used to specify the analog voltage output from each D/A converter.
The output signal from D/A converter can be used as the reference voltage for the configurable amplifier channels, general-purpose operational amplifier Ch2, low-pass filter, and high-pass filter.
Reset signal input sets this register to 80H.

Address: 0DH (n = 1), 0EH (n = 2), 0FH (n = 3), 10H (n = 4), 15H (n = 5), 16H (n = 6), 17H (n = 7)
After reset: 80H R/W

	7	6	5	4	3	2	1	0
DACnC	DACn7	DACn6	DACn5	DACn4	DACn3	DACn2	DACn1	DACn0

Remark1. n = 1 to 7
2. To calculate the output voltage, see **4. 1 Overview of D/A converter features**.

(3) Power control register 1 (PC1)

This register is used to enable or disable operation of the configurable amplifiers, the general-purpose operational amplifier, and the D/A converters.
Use this register to stop unused functions to reduce power consumption and noise.
When using one of D/A converter channels Ch1 to Ch4, be sure to set the control bit that corresponds to the channel (bits 7 to 4) to 1.
Reset signal input clears this register to 00H.

Address: 11H After reset: 00H R/W

	7	6	5	4	3	2	1	0
PC1	DAC4OF	DAC3OF	DAC2OF	DAC1OF	AMP4OF	AMP3OF	AMP2OF	AMP1OF

DAC4OF	Operation of D/A converter Ch4
0	Stop operation of D/A converter Ch4.
1	Enable operation of D/A converter Ch4.

DAC3OF	Operation of D/A converter Ch3
0	Stop operation of D/A converter Ch3.
1	Enable operation of D/A converter Ch3.

DAC2OF	Operation of D/A converter Ch2
0	Stop operation of D/A converter Ch2.
1	Enable operation of D/A converter Ch2.

DAC1OF	Operation of D/A converter Ch1
0	Stop operation of D/A converter Ch1.
1	Enable operation of D/A converter Ch1.

(4) Power control register 2 (PC2)

This register is used to enable or disable operation of the D/A converters, the general-purpose operational amplifier, low-pass filter, high-pass filter, variable output voltage regulator, and temperature sensor.
Use this register to stop unused functions to reduce power consumption and noise.
When using one of D/A converter channels Ch5 to Ch7, be sure to set the control bit that corresponds to the channel (bits 7 to 5) to 1.
Reset signal input clears this register to 00H.

Address: 12H After reset: 00H R/W

	7	6	5	4	3	2	1	0
PC2	DAC7OF	DAC6OF	DAC5OF	AMP5OF	LPFOF	HPFOF	LDOOF	TEMPOF

DAC7OF	Operation of D/A converter Ch7
0	Stop operation of D/A converter Ch7.
1	Enable operation of D/A converter Ch7.

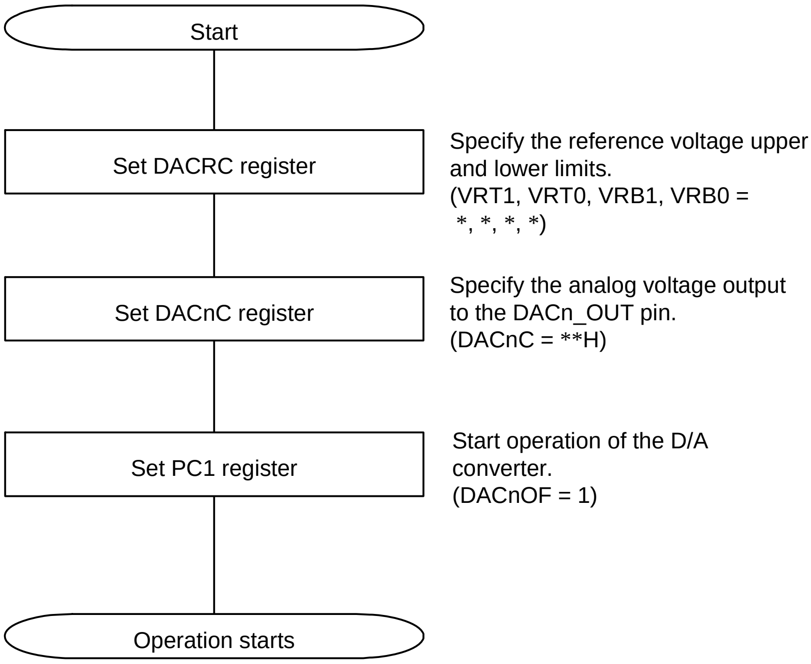
DAC6OF	Operation of D/A converter Ch6
0	Stop operation of D/A converter Ch6.
1	Enable operation of D/A converter Ch6.

DAC5OF	Operation of D/A converter Ch5
0	Stop operation of D/A converter Ch5.
1	Enable operation of D/A converter Ch5.

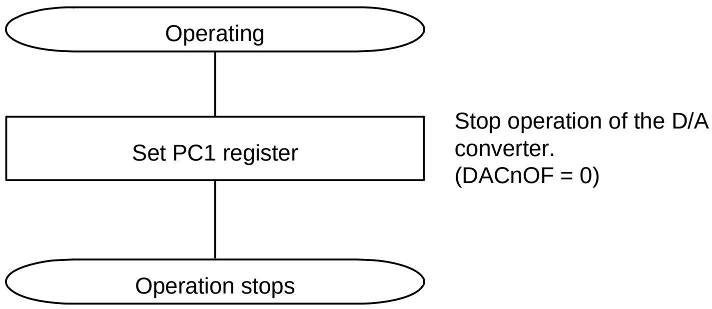
4.4 Procedure for Operating the D/A Converters

Follow the procedures below to start and stop the D/A converters.

Example of procedure for starting the D/A converters



Example of procedure for stopping the D/A converters



Remark *: don't care
n = 1 to 7

4.5 Notes on Using D/A Converters

Observe the following points when using the D/A converters:

(1) Only a very small current can flow from the DACn_OUT pin because the output impedance of the D/A converters is high. If the load input impedance is low, insert a follower amplifier between the load and the DACn_OUT pin. Also, make sure that the wiring between the pin and the follower amplifier or load is as short as possible (because of the high output impedance). If it is not possible to keep the wiring short, take measures such as surrounding the pin with a ground pattern.

(2) If inputting an external reference power supply to the VREFINn pin, be sure to set the DACnOF bit to 0.

Remark n = 1 to 4

5. Low-Pass Filter

The RAA730300 has one on-chip switched-capacitor low-pass filter channel.

<R> 5.1 Overview of Low-Pass Filter Features

The low-pass filter has the following features:

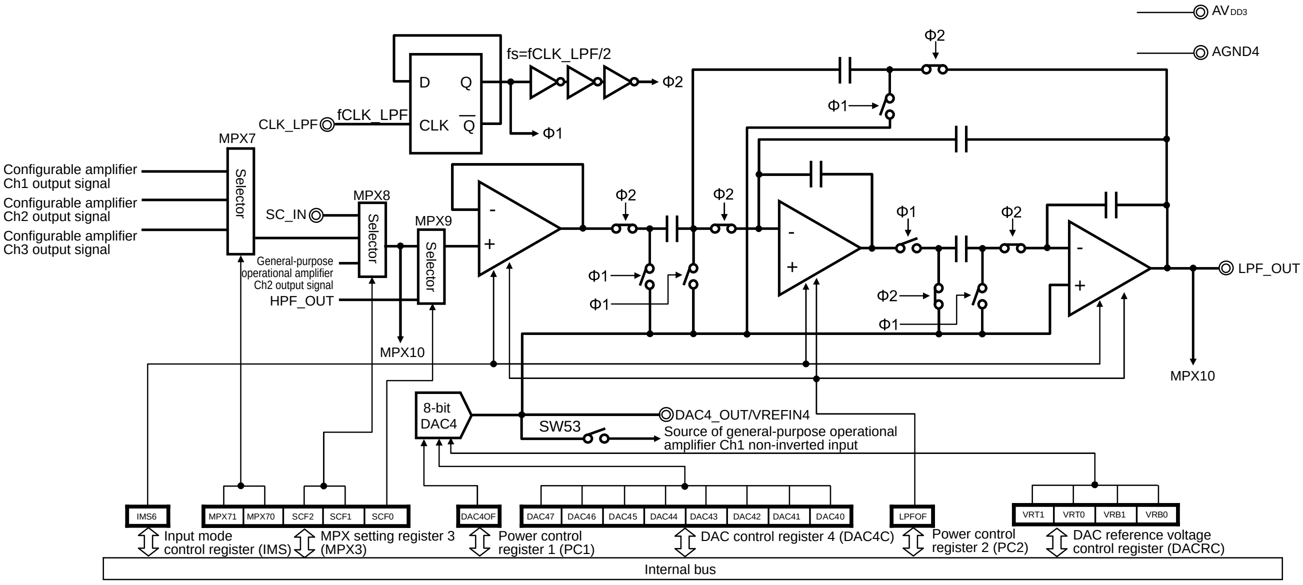
- Butterworth characteristics (Q value = 0.702)
- Cutoff frequency (fc) range: 9 Hz to 900 Hz
- External input clock frequency (f_{CLK_LPF}) range: 2 × fc/0.0087 = 2 kHz to 200 kHz
- Includes a power-off function.

And also, the output signal from D/A converter Ch4 can be used as the reference voltage for low-pass filter. If D/A converter Ch4 is powered off, the external reference voltage is to be input to DAC4_OUT/VREFIN4 pin. For details about use of D/A converter, see **4. D/A Converter**.

Remarks 1. The internal control clock (fs) of the low-pass filter has a duty of 50%, so the external input clock is divided by two at the internal D flip-flop before being used for the low-pass filter. If the internal control clock frequency (fs) is 100 kHz, therefore, input a 200 kHz clock signal to the CLK_LPF pin.

2. The phase of the signal input to the low-pass filter inverts after passing through the low-pass filter.

5.2 Block Diagram



5.3 Registers Controlling the Low-Pass Filter

The low-pass filter is controlled by the following 3 registers:

- MPX setting register 3 (MPX3)
- Power control register 2 (PC2)
- Input mode control register (IMS)

(1) MPX setting register 3 (MPX3)

This register is used to control MPX7, MPX8, MPX9, and MPX10.
When selecting the signal to be input to the filter circuits, use bits 5 and 4.
When switching the order in which signals are processed by the low-pass and high-pass filters, use bit 3.
When switching the output signal from MPX7, use bits 1 and 0.
Reset signal input clears this register to 00H.

Address: 05H After reset: 00H R/W

	7	6	5	4	3	2	1	0
MPX3	0	0	SCF2	SCF1	SCF0	SW53	MPX71	MPX70

SCF2	SCF1	Source of input to filter circuits
0	0	SC_IN pin
0	1	MPX7 output signal
1	0	General-purpose operational amplifier Ch2 output signal
1	1	Setting prohibited

SCF0	Specification of the order of filter signal processing
0	The MPX9 output signal passes the low-pass filter and then is input to the high-pass filter.
1	The MPX9 output signal passes the high-pass filter and then is input to the low-pass filter.

MPX71	MPX70	Specification of MPX7 output signal
0	0	Open pin
0	1	Configurable amplifier Ch1 output signal
1	0	Configurable amplifier Ch2 output signal
1	1	Configurable amplifier Ch3 output signal

Remark Bits 7 and 6 can be set to 1, but this has no effect on the function.

(2) Power control register 2 (PC2)

This register is used to enable or disable operation of the D/A converters, general-purpose operational amplifiers, the low-pass filter, high-pass filter, variable output voltage regulator, and temperature sensor.
Use this register to stop unused functions to reduce power consumption and noise.
When using the low-pass filter, be sure to set bit 3 to 1.
Reset signal input clears this register to 00H.

Address: 12H After reset: 00H R/W

	7	6	5	4	3	2	1	0
PC2	DAC7OF	DAC6OF	DAC5OF	AMP5OF	LPFOF	HPFOF	LDOOF	TEMPOF

LPFOF	Operation of low-pass filter
0	Stop operation of the low-pass filter.
1	Enable operation of the low-pass filter.

(3) Input mode control register (IMS)

This register is used to specify the input mode of the configurable amplifiers, general-purpose operational amplifiers, the low-pass filter, and high-pass filter.
When using the low-pass filter or the high-pass filter, be sure to set the control bit that corresponds to the channel (bit 5).
Reset signal input clears this register to 00H.

Address: 14H After reset: 00H R/W

	7	6	5	4	3	2	1	0
IMS	0	0	IMS6	IMS5	IMS4	IMS3	IMS2	IMS1

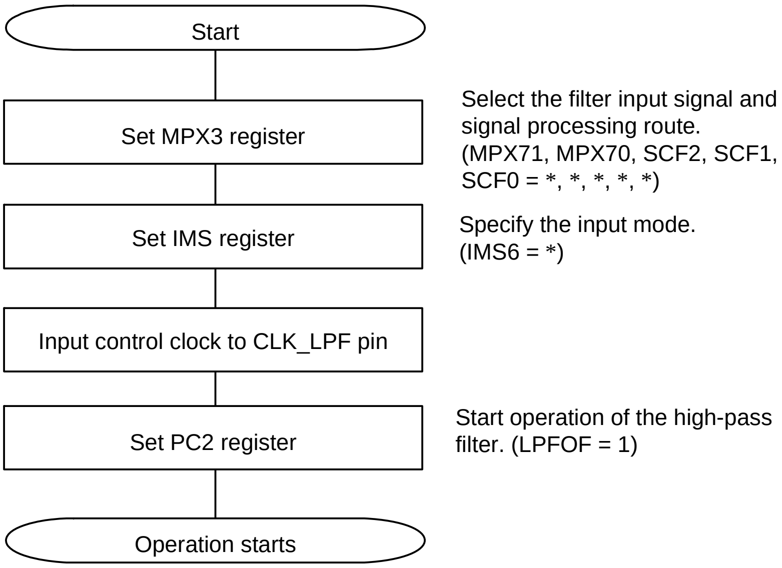
IMS6	Input mode of low-pass filter and high-pass filter
0	Rail-to-rail input mode
1	P-ch single-ended input mode

Remark Bits 7 and 6 can be set to 1, but this has no effect on the function.

5.4 Procedure for Operating the Low-Pass Filter

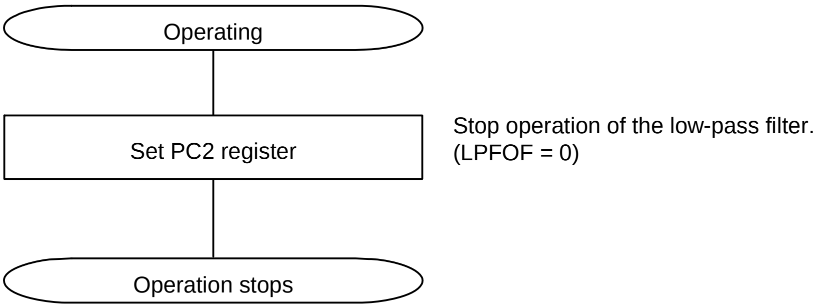
Follow the procedures below to start and stop the low-pass filter.

Example of procedure for starting the low-pass filter



Remark *: don't care

Example of procedure for stopping the low-pass filter



6. High-Pass Filter

The RAA730300 has one on-chip switched-capacitor high-pass filter channel.

<R> 6.1 Overview of High-Pass Filter Features

The high-pass filter has the following features:

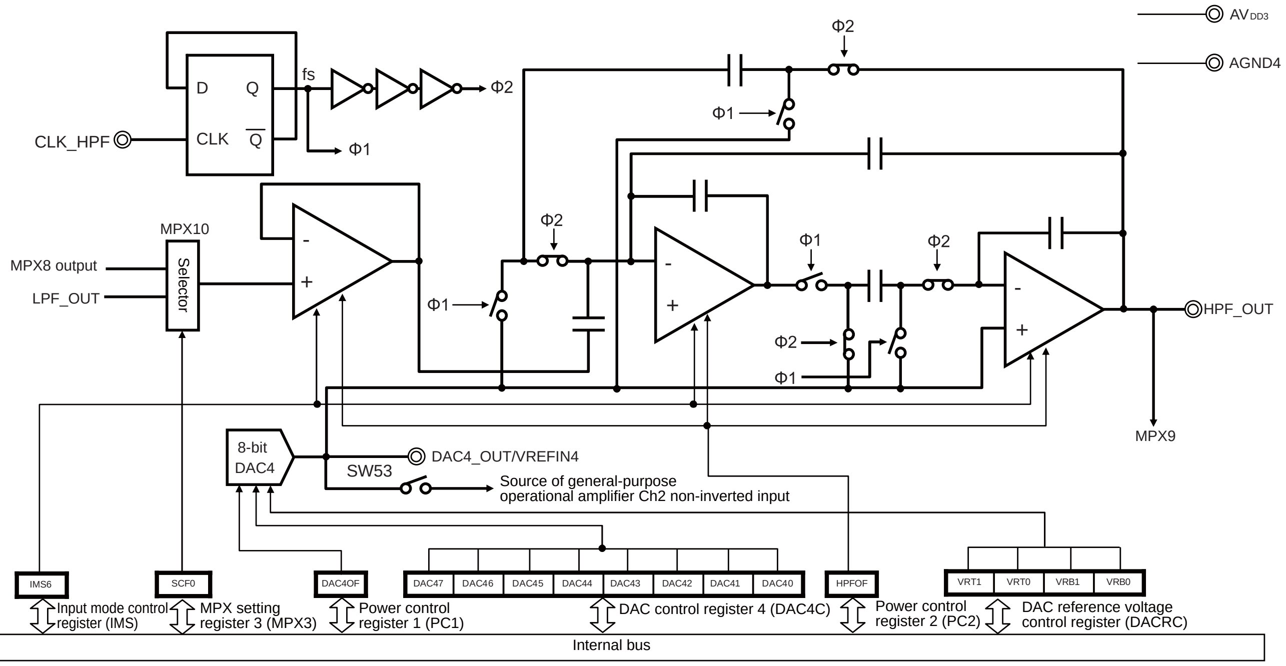
- Butterworth characteristics (Q value = 0.702)
- Cutoff frequency (fc) range: 8 Hz to 800 Hz
- External input clock frequency (f_{CLK_HPF}) range: $2 \times f_C / 0.0074$ = 2 kHz to 200 kHz
- Includes a power-off function.

And also, the output signal from D/A converter Ch4 can be used as the reference voltage for high-pass filter. If D/A converter Ch4 is powered off, the external reference voltage is to be input to DAC4_OUT/VREFIN4 pin. For details about use of D/A converter, see **4. D/A Converter**.

Remarks1. The internal control clock (fs) of the high-pass filter has a duty of 50%, so the external input clock is divided by two at the internal D flip-flop before being used for the low-pass filter. If the internal control clock frequency (fs) is 100 kHz, therefore, input a 200 kHz clock signal to the CLK_HPF pin.

2. The phase of the signal input to the high-pass filter inverts after passing through the low-pass filter.

6.2 Block Diagram



6.3 Registers Controlling the High-Pass Filter

The high-pass filter is controlled by the following 3 registers:

- MPX setting register 3 (MPX3)
- Power control register 2 (PC2)
- Input mode control register (IMS)

<R> **(1) MPX setting register 3 (MPX3)**

This register is used to control MPX7, MPX8, MPX9, and MPX10.
When selecting the signal to be input to the filter circuits, use bits 5 and 4.
When switching the order in which signals are processed by the low-pass and high-pass filters, use bit 3.
When switching the output signal from MPX7, use bits 1 and 0.
Reset signal input clears this register to 00H.

Address: 05H After reset: 00H R/W

	7	6	5	4	3	2	1	0
MPX3	0	0	SCF2	SCF1	SCF0	SW53	MPX71	MPX70

SCF2	SCF1	Source of input to filter circuits
0	0	SC_IN pin
0	1	MPX7 output signal
1	0	General-purpose operational amplifier Ch2 output signal
1	1	Setting prohibited

SCF0	Specification of the order of filter signal processing
0	The MPX9 output signal passes the low-pass filter and then is input to the high-pass filter.
1	The MPX9 output signal passes the high-pass filter and then is input to the low-pass filter.

MPX71	MPX70	Specification of MPX7 output signal
0	0	Open pin
0	1	Configurable amplifier Ch1 output signal
1	0	Configurable amplifier Ch2 output signal
1	1	Configurable amplifier Ch3 output signal

Remark Bits 7 and 6 can be set to 1, but this has no effect on the function.

(2) Power control register 2 (PC2)

This register is used to enable or disable operation of the D/A converters, general-purpose operational amplifiers, the low-pass filter, high-pass filter, variable output voltage regulator, and temperature sensor.
Use this register to stop unused functions to reduce power consumption and noise.
When using the high-pass filter, be sure to set bit 2 to 1.
Reset signal input clears this register to 00H.

Address: 12H After reset: 00H R/W

	7	6	5	4	3	2	1	0
PC2	DAC7OF	DAC6OF	DAC5OF	AMP5OF	LPFOF	HPFOF	LDOOF	TEMPOF

HPFOF	Operation of high-pass filter
0	Stop operation of the high-pass filter.
1	Enable operation of the high-pass filter.

(3) Input mode control register (IMS)

This register is used to specify the input mode of the configurable amplifiers, general-purpose operational amplifiers, the low-pass filter, and high-pass filter.
When using the low-pass filter or the high-pass filter, be sure to set the control bit that corresponds to the channel (bit 5).
Reset signal input clears this register to 00H.

Address: 14H After reset: 00H R/W

	7	6	5	4	3	2	1	0
IMS	0	0	IMS6	IMS5	IMS4	IMS3	IMS2	IMS1

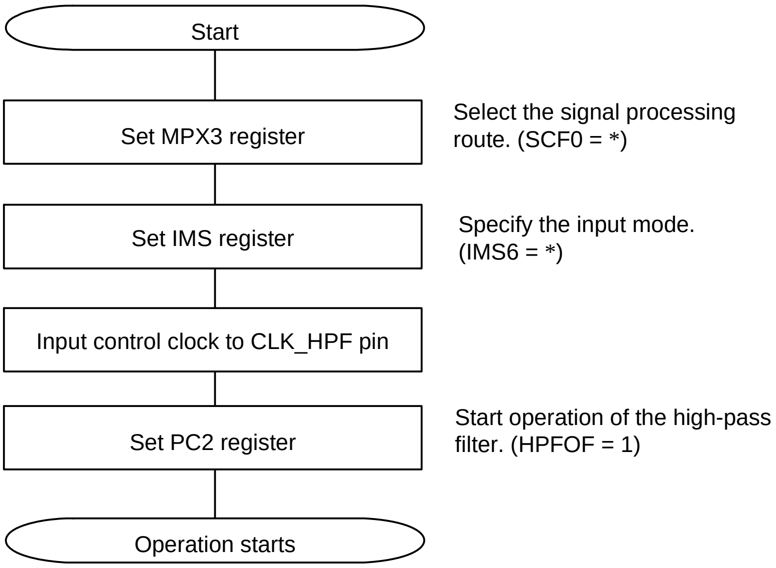
IMS6	Input mode of low-pass filter and high-pass filter
0	Rail-to-rail input mode
1	P-ch single-ended input mode

Remark Bits 7 and 6 can be set to 1, but this has no effect on the function.

6.4 Procedure for Operating the High-Pass Filter

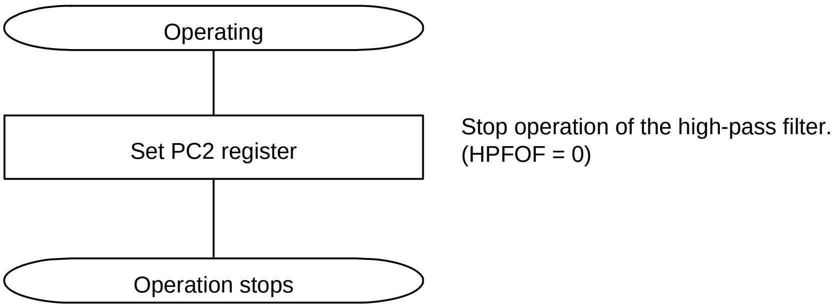
Follow the procedures below to start and stop the high-pass filter.

Example of procedure for starting the high-pass filter



Remark *: don't care

Example of procedure for stopping the high-pass filter



7. Temperature Sensor

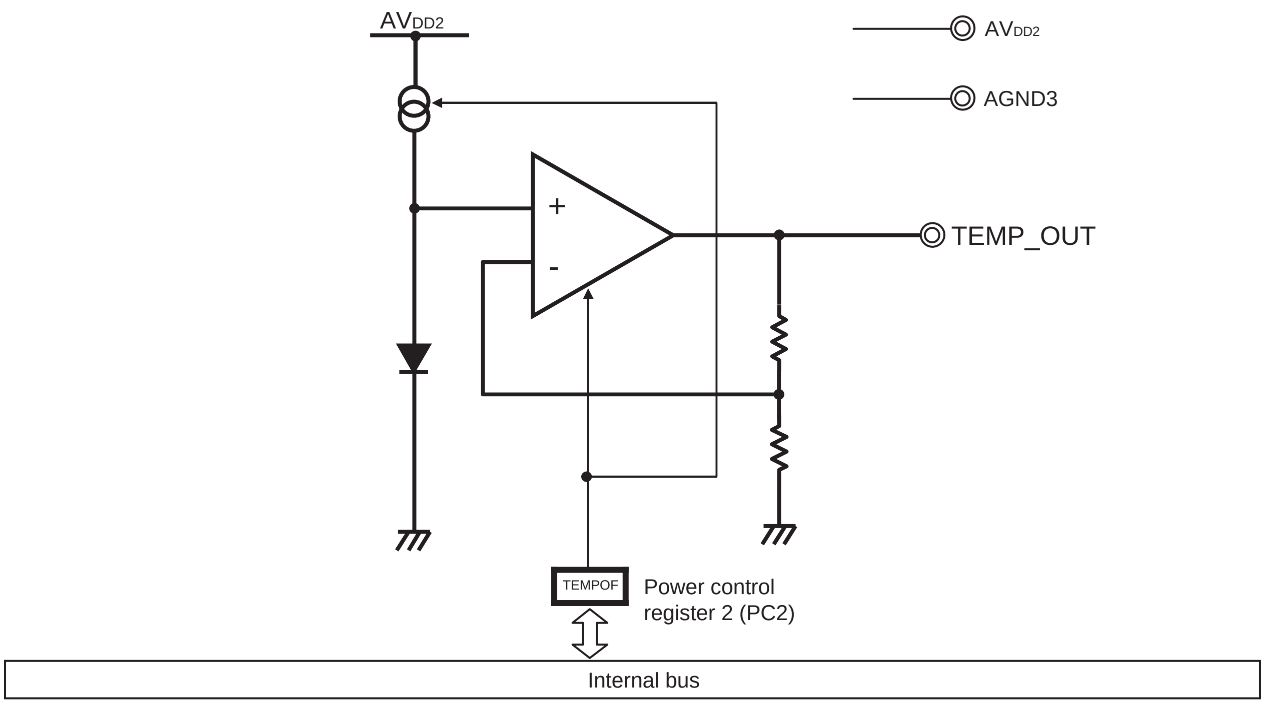
The RAA730300 has one on-chip temperature sensor channel.

7.1 Overview of Temperature Sensor Features

The temperature sensor has the following features:

- Output voltage temperature coefficient: −4 mV/°C (Typ.)
- Includes a power-off function.

7.2 Block Diagram



7.3 Registers Controlling the Temperature Sensor

The temperature sensor is controlled by power control register 2 (PC2).

(1) Power control register 2 (PC2)

This register is used to enable or disable operation of the D/A converters, general-purpose operational amplifiers, the low-pass filter, high-pass filter, variable output voltage regulator, and temperature sensor.
Use this register to stop unused functions to reduce power consumption and noise.
When selecting the signal to be input to the temperature sensor, be sure to set bit 0 to 1.
Reset signal input clears this register to 00H.

Address: 12H After reset: 00H R/W

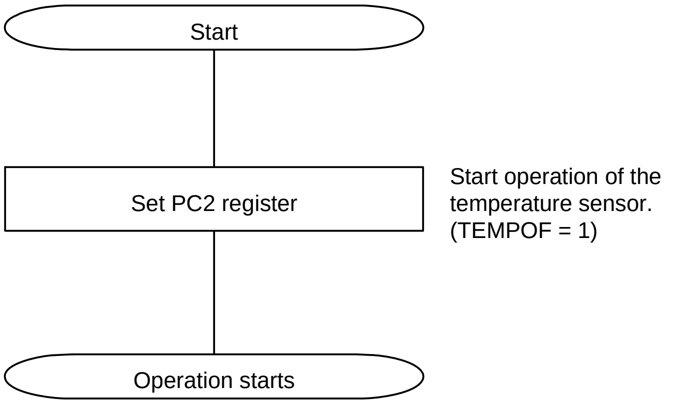
	7	6	5	4	3	2	1	0
PC2	DAC7OF	DAC6OF	DAC5OF	AMP5OF	LPFOF	HPFOF	LDOOF	TEMPOF

TEMPOF	Operation of temperature sensor
0	Stop operation of the temperature sensor.
1	Enable operation of the temperature sensor.

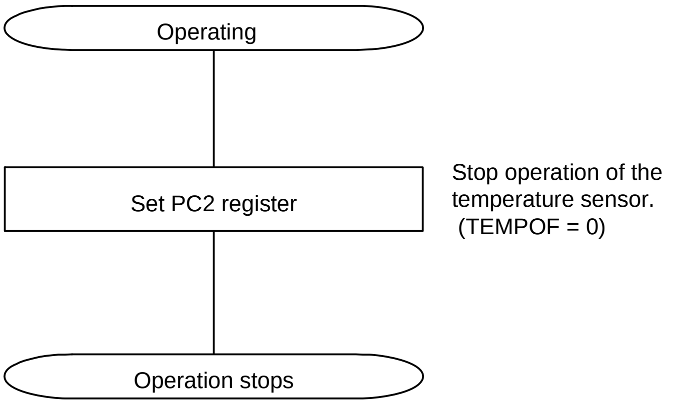
7.4 Procedure for Operating the Temperature Sensor

Follow the procedures below to start and stop the temperature sensor.

Example of procedure for starting the temperature sensor



Example of procedure for stopping the temperature sensor



8. Variable Output Voltage Regulator

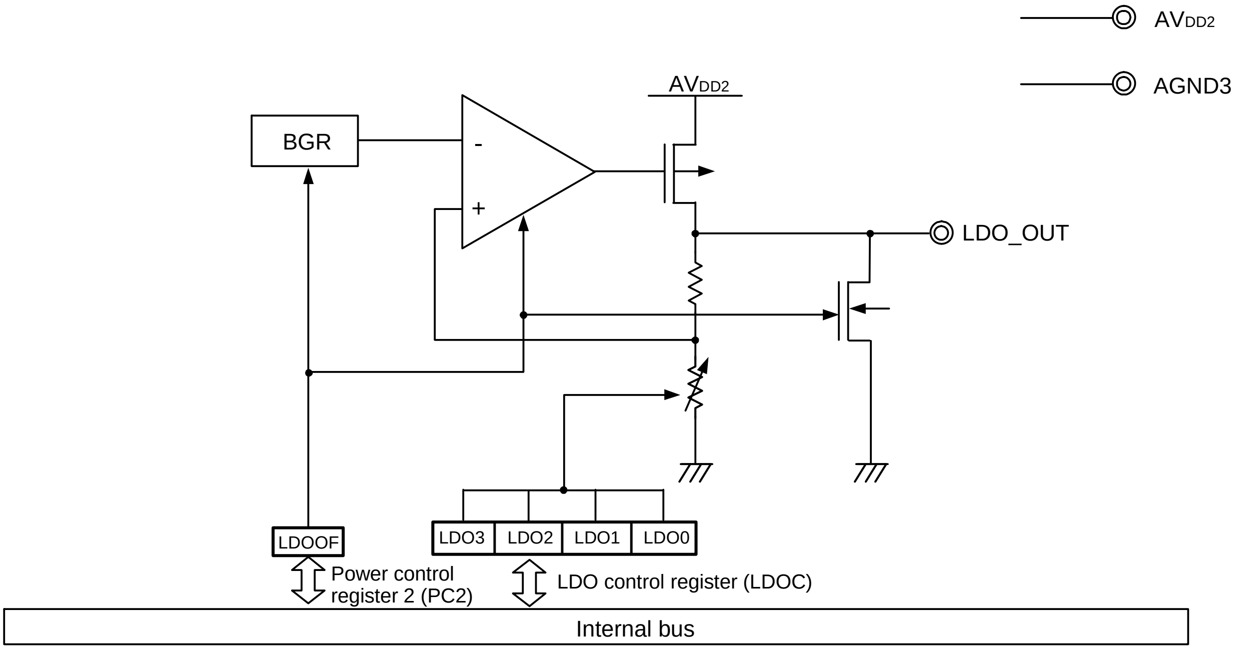
The RAA730300 has one on-chip variable output voltage regulator channel. This is a series regulator that generates a voltage of 1.8 V (default) from a supplied voltage of 3 V.

8.1 Overview of Variable Output Voltage Regulator Features

The variable output voltage regulator has the following features:

- Output voltage range: 1.8 to 3.1 V (Typ.)
- Output current: 15 mA (Max.)
- Includes a power-off function.

8.2 Block Diagram



8.3 Registers Controlling the Variable Output Voltage Regulator

The variable output voltage regulator is controlled by the following 2 registers:

- LDO control register (LDOC)
- Power control register 2 (PC2)

(1) LDO control register (LDOC)

This register is used to specify the output voltage of the variable output voltage regulator.
Reset signal input clears this register to 00H.

Address: 0BH After reset: 00H R/W

	7	6	5	4	3	2	1	0
LDOC	0	0	0	0	LDO3	LDO2	LDO1	LDO0

LDO3	LDO2	LDO1	LDO0	Output Voltage of Variable Output Voltage Regulator (Typ.)[Note]
0	0	0	0	1.8 V
0	0	0	1	1.9 V
0	0	1	0	2.0 V
0	0	1	1	2.1 V
0	1	0	0	2.2 V
0	1	0	1	2.3 V
0	1	1	0	2.4 V
0	1	1	1	2.5 V
1	0	0	0	2.6 V
1	0	0	1	2.7 V
1	0	1	0	2.8 V
1	0	1	1	2.9 V
1	1	0	0	3.0 V
1	1	0	1	3.1 V
Other than above				Setting prohibited

Note Output voltage is determined in consideration of dropout voltage.

Remark Bits 7 to 4 can be set to 1, but this has no effect on the function.

(2) Power control register 2 (PC2)

This register is used to enable or disable operation of the D/A converters, general-purpose operational amplifiers, the low-pass filter, high-pass filter, variable output voltage regulator, and temperature sensor.
Use this register to stop unused functions to reduce power consumption and noise.
When using the variable output voltage regulator, be sure to set bit 1 to 1.
Reset signal input clears this register to 00H.

Address: 12H After reset: 00H R/W

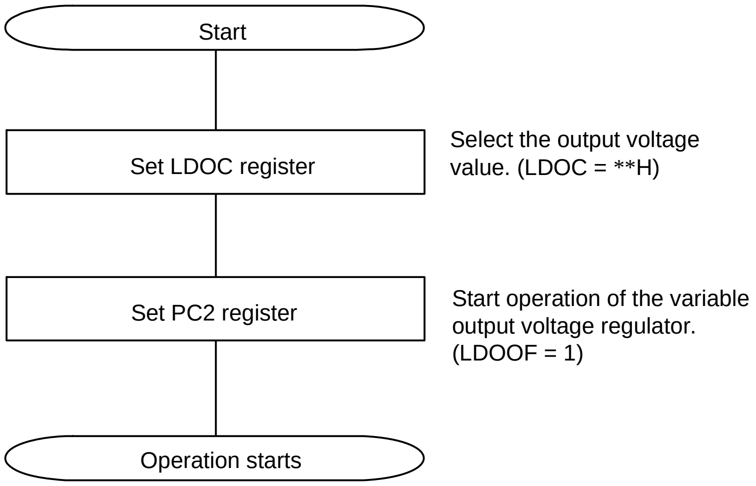
	7	6	5	4	3	2	1	0
PC2	DAC7OF	DAC6OF	DAC5OF	AMP5OF	LPFOF	HPFOF	LDOOF	TEMPOF

LDOOF	Operation of variable output voltage regulator
0	Stop operation of the variable output voltage regulator.
1	Enable operation of the variable output voltage regulator.

8.4 Procedure for Operating the Variable Output Voltage Regulator

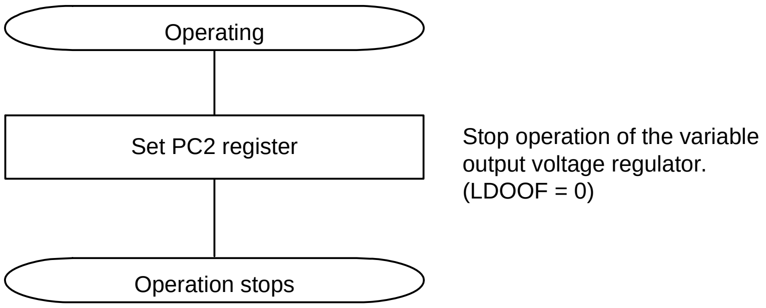
Follow the procedures below to start and stop the variable output voltage regulator.

Example of procedure for starting the variable output voltage regulator



Remark *: don't care

Example of procedure for stopping the variable output voltage regulator



9. SPI

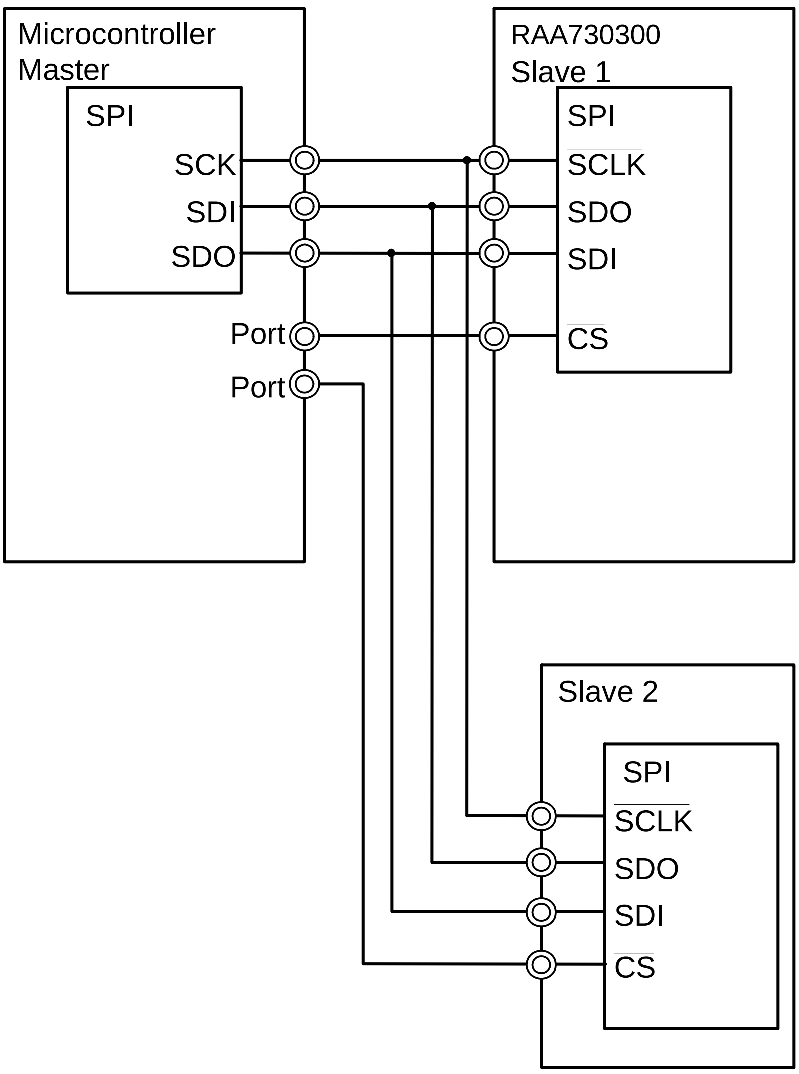
9.1 Overview of SPI Features

The SPI is used to allow control from external devices by using clocked communication via four lines: a serial clock line ($\overline{\text{SCLK}}$), two serial data lines (SDI and SDO), and a chip select input line ($\overline{\text{CS}}$).

Data transmission/reception:

- 16-bit data unit
- MSB first

Figure 9-1. SPI Configuration Example



<R> **Caution After turning on DV_{DD}, be sure to generate external reset by inputting a reset signal to $\overline{\text{RESET}}$ pin before starting SPI communication. For details, see 10 Reset.**

9.2 SPI Communication

The SPI transmits and receives data in 16-bit units. Data can be transmitted and received when $\overline{\text{CS}}$ is low. Data is transmitted one bit at a time in synchronization with the falling edge of the serial clock, and is received one bit at a time in synchronization with the rising edge of the serial clock. When the R/W bit is 1, data is written to the SPI control register in accordance with the address/data setting after the 16th rising edge of $\overline{\text{SCLK}}$ has been detected following the fall of $\overline{\text{CS}}$. The operation specified by the data is then executed. When the R/W bit is 0, the data is output from the register in accordance with the address/data setting in synchronization with the 9th and later falling edges of $\overline{\text{SCLK}}$ following the fall of $\overline{\text{CS}}$.

Figure 9-2. SPI Communication Timing

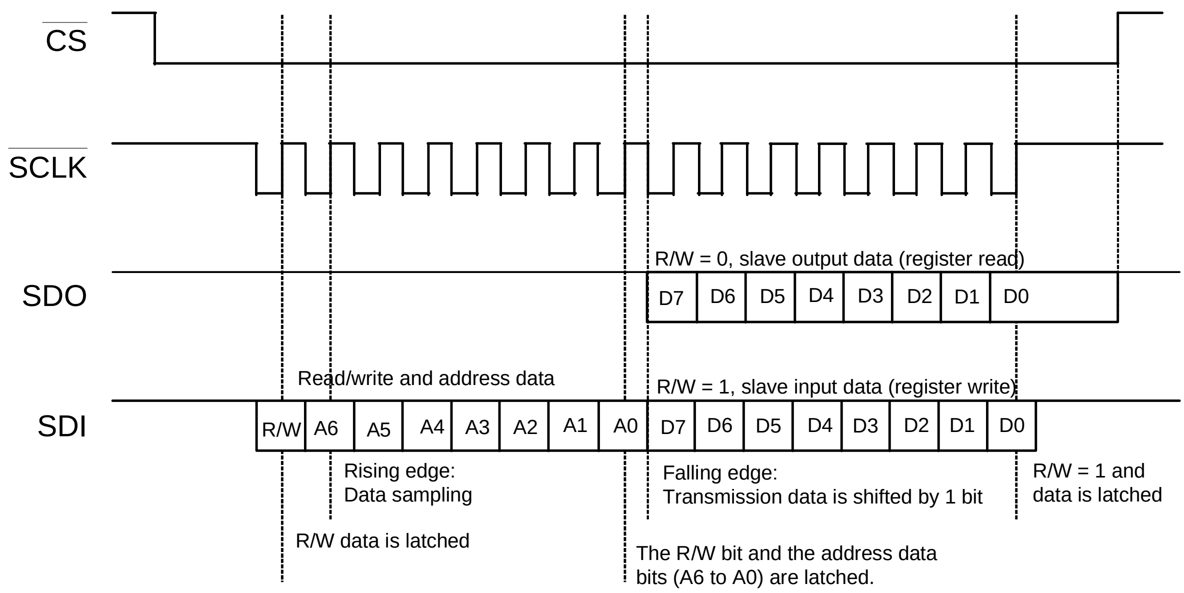


Table 9-1. SPI Control Registers

Address	SPI Control Register	R/W	After Reset
00H	Configuration register 1 (CONFIG1)	R/W	88H
01H	Configuration register 2 (CONFIG2)	R/W	80H
03H	MPX setting register 1 (MPX1)	R/W	00H
04H	MPX setting register 2 (MPX2)	R/W	00H
05H	MPX setting register 3 (MPX3)	R/W	00H
06H	Gain control register 1 (GC1)	R/W	00H
07H	Gain control register 2 (GC2)	R/W	00H
08H	Gain control register 3 (GC3)	R/W	00H
09H	AMP operation mode control register (AOMC)	R/W	00H
0BH	LDO control register (LDOC)	R/W	00H
0CH	DAC reference voltage control register (DACRC)	R/W	00H
0DH	DAC control register 1 (DAC1C)	R/W	80H
0EH	DAC control register 2 (DAC2C)	R/W	80H
0FH	DAC control register 3 (DAC3C)	R/W	80H
10H	DAC control register 4 (DAC4C)	R/W	80H
11H	Power control register 1 (PC1)	R/W	00H
12H	Power control register 2 (PC2)	R/W	00H
13H	Reset control register (RC)	R/W	00H[Note]
14H	Input mode control register (IMS)	R/W	00H
15H	DAC control register 5 (DAC5C)	R/W	80H
16H	DAC control register 6 (DAC6C)	R/W	80H
17H	DAC control register 7 (DAC7C)	R/W	80H

Note The reset control register (RC) is not initialized to 00H by generating internal reset of the reset control register (RC). For details, see **10. Reset**.

<R> 10. Reset

10.1 Overview of Reset Feature

The RAA730300 has an on-chip reset function. The SPI control registers are initialized by reset. A reset can be generated in the following two ways:

- External reset by inputting an external reset signal to the $\overline{\text{RESET}}$ pin
- Internal reset by writing 1 to the RESET bit of the reset control register (RC)

The functions of the external reset and the internal reset are described below.

- After turning on DV_{DD}, be sure to generate external reset by inputting a reset signal to $\overline{\text{RESET}}$ pin before starting SPI communication.
- During reset, each function is shifted to the status shown in Table 10-1. The status of each SPI control register after reset has been acknowledged is shown in Table 10-2. After reset, the status of each pin is shown in Table 10-3.
- External reset is generated when a low-level signal is input to the $\overline{\text{RESET}}$ pin. On the other hand, internal reset is generated when 1 is written to the RESET bit of the reset control register (RC).
- External reset is subsequently cancelled by inputting a high-level signal to $\overline{\text{RESET}}$ pin after a low-level signal is input to this pin. On the other hand, internal reset is subsequently cancelled by writing 0 to the RESET bit of the reset control register (RC) after 1 is written to the same bit of this register.

Caution When generating an external reset, input a low-level signal to the $\overline{\text{RESET}}$ pin for at least 10 μs.

Table 10-1. Statuses During Reset

Function Block	External Reset from $\overline{\text{RESET}}$ Pin	Internal Reset by Reset Control Register (RC)
Configurable amplifier	Operation stops.	
General-purpose operational amplifier	Operation stops.	
D/A converter	Operation stops.	
Low-pass filter	Operation stops.	
High-pass filter	Operation stops.	
Temperature sensor	Operation stops.	
Variable output voltage regulator	Operation stops.	
SPI	Operation stops.	Operation is enabled.

Table 10-2. Statuses of SPI Control Registers After a Reset Is Acknowledged

Address	SPI Control Register	Status After a Reset Is Acknowledged	
		External Reset	Internal Reset
00H	Configuration register 1 (CONFIG1)	88H	88H
01H	Configuration register 2 (CONFIG2)	80H	80H
03H	MPX setting register 1 (MPX1)	00H	00H
04H	MPX setting register 2 (MPX2)	00H	00H
05H	MPX setting register 3 (MPX3)	00H	00H
06H	Gain control register 1 (GC1)	00H	00H
07H	Gain control register 2 (GC2)	00H	00H
08H	Gain control register 3 (GC3)	00H	00H
09H	AMP operation mode control register (AOMC)	00H	00H
0BH	LDO control register (LDOC)	00H	00H
0CH	DAC reference voltage control register (DACRC)	00H	00H
0DH	DAC control register 1 (DAC1C)	80H	80H
0EH	DAC control register 2 (DAC2C)	80H	80H
0FH	DAC control register 3 (DAC3C)	80H	80H
10H	DAC control register 4 (DAC4C)	80H	80H
11H	Power control register 1 (PC1)	00H	00H
12H	Power control register 2 (PC2)	00H	00H
13H	Reset control register (RC)	00H	01H[Note]
14H	Input mode control register (IMS)	00H	00H
15H	DAC control register 5 (DAC5C)	80H	80H
16H	DAC control register 6 (DAC6C)	80H	80H
17H	DAC control register 7 (DAC7C)	80H	80H

Note The reset control register (RC) is not initialized by generating internal reset of the reset control register (RC), but it can be done to 00H by generating external reset from $\overline{\text{RESET}}$ pin or by writing 0 to the RESET bit of the reset control register (RC).

Table 10-3. Pin Statuses After a Reset

Pin Name	External Reset from $\overline{\text{RESET}}$ Pin	Internal Reset by Reset Control Register (RC)
SC_IN	Hi-Z	Hi-Z
AMP5_OUT	Hi-Z	Hi-Z
AMP5_INN	Hi-Z	Hi-Z
AMP5_INP	Hi-Z	Hi-Z
MPXIN61	Hi-Z	Hi-Z
MPXIN51	Hi-Z	Hi-Z
MPXIN60	Hi-Z	Hi-Z
MPXIN50	Hi-Z	Hi-Z
AMP3_OUT	Hi-Z	Hi-Z
DAC3_OUT/VREFIN3	Hi-Z	Hi-Z
AMP2_OUT	Hi-Z	Hi-Z
AMP1_OUT	Hi-Z	Hi-Z
DAC2_OUT/VREFIN2	Hi-Z	Hi-Z
DAC1_OUT/VREFIN1	Hi-Z	Hi-Z
MPXIN41	Hi-Z	Hi-Z
MPXIN31	Hi-Z	Hi-Z
MPXIN40	Hi-Z	Hi-Z
MPXIN30	Hi-Z	Hi-Z
MPXIN21	Hi-Z	Hi-Z
MPXIN11	Hi-Z	Hi-Z
MPXIN20	Hi-Z	Hi-Z
MPXIN10	Hi-Z	Hi-Z
LDO_OUT	Pull-down	Pull-down
AMP4_OUT	Hi-Z	Hi-Z
AMP4_INN	Hi-Z	Hi-Z
AMP4_INP	Hi-Z	Hi-Z
TEMP_OUT	Pull down	Pull down
$\overline{\text{SCLK}}$	Pull-up input	Hi-Z
SDO	Pull-up	Hi-Z
SDI	Pull-up input	Hi-Z
$\overline{\text{CS}}$	Pull-up input	Hi-Z
DAC4_OUT/VREFIN4	Hi-Z	Hi-Z
HPF_OUT	Hi-Z	Hi-Z
CLK_HPF	Pull-down input	Pull-down input
CLK_LPF	Pull-down input	Pull-down input
LPF_OUT	Hi-Z	Hi-Z

10.2 Registers Controlling the Reset Feature

(1) Reset control register (RC)

This register is used to control the reset feature.

An internal reset can be generated by writing 1 to the RESET bit. The reset control register (RC) is initialized to 00H by generating external reset from $\overline{\text{RESET}}$ pin or by writing 0 to the RESET bit of the reset control register (RC).

Address: 13H After reset: 00H[Note] R/W

	7	6	5	4	3	2	1	0
RC	0	0	0	0	0	0	0	RESET

RESET	Reset request by internal reset signal
0	Do not make a reset request by using the internal reset signal, or cancel the reset.
1	Make a reset request by using the internal reset signal, or the reset signal is currently being input.

Note The reset control register (RC) is not initialized by generating internal reset of the reset control register (RC), but it can be done to 00H by generating external reset from $\overline{\text{RESET}}$ pin or by writing 0 to the RESET bit of the reset control register (RC).

Caution When the RESET bit is 1, writing to any register other than the reset control register (RC) is ignored. Initializing the reset control register (RC) to 00H by external reset, or writing 0 to the RESET bit enable writing to all the registers.

Remark Bits 7 to 1 are fixed at 0 of read only.

11. Electrical Specifications

11.1 Absolute Maximum Ratings

(T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	AV_{DD}	AV_{DD1}, AV_{DD2}, AV_{DD3}	–0.3 to +4.0	V
	DV_{DD}	DV_{DD}	–0.3 to +4.0	V
	AGND	AGND1, AGND2, AGND3, AGND4	–0.3 to +0.3	V
	DGND	DGND	–0.3 to +0.3	V
Input voltage	V_{I1}	MPXIN10, MPXIN11, MPXIN20, MPXIN21, MPXIN30, MPXIN31, MPXIN40, MPXIN41, MPXIN50, MPXIN51, MPXIN60, MPXIN61, SC_IN, VREFIN1, VREFIN2, VREFIN3, VREFIN4, AMP4_INN, AMP4_INP, AMP5_INN, AMP5_INP, CLK_LPF, CLK_HPF, $\overline{RESET}$	–0.3 to AV_{DD} + 0.3[Note]	V
	V_{I2}	$\overline{SCLK}$, SDI, $\overline{CS}$	–0.3 to DV_{DD} + 0.3[Note]	V
Output voltage	V_{O1}	LDO_OUT, BGR_OUT, AMP1_OUT, AMP2_OUT, AMP3_OUT, AMP4_OUT, AMP5_OUT, LPF_OUT, HPF_OUT, DAC1_OUT, DAC2_OUT, DAC3_OUT, DAC4_OUT, TEMP_OUT, LDO_OUT	–0.3 to AV_{DD} + 0.3[Note]	V
	V_{O2}	SDO	–0.3 to DV_{DD} + 0.3[Note]	V
Output current	I_{O1}	AMP1_OUT, AMP2_OUT, AMP3_OUT, AMP4_OUT, AMP5_OUT, LPF_OUT, HPF_OUT, DAC1_OUT, DAC2_OUT, DAC3_OUT, DAC4_OUT, TEMP_OUT	1	mA
	I_{O2}	SDO	±4	mA
	I_{LDOOUT}	LDO_OUT	15	mA
Operating ambient temperature	T_A		–40 to +105	°C
<R> Storage temperature	T_{stg}		–40 to +125	°C

Note Must be 4.0 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

<R> 11.2 Operating Condition

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Power supply voltage Range	V_{DDOP}	AV_{DD1}, AV_{DD2}, AV_{DD3}, DV_{DD}	2.2	–	3.6	V
Operating temperature Range	T_{OP}		–40	–	+105	°C

11.3 Supply Current Characteristics

(–40°C ≤ T_A ≤ 105°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 3.0 V)

Parameter	Symbol	Conditions		Ratings			Unit
				MIN	TYP	MAX	
Supply current	Istby11Note	PC1 = 00H, PC2 = 00H	TA = 25°C	–	0.11	0.35	µA
			TA = 85°C	–	0.75	5	µA
			TA = 105°C	–	1.80	10	µA
	Im111Note	PC1 = 47H, PC2 = 03H (configurable amplifier channels Ch1 to Ch3, D/A converter Ch3 (instrumentation amplifier), variable output voltage regulator, and temperature sensor are operating), CCn1, CCn0 = 0, 0		–	1.25	1.90	mA
	Im112Note	PC1 = 7FH, PC2 = 13H (configurable amplifier channels Ch1 to Ch3, general-purpose operational amplifier channels Ch1 to Ch2, D/A converter channels Ch5 to Ch7, variable output voltage regulator, and temperature sensor are operating), CCn1, CCn0 = 0, 0		–	2.10	3.15	mA
	Im113Note	PC1 = FFH, PC2 = 1FH (configurable amplifier channels Ch1 to Ch3, general-purpose operational amplifier channels Ch1 to Ch2, D/A converter channels Ch4 to Ch7, low-pass filter, high-pass filter, variable output voltage regulator, and temperature sensor are operating), CCn1, CCn0 = 0, 0		–	3.70	5.60	mA
	Im114Note	PC1 = FFH, PC2 = FFH (configurable amplifier channels Ch1 to Ch3, general-purpose operational amplifier channels Ch1 to Ch2, D/A converter channels Ch1 to Ch7, low-pass filter, high-pass filter, variable output voltage regulator, and temperature sensor are operating), CCn1, CCn0 = 0, 0		–	4.15	6.25	mA
	Im121Note	PC1 = 47H, PC2 = 03H (configurable amplifier channels Ch1 to Ch3, D/A converter Ch3 (instrumentation amplifier), variable output voltage regulator, and temperature sensor are operating), CCn1, CCn0 = 1, 1		–	0.60	0.90	mA
	Im122Note	PC1 = 7FH, PC2 = 13H (configurable amplifier channels Ch1 to Ch3, general-purpose operational amplifier channels Ch1 to Ch2, D/A converter channels Ch5 to Ch7, variable output voltage regulator, and temperature sensor are operating), CCn1, CCn0 = 1, 1		–	1.45	2.20	mA
	Im123Note	PC1 = FFH, PC2 = 1FH (configurable amplifier channels Ch1 to Ch3, general-purpose operational amplifier channels Ch1 to Ch2, D/A converter channels Ch4 to Ch7, low-pass filter, high-pass filter, variable output voltage regulator, and temperature sensor are operating), CCn1, CCn0 = 1, 1		–	3.10	4.65	mA
	Im124Note	PC1 = FFH, PC2 = FFH (configurable amplifier channels Ch1 to Ch3, general-purpose operational amplifier channels Ch1 to Ch2, D/A converter channels Ch1 to Ch7, low-pass filter, high-pass filter, variable output voltage regulator, and temperature sensor are operating), CCn1, CCn0 = 1, 1		–	3.50	5.25	mA

Note Total current flowing to internal power supply pins AV_{DD1}, AV_{DD2}, AV_{DD3}, and DV_{DD}. Current flowing through the pull-up resistor is not included. The input leakage current flowing when the level of the input pin is fixed to AV_{DD1}, AV_{DD2}, AV_{DD3} or DV_{DD}, or AGND1, AGND2, AGND3, AGND4, or DGND is included. See the table below to check the definition of those symbols of the current flowing.

Remark n = 1 to 3

Parameter	Symbol	Analog function with power on															
		Configurable amplifier			General-purpose operational amplifier		D/A converter							Low-pass filter	High-pass filter	Temperature sensor	Variable output voltage regulator
		Ch1	Ch2	Ch3	Ch1	Ch2	Ch1	Ch2	Ch3	Ch4	Ch5	Ch6	Ch7				
Supply current	Im111[Note1]	ON	ON	ON	–	–	–	–	ON	–	–	–	–	–	–	ON	ON
	Im112[Note1]	ON	ON	ON	ON	ON	–	–	–	–	ON	ON	ON	–	–	ON	ON
	Im113[Note1]	ON	ON	ON	ON	ON	–	–	–	ON	ON	ON	ON	ON	ON	ON	ON
	Im114[Note1]	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
	Im121[Note2]	ON	ON	ON	–	–	–	–	ON	–	–	–	–	–	–	ON	ON
	Im122[Note2]	ON	ON	ON	ON	ON	–	–	–	–	ON	ON	ON	–	–	ON	ON
	Im123[Note2]	ON	ON	ON	ON	ON	–	–	–	ON	ON	ON	ON	ON	ON	ON	ON
	Im124[Note2]	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON

Note1. CCn1, CCn0 = 0, 0

2. CCn1, CCn0 = 1, 1

11.4 Electrical Specifications of Each Block

(1) Configurable amplifier block characteristics

($-40°C \leq T_A \leq 105°C$, $AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD}$ = 3.0 V, VREFIN1 = VREFIN2 = VREFIN3 = 1.5 V, AMP1OF = AMP2OF = AMP3OF = 1, DAC1OF = DAC2OF = DAC3OF = 0, non-inverting amplifier)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption Note	Icc00	CCn1, CCn0 = 0, 0	–	330	500	µA
	Icc01	CCn1, CCn0 = 0, 1	–	250	380	µA
	Icc10	CCn1, CCn0 = 1, 0	–	170	260	µA
	Icc11	CCn1, CCn0 = 1, 1	–	90	150	µA
Input voltage 1	VINL1	IMSn = 0	AGND1 – 0.05	–	–	V
	VINH1	IMSn = 0	–	–	AV_{DD1} + 0.1	V
Input voltage 2	VINL2	IMSn = 1	AGND1 – 0.05	–	–	V
	VINH2	IMSn = 1	–	–	AV_{DD1} – 1.4	V
Output voltage	VOUTL	IOL = –200 µA	–	–	AGND1 + 0.1	V
	VOUTH	IOH = 200 µA	AV_{DD1} – 0.1	–	–	V
Settling time	t_{SET_AMP00}	GCn = 00H (9.5 dB), CCn1, CCn0 = 0, 0, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	8	µs
	t_{SET_AMP01}	GCn = 00H (9.5 dB), CCn1, CCn0 = 0, 1, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	10	µs
	t_{SET_AMP10}	GCn = 00H (9.5 dB), CCn1, CCn0 = 1, 0, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	16	µs
	t_{SET_AMP11}	GCn = 00H (9.5 dB), CCn1, CCn0 = 1, 1, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	42	µs
Gain bandwidth	GBW00	CL_{MAX} = 30 pF, CCn1, CCn0 = 0, 0 GCn = 11H (40.1 dB)	–	1.35	–	MHz
	GBW01	CL_{MAX} = 30 pF, CCn1, CCn0 = 0, 1 GCn = 11H (40.1 dB)	–	1.1	–	MHz
	GBW10	CL_{MAX} = 30 pF, CCn1, CCn0 = 1, 0 GCn = 11H (40.1 dB)	–	0.75	–	MHz
	GBW11	CL_{MAX} = 30 pF, CCn1, CC0 = 1, 1 GCn = 11H (40.1 dB)	–	0.4	–	MHz
Equivalent input noise	En00	CCn1, CCn0 = 0, 0 f = 1 kHz, GCn = 11H (40.1 dB)	–	67	–	nV/√ Hz
	En01	CCn1, CCn0 = 0, 1 f = 1 kHz, GCn = 11H (40.1 dB)	–	75	–	nV/√ Hz
	En10	CCn1, CCn0 = 1, 0 f = 1 kHz, GCn = 11H (40.1 dB)	–	110	–	nV/√ Hz
	En11	CCn1, CCn0 = 1, 1 f = 1 kHz, GCn = 11H (40.1 dB)	–	145	–	nV/√ Hz

Note These are the values for one channel of configurable amplifier.

Remark n = 1 to 3

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Input conversion offset voltage	VOFF1	CCn1, CCn0 = 0, 0, T_A = 25°C GCn = 0AH (26.4 dB)	–7	–	7	mV
	VOFF2	CCn1, CCn0 = 0, 1, T_A = 25°C GCn = 0AH (26.4 dB)	–10	–	10	mV
	VOFF3	CCn1, CCn0 = 1, 0, T_A = 25°C GCn = 0AH (26.4 dB)	–10	–	10	mV
	VOFF4	CCn1, CCn0 = 1, 1, T_A = 25°C GCn = 0AH (26.4 dB)	–12	–	12	mV
Input conversion offset voltage temperature coefficient	VOTC00	CCn1, CCn0 = 0, 0	–	±3.5	–	µV/℃
	VOTC01	CCn1, CCn0 = 0, 1	–	±3.5	–	µV/℃
	VOTC10	CCn1, CCn0 = 1, 0	–	±4.0	–	µV/℃
	VOTC11	CCn1, CCn0 = 1, 1	–	±4.5	–	µV/℃
Slew rate	SR00	CCn1, CCn0 = 0, 0, CL = 30 pF GCn = 00H (9.5 dB)	–	1.1	–	V/µs
	SR01	CCn1, CCn0 = 0, 1, CL = 30 pF GCn = 00H (9.5 dB)	–	0.8	–	V/µs
	SR10	CCn1, CCn0 = 1, 0, CL = 30 pF GCn = 00H (9.5 dB)	–	0.5	–	V/µs
	SR11	CCn1, CCn0 = 1, 1, CL = 30 pF GCn = 00H (9.5 dB)	–	0.25	–	V/µs
Power supply rejection ratio	PSRR00	CCn1, CCn0 = 0, 0, GCn = 00H (9.5 dB) , f = 1 KHz	–	80	–	dB
	PSRR01	CCn1, CCn0 = 0, 1, GCn = 00H (9.5 dB) , f = 1 KHz	–	80	–	dB
	PSRR10	CCn1, CCn0 = 1, 0, GCn = 00H (9.5 dB) , f = 1 KHz	–	75	–	dB
	PSRR11	CCn1, CCn0 = 1, 1, GCn = 00H (9.5 dB) , f = 1 KHz	–	75	–	dB
Gain setting error	GAIN_Accu1	T_A = 25°C	–0.6	–	0.6	dB
	GAIN_Accu2	T_A = –40 to 105°C	–1.0	–	1.0	dB

Remark n = 1 to 3

(–40°C ≤ T_A ≤ 105°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 3.0 V, VREFIN1 = VREFIN2 = VREFIN3 = 1.5 V, AMP1OF = AMP2OF = AMP3OF = 1, DAC1OF = DAC2OF = DAC3OF, inverting amplifier)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption Note	Icc100	CCn1, CCn0 = 0, 0	–	330	500	µA
	Icc101	CCn1, CCn0 = 0, 1	–	250	380	µA
	Icc110	CCn1, CCn0 = 1, 0	–	170	260	µA
	Icc111	CCn1, CCn0 = 1, 1	–	90	150	µA
Input voltage 1	VINL1	IMSn = 0	AGND1 – 0.05	–	–	V
	VINH1	IMSn = 0	–	–	A_{VDD1} + 0.1	V
Input voltage 2	VINL2	IMSn = 1	AGND1 – 0.05	–	–	V
	VINH2	IMSn = 1	–	–	A_{VDD1} – 1.4	V
Output voltage	VOUTL	IOL = –200 µA	–	–	AGND1 + 0.1	V
	VOUTH	IOH = 200 µA	A_{VDD1} – 0.1	–	–	V
Settling time	t_{SET_AMP00}	GCn = 00H (6 dB), CCn1, CCn0 = 0, 0, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	8	µs
	t_{SET_AMP01}	GCn = 00H (6 dB), CCn1, CCn0 = 0, 1, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	10	µs
	t_{SET_AMP10}	GCn = 00H (6 dB), CCn1, CCn0 = 1, 0, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	16	µs
	t_{SET_AMP11}	GCn = 00H (6 dB), CCn1, CCn0 = 1, 1, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	42	µs
Gain bandwidth	GBW100	CL_{MAX} = 30 pF, CCn1, CCn0 = 0, 0 GCn = 11H (40 dB)	–	1.0	–	MHz
	GBW101	CL_{MAX} = 30 pF, CCn1, CCn0 = 0, 1 GCn = 11H (40 dB)	–	0.85	–	MHz
	GBW110	CL_{MAX} = 30 pF, CCn1, CCn0 = 1, 0 GCn = 11H (40 dB)	–	0.60	–	MHz
	GBW111	CL_{MAX} = 30 pF, CCn1, CCn0 = 1, 1 GCn = 11H (40 dB)	–	0.30	–	MHz
Equivalent input noise	En100	CCn1, CCn0 = 0, 0 f = 1 kHz, GCn = 11H (40 dB)	–	67	–	nV/√ Hz
	En101	CCn1, CCn0 = 0, 1 f = 1 kHz, GCn = 11H (40 dB)	–	75	–	nV/√ Hz
	En110	CCn1, CCn0 = 1, 0 f = 1 kHz, GCn = 11H (40 dB)	–	110	–	nV/√ Hz
	En111	CCn1, CCn0 = 1, 1 f = 1 kHz, GCn = 11H (40 dB)	–	145	–	nV/√ Hz

Note These are the values for one channel of configurable amplifier.

Remark n = 1 to 3

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Input conversion offset voltage	VOFF1	CCn1, CCn0 = 0, 0, T_A = 25°C GCn = 0AH (26 dB)	–7	–	7	mV
	VOFF2	CCn1, CCn0 = 0, 1, T_A = 25°C GCn = 0AH (26 dB)	–10	–	10	mV
	VOFF3	CCn1, CCn0 = 1, 0, T_A = 25°C GCn = 0AH (26 dB)	–10	–	10	mV
	VOFF4	CCn1, CCn0 = 1, 1, T_A = 25°C GCn = 0AH (26 dB)	–12	–	12	mV
Input conversion offset voltage temperature coefficient	VOTC00	CCn1, CCn0 = 0, 0	–	±3.5	–	µV/℃
	VOTC01	CCn1, CCn0 = 0, 1	–	±3.5	–	µV/℃
	VOTC10	CCn1, CCn0 = 1, 0	–	±4.0	–	µV/℃
	VOTC11	CCn1, CCn0 = 1, 1	–	±4.5	–	µV/℃
Slew rate	SR100	CCn1, CCn0 = 0, 0, CL = 30 pF GCn = 00H (6 dB)	–	1.2	–	V/µs
	SR101	CCn1, CCn0 = 0, 1, CL = 30 pF GCn = 00H (6 dB)	–	0.9	–	V/µs
	SR110	CCn1, CCn0 = 1, 0, CL = 30 pF GCn = 00H (6 dB)	–	0.6	–	V/µs
	SR111	CCn1, CCn0 = 1, 1, CL = 30 pF GCn = 00H (6 dB)	–	0.3	–	V/µs
Power supply rejection ratio	PSRR100	CCn1, CCn0 = 0, 0, GCn = 00H (6 dB), f = 1 kHz	–	80	–	dB
	PSRR101	CCn1, CCn0 = 0, 1, GCn = 00H (6 dB) , f = 1 kHz	–	80	–	dB
	PSRR110	CCn1, CCn0 = 1, 0, GCn = 00H (6 dB) , f = 1 kHz	–	80	–	dB
	PSRR111	CCn1, CCn0 = 1, 1, GCn = 00H (6 dB) , f = 1 kHz	–	80	–	dB
Gain setting error	GAIN_Accu1	T_A = 25°C	–0.6	–	0.6	dB
	GAIN_Accu2	T_A = –40 to 105°C	–1.0	–	1.0	dB

Remark n = 1 to 3

(–40°C ≤ T_A ≤ 105°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 3.0 V, VREFIN = VREFIN2 = VREFIN3 = 1.5 V, AMP1OF = AMP2OF = AMP3OF = 1, DAC1OF = DAC2OF = DAC3OF = 0, differential amplifier)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption Note	Icc00	CCn1, CCn0 = 0, 0	–	330	500	µA
	Icc01	CCn1, CCn0 = 0, 1	–	250	380	µA
	Icc10	CCn1, CCn0 = 1, 0	–	170	260	µA
	Icc11	CCn1, CCn0 = 1, 1	–	90	150	µA
Input voltage 1	VINL1	IMSn = 0	AGND1 – 0.05	–	–	V
	VINH1	IMSn = 0	–	–	AV_{DD1} + 0.1	V
Input voltage 2	VINL2	IMSn = 1	AGND1 – 0.05	–	–	V
	VINH2	IMSn = 1	–	–	AV_{DD1} – 1.4	V
Output voltage	VOUTL	IOL = –200 µA	–	–	AGND1 + 0.1	V
	VOUTH	IOH = 200 µA	AV_{DD1} – 0.1	–	–	V
Settling time	t_{SET_AMP00}	GCn = 00H (6 dB), CCn1, CCn0 = 0, 0, CL = 30 pF, output voltage = 1V_{PP}, output convergence voltage V_{PP} = 999 mV	–	–	8	µs
	t_{SET_AMP01}	GCn = 00H (6 dB), CCn1, CCn0 = 0, 1, CL = 30 pF, output voltage = 1V_{PP}, output convergence voltage V_{PP} = 999 mV	–	–	10	µs
	t_{SET_AMP10}	GCn = 00H (6 dB), CCn1, CCn0 = 1, 0, CL = 30 pF, output voltage = 1V_{PP}, output convergence voltage V_{PP} = 999 mV	–	–	16	µs
	t_{SET_AMP11}	GCn = 00H (6 dB), CCn1, CCn0 = 1, 1, CL = 30 pF, output voltage = 1V_{PP}, output convergence voltage V_{PP} = 999 mV	–	–	42	µs
Gain bandwidth	GBW00	CL_{MAX} = 30 pF, CCn1, CCn0 = 0, 0 GCn = 11H (40 dB)	–	1.0	–	MHz
	GBW01	CL_{MAX} = 30 pF, CCn1, CCn0 = 0, 1 GCn = 11H (40 dB)	–	0.85	–	MHz
	GBW10	CL_{MAX} = 30 pF, CCn1, CCn0 = 1, 0 GCn = 11H (40 dB)	–	0.60	–	MHz
	GBW11	CL_{MAX} = 30 pF, CCn1, CCn0 = 1, 1 GCn = 11H (40 dB)	–	0.30	–	MHz
Equivalent input noise	En00	CCn1, CCn0 = 0, 0 f = 1 kHz, GCn = 11H (40 dB)	–	67	–	nV/√ Hz
	En01	CCn1, CCn0 = 0, 1 f = 1 kHz, GCn = 11H (40 dB)	–	75	–	nV/√ Hz
	En10	CCn1, CCn0 = 1, 0 f = 1 kHz, GCn = 11H (40 dB)	–	110	–	nV/√ Hz
	En11	CCn1, CCn0 = 1, 1 f = 1 kHz, GCn = 11H (40 dB)	–	145	–	nV/√ Hz

Note These are the values for one channel of configurable amplifier.

Remark n = 1 to 3

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Input conversion offset voltage	VOFF1	CCn1, CCn0 = 0, 0, T_A = 25°C GCn = 0AH (26 dB)	–7	–	7	mV
	VOFF2	CCn1, CCn0 = 0, 1, T_A = 25°C GCn = 0AH (26 dB)	–10	–	10	mV
	VOFF3	CCn1, CCn0 = 1, 0, T_A = 25°C GCn = 0AH (26 dB)	–10	–	10	mV
	VOFF4	CCn1, CCn0 = 1, 1, T_A = 25°C GCn = 0AH (26 dB)	–12	–	12	mV
Input conversion offset voltage temperature coefficient	VOTC00	CCn1, CCn0 = 0, 0	–	±3.5	–	μV/℃
	VOTC01	CCn1, CCn0 = 0, 1	–	±3.5	–	μV/℃
	VOTC10	CCn1, CCn0 = 1, 0	–	±4.0	–	μV/℃
	VOTC11	CCn1, CCn0 = 1, 1	–	±4.5	–	μV/℃
Slew rate	SR00	CCn1, CCn0 = 0, 0, CL = 30 pF GCn = 00H (6 dB)	–	1.15	–	V/μs
	SR01	CCn1, CCn0 = 0, 1, CL = 30 pF GCn = 00H (6 dB)	–	0.85	–	V/μs
	SR10	CCn1, CCn0 = 1, 0, CL = 30 pF GCn = 00H (6 dB)	–	0.6	–	V/μs
	SR11	CCn1, CCn0 = 1, 1, CL = 30 pF GCn = 00H (6 dB)	–	0.3	–	V/μs
Common mode rejection ratio	CMRR00	CCn1, CCn0 = 0, 0, GCn = 11H (40 dB), f = 1 kHz	–	80	–	dB
	CMRR01	CCn1, CCn0 = 0, 1, GCn = 11H (40 dB), f = 1 kHz	–	80	–	dB
	CMRR10	CCn1, CCn0 = 1, 0, GCn = 11H (40 dB), f = 1 kHz	–	80	–	dB
	CMRR11	CCn1, CCn0 = 1, 1, GCn = 11H (40 dB), f = 1 kHz	–	80	–	dB
Power supply rejection ratio	PSRR00	CCn1, CCn0 = 0, 0, GCn = 00H (6 dB), f = 1 kHz	–	80	–	dB
	PSRR01	CCn1, CCn0 = 0, 1, GCn = 00H (6 dB), f = 1 kHz	–	80	–	dB
	PSRR10	CCn1, CCn0 = 1, 0, GCn = 00H (6 dB), f = 1 kHz	–	80	–	dB
	PSRR11	CCn1, CCn0 = 1, 1, GCn = 00H (6 dB), f = 1 kHz	–	80	–	dB
Gain setting error	GAIN_Accu1	T_A = 25°C	–0.6	–	0.6	dB
	GAIN_Accu2	T_A = –40 to 105°C	–1.0	–	1.0	dB

Remark n = 1 to 3

($–40°C \le T_A \le 105°C$, $AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 3.0$ V, VREFIN1 = VREFIN2 = VREFIN3 = 1.5 V, AMP1OF = AMP2OF = AMP3OF = 1, DAC1OF = DAC2OF = DAC3OF = 0, transimpedance amplifier)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption Note	Icc00	CCn1, CCn0 = 0, 0	–	330	500	µA
	Icc01	CCn1, CCn0 = 0, 1	–	250	380	µA
	Icc10	CCn1, CCn0 = 1, 0	–	170	260	µA
	Icc11	CCn1, CCn0 = 1, 1	–	90	150	µA
Input voltage1	VINL1	IMSn = 0	AGND1 – 0.05	–	–	V
	VINH1	IMSn = 0	–	–	AV_{DD1} + 0.1	V
Input voltage2	VINL2	IMSn = 1	AGND1 – 0.05	–	–	V
	VINH2	IMSn = 1	–	–	AV_{DD1} - 1.4	V
Output voltage	VOUTL	IOL = –200 µA	–	–	AGND1 + 0.1	V
	VOUTH	IOH = 200 µA	AV_{DD1} – 0.1	–	–	V
Settling time	t_{SET_AMP00}	GCn = 00H (20 kΩ), CCn1, CCn0 = 0, 0, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	8	µs
	t_{SET_AMP01}	GCn = 00H (20 kΩ), CCn1, CCn0 = 0, 1, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	10	µs
	t_{SET_AMP10}	GCn = 00H (20 kΩ), CCn1, CCn0 = 1, 0, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	16	µs
	t_{SET_AMP11}	GCn = 00H (20 kΩ), CCn1, CCn0 = 1, 1, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	42	µs
Current-to-voltage conversion gain bandwidth	GBW00_0	CL_{MAX} = 30 pF, CCn1, CCn0 = 0, 0, GCn = 00H (Rfb = 20 kΩ)	–	0.75	–	MHz
	GBW00_1	CL_{MAX} = 30 pF, CCn1, CCn0 = 0, 0, GCn = 0FH (Rfb = 640 kΩ)	–	0.75	–	MHz
	GBW01_0	CL_{MAX} = 30 pF, CCn1, CCn0 = 0, 1, GCn = 00H (Rfb = 20 kΩ)	–	0.65	–	MHz
	GBW01_1	CL_{MAX} = 30 pF, CCn1, CCn0 = 0, 1, GCn = 0FH (Rfb = 640 kΩ)	–	0.7	–	MHz
	GBW10_0	CL_{MAX} = 30 pF, CCn1, CCn0 = 1, 0, GCn = 00H (Rfb = 20 kΩ)	–	0.45	–	MHz
	GBW10_1	CL_{MAX} = 30 pF, CCn1, CCn0 = 1, 0, GCn = 0FH (Rfb = 640 kΩ)	–	0.5	–	MHz
	GBW11_0	CL_{MAX} = 30 pF, CCn1, CCn0 = 1, 1, GCn = 00H (Rfb = 20 kΩ)	–	0.25	–	MHz
	GBW11_1	CL_{MAX} = 30 pF, CCn1, CCn0 = 1, 1, GCn = 0FH (Rfb = 640 kΩ)	–	0.3	–	MHz

Note These are the values for one channel of configurable amplifier.

Remark n = 1 to 3

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Equivalent input noise	En00	CCn1, CCn0 = 0, 0 f = 1 kHz, GCn = 00H (Rfb = 20 kΩ)	–	3	–	pA/√Hz
	En01	CCn1, CCn0 = 0, 1 f = 1 kHz, GCn = 00H (Rfb = 20 kΩ)	–	4	–	pA/√Hz
	En10	CCn1, CCn0 = 1, 0 f = 1 kHz, GCn = 00H (Rfb = 20 kΩ)	–	5	–	pA/√Hz
	En11	CCn1, CCn0 = 1, 1 f = 1 kHz, GCn = 00H (Rfb = 20 kΩ)	–	7	–	pA/√Hz
Input conversion offset voltage	VOFF1	CCn1, CCn0 = 0, 0, T_A = 25°C GCn = 0AH (Rfb = 160 kΩ)	–7	–	7	mV
	VOFF2	CCn1, CCn0 = 0, 1, T_A = 25°C GCn = 0AH (Rfb = 160 kΩ)	–10	–	10	mV
	VOFF3	CCn1, CCn0 = 1, 0, T_A = 25°C GCn = 0AH (Rfb = 160 kΩ)	–10	–	10	mV
	VOFF4	CCn1, CCn0 = 1, 1, T_A = 25°C GCn = 0AH (Rfb = 160 kΩ)	–12	–	12	mV
Input conversion offset voltage temperature coefficient	VOTC00	CCn1, CCn0 = 0, 0	–	±3.5	–	µV/℃
	VOTC01	CCn1, CCn0 = 0, 1	–	±3.5	–	µV/℃
	VOTC10	CCn1, CCn0 = 1, 0	–	±4.0	–	µV/℃
	VOTC11	CCn1, CCn0 = 1, 1	–	±4.5	–	µV/℃
Slew rate	SR00	CCn1, CCn0 = 0, 0, GCn = 00H (Rfb = 20 kΩ)	–	1.15	–	V/µs
	SR01	CCn1, CCn0 = 0, 1, GCn = 00H (Rfb = 20 kΩ)	–	0.85	–	V/µs
	SR10	CCn1, CCn0 = 1, 0, GCn = 00H (Rfb = 20 kΩ)	–	0.6	–	V/µs
	SR11	CCn1, CCn0 = 1, 1, GCn = 00H (Rfb = 20 kΩ)	–	0.3	–	V/µs
Power supply rejection ratio	PSRR00	CCn1, CCn0 = 0, 0, GCn = 00H (Rfb = 20 kΩ), f = 1 kHz	–	60	–	dB
	PSRR01	CCn1, CCn0 = 0, 1, GCn = 00H (Rfb = 20 kΩ), f = 1 kHz	–	60	–	dB
	PSRR10	CCn1, CCn0 = 1, 0, GCn = 00H (Rfb = 20 kΩ), f = 1 kHz	–	60	–	dB
	PSRR11	CCn1, CCn0 = 1, 1, GCn = 00H (Rfb = 20 kΩ), f = 1 kHz	–	60	–	dB
Rfb setting error	Rfb_Accu1	T_A = 25°C	–25	–	25	%
	Rfb_Accu2	T_A = –40 to 105°C	–35	–	35	%

Remark n = 1 to 3

(–40°C ≤ TA ≤ 105°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 3.0 V, VREFIN1 = VREFIN2 = VREFIN3 = 1.5 V, AMP1OF = AMP2OF = AMP3OF = 1, DAC1OF = DAC2OF = DAC3OF = 0, GC1 = GC2 = 00H, instrumentation amplifier)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption	Icc00	AMP1OF = AMP2OF = AMP3OF = 1, CCn1, CCn0 = 0, 0	–	960	1400	µA
	Icc01	AMP1OF = AMP2OF = AMP3OF = 1, CCn1, CCn0 = 0, 1	–	750	1100	µA
	Icc10	AMP1OF = AMP2OF = AMP3OF = 1, CCn1, CCn0 = 1, 0	–	520	750	µA
	Icc11	AMP1OF = AMP2OF = AMP3OF = 1, CCn1, CCn0 = 1, 1	–	310	450	µA
Input voltage 1	VINL1	IMSn = 0	AGND1 – 0.05	–	–	V
	VINH1	IMSn = 0	–	–	AV_{DD1} + 0.1	V
Input voltage 2	VINL2	IMSn = 1	AGND1 – 0.05	–	–	V
	VINH2	IMSn = 1	–	–	AV_{DD1} – 1.4	V
Output voltage	VOUTL	IOL = –200 µA	–	–	AGND1 + 0.05	V
	VOUTH	IOH = 200 µA	AV_{DD1} – 0.05	–	–	V
Settling time	t_{SET_AMP00}	GCn = 00H (15.5 dB), CCn1, CCn0 = 0, 0, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	9	µs
	t_{SET_AMP01}	GCn = 00H (15.5 dB), CCn1, CCn0 = 0, 1, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	12	µs
	t_{SET_AMP10}	GCn = 00H (15.5 dB), CCn1, CCn0 = 1, 0, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	20	µs
	t_{SET_AMP11}	GCn = 00H (15.5 dB), CCn1, CCn0 = 1, 1, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	56	µs
Gain bandwidth	GBW00	CL_{MAX} = 30 pF, CCn1, CCn0 = 0, 0 GC3 = 09H (33.5 dB)	–	1.0	–	MHz
	GBW01	CL_{MAX} = 30 pF, CCn1, CCn0 = 0, 1 GC3 = 09H (33.5 dB)	–	0.9	–	MHz
	GBW10	CL_{MAX} = 30 pF, CCn1, CCn0 = 1, 0 GC3 = 09H (33.5 dB)	–	0.65	–	MHz
	GBW11	CL_{MAX} = 30 pF, CCn1, CCn0 = 1, 1 GC3 = 09H (33.5 dB)	–	0.35	–	MHz
Equivalent input noise	En00	CCn1, CCn0 = 0, 0 GC3 = 09H (33.5 dB), f = 1 kHz	–	95	–	nV/√ Hz
	En01	CCn1, CCn0 = 0, 1 GC3 = 09H (33.5 dB), f = 1 kHz	–	110	–	nV/√ Hz
	En10	CCn1, CCn0 = 1, 0 GC3 = 09H (33.5 dB), f = 1 kHz	–	135	–	nV/√ Hz
	En11	CCn1, CCn0 = 1, 1 GC3 = 09H (33.5 dB), f = 1 kHz	–	200	–	nV/√ Hz

Remark n = 1 to 3

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Input conversion offset voltage	VOFF1	CCn1, CCn0 = 0, 0, T_A = 25°C GC3 = 05H (25.5 dB)	–7	–	7	mV
	VOFF2	CCn1, CCn0 = 0, 1, T_A = 25°C GC3 = 05H (25.5 dB)	–10	–	10	mV
	VOFF3	CCn1, CCn0 = 1, 0, T_A = 25°C GC3 = 05H (25.5 dB)	–10	–	10	mV
	VOFF4	CCn1, CCn0 = 1, 1, T_A = 25°C GC3 = 05H (25.5 dB)	–12	–	12	mV
Input conversion offset voltage temperature coefficient	VOTC00	CCn1, CCn0 = 0, 0	–	±2.5	–	μV/℃
	VOTC01	CCn1, CCn0 = 0, 1	–	±2.5	–	μV/℃
	VOTC10	CCn1, CCn0 = 1, 0	–	±3.0	–	μV/℃
	VOTC11	CCn1, CCn0 = 1, 1	–	±4.5	–	μV/℃
Slew rate	SR00	CCn1, CCn0 = 0, 0, CL = 30 pF GC3 = 00H (15.5 dB)	–	1.1	–	V/μs
	SR01	CCn1, CCn0 = 0, 1, CL = 30 pF GC3 = 00H (15.5 dB)	–	0.8	–	V/μs
	SR10	CCn1, CCn0 = 1, 0, CL = 30 pF GC3 = 00H (15.5 dB)	–	0.5	–	V/μs
	SR11	CCn1, CCn0 = 1, 1, CL = 30 pF GC3 = 00H (15.5 dB)	–	0.25	–	V/μs
Common mode rejection ratio	CMRR00	CCn1, CCn0 = 0, 0 GC3 = 09H (33.5 dB), f = 1 kHz	–	70	–	dB
	CMRR01	CCn1, CCn0 = 0, 1 GC3 = 09H (33.5 dB), f = 1 kHz	–	70	–	dB
	CMRR10	CCn1, CCn0 = 1, 0 GC3 = 09H (33.5 dB), f = 1 kHz	–	70	–	dB
	CMRR11	CCn1, CCn0 = 1, 1 GC3 = 09H (33.5 dB), f = 1 kHz	–	70	–	dB
Power supply rejection ratio	PSRR00	CCn1, CCn0 = 0, 0 GC3 = 00H (15.5 dB), f = 1 kHz	–	75	–	dB
	PSRR01	CCn1, CCn0 = 0, 1 GC3 = 00H (15.5 dB), f = 1 kHz	–	70	–	dB
	PSRR10	CCn1, CCn0 = 1, 0 GC3 = 00H (15.5 dB), f = 1 kHz	–	70	–	dB
	PSRR11	CCn1, CCn0 = 1, 1 GC3 = 00H (15.5 dB), f = 1 kHz	–	65	–	dB
Gain setting error	GAIN_Accu	T_A = 25°C	–0.8		0.8	dB
		T_A = –40 to 105°C	–1.2		1.2	dB

Remark n = 1 to 3

($-40°C \le T_A \le 105°C$, $AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 3.0$ V, VREFIN1 = VREFIN2 = VREFIN3 = 1.5 V, AMP1OF = AMP2OF = AMP3OF = 1, DAC1OF = DAC2OF = DAC3OF = 0, general-purpose operational amplifier)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption Note	Icc00	CCn1, CCn0 = 0, 0		330	500	µA
	Icc01	CCn1, CCn0 = 0, 1		250	380	µA
	Icc10	CCn1, CCn0 = 1, 0		170	260	µA
	Icc11	CCn1, CCn0 = 1, 1		90	150	µA
Input voltage 1	VINL1	IMSn = 0	AGND1 – 0.05	–	–	V
	VINH1	IMSn = 0	–	–	AV_{DD1} + 0.1	V
Input voltage 2	VINL2	IMSn = 1	AGND1 – 0.05	–	–	V
	VINH2	IMSn = 1	–	–	AV_{DD1} – 1.4	V
Output voltage	VOUTL	IOL = –200 µA	–	–	AGND1 + 0.1	V
	VOUTH	IOH = 200 µA	AV_{DD1} – 0.1	–	–	V
Gain bandwidth	GBW00	Configured as an inverting amplifier with 20 dB gain, CL_{MAX} = 30 pF, CCn1, CCn0 = 0, 0	–	1.6	–	MHz
	GBW01	Configured as an inverting amplifier with 20 dB gain, CL_{MAX} = 30 pF, CCn1, CCn0 = 0, 1	–	1.1	–	MHz
	GBW10	Configured as an inverting amplifier with 20 dB gain, CL_{MAX} = 30 pF, CC1n, CCn0 = 1, 0	–	0.65	–	MHz
	GBW11	Configured as an inverting amplifier with 20 dB gain, CL_{MAX} = 30 pF, CCn1, CCn0 = 1, 1	–	0.25	–	MHz
Equivalent input noise	En00	Configured as an inverting amplifier with 20 dB gain, CCn1, CCn0 = 0, 0, f = 1 kHz	–	76	–	nV/√ Hz
	En01	Configured as an inverting amplifier with 20 dB gain, CCn1, CCn0 = 0, 1, f = 1 kHz	–	90	–	nV/√ Hz
	En10	Configured as an inverting amplifier with 20 dB gain, CCn1, CCn0 = 1, 0, f = 1 kHz	–	110	–	nV/√ Hz
	En11	Configured as an inverting amplifier with 20 dB gain, CCn1, CCn0 = 1, 1, f = 1 kHz	–	165	–	nV/√ Hz
Input conversion offset voltage	VOFF1	Configured as an inverting amplifier with 20 dB gain, CCn1, CCn0 = 0, 0, T_A = 25°C	–7	–	7	mV
	VOFF2	Configured as an inverting amplifier with 20 dB gain, CCn1, CCn0 = 0, 1, T_A = 25°C	–10	–	10	mV
	VOFF3	Configured as an inverting amplifier with 20 dB gain, CCn1, CCn0 = 1, 0, T_A = 25°C	–10	–	10	mV
	VOFF4	Configured as an inverting amplifier with 20 dB gain, CCn1, CCn0 = 1, 1, T_A = 25°C	–12	–	12	mV

Note These are the values for one channel of configurable amplifier.

Remark n = 1 to 3

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Input conversion offset voltage temperature coefficient	VOTC00	Configured as an inverting amplifier with 20 dB gain, CCn1, CCn0 = 0, 0	–	±3.5	–	μV/℃
	VOTC01	Configured as an inverting amplifier with 20 dB gain, CCn1, CCn0 = 0, 1	–	±3.5	–	μV/℃
	VOTC10	Configured as an inverting amplifier with 20 dB gain, CCn1, CCn0 = 1, 0	–	±4.0	–	μV/℃
	VOTC11	Configured as an inverting amplifier with 20 dB gain, CCn1, CCn0 = 1, 1	–	±4.5	–	μV/℃
Slew rate	SR00	Configured as a voltage follower, CCn1, CCn0 = 0, 0, CL = 30 pF	–	0.98	–	V/μs
	SR01	Configured as a voltage follower, CCn1, CCn0 = 0, 1, CL = 30 pF	–	0.74	–	V/μs
	SR10	Configured as a voltage follower, CCn1, CCn0 = 1, 0, CL = 30 pF	–	0.49	–	V/μs
	SR11	Configured as a voltage follower, CCn1, CCn0 = 1, 1, CL = 30 pF	–	0.22	–	V/μs
Common mode rejection ratio	CMRR00	Configured as a differential amplifier with 20 dB gain, CCn1, CCn0 = 0, 0, f = 1 kHz	–	85	–	dB
	CMRR01	Configured as a differential amplifier with 20 dB gain, CCn1, CCn0 = 0, 1, f = 1 kHz	–	85	–	dB
	CMRR10	Configured as a differential amplifier with 20 dB gain, CCn1, CCn0 = 1, 0, f = 1 kHz	–	85	–	dB
	CMRR11	Configured as a differential amplifier with 20 dB gain, CCn1, CCn0 = 1, 1, f = 1 kHz	–	85	–	dB
Power supply rejection ratio	PSRR00	Configured as a voltage follower, CCn1, CCn0 = 0, 0, f = 1 kHz	–	80	–	dB
	PSRR01	Configured as a voltage follower, CCn1, CCn0 = 0, 1, f = 1 kHz	–	80	–	dB
	PSRR10	Configured as a voltage follower, CCn1, CCn0 = 1, 0, f = 1 kHz	–	80	–	dB
	PSRR11	Configured as a voltage follower, CCn1, CCn0 = 1, 1, f = 1 kHz	–	80	–	dB

Remark n = 1 to 3

(2) General-purpose operational amplifier

(−40°C ≤ T_A ≤ 105°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 3.0 V, AMP4OF = AMP5OF = 1)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption	IccA			320	450	µA
Input voltage 1	VINL1	IMSn = 0	AGND1 – 0.05	–	–	V
	VINH1	IMSn = 0	–	–	AV_{DD1} + 0.1	V
Input voltage 2	VINL2	IMSn = 1	AGND1 – 0.05	–	–	V
	VINH2	IMSn = 1	–	–	AV_{DD1} – 1.4	V
Output voltage	VOUTL	IOL = –200 µA	–	–	AGND1 + 0.05	V
	VOUTH	IOH = 200 µA	AV_{DD1} – 0.05	–	–	V
Gain bandwidth	GBW	Configured as an inverting amplifier with 20 dB gain, CL_{MAX} = 30 pF	–	2.0	–	MHz
Input conversion offset voltage	VOFF	Configured as an inverting amplifier with 20 dB gain, T_A = 25°C, AMP4_INP = AMP5_INP = 1.5 V	–7	–	7	mV
Input conversion offset voltage temperature coefficient	VOTC	Configured as an inverting amplifier with 20 dB gain	–	±2.0	–	µV/°C
Slew rate	SR	Configured as a voltage follower, CL = 30 pF	–	0.9	–	V/µs
Equivalent input noise	En_Gain	Configured as an inverting amplifier with 20 dB gain, f = 1 kHz	–	77	–	nV/√ Hz
Common mode rejection ratio	CMRR	Configured as a differential amplifier with 20 dB gain, f = 1 kHz	–	75	–	dB
Power supply rejection ratio	PSRR	Configured as an inverting amplifier with 20 dB gain, f = 1 kHz	–	55	–	dB

Remark n = 4, 5

(3) D/A converter

(–40°C ≤ T_A ≤ 105°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 3.0 V, DAC1OF = DAC2OF = DAC3OF = DAC4OF = DAC5OF = DAC6OF = DAC7OF = 1)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
<R> DAC ALL ON current consumption 1	I_{DAC_ON1}	DAC1OF = DAC2OF = DAC3OF = DAC4OF = DAC5OF = DAC6OF = DAC7OF = 1, VRB1, VRB0 = 0, 0	–	1.10	1.65	mA
<R> DAC ALL ON current consumption 2	I_{DAC_ON2}	DAC1OF = DAC2OF = DAC3OF = DAC4OF = DAC5OF = DAC6OF = DAC7OF = 1, VRB1, VRB0 = 0, 1	–	1.25	1.85	mA
Buffer AMP ON current consumption 1 Note1	I_{DAC_Buff1}	DACxOF = 1, VRB1, VRB0 = 0, 0 (x = 1, 2, 3, 4, 5, 6, 7)	–	180	220	µA
Buffer AMP ON current consumption 2 Note1	I_{DAC_Buff2}	DACxOF = 1, VRB1, VRB0 = 0, 1 (x = 1, 2, 3, 4, 5, 6, 7)	–	330	400	µA
DACx GAMP ON current consumption (x = 1, 2, 3, 5, 6, 7)	I_{DAC_AMP1} I_{DAC_AMP2} I_{DAC_AMP3} I_{DAC_AMP5} I_{DAC_AMP6} I_{DAC_AMP7}	DACxOF = 1 (x = 1, 2, 3, 5, 6, 7)	–	110	180	µA
DAC4 GAMP ON current consumption	I_{DAC_AMP4}	DAC4OF = 1	–	260	350	µA
Resolution	R_{ES}		–	–	8	bit
Settling time	t_{SET}		–	–	50	µs
Differential non-linearity error Note2	DNL	VRT1 = VRT0 = 0, VRB1 = VRB0 = 0	–2	–	2	LSB
Integral non-linearity error	INL	VRT1 = VRT0 = 0, VRB1 = VRB0 = 0	–2	–	2	LSB

Note1. Buffer amplifier is powered on when one of DACx (x = 1, 2, 3, 4, 5, 6, 7) is powered on at least. For example, the current consumption ($I_{EXAMPLE}$) is shown as a following equation when "DAC1OF=DAC2OF=1", and "VRB1, VRB0=0, 0". $I_{EXAMPLE} = I_{DAC\_Buff1} + I_{DAC\_AMP1} + I_{DAC\_AMP2}$

2. Guaranteed monotonic.

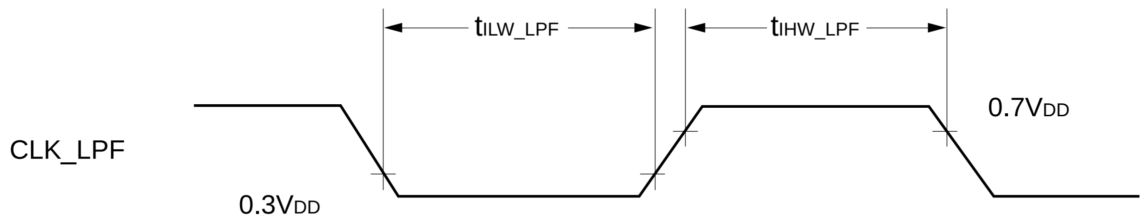
(4) Low-pass filter

($-40°C \leq T_A \leq 105°C$, $AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 3.0$ V, LPFOF = 1)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption	IccA		–	800	1200	µA
Input voltage 1	V_{ILLPF1}	IMSn = 0	AGND4 + 0.2	–	–	V
	V_{IHLPF1}	IMSn = 0	–	–	AV_{DD3} – 0.2	V
Input voltage 2	V_{ILLPF2}	IMSn = 1	AGND4 + 0.2	–	–	V
	V_{IHLPF2}	IMSn = 1	–	–	AV_{DD3} – 1.4	V
Output voltage	V_{OLLPF}	IOL = –200 µA	–	–	AGND4 – 0.2	V
	V_{OHLPF}	IOH = 200 µA	AV_{DD3} – 0.2	–	–	V
Input conversion offset voltage	VOFF	DAC4OF = 1, DAC4C = 80H	-100	–	100	mV
Cutoff frequency	fc1	f_{CLK_LPF} = 2 kHz	–	8.7	–	Hz
	fc2	f_{CLK_LPF} = 200 kHz	–	870	–	Hz
CLK_LPF low-level input voltage	V_{ILCLK_LPF}				$0.3 \times AV_{DD3}$	V
CLK_LPF high-level input voltage	V_{IHCLK_LPF}		$0.7 \times AV_{DD3}$			V
CLK_LPF Input frequency	f_{CLK_LPF}		2	–	200	kHz
CLK_LPF Input low-level-width Input high-level-width	t_{ILW_LPF} t_{IHW_LPF}		200	–	–	ns

Remark n = 6

Clock Timing



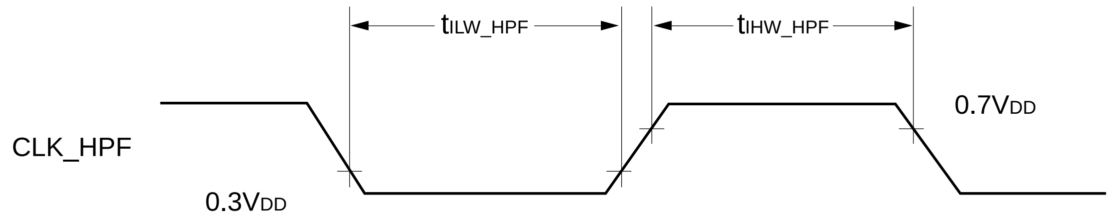
(5) High-pass filter

(–40°C ≤ T_A ≤ 105°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 3.0 V, HPFOF = 1)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption	IccA		–	800	1200	μA
Input voltage 1	V_{ILHPF1}	IMSn = 0	AGND4 + 0.2	–	–	V
	V_{IHHPF1}	IMSn = 0	–	–	AV_{DD3} – 0.2	V
Input voltage 2	V_{ILHPF2}	IMSn = 1	AGND4 + 0.2	–	–	V
	V_{IHHPF2}	IMSn = 1	–	–	AV_{DD3} – 1.4	V
Output voltage	V_{OLHPF}	IOL = –200 μA	–	–	AGND4 – 0.2	V
	V_{OHHPF}	IOH = 200 μA	AV_{DD3} – 0.2	–	–	V
Input conversion offset voltage	VOFF	DAC4OF = 1, DAC4C = 80H	-100	–	100	mV
Cutoff frequency	fc1	f_{CLK_HPF} = 2 kHz	–	7.4	–	Hz
	fc2	f_{CLK_HPF} = 200 kHz	–	740	–	Hz
CLK_HPF low-level input voltage	V_{ILCLK_HPF}				0.3 × AV_{DD3}	V
CLK_HPF high-level input voltage	V_{IHCLK_HPF}		0.7 × AV_{DD3}			V
CLK_HPF Input frequency	f_{CLK_HPF}		2	–	200	kHz
CLK_HPF Input low-level-width Input high-level-width	t_{ILW_HPF} t_{IHW_HPF}		200	–	–	ns

Remark n = 6

Clock Timing



(6) Temperature sensor

($-40°C \le T_A \le 105°C$, $AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 3.0$ V, TEMPOF = 1)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption	IccA		–	90	140	µA
Output voltage	V_O	T_A = 25°C	–	1.28	–	V
Temperature sensitivity	T_{SE}		–	–4.0	–	mV/°C

(7) Variable output voltage regulator

($-40°C \le T_A \le 105°C$, $AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 3.0$ V, LDOOF = 1)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption	IccON	Iout = 0 mA	–	80	120	µA
Output voltage accuracy	V_Accu	Iout = 0 mA	–10	–	10	%
Load current characteristics	Vout_load	Iout = 0 to 5 mA	–	15	30	mV
Output current	Iout		–	–	15	mA
Dropout voltage Note1	Vd	Iout = 15 mA	–	–	0.4	V
Power supply rejection ratio	PSRR	f = 1 kHz, CL = 1.0 µF, Iout = 5 mA, AV_{DD2} = 3.0 V, LDOC = 08H (2.6 V)	–	45	–	dB
Discharge resistance	Rs	LDOOF = 0	–	1.0	1.5	kΩ
Settling time	Tset_rise Note2	CL = 1.0 µF, Iout = 0 mA, LDOC = 08H (2.6 V)	–	–	200	µs
	Tset_fall Note2	CL = 1.0 µF, Iout = 0 mA, LDOC = 08H (2.6 V)	–	–	5	ms

Note1. The output voltage range is determined not only by dropout voltage but also by output voltage accuracy.

2. Tset_rise is defined as the time between operation enabled by power control register PC2 to output voltage being at 90% of its nominal value.

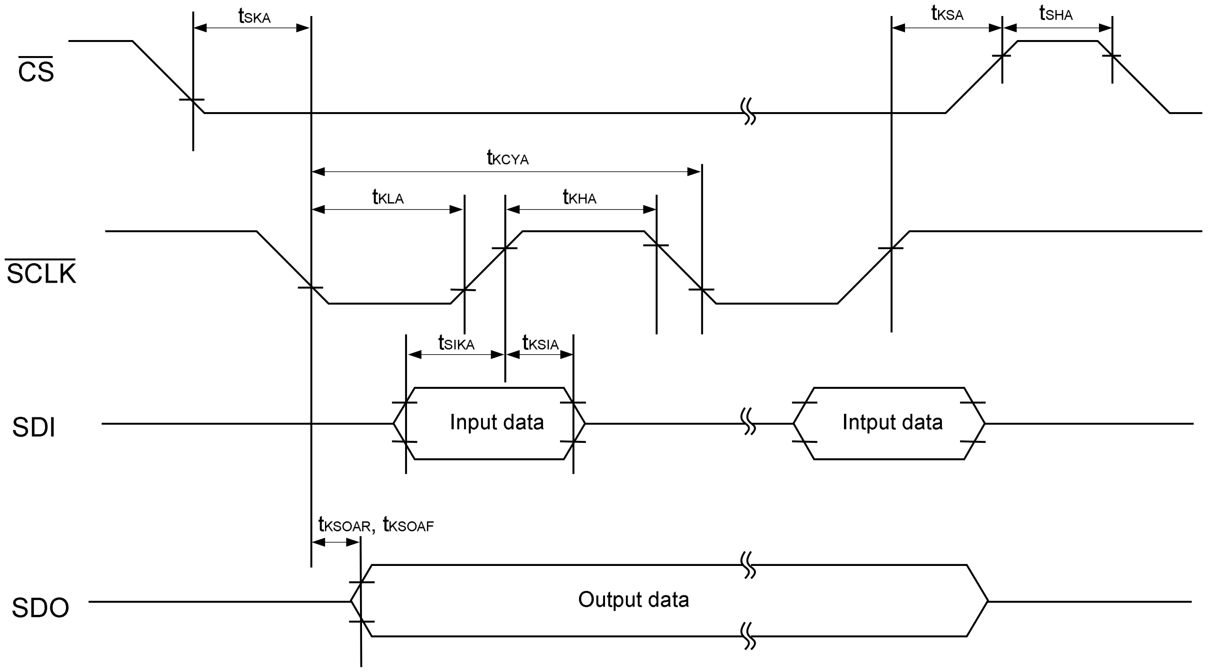
3. Tset_fall is defined as the time between operation disabled by power control register PC2 to output voltage being at 10% of its nominal value.

(8) SPI

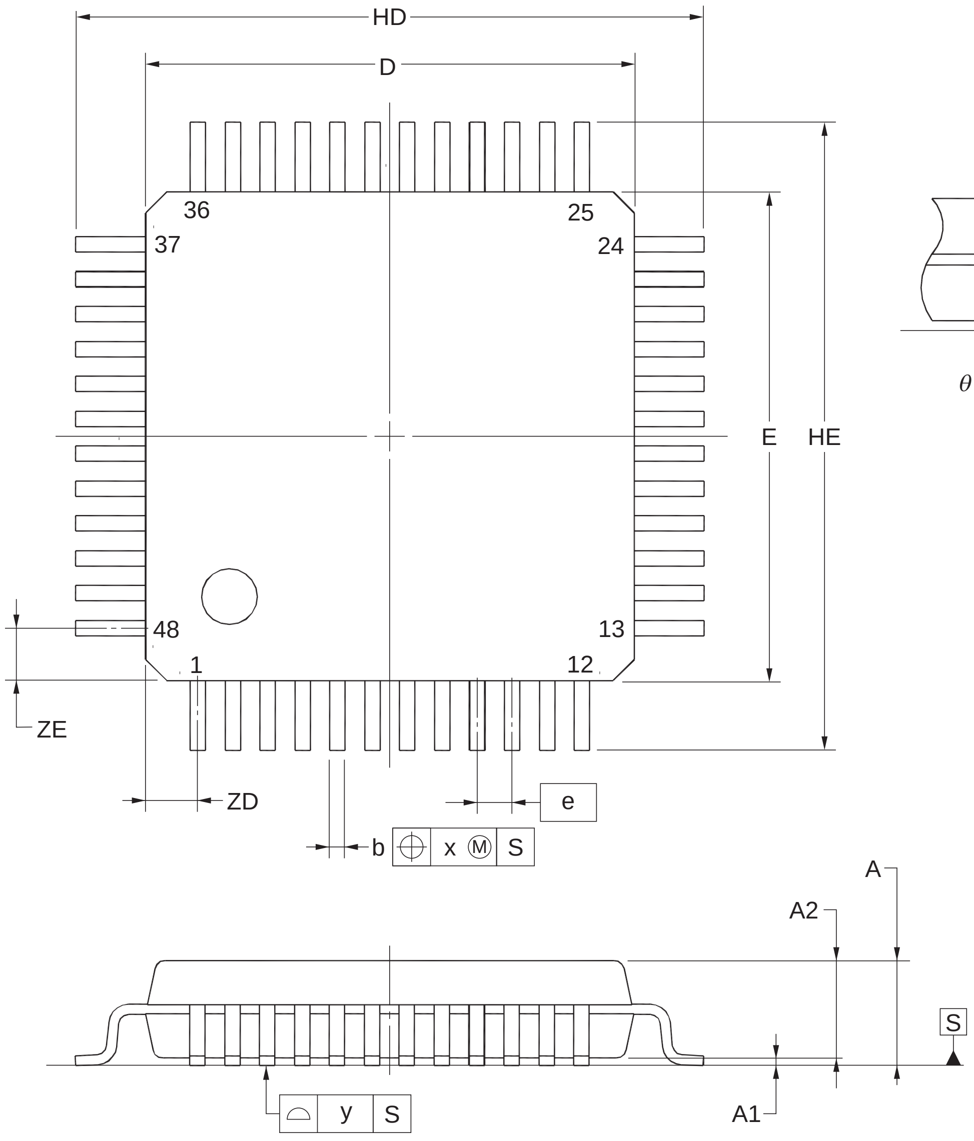
($-40°C \le T_A \le 105°C$, $AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 3.0$ V)

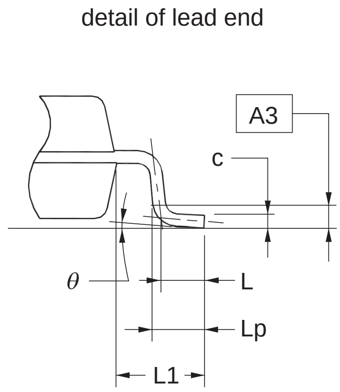
Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Input voltage, high	V_{IH}	$\overline{\text{CS}}$ pin, SDI pin, $\overline{\text{SCLK}}$ pin, $\overline{\text{RESET}}$ pin	$DV_{DD} \times 0.7$	–	$DV_{DD} + 0.1$	V
Input voltage, low	V_{IL}	$\overline{\text{CS}}$ pin, SDI pin, $\overline{\text{SCLK}}$ pin, $\overline{\text{RESET}}$ pin	DGND – 0.1	–	$DV_{DD} \times 0.3$	V
Leakage current during high level input	I_{leak_Hi1}	$\overline{\text{CS}}$ pin, SDI pin, $\overline{\text{SCLK}}$ pin	–2	–	2	µA
	I_{leak_Hi2}	$\overline{\text{RESET}}$ pin	–2	–	2	µA
Leakage current during low level input	I_{leak_Lo1}	$\overline{\text{CS}}$ pin, SDI pin, $\overline{\text{SCLK}}$ pin	–2	–	2	µA
	I_{leak_Lo2}	$\overline{\text{RESET}}$ pin	–2	–	2	µA
Low-level output voltage at SDO pin	V_{SDO_Lo}	I_O = -4 mA	–	250	400	mV
Leakage current when SDO pin is off	I_{leak_SDO}		–2	–	2	µA
Pull-up resistance	R_{SPI}	$\overline{\text{CS}}$ pin, SDI pin, $\overline{\text{SCLK}}$ pin RESET = L	–	50	75	kΩ
$\overline{\text{SCLK}}$ cycle time	t_{KCYA}		100	–	–	ns
$\overline{\text{SCLK}}$ high-level width low-level width	t_{KHA}, t_{KLA}		$0.8t_{KCYA}/2$	–	–	ns
SDI setup time (to $\overline{\text{SCLK}}$ ↑)	t_{SIKA}		40	–	–	ns
SDI hold time (from $\overline{\text{SCLK}}$ ↑)	t_{KSIA}		10	–	–	ns
Delay time from $\overline{\text{SCLK}}$ ↓ to SDO output	t_{KSOAR}	CL = 5 pF, VSDO = 3 V	–	–	40	ns
	t_{KSOAF}	CL = 5 pF, VSDO = 3 V	–	–	40	ns
$\overline{\text{CS}}$ high-level width	t_{SHA}		200	–	–	ns
Delay time from $\overline{\text{CS}}$ ↓ to $\overline{\text{SCLK}}$ ↓	t_{SKA}		200	–	–	ns
Delay time from $\overline{\text{SCLK}}$ ↑ to $\overline{\text{CS}}$ ↑	t_{KSA}		200	–	–	ns

SPI transfer clock timing



12. Package Drawing





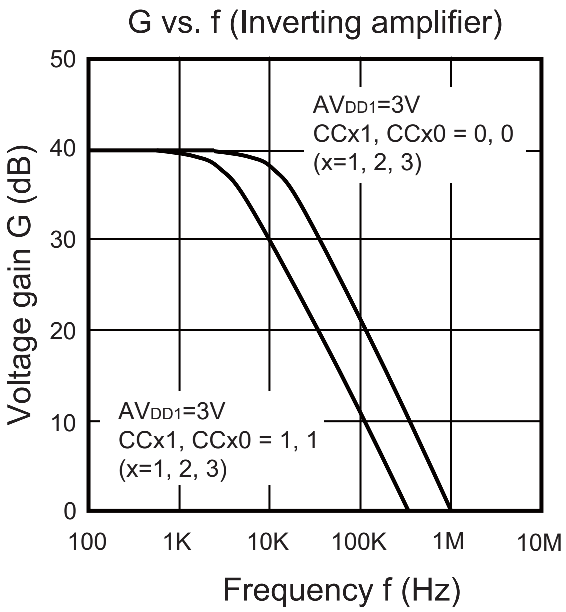
(UNIT:mm)

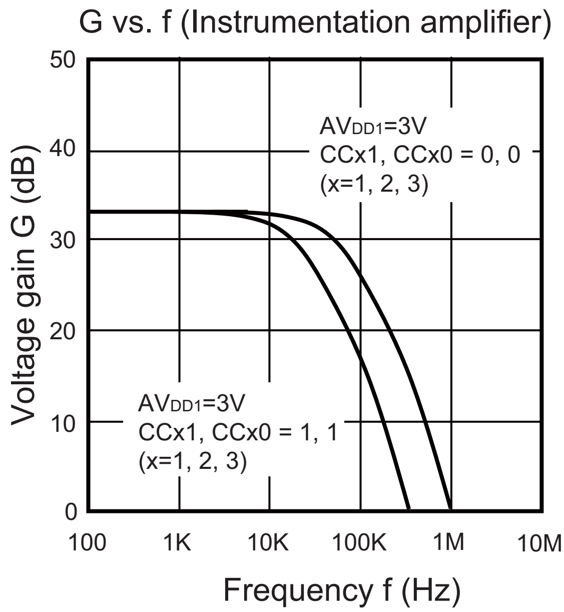
ITEM	DIMENSIONS
D	7.00±0.20
E	7.00±0.20
HD	9.00±0.20
HE	9.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	0.75
ZE	0.75

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

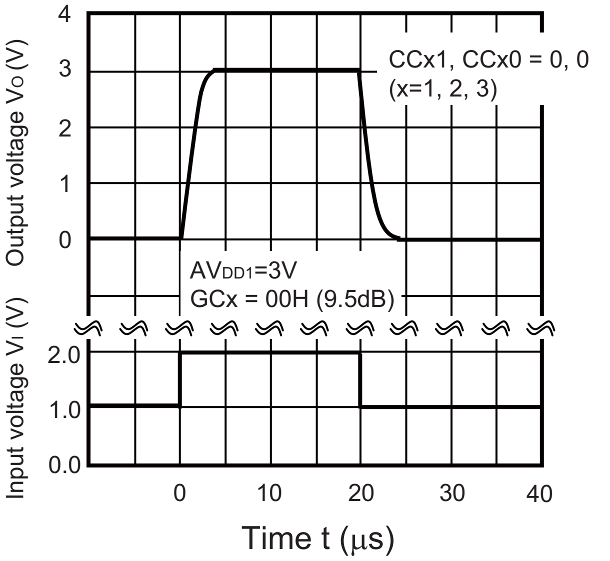
Characteristics Curve (T_A = 25°C, TYP.) (reference value)

- Configurable amplifier

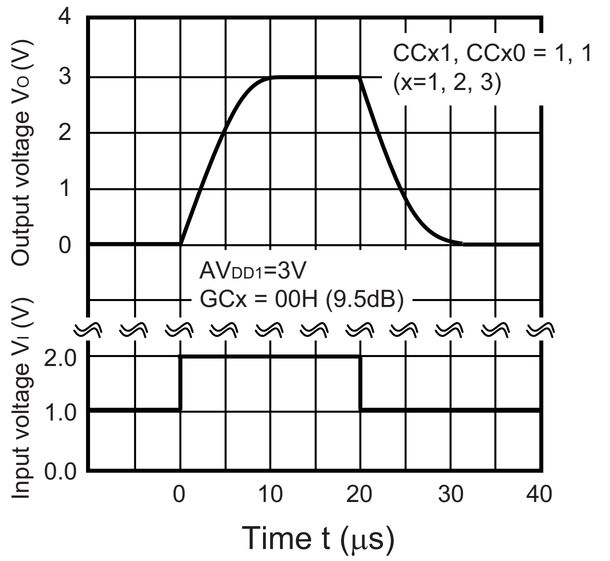




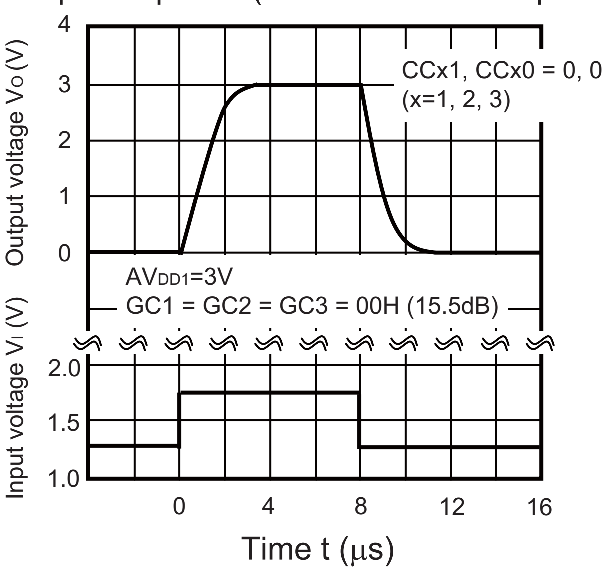
Output response (Non-inverting amplifier)



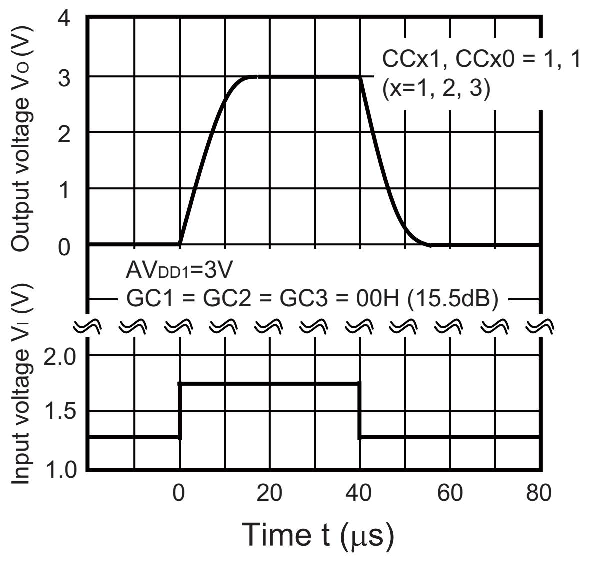
Output response (Non-inverting amplifier)

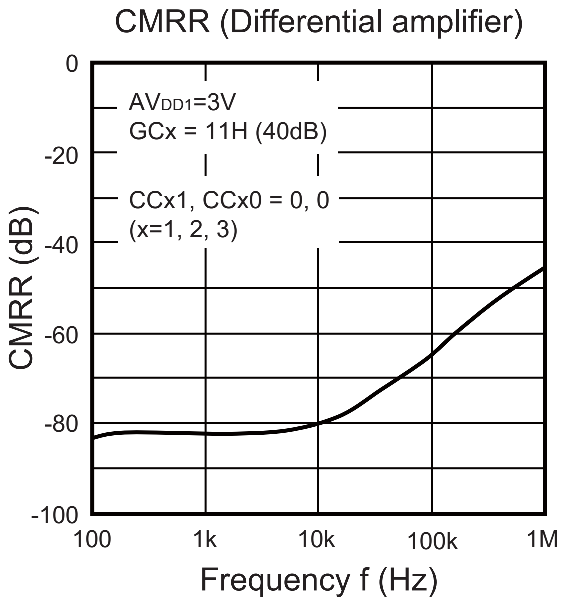


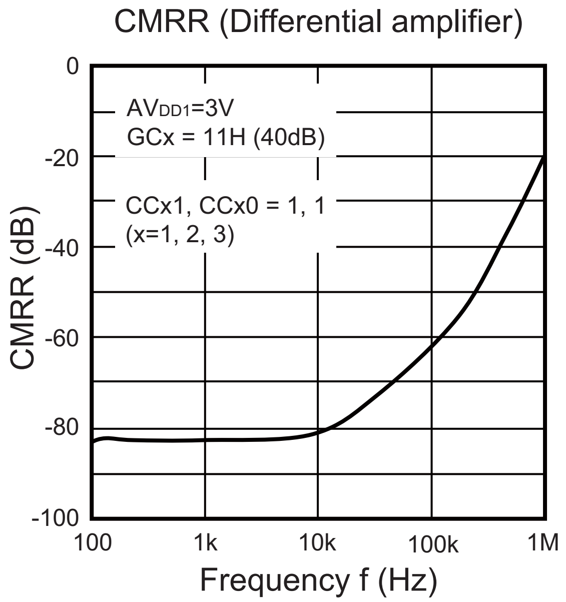
Output response (Instrumentation amplifier)

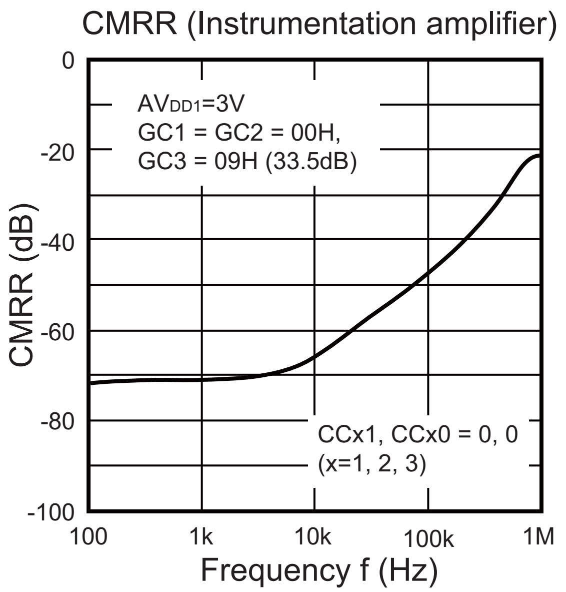


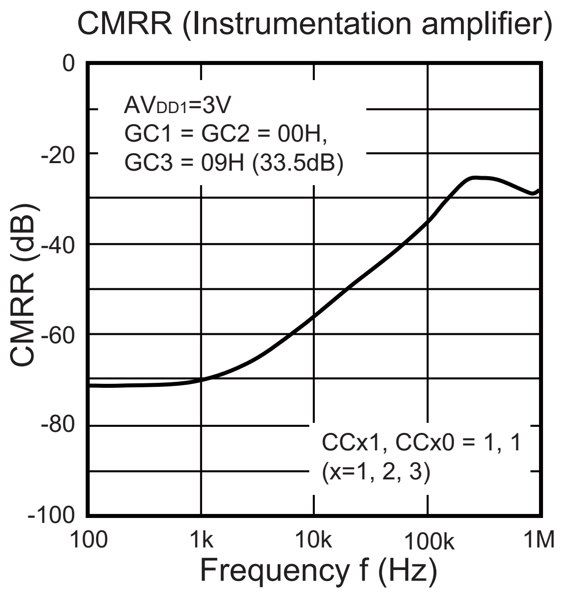
Output response (Instrumentation amplifier)



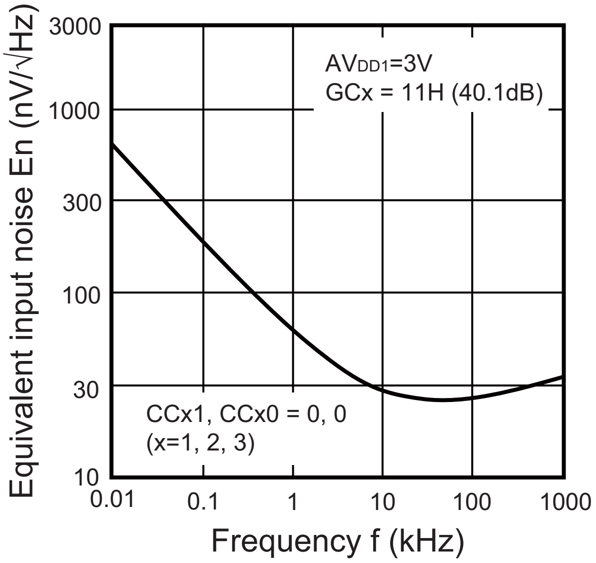

CMRR (Differential amplifier)
AVDD1=3V
GCx = 11H (40dB)
CCx1, CCx0 = 0, 0
(x=1, 2, 3)
CMRR (dB)
0
-20
-40
-60
-80
-100
100
1k
10k
100k
1M
Frequency f (Hz)


CMRR (Differential amplifier)
AVDD1=3V
GCx = 11H (40dB)
CCx1, CCx0 = 1, 1
(x=1, 2, 3)
CMRR (dB)
0
-20
-40
-60
-80
-100
100
1k
10k
100k
1M
Frequency f (Hz)

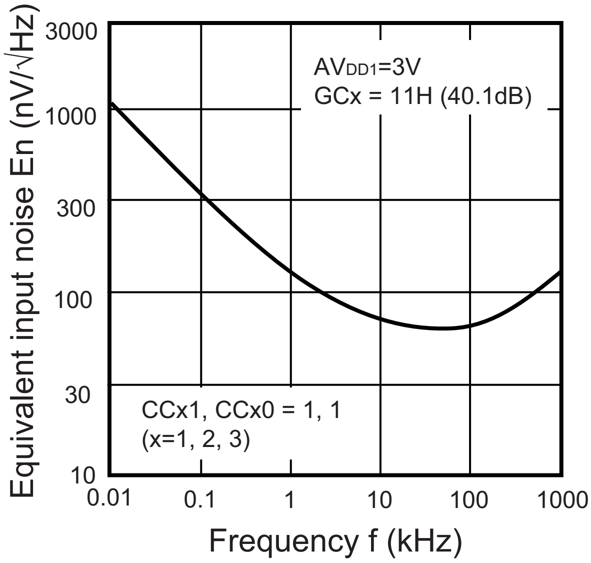

CMRR (Instrumentation amplifier)
AVDD1=3V
GC1 = GC2 = 00H,
GC3 = 09H (33.5dB)
CCx1, CCx0 = 0, 0
(x=1, 2, 3)
CMRR (dB)
0
-20
-40
-60
-80
-100
100
1k
10k
100k
1M
Frequency f (Hz)


CMRR (Instrumentation amplifier)
AVDD1=3V
GC1 = GC2 = 00H,
GC3 = 09H (33.5dB)
CCx1, CCx0 = 1, 1
(x=1, 2, 3)
CMRR (dB)
0
-20
-40
-60
-80
-100
100
1k
10k
100k
1M
Frequency f (Hz)

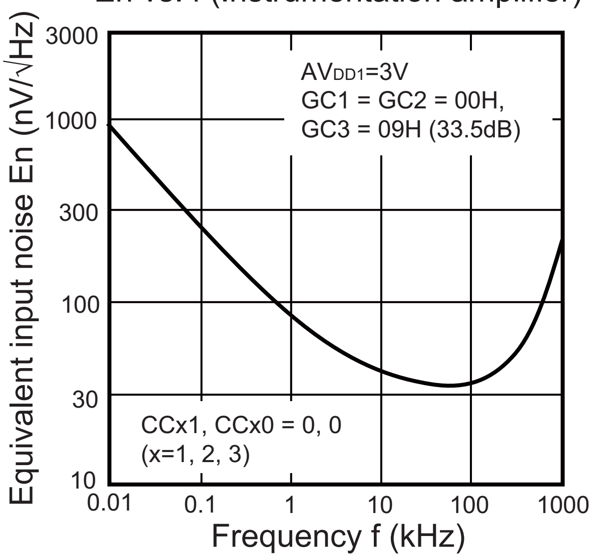
En vs. f (Non-inverting amplifier)



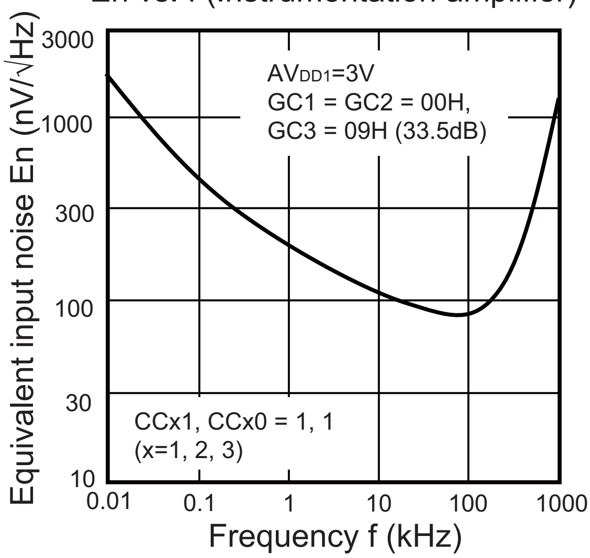
En vs. f (Non-inverting amplifier)



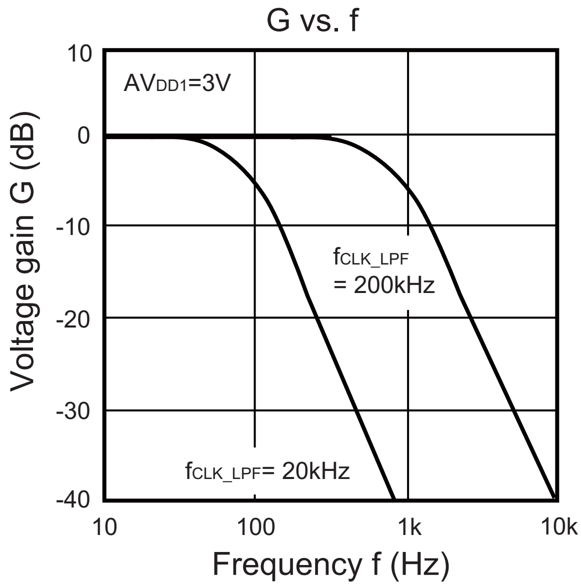
En vs. f (Instrumentation amplifier)

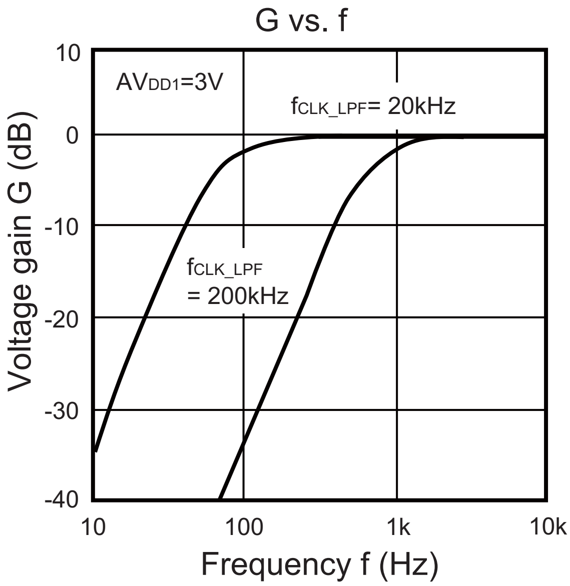


En vs. f (Instrumentation amplifier)

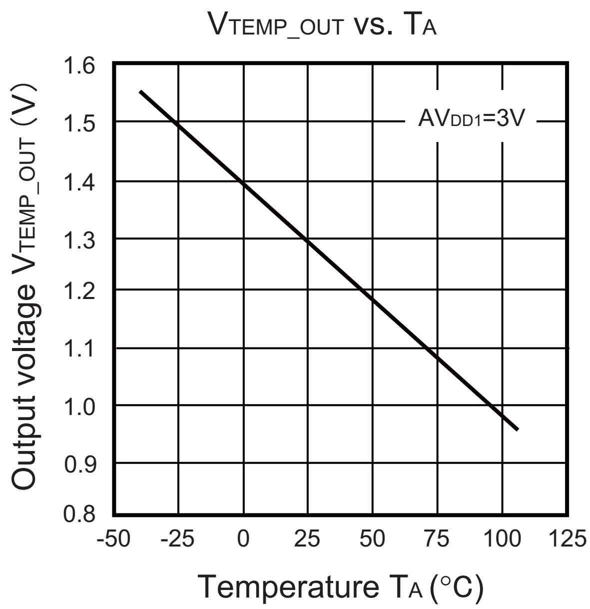


- Low-pass filter and high-pass filter

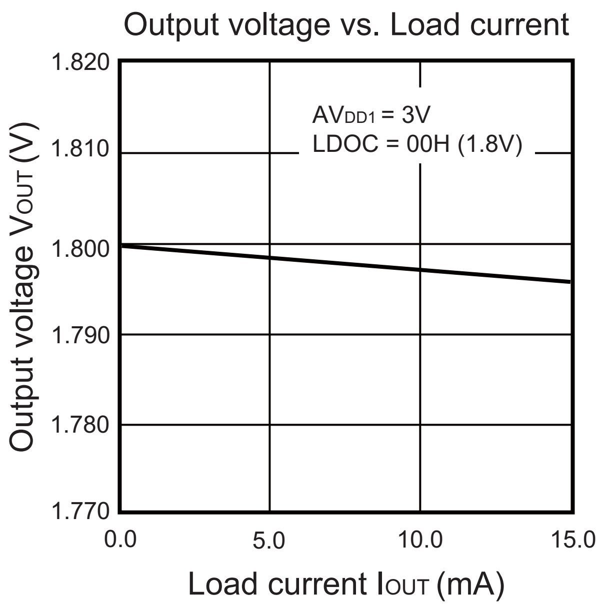


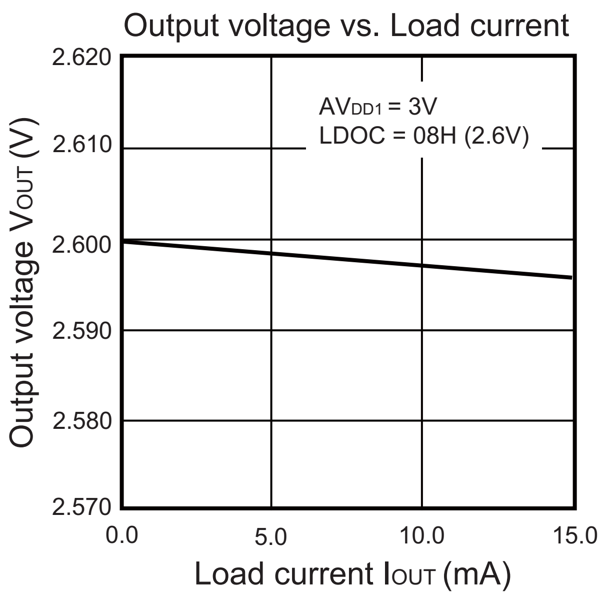


- Temperature sensor



- Variable output voltage regulator





Revision History	RAA730300 Monolithic Programmable Analog IC

Rev.	Date	Description	
		Page	Summary
1.00	Mar. 29, 2013	–	First edition issued.
1.10	May. 31, 2014	14	Change of description about reference voltage in *2. 1 Configurable Amplifiers*
		16	Correction of the register name controlling SW02 in *Figure 2-2*.
		34	Change of description in *2. 3 (9) Power control register 1 (PC1)*
		53	Change of description about reference voltage in *3. 1 General-Purpose Operational Amplifier*
		54	Addition of the register controlling SW53 to *Figure 3-2.*
		55	Change of description in *3. 3 (1) Power control register 1 (PC1)*
		59	Change of the calculating formula about output voltage in *4. 1 D/A Converters*
		61	Change of description in *4. 3 (1) DAC reference voltage control register (DACRC)*
		66	Change of description about reference voltage in *5. 1 Low-pass Filter*
		70	Change of description about reference voltage in *6. 1 High-Pass Filter*
		71	Change of description in *6. 3 (1) MPX setting register3 (MPX3)*
		81	Addition of Caution about external reset to *9. SPI*
		84	Change of description in *10. Reset*
		88	Deletion of Junction temperature from *11. 1 Absolute Maximum Ratings*
		89	Change of the title to Operation condition in *11. 2*
		105	Correction of the units of DAC ALL ON current consumption 1 and DAC ALL ON current consumption 2 in *11. 4 (3)*

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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