

NP75N04YUK

40 V - 75 A - N-channel Power MOS FET Application: Automotive

R07DS1004EJ0200 Rev.2.00 May 24, 2018

Description

The NP75N04YUK is N-channel MOS Field Effect Transistors designed for high current switching applications.

Features

- Super low on-state resistance $R_{DS(on)} = 3.3 \ m\Omega \ MAX. \ (V_{GS} = 10 \ V, \ I_D = 38 \ A)$
- Non logic level drive type
- Designed for automotive application and AEC-Q101 qualified

Ordering Information

Part No.	Lead Plating	Pac	Package	
NP75N04YUK-E1-AY *1	Pure Sn (Tin)	Tape 2500 p/reel	Taping (E1 type)	8-pin HSON
NP75N04YUK-E2-AY *1			Taping (E2 type)	

Note: *1 Pb-free (This product does not contain Pb in the external electrode)

Absolute Maximum Ratings $(T_A = 25^{\circ}C)$

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V _{GS} = 0 V)	V _{DSS}	40	V
Gate to Source Voltage (V _{DS} = 0 V)	V _{GSS}	±20	V
Drain Current (DC) (T _C = 25°C)	I _{D(DC)}	±75	Α
Drain Current (pulse) *1, 4	I _{D(pulse)}	±300	Α
Total Power Dissipation (T _C = 25°C)	P _{T1}	138	W
Total Power Dissipation (T _A = 25°C) *2	P _{T2}	1.0	W
Channel Temperature	T _{ch}	175	°C
Storage Temperature	T _{stg}	-55 to +175	°C
Repetitive Avalanche Current *3, 4	I _{AR}	35	Α
Repetitive Avalanche Energy *3, 4	E _{AR}	123	mJ

Thermal Resistance

Notes: *1 T_C = 25°C, $P_W \le 10~\mu s$, Duty Cycle $\le 1\%$

*2 Mounted on glass epoxy substrate of 40 mm \times 40 mm \times 1.6 mmt with 4% Copper area (35 μ m)

*3 R_G = 25 Ω , V_{GS} = 20 V \rightarrow 0 V

*4. Not subject of production test. Verified by design/characterization.

Electrical Characteristics (T_A = 25°C)

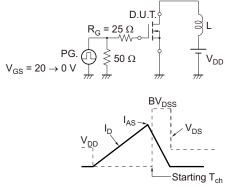
Item	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions	
Zero Gate Voltage Drain Current	I _{DSS}	_	_	1	μΑ	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}$	
Gate Leakage Current	I _{GSS}	_	_	±100	nA	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	
Gate to Source Threshold Voltage	$V_{GS(th)}$	2.0	3.0	4.0	V	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	
Forward Transfer Admittance *1	y _{fs}	31	62	_	S	$V_{DS} = 5 \text{ V}, I_{D} = 38 \text{ A}$	
Drain to Source On-state Resistance *1	R _{DS(on)}	_	2.6	3.3	mΩ	$V_{GS} = 10 \text{ V}, I_D = 38 \text{ A}$	
Input Capacitance *2	C _{iss}	_	3400	5100	pF	V _{DS} = 25 V	
Output Capacitance *2	Coss	_	480	720	pF	$V_{GS} = 0 V$	
Reverse Transfer Capacitance *2	C _{rss}	_	180	330	pF	f = 1 MHz	
Turn-on Delay Time *2	t _{d(on)}	_	24	48	ns	$V_{DD} = 20 \text{ V}, I_D = 38 \text{ A}$	
Rise Time *2	t _r	_	10	25	ns	V _{GS} = 10 V	
Turn-off Delay Time *2	$t_{d(off)}$	_	60	120	ns	$R_G = 0 \Omega$	
Fall Time *2	t _f	_	7	17	ns		
Total Gate Charge *2	Q_{G}	_	58	87	nC	V _{DD} = 32 V	
Gate to Source Charge	Q _{GS}	_	16	_	nC	V _{GS} = 10 V	
Gate to Drain Charge	Q _{GD}	_	15	_	nC	I _D = 75 A	
Body Diode Forward Voltage *1	V _{F(S-D)}	_	0.9	1.5	V	I _F = 75 A, V _{GS} = 0 V	
Reverse Recovery Time	t _{rr}	_	42		ns	I _F = 75 A, V _{GS} = 0 V	
Reverse Recovery Charge	Qrr	_	51	_	nC	di/dt = 100 A/μs	

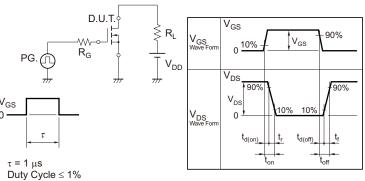
Note: *1 Pulsed test

Note: *2 Not subject of production test. Verified by design/characterization.

TEST CIRCUIT 1 AVALANCHE CAPABILITY

D.(



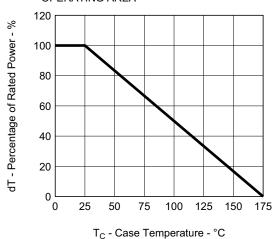


TEST CIRCUIT 2 SWITCHING TIME

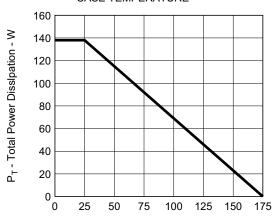
TEST CIRCUIT 3 GATE CHARGE

Typical Characteristics (T_A = 25°C)

DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

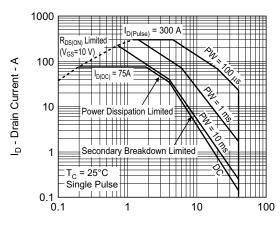


TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



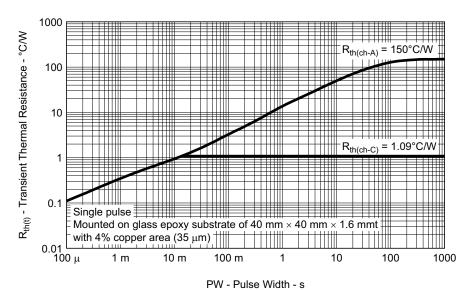
T_C - Case Temperature - °C

FORWARD BIAS SAFE OPERATING AREA



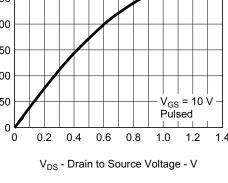
V_{DS} - Drain to Source Voltage - V

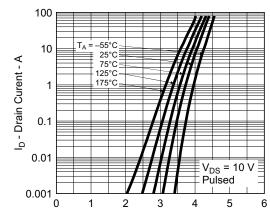
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



V_{GS(th)} - Gate to Source Threshold Voltage - V

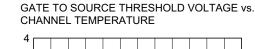
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE 350 300 I_D - Drain Current - A 250 200 150 100 V_{GS} = 10 V 50 Pulsed 0 0.4 0.8 0 0.2 0.6 1.0 1.2 1.4

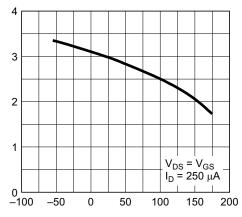




V_{GS} - Gate to Source Voltage - V

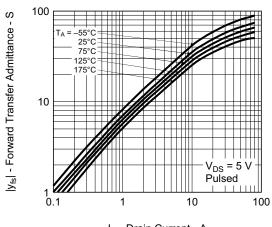
FORWARD TRANSFER CHARACTERISTICS

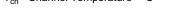


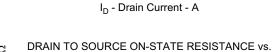


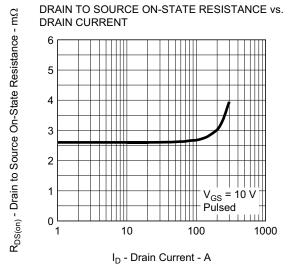


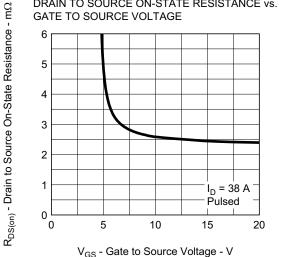
FORWARD TRANSFER ADMITTANCE vs. **DRAIN CURRENT**





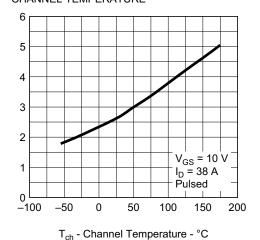




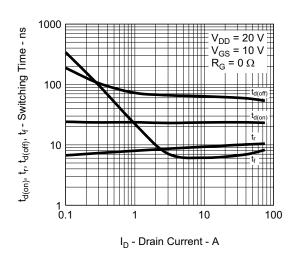


 $R_{DS(on)}$ - Drain to Source On-State Resistance - $m\Omega$

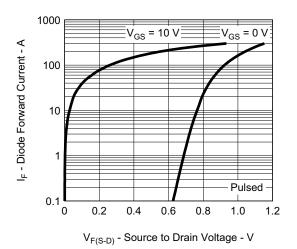
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



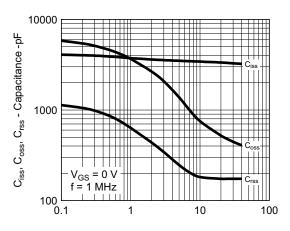
SWITCHING CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

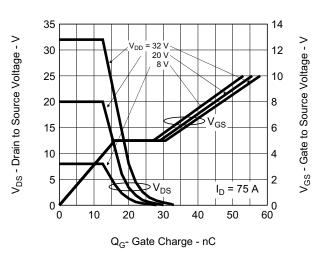


CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

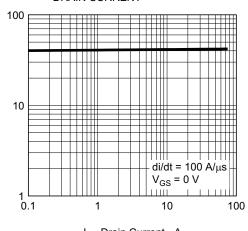


V_{DS} - Drain to Source Voltage - V

DYNAMIC INPUT/OUTPUT CHARACTERISTICS



REVERSE RECOVERY TIME vs. DRAIN CURRENT

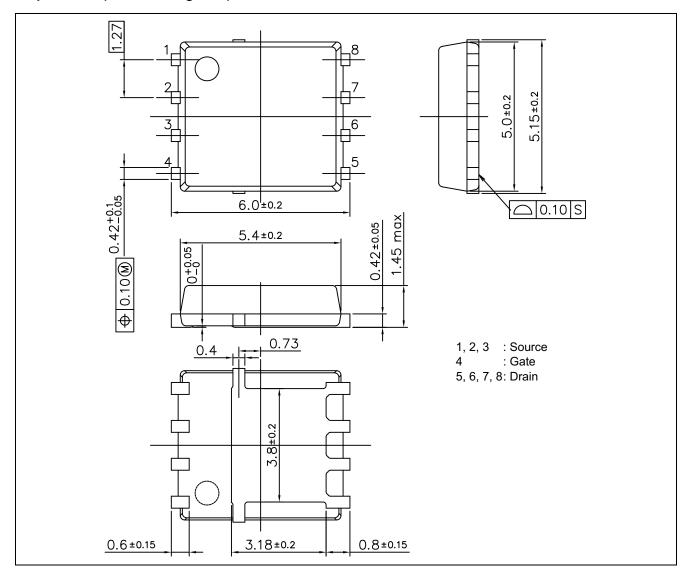


I_F - Drain Current - A

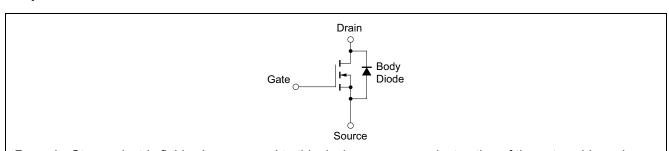
t_{rr} - Reverse Recovery Time - ns

Package Drawing (Unit: mm)

8-pin HSON (Mass: 0.128 g TYP.)



Equivalent Circuit



Remark: Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Revision History

NP75N04YUK Data Sheet

		Description		
Rev.	Date	Page	Summary	
1.00	Feb 08, 2013	_	First Edition Issued	
2.00	May 24 ,2018	1	Note 4 was added	
		2	Note 2 was added	

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