ISL9123

Ultra-Low IQ Buck Regulator with Bypass

The ISL9123 is a highly integrated buck switching regulator that is capable of supplying output voltage down to 0.4V. It features an extremely low quiescent current consumption of 950nA in Regulation mode, 140nA in Forced Bypass mode, and 7nA in Shutdown mode. It provides 80% efficiency at 10µA load and has a peak efficiency of 97%. It supports input voltages from 1.8V to 5.5V.

The ISL9123 has automatic bypass functionality for situations in which the input voltage is close to the output voltage. In addition to the automatic bypass functionality, the Forced Bypass power saving mode can be chosen if voltage regulation is not required. Forced Bypass power saving mode is accessible using the I^2C interface bus.

The ISL9123 is capable of delivering up to 600mA of output current (V_{IN} = 3.6V, V_{OUT} = 1.8V) and provides excellent efficiency due to its adaptive frequency hysteretic control architecture.

The ISL9123 is designed for stand-alone applications and supports a default output voltage at Power-On Reset (POR). After POR, the output voltage can be adjusted in the range of 0.4V to 5.375V by using the I^2C interface bus. Specific default output voltages are available upon request.

The ISL9123 requires only a single EIA 0603 size inductor and two external capacitors. Power supply solution size is minimized by a 1.8mmx1.0mm WLCSP and is also available in 8 Ld plastic DFN.

Related Literature

For a full list of related documents, visit our website:

- ISL9123 device page

Features

- 950nA quiescent current
- 80% efficiency at 10µA load
- 97% peak efficiency
- Input voltage range: 1.8V to 5.5V
- Output voltage range: 0.4V to 5.375V
- Output current: up to 600mA (V_{IN} = 3.6V, V_{OUT} = 1.8V)
- Selectable Forced and Auto Bypass power saving modes
- PFM and PWM modes with seamless transition
- Ultrasonic mode for acoustic noise suppression
- I^2C control and voltage adjustability
- Hysteretic controller
- Small 1.8mmx1.0mm WLCSP and 8 Ld DFN packages

Applications

- Smart watches and wristband devices
- Wireless earphones
- Internet of Things (IoT) devices
- Water, gas, and oil meters
- Portable medical devices
- Hearing aid devices

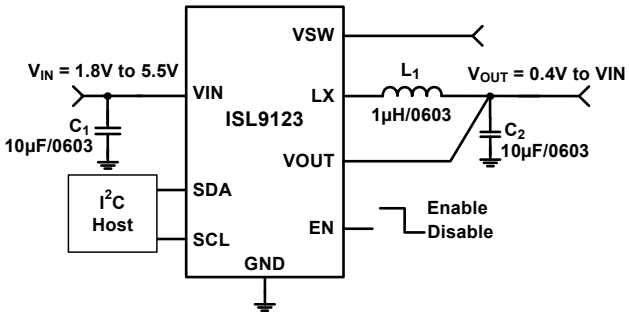

Figure 1. Typical Application

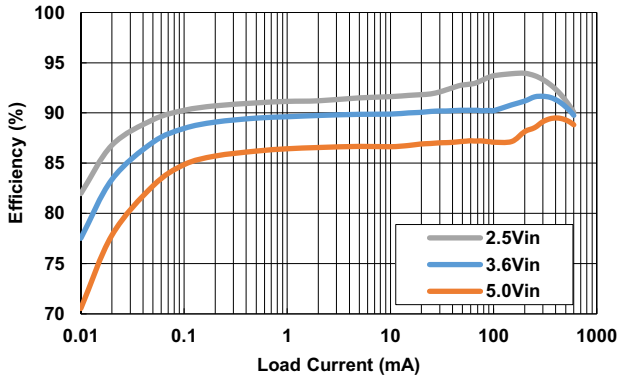

Figure 2. Efficiency vs Load Current: V_{OUT} = 1.8V, T_A = +25°C

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1. Overview

1.1 Block Diagram

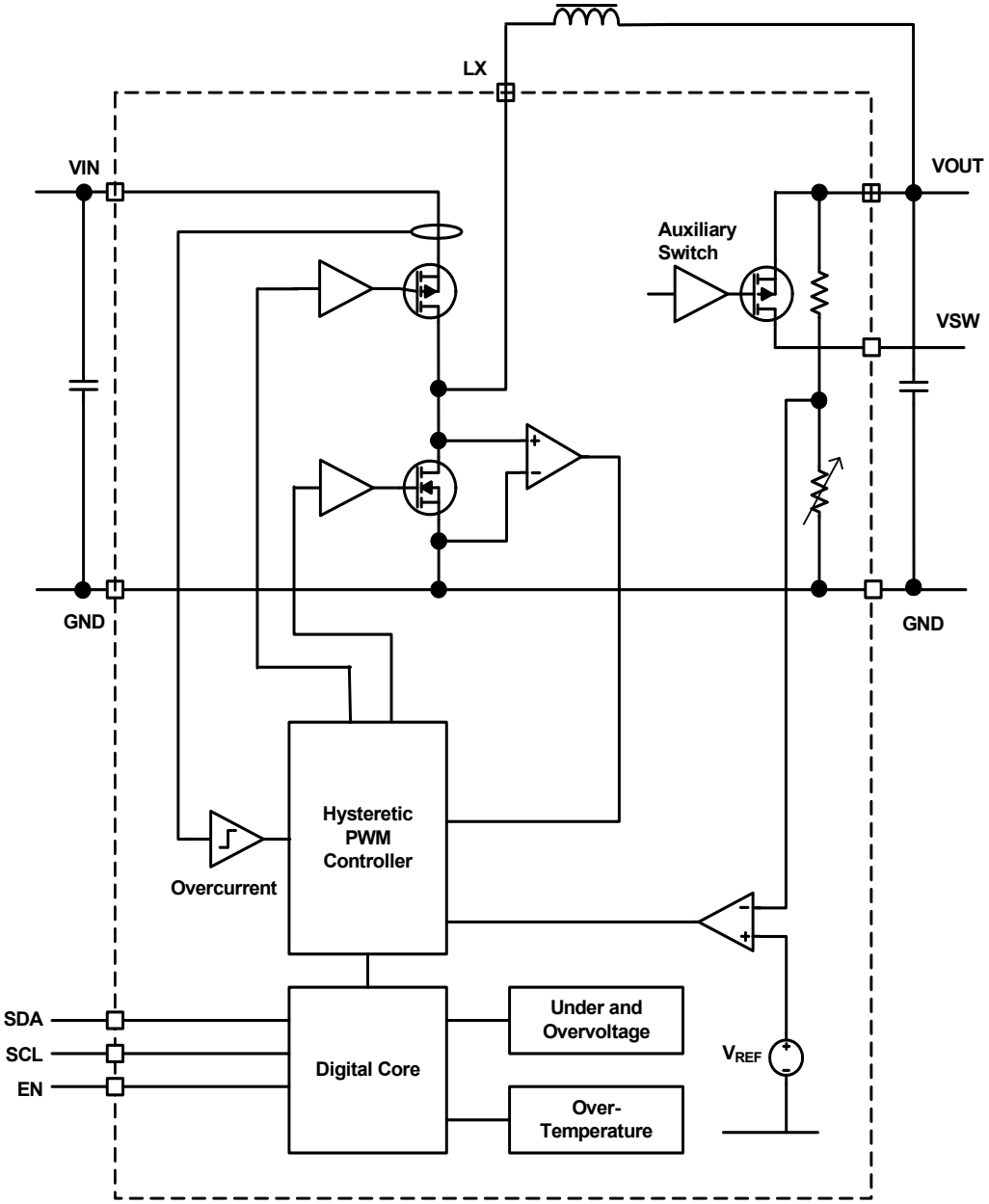


Figure 3. Block Diagram

1.2 Ordering Information

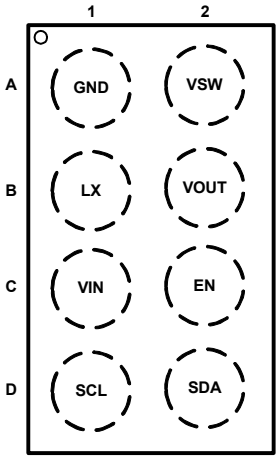
Part Number (Note 4)	Part Marking	Default V_{OUT} (V)	I^2C Address	Temp Range (°C)	Tape and Reel (Units) (Note 1)	Package (RoHS Compliant)	Pkg. Dwg. #
ISL9123IINZ-T (Note 2)	9123	3.0V	0x1C	-40 to +85	3k	8 Bump WLCSP	W2x4.8
ISL9123IICZ-T (Note 2)	C123	1.8V	0x1C	-40 to +85	3k	8 Bump WLCSP	W2x4.8
ISL9123II4Z-T (Note 2)	1234	1.0V	0x1C	-40 to +85	3k	8 Bump WLCSP	W2x4.8
ISL9123II7Z-T (Note 2)	1237	0.7V	0x1C	-40 to +85	3k	8 Bump WLCSP	W2x4.8
ISL9123IRNZ-T (Note 3)	A23	3.0V	0x1C	-40 to +85	6k	8 Ld DFN	L8.2x3
ISL9123IRNZ-T7A (Note 3)	A23	3.0V	0x1C	-40 to +85	250	8 Ld DFN	L8.2x3
ISL9123IRCZ-T (Note 3)	C23	1.8V	0x1C	-40 to +85	6k	8 Ld DFN	L8.2x3
ISL9123IRCZ-T7A (Note 3)	C23	1.8V	0x1C	-40 to +85	250	8 Ld DFN	L8.2x3
ISL9123IRQZ-T (Note 3)	D23	3.3V	0x1C	-40 to +85	6k	8 Ld DFN	L8.2x3
ISL9123IRQZ-T7A (Note 3)	D23	3.3V	0x1C	-40 to +85	250	8 Ld DFN	L8.2x3
ISL9123IIC-EVZ	Evaluation Board for the ISL9123IICZ						
ISL9123IRC-EVZ	Evaluation Board for the ISL9123IRCZ						
ISL9123IIN-EVZ	Evaluation Board for the ISL9123IINZ						
ISL9123IRN-EVZ	Evaluation Board for the ISL9123IRNZ						

Notes:

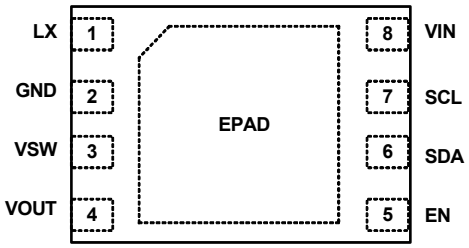
1. See TB347 for details about reel specifications.
2. These Pb-free WLCSP packaged products employ special Pb-free material sets; molding compounds/die attach materials and SnAgCu - e1 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free WLCSP packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
3. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
4. For Moisture Sensitivity Level (MSL), see the ISL9123 device page. For more information about MSL, see TB363.

1.3 Pin Configuration

8 Bump WLCSP
Top View



8 Ld DFN
Top View



1.4 Pin Descriptions

WLCSP Ball Number	DFN Pin Number	Pin Names	Description
A1	2	GND	Ground connection
A2	3	VSW	Auxiliary output
B1	1	LX	Inductor connection
B2	4	VOUT	Buck output
C1	8	VIN	Power supply input
C2	5	EN	Logic input, drive HIGH to enable device. Do not leave floating
D1	7	SCL	I^2C clock input
D2	6	SDA	I^2C data input
	N/A	EPAD	Exposed pad. Must be soldered to PCB GND

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
VIN, VOUT	-0.3	6.5	V
LX	-0.3	6.5	V
All Other Pins	-0.3	6.5	V
ESD Rating	**Value**		**Unit**
Human Body Model (Tested per JS-001-2017)	2		kV
Charged Device Model (Tested per JS-002-2014)	1		kV
Latch-Up (Tested per JESD78E; Class 2, Level A)	100		mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)	θ_{JB} (°C/W)
8 Bump WLCSP Package (Notes 5, 6)	110	-	28
8 Ld 2x3 DFN Package (Notes 5, 7)	55	5.5	-

Notes:

5. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
6. For θ_{JB}, the board temperature is taken on the board near the edge of the package, on a copper trace at the center of one side. See TB379.
7. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature		+125	°C
Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	See TB493		

2.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Ambient Temperature (T_A) Range	-40	+85	°C
Supply Voltage (V_{IN}) Range	1.8	5.5	V
Load Current (I_{OUT}) Range (DC)	0	600	mA

2.4 Analog Specifications

V_{IN} = V_{EN} = 3.6V, V_{OUT} = 1.8V, I^2C pull-up voltage = V_{IN}, L_1 = 1µH, C_1 = 10µF, C_2 = 10µF, T_A = +25°C. **Boldface limits apply across the operating temperature range (-40°C to +85°C) and input voltage range (1.8V to 5.5V) unless specified otherwise.**

Parameter	Symbol	Test Conditions	Min (Note 8)	Typ	Max (Note 8)	Unit
Power Supply						
Input Voltage Range	V_{IN}		**1.8**		**5.5**	V
V_{IN} Undervoltage Lockout Threshold	V_{UVLO}	V_{IN} rising			**1.791**	V
Hysteresis				100		mV
V_{IN} Quiescent Current	I_Q	V_{IN} = 3.6V, I_{OUT} = 0A (Note 9)		950	**1800**	nA
V_{IN} Supply Current, Shutdown	I_{SD}	V_{IN} = 3.6V, EN = GND		7	**450**	nA
V_{IN} Supply Current, Soft Shutdown	I_{SSD}	V_{IN} = 3.6V, shutdown using I^2C register. EN_AND = CONV_CFG[7] = 0		30	**450**	nA
V_{IN} Supply Current, Forced Bypass Mode	I_{BYP}	V_{IN} = 3.6V, I_{OUT} = 0A, averaged > 1ms		140	**850**	nA
Output Voltage Regulation						
Output Voltage Range, Buck Mode (Note 10)	V_{OUT}	V_{IN} > V_{SET}, I_{OUT} = 1mA	**0.4**		**5.375**	V
Output Voltage Accuracy						
ISL9123IICZ, ISL9123IRCZ	V_{OUT_ACC}	V_{IN} = 3.6V, V_{OUT} = 1.8V, I_{OUT} = 0A, forced PWM	-2.5		+2.5	%
		V_{IN} = 3.6V, V_{OUT} = 1.8V, I_{OUT} = 1mA, PFM	-3.6		+3.6	%
ISL9123IINZ, ISL9123IRNZ		V_{IN} = 3.6V, V_{OUT} = 3.0V, I_{OUT} = 0A, forced PWM	-2.0		+2.0	%
		V_{IN} = 3.6V, V_{OUT} = 3.0V, I_{OUT} = 1mA, PFM	-3.6		+3.6	%
ISL9123II4Z		V_{IN} = 3.6V, V_{OUT} = 1.0V, I_{OUT} = 0A, forced PWM	-65		+65	mV
		V_{IN} = 3.6V, V_{OUT} = 1.0V, I_{OUT} = 1mA, PFM	-80		+80	mV
ISL9123IRQZ		V_{IN} = 3.6V, V_{OUT} = 3.3V, I_{OUT} = 0A, forced PWM	-2.0		+2.0	%
		V_{IN} = 3.6V, V_{OUT} = 3.3V, I_{OUT} = 1mA, PFM	-3.6		+3.6	%
Soft-Start and Soft Discharge						
Time to Read OTP	t_{OTP}	Time from when V_{IN} > V_{UVLO} and EN signal asserts until switching starts		125		µs
V_{OUT} Ramp Rate for Soft-Start and During Dynamic Voltage Scaling (applicable only for V_{OUT} ramp-up, not ramp-down)	DVSRATE	Default at POR		3.125		mV/µs
		Programmable using I^2C after POR		6.25 0.78125 1.5625		mV/µs
V_{OUT} Soft Discharge ON-Resistance	r_{DISCHG}	EN < EN_{IL}		125		Ω
Power MOSFET (WLCSP Package)						
P-Channel MOSFET ON-Resistance	r_{DSON_P}	V_{IN} = 3.6V, V_{OUT} = 3.6V	**50**	95	**140**	mΩ
N-Channel MOSFET ON-Resistance	r_{DSON_N}	V_{IN} = 3.6V, V_{OUT} = 3.6V	**50**	100	**140**	mΩ
Auxiliary Switched Output MOSFET ON-Resistance	r_{DSON_VAUX}	V_{IN} = 3.6V, V_{OUT} = 3.6V		55	**70**	mΩ
Power MOSFET (DFN Package)						
P-Channel MOSFET ON-Resistance	r_{DSON_P}	V_{IN} = 3.6V, V_{OUT} = 3.6V		150		mΩ
N-Channel MOSFET ON-Resistance	r_{DSON_N}	V_{IN} = 3.6V, V_{OUT} = 3.6V		150		mΩ
Auxiliary Switched Output MOSFET ON-Resistance	r_{DSON_VAUX}	V_{IN} = 3.6V, V_{OUT} = 3.6V		100		mΩ

V_{IN} = V_{EN} = 3.6V, V_{OUT} = 1.8V, I^2C pull-up voltage = V_{IN}, L_1 = 1µH, C_1 = 10µF, C_2 = 10µF, T_A = +25°C. **Boldface limits apply across the operating temperature range (-40°C to +85°C) and input voltage range (1.8V to 5.5V) unless specified otherwise. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 8)	Typ	Max (Note 8)	Unit
Bypass Mode						
Auto Bypass Thresholds	V_{IN_BYP}	Auto bypass exit threshold - V_{IN} offset above regulated output voltage V_{OUT}. I_{OUT} = 10mA		30		mV
		Auto bypass entry threshold - V_{IN} offset above regulated output voltage V_{OUT}. I_{OUT} = 10mA		20		mV
Inductor Peak Current Limit						
Peak Current Limit	I_{LIM}	2.5V < V_{IN} < 5.5V		1.4		A
		1.8V < V_{IN} < 2.5V		1.2		A
Output Current						
Maximum Load Current	I_{OUT_MAX}	2.5V < V_{IN} < 5.5V		600		mA
Maximum Load Current at Low V_{IN}	I_{OUT_DERATE}	1.8V < V_{IN} < 2.5V		300		mA
Efficiency						
Efficiency		I_{OUT} = 50mA, V_{IN} = 3.7V, V_{OUT} = 3.3V		96		%
		I_{OUT} = 10µA, V_{IN} = 3.7V, V_{OUT} = 3.3V		86		%
		I_{OUT} = 50mA, V_{IN} = 3.6V, V_{OUT} = 1.8V		91		%
		I_{OUT} = 10µA, V_{IN} = 3.6V, V_{OUT} = 1.8V		78		%
Switching Frequency						
Switching Frequency	f_{SW}	CCM (with frequency control)		2.5		MHz
		DCM, Ultrasonic		30		kHz
Hiccup Mode						
Hiccup Time	t_{FLT_WAIT}	Time from shutdown to restart		100		ms
Thermal Protection						
Thermal Shutdown Threshold	T_{SD}	Rising temperature		140		°C
Thermal Shutdown Hysteresis	T_{SD_HYS}			25		°C
Logic Levels						
Input Leakage	I_{LEAK}	EN pin		9	**300**	nA
		SCL pin		8	**300**	nA
		SDA pin		8	**300**	nA
EN Input HIGH Voltage	EN_{IH}	V_{IN} = 3.6V	**1.6**			V
EN Input LOW Voltage	EN_{IL}				**0.36**	V
SCL/SDA Input HIGH Voltage	SCL/SDA_{IH}		**1.45**			V
SCL/SDA Input LOW Voltage	SCL/SDA_{IL}				**0.36**	V

Notes:

8. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits are established by characterization and are not production tested.
9. Quiescent current measurements are taken when the device is not switching.
10. Minimum load of 300nA is needed to maintain V_{OUT}, for VSET less than 1.1V.

2.5 I^2C Interface Timing Specifications

Applicable to SCL and SDA in the Fast mode I^2C operation, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min (Note 11)	Typ	Max (Note 11)	Unit
I^2C Frequency Capability	f_{I2C}			3.4		MHz
Pulse Width Suppression Time at SDA and SCL Inputs	t_{SP}	Any pulse narrower than the maximum specification is suppressed			50	ns
Data Valid Time	$t_{VD;DAT}$	Time from SCL falling edge crossing SCL_{IL} to SDA exiting the SDA_{IL} to SDA_{IH} window			900	ns
Data Valid Acknowledge Time	$t_{VD;ACK}$	Time from SCL falling edge crossing SCL_{IL} to SDA exiting the SDA_{IL} to SDA_{IH} window, during acknowledgment			900	ns
Bus Free Time Between a STOP and START Condition	t_{BUF}	Time from SDA crossing SDA_{IH} at STOP to SDA crossing SDA_{IH} at the following START	1300			ns
SCL Low Time	t_{LOW}	Measured at the SCL_{IL} crossing	1300			ns
SCL High Time	t_{HIGH}	Measured at the SCL_{IH} crossing	600			ns
START Condition Setup Time	$t_{SU;STA}$	Time from SCL rising edge crossing SCL_{IH} to SDA falling edge crossing SDA_{IH}	600			ns
START Condition Hold Time	$t_{HD;STA}$	Time from SDA falling edge crossing SDA_{IL} to SCL falling edge crossing SCL_{IH}	600			ns
Data Set-Up Time	$t_{SU;DAT}$	Time from SDA exiting the SDA_{IL} to SDA_{IH} window to SCL rising edge crossing SCL_{IL}	100			ns
Data Hold Time	$t_{HD;DAT}$	Time from SCL falling edge crossing SCL_{IL} to SDA entering the SDA_{IL} to SDA_{IH} window	50			ns
STOP Condition Set-Up Time	$t_{SU;STO}$	Time from SCL rising edge crossing SCL_{IH} to SDA rising edge crossing SDA_{IL}	600			ns
SCL/SDA Capacitive Loading	C_b	Capacitive load for each bus line			400	pF

Note:
11. Limits established by design and are not production tested.

3. Typical Performance Curves

Unless otherwise noted, operating conditions are: V_{IN} = VEN = 3.6V, V_{OUT} = 1.8V, I^2C pull-up voltage = V_{IN}, L_1 = 1µH, C_1 = 10µF, C_2 = 10µF, T_A = +25°C

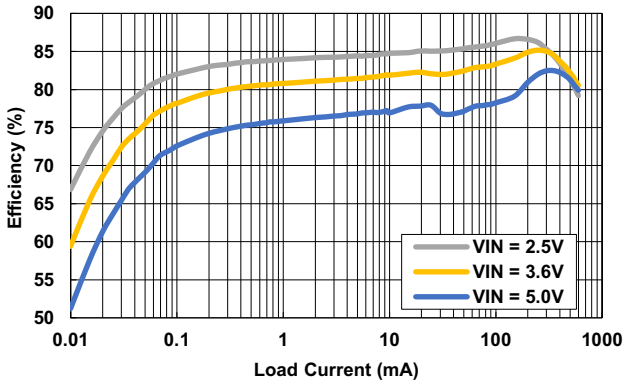


Figure 4. Efficiency vs Load Current: V_{OUT} = 0.8V

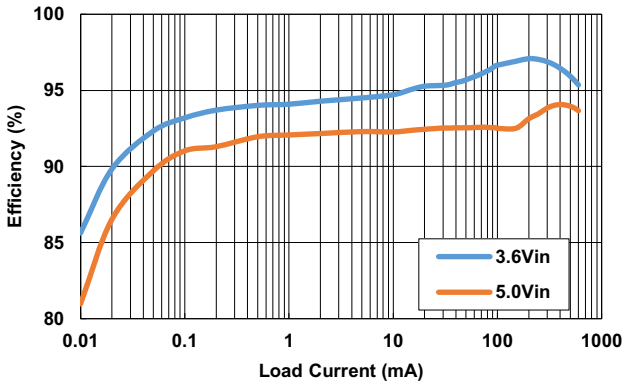


Figure 5. Efficiency vs Load Current: V_{OUT} = 3.3V

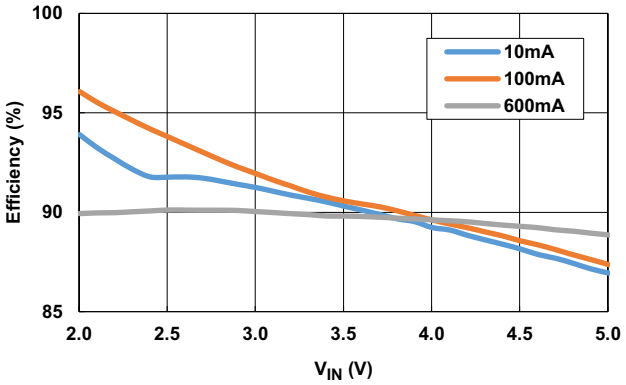


Figure 6. Efficiency vs Input Voltage: V_{OUT} = 1.8V

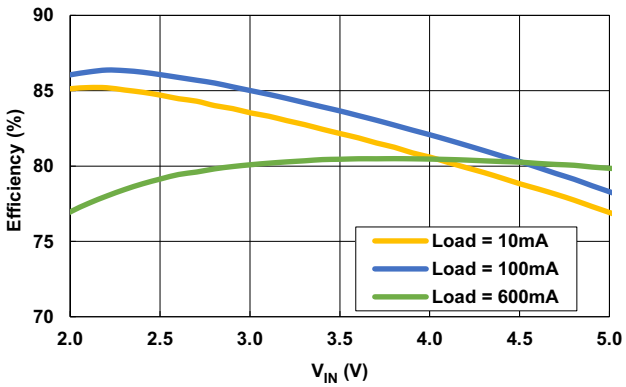


Figure 7. Efficiency vs Input Voltage: V_{OUT} = 0.8V

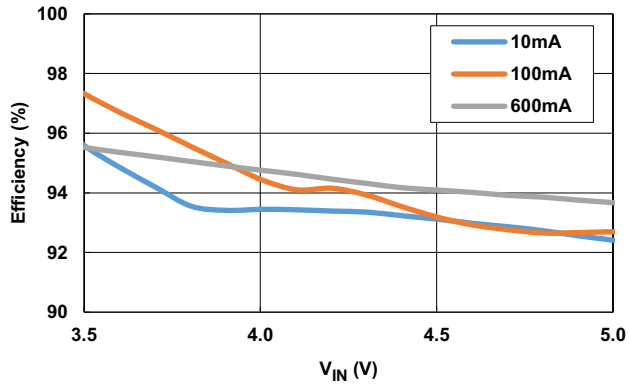


Figure 8. Efficiency vs Input Voltage: V_{OUT} = 3.3V

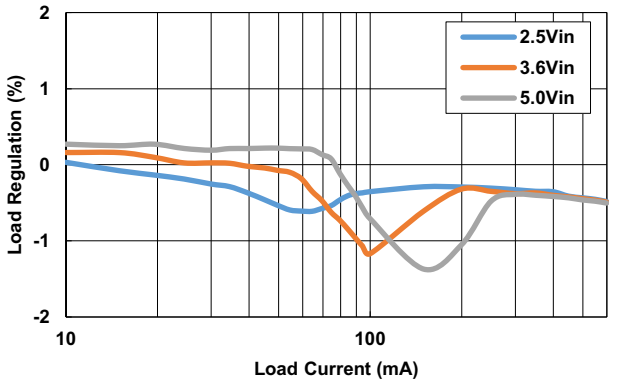


Figure 9. Output Voltage Accuracy vs Load Current: V_{OUT} = 1.8V

Unless otherwise noted, operating conditions are: V_{IN} = VEN = 3.6V, V_{OUT} = 1.8V, I^2C pull-up voltage = V_{IN}, L_1 = 1µH, C_1 = 10µF, C_2 = 10µF, T_A = +25°C **(Continued)**

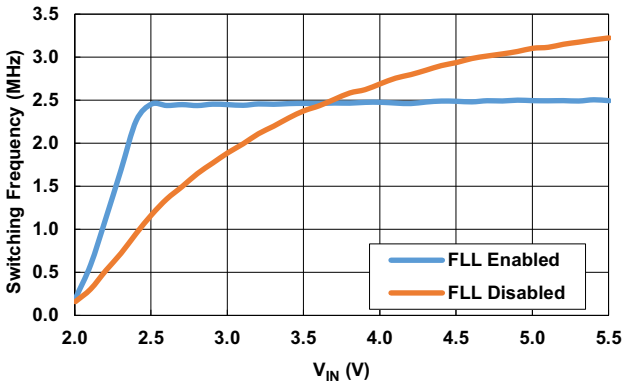


Figure 10. Switching Frequency vs Input Voltage: Load = 600mA, V_{OUT} = 1.8V

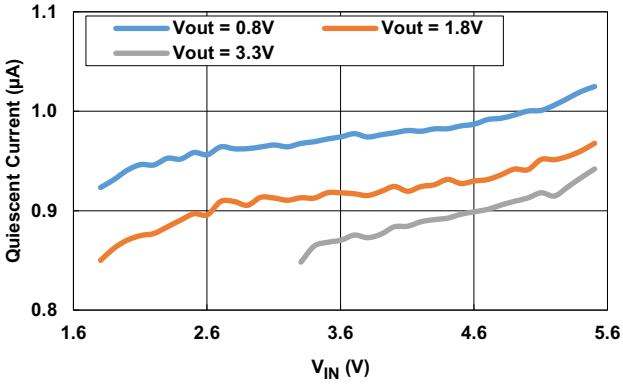


Figure 11. Quiescent Current vs Input Voltage

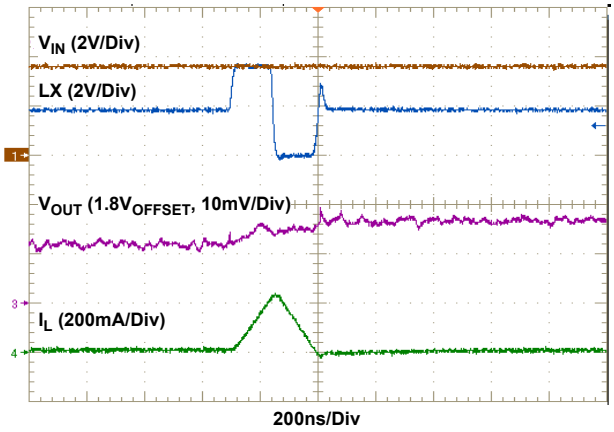


Figure 12. Steady-State Operation in PFM: V_{IN} = 3.6V, V_{OUT} = 1.8V, No Load

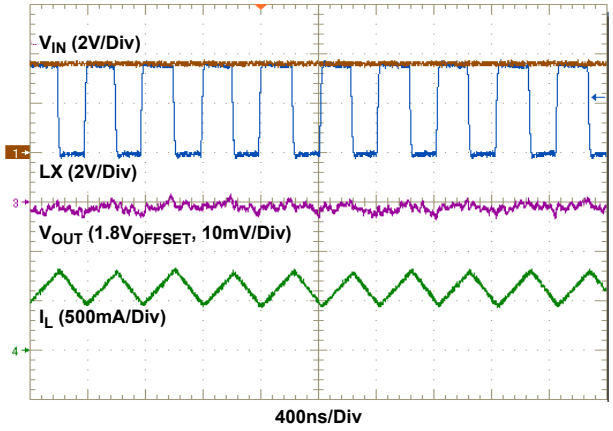


Figure 13. Steady-State Operation in PWM: V_{IN} = 3.6V, V_{OUT} = 1.8V, Load = 600mA

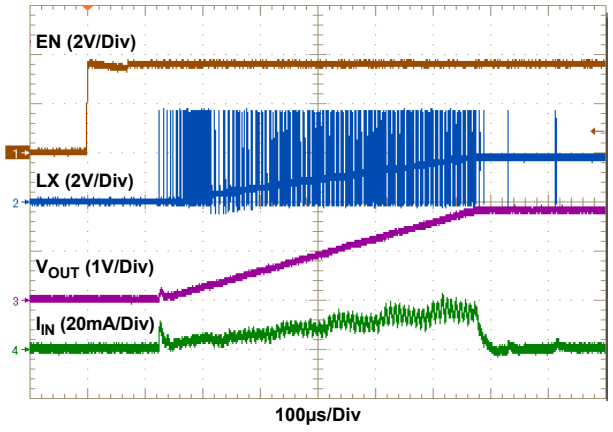


Figure 14. Soft-Start: V_{IN} = 3.6V, V_{SET} = 1.8V, No Load

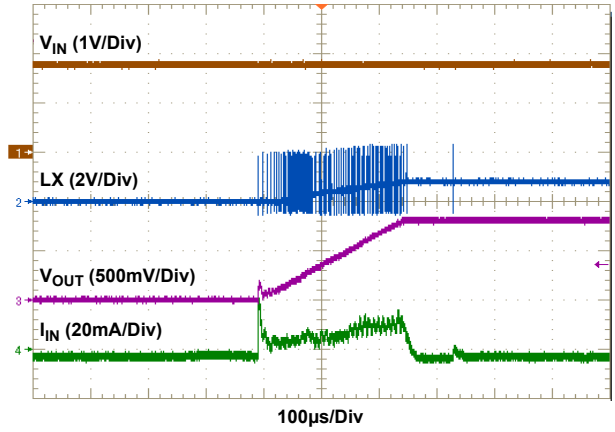


Figure 15. Soft-Start: V_{IN} = 1.8V, V_{SET} = 0.8V, No Load

Unless otherwise noted, operating conditions are: V_{IN} = VEN = 3.6V, V_{OUT} = 1.8V, I^2C pull-up voltage = V_{IN}, L_1 = 1µH, C_1 = 10µF, C_2 = 10µF, T_A = +25°C **(Continued)**

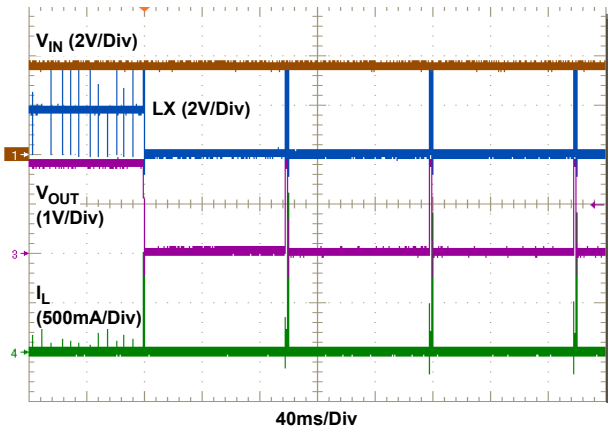


Figure 16. Output Short-Circuit Behavior (Hiccup Mode)

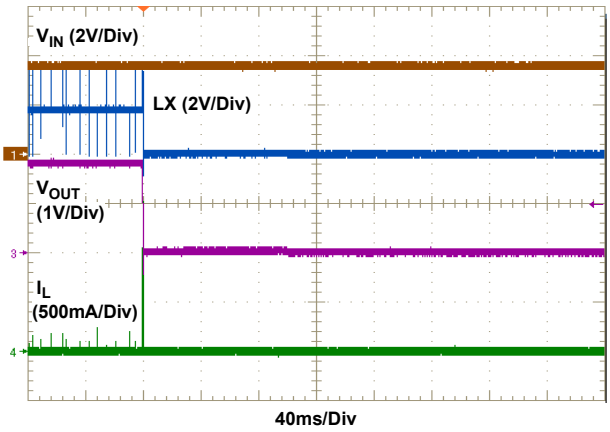


Figure 17. Output Short-Circuit Behavior (Shutdown Mode)

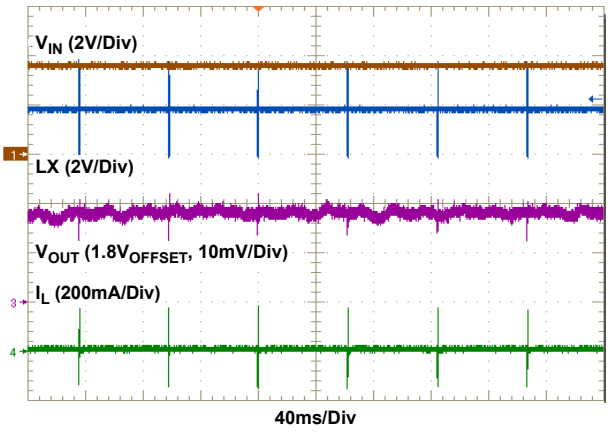


Figure 18. Steady-State Operation in Ultrasonic Mode: V_{IN} = 3.6V, V_{OUT} = 1.8V, No Load

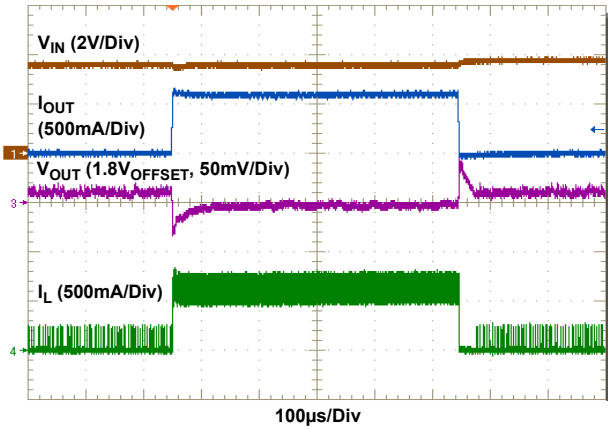


Figure 19. Load Transient: V_{IN} = 3.6V, V_{OUT} = 1.8V, Load = 0.01A to 0.60A, Slew Rate = 1A/µs, Type II Error Amplifier

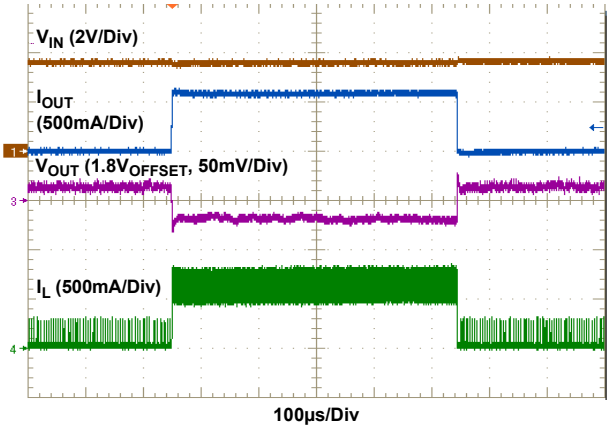


Figure 20. Load Transient: V_{IN} = 3.6V, V_{OUT} = 1.8V, Load = 0.01A to 0.60A, Slew Rate = 1A/µs, Type I Error Amplifier

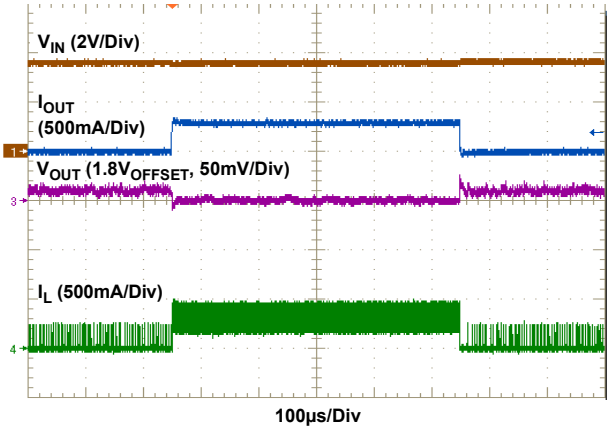


Figure 21. Load Transient: V_{IN} = 3.6V, V_{OUT} = 1.8V, Load = 0.01A to 0.30A, Slew Rate = 1A/µs, Type II Error Amplifier

Unless otherwise noted, operating conditions are: V_{IN} = VEN = 3.6V, V_{OUT} = 1.8V, I^2C pull-up voltage = V_{IN}, L_1 = 1µH, C_1 = 10µF, C_2 = 10µF, T_A = +25°C **(Continued)**

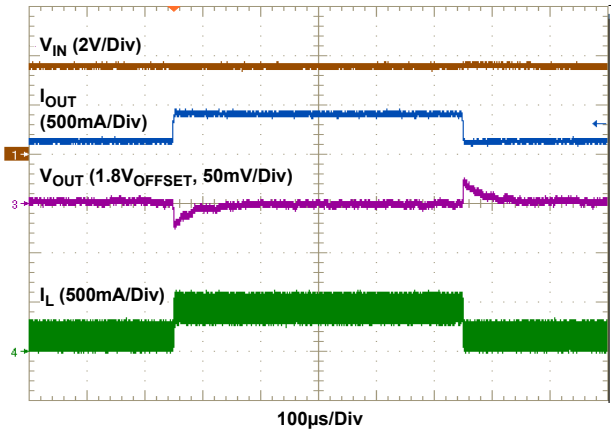


Figure 22. Load Transient: V_{IN} = 3.6V, V_{OUT} = 1.8V, Load = 0.15A to 0.45A, Slew Rate = 1A/µs, Type II Error Amplifier

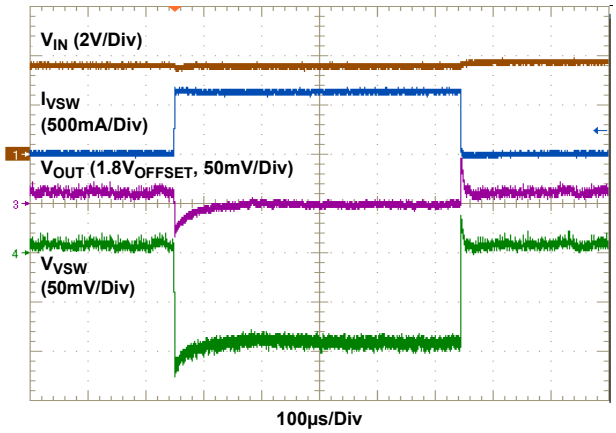


Figure 23. Load Transient: V_{IN} = 3.6V, V_{OUT} = 1.8V, Load at VSW = 0.01A to 0.60A, Slew Rate = 1A/µs, Type II Error Amplifier

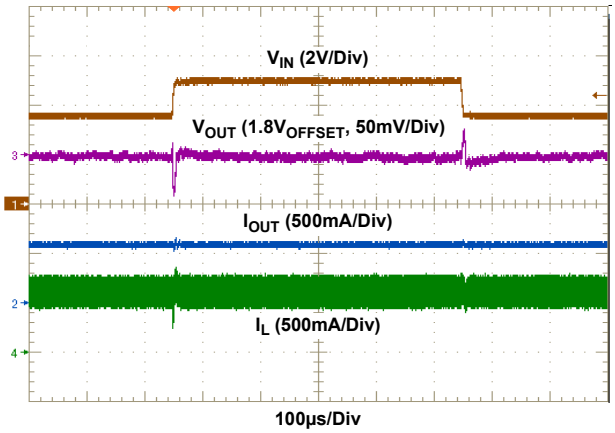


Figure 24. Line Transient: V_{IN} = 3.6V to 5.0V, Slew Rate = 0.5V/µs, V_{OUT} = 1.8V, Load = 600mA, Type II Error Amplifier

4. Functional Description

The ISL9123 implements a complete buck switching regulator, with a PWM controller, internal switches, references, protection circuitry, and control inputs. For more information see the "Block Diagram" on page 3.

4.1 Enable Input

The device is enabled by asserting the EN pin HIGH. Driving the EN LOW invokes Power-Down mode, in which most internal device functions are disabled.

4.2 Soft Discharge

Whenever the converter is disabled over I^2C, an internal discharge resistor between VOUT and GND can be activated to slowly discharge the output capacitor. This internal discharge resistor has a typical resistance of 125Ω. The soft discharge function is accessed using I^2C while keeping the EN pin HIGH. Using the CONV_CFG register, set the DISCH bit to 1, and disable the IC by setting the EN_AND bit to 0 (see Table 5 on page 20 for details). When the device is disabled by setting EN pin low, while the input voltage is still present, the internal discharge resistor is present between VOUT and GND.

4.3 Startup

The power-on sequence starts when the input voltage rises above the undervoltage lockout threshold and EN is asserted HIGH. First, the IC is initialized and its One-Time Programmable (OTP) memory is read. After the OTP has been read and the controller knows the target output voltage and ramp rate, soft-start begins and the output voltage rises at the programmed ramp rate until it reaches the target output voltage.

4.4 Overcurrent/Short-Circuit Protection

The ISL9123 provides overcurrent protection by monitoring the inductor current. When the peak inductor current hits its current limit, the IC enters Hiccup mode, Shutdown mode, or Current Limit mode according to the setting of the OC_FAULT_MODE bits in the INT_FLAG_MASK register. During Hiccup mode, the IC shuts down for 100ms and then tries to restart.

4.5 Thermal Shutdown

The ISL9123 thermal shutdown feature protects the device from damage due to overheating. An integrated temperature sensor circuit monitors the internal IC temperature. When the temperature exceeds T_{SD}, the device stops switching and waits for the temperature to fall. When the temperature falls by T_{SDHYS}, the controller first goes through the soft-start phase and then starts regulating at the target output voltage as defined by the I^2C register value.

4.6 Buck Conversion Topology

The ISL9123 operates in either Bypass or Buck mode. When operating in conditions in which V_{IN} is close to V_{OUT}, the ISL9123 automatically switches from Buck mode to Bypass mode. For other conditions, the device performs Buck regulation.

Figure 25 shows a simplified diagram of the internal switches and external inductor. Switch D is used for the auxiliary switched output connection.

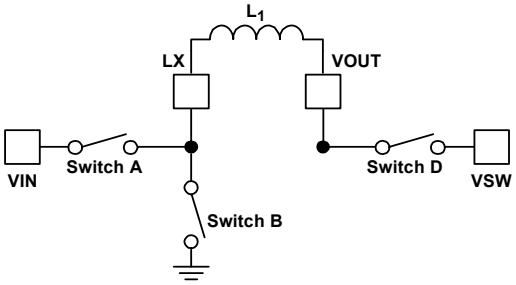


Figure 25. Buck Topology

4.7 PWM Operation

In Buck PWM mode, Switches A and B operate as a synchronous buck converter. Switch D can be controlled by using the AUX_SW bit in the INTFLG_MASK register.

4.8 PFM Operation

During PFM operation in Buck mode, Switches A and B operate in Discontinuous mode. The ISL9123 closes Switch A to ramp up the current in the inductor and the output voltage. When the inductor current reaches a certain threshold, the device turns off Switch A, then turns on Switch B. With Switch B closed, output voltage decreases as the inductor current ramps down.

In some operating conditions, there are multiple PFM pulses to charge up the output capacitor. These pulses continue until V_{OUT} has achieved the upper threshold of the PFM hysteretic controller. Switching then stops and remains stopped until V_{OUT} decays to the lower threshold of the hysteretic PFM controller.

4.9 Operation with V_{IN} Close to V_{OUT}

When the output voltage is close to the input voltage, the ISL9123 rapidly and smoothly switches between Buck mode and Bypass mode as needed to maintain the regulated output voltage. This behavior provides excellent efficiency and very low output voltage ripple.

4.10 Forced Operating Modes

Forced operating modes include Ultrasonic mode, Forced PWM mode, and Forced Bypass mode. Forced operating modes are selected using the FMODE bits in the CONV_CFG register (see Table 5 on page 20 for details).

The power-up default mode is Normal operation with automatic mode transitions to optimize efficiency. Ultrasonic mode can be selected to keep the DCM switching frequency above the audio range. If V_{IN} approaches V_{OUT}, switching instances reduce and smoothly transition from Switching to Bypass mode. Forced PWM mode can be selected to minimize frequency variation. Forced Bypass mode can be selected to minimize power losses when output voltage regulation is not required.

When the device enters Bypass mode, the high-side FET is turned ON, providing a direct path from the input to output through the high-side FET and the inductor. In Bypass mode, all other blocks, except POR and I^2C, are turned off to minimize quiescent current consumption. There should be at least 1ms of time delay between entry into or exit out of Bypass mode, when transitioning between Bypass mode and Buck mode. **Note:** There is no overcurrent protection in Bypass mode.

4.11 I^2C Serial Interface

The ISL9123 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL9123 operates as a slave device in all applications.

The IC supports the following data transfer rates and modes as defined in the I^2C specification:

- Up to 100kbit/s in Standard mode
- Up to 400kbit/s in Fast mode
- Up to 1Mbit/s in Fast-Mode Plus
- Up to 3.4Mbit/s in the High-Speed mode

All communication over the I^2C interface is conducted by sending the MSB of each byte of data first.

4.11.1 Protocol Conventions

Data states on the SDA line can change only during SCL LOW periods. The SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 26). At power-up of the ISL9123, the SDA pin is in input mode.

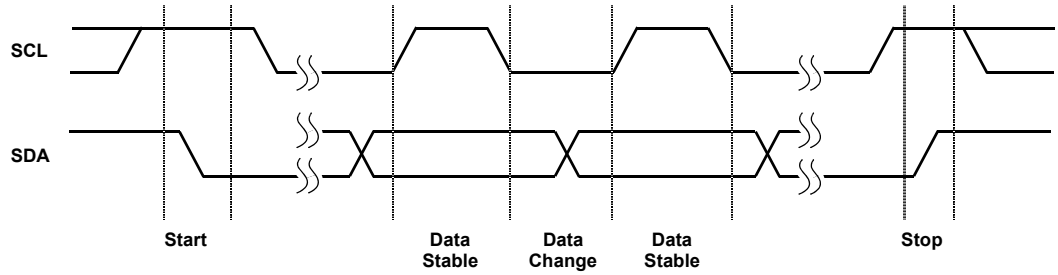


Figure 26. Valid Data Changes, Start, and Stop Conditions

All I^2C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL9123 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 26). A START condition is ignored during the power-up sequence and when the EN input is low.

All I^2C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 26). A STOP condition at the end of a write operation initiates the reconfiguration for the voltage feedback loop of the ISL9123 as necessary to provide the programmed output voltage.

An acknowledge (ACK) is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (see Figure 27).

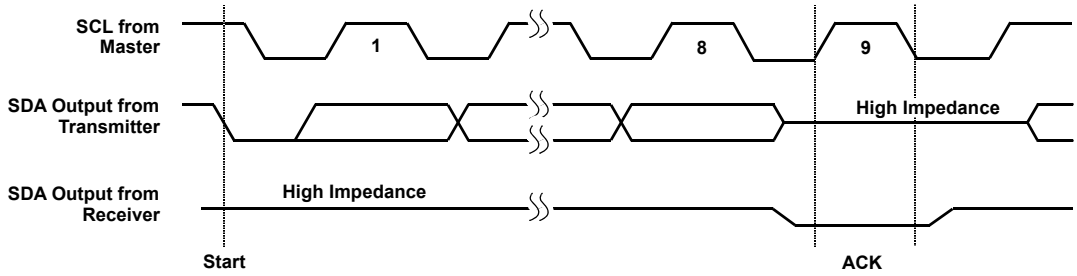


Figure 27. Acknowledge Response from Receiver

The ISL9123 responds with an ACK after recognition of a START condition followed by a valid 7-bit slave address, and once again after successful receipt of a register address byte. The ISL9123 also responds with an ACK after receiving a data byte of a write operation. The master must respond with an ACK after receiving a data byte of a read operation.

As a default option, the 7-bit slave address is set in trim to 0x1C. The 7-bit address is followed by a Read/$\overline{\text{Write}}$ bit whose value is “1” for a Read operation, and “0” for a Write operation (see Table 1).

Table 1. 7-Bit Address Format

0	0	1	1	1	0	0	R/$\overline{\text{W}}$
(MSB)							(LSB)

4.11.2 Write Operation

Write operations are shown in Figure 28. A write operation requires a START condition, followed by a valid 7-bit slave address with the R/$\overline{W}$ bit set to 0, a valid register address byte, one or more data bytes, and a STOP condition. After each of the bytes, the ISL9123 responds with an ACK. After each data byte is acknowledged, the ISL9123 increments its register address to support block writes. The master sends a STOP to complete the command.

STOP conditions that terminate write operations must be sent by the master after sending at least one full data byte and its associated ACK signal. If a STOP condition is issued in the middle of a data byte, or before one full data byte + ACK is sent, the ISL9123 ignores the command, and does not change the output voltage or other settings.

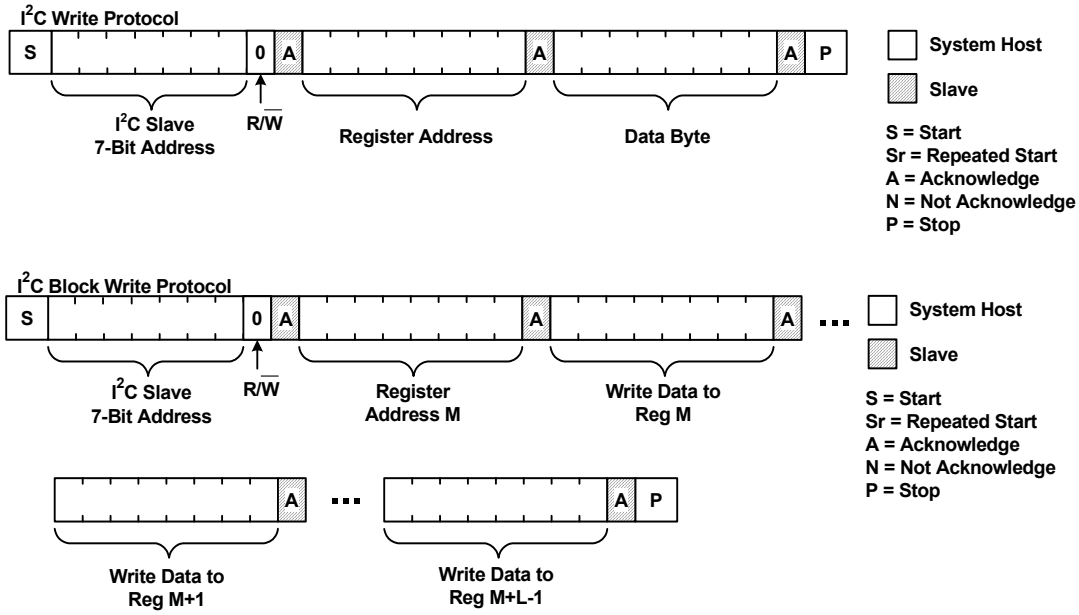


Figure 28. I2C Register Write Protocols

4.11.3 Read Operation

Read operations are shown in Figure 29 on page 18. They consist of four or more bytes. The host generates a START condition, then transmits the 7-bit slave address with the R/$\overline{W}$ bit set to 0. The ISL9123 responds with an ACK. The host then transmits the register address byte, and the ISL9123 responds with another ACK.

The host then generates a repeat START condition and transmits the 7-bit slave address with the R/$\overline{W}$ bit set to 1. The ISL9123 responds with an ACK, indicating it is ready to begin providing the requested data.

The ISL9123 then transmits the data byte by asserting control of the SDA pin while the host generates clock pulses on the SCL pin. After each data byte is complete, the host generates an ACK condition, and the ISL9123 increments its register address to support block reads. After the last data byte is complete and acknowledged, the host sends a STOP condition. This completes the I2C Read operation.

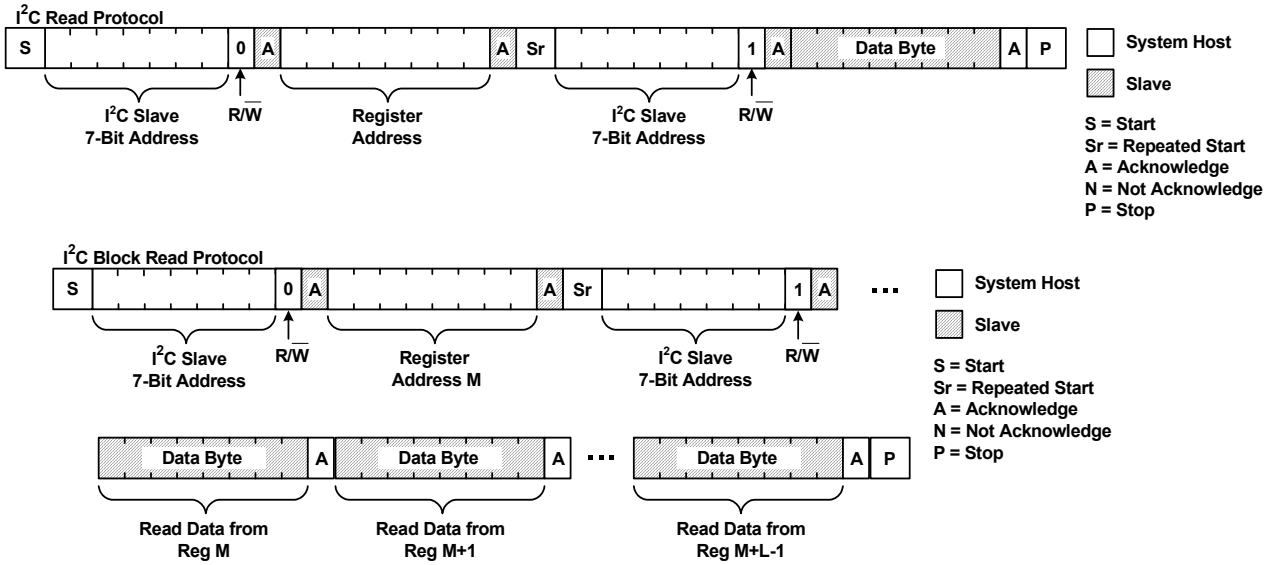


Figure 29. I²C Register Read Protocols

4.11.4 High-Speed Mode

Entering High-Speed mode (HS-mode) requires an additional 8-bit master code (0b00001xxx), NACK, and repeated START be inserted after the initial START condition. See the I²C specification for details.

5. Register Descriptions

The ISL9123 has five I²C accessible control registers whose functions are described in Tables 2 through 6. These registers can be accessed any time the ISL9123 is enabled. Attempts to communicate with the ISL9123 through its I²C interface when disabled (EN = Low), are not supported.

5.1 RO_REG1

The RO_REG1 register contains the hardware identification bits as described in Table 2.

Table 2. Register Address 0x02: RO_REG1

Bit	Name	Type	Reset	Description
7:6	FAMILY_ID[1:0]	R	0x0	Chip family identifier 0x0 = ISL9122 stand-alone converter family
5:3	HW_REV[2:0]	R	0x3	Chip revision level 0x3 = Hardware revision D
2:0	RAIL_VAR[2:0]	R	0x4	Converter variant identifier 0x4 = Buck (ISL9123)

5.2 INTFLG_REG

The INTFLG_REG register contains fault flags. Each bit represents a different type of fault as described in Table 3. A 0 indicates no fault, and a 1 indicates a fault. Each bit is set by a fault event and is cleared when read.

Table 3. Register Address 0x03: INTFLG_REG

Bit	Name	Type	Reset	Description
3	INT3	R	0x0	Voltage setting under range
2	INT2	R	0x0	Voltage setting over range
1	INT1	R	0x0	Over-temperature
0	INT0	R	0x0	Overcurrent

5.3 VSET

The VSET register contains the output voltage setting in 25mV steps as shown in Equation 1. The VSET can be changed after the IC is enabled and operating. When the output voltage is changed, it ramps at the rate set in the DVSRATE bits of CONV_CFG register.

(EQ. 1) $$V_{OUT} = VSET \times 0.025V$$

The output voltage range is digitally limited to be between the minimum and maximum values shown in Table 4. Setting values above or below the limits results in the output voltage ramping to the limit and the appropriate overvoltage or undervoltage interrupt flag in INTFLG_REG being set.

Table 4. Register Address 0x11: VSET

Bit	Name	Type	Reset	Description
7:0	VSET[7:0]	R/W		Output voltage setting Minimum limit = 0.4V Maximum limit = 5.375V

5.4 CONV_CFG

The CONV_CFG register settings are described in Table 5.

Table 5. Register Address 0x12: CONV_CFG

Bit	Name	Type	Reset	Description
7	EN_AND	R/W	0x1	Enable bit. ANDed with the enable input 0x0 = EN pin going high wakes up the I^2C, but does not start the converter. The converter is started by writing 1 to this bit using I^2C while the EN pin is high 0x1 = EN pin going high wakes up the I^2C and starts the converter **Note:** EN pin low always disables the converter and I^2C
6	DISCH	R/W	0x0	0x0 = No discharge resistor present when converter is disabled over I^2C 0x1 = Discharge resistor present when converter is disabled over I^2C
5:4	DVSRATE[1:0]	R/W	0x0	Dynamic Voltage Scaling slew rate applied when the output voltage setting is changed. 0x0 = 3.125mV/µs 0x1 = 6.25mV/µs 0x2 = 0.78125mV/µs 0x3 = 1.5625mV/µs
3:2	FMODE	R/W	0x0	Forced operating modes 0x0 = Normal operation with automatic mode transitions 0x1 = Ultrasonic mode with enforced minimum PFM frequency 0x2 = Forced PWM mode with no PFM operation 0x3 = Forced bypass. Disables switching. If the Forced Bypass mode is selected and the part is disabled over I^2C (CONV_CFG[7] = EN_AND = 0x0), the converter remains in Forced Bypass
1	CONV_RSVD	R/W	0x0	Reserved
0	TYPE1	R/W	0x1	0x0 = Type I error amplifier for best transient response with voltage positioning 0x1 = Type II error amplifier for best steady state voltage accuracy. **DO NOT USE** Type II error amplifier if overcurrent fault handling is disabled (INTFLG_MASK[7] = OC_FAULT_MODE = 0x2 or 0x3)

5.5 INTFLG_MASK

The INTFLG_MASK register settings are described in Table 6.

Table 6. Register Address 0x13: INTFLG_MASK

Bit	Name	Type	Reset	Description
7:6	OC_FAULT_MODE	R/W	0x0	Overcurrent fault handling modes 0x0 = Hiccup mode with 100ms wait 0x1 = Shutdown mode. Requires restart over I^2C or EN pin 0x2 = Current limit with no fault action taken. USE ONLY with Type I error amplifier (CONV_CFG[0] = TYPE1 = 0x0) 0x3 = Reserved. USE ONLY with Type I error amplifier (CONV_CFG[0] = TYPE1 = 0x0)
5	AUX_SW	R/W	0x0	Auxiliary switched output control 0x0 = VSW pin disconnected 0x1 = VSW pin connected to the VOUT pin by power switch
4	EN_OR	R/W	0x0	Enable override bit for I^2C control of converter. Implements push-button ON operation; the button pulls EN high and the part starts. If EN_OR is set from OTP or over I^2C, the part remains enabled when the button is released. 0x0 = Controlled by the EN pin 0x1 = Held in enable state - EN pin is ignored

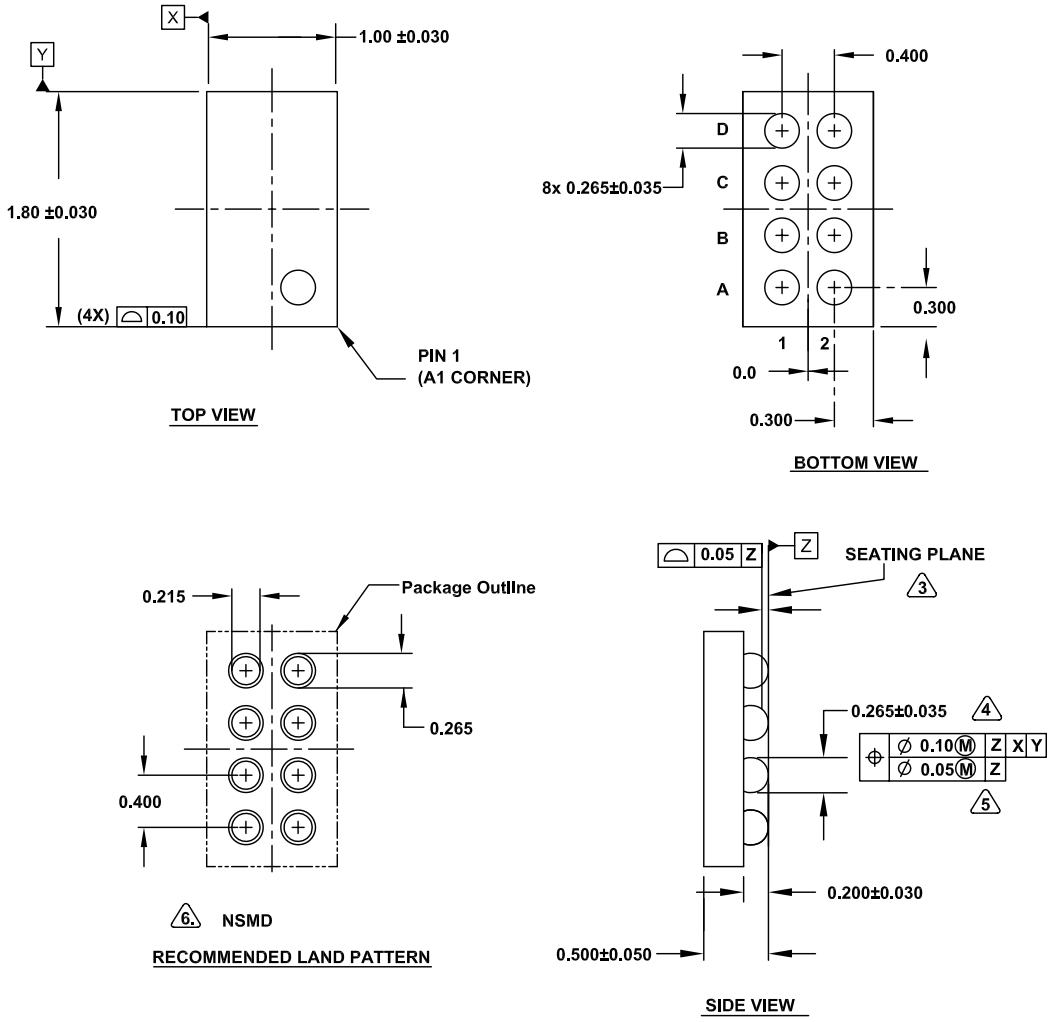
6. Revision History

Rev.	Date	Description
2.00	Jan.20.21	Added DFN package option information throughout. Added ISL9123II7Z-T to the ordering information table.
1.00	Sep.11.19	Changed the minimum values to typical values for the Maximum Load Current and Maximum Load Current at Low Vin specifications. Removed the bolding on the Output Voltage Accuracy specifications minimum and maximum values.
0.00	Aug.26.19	Initial release

7. Package Outline Drawing

For the most recent package outline drawing, see W2x4.8.

W2x4.8
8 Ball Wafer Level Chip Scale Package (WLCSP) 0.4mm Pitch
Rev 0, 6/17

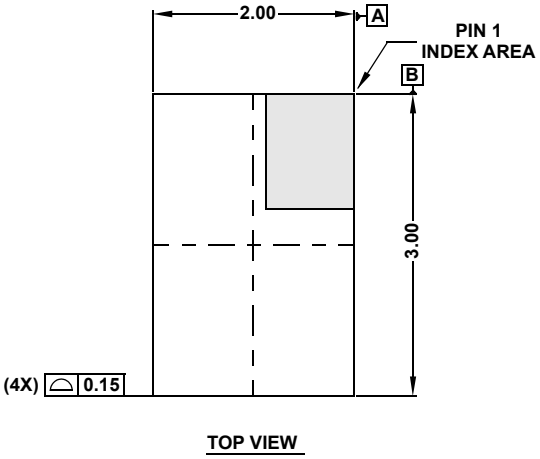


NOTES:

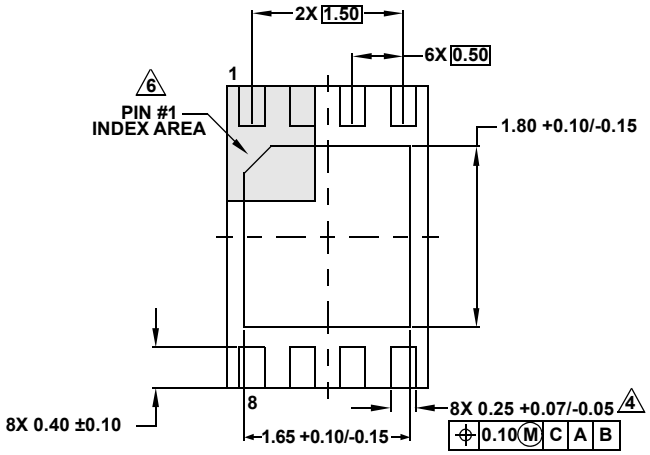
1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASMEY 14.5-1994
3. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
4. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
5. Bump position designation per JESD 95-1, SPP-010.
6. NSMD refers to non-solder mask defined pad design per Intersil Techbrief. http://www.intersil.com/data/tb/tb451.pdf

L8.2x3
8 Lead Dual Flat No-Lead Plastic Package
Rev 2, 3/15

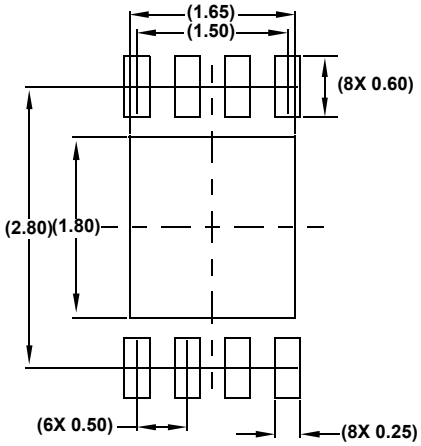
For the most recent package outline drawing, see L8.2x3.



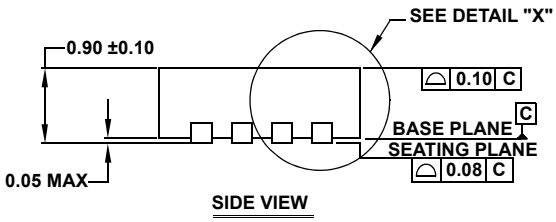
TOP VIEW



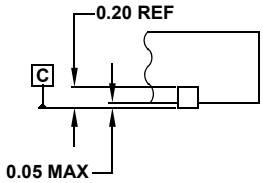
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.25mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Compies to JEDEC MO-229 VCED-2.

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