

ISL71001SLHM

Radiation Hardened 6A Synchronous Buck Regulator with Integrated MOSFETs

Description

The **ISL71001SLHM** is a radiation hardened and high-efficiency monolithic synchronous buck regulator with integrated MOSFETs. This single-chip power solution operates across an input voltage range of 3V to 5.5V and provides a tightly regulated output voltage that is externally adjustable from 0.8V to ~85% of the input voltage with an output load current capacity of 6A. The ISL71001SLHM is available in a plastic 64 Ld Thin Quad Flatpack (EP-TQFP) package.

The ISL71001SLHM uses peak current-mode control for excellent output load transient response and features integrated compensation and switches at a fixed frequency of 1MHz to reduce component size and count. The ISL71001SLHM can be synchronized to an external clock to control the input ripple current and EMI. The internal synchronous power switches are optimized for high efficiency and good thermal performance.

The ISL71001SLHM incorporates fault protection for the regulator. The protection circuits include input undervoltage, output undervoltage, and output overcurrent.

High integration makes the ISL71001SLHM an ideal choice to power many of today's small form factor applications. Two devices can be synchronized to provide a complete power solution for large-scale digital ICs, like Field Programmable Gate Arrays (FPGAs), that require separate core and I/O voltages.

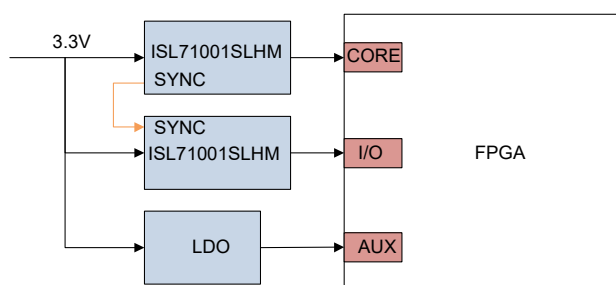


Figure 1. Typical Application

Features

- Qualified to Renesas Rad Hard Plastic Production and QCI Flow ([R34ZZ0006EU](#))
 - All screening and QCI is in accordance with SAE AS6294/1 and NASA PEMS-INST-001)
- Passes NASA low outgassing specifications
- Operates from 3V to 5.5V supply
- Current mode controlled feedback
- Fixed 1MHz switching frequency
- $\pm 1.2\%$ reference voltage
- Highly efficient: 95% peak efficiency
- SYNC pin allows synchronization of two devices
- Adjustable output voltage
- Output undervoltage and output overcurrent protection with power-good output voltage monitor
- TID Rad Hard Assurance (RHA) Wafer-by-Wafer testing
 - LDR ($\leq 10\text{mrads(Si)/s}$): 75krad(Si)
- SEE Characterization
 - No DSEE with $V_{IN} = 5.7\text{V}$ and $I_{OUT} = 7\text{A}$ at $86\text{MeV}\cdot\text{cm}^2/\text{mg}$
 - LX SET less than 1 pulse and $V_{OUT\text{ SET}} < 1\%$ at $86.4\text{MeV}\cdot\text{cm}^2/\text{mg}$
 - SEFI $< 140\mu\text{m}^2$ at $86.4\text{MeV}\cdot\text{cm}^2/\text{mg}$

Applications

- FPGA, CPLD, DSP, CPU Core, or I/O voltages
- Low-voltage, high-density distributed power systems
- Medium/Geostationary Earth Orbit (MEO/GEO)
- Launch Vehicles and High Altitude Avionics

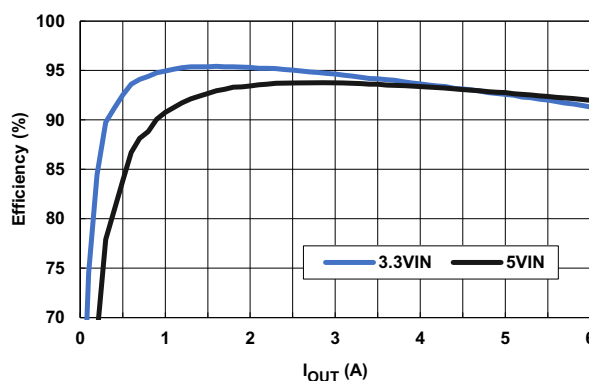


Figure 2. Efficiency vs V_{IN} for 2.5V Output, $T_C = +25^\circ\text{C}$

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1. Overview

1.1 Typical Application Schematics

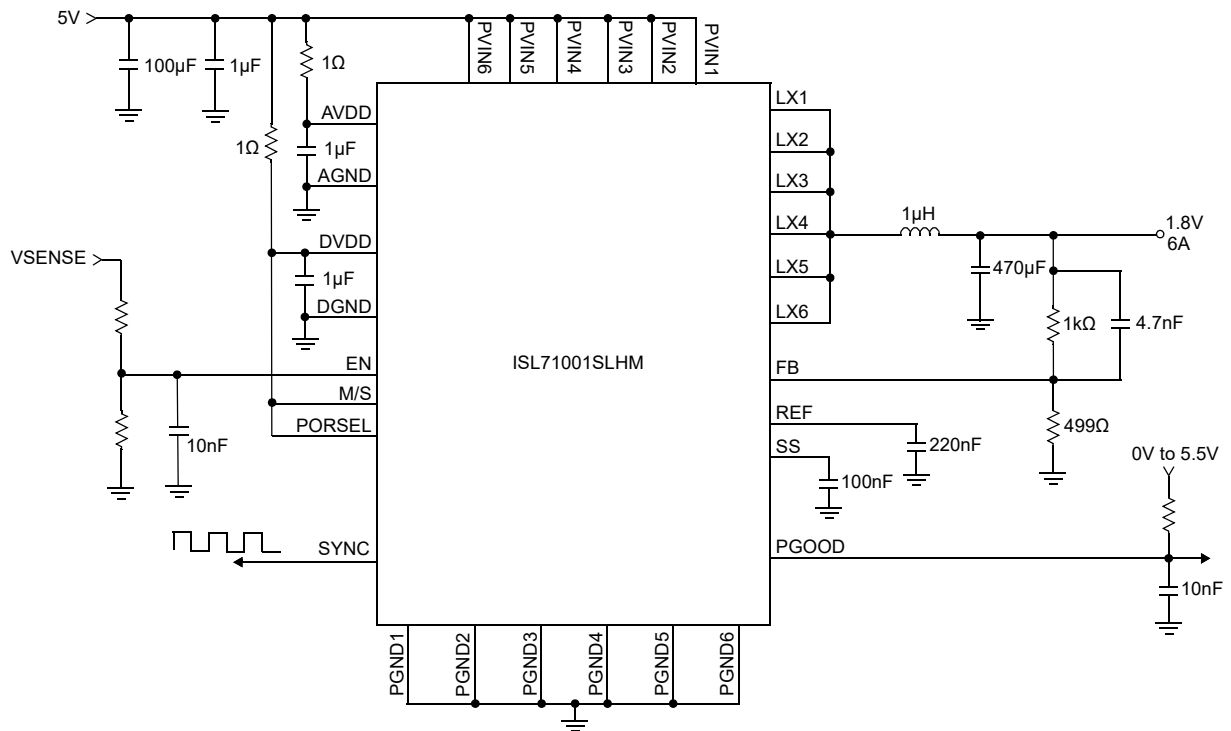


Figure 3. 5V Input Supply Voltage with Master Mode Synchronization

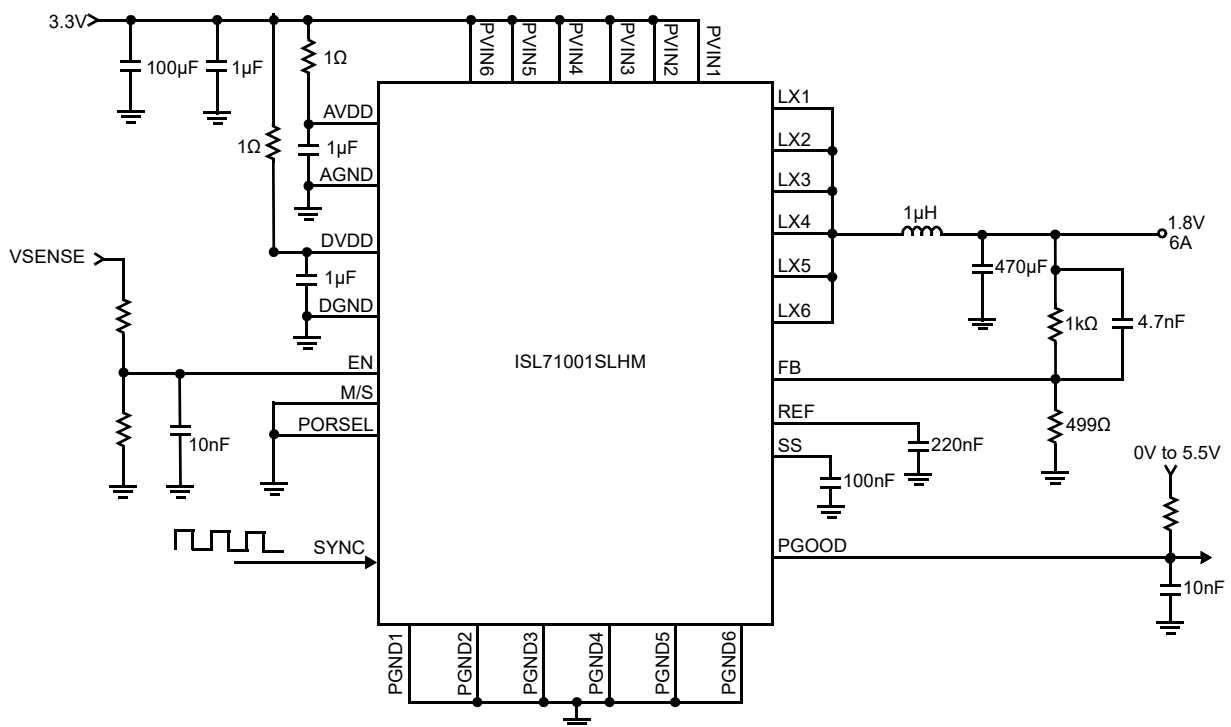


Figure 4. 3.3V Input Supply Voltage with Clock Slave Mode Synchronization

1.2 Functional Block Diagram

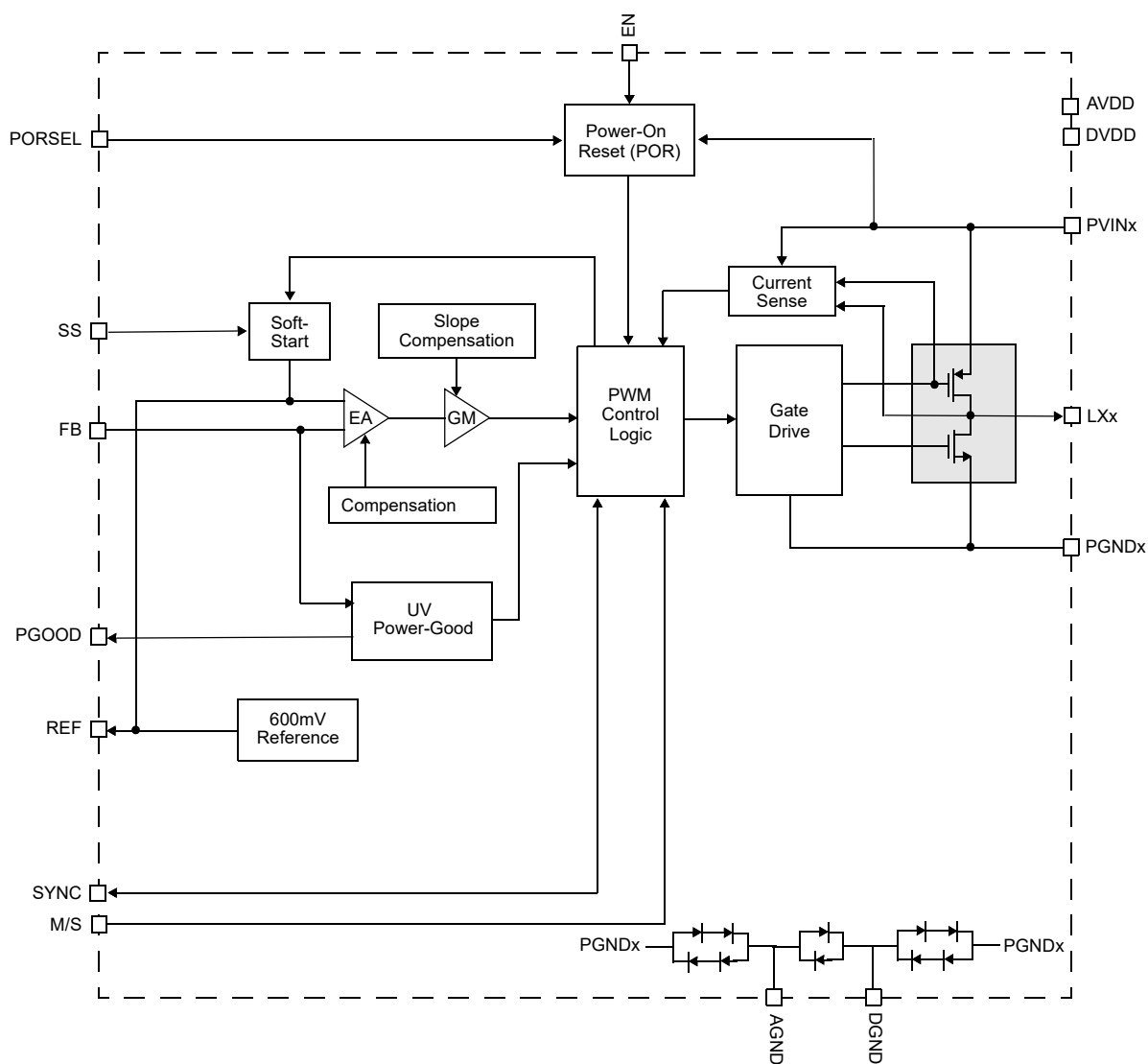
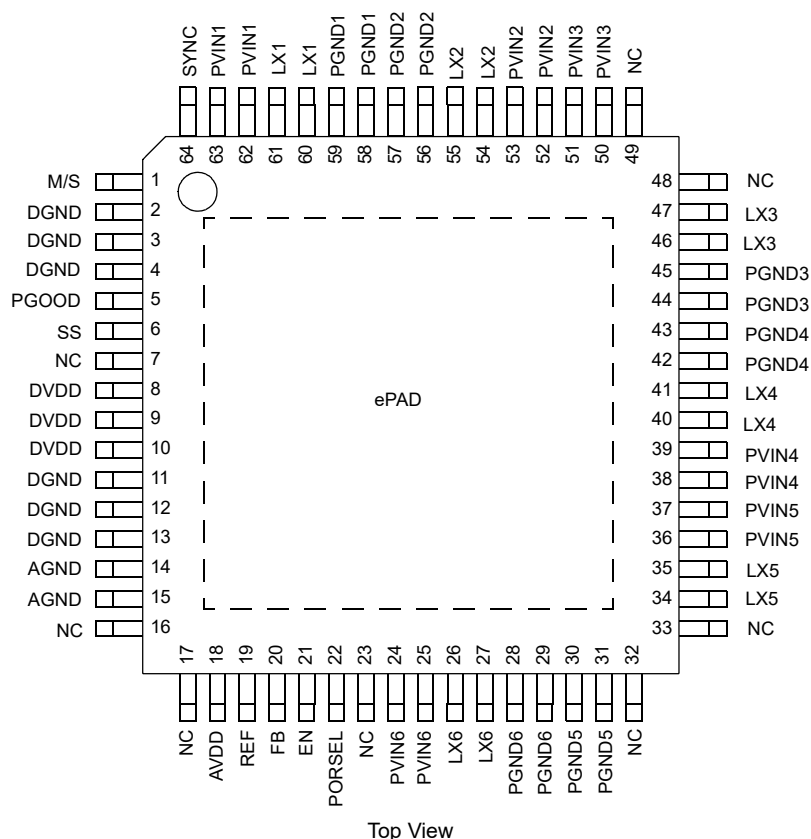


Figure 5. Block Diagram

2. Pin Information

2.1 Pin Assignments



2.2 Pin Descriptions

Pin Number	Pin Name	Description
1	M/S	Master/Slave input for selecting the direction of the bidirectional SYNC pin. For SYNC = Output (Master mode), connect this pin to DVDD. For SYNC = Input (Slave Mode), connect this pin to DGND.
2, 3, 4, 11, 12, 13	DGND	The digital ground associated with the internal digital control circuitry. Connect these pins directly to the ground plane.
5	PGOOD	Power-good output. This pin is an open-drain logic output that is pulled to DGND when the output voltage is outside a $\pm 11\%$ typical regulation window. This pin can be pulled up to any voltage from 0V to 5.5V, independent of the supply voltage. A nominal 1k Ω to 10k Ω pull-up resistor is recommended. Bypass this pin to DGND with a 10nF ceramic capacitor to mitigate SEE.
6	SS	<p>The soft-start input. Connect a ceramic capacitor from this pin to AGND to set the soft-start output ramp time in accordance with Equation 1:</p> <p>(EQ. 1) $t_{SS} = C_{SS} \cdot V_{REF} / I_{SS}$</p> <p>where:</p> <ul style="list-style-type: none"> t_{SS} = Soft-start output ramp time C_{SS} = Soft-start capacitor V_{REF} = Reference voltage (0.6V typical) I_{SS} = Soft-start charging current (23μA typical) <p>Soft-start time is adjustable from approximately 2ms to 200ms. The range of the soft-start capacitor should be 82nF to 8.2μF, inclusive.</p>
7, 16, 17, 23, 32, 33, 48, 49	NC	There is no internal connection on this pin

Pin Number	Pin Name	Description
8, 9, 10	DVDD	Bias supply inputs to the internal digital control circuitry. Connect these pins together at the IC and locally filter them to DGND using a 1Ω resistor and a 1μF ceramic capacitor. Locate both filter components as close as possible to the IC.
14, 15	AGND	Analog ground associated with the internal analog control circuitry. Connect these pins directly to the ground plane.
18	AVDD	Bias supply input to the internal analog control circuitry. Locally filter this pin to AGND using a 1Ω resistor and a 1μF ceramic capacitor. Locate both filter components as close as possible to the IC.
19	REF	Internal reference voltage output. Bypass this pin to AGND with a 220nF ceramic capacitor located as close as possible to the IC. The bypass capacitor is needed to mitigate SEE. No current (sourcing or sinking) is available from this pin.
20	FB	<p>Voltage feedback input to the internal error amplifier. Connect a resistor from FB to VOUT and from FB to AGND to adjust the output voltage in accordance with Equation 2:</p> <p>(EQ. 2) $V_{OUT} = V_{REF} \cdot [1 + (R_T/R_B)]$</p> <p>where:</p> <ul style="list-style-type: none"> • V_{OUT} = Output voltage • V_{REF} = Reference voltage (0.6V typical) • R_T = Top divider resistor (Must be 1kΩ) • R_B = Bottom divider resistor <p>The top divider resistor must be 1kΩ to mitigate SEE. Connect a 4.7nF ceramic capacitor across R_T to mitigate SEE and to improve stability margins.</p>
21	EN	Enable input to the IC. This is a comparator type input with a rising threshold of 0.6V and programmable hysteresis. Driving this pin above 0.6V enables the IC. Bypass this pin to AGND with a 10nF ceramic capacitor to mitigate SEE.
22	PORSEL	Input for selecting the rising and falling POR (Power-On-Reset) thresholds. For a nominal 5V supply, connect this pin to DVDD. For a nominal 3.3V supply, connect this pin to DGND. For nominal supply voltages between 5V and 3.3V, connect this pin to DGND.
24, 25, 36, 37, 38, 39, 50, 51, 52, 53, 62, 63	PVINx	Power supply inputs to the corresponding internal power blocks. These pins must be connected to a common power supply rail, which must fall in the range of 3V to 5.5V. Bypass these pins directly to PGNDx with ceramic capacitors located as close as possible to the IC.
26, 27, 34, 35, 40, 41, 46, 47, 54, 55, 60, 61	LXx	Outputs of the corresponding internal power blocks and should be connected to the output filter inductor. Internally, these pins are connected to the synchronous MOSFET power switches.
28, 29, 30, 31, 42, 43, 44, 45, 56, 57, 58, 59	PGNDx	Power grounds associated with the corresponding internal power blocks. Connect these pins directly to the ground plane. These pins should also connect to the negative terminals of the input and output capacitors. Locate the input and output capacitors as close as possible to the IC.
64	SYNC	Synchronization I/O for the IC. When configured as an output (Master mode), this pin drives the SYNC input of another ISL71001SLHM. When configured as an input (Slave mode), this pin accepts the SYNC output from another ISL71001SLHM or an external clock. Synchronization of the slave unit is 180° out-of-phase with respect to the master unit. If synchronizing to an external clock, the clock must be SEE hardened and the frequency must be within the range of 1MHz ±20%.
EPAD	Heatsink	Bottom thermal pad. It is not connected to any electrical potential of the IC. In the layout, it must be connected to a PCB large ground copper plane that doesn't contain noisy power flows. Put multiple vias (as many as possible) in this pad connecting to the ground copper plane, to help reduce the θ_{JA} .

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
AVDD, DVDD, LXx, PVINx	GND - 0.3	6.5	V
Signal Pins (EN, FB, PORSEL, and REF)	-	AVDD	
Digital Control Pins (M/S, SYNC)	-	DVDD	
PGOOD	GND - 0.3	6.5	V
SS	GND - 0.3	2.5	V
DC Current per Phase	-	1.2	A
Storage Temperature Range	-55	+125	°C
Maximum Operating Junction Temperature	-	+145	°C
Human Body Model (Tested per JS-001-2014)	-	4	kV
Charged Device Model (Tested per JS-002-2014)	-	2	kV
Machine Model (Tested per JESD22-A115C)	-	200	V
Latch-Up (Tested per JESD-78E; Class 2, Level A)	-	100	mA

3.2 Recommended Operation Conditions

Parameter	Minimum	Maximum	Unit
AVDD, DVDD, LXx, PVINx	3	5.5	V
Signal Pins (EN, FB, PORSEL, and REF)	-	AVDD	
Digital Pins (M/S, SYNC)	-	DVDD	
REF, SS	-	Internally Set	V
I_{LXx} ($T_J \leq +145^\circ\text{C}$)	0	1.0	A
Ambient Temperature Range	-55	+125	°C

3.3 Outgas Testing

Specification (Tested per ASTM E595, 1.5)	Value	Unit
Total Mass Loss ^[1]	0.06	%
Collected Volatile Condensable Material ^[1]	<0.01	%
Water Vapor Recovered	0.03	%

1. Outgassing results meet NASA requirements of total mass loss <1% and collected volatile condensable material of <0.1%.

3.4 Thermal Information

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	64 Ld EP-TQFP Package)	$\theta_{JA}^{[1]}$	Junction to ambient	21	°C/W
		$\theta_{JC}^{[2]}$	Junction to case	0.5	°C/W

- θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See [TB379](#).
- For θ_{JC} , the case temperature location is the center of the exposed metal pad on the package underside.

3.5 Electrical Specifications

Unless otherwise noted, $V_{IN} = AVDD = DVDD = PVINx = EN = M/S = 3V$ or $5.5V$; $GND = AGND = DGND = PGNDx = 0V$; $FB = 0.65V$; $PORSEL = V_{IN}$ for $4.5V \leq V_{IN} \leq 5.5V$ and GND for $V_{IN} < 4.5V$; $SYNC = LXx =$ open circuit; $PGOOD$ is pulled up to V_{IN} with a 1k resistor; REF is bypassed to GND with a 220nF capacitor; SS is bypassed to GND with a 100nF capacitor; $I_{OUT} = 0A$; **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s.**

Parameter	Test Conditions	Min ^[1]	Typ ^[2]	Max ^[1]	Unit
Power Supply					
Operating Supply Current ^[3]	$V_{IN} = 5.5V$	-	40	65	mA
	$V_{IN} = 3.6V$	-	25	45	mA
Shutdown Supply Current ^[4]	$V_{IN} = 5.5V$, $EN = GND$	-	2	6	mA
	$V_{IN} = 3.6V$, $EN = GND$	-	1.4	4.5	mA
Output Voltage					
Reference Voltage Tolerance	-	0.593	0.6	0.607	V
Feedback (FB) Input Leakage Current	$V_{IN} = 5.5V$, $V_{FB} = 0.6V$	-1	0	1	μA
PWM Control Logic					
Oscillator Accuracy	-	0.82	1	1.18	MHz
External Oscillator Range	-	0.8	1	1.2	MHz
Minimum LXx On Time	$V_{IN} = 5.5V$, Test mode	-	107	150	ns
Minimum LXx Off Time	$V_{IN} = 5.5V$, Test mode	-	41	100	ns
Minimum LXx On Time	$V_{IN} = 3.6V$, Test mode	-	142	210	ns
Minimum LXx Off Time	$V_{IN} = 3.6V$, Test mode	-	41	100	ns
Master/Slave (M/S) Input Voltage	Input high threshold	$V_{IN} - 0.5$	1.9	-	V
	Input low threshold	-	1.3	0.5	V
Master/Slave (M/S) Input Leakage Current	$V_{IN} = 5.5V$, $M/S = GND$ or V_{IN}	-1	0	1	μA
Synchronization (SYNC) Input Voltage	Input high threshold, $M/S = GND$	2.3	1.7	-	V
	Input low threshold, $M/S = GND$	-	1.5	1	V
Synchronization (SYNC) Input Leakage Current	$V_{IN} = 5.5V$, $M/S = GND$, $SYNC = GND$ or V_{IN}	-1	0	1	μA
Synchronization (SYNC) Output Voltage	$V_{IN} - V_{OH}$ at $I_{OH} = -1mA$	-	0.16	0.4	V
	V_{OL} at $I_{OL} = 1mA$	-	0.14	0.4	V
Power Blocks					
Upper Device $r_{DS(ON)}$	$V_{IN} = 3V$, 0.4A per power block, Test mode	80	142	220	mΩ
Lower Device $r_{DS(ON)}$	$V_{IN} = 3V$, 0.4A per power block, Test mode	40	85	140	mΩ

Unless otherwise noted, $V_{IN} = AVDD = DVDD = PVINx = EN = M/S = 3V$ or $5.5V$; $GND = AGND = DGND = PGNDx = 0V$; $FB = 0.65V$; $PORSEL = V_{IN}$ for $4.5V \leq V_{IN} \leq 5.5V$ and GND for $V_{IN} < 4.5V$; $SYNC = LXx =$ open circuit; $PGOOD$ is pulled up to V_{IN} with a $1k$ resistor; REF is bypassed to GND with a $220nF$ capacitor; SS is bypassed to GND with a $100nF$ capacitor; $I_{OUT} = 0A$; **Boldface limits apply across the operating temperature range, $-55^{\circ}C$ to $+125^{\circ}C$ by production testing; over a total ionizing dose of $75krad(Si)$ at $+25^{\circ}C$ with exposure at a low dose rate of $<10mrads(Si)/s$.** (Cont.)

Parameter	Test Conditions	Min ^[1]	Typ ^[2]	Max ^[1]	Unit
LXx Output Leakage	$V_{IN} = 5.5V$, $EN = LXx = GND$, single LXx output	-1	0	1	μA
	$V_{IN} = 5.5V$, $EN = GND$, $LXx = V_{IN}$, single LXx output	-15	0	15	μA
Dead Time	Within a single power block or between power blocks	1.7	5	-	ns
Efficiency	$V_{IN} = 3.3V$, $V_{OUT} = 1.8V$, $I_{OUT} = 3A$	-	94	-	%
	$V_{IN} = 5V$, $V_{OUT} = 3.3V$, $I_{OUT} = 3A$	-	95	-	%
Power-On Reset					
POR Select (PORSEL)	Input high threshold	$V_{IN} - 0.5$	1.4	-	V
	Input low threshold	-	1.3	0.5	V
POR Select (PORSEL) Input Leakage Current	$V_{IN} = 5.5V$, $PORSEL = GND$ or V_{IN}	-1	0	1	μA
VIN POR	Rising threshold, $PORSEL = V_{IN}$	4.1	4.28	4.45	V
	Hysteresis, $PORSEL = V_{IN}$	225	331	425	mV
	Rising threshold, $PORSEL = GND$	2.65	2.8	2.95	V
	Hysteresis, $PORSEL = GND$	90	168	260	mV
Enable (EN) Input Voltage	Rising/falling threshold	0.56	0.6	0.64	V
Enable (EN) Input Leakage Current	$V_{IN} = 5.5V$, $EN = GND$ or V_{IN}	-3	0	3	μA
Enable (EN) Sink Current	$EN = 0.3V$	6.4	11	16.6	μA
Soft-Start					
Soft-Start Source Current	$SS = GND$	20	23	27	μA
Soft-Start Discharge ON-Resistance	-	-	2.1	4.7	Ω
Soft-Start Discharge Time	-	-	256	-	Clock Cycles
Power-Good Signal					
Rising Threshold	V_{FB} as a percent of V_{REF} , Test mode	107	112	115	%
Rising Hysteresis	V_{FB} as a percent of V_{REF} , Test mode	2	3.7	5	%
Falling Threshold	V_{FB} as a percent of V_{REF} , Test mode	85	88	93	%
Falling Hysteresis	V_{FB} as a percent of V_{REF} , Test mode	2	3.6	5	%
Power-Good Drive	$V_{IN} = 3V$, $PGOOD = 0.4V$, $EN = GND$	7.3	8.2	-	mA
Power-Good Leakage	$V_{IN} = PGOOD = 5.5V$	-	0.001	1	μA
Protection Features					
Undervoltage Monitor					
Undervoltage Trip Threshold	$V_{IN} = 3V$, V_{FB} as a percent of V_{REF} , Test mode	71	75	79	%
Undervoltage Recovery Threshold	$V_{IN} = 3V$, V_{FB} as a percent of V_{REF} , Test mode	84	88	92	%

Unless otherwise noted, $V_{IN} = AVDD = DVDD = PVINx = EN = M/S = 3V$ or $5.5V$; $GND = AGND = DGND = PGNDx = 0V$; $FB = 0.65V$; $PORSEL = V_{IN}$ for $4.5V \leq V_{IN} \leq 5.5V$ and GND for $V_{IN} < 4.5V$; $SYNC = LXx =$ open circuit; $PGOOD$ is pulled up to V_{IN} with a $1k$ resistor; REF is bypassed to GND with a $220nF$ capacitor; SS is bypassed to GND with a $100nF$ capacitor; $I_{OUT} = 0A$; **Boldface limits apply across the operating temperature range, $-55^{\circ}C$ to $+125^{\circ}C$ by production testing; over a total ionizing dose of $75krad(Si)$ at $+25^{\circ}C$ with exposure at a low dose rate of $<10mrads(Si)/s$.** (Cont.)

Parameter	Test Conditions	Min ^[1]	Typ ^[2]	Max ^[1]	Unit
Overcurrent Monitor					
Overcurrent Trip Level	LX4 power block, Test mode	1.3	1.7	2.5	A
Overcurrent Trip Counts	LX4 power block, Test mode	-	2	-	-
Overcurrent or Short-Circuit Duty-Cycle	$V_{IN} = 3V$, SS interval = $200\mu s$, Test mode, fault interval divided by hiccup interval	-	0.8	5	%

1. Compliance to datasheet limits is assured by one or more methods: analysis, characterization, design, or production test.
2. Typical values shown are not guaranteed.
3. $L = 1\mu H$ connected to Lx .
4. $1k\Omega$ $PGOOD$ pull-up resistor is not populated.

4. Typical Operating Performance

Unless otherwise noted, $T_A = +25^\circ\text{C}$, $V_{IN} = 5\text{V}$, $EN = 5\text{V}$, $L = 1.0\mu\text{H}$, $C_{IN} = 2 \times 47\mu\text{F}$, $C_{OUT} = 3 \times 47\mu\text{F}$ and $1 \times 150\mu\text{F}$, $V_{OUT} = 1.2\text{V}$.

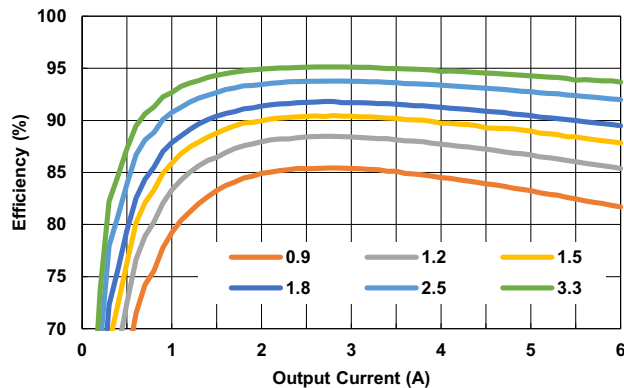


Figure 6. 5V V_{IN} Efficiency for Multiple V_{OUT} Levels

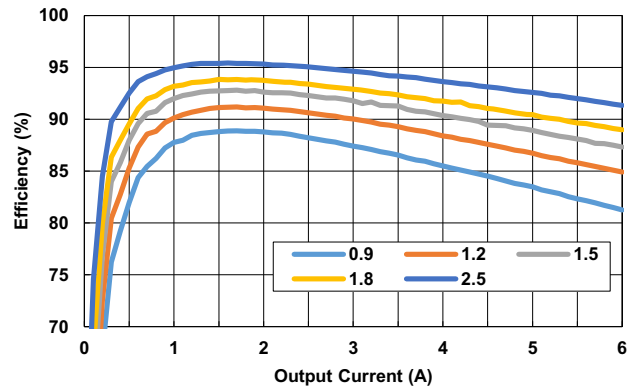


Figure 7. 3.3V V_{IN} Efficiency for Multiple V_{OUT} Levels

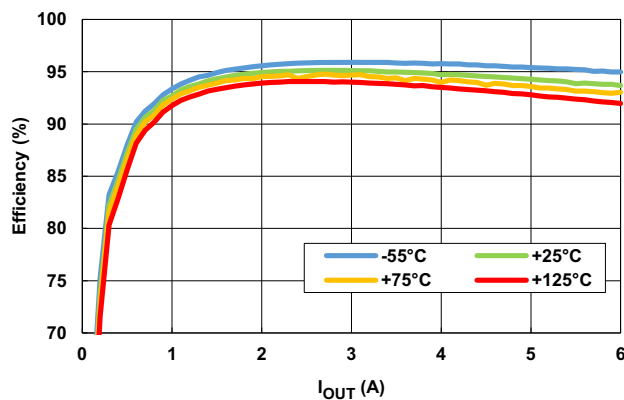


Figure 8. 5V V_{IN} Efficiency, 3.3V V_{OUT} Over Temperature

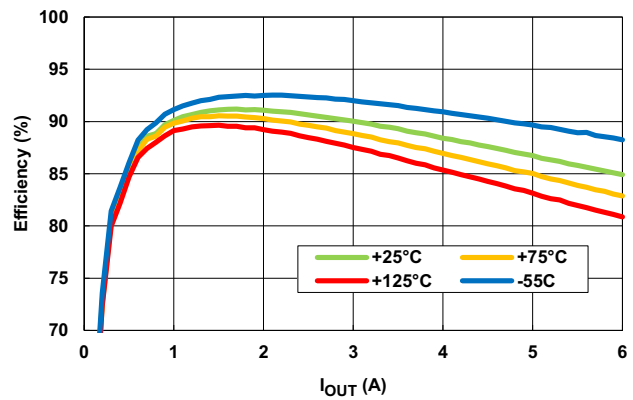


Figure 9. 3.3V V_{IN} Efficiency, 1.2V V_{OUT} Over Temperature

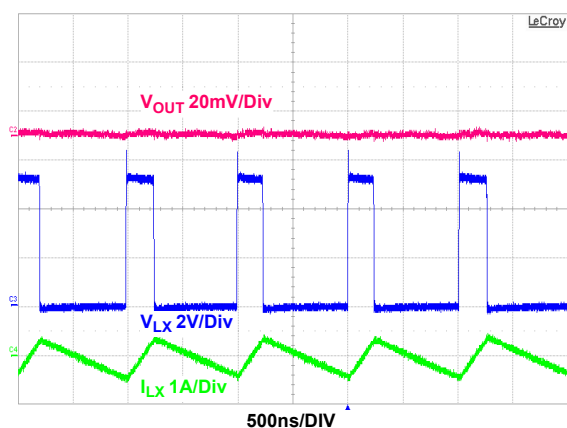


Figure 10. LX, V_{OUT} and Inductor Current Waveforms, $I_O = 0\text{A}$

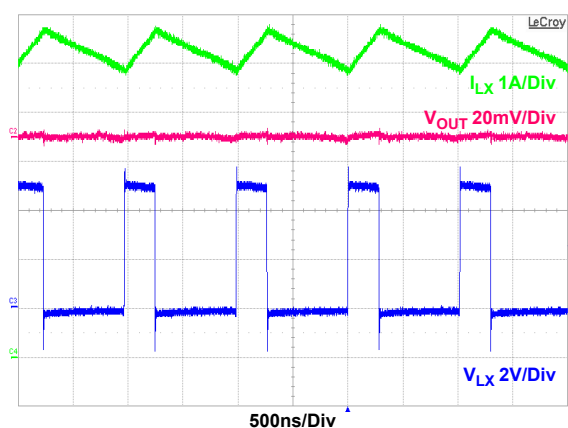


Figure 11. LX, V_{OUT} and Inductor Current Waveforms, $I_O = 6\text{A}$

Unless otherwise noted, $T_A = +25^\circ\text{C}$, $V_{IN} = 5\text{V}$, $EN = 5\text{V}$, $L = 1.0\mu\text{H}$, $C_{IN} = 2 \times 47\mu\text{F}$, $C_{OUT} = 3 \times 47\mu\text{F}$ and $1 \times 150\mu\text{F}$, $V_{OUT} = 1.2\text{V}$. (Cont.)

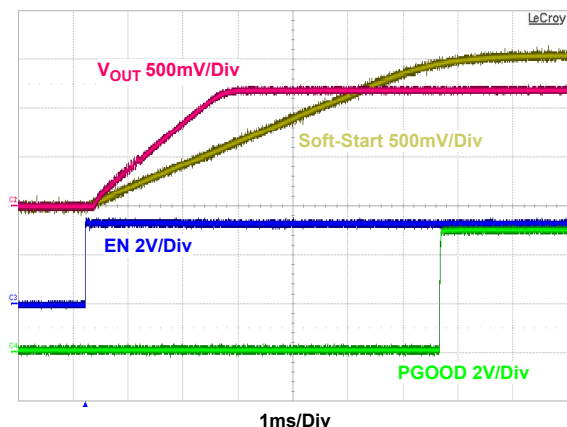


Figure 12. Enabled Start-Up Waveforms

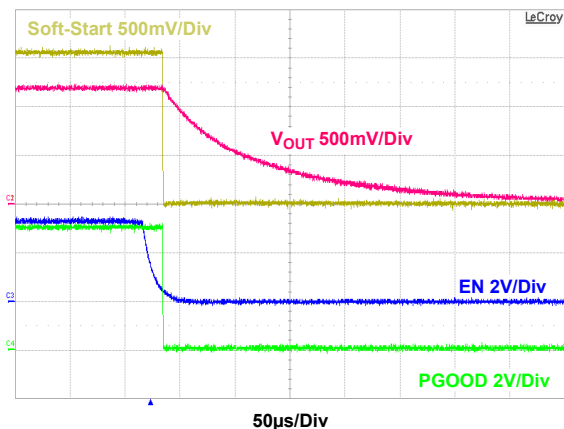


Figure 13. Disabled Turn-Off Waveforms

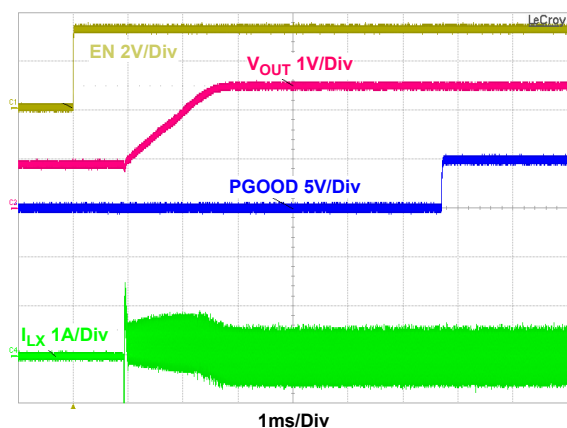
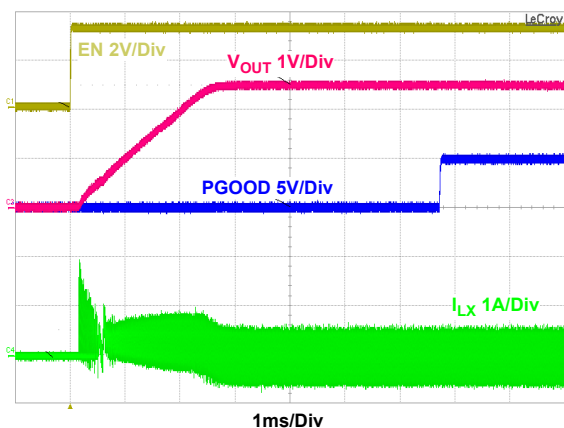
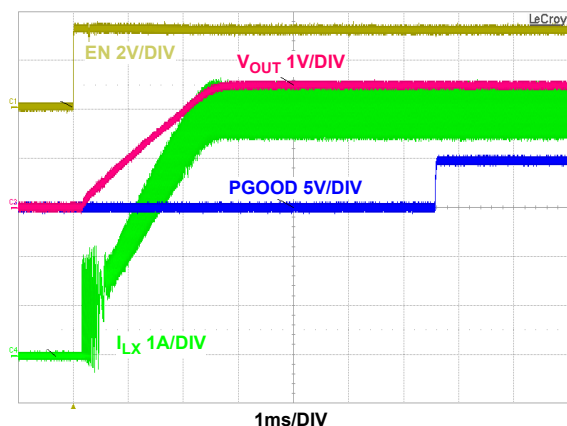
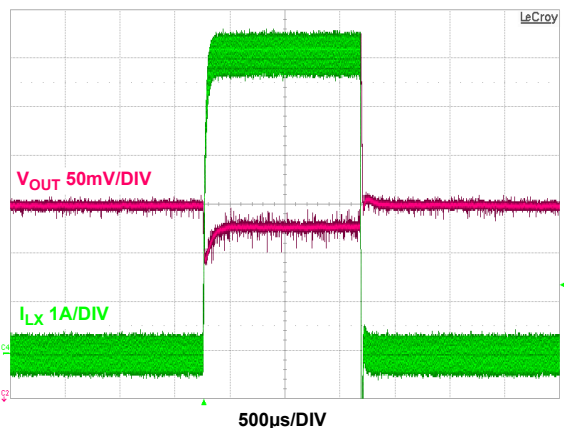
Figure 14. 0.5V Prebiased Start-Up to 2.5V V_{OUT} Waveforms $I_O = 0\text{A}$ Figure 15. Start-Up to 2.5V V_{OUT} Waveforms $I_O = 0\text{A}$ Figure 16. Start-Up to 2.5V V_{OUT} Waveforms $I_O = 5\text{A}$ 

Figure 17. Load Transient 0 to 6A

Unless otherwise noted, $T_A = +25^\circ\text{C}$, $V_{IN} = 5\text{V}$, $EN = 5\text{V}$, $L = 1.0\mu\text{H}$, $C_{IN} = 2 \times 47\mu\text{F}$, $C_{OUT} = 3 \times 47\mu\text{F}$ and $1 \times 150\mu\text{F}$, $V_{OUT} = 1.2\text{V}$. (Cont.)

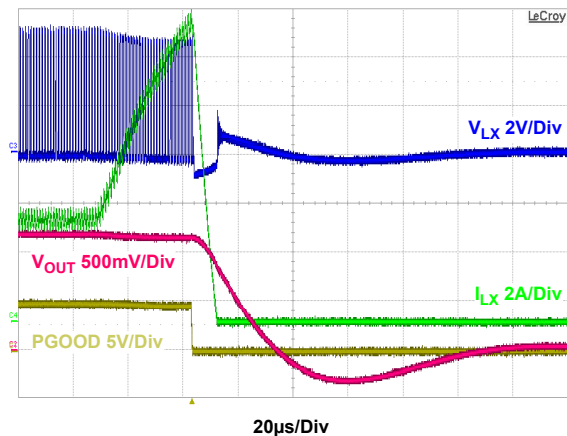


Figure 18. Into Overcurrent Waveforms

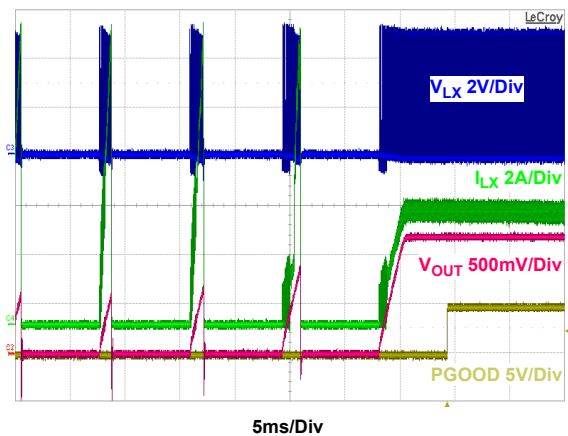


Figure 19. Out of Overcurrent Recovery Waveforms

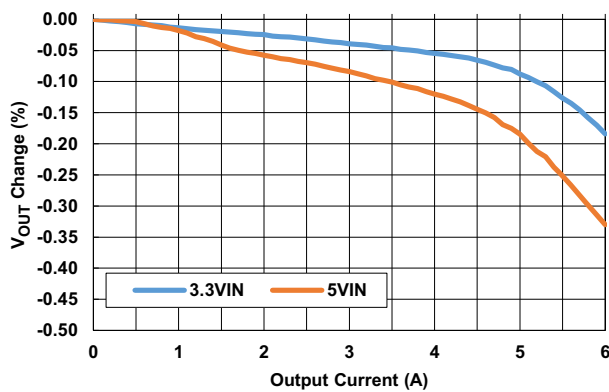


Figure 20. V_{IN} Load Regulation $1.2\text{V } V_{OUT}$

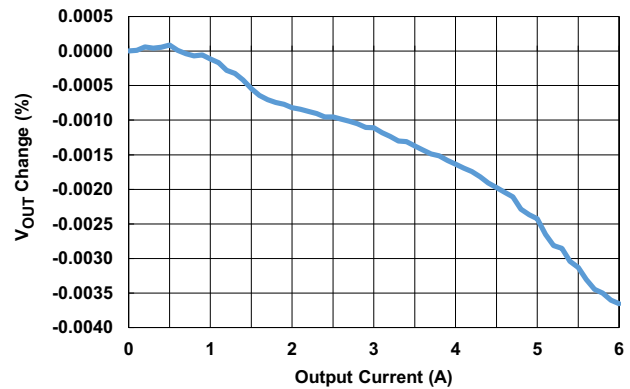


Figure 21. V_{IN} Line Regulation, $V_{OUT} = 2.5\text{V } (5V_{IN} - 3.3V_{IN})$

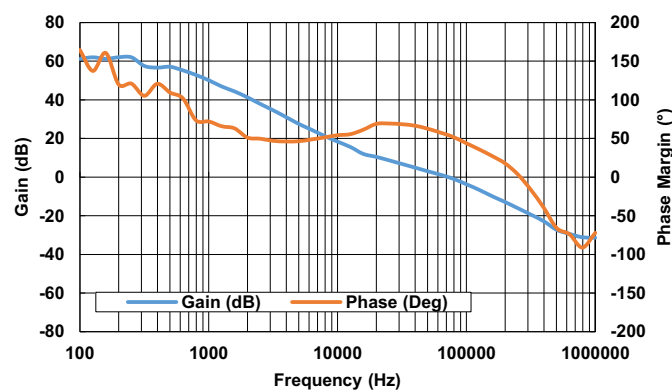


Figure 22. Gain Phase Graph

5. Device Information

5.1 Functional Description

The ISL71001SLHM is a monolithic, fixed frequency, current-mode synchronous buck regulator with user-configurable power blocks. Using two ISL71001SLHM devices can provide a total DC/DC solution for FPGAs, CPLDs, DSPs, and CPUs.

5.1.1 Power Blocks

The power output stage of the regulator consists of six 1A capable power blocks that are paralleled to provide full 6A output current capability. The block diagram in [Figure 23](#) shows a top level view of the individual power blocks.

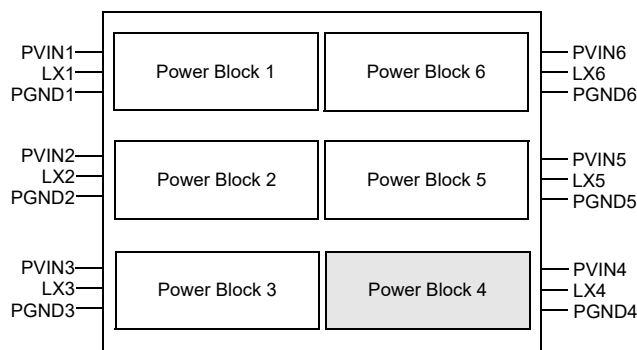


Figure 23. Power Block Diagram

Each power block has a power supply input pin (PVIN_x), a phase output pin (LX_x), and a power supply ground pin (PGND_x). All PVIN_x pins must be connected to a common power supply rail and all PGND_x pins must be connected to a common ground. The LX_x pins should be connected to the output inductor based on the required load current, but must include the LX4 pin. For example, if 3A of output current is needed, any three LX_x pins can be connected to the inductor as long as one of them is the LX4 pin. The unused LX_x pins should be left unconnected. Connecting all six LX_x pins to the output inductor provides a maximum 6A of output current. See the [Typical Application Schematics](#) for pin connection guidance.

A scaled pilot device associated with each power block provides current feedback. Power Block 4 contains the master pilot device and this is why it must be connected to the output inductor.

5.1.2 Main Control Loop

During normal operation, the internal top power switch is turned on at the beginning of each clock cycle. Current in the output inductor ramps up until the current comparator trips and turns off the top power MOSFET. The bottom power MOSFET turns on and the inductor current ramps down for the rest of the cycle.

The current comparator compares the output current at the ripple current peak to a current pilot. The error amplifier monitors V_{OUT} and compares it with an internal reference voltage. The output voltage of the error amplifier drives a proportional current to the pilot. If V_{OUT} is low, the current level of the pilot is increased and the trip off current level of the output is increased. The increased output current raises V_{OUT} until it is in agreement with the reference voltage.

5.1.3 Output Voltage Selection

The output voltage of the ISL71001SLHM can be adjusted using an external resistor divider as shown in Figure 24.

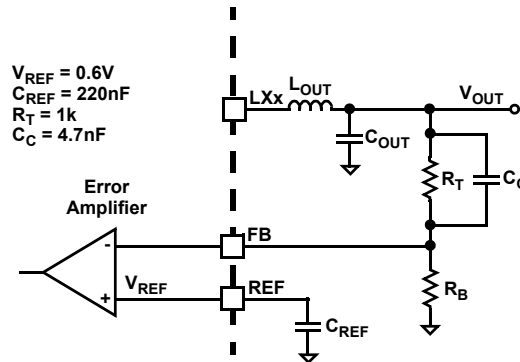


Figure 24. Output Voltage Selection

R_T should be selected as 1k Ω to mitigate single event transients. R_T should be shunted by a 4.7nF ceramic capacitor (C_C) to mitigate single event transients and to improve loop stability margins. The REF pin should be bypassed to AGND with a 220nF ceramic capacitor to mitigate single-event transients. **Note:** No current (sourcing or sinking) is available from the REF pin. R_B can be determined from Equation 3. You can configure the output voltage from 0.8V to 85% of the input voltage.

$$(EQ. 3) \quad R_B = R_T \cdot \frac{V_{REF}}{V_{OUT} - V_{REF}}$$

5.1.4 Switching Frequency/Synchronization

The ISL71001SLHM features an internal oscillator running at a fixed frequency of 1MHz. The regulator can be configured to run from the internal oscillator or can be synchronized to another ISL71001SLHM or an external clock with a frequency range of 1MHz \pm 20%.

To run the regulator from the internal oscillator, connect the M/S pin to DVDD. In this case, the output of the internal oscillator appears on the SYNC pin. To synchronize the regulator to an external clock, connect the M/S pin to DGND. In this case, the SYNC pin is an input that accepts an external synchronizing signal. When synchronizing multiple devices, slave regulators are synchronized 180° out-of-phase with respect to the external clock.

When using an ISL71001SLHM in clock slave mode and applying an external clock to SYNC (whether from a clock master ISL71001SLHM or another external clock), all the clock slaves using the external clock signal must have their switching disabled through their EN input before any stoppage of the clock on the SYNC input. If the external clock signal on the SYNC pin stops or is otherwise removed while the clock slave ISL71001SLHM is enabled, the internal lower FET turns on and remains on as the ISL71001SLHM control circuit waits for the next rising edge of the external clock that never arrives (see Figure 25). Current from the load then recirculates through the stuck-on lower FET. Figure 25 shows the SYNC stopping at a low level. If the SYNC stops at a level greater than the SYNC voltage threshold (V_{th}), and then decreases through the SYNC V_{th} , there is a solitary LX pulse.

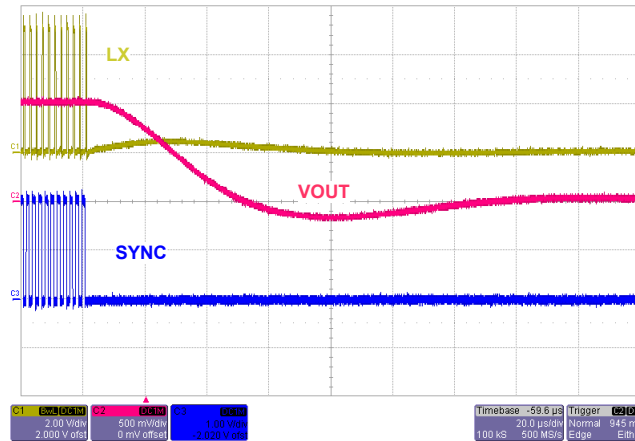


Figure 25. SYNC Loss Showing LX Pulled Low

5.2 Operation Initialization

The ISL71001SLHM initializes based on the state of the Power-On Reset (POR) monitor of the PVINx inputs and the state of the EN input. Successful initialization prompts a soft-start interval, and the regulator begins slowly ramping the output voltage. When the commanded output voltage is within the proper window of operation, the power-good signal changes state from low to high, indicating proper regulator operation.

5.2.1 Power-On Reset

The POR circuitry prevents the controller from attempting to soft-start before sufficient bias is present at the PVINx pins.

The POR threshold of the PVINx pins is controlled by the PORSEL pin. For a nominal 5V supply voltage, connect PORSEL to DVDD. For a nominal 3.3V supply voltage, connect PORSEL to DGND. For nominal supply voltages between 5V and 3.3V, connect PORSEL to DGND. The POR rising and falling thresholds are shown in [Power-On Reset](#).

Hysteresis between the rising and falling thresholds ensures that small perturbations on PVINx seen during turn-on/turn-off of the regulator do not cause inadvertent turn-off/turn-on of the regulator. When the PVINx pins are below the POR rising threshold, the internal synchronous power MOSFET switches are turned off, and the LXx pins are held in a high-impedance state.

5.2.2 Enable and Disable

After the POR input requirement is met, the ISL71001SLHM remains in shutdown until the voltage at the enable input rises above the enable threshold. As shown in [Figure 26](#), the enable circuit features a comparator-type input. In addition to simple logic on/off control, the enable circuit allows the level of an external voltage to precisely gate the turn-on/turn-off of the regulator. An internal I_{EN} current sink with a typical value of $11\mu A$ is only active when the voltage on the EN pin is below the enable threshold. The current sink pulls the EN pin low. As V_{IN2} rises, the enable level is not set exclusively by the resistor divider from V_{IN2} .

With the current sink active, the enable level is defined by [Equation 4](#). R_1 is the resistor from the EN pin to V_{IN2} and R_2 is the resistor from the EN pin to the AGND pin.

$$(EQ. 4) \quad V_{ENABLE} = V_R \cdot \left[1 + \frac{R_1}{R_2} \right] + I_{EN} \cdot R_1$$

When the voltage at the EN pin reaches the enable threshold, the I_{EN} current sink turns off.

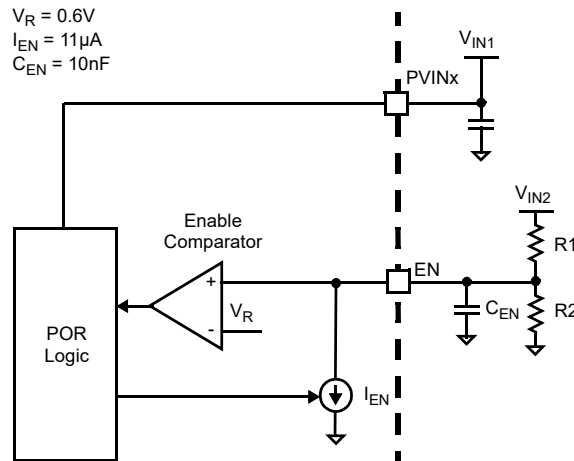


Figure 26. Enable Circuit

With the part enabled and the I_{EN} current sink off, the disable level is set by the resistor divider. The disable level is defined by Equation 5.

$$(EQ. 5) \quad V_{DISABLE} = V_R \cdot \left[1 + \frac{R_1}{R_2} \right]$$

The difference between the enable and disable levels provides adjustable hysteresis so that noise on V_{IN2} does not interfere with the enabling or disabling of the regulator.

To mitigate single-event transients, the EN pin should be bypassed to the AGND pin with a 10nF ceramic capacitor.

5.2.3 Soft-Start

When the POR and enable circuits are satisfied, the regulator initiates a soft-start. Figure 27 shows that the soft-start circuit clamps the error amplifier reference voltage to the voltage on an external soft-start capacitor connected to the SS pin.

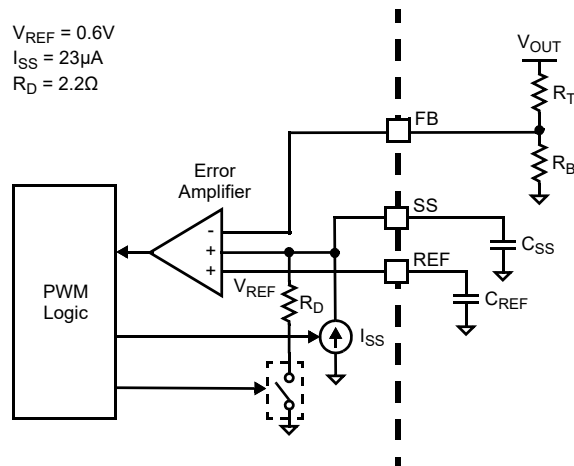


Figure 27. Soft-Start Circuit

The soft-start capacitor is charged by an internal I_{SS} current source. As the soft-start capacitor is charged, the output voltage slowly ramps to the set point determined by the reference voltage and the feedback network. When the voltage on the SS pin is equal to the internal reference voltage, the soft-start interval is complete. The controlled ramp of the output voltage reduces the inrush current during start-up. The soft-start output ramp interval

is defined in [Equation 6](#) and is adjustable from approximately 2ms to 200ms. The value of the soft-start capacitor, C_{SS} , should range inclusively from 8.2nF to 8.2μF. The peak inrush current can be computed from [Equation 7](#). The soft-start interval should be long enough to ensure that the peak inrush current plus the peak output load current does not exceed the overcurrent trip level of the regulator.

$$(EQ. 6) \quad t_{SS} = C_{SS} \cdot \frac{V_{REF}}{I_{SS}}$$

$$(EQ. 7) \quad I_{INRUSH} = C_{OUT} \cdot \frac{V_{OUT}}{t_{SS}}$$

The soft-start capacitor is immediately discharged by a 2.2Ω resistor whenever POR conditions are not met or EN is pulled low. The soft-start discharge time is equal to 256 clock cycles.

5.2.4 Power-Good

The Power-Good (PGOOD) pin is an open-drain logic output that indicates when the output voltage of the regulator is within regulation limits. The power-good pin pulls low during shutdown and remains low when the controller is enabled. After a successful soft-start, the PGOOD pin releases, and the voltage rises with an external pull-up resistor. The power-good signal transitions low immediately when the EN pin is pulled low.

The power-good circuitry monitors the FB pin and compares it to the rising and falling thresholds shown in [Power-Good Signal](#). If the feedback voltage exceeds the typical rising limit of 111% of the reference voltage, the PGOOD pin pulls low. The PGOOD pin continues to pull low until the feedback voltage falls to a typical of 107.5% of the reference voltage. If the feedback voltage drops below a typical of 89% of the reference voltage, the PGOOD pin pulls low. The PGOOD pin continues to pull low until the feedback voltage rises to a typical 92.5% of the reference voltage. The PGOOD pin then releases and signals the return of the output voltage to within the power-good window.

The PGOOD pin can be pulled up to any voltage from 0V to 5.5V, independently from the supply voltage. The pull-up resistor should have a nominal value from 1kΩ to 10kΩ. The PGOOD pin should be bypassed to DGND with a 10nF ceramic capacitor to mitigate single-event transients.

5.3 Fault Monitoring and Protection

The ISL71001SLHM actively monitors output voltage and current to detect fault conditions. Fault conditions trigger protective measures to prevent damage to the regulator and external load device.

5.3.1 Undervoltage Protection

A hysteretic comparator monitors the FB pin of the regulator. The feedback voltage is compared to an undervoltage threshold that is a fixed percentage of the reference voltage. When the comparator trips, indicating a valid undervoltage condition, an undervoltage counter increments. The counter is reset if the feedback voltage rises back above the undervoltage threshold, plus a specified amount of hysteresis outlined in the [Electrical Specifications](#) table. If the undervoltage condition exists for three consecutive counts, the counter overflows and the undervoltage protection logic shuts down the regulator.

After the regulator shuts down, it enters a delay interval equivalent to the soft-start interval, which allows the device to cool. The undervoltage counter is reset when the device enters the delay interval. The protection logic initiates a normal soft-start when the delay interval ends. If the output successfully soft-starts, the power-good signal goes high, and normal operation continues. If undervoltage conditions continue to exist during the soft-start interval, the undervoltage counter must overflow before the regulator shuts down again. This hiccup mode continues indefinitely until the output soft-starts successfully.

5.3.2 Overcurrent Protection

A pilot device integrated into the PMOS transistor of Power Block 4 samples current each cycle. This current feedback is scaled and compared to an overcurrent threshold based on the number of power blocks connected.

Each additional power block connected beyond Power Block 4 increases the overcurrent limit by 2A. For example, if three power blocks are connected, the typical current limit threshold would be $3 \times 2A = 6A$.

If the sampled current exceeds the overcurrent threshold, an overcurrent counter increments by one. When the overcurrent counter reaches a count of 3, it overflows and the regulator shuts down. If the sampled current falls below the threshold before the counter overflows, the counter is reset.

After the regulator shuts down, it enters a delay interval, equivalent to the soft-start interval, which allows the device to cool. The overcurrent counter is reset when the device enters the delay interval. The protection logic initiates a normal soft-start when the delay interval ends. If the output successfully soft-starts, the power-good signal goes high, and normal operation continues. If overcurrent conditions continue to exist during the soft-start interval, the overcurrent counter must overflow before the regulator shuts down the output again. This hiccup mode continues indefinitely until the output soft-starts successfully.

5.4 Feedback Loop Compensation

To reduce the number of external components and to simplify the process of determining compensation components, the ISL71001SLHM buck regulator has an internally compensated error amplifier.

Because of the current loop feedback in peak current mode control, the modulator has a single-pole response with -20dB slope at a frequency determined by the load (Equation 8):

$$(EQ. 8) \quad F_{PO} = \frac{1}{2\pi \cdot R_O \cdot C_{OUT}}$$

where R_O is load resistance and C_{OUT} is the output load capacitance. For this type of modulator, a Type 2 compensation circuit is usually sufficient.

Figure 28 shows a Type 2 amplifier and its response, along with the responses of the current-mode modulator and the converter.

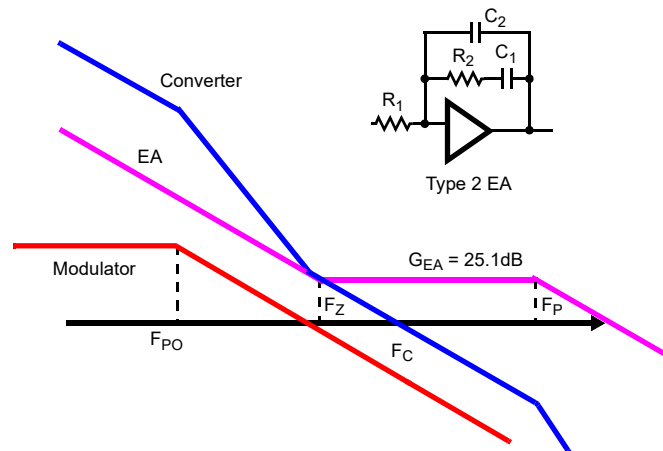


Figure 28. Feedback Loop Compensation

The Type 2 amplifier, in addition to the pole at origin, has a zero-pole pair that causes a flat gain region at frequencies between the zero and the pole (Equation 9 and Equation 10).

$$(EQ. 9) \quad F_Z = \frac{1}{2\pi \cdot R_2 \cdot C_1} = 8.6\text{kHz}$$

$$(EQ. 10) \quad F_P = \frac{1}{2\pi \cdot R_1 \cdot C_2} = 546\text{kHz}$$

Zero frequency and amplifier high-frequency gain were chosen to satisfy typical applications. The crossover frequency appears at the point where the modulator attenuation equals the amplifier high frequency gain. The only task that the system designer has to complete is to specify the output filter capacitors, to position the load main

pole somewhere within one decade lower than the amplifier zero frequency. Equation 13 approximates the amount of capacitance needed to achieve an optimal pole location depending on the number of LXx pins connected. With this type of compensation, plenty of phase margin is easily achieved because of zero-pole pair phase boost.

Conditional stability may occur only when the main load pole is positioned too much to the left side on the frequency axis because of excessive output filter capacitance. In this case, the ESR zero placed within the 1.2kHz to 30kHz range gives some additional phase boost. Some phase boost is also achieved by connecting the recommended capacitor C_C in parallel with the upper resistor R_T of the divider that sets the output voltage value, as demonstrated in Figure 24.

5.5 Component Selection Guide

This design guide provides a high-level explanation of the steps necessary to create a power converter. It is assumed you are familiar with many of the basic skills and techniques referenced in the following. In addition to this guide, a complete evaluation board that includes schematic, BOM, and an example PCB layout (see the Ordering Information) is provided.

5.5.1 Output Filter Design

The output inductor and the output capacitor bank together form a low-pass filter responsible for smoothing the pulsating voltage at the phase node. The filter must also provide the transient energy until the regulator can respond. Because the filter has low bandwidth relative to the switching frequency, it limits the system transient response. The output capacitors must supply or sink current while the current in the output inductor increases or decreases to meet the load demand.

5.5.2 Output Capacitor Selection

The critical load parameters in choosing the output capacitors are the maximum size of the load step (ΔI_{STEP}), the load-current slew rate (di/dt), and the maximum allowable output voltage deviation under transient loading (ΔV_{MAX}). Capacitors are characterized according to their capacitance, Equivalent Series Resistance (ESR), and Equivalent Series Inductance (ESL).

At the beginning of a load transient, the output capacitors supply all of the transient current. The output voltage initially deviates by an amount approximated by the voltage drop across the ESL. As the load current increases, the voltage drop across the ESR increases linearly until the load current reaches its final value. Neglecting the contribution of inductor current and regulator response, the output voltage initially deviates by an amount shown in Equation 11.

$$(EQ. 11) \quad \Delta V_{MAX} \approx \left[ESL \times \frac{di}{dt} \right] + [ESR \times \Delta I_{STEP}]$$

The filter capacitors selected must have sufficiently low ESL and ESR such that the total output voltage deviation is less than the maximum allowable ripple.

Most capacitor solutions rely on a mixture of high frequency capacitors with relatively low capacitance in combination with bulk capacitors having high capacitance but larger ESR. Minimizing the ESL of the high-frequency capacitors allows them to support the output voltage as the current increases. Minimizing the ESR of the bulk capacitors allows them to supply the increased current with less output voltage deviation.

Ceramic capacitors with X7R dielectric are recommended. Alternately, a combination of low ESR solid tantalum capacitors and ceramic capacitors with X7R dielectric can be used.

The ESR of the bulk capacitors is responsible for most of the output voltage ripple. As the bulk capacitors sink and source the inductor AC ripple current, a voltage, $V_{P-P(MAX)}$, develops across the bulk capacitor according to Equation 12.

$$(EQ. 12) \quad V_{P-P(MAX)} = ESR \times \left[\frac{(V_{IN} - V_{OUT})V_{OUT}}{L_{OUT} \times f_s \times V_{IN}} \right]$$

In addition to ESL and ESR, another consideration in selecting the output capacitors is loop stability. The total output capacitance sets the dominant pole of the PWM. Because the ISL71001SLHM uses integrated compensation techniques, it is necessary to restrict the output capacitance to optimize loop stability. The recommended load capacitance is estimated using [Equation 13](#).

$$(EQ. 13) \quad C_{OUT} = 75\mu F \times \text{Number of LXx Pins Connected} \times \frac{1.8V}{V_{OUT}}$$

Another stability requirement on the selection of the output capacitor is that the ESR zero (f_{ZESR}) is placed at 60kHz to 90kHz. This range is set by an internal, single compensation zero at 8.6kHz. This ESR zero location contributes to an increased phase margin of the control loop; therefore, if a capacitor is chosen with an inadequate ESR, stability can be compromised. [Equation 14](#) calculates the required ESR to place the ESR zero in the recommended range:

$$(EQ. 14) \quad ESR = \frac{1}{2\pi(f_{ZESR})(C_{OUT})}$$

In conclusion, the output capacitors must meet three criteria:

- They must have sufficient bulk capacitance to sustain the output voltage during a load transient while the output inductor current is slewing to the value of the load transient.
- The ESR must be sufficiently low to meet the desired output voltage ripple because of the output inductor current.
- The ESR zero should be placed in a rather large range to provide additional phase margin.

5.5.3 Output Inductor Selection

When the output capacitors are selected, the maximum allowable ripple voltage ($V_{P-P(MAX)}$) determines the lower limit on the inductance as shown in [Equation 15](#).

$$(EQ. 15) \quad L_{OUT} \geq ESR \times \left[\frac{(V_{IN} - V_{OUT})V_{OUT}}{f_s \times V_{IN} \times V_{P-P(MAX)}} \right]$$

Because the output capacitors are supplying a decreasing portion of the load current while the regulator recovers from the transient, the capacitor voltage becomes slightly depleted. The output inductor must be capable of assuming the entire load current before the output voltage decreases more than ΔV_{MAX} . This places an upper limit on inductance.

[Equation 16](#) gives the upper limit on output inductance for the case when the trailing edge of the current transient causes a greater output voltage deviation than the leading edge. [Equation 17](#) addresses the leading edge.

Normally, the trailing edge dictates the inductance selection because duty cycles are usually <50%. Nevertheless, evaluate both inequalities and govern inductance based on the lower of the two results. In each equation, L_{OUT} is the output inductance, C_{OUT} is the total output capacitance, and $\Delta I_{L(P-P)}$ is the peak-to-peak ripple current in the output inductor.

$$(EQ. 16) \quad L_{OUT} \leq \frac{2 \cdot C_{OUT} \cdot V_{OUT}}{(\Delta I_{STEP})^2} \left[\Delta V_{MAX} - (\Delta I_{L(P-P)} \cdot ESR) \right]$$

$$(EQ. 17) \quad L_{OUT} \leq \frac{2 \cdot C_{OUT}}{(\Delta I_{STEP})^2} \left[\Delta V_{MAX} - (\Delta I_{L(P-P)} \cdot ESR) \right] (V_{IN} - V_{OUT})$$

Another concern when selecting an output inductor is ensuring there is adequate slope compensation when the regulator is operated above 50% duty cycle. Because the internal slope compensation is fixed, output inductance should satisfy [Equation 18](#) to ensure this requirement is met.

$$(EQ. 18) \quad L_{OUT} \geq \frac{4.32\mu H}{\text{Number of LXx Pins Connected}}$$

5.5.4 Input Capacitor Selection

Input capacitors are responsible for sourcing the AC component of the input current flowing into the switching power devices. Their RMS current capacity must be sufficient to handle the AC component of the current drawn by the switching power devices, which is related to duty cycle. The maximum RMS current required by the regulator is closely approximated by [Equation 19](#).

$$(EQ. 19) \quad I_{RMS_MAX} = \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(I_{OUT(MAX)}^2 + \frac{1}{12} \times \left(\frac{V_{IN} - V_{OUT}}{L_{OUT} \times f_s} \times \frac{V_{OUT}}{V_{IN}} \right)^2 \right)}$$

The important parameters to consider when selecting an input capacitor are the voltage rating and the RMS ripple current rating. For reliable operation, select capacitors with voltage ratings at least 1.5x greater than the maximum input voltage. The capacitor RMS ripple current rating should be higher than the largest RMS ripple current required by the circuit.

Ceramic capacitors with X7R dielectric are recommended. Alternately, a combination of low ESR solid tantalum capacitors and ceramic capacitors with X7R dielectric can be used. The ISL71001SLHM requires a minimum effective input capacitance of 100μF for stable operation.

6. PCB Design

PCB design is critical to high-frequency switching regulator performance. Careful component placement and trace routing are necessary to reduce voltage spikes and minimize undesirable voltage drops. Selection of a suitable thermal interface material is also required for optimum heat dissipation and to provide lead strain relief.

6.1 PCB Plane Allocation

Four layers of 2 oz. copper are recommended. Layer 2 should be a dedicated ground plane with all critical component ground connections made with vias to this layer. Layer 3 should be a dedicated power plane split between the input and output power rails. Layers 1 and 4 should be used primarily for signals but can also provide additional power and ground islands, as required.

6.2 PCB Component Placement

Place components as close as possible to the IC to minimize stray inductance and resistance. Prioritize the placement of bypass capacitors on the pins of the IC in the order shown: REF, SS, AVDD, DVDD, PVINx (high frequency capacitors), EN, PGOOD, PVINx (bulk capacitors).

Locate the output voltage resistive divider as close as possible to the FB pin of the IC. Connect the top leg of the divider directly to the POL (Point of Load) and connect the bottom leg of the divider directly to AGND. Connect the junction of the resistive divider directly to the FB pin.

A small series R-C snubber connected from the LXx pins to the PGNDx pins can be used to damp high frequency ringing on the LXx pins, if required (see [Figure 29](#)).

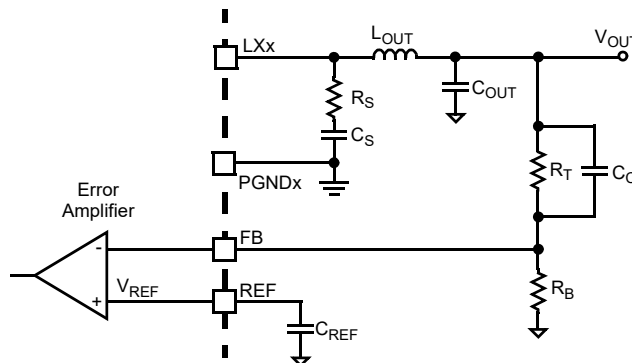


Figure 29. R-C Snubber

6.3 PCB Layout

Use a small island of copper to connect the LXx pins of the IC to the output inductor on Layers 1 and 4. To minimize capacitive coupling to the power and ground planes, void the copper on Layers 2 and 3 adjacent to the island.

Keep all other signal traces as short as possible.

6.4 Package Thermal Management

For optimum thermal performance, place a pattern of vias and a thermal land on the top layer of the PCB directly underneath the EPAD. Connect the vias to the plane which serves as a heatsink. To ensure good thermal contact, use solder to connect the EPAD to the thermal land on the PCB. The ISL71001SLHM weighs 0.29 grams.

7. Package Outline Drawing

The package outline drawing is located at the end of this document and is accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

8. Ordering Information

Part Number ^{[1][2]}	Part Marking	Radiation Tolerance (Total Ionizing Dose)	Package Description ^[3] (RoHS Compliant)	Pkg. Dwg. #	Carrier Type	Temp. Range
ISL71001SLHMNZ	ISL71001 SLHMNZ	LDR to 75krad(Si)	64 Ld ePAD TQFP	Q64.10x10J	Tray	-55 to +125°C
ISL71001MEVAL1Z	Evaluation Board					

1. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu-Ag plate -e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. For Moisture Sensitivity Level (MSL), see the [ISL71001SLHM](#) product page. For more information about MSL, see [TB363](#).
3. For the Pb-Free Reflow Profile, see [TB493](#).

9. Revision History

Revision	Date	Description
1.02	Oct 24, 2025	Applied latest template. Corrected Revision format. Updated description on page 1. Updated features bullets. Updated EC Spec boilerplate and bolded min/max limits. Updated POD to the latest revision. Added ECAD Information.
1.01	Aug 10, 2021	In Ordering Information table, updated Note 2 to provide more navigation details for customers.
1.00	Jun 2, 2021	Initial release.

A. ECAD Design Information

This information supports the development of the PCB ECAD model for this device. It is intended to be used by PCB designers.

A.1 Part Number Indexing

Orderable Part Number	Number of Pins	Package Type	Package Code/POD Number
ISL71001SLHMNZ	64	EP-TQFP	Q64.10x10J/PT0064AA

A.2 Symbol Pin Information

A.2.1 64-EP-TQFP

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	M/S	Input	-
2	DGND	Power	-
3	DGND	Power	-
4	DGND	Power	-
5	PGOOD	Output	-
6	SS	Passive	-
7	NC	Passive	-
8	DVDD	Power	-
9	DVDD	Power	-
10	DVDD	Power	-
11	DGND	Power	-
12	DGND	Power	-
13	DGND	Power	-
14	AGND	Power	-
15	AGND	Power	-
16	NC	Passive	-
17	NC	Passive	-
18	AVDD	Power	-
19	REF	Passive	-
20	FB	Input	-
21	EN	Input	-
22	PORSEL	Input	-
23	NC	Passive	-
24	PVIN6	Power	-
25	PVIN6	Power	-
26	LX6	Power	-
27	LX6	Power	-
28	PGND6	Power	-
29	PGND6	Power	-
30	PGND5	Power	-
31	PGND5	Power	-
32	NC	Passive	-
33	NC	Passive	-
34	LX5	Power	-
35	LX5	Power	-
36	PVIN5	Power	-
37	PVIN5	Power	-
38	PVIN4	Power	-
39	PVIN4	Power	-
40	LX4	Power	-
41	LX4	Power	-
42	PGND4	Power	-
43	PGND4	Power	-

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
44	PGND3	Power	-
45	PGND3	Power	-
46	LX3	Power	-
47	LX3	Power	-
48	NC	Passive	-
49	NC	Passive	-
50	PVIN3	Power	-
51	PVIN3	Power	-
52	PVIN2	Power	-
53	PVIN2	Power	-
54	LX2	Power	-
55	LX2	Power	-
56	PGND2	Power	-
57	PGND2	Power	-
58	PGND1	Power	-
59	PGND1	Power	-
60	LX1	Power	-
61	LX1	Power	-
62	PVIN1	Power	-
63	PVIN1	Power	-
64	SYNC	I/O	-
EPAD65	GND	Power	-

A.3 Symbol Parameters

Orderable Part Number	Qualification	Radiation Qualification	LDR	Mounting Type	RoHS	Min Operating Temperature	Max Operating Temperature	Min Input Voltage	Max Input Voltage	Switching Frequency
ISL71001SLHMNZ	Space	QML Class V Equiv.	75 krad(Si)	SMD	Compliant	-55 °C	125 °C	3 V	5.5 V	1 MHz

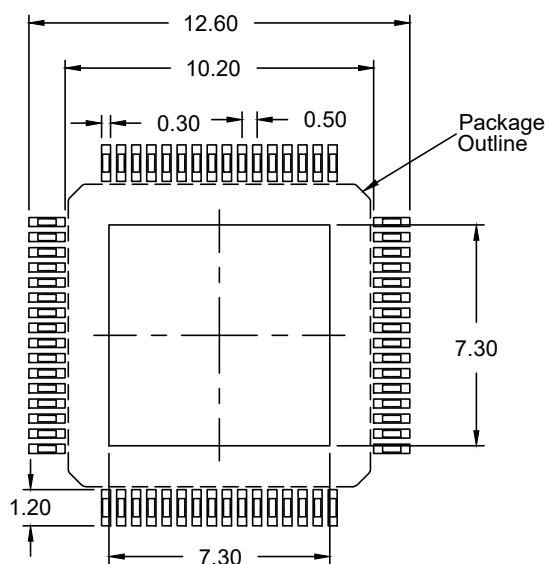
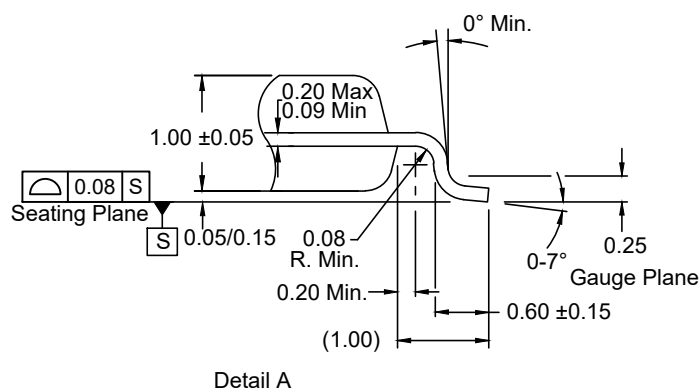
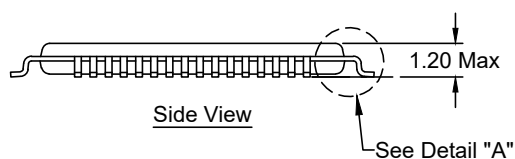
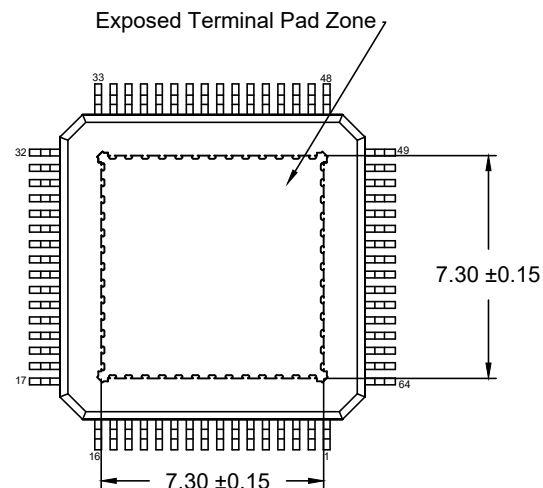
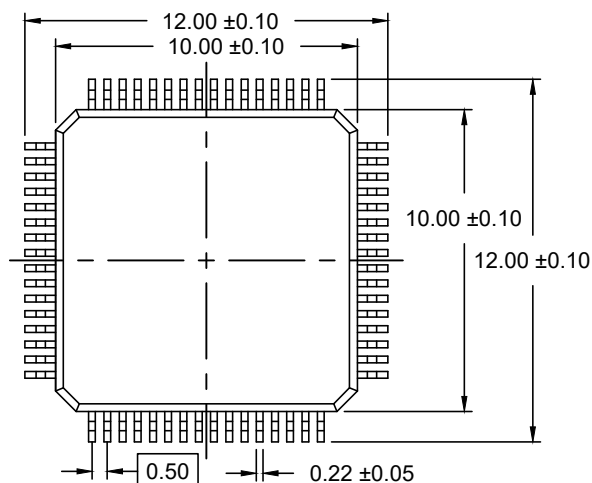
A.4 Footprint Design Information

A.4.1 64-EP-TQFP

IPC Footprint Type	Package Code/ POD Number	Number of Pins
QFP	Q64.10x10J/PT0064AA	64

Description	Dimension	Value (mm)	Diagram
Minimum lead span (vertical side)	Dmin	11.90	<p>Bottom View</p> <p>Side View</p>
Maximum lead span (vertical side)	Dmax	12.10	
Minimum lead span (horizontal side)	Emin	11.90	
Maximum lead span (horizontal side)	Emax	12.10	
Minimum body span (vertical side)	D1min	9.90	
Maximum body span (vertical side)	D1max	10.10	
Minimum body span (horizontal side)	E1min	9.90	
Maximum body span (horizontal side)	E1max	10.10	
Minimum Lead Width	Bmin	0.17	
Maximum Lead Width	Bmax	0.27	
Number of pins (vertical side)	PinCountD	16	
Number of pins (horizontal side)	PinCountE	16	
Distance between the center of any two adjacent pins	Pitch	0.50	
Location of pin 1; S2 = corner of D side, C1 = center of E side	Pin1	S2	
Minimum thermal pad size (vertical side)	D2min	7.15	
Maximum thermal pad size (vertical side)	D2max	7.45	
Minimum thermal pad size (horizontal side)	E2min	7.15	
Maximum thermal pad size (horizontal side)	E2max	7.45	
Minimum Lead Length	Lmin	0.45	
Maximum Lead Length	Lmax	0.75	
Maximum Height	Amax	1.20	
Minimum Standoff Height	A1min	0.05	
Minimum Lead Thickness	cmin	0.09	
Maximum Lead Thickness	cmax	0.20	

Recommended Land Pattern			Diagram
Description	Dimension	Value (mm)	<p>PCB Top View</p>
Distance between left pad toe to right pad toe (horizontal side)	ZE	12.60	
Distance between top pad toe to bottom pad toe (vertical side)	ZD	12.60	
Distance between left pad heel to right pad heel (horizontal side)	GE	10.20	
Distance between top pad heel to bottom pad heel (vertical side)	GD	10.20	
Pad Width	X	0.30	
Pad Length	Y	1.20	



Notes:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ± 0.05 mm for the non-toleranced dimensions.
4. Foot length is measured at gauge plane 0.25 mm above seating plane.

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