

Boot-up Configuration

| Device 8-bit I ² C Address | Default Configuration |
|---------------------------------------|-----------------------|
| 0xd8 | OTP |

Inputs

| Crystal Frequency | Input CLK0 | Input CLK1 |
|-------------------|------------|------------|
| 49.152MHz | — | — |

Outputs

| Output | Frequency (MHz) | Type | Enable | Polarity | Voltage | Source | Divider | Err |
|--------|-----------------|--------|----------|----------|---------|--------|---------|-----|
| Q0 | — | LVPECL | Disabled | Normal | 3.3 | PLL | — | — |
| Q1 | — | LVPECL | Disabled | Normal | 3.3 | PLL | — | — |
| Q2 | — | LVPECL | Disabled | Normal | 3.3 | PLL | — | — |
| Q3 | — | LVPECL | Disabled | Normal | 3.3 | PLL | — | — |

PLL

| Frequency | Mode | Acquire BW | Lock BW | CLK0 PFD | CLK1 PFD |
|-----------|-------------|------------|---------|----------|----------|
| — | Synthesizer | 25Hz | 25Hz | — | — |

GPIOs

| GPIO0 | GPIO1 | GPIO2 | GPIO3 |
|--------|--------|---------|--------|
| In-OE0 | In-OE1 | In-CSEL | In-GPI |

[illegible]

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| 00 00 00 00 85 00 00 9C 01 D4 02 71 00 00 00 00 |
| 00 83 00 10 02 08 8C |

Revision History

Table 1. Revision History

| Revision Date | Description of Change |
|---------------|-----------------------|
| July 12, 2017 | Initial release. |

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