





THE NEXT-GENERATION PROCESSOR TO MEET THE NEEDS OF THE SMART SOCIETY HAS ARRIVED.



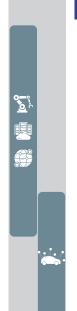
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The utilization of intelligent technology is advancing in all aspects of our lives, including electric household appliances, industrial equipment, building management, power grids, and transportation. The cloud-connected "smart society" is coming ever closer to realization. Microcontrollers are now expected to provide powerful capabilities not available previously, such as high-performance and energy-efficient control combined with interoperation with IT networks, support for human-machine interfaces, and more. To meet the demands of this new age, Renesas has drawn on its unmatched expertise in microcontrollers to create the RZ family of embedded processors. The lineup of these "next-generation processors that are as easy to use as conventional microcontrollers" to meet different customer requirements.

The Zenith of the Renesas micro

As embedded processors to help build the next generation of advanced products, the RZ family offers features not available elsewhere and brings new value to customer applications.

Positioning of the RZ Family



Microcontrollers & Microprocessors, System-on-Chips (SoCs)

RENESAS

High-end 32/64-bit MPUs

High-resolution HMI, Industrial network & real-time control



Advanced 32-bit MCUs

Arm ecosystem, Advanced security, Intelligent IoT



High Power Efficiently 32-bit MCUs Motor control, Capacitive touch, Functional safety, GUI

RISC-V products

General-purpose 64-bit MPUs (RZ/Five Group) Application-specific 32-bit MCUs



Ultra-low Energy 8/16-bit MCUs Bluetooth® Low Energy, SubGHz, LoRa®-based Solutions Automotive actuators & sensors, Low-end ECUs



Automotive 32-bit MCUs

Rich functional safety and embedded security features



Automotive SoCs

Next generation of automotive computing

Analog and Power Devices

- Analog products
- Clocks & Timing
- Interface & Connectivity
- Memory & Logic
- Power & Power management
- Programmable Mixed-signal, ASIC, & IP products
- RF products
- Sensor products
- Space & Harsh environment

- Timing
- Wireless Power
- Battery Management
- Power Devices
- Power Management
- Sensors
- Video & Display



RZ Family Portfolio

RZ/V Series

64-bit Cortex®-A CPU, Up to 1.8GHz Low-power Embedded AI for Vision-AI Application

RZ/N Series

32/64-bit Cortex®-A/R/M CPU, Up to 1.2GHz Multi-protocol Industrial Network and TSN for PLC, Remote IO, Gateway

RZ/T Series

32/64-bit Cortex®-A/R/M CPU, Up to 1.2GHz Real-time Control Multi-protocol Industrial Network and TSN, Multi-protocol Encoder I/F for AC servo, Actuator, Inverter

RZ/G Series

32/64-bit Cortex®-A CPU, Up to 1.5Hz 64-bit RISC-V CPU, Up to 1.0GHz for HMI and IoT Application

RZ/A Series

32/64-bit Cortex®-A CPU, Up to 1GHz

- DDR3L/4 (RZ/A3UL)
- Up to 10MB Embedded RAM for HMI Application

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Linux / Android™ / Multi-OS with RTOS **RTOS Vision Al** RZ/V2M RZ/V2H **RZ/V Series** 1.0GHz Dual-core Cortex-A53, DRP-AI(576-MAC), 4K-ISP 1.8GHz Quad-core Cortex-A55, DRP-AI3(4K-MAC), 4K-ISP, 3D-GPU RZ/V2MA RZ/V2N 1.0GHz Dual-core Cortex-A53, 1.8GHz Quad-core Cortex-A55, DRP-AI(576-MAC), OpenCV Accelerator DRP-AI3(2K-MAC), 4K-ISP,3D-GPU RZ/V2L 1.2GHz Dual-core Cortex-A55, DRP-AI(576-MAC), 3D-GPU **Industrial** RZ/N2H RZ/N1D RZ/N1S RZ/N2L 1.2GHz Quad-core Cortex-A55 500MHz Dual-core Cortex-A7, 500MHz Cortex-A7,125MHz Cortex-M3, 400MHz Cortex-R52, Network 1.0GHz Dual-core Cortex-R52 125MHz Cortex-M3, Industrial Ethernet Industrial Ethernet Industrial Ethernet Industrial Ethernet, 6-axis Motor Control RZ/N1L 125MHz Cortex-M3, Industrial Ethernet RZ/T2H RZ/T2ME **Real-time** 1.2GHz Quad-core Cortex-A55, 1.0GHz Dual-core Cortex-R52, 800MHz Dual-core Cortex-R52, 2-axis Motor Control, Industrial Ethernet, Control axis Motor Control, Industrial Ethernet OTFD **RZ/T Series** RZ/T1 RZ/T2M 600MHz Cortex-R4, 150MHz Cortex-M3, 1-axis Motor Control, Industrial Ethernet 800MHz Dual-core Cortex-R52, 2-axis Motor Control, Industrial Ethernet RZ/T2L 800MHz Cortex-R52, 2-axis Motor Control, EtherCAT **IoT Edge** RZ/G3S **RZ/Five** 1.1GHz Cortex-A55, 250MHz Dual-core RISC-V, 1.0GHz AX45MP, DDR4/3L, **RZ/G Series** Cortex-M33, LPDDR4/DDR4 GbEthernet, CAN-FD HMI RZ/G1H RZ/G2H RZ/A1H RZ/A2M 1.4GHz Quad-core Cortex-A15 + Cortex-A7, DDR3, 3DG, H.264 1.5GHz Quad-core Cortex-A57 + Cortex-A53, LPDDR4, 3DG, H.264/5 400MHz Cortex-A9, 10MB RAM, LCDC, JPEG, Ethernet, USB 528MHz Cortex-A9, 4MB RAM, LCDC, JPEG, MIPI-CSI, Ethernet, USB **RZ/G Series RZ/A Series** RZ/G1M RZ/G2M RZ/A1M RZ/A3UL 1.0GHz Cortex-A55, DDR4/3L, 1.5GHz Dual-core Cortex-A15, 1.5GHz Dual-core Cortex-A57 + Cortex-A53, 400MHz Cortex-A9, 5MB RAM, DDR3L, 3DG, H.264 LPDDR4, 3DG, H.264/5 LCDC, JPEG, Ethernet, USB LCDC, GbEthernet, USB RZ/G1N RZ/G2N RZ/A1LU 1.5GHz Dual-core Cortex-A15, 1.5GHz Dual-core Cortex-A57, 400MHz Cortex-A9, 3MB RAM, LPDDR4, 3DG, H.264/5 DDR3L, 3DG, H,264 LCDC, JPEG, Ethernet, USB RZ/G1E RZ/G2E RZ/A1L 1.0GHz Dual-core Cortex-A7, DDR3, 3DG, H.264 400MHz Cortex-A9, 3MB RAM, 1.2GHz Dual-core Cortex-A53, DDR3L, 3DG, H.264/5 LCDC, Ethernet, USB RZ/G2L RZ/A1LC 1.2GHz Dual-core Cortex-A55, 400MHz Cortex-A9, 2MB RAM, DDR4/3L, 3DG, H.264, CAN-FD LCDC. Ethernet, USB RZ/G2LC 1.2GHz Dual-core Cortex-A55, DDR4/3L, 3DG, CAN-FD RZ/G2UL 1.0GHz Cortex-A55 DDR4/3L, CAN-FD, ADC

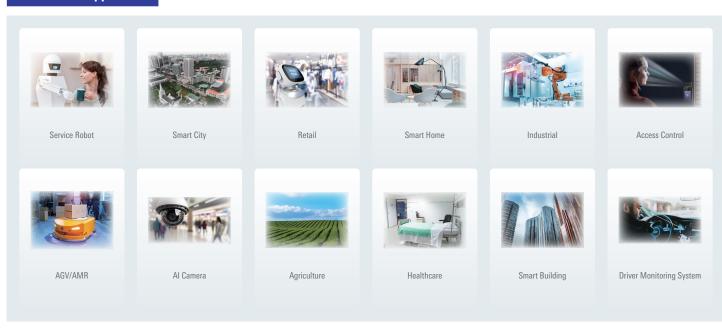


RZ/V Series

RZ/V Series Features

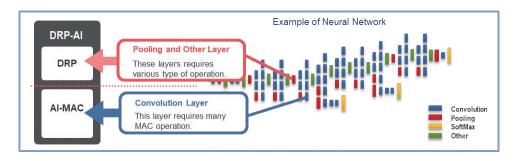
- Al performance scalability to cover wide range of applications
- Integrates Renesas original AI accelerator DRP-AI to deliver up to 80TOPS
- Realize best AI power efficiency up to 10TOPS/W
- Integrated ISP (upto 4k) and Video Codec
- Provides Vision Processing Accelerator (OpenCV) as DRP library
- Equipped with a 3D Graphics Engine for fast image rendering
- * DRP: Dynamically Reconfigurable Processor

RZ/V Series Application



Features of DRP-AI

DRP-Al consists of Al-MAC (multiply-accumulate processor) and DRP (reconfigurable processor). All processing can be executed at high speed by assigning Al-MAC for operations on the convolution layer and fully connected layer, and DRP for other complex processing such as preprocessing and pooling layer.

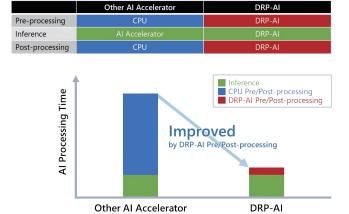


For more detailed technical information on DRP-AI, please refer to the following white paper.

White Paper: Embedded Al-Accelerator DRP-Al ☐

Next Generation Highly Power-Efficient Al Accelerator (DRP-Al3): 10x Faster Embedded Processing in Advanced Al for Autonomous Systems 🔀

While most Al accelerators specialize only in Al inference and rely on the CPU for pre- and post-processing, DRP-Al integrates pre- and post-processing and Al inference into a single DRP-Al hardware to achieve superior Al processing performance.



RZ/V Series Specification

Items	RZ/V2H	NEW RZ/V2N	RZ/V2L	RZ/V2M	RZ/V2MA
Main CPU	Cortex-A55 × 4 Cortex-R8 × 2	Cortex-A55 × 4	Cortex-A55 × 2	Cortex-A53 × 2	Cortex-A53 × 2
Sub CPU	Cortex-M33	Cortex-M33	Cortex-M33	-	-
Al Accelerator Performance (DRP-Al)	10 TOPS/W Max. 80 TOPS (Sparse model) Resnet50: 830 Inference/Sec	10 TOPS/W Max. 15 TOPS (Sparse model) Resnet50: 769 Inference/Sec	1 TOPS/W Max. 0.5 TOPS Resnet50: 17 Inference/Sec	1 TOPS/W Max. 1 TOPS Resnet50: 28 Inference/Sec	1 TOPS/W Max. 1 TOPS Resnet50: 28 Inference/Sec
ISP for Camera	4K ISP (option) (hardware)	4K ISP (option) (hardware)	Simple ISP (software)	4K ISP (hardware)	_
MIPI CSI-2 I/F	4-lane × 4ch	4-lane × 2ch	4-lane × 1ch	4-lane × 2ch	_
Computer Vision Accelerator	OpenCV Accelerator	OpenCV Accelerator	OpenCV Accelerator	_	OpenCV Accelerator
Video Codec	H.265, H.264	H.265, H.264	H.264	H.265, H.264	H.265, H.264
Graphics	3D Graphics (option)	3D Graphics (option)	3D Graphics	2D Graphics	-
Package	1368-pin FCBGA, 19mm × 19mm 0.5mm ball pitch	840-pin FCBGA, 15mm × 15mm 0.5mm ball pitch	551-pin PBGA, 21mm × 21mm 0.8mm ball pitch 456-pin PBGA, 15mm × 15mm 0.5mm ball pitch	841-pin FCBGA, 15mm × 15mm 0.5mm ball pitch	841-pin FCBGA, 15mm × 15mm 0.5mm ball pitch



Features of ISP

Supports ISP function to realize Vision System

ISP Comparison Table

Item		RZ/V2H	NEW RZ/V2N	RZ/V2L	RZ/V2M
ISP		H/W ISP Arm Mali™-C55 ISP	H/W ISP Arm Mali™-C55 ISP	S/W ISP Simple ISP by DRP library	H/W ISP 3rd party IP
Maximum Re	solution	Up to 4K	Up to 4K	Up to 5M	Up to 4K
Support CMOS Sensor		User's choice	User's choice	User's choice	Select from IMX415, IMX462, IMX568, AR1335
Camera I/F		4× MIPI CSI-2 (4-lane)	2× MIPI CSI-2 (4-lane)	1× MIPI CSI-2 (4-lane), 1× Parallel	2× MIPI CSI-2 (4-lane)
	ISP H/W Specifications	✓	✓	✓	_
Deliverables	Driver/API Specifications	✓	✓	✓	✓
Deliverables	Software	✓	✓	✓	✓
	Image Tuning Tool	✓	✓	✓	✓

ISP Function

ltem	RZ/V2H	NEW RZ/V2N	RZ/V2L	RZ/V2M
Support Image Size	3840 × 2160 p × 30 fps × 2 1920 × 1080 p × 60 fps × 2	3840 × 2160 p × 30 fps 1920 × 1080 p × 30 fps × 2	1920 × 1080 p × 15 fps	3840 × 2160 p × 30 fps 1920 × 1080 p × 30 fps × 2
AE (Auto Exposure), AWB (Auto White Balance)	✓	√	✓	√
Black Level Correction	✓	✓	✓	✓
Demosaic	✓	✓	✓	✓
Flicker Correction	✓	✓		✓
Obtain Focus Analysis Results	✓	✓		✓
Tone Mapping Settings	✓	✓		✓
Wide Dynamic Range Correction	✓	✓		✓
Chromatic Aberration Correction	✓	✓	✓	✓
Purple Fringing Correction	✓	✓		✓
Shading Correction	✓	✓		✓
Sharpness Correction	✓	✓	✓	✓
2D Noise Reduction	✓	✓	✓	✓
3D Noise Reduction	✓	✓	✓	
JPEG Conversion				✓
Resize	✓ (Downscale only)	√ (Downscale only)	✓ (Downscale only)	✓

RZ/V2M Group

CPU

■ 2× Cortex-A53 (up to 1.0GHz)

Vision and AI

- Al Accelerator; DRP-Al at 1.0 TOPS/W class
- Image Signal Processor (ISP) of multi-stream available
- Camera Interface; 2× MIPI CSI-2
- Face and Human Detection Engine

Video and Graphics

- H.265/H.264 Multi Codec
- JPEG Codec Engine
- 2D Graphics Engine

Display Interface

■ HDMI 1.4a

Audio Interface

■ Serial Sound Interface × 1ch

Communication Interface

- SD Host × 2ch
- PCI-Express 2.0 (2-lane) × 1ch
- Gigabit Ethernet × 1ch
- USB3.1 Gen1 Host/Function × 1ch
- I²C Bus × 4ch
- CSI × 6ch
- UART × 2ch

Memory Interface

- eMMC 4.5.1 × 1ch
- 32-bit LPDDR4-3200 × 1ch

Security

Hardware Security Engine

■ RZ/V2M Group Block Diagram

System	CI	PU	Peripheral I/F
Arm Debugger (CoreSight™)	Arm® Cortex®-A53: 1GHz	Arm® Cortex®-A53: 1GHz	SDI (2ch)
DMAC (16ch)	L1 I\$: 32KB L1 D\$: 32KB		USB3.1 (1ch)
Power control	NEON FPU	NEON FPU	(Host/Peripheral)
Timers	L2\$: 5	512KB	PCIe Gen2 (2Lane)
Timer (32ch)	Mom	nories	Gbit Ethernet MAC (1ch)
` '	RAMA 200KB	RAMB 1MB	I2C (4ch)
PWM (16ch)	TIAIVIA 200KB	HAIND IIVD	CSI (6ch)
WDT (2ch)	Sensing an	d Analyzing	UART (2ch)
Image Sensor I/F		tor (DRP-AI)	GPI0
MIPI CSI-2 v1.2 (4-lane, 2ch)	General Processing Accelerator	Multi-target detection (Face, Person's body)	External Memory I/F
Display I/F	Video and	d Graphics	LPDDR4 (32-bit)
HDMI v1.4a TX (1ch)	Camera ISP	2D Graphics engine	eMMC (1ch)
Audio I/F	H.264/265 Multi Codec	JPEG Codec	Analog
I2S (1ch)	Sec	ADC (20ch,12bit)	
120 (1011)	Trusted	Temperature sensor (2ch)	

RZ/V2L Group

- 2× Cortex-A55 or 1× Cortex-A55 (up to 1.2GHz)
- 1× Cortex-M33 (up to 200MHz)

Vision and AI

- Al Accelerator; DRP-Al
 - * Image Signal Processor (Simple ISP) Function is provided as DRP Library
- Camera Interface; 1× MIPI CSI-2 / 1× Digital Parallel

Video and Graphics

- H.264 Codec
- 3D Graphics Engine

Display Interface

- MIPI DSI (4-lane)
- Digital Parallel

Audio Interface

■ Serial Sound Interface × 4ch

Communication Interface

- Gigabit Ethernet × 2ch
- USB2.0 Host × 1ch
- USB2.0 Host/Function × 1ch
- I²C Bus × 4ch
- SCI × 2ch
- UART × 5ch

Memory Interface

- SPI Multi I/O (8bit DDR) × 1ch
- SDHI (UHS-I) / eMMC × 1ch
- 16-bit DDR3L-1333/DDR4-1600 × 1ch

Security

■ Hardware Security Engine (Option)

■ RZ/V2L Group Block Diagram

	9					
System	C	PU		Peripheral I/F		
Arm Debugger (CoreSight™)	Arm® Cortex®-A55: 1.2GHz Arn	Arm® Cortex®-A55: 1.2GHz Arm® Cortex®-A55: 1.2GHz Arm®				
DMAC (16ch)	L1 I\$: 32KB L1 D\$: 32KB L1		Cortex® -M33	USB2.0 (Host, 1ch)		
Power control	NEON FPU I	NEON FPU	200MHz	USB2.0 (Host/Peripheral, 1ch)		
Timers	L3\$: 256KB v	v/ECC		Gbit Ethernet MAC (2ch)		
32-bit Timer (1ch)	Men	nories		I2C (4ch)		
16-bit Timer (8ch)		RKB w/ECC		SCI 8/9-bit (2ch)		
PWM (8ch)				SCIF(UART) (5ch)		
WDT (3ch)		Sensing and Analyzing				
	Al-accelera		CAN-FD (2ch)			
Image Sensor I/F	Video an	d Graphics		GPI0		
MIPI CSI-2 (4-lane, 1ch)	Image Scaling Unit (5M pixel)	3D GPU (Mali™	-G31)	External Memory I/F		
Parallel (HD-30fps, 1ch)	H.264 Enc/Dec (192	0 × 1080pixel, 30fps)		DDR3L/DDR4-1600 (16-bit)		
Display I/F	Security	/ (option)		SPI Multi I/O (8-bit DDR, 1ch)		
MIPI DSI (4-lane, 1ch)	Secure Boot	Device Unique	e ID	SDHI (UHS-I) / eMMC (1ch)		
Parallel (WXGA-60fps, 1ch)	Crypto Engine					
Audio I/F	TRNG	OTP 4K-bit	: 1	Analog		
SSI (I2S, 4ch)				12-bit ADC (8ch)		
SRC (1ch)				Thermal Sensor (1ch)		
0110 (1011)						



RZ/V2MA Group

CPU

■ 2× Cortex-A53 (up to 1.0GHz)

Vision and AI

- Al Accelerator; DRP-Al at 1.0 TOPS/W class
- OpenCV Accelerator (DRP)

Video and Graphics

H.265/H.264 Multi Codec

Communication Interface

- SD Host × 2ch
- PCI-Express 2.0 (2-lane) × 1ch
- Gigabit Ethernet × 1ch
- USB3.1 Gen1 Host/Function × 1ch
- I^2C Bus × 4ch
- CSI × 6ch
- UART × 2ch

Memory Interface

- eMMC 4.5.1 × 1ch
- 32-bit LPDDR4-3200 × 1ch

RZ/V2H Group

CPU

- 4× Cortex-A55 (up to 1.8GHz)
- 2× Cortex-R8 (up to 800MHz)
- 1× Cortex-M33 (up to 200MHz)

Vision and AI

- Al Accelerator: DRP-Al at 10TOPS/W class
- OpenCV Accelerator (DRP)
- Camera Interface: MIPI CSI-2 (1/2/4-lane) × 4ch Video and Graphics
- H.265/H.264 Multi Codec
- 3D Graphics Engine Mali-G31 (Option)
- Image Signal Processor (ISP) Mali-C55 (Option)
- Display OUT: MIPI DSI (1/2/4-lane) × 1ch

Communication Interface

- SD Host × 2ch
- PCI-Express 3.0 (4-lane × 1/2-lane × 2)
- Gigabit Ethernet × 2ch
- USB3.2 × 2ch, USB2.0 × 2ch

Memory Interface

- eMMC 4.5.1 × 1ch
- 32bit LPDDR4/4X-3200 \times 2ch

Security

Hardware Security Engine (Option)

■ RZ/V2MA Group Block Diagram

System	CI	Peripheral I/F	
Arm Debugger (CoreSight™)	Arm® Cortex®-A53: 1GHz	Arm® Cortex®-A53: 1GHz	SDI (2ch)
DMAC (16ch)	L1 I\$: 32KB L1 D\$: 32KB NEON FPU	L1 I\$: 32KB L1 D\$: 32KB NEON FPU	USB3.1 (1ch) (Host/Peripheral)
Timers	L2\$: 5	512KB	PCle Gen2 (2-lane)
Timer (32ch)		Gbit Ethernet MAC (1ch)	
PWM (16ch)		nories RAMB 1MB	IIC (4ch)
WDT (2ch)	RAMA 200KB	KAIVIB IIVIB	CSI (6ch)
Analog	Sensing an	d Analyzing	UART (2ch)
Temperature sensor (2ch)	Al-accelerator (DRP-AI)	Vision Accelerator (DRP)	GPI0
	Video H.264/265	External Memory I/F LPDDR4 (32-bit)	
			eMMC (1ch)

■ RZ/V2H Group Block Diagram

Svstem		СР	11		Interfaces
Arm Debugger		55 Arm® Cortex®-R8		Arm® Cortex®-M33	LPDDR4/4X w/ECC 32-bit × 2 (12.8GB/s × 2)
Arm Trust Zone	Quad 1.8GHz	Dual 80	JUIVIHZ	200MHz	xSPI (4. 8-bit DTR)
Interrupt Controller		L1:(I=32KB+D CM:(I=128KB+	=32KB)/core D=128KB)/core	FPU DSP extension	SDIO + eMMC × 1ch SDIO × 2ch
PLL / SSCG					0510 A 2011
Standby					USB3.2 (Gen2 × 1) - Host × 2ch
DMAC 80ch	Inter		red Mem	ory	USB2.0 - Host / Func. × 1ch
Event Link Controller	F	RAM 6M	B w/ECC		- Host × 1ch
					GbEthernet × 2ch
Timers	Al Accerelato	r	Dynamically	Reconfigurable Processor	PCIe Gen3 4-lane × 1/2-lane × 2
GPT × 16ch	DRP-AI3			DRP	IRO × 16ch
RTC					NMI
GTM (32-bit × 8ch)	10	91	0		I ³ C × 1ch
CMTW (32-bit × 8ch)			Graphics		1°C × 9ch
WDT × 4ch	GPU [Mali™ G31] (-	ali™ C55] (option)	SCIF × 1ch
	Camera IN: MIPI CSI-2 (1/2/4-	-lane) × 4ch	H.264	1/265 Enc./Dec.	RSCI(UART/SPI/I ² C host) × 10ch
Audio	Display OUT: MIPI DSI (1/2/4-	lane) × 1ch	Imag	e Scaling Unit	RSPI × 3ch
SSI (I ² S) TDM × 10ch					CAN-FD × 6ch
SPDIF × 3ch	Se	ecurity II	P (option)	GPIO × 86port
SCU / ADMAC	Secure Boot		101000	ice Unique ID	Analog
ADG	Crypto Engine	е	J	TAG Disable	12-bit 2.5Msps ADC × 8ch
PDM (input) × 6ch	TRNG		C	TP 32K-bit	Temp. Sensor × 2ch

RZ/V2N Group



- 4× Cortex-A55 (up to 1.8GHz)
- 1× Cortex-M33 (up tp 200MHz)
- Vision and AI
- Al Accelerator: DRP-Al at 10TOPS/W class
- Camera Interface: MIPI CSI-2 (1/2/4-lane) × 2ch Video and Graphics
- H.265/H.264 Multi Codec
- 3D Graphics Engine Mali-G31 (Option)
- Image Signal Processor (ISP) Mali-C55 (Option)
- Display OUT: MIPI DSI (1/2/4-lane) × 1ch

Communication Interface

- SD Host × 2ch
- PCI-Express 3.0 (2-lane × 1)
- Gigabit Ethernet × 2ch
- USB3.2 × 1ch, USB2.0 × 1ch

Memory Interface

- eMMC 4.5.1 × 1ch
- 32bit LPDDR4/4X-3200 × 1ch

Security

■ Hardware Security Engine (Option)

■ RZ/V2N Group Block Diagram

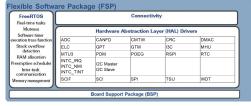
System	CF	บ	Interfaces
Arm Debugger	Arm® Cortex®-A55	Arm® Cortex®-M33	LPDDR4/4X w/ECC 32-bit × 1 (12.8GB/s × 1)
Arm Trust Zone	Quad 1.8GHz	200MHz	xSPI (4, 8-bit DTR)
Interrupt Controller	L1:(I=32KB+D=32KB)/core I3:1MB	FPU DSP extension	SDIO + eMMC × 1ch
PLL / SSCG	L3:1MB	DSP extension	SDIO × 2ch - SDIO: v3.0/UHS-I - eMMC: JEDEC 4.5.1
Standby			USB3.2 (Gen2 × 1)
DMAC (80ch)	Internal Sha	red Memory	- Host × 1ch
Event Link Controller	RAM 1.5N	/IB w/ECC	USB2.0 - Host / Func. × 1ch
Timers		GbEthernet × 2ch (IEEE1588)	
GPTW × 16ch	Al Acce		PCIe Gen3 2-lane x 1
RTC	DRP-AI3	15TOPS	IRQ × 16ch
OSTM (32-bit × 8ch)			NMI
<u> </u>	Video and	Graphics	I ³ C × 1ch
CMTW (32-bit × 8ch)	GPU [Mali™ G31] (option)	ISP [Mali™ C55] (option)	I²C × 9ch
WDT × 4ch	Camera IN: MIPI CSI-2 (1/2/4-lane) × 2ch	H.264/265 Enc./Dec.	SCIF × 1ch
	Display OUT: MIPI DSI (1/2/4-lane) × 1ch		RSCI(UART/SPI/I ² C host) × 10ch
Audio	Display Out. Will 1 Doi (1/2/4-laile) X Toli	illiage scalling offic	RSPI × 3ch
SSI (I ² C) TDM × 10ch			CAN-FD × 6ch
SPDIF × 3ch	Security I	GPIO × 86port	
ASRC / ADMAC	Secure Boot	Device Unique ID	Analog
ADG	Crypto Engine	JTAG Disable	12-bit 2.5Msps ADC × 24ch
PDM (input) × 6ch	TRNG	OTP 32K-bit	Temp. Sensor × 2ch

Code Generation Support: Flexible Software Package (FSP) + Smart Configurator (SC)

(Supported products: RZ/V2L, RZ/V2H, RZ/V2N)

The FSP includes everything you'll need to start developing software: board-dependent programs, peripheral function drivers, middleware, and documentation on how to use them.

Smart Configurator is a utility based on the concept of "combining software components freely." The intuitive GUI makes it easy to configure pins and FSP driver settings and to generate source code customized for your use case. It works together with integrated development environments such as e^2 studio.







Flexible Development Kits

These products are evaluation boards with RZ/V series configured as the key device and are capable of easily implementing software development such as camera sensor input image processing, low power consumption AI inference, video streaming, and etc.

■ RZ/V2H Evaluation Board Kit



- P/N: RTK0EF0168C04000BJ
- LPDDR4X: 8GB × 2
- xSPI Flash Memory: 64MB
- micro SD × 2
- High Speed Interface
 - Gigabit Ethernet \times 2
- USB3.2 Gen × 2 (Host)
- USB2.0 \times 2 (OTG \times 1, Host-only \times 1)
- PCle Gen3 × 1 (4-lane) (Root Complex)
- MIPI CSI-2 Camera Interface × 4
- MIPI DSI Display Interface × 1

■ RZ/V2N Evaluation Board Kit NEW



- P/N: RTK0EF0186C03000BJ
- LPDDR4X: 8GB × 1
- xSPI Flash Memory: 64MB
- eMMC × 1 or micro SD × 1
- micro SD × 1
- High Speed Interface
 - Gigabit Ethernet × 2
- USB3.2 Gen × 1 (Host)
- USB2.0 \times 1 (OTG)
- PCIe Gen3 × 1 (2-lane) (Root Complex)
- MIPI CSI-2 Camera Interface × 2
- $-\,$ MIPI DSI Display Interface $\times\,1$

■ RZ/V2L Evaluation Board Kit



- P/N: RTK9754L23S01000BE
- P/N: RTK9754L27S01000BE (Secure Type)
- DDR4 SDRAM: 2GB
- eMMC: 64GB
- QSPI NOR Flash: 512MB
- microSD × 1
- A/D Converter Interface

■ RZ/V2M Evaluation Board Kit



- P/N: V2M EVK
- CMOS image sensor equipped board included (SONY/IMX415, CS mount equipped)
- LPDDR4: 32Gbit
- eMMC: 16GB
- HDMI Type-A × 1
- USB3.1 Gen1 Type-C × 1
- microSD × 1

■ RZ/V2MA Evaluation Board Kit

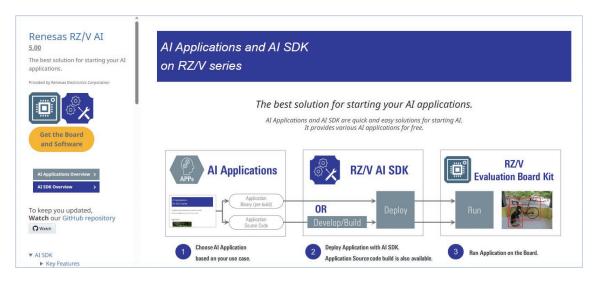


- P/N: SBEV-RZ/V2MA-KIT
- LPDDR4: 32Gbit
- eMMC: 16GB
- Ethernet × 1
- USB3.1 Gen1 Type-C × 1
- microSD × 1
- PCle × 4 slot (2-lane available)

"Easy to Use" with AI SDK



AI SDK eliminates complex build tasks and enables immediate AI evaluation



The customers only need to select their use case w/o requiring AI training. Provided as a free Open-Source Software on Github and can be used in MP.

■ Agriculture





■ Smart Building





■ Smart City





■ Smart Home





Industrial





Retail





■ Healthcare







RZ/N Series

RZ/N Series Features

- 1. Provides optimized microcontrollers for a variety of industrial network applications
- 2. Integrated Ethernet switch and EtherCAT slave controller alongside support for major Industrial Ethernet protocols and TSN
- 3. Redundant network configuration reduces network downtime to zero

1. Provides optimized microcontrollers for a variety of industrial network applications

The RZ/N2H is optimized for industrial controller equipment such as PLC, DCS, CNC and motion controller. It integrates Quad Arm® Cortex®-A55 cores (1.2GHz) for application processing and two Arm Cortex-R52 cores (1.0GHz) for real-time control. The flexible Ethernet functionalities supporting TSN execute both industrial Ethernet controller and device. Also, RZ/N2H can support up to 6-axis motor control, suitable for applications requiring multi-axis.

The RZ/N2L is optimized for the role of dedicated network companion chip, simplifying the task of adding network functionality to industrial equipment. Since it handles network-related processing independently of the external CPU, Industrial Ethernet support can be implemented without the need to make major changes to the existing application software.

RZ/N2 Specification

ltem	RZ/N2H	RZ/N2L
Application Core	Cortex-A55 1.2GHz ×4	-
Realtime Core	Cortex-R52 1.0GHz ×2	Cortex-R52 400MHz
DDR	LPDDR4-3200 32-bit	_
Industrial Ethernet	4 Ether ports 3 GMAC Ethernet Switch ESC, TSN	3 Ether ports 1 GMAC Ethernet Switch ESC, TSN
Motor Control	Up to 6-axis	-
PCle	PCIe (Gen3) ×2	-
HMI	Parallel RGB	-
Host IF	Serial	Serial / Parallel
Package	FCBGA 576-pin (23mm × 23mm)	FBGA 225-pin (23mm × 23mm) FBGA 121-pin (10mm × 10mm)

2. Integrated Ethernet switch and EtherCAT slave controller alongside support for major Industrial Ethernet protocols and TSN

A wide range of Industrial Ethernet protocols are supported. Separating application processing and network processing allows for more efficient application control.



	CUSTOMER Application								
RT/						CoE, EoE, FoE, SoE	Modbus/ RTU, ASCII Modbus	CAN Open	
	EtherCAT SSC TCP/IP, UDP/IP, PTP control, TDMA control						SSC	PROFIBUS PROFIT®	Device Net Device Net
	Driver Ether CAT					Driver	Driver		
	Slave Gigabit Ether MAC, Gigabit TSN Switch Controller						UART Contro ll er	CAN Contro ll er	
	Ether PHY					RS-485 transceiver	CAN transceiver		

3. Redundant network configuration reduces network downtime to zero

Advanced redundant network configuration support helps eliminate network downtime.

- Redundant network connections: Parallel Redundancy Protocol (PRP)
- Looped network connections: HSR (High-availability Seamless Redundancy), DLR (Device Level Ring), RSTP (Rapid Spawning Trees)

RZ/N Series Application





RZ/N2H Group

CPU core

- Arm® Cortex®-A55, Quad/Dual/Single-core Max operating frequency: 1.2GHz L1 I/D-cache 32KB per core, L3 cache 1MB
- Arm® Cortex®-R52, Dual-core
 Max operating frequency: 1.0GHz
 L1 I/D-cache 16KB,
 Tightly Coupled Memory (TCM): 512KB (w/ ECC) + 64KB (w/ ECC)
 per core

Features

- On-chip system SRAM 2.0MB (w/ ECC)
- LPDDR4-3200 32-bit
- SD/eMMC
- Motor Control Peripherals (Support up to 6-axis)
 - PWM Timer: MTU3 9ch PWM Timer: GPT 56ch $\Delta\Sigma$ interface: 23ch
 - 12-bit ADC: 3units - Encoder IF: 14ch
 - Trigonometric function unit
- Industrial Ethernet
 - Ethernet Switch w/ TSN
 - 3ch Gigabit Ethernet MAC w/ TSN
 - $-4 \times$ Ethernet ports
 - EtherCAT Slave Controller (ESC)
- PCI Express Gen3
- PGI Express della
- Serial host interface
- LCD Controller
- CAN-FD
- USB2.0
- SPI, SCI, I²C
- xSPI

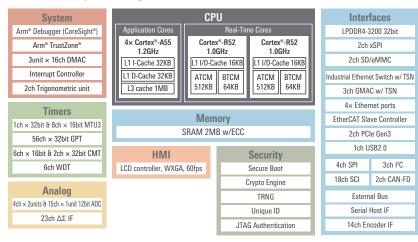
Safety functions

- Register write protection, input clock oscillation stop detection, and CRC
- Isolated peripheral function access via MPU

Package

- 576-pin FCBGA (21mm × 21mm, 0.8mm pitch)
- $T_i = -40^{\circ}C \text{ to } +125^{\circ}C$

■ RZ/N2H Group Block Diagram



RZ/N2H Product Lineup

Security	R9A09G087M48GBG	R9A09G087M28GBG	R9A09G087M08GBG			
Non-Security	R9A09G087M44GBG	R9A09G087M24GBG	R9A09G087M04GBG			
Cortex-A55	Quad	Dual	Single			
Cortex-R52		Two CPUs				
Package	FCBGA 576-pin, 21mm × 21mm, 0.8mm pitch					
Power Supply	0.8V, 1.1V, 1.8V, 3.3V					
Operating Temperature	$Tj = -40^{\circ}C \text{ to } +125^{\circ}C$					

RZ/N2L Group

CPU core

- Arm® Cortex®-R52
- Operating frequency: 400MHz/200MHz
- Single-precision/double-precision floating-point unit

On-chip memory

- Tightly Coupled Memory: 128KB (w/ ECC) + 128KB (w/ ECC)
- 1.5MB on-chip RAM (with ECC)

Features

- TSN support
- 3-port Gigabit Ethernet switch
- EtherCAT slave controller
- Parallel host/serial host interface
- PWM timer
- ∆∑interface
- ADC
- Trigonometric function unit
- CAN-FD
- USB2.0
- SPI, SCI, I²C
- xSPI

Safety functions

- Register write protection, input clock oscillation stop detection, and CRC
- Isolated peripheral function access via MPU

Package

- 225-pin FBGA (13mm × 13mm, 0.8mm pitch)
- 121-pin FBGA (10mm × 10mm, 0.8mm pitch)
- $T_j = -45^{\circ}C \text{ to } +125^{\circ}C$

■ RZ/N2L Group Block Diagram

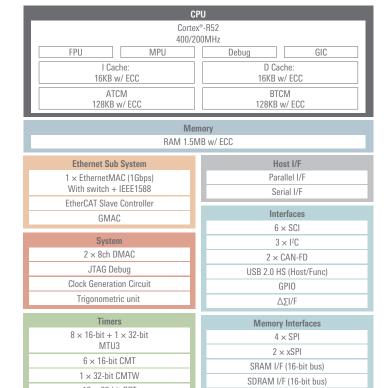
18 × 32-bit GPT

1 × 14-bit WDT

Security

Secure boot

JTAG w/ disable function



Burst ROM I/F (16-bit bus)

Analog

(4 + 8) × 12-bit ADC

RZ/N2L Product Lineup

It	em	R9A07G084M08GBG	R9A07G084M04GBG	R9A07G084M08GBA	R9A07G084M04GBA	
CPU Cortex®-R52 (Max 400MHz)						
Tightly Coupled Me	mory	ATCM 128KB (w/ECC) / BTCM 128KB (w/ECC)				
RAM			1.5MB	(w/ECC)		
External bus		8, 1	6bit	Not Sup	pported	
Host I/F	Serial Host	OSPI	/QSPI	QS	PI	
HUSt I/F	Parallel Host	8, 1	6bit	Not Sup	ported	
Industrial Ethernet	Protocol	EtherCAT®, PROFINET RT/IRT, EtherNet/IP™, TSN (IEC/IEEE 60802 Industrial Profile), CC-Link IE Field Basic, OPC UA over TSN				
Ether Port		3 p	orts	2 ports		
Motor Control Perip	herals	PWM Timer (MTU3, GPT), ADC*, ΔΣ Interface, Trigonometric function unit				
Security		Supported	Not Supported	Supported	Not Supported	
Power 1.1V, 1.8V, 3.3V			8V, 3.3V			
Operating Tempera	ture	$Tj = -40 \text{ to } +125^{\circ}\text{C}$				
Package FBGA			GA	FBGA		
Pin Count		225-pin		121-pin		
Package Information	n	13mm × 13mn	n, 0.8mm pitch	10mm × 10mm	ı, 0.8mm pitch	



RZ/N1D Group

CPU core

- Arm® Cortex®-A7 dual-core processor
- Operating frequency: 500MHz

Cache memory

- L1 I-cache: 16KB × 2, D-cache: 16KB × 2
- L2: 256KB

Internal memory

= 2MB (ECC)

External memory

- DDR2/DDR3 controller
- Quad I/O SPI
- SDIO eMMC
- NAND flash controller

R-IN engine

- Arm® Cortex®-M3
- Operating frequency: 125MHz
- HW-RTOS accelerator
- Ethernet accelerator

Main Ethernet communication functions

- EtherCAT slave controller
- Sercos® III slave controller
- HSR switch (400-pin)
- 5-port Ethernet switch

Other communication functions

- UART × 8 channels
- $I^2C \times 2$ channels
- USB Host/Function × 1 channel, Host 1 channel
- SPI × 6 channels (master × 4 channels, slave × 2 channels)
- CAN

Other functions

- LCD controller
- ADC: 12-bit × 8 channels × 2 units (400-pin)
- ADC: 12-bit × 8 channels × 1 unit (324-pin)
- PWM timer, GPT

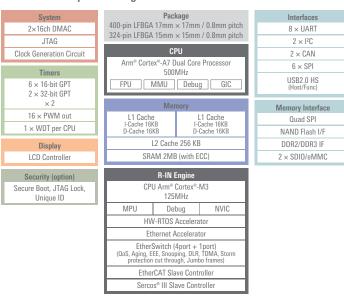
Package

- 400-pin: LFBGA, 17mm × 17mm, 0.8mm pin pitch
- 324-pin: LFBGA, 15mm × 15mm, 0.8mm pin pitch

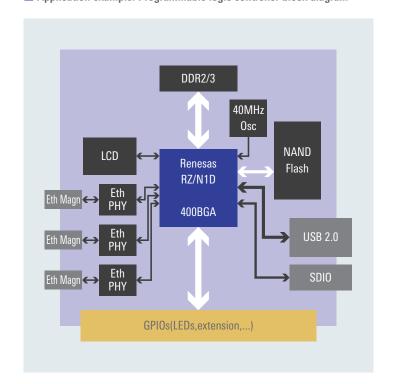
Operating temperature

■ Tj = -40°C to +110°C

■ RZ/N1D Group Block Diagram



■ Application example: Programmable logic controller block diagram



RZ/N1S Group

CPU core

- Arm® Cortex®-A7 single-core processor
- Operating frequency: 500MHz

Cache memory

- L1 I-cache: 16KB, D-cache: 16KB
- L2: 128KB

Internal memory

- 6MB (ECC)
- External memory
- Quad I/O SPI
- SDIO eMMC
- NAND flash controller

R-IN engine

- Arm® Cortex®-M3
- Operating frequency: 125MHz
- HW-RTOS accelerator
- Ethernet accelerator

Main Ethernet communication functions

- EtherCAT slave controller
- Sercos® III slave controller
- 5-port Ethernet switch

Other communication functions

- UART × 8 channels
- $I^2C \times 2$ channels
- USB Host/Function × 1 channel, Host 1 channel
- SPI × 6 channels (master × 4 channels, slave × 2 channels)
- CAN

Other functions

- LCD controller
- ADC: 12-bit × 8 channels × 1 unit
- PWM timer, GPT

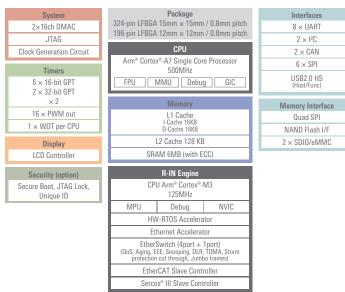
Package

- 324-pin: LFBGA, 15mm × 15mm, 0.8mm pin pitch
 196-pin: LFBGA, 12mm × 12mm, 0.8mm pin pitch

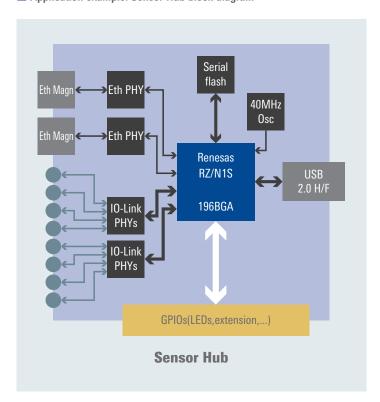
Operating temperature

■ Tj = -40°C to +110°C

■ RZ/N1S Group Block Diagram



Application example: Sensor Hub block diagram





RZ/N1L Group

R-IN engine

- Arm® Cortex®-M3
- Operating frequency: 125MHz
- HW-RTOS accelerator
- Ethernet accelerator

Internal memory

■ 6MB (ECC)

- External memory
- Quad I/O SPI ■ SDIO eMMC
- NAND flash controller
- Main Ethernet communication functions
- EtherCAT slave controller
- Sercos® III slave controller
- GbE Ethernet switch

Other communication functions

- UART × 8 channels
- $I^2C \times 2$ channels
- USB Host/Function × 1 channel, Host 1 channel
- $\blacksquare \ \ \mathsf{SPI} \times \mathsf{6} \ \mathsf{channels} \ \mathsf{(master} \times \mathsf{4} \ \mathsf{channels}, \ \mathsf{slave} \times \mathsf{2} \ \mathsf{channels}) \\$
- CAN × 2 channels

Other functions

- LCD controller
- ADC: 12-bit × 8 channels × 1 unit
- PWM timer, GPT

Package

■ 196-pin: LFBGA, 12mm × 12mm, 0.8mm pin pitch

Operating temperature $Tj = -40^{\circ}C \text{ to } +110^{\circ}C$

■ RZ/N1L Group Block Diagram

System	Package		
2×16ch DMAC	196-pin LFBGA	12mm × 12mm	/ 0.8mm pitch
JTAG		Memory	
Clock Generation Circuit	SRA	AM 6MB (with E	CC)
Timers		R-IN Engine	
6 × 16-bit GPT 2 × 32-bit GPT	CPI	J Arm® Cortex®- 125MHz	M3
× 2	MPU	Debug	NVIC
16 × PWM out	HV	/-RTOS Accelera	itor
1 × WDT per CPU	Et	hernet Accelerat	tor
	Ethers (QoS, Aging, E protection	Switch (2port + EE, Snooping, DLR cut through, Juml	1port) , TDMA, Storm oo frames)
	Ether	CAT Slave Cont	roller
	Sercos® III Slave Controller		

Interfaces
8 × UART
2 × I ² C
2 × CAN
6 × SPI
USB2.0 HS (Host/Func)
Memory Interface
Quad SPI
NAND Flash I/F
1 × SDIO/eMMC

RZ/N2H, RZ/N2L: Development Environments (Integrated Development Environments)

	iar	RENESAS
Development environments	IAR Embedded Workbench® for Arm®	• e² studio*1 e² studio e² studio
Compilers	• IAR C/C++ compiler*2	• GNU tool*4
Other tools	AP4 and FSP Smart Configurator code generation tools from Renesas can be used.	Code generation function available as a plug-in.
ICEs	I-jet™/I-jet Trace™ for Arm Cortex®-A/R/M JTAGjet-Trace	• J-Link LITE from Segger • J-Link series from Segger*5

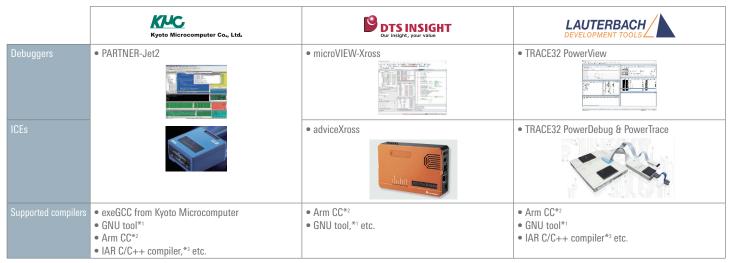
^{*1.} Eclipse-based development environment from Renesas (http://renesas.com/e2studio)

^{1.} Two versions of the software are available for download free of charge. One limits the code size to 32KB and can be used with no time limitation. The other has no limit on code size and expires after 30 days. (https://www.iar.com/EWARM)

^{*3.} Arm CC is included in DS-5. In addition to the popularly priced DS-5 R2/A and R2/T editions, a fully functional evaluation version of DS-5 that expires after 30 days is available free of charge. Contact your DS-5 dealer for details.

^{*4.} GNU TOOLS & SUPPORT Website (https://llvm-gcc-renesas.com/) *5. Renesas does not handle ICEs from Segger. Contact a sales agent for details.

RZ/N2H, RZ/N2L: Development Tools (Debuggers, ICEs)



- *1. GNU TOOLS & SUPPORT Website (https://llvm-gcc-renesas.com/)
- *2. Arm CC is included in DS-5. In addition to the popularly priced DS-5 RZ/A and RZ/T editions, a fully functional evaluation version of DS-5 that expires after 30 days is available free of charge. Contact your DS-5 dealer for details.
- *3. Two versions of the software are available for download free of charge. One limits the code size to 32KB and can be used with no time limitation. The other has no limit on code size and expires after 30 days. (https://www.iar.com/EWARM)

Code Generation Support: Flexible Software Package (FSP) + Smart Configurator (SC)

The FSP includes everything you'll need to start developing software: board-dependent programs, peripheral function drivers, middleware, and documentation on how to use them.

Smart Configurator is a utility based on the concept of "combining software components freely." The intuitive GUI makes it easy to configure pins and FSP driver settings and to generate source code customized for your use case. It works together with integrated development environments such as IAR Embedded Workbench® for Arm from IAR Systems and e² studio.

(Supported products: RZ/N2H, RZ/N2L)







Development Kits

These products are evaluation boards with RZ/N series configured as the key device and are capable of easily implementing software development.

■ RZ/N2H Evaluation Board Kit www.renesas.com/rzn2h-evkit □

- Easy evaluation of each RZ/N2H function with Segger's on-board debugger
- Ordering number: RTK9RZN2H0S00000BJ



- 576-pin RZ/N2H MPU (R9A09G087M44GBG)
- 4 ports of Ethernet connectors
- LPDDR4: 8GB, QSPI Flash, Octa Flash, eMMC
- PCle 2 lane, micro SD slot ×1
- Pmod™/Grove®/QWIIC®/mikroBUS™
- Three USB cables are bundled for power supply (Type C, 15V), on-board emulator connection (Micro B) and terminal debugging (Mini B).

■ RZ/N2L Remote I/O Solution Kit www.renesas.com/rzn2l-remote-io-solution [7]

- The RZ/N2L Remote I/O Solution Kit is a development kit for evaluating remote I/O applications which is equipped with digital IO interface with photocoupler isolation and analog input.
- Provide sample programs for industrial network communication and DI/DO.
- Ordering number: CN032-GATEWAYREFZ



- Digital IO interface with photocoupler isolation (IN: 8, OUT: 8)
- Analog Input interface (4-20mA: 2, 0-10V: 2)
- Support industrial network protocols: EtherCAT, EtherNet/IP
- RS485 Transceiver, CAN Transceiver, D-sub connector
- Ethernet PHY, RJ45 connector
- Memory (Quad SPI flash, EEPROM, SDRAM)

■ Renesas Starter Kit+ for RZ/N2L www.renesas.com/rskrzn2l []

- The board is mounted with a RZ/N2L with a 225BGA package and can be used to evaluate almost all of the device's functions.
- Emulator circuit is mounted, can start program debugging by simply connecting USB cable to PC.
- Ordering number: RTK9RZN2L0S00000BE



- 225-pin RZ/N2L MPU (R9A07G084M04GBG)
- Gigabit Ethernet PHY
- Octal flash memory
- Pmod[™], Grove[®], QWIIC[®], and mikro-BUS™ connectors
- Pin header for external expansion
- Includes a USB power cable that can also be used to connect an emulator.

■ RZ/N2L Industrial Network SOM Kit www.renesas.com/yconnect-it-rzn2l [



- YCONNECT-IT-RZN2L is a compact reference kit for evaluating applications using Industrial Ethernet communication
- Flexible power supply from either USB or 24V DC terminal or Arduino host board
- Ordering number: YCONNECT-IT-RZN2L



- 2x Gigabit Industrial Ethernet connectors
- 2x PMOD connectors
- Arduino dual-use connector
- 9-pin connector for external debugger connection and Segger J-Link OB for debugging via USB

■ CONNECT IT! ETHERNET RZ/N www.renesas.com/RZN-YConnect-It

- CONNECT IT! ETHERNET RZ/N is the perfect solution kit for developers new to developing with the RZ/N1.
- The kit comes with not only an evaluation board, but also a JTAG emulator and various sample software.
- It is possible to evaluate master communication / slave communication of industrial networks.



- JTAG emulator
 - IAR I-jet Lite (20-pin flat ribbon/USB cable)
- 2 USB cables
- Startup manuals
- Pin setting tool
- RZ/N Solution Kit DVD
 - User's manual
 - OS (Linux, ThreadX®(Evaluation version), HW-RTOS)
- Software PLC Codesys
- Protocol stacks

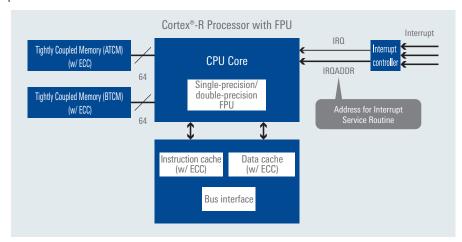
MEMO		



RZ/T Series

RZ/T Series Features

- High-performance, high-speed real-time control
- Integrated peripheral functions
- High-performance, high-speed real-time control



- High-speed RAM directly coupled to the CPU allows fast processing and bypassing of the cache for reliable real-time responsiveness.
- ECC for enhanced reliability
- Assures responsive interrupt handling suitable for embedded control applications.

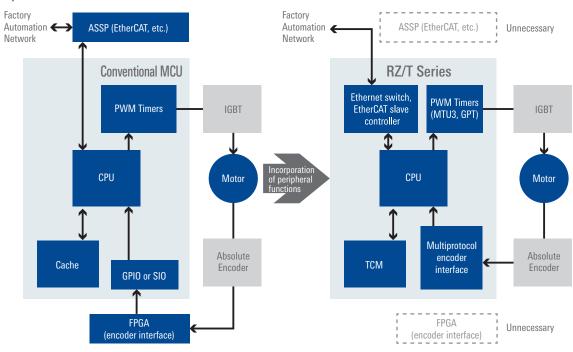
RZ/T2H Features

- RZ/T2H is an advanced high-end microprocessor (MPU) equipped with Quad Arm® Cortex®-A55 cores (1.2GHz) for application processing and two Arm Cortex-R52 cores (1.0GHz) for real-time control.
- The peripheral functions are capable of controlling motors of up to 9-axis with low latency access from a Cortex-R52 CPU.
- The Ethernet functionalities supporting TSN and flexible for both industrial Ethernet controller and device.

RZ/T2 Specification

Item		RZ/T2H	RZ/T2ME	RZ/T2M	RZ/T2L
Application Cor	e	Cortex-A55 1.2GHz ×4	_	_	_
Realtime Core		Cortex-R52 1.0GHz ×2	Cortex-R52 800MHz ×2	Cortex-R52 800MHz ×2	Cortex-R52 800MHz
DDR		LPDDR4-3200 32-bit	_	_	_
Industrial Ether	net	4 Ether ports 3 Ether ports 3 Ether ports 3 GMAC 1 GMAC 1 GMAC Ethernet Switch Ethernet Switch ESC, TSN ESC, TSN ESC, TSN		ESC	
	GPT/MTU (for motor control)	56ch/9ch (Up to 9-axis)	7ch/9ch (2-axis)	7ch/9ch (2-axis)	7ch/9ch (2-axis)
Motor Control Sigma Delta I/F Absolute Encoder I/F		30ch	6ch	6ch	6ch
		16ch	2ch	2ch	2ch
PCle		PCIe (Gen3) ×2	_		
HMI		Parallel RGB	_	_	_
On-The-Fly-Decryption		_	Supported	_	_
Host IF		Serial	_	_	Serial
Package		FCBGA 729-pin (23mm × 23mm)	FBGA 320-pin (17mm × 17mm) FBGA 225-pin (13mm × 13mm)	FBGA 320-pin (17mm × 17mm) FBGA 225-pin (13mm × 13mm) LQFP 176-pin (24mm × 24mm) LQFP 126-pin (14mm × 20mm)	FBGA 196-pin (12mm × 12mm)

■ Integrated peripheral functions



- Integrates communication ASSP that would previously have been implemented as an external device.
- Integrates encoder interface that would previously have been implemented by an FPGA or ASIC.

	EnDat 2.2	BiSS-C	NIKON A-format	FA-CODER	HIPERFACE DSL
Related specifications	Heidenhein Corp http://www.heidenhain.de	iC-Haus GmbH http://www.biss-interface.com	NIKON Corporation http://www.nikon.co.jp	TAMAGAWA SEIKI CO.,LTD. http://www.tamagawa-seiki.co.jp	SICK STEGMANN GmbH http://www.sick.com
Communication system	Clock synchronous	Clock synchronous	Asynchronous	Asynchronous	Asynchronous
Transmission link	RS-485	RS-422	RS-485	RS-485	RS-485
Supported frequencies/data transfer rates	100kHz to 16.7MHz	62.5kHz to 10MHz	2.5Mbps, 4Mbps, 6.67Mbps, 8Mbps, 16Mbps	2.5Mbps, 5Mbps	9.375Mbps
I/O pin count/ signal level	4/3.3V TTL level	2 / 3.3V TTL level	3 / 3.3V TTL level	3 / 3.3V TTL level	3 / 3.3V TTL level
Compatible functions on T series	- Propagation delay function - Not supported for incremental signals	Delay compensation function Supported in C mode (not supported in B mode) Not supported for incremental signals Supported on 1-to-1 connections (not supported on bus connections)	- Supported on 1-to-1 connections and bus connections	Baseband NRZ code support Not supported for incremental signals or synchronous Manchester code	- External synchronous communication (sync mode) - Asynchronous communication (free running mode) - Estimator function (position estimation when error occurs) - RSSI, quality monitoring



RZ/T Series Application

A fast Cortex-R CPU operating at 300MHz to 1000MHz and large-capacity tightly-coupled memory provide the high performance and advanced functionality required by industrial applications such as industrial motors or AC servo drives. The RZ/T series is powerful enough to handle Industrial Ethernet processing of various types while still maintaining real-time performance. Furthermore, RZ/T2H has high performance Cortex-A CPU for application processing.



RZ/T2H Group

CPU core

- Arm® Cortex®-A55, Quad/Dual/Single-core Max operating frequency: 1.2GHz
 L1 I/D-cache 32KB per core, L3 cache 1MB
- Arm® Cortex®-R52, Dual-core Max operating frequency: 1.0GHz L1 I/D-cache 16KB.

Tightly Coupled Memory (TCM): 512KB (w/ ECC) + 64KB (w/ ECC) per core

Features

- On-chip system SRAM 2.0MB (w/ ECC)
- LPDDR4-3200 32-bit
- SD/eMMC
- Motor Control Peripherals (Support up to 9-axis)
 - PWM Timer: MTU3 9ch– PWM Timer: GPT 56ch
 - $-\Delta\Sigma$ interface: 30ch
 - 12-bit ADC: 3units
 - 12-bit ADC: 3units – Encoder IF: 16ch
 - Trigonometric function unit
- Industrial Ethernet
 - 3-port Ethernet Switch w/TSN
 - $-\,3\text{ch}$ Gigabit Ethernet MAC w/ TSN
 - $-4 \times$ Ethernet ports
 - EtherCAT Slave Controller (ESC)
- PCI Express Gen3
- Serial host interface
- LCD Controller
- CAN-FD
- USB2.0
- SPI, SCI, I²C
- xSPI

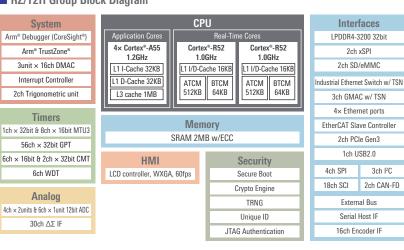
Safety functions

- Register write protection, input clock oscillation stop detection, and CRC
- Isolated peripheral function access via MPU

Package

- 729-pin FCBGA (23mm × 23mm, 0.8mm pitch)
- Tj = -40°C to +125°C

■ RZ/T2H Group Block Diagram



RZ/T2H Product Lineup

Security	R9A09G077M48GBG	R9A09G077M28GBG	R9A09G077M08GBG		
Non-Security	R9A09G077M44GBG	R9A09G077M24GBG	R9A09G077M04GBG		
Cortex-A55	Quad	Dual	Single		
Cortex-R52	Two CPUs				
Package	FCBGA 729-pin, 23mm × 23mm, 0.8mm pitch				
Power Supply	0.8V, 1.1V, 1.8V, 3.3V				
Operating Temperature		Tj = -40°C to $+125$ °C			

RZ/T2M & T2ME Group

CPU core

- Arm® Cortex®-R52 × 2
- Operating frequency: 800MHz/400MHz/200MHz
- Single-precision/double-precision floating-point unit

On-chip memory

- Tightly Coupled Memory: 512KB (W/ ECC) + 64KB (W/ ECC)
- 2MB on-chip RAM (with ECC)

Features

- Low latency peripheral port (LLPP) bus
- TSN support
- 3-port Gigabit Ethernet switch
- EtherCAT slave controller
- Encoder interface
- PWM timer
- ∆∑ interface
- ADC
- Trigonometric function unit
- xSPI
- CAN-FD
- USB2.0
- SPI, SCI, I²C

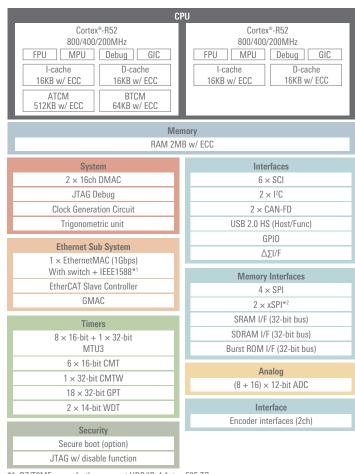
Safety functions

- Register write protection, input clock oscillation stop detection, and CRC
- Isolated peripheral function access via MPU

Package

- 320-pin FBGA (17mm × 17mm, 0.8mm pitch)
- 225-pin FBGA (13mm \times 13mm, 0.8mm pitch)
- 176-pin LQFP (24mm × 24mm, 0.5mm pitch)
- 128-pin LOFP (14mm × 20mm, 0.5mm pitch)
- $Tj = -45^{\circ}C \text{ to } +125^{\circ}C$

■ RZ/T2M & T2ME Group Block Diagram



- *1: RZ/T2ME group further support UDP/IPv4 1step E2E TC
- *2: RZ/T2ME group further support On-The-Fly-Decryption



RZ/T2M & T2ME Product Lineup

Security	R9A07G075M28GBG	R9A07G075M26GBG	R9A07G075M28GBA	R9A07G075M26GBA	R9A07G075M27GBA	-	R9A07G075M05GFP	R9A07G075M05GFA	R9A07G075M29GBG	R9A07G075M29GBA
Non-Security	R9A07G075M24GBG	R9A07G075M22GBG	R9A07G075M24GBA	R9A07G075M22GBA		R9A07G075M21GBA	R9A07G075M01GFP	R9A07G075M01GFA		
СРИ		Dual Cortex®-R52 (800+800MHz) Single Cortex®-R52 (800MHz)					Dual Cortex®-R52 (800+800MHz)			
System RAM			2.0MB	w/ECC			1.5MB	w/ECC	2.0MB	w/ECC
TCM Memory		CPU0 : ATCM: 512KB w/ECC, BTCM: 64KB w/ECC CPU1 : ATCM: none, BTCM: none CPU0 : ATCM: 512KB w/ECC, BTCM: 64KB w/ECC				BTCM: 64 CPU1: ATCM:	512KB w/ECC, KB w/ECC none, BTCM:			
∆∑ interface					3ch ×	2 units				
Encoder I/F Protocol		A-format™, BiSS-C, EnDat2.2, FA-CODER®, HIPERFACE DSL®								
Motor Control Peripherals			PWM Timer (M	ITU3, GPT), ΔΣ Ir	nterface, 12bit A	DC, Encoder Inte	erface, Trigonome	tric Accelerator		
Ethernet Port	3ports (100/1000Mbps) None				one 3ports (100/1000Mbps support UDP/IPv4 1step E2					
EtherCAT Port	N	lax 3ports (Exclus	sive with Etherne	et)		No	one			3ports ith Ethernet)
Industrial Ethernet Protocol	EtherCAT®, PROFINET RT/IRT, EtherNet/IP™, CC-Link IE Basic, TSN (IEC/IEEE 60802 Industrial Profile), OPC UA over TSN					EtherNet/IP™, (TSN (IEC/IEEE (OFINET RT/IRT, CC-Link IE Basic, 60802 Industrial UA over TSN			
CAN	CAN FD ×2ch	Classic CAN ×2ch	CAN FD ×2ch	Classic CAN ×2ch	CAN FD ×2ch	Classic CAN ×2ch	Classic CAN ×2ch	Classic CAN ×2ch	CAN FI	O × 2ch
xSPI	2ch					2ch w	/ OTFD			
Package	BGA320 BGA225 (17mm×17mm, 0.8mm pitch) (13mm×13mm, 0.8mm pitch)					QFP176 (24mm×24mm, 0.5mm pitch)	QFP128 (14mm×20mm, 0.5mm pitch)	BGA320 (17mm×17mm, 0.8mm pitch)	BGA225 (13mm×13mm, 0.8mm pitch)	
Power Supply		1.1V, 1.8V, 3.3V								
Operating Temperature					Tj = -40	to +125°C				

RZ/T2L Group

CPU core

- Arm® Cortex®-R52
- Operating frequency: 800MHz/400MHz/200MHz
- Single-precision/double-precision floating-point unit

On-chip memory

- Tightly Coupled Memory: 512KB (W/ ECC) + 64KB (W/ ECC)
- 1MB on-chip RAM (with ECC)

Features

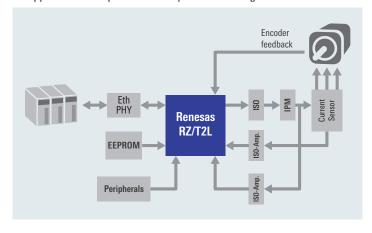
- Low latency peripheral port (LLPP) bus
- EtherCAT slave controller
- Gigabit Ether MAC
- Encoder interface
- PWM timer
- ∆∑interface
- ADC
- Trigonometric function unit
- Serial host interface
- xSPI
- CAN-FD
- USB2.0
- SPI, SCI, I²C

Safety functions

- Register write protection, input clock oscillation stop detection, and CRC
- Isolated peripheral function access via MPU

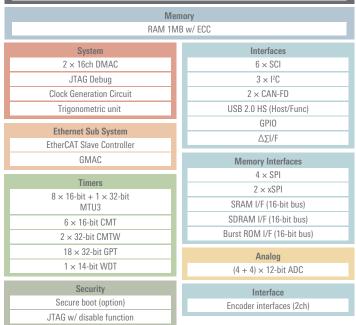
- FBGA 196-pin (12mm × 12mm, 0.8mm pitch)
- Tj = -45° C to $+125^{\circ}$ C

■ Application example: AC servo system block diagram



■ RZ/T2L Group Block Diagram

CPU				
Cortex®-R52 800MHz/400MHz/200MHz				
FPU	MPU	Debug	GIC	
	che v/ ECC	D-ca 16KB v	nche v/ ECC	
512KB	CM w/ ECC	BT(64KB v	CM v/ ECC	



RZ/T2L Product Lineup

Part Number	R9A07G074M08GBG	R9A07G074M05GBG	R9A07G074M04GBG	R9A07G074M01GBG		
CPU		Cortex®-R52 (Max 800MHz)			
System RAM		1.0MB	(w/ECC)			
TCM Memory		ATCM 512KB (w/ECC)	/ BTCM 64KB (w/ECC)			
External bus		8, 1	6 bit			
Peripheral functions for motor control	PWM Timer (MTU3, GPT), ADC, $\Delta\Sigma$ interface, Trigonometric function unit					
GMAC	1 ch					
Ethernet Port		3 ports				
EtherCAT	Supported	Not Supported	Supported	Not Supported		
CAN	CAN-FD	CAN	CAN-FD	CAN		
Security	Supported Supported Not Supported Not Supported					
Package	BGA196 (12mm × 12mm, 0.8mm pitch)					
Power Supply	1.1V, 1.8V, 3.3V					
Operating Temperature		$T_i = -40.1$	to +125°C			



RZ/T1 Group

CPU core

- Arm® Cortex®-R4
- Operating frequency: 600MHz/450MHz/300Hz
- High-performance, high-speed real-time control
- Single-precision/double-precision floating-point unit

Renesas R-IN engine ("R-IN engine")

- Arm® Cortex®-M3
- Operating frequency: 125MHz
- HW-RTOS accelerator
- R-IN engine instruction memory: 512KB (w/ ECC) + data memory: 512KB (w/ ECC) On-chip memory
- Tightly Coupled Memory: 512KB (w/ ECC) + 32KB (w/ ECC)
- Extended RAM instruction memory 512KB (w/ ECC) + data memory: 512KB (w/ ECC) Features
- Industrial Ethernet communication accelerator with multi-protocol support (R-IN engine)
- EtherCAT slave controller
- PWM timer: MTU3a, GPT
- Encoder interface (Nikon A-formatTM/BiSS-C/EnDat2.2/HIPERFACE DSL®/ FA-CODER®)

Note: 2ch encoder support depends on the combination of the selected protocol.

- High Speed USB
- Secure boot (option)
- Safety functions
 - ECC memory
 - CRC (32-bit)
 - Independent WDT: Operating on dedicated on-chip oscillator
- ΔΣ interface
- 100Mbps EtherMAC (with Ethernet switch)
- Ethernet accelerator
- Power supply voltage: 1.2V, 3.3V

Package

- FBGA 320-pin (17mm × 17mm, 0.8mm pitch)
- Tj = -45°C to +125°C

■ RZ/T1 Group Block Diagram

CPU					
Cortex®-R4 600MHz/450MHz/300Hz					
FPU	MPU	Debug	VIC		
	che ı/ ECC	D-ca 8KB w			
512KB	CM w/ ECC	BT(32KB v			

Memory (option)

RAM 1MB w/ECC

R-IN Engine (option)			
	CPU Cortex®-M3 125MHz		
MPU	Debug HW-RTOS Accelerator	NVIC	
	Memory		
	nstruction RAM: 512KB with ECC Data RAM: 512KB with ECC		

System 2 × 16ch DMAC

JTAG Debug Clock Generation Circuit

Timers

8 × 16-bit + 1 × 32-bit MTU3a 6 × 16-bit CMT

2 × 32-bit CMT2

4 × 16-bit GPT

 $1 \times WDT$

1 × iWDT 12 × 16-bit TPU

2 × 4gr× 4-bit PPG

Security
Secure boot (option)

JTAG w/ disable function

5 × SCIF
$2 \times I^2 \mathbb{C}$
2 × CAN
1 × EthernetMAC (100Mbps) With switch + IEEE1588
USB 2.0 HS (Host/Func)
GPI0
ΔΣI/F
EtherCAT Slave Controller (option)
Memory Interfaces
4 × SPI

Interfaces

QSPI (Flash I/F)with Direct Access from CPU

SRAM I/F (32-bit bus)

SDRAM I/F (32-bit bus)
Burst ROM I/F (32-bit bus)

Analog

 $(8 + 16) \times 12$ -bit ADC

Interface
Encoder interfaces (2ch) (option)

RZ/T1 Product Lineup

CPU	Tightly coupled memory	Extended RAM						
600 MHz + R-IN Engine (150MHz)	512KB+32KB	– (1MB for R-IN)					R7S910017	R7S910018
450 MHz + R-IN Engine (150MHz)	512KB+32KB	– (1MB for R-IN)					R7S910015	R7S910016
600 MHz	512KB+32KB	1MB	R7S910007	R7S910013	R7S910027	R7S910028		
4F0 MII-	E40VD . 20VD	1MB	R7S910006		R7S910025	R7S910026		
450 MHz	512KB+32KB	_	R7S910002	R7S910011				
300 MHz	512KB+32KB	_			R7S910035	R7S910036		
Package		320 BGA	320 BGA	320 BGA	320 BGA	320 BGA	320 BGA	
Encoder I/F		_	Yes	_	Yes	_	Yes	
Industrial Ethernet		(Standard	– I Ethernet)	Ethe	rCAT	Multi-proto	col support	

Utilizing the Arm® Ecosystem

■ Utilizing Renesas' Experience and the Arm® Ecosystem

Customers can benefit from solutions combining Renesas' accumulated experience in the microcontroller industry and the global ecosystem of Arm® partners. Products such as development environments, OS, and middleware are available from partner companies supporting the RZ/T series.



RZ/T Series: Development Environments (Integrated Development Environments)

	iar	RENESAS	
Development environments	IAR Embedded Workbench® for Arm®	• e² studio*1 e² studio e² studio	
Compilers	• IAR C/C++ compiler*2	• GNU tool*4	
Other tools	AP4 and FSP Smart Configurator code generation tools from Renesas can be used.	Code generation function available as a plug-in.	
ICEs	I-jet™/I-jet Trace™ for Arm Cortex®-A/R/M JTAGjet-Trace	J-Link LITE from Segger J-Link series from Segger*5	

- *1. Eclipse-based development environment from Renesas (http://renesas.com/e2studio)
- *2. Two versions of the software are available for download free of charge. One limits the code size to 32KB and can be used with no time limitation. The other has no limit on code size and expires after 30 days. (https://www.iar.com/EWARM)
- *3. Arm CC is included in DS-5. In addition to the popularly priced DS-5 RZ/A and RZ/T editions, a fully functional evaluation version of DS-5 that expires after 30 days is available free of charge. Contact your DS-5 dealer for details.
- *4. GNU TOOLS & SUPPORT Website (https://llvm-gcc-renesas.com/)
- *5. Renesas does not handle ICEs from Segger. Contact a sales agent for details.

RZ/T Series: Development Tools (Debuggers, ICEs)

	Kyoto Microcomputer Co., Ltd.	P DTS INSIGHT Our insight, your value	LAUTERBACH DEVELOPMENT TOOLS	Computex*
Debuggers	• PARTNER-Jet2	• microVIEW-Xross	• TRACE32 PowerView	• CSIDE version 7
ICEs		• adviceXross	TRACE32 PowerDebug & PowerTrace	PALMICE4 PALMICE4 Computer JTAG model Large capacity trace model
Supported compilers	exeGCC from Kyoto Microcomputer GNU tool*1 Arm CC*2 IAR C/C++ compiler,*3 etc.	• Arm CC*2 • GNU tool,*1 etc.	• Arm CC*2 • GNU tool*1 • IAR C/C++ compiler*3 etc.	• Arm CC*2 • IAR C/C++ compiler*3 • GNU tool,*1 etc.
Supported product	RZ/T2H, RZ/T2ME, RZ/T2M, RZ/T1	RZ/T2H, RZ/T2ME, RZ/T2M, RZ/T1	RZ/T2H, RZ/T2ME, RZ/T2M, RZ/T2L, RZ/T1	RZ/T1

- *1. GNU TOOLS & SUPPORT Website (https://llvm-gcc-renesas.com/)
- *2. Arm CC is included in DS-5. In addition to the popularly priced DS-5 R2/A and R2/T editions, a fully functional evaluation version of DS-5 that expires after 30 days is available free of charge. Contact your DS-5 dealer for details.
- *3. Two versions of the software are available for download free of charge. One limits the code size to 32KB and can be used with no time limitation. The other has no limit on code size and expires after 30 days. (https://www.iar.com/EWARM)



Code Generation Support: Flexible Software Package (FSP) + Smart Configurator (SC)

(Supported products: RZ/T2H, RZ/T2ME, RZ/T2M, RZ/T2I)

The FSP includes everything you'll need to start developing software: board-dependent programs, peripheral function drivers, middleware, and documentation on how to use them.

Smart Configurator is a utility based on the concept of "combining software components freely." The intuitive GUI makes it easy to configure pins and FSP driver settings and to generate source code customized for your use case. It works together with integrated development environments such as IAR Embedded Workbench® for Arm from IAR Systems and e² studio.



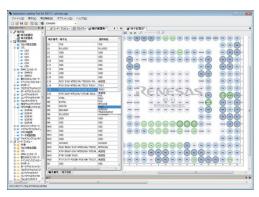


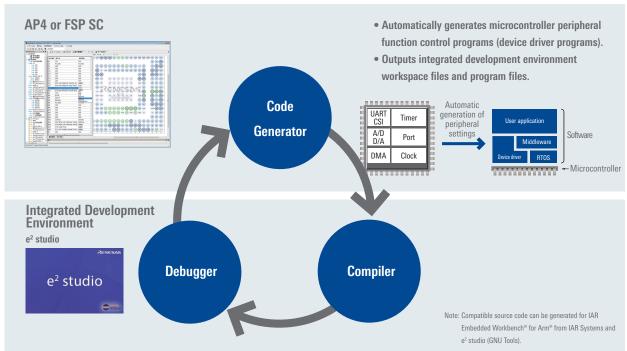
Code Generation Support Tool: AP4

(Supported product: RZ/T1)

AP4 is a standalone tool that automatically generates peripheral function control programs (device driver programs) based on settings entered by the user. The build tool (compiler) is selectable. This makes it possible to generate peripheral function control program code to match a specific build tool and enables interoperation with integrated development environments. (https://www.renesas.com/ap4)

The version of AP4 that is compatible with the RZ/T1 group can generate compatible source code for IAR Embedded Workbench® for Arm® from IAR Systems, Development Studio (DS-5™) from Arm®, and e² studio (GNU Tools).





Development Kits

RZ/T2 evaluation boards has Segger's on-board debugger and user can start evaluation immediately. AC servo solution kit and Inverter boards Kit are available for customers who want to develop servo motor control using RZ/T2 series.

■ RZ/T2H Evaluation Board Kit www.renesas.com/rzt2h-evkit []



- 729-nin R7/T2H MPU (R9A09G077M44GBG)
- Easy evaluation of each RZ/T2H function with on-board debugger
- 4 ports of Ethernet connectors
- LPDDR4: 8GB, QSPI Flash, Octa Flash, eMMC
- PCle 2-lane, micro SD slot ×1
- Pmod[™]/Grove[®]/QWIIC[®]/mikroBUS[™]
- Motor Control up to 9-axis can be evaluated connecting with RZ/T Series Inverter Board and Bus Board
- Three USB cables are bundled for power supply (Type C, 15V), on-board emulator connection (Micro B) and terminal debugging (Mini B).
- Ordering number: RTK9RZT2H0S00000BJ

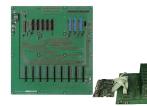
■ RZ/T Series Inverter Board Kit www.renesas.com/invb-lv-rzt-b



Development Tools

- Kit of Inverter board, BLDC motor and cable
- Power supply: DC 24V
- By using in combination with a compatible CPU board such as RZ/T2H Evaluation Board Kit, users can immediately start evaluating motor control.
- Ordering number: RTK0EM0000S05010BJ

■ Bus Board for RZ/T2H www.renesas.com/busb-rzt2h-b



- Interface board for evaluating multi axis motor control with RZ/T2H.
- User can evaluate up-to 9-axis motor control with RZ/T2H by connecting RZ/ T2H Evaluation Board and RZ/T Series Inverter Board Kits.
- Ordering number: RTK0EM0000Z03000BJ

■ Renesas Starter Kit+ for RZ/T2M www.renesas.com/rskrzt2m □



- 320-pin RZ/T2M MPU (R9A07G075M24GBG)
- Gigabit Ethernet PHY
- Octal flash memory
- Pmod[™], Grove[®], QWIIC[®], and mikro-BUS™ connectors
- Pin header for external expansion
- Includes a USB power cable that can also be used to connect an emulator.
- Ordering number: RTK9RZT2M0S00000BE

■ Renesas Starter Kit+ for RZ/T2ME www.renesas.com/rskrzt2me []



- 320-pin RZ/T2ME MPU (R9A07G075M29GBG)
- Gigabit Ethernet PHY
- Octal flash memory
- Pmod[™], Grove[®], QWIIC[®], and mikro-BUS™ connectors
- Pin header for external expansion
- Includes a USB power cable that can also be used to connect an emulator.
- Ordering number: RTK9RZT2M1S00000BE

■ Renesas Starter Kit+ for RZ/T2L www.renesas.com/rskrzt2l []



- 196-pin RZ/T2L MPU (R9A07G074M04GBG)
- Gigabit Ethernet PHY
- Octal flash memory
- Pmod[™], Grove[®], QWIIC[®], and mikro-BUS™ connectors
- Pin header for external expansion
- Includes a USB power cable that can also be used to connect an emulator.
- Ordering number: RTK9RZT2L0S00000BJ

■ RZ/T1-Starter-Kit-Plus www.renesas.com/RZT1-Starter-Kit-Plus □



- RZ/T1 (R7S910018)
- QSPI FlashROM: 64MB
- SDRAM: 64MB × 2
- NOR Flash: 64MB × 2
- Rich interface
- Serial, USB, CAN
- Digilent Pmod I/F (PMOD connector)
- ΔΣ I/F (DSMI connector)
- Ethernet (10/100Base, EtherCAT) I/F etc.
- Audio codec
- Includes SEGGER's simple debug probe "J-Link LITE"
- Includes LCD for debugging
- Ordering number: RTK7910018S01000BE

■ AC Servo Solution Kit www.renesas.com/AC-servo-solution-kit □



- Controller board (equipped with RZ/ T2M, RZ/T2L or RZ/N2L)
- Inverter board that can drive 220V AC servo motor
- 220V AC Servo Motor
- Renesas offers the utility tool on a PC that can operate the motor with position or speed control by sending control commands via serial communication.



RZ/G Series

RZ/G3 Highlights

Inherits features such as RZ/G2's 64-bit Arm Cortex-A and CIP Linux, and enhances low power consumption, high-speed interface, and security functions.

- Connectivity
 - Equipped with PCI-Express and Gbit Ether, it enhances support for high-speed connectivity such as WiFi-6 and LTE
- Real-time sensing
 - Sub system for real-time sensing powered by Cortex®-M + RTOS, not only main system by Cortex®-A + Linux
- Less than 1mW ultra low power consumption standby mode
 Enables less than 1mW ultra low power consumption standby and quick return in Linux applications
- Security with tamper detection
 - Enhanced security for tamper detection in addition to fundamental security features for IoT applications

RZ/G3S Features and Specification

The RZ/G3S microprocessor is equipped with one Cortex®-A55 (1.1GHz) CPU core and two Cortex®-M33 (250MHz) CPU cores and is an entry-class device for IoT applications that supports ultra-low power consumption mode. It has interfaces suitable for IoT edge devices such as 16-bit LPDDR4 or DDR4, PCIe, CAN-FD, and 12-bit ADC.

Items	RZ/G3S
CPU Cortex-A®	1× Cortex®-A55@1.1GHz L1,L3 Parity/ECC
CPU Cortex-M®	2× Cortex®-M33@250MHz
DRAM I/F	16-bit ×1ch LPDDR4/DDR4-1600 w/ECC
USB	USB2.0×2ch (1Host, 1Host/Function/OTG)
PCle	PCI-Express Gen2 1ch *14mm Sq Package only
Gbit Ether	2ch
CAN	2ch (support CAN-FD)
12-bit ADC	2ch
Package	359-pin, LFBGA, 14mm x 14mm, 0.5mm pitch 361-pin, LFBGA, 13mm x 13mm, 0.5mm pitch

RZ/G2 Highlights

- High Performance
 - 64-bit Arm Cortex-A cores, plus powerful 3D graphics engine and video engine capable of supporting up to 4K UHD, to offer the highest performance
- Wide Coverage
 - Entry-level RZ/G2L Group 3 products equipped with Cortex-A55 with improved processing performance have been the RZ/G2 lineup
- High Reliability
 - Built-in Error Correction Code (ECC) for internal and external memory, which is essential for high-reliability mission critical systems
- Super Long Term Support (SLTS)
 - Applying Civil Infrastructure Platform (CIP) Linux, the Linux kernel will be provided with over 10 years of maintenance
- Verified Linux Package
- Renesas verifies and provides a Linux package that combines CIP and Linux basic software. Minimize your Linux maintenance resources

RZ/G2 Specification 1

Items	RZ/G2L	RZ/G2LC	RZ/G2UL
CPU (Arm® Cortex®-A)	1× or 2× Cortex®-A55@1.2GHz L1,L3 Parity/ECC	1× or 2× Cortex®-A55@1.2GHz L1,L3 Parity/ECC	1× Cortex®-A55@1.0GHz L1,L3 Parity/ECC
CPU (Arm® Cortex®-M)	1× Cortex®-M33@200MHz	1× Cortex®-M33@200MHz	1× Cortex®-M33@200MHz
DRAM I/F	16-bit ×1ch DDR4-1600/DDR3L-1333 w/ECC	16-bit ×1ch DDR4-1600/DDR3L-1333 w/ECC	16-bit ×1ch DDR4-1600/DDR3L-1333 w/ECC
Video in	1×MIPI CSI-2 or 1×Digital Parallel input	1×MIPI CSI-2	1×MIPI CSI-2
Video Codec	Support up to Full HD @30fps resolutions Encoding and Decoding: H.264	_	_
3D GFX	Arm Mali-G31 GPU @500MHz	Arm Mali-G31 GPU @500MHz	_
Display out	1×MIPI DSI or 1×Digital Parallel output	1×MIPI DSI	1×Digital Parallel output
USB	USB2.0×2ch (1Host, 1Host/Function/OTG)	USB2.0×2ch (1Host, 1Host/Function/OTG)	USB2.0×2ch (1Host, 1Host/Function/OTG)
Gbit Ether	2ch	1ch	2ch
CAN	2ch (support CAN-FD)	2ch (support CAN-FD)	2ch (support CAN-FD)
12-bit ADC	8ch	-	2ch
Package	551-pin LFBGA, 21mm×21mm, 0.8mm ball pitch 456-pin LFBGA, 15mm×15mm, 0.5mm ball pitch	361-pin LFBGA, 13mm×13mm, 0.5mm ball pitch	361-pin LFBGA, 13mm×13mm, 0.5mm ball pitch

RZ/G2 Specification 2

Items	RZ/G2H	RZ/G2M	RZ/G2N	RZ/G2E
CPU (Arm® Cortex®-A)	4× Cortex®-A57@1.5GHz 4× Cortex®-A53@1.2GHz L1,L2 Parity/ECC	2× Cortex®-A57@1.5GHz 4× Cortex®-A53@1.2GHz L1,L2 Parity/ECC	2× Cortex®-A57@1.5GHz L1,L2 Parity/ECC	2× Cortex®-A53@1.2GHz L1,L2 Parity/ECC
CPU (Arm® Cortex®-R)	1× Cortex®-R7@800MHz L1,TCM w/ECC	1× Cortex®-R7@800MHz L1,TCM w/ECC	1× Cortex®-R7@800MHz L1,TCM w/ECC	1× Cortex®-R7@800MHz L1,TCM w/ECC
DRAM I/F	32-bit ×2ch LPDDR4(3200)	32-bit ×2ch LPDDR4(3200)	32-bit ×1ch LPDDR4(3200)	32-bit ×1ch DDR3L(1856)
Video in	2×MIPI CSI-2, 2×Digital (RGB/YCbCr) up to 8 input image can be captured	2×MIPI CSI-2, 2×Digital (RGB/YCbCr) up to 8 input image can be captured	2×MIPI CSI-2, 2×Digital (RGB/YCbCr) up to 8 input image can be captured	1×MIPI CSI-2, 1×Digital(RGB/YCbCr) up to 2 input image can be captured
Video Codec	Support up to 4k resolutions Decoding: H.265, Encoding and Decoding: H.264	Support up to 4k resolutions Decoding: H.265, Encoding and Decoding: H.264	Support up to 4k resolutions Decoding: H.265, Encoding and Decoding: H.264	Support up to FHD resolutions Decoding: H.265, Encoding and Decoding: H.264
3D GFX	PowerVR GX6650@600MHz	PowerVR GX6250@600MHz	PowerVR GE7800@600MHz	PowerVR GE8300@600MHz
Display out	1×HDMI, 1×LVDS, 1×Digital RGB	1×HDMI, 1×LVDS, 1×Digital RGB	1×HDMI, 1×LVDS, 1×Digital RGB	2×LVDS or 1×LVDS, 1×Digital RGB
USB	USB2.0×2ch (1H, 1H/F/OTG) USB3.0/2.0×1ch (DRD)	USB2.0×2ch (1H, 1H/F/OTG) USB3.0/2.0×1ch (DRD)	USB2.0×2ch (1H, 1H/F/OTG) USB3.0/2.0×1ch (DRD)	USB2.0×1ch (H/F) USB3.0/2.0×1ch (DRD)
Gbit Ether	1ch	1ch	1ch	1ch
CAN	2ch (support CAN-FD)	2ch (support CAN-FD)	2ch (support CAN-FD)	2ch (support CAN-FD)
PCIe	2ch (Rev2.0 1Lane) one of the 2ch is shared with SATA	2ch (Rev2.0 1Lane)	2ch (Rev2.0 1Lane) one of the 2ch is shared with SATA	1ch (Rev2.0 1Lane)
SATA	1ch (Pin Shared)	No	1ch (Pin Shared)	No
Package	1022-pin FCBGA, 29mm×29mm 0.8mm ball pitch	1022-pin FCBGA, 29mm×29mm 0.8mm ball pitch	1022-pin FCBGA, 29mm×29mm 0.8mm ball pitch	552-pin FCBGA, 21mm×21mm 0.8mm ball pitch

Pin Compatible —

RZ/Five (RISC-V) Features and Specification

The RZ/Five is an entry-class general-purpose Linux MPU with a 64-bit RISC-V architecture.

- General-purpose MPU adopting an Open Instruction Set Architecture RISC-V
- Provide development environment to easy mutual migration between ARM and RISC-V
- General-purpose MPU specialized for IoT Edge

Items	RZ/Five
CPU	64bit RISC-V CPU Core AndesCore™ AX45MP Single core 1.0 GHz
DRAM I/F	16-bit × 1ch DDR4-1600/DDR3L-1333 w/ECC
USB	USB2.0 × 2ch (1Host, 1Host/Function/OTG)
Gbit Ether	2ch : 13mm × 13mm Package 1ch : 11mm × 11mm Package
CAN	2ch (support CAN-FD)
12-bit ADC	2ch
Package	361-pin, LFBGA, 13mm × 13mm, 0.5mm pitch 266-pin, LFBGA, 11mm × 11mm, 0.5mm pitch

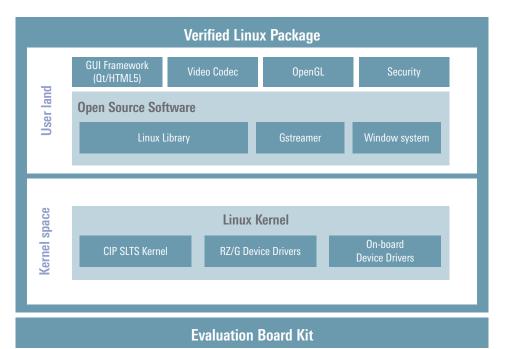


Super Long Term Software Support

The Linux kernel for Renesas RZ MPUs is a Super Long Term Support (SLTS) kernel based on the Civil Infrastructure Platform (CIP). This solution meets the long-term operation needs of manufacturers of industrial infrastructure and building automation equipment. The CIP SLTS Linux kernel supports countermeasures against vulnerability to security attacks with a longterm maintenance period of 10 years or more. This reduces Linux maintenance costs and simplifies adoption of reliable industrial-grade Linux.

Verified Linux Package(VLP) Reduces Cost and Simplifies Design

The "Verified Linux Package (VLP)" for the RZ/G series is the basic software (CIP SLTS Kernel, RZ/G Device Driver, multimedia, graphics, security, etc). This packaged software is verified by Renesas and is available from the Renesas RZ Linux platform site. With VLPs, you can start developing applications quickly while minimizing Linux maintenance resources.



GUI Framework

- Ot application framework
- HTML5 application framework

Multimedia

- H.264 Codec
- H.265 Decoder
- 3D graphics

Secure Middle Ware

- Encrypted kernel boot
- Security communication
- Secure storage

CIP SLTS Kernel

- Civil Infrastructure Platform project
- 10+ years super long term support Reliability/Security/Real-time

Flexible Development Kits

RZ/G2 development kits support the industry standard 96Boards specification and SMARC specification to enable evaluation and speed development with wide variety of mezzanine boards and existing carrier boards. Renesas provides circuit schematics, component BOMs, and board layout data to make it easy to spin your own custom hardware.

RZ/G3S SMARC Module + Carrier Board II



- RZ/G3S SMARC Module
 - Size: 82mm × 80mm
 - Processor: RZ/G3S
 - Main Memory: 1GB LPDDR4 (1GB \times 1)
 - QSPI NOR FLASH: 16MB
 - eMMC Memory: 64GB
 - External Storage: micro SD × 2
 - A/D Converter
 - JTAG connector

- Carrier Board II
 - Size: 190mm × 130mm
 - PCle 4-lane slot
 - M.2 Key E interface, M.2 Key B interface and SIM card interface
 - Gigabit Ethernet × 2
 - USB2.0 \times 2ch (OTG \times 1ch, Host \times 1ch)
 - CAN-FD \times 2

- External Storage: micro SD × 1
- Audio Line In × 1
- Audio Line Out × 1
- $PMOD \times 2$
- USB-Type C for Power Input

■ RZ SMARC v2.1 Module + Carrier Board



- RZ/G2L, RZ/G2LC, RZ/G2UL SMARC Module
 - Size: 82mm \times 50mm
 - Processor: RZ/G2L, RZ/G2LC, RZ/G2UL
 - Main Memory: 2GB DDR4 (1GB \times 2) *G2UL: 1GB (1GB \times 1)
 - QSPI NOR FLASH: 16MB
 - eMMC Memory: 64GB
 - External Storage: micro SD \times 1
 - A/D Converter Interface × 2
 - JTAG connector



- Size: 82mm × 50mm - Processor: RZ/Five
 - Main Memory: 1GB DDR4 (1GB x 1)
 - QSPI NOR FLASH: 16MB
 - eMMC Memory: 64GB
 - External Storage: micro SD x 1
 - A/D Converter Interface × 2
 - JTAG connector

- Carrier Board
 - Size: 150mm × 90mm
 - Gigabit Ethernet × 2
 - USB2.0 \times 2ch (OTG \times 1ch, Host \times 1ch)
 - MIPI CSI-2 Camera connector (can connect to Google Coral Camera)
 - Micro HDMI (output) connector
 - CAN-FD \times 2

- External Storage: micro SD × 1
- Audio Line In x 1
- Audio Line Out × 1
- $PMOD \times 2$
- USB-Type C for Power Input

■ RZ/G2H, G2M, G2N Development Kit (96Boards format compatible)



- Main Memory: 4 GB DDR4
- OSPI NOR FLASH: 64MB
- I²C EEPROM: 512bytes
- External Storage: micro SD × 1
- Connectivity: USB 2.0 × 2ch, USB 3.0×1 ch, GbE $\times 1$
- HDMI out / LVDS out or MIPI DSI out
- Wi-Fi + BT

RZ/G2E Development Kit (96Boards format compatible)



- Main Memory: 2 GB DDR3L
- QSPI NOR FLASH: 64MB
- I²C EEPROM: 512bytes
- External Storage: micro SD x 1
- Connectivity: USB 2.0 × 2ch, USB 3.0×1 ch, GbE $\times 1$
- HDMI out / LVDS out or MIPI DSI out
- Wi-Fi + BT



RZ/G Series Application

[IoT Application] Optimized for IoT devices by taking advantage of CPU performance, various interface functions, and security functions



Solar Inverter



Secure Home Gateway



EV Charger



Industrial Gateway



Infra Sensing Gateway



Smart Home Gateway



Smart Meter



Fleet Tracker & Asset Tracker



Smart Agriculture Gateway

RZ/G3S Group

CPU core

- Arm® Cortex®-A55 single-core Max. operating frequency: 1.1GHz
- Arm® Cortex®-M33 core x2 Max. operating frequency: 250MHz Cache memory (Cortex®-A55)
- L1 instruction cache: 32KB
- L1 data cache: 32KB
- L3 cache: 256KB

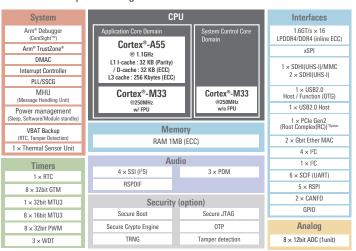
External memory

- Ability to connect LDDR4-SDRAM / DDR4-SDRAM via DDR dedicated bus
- Data bus width: 16 bits × 1 channel Storage interfaces
- USB 2.0 × 2 channels (Host only 1 channel/Host-Function 1 channel)
- SD host interface × 2 channels
- Multimedia card interface × 1 channel (Shared with SDHI)

Other peripheral functions

- 16-bit timer × 8 channels
- I²C bus interface × 4 channels
- Serial communication interface with FIFO (SCIF) × 6 channels
- SPI Multi I/O Bus Controller × 1 channel (4bit Double data rate)
- Serial Peripheral Interface (RSPI) × 5 channels
- Gigabit Ethernet controller × 2 channels
- Controller area network (CAN) interface × 2 channels (support CAN FD)
- 12-bit A/D converter × 8 channels
- Interrupt controller
- Clock generator (CPG): on-chip PLL
- On-chip debug function

■ RZ/G3S Group Block Diagram



RZ/Five [RISC-V] Group

CPU core

■ 64bit RISC-V CPU Core AndesCore™ AX45MP Single core 1.0GHz

Cache memory

- L1 instruction Cache: 32KB
- L1 data cache: 32KB
- L2 cache: 256KB

External memory

- Ability to connect DDR4-SDRAM / DDR3L-SDRAM via DDR dedicated bus
- Data bus width: 16 bits × 1 channel Audio functions
- Serial sound interface × 4 channels Storage interfaces
- USB 2.0 × 2 channels (Host only 1 channel/Host-Function 1 channel)
- SD host interface × 2 channels
- Multimedia card interface × 1 channel (Shared with SDHI)

Other peripheral functions

- 16-bit timer × 8 channels ■ I²C bus interface × 4 channels
- Serial communication interface with
- FIFO (SCIF) × 5 channels
- Serial communication interface (SCI) × 2 channels
- SPI Multi I/O Bus Controller × 1 channel (4bit Double data rate)
- Serial Peripheral Interface (RSPI) × 3 channels
- Gigabit Ethernet controller × 2 channels
- Controller area network (CAN) interface × 2 channels (support CAN FD)
- 12-bit A/D converter × 2 channels
- Interrupt controller
- Clock generator (CPG): on-chip PLL
- On-chip debug function

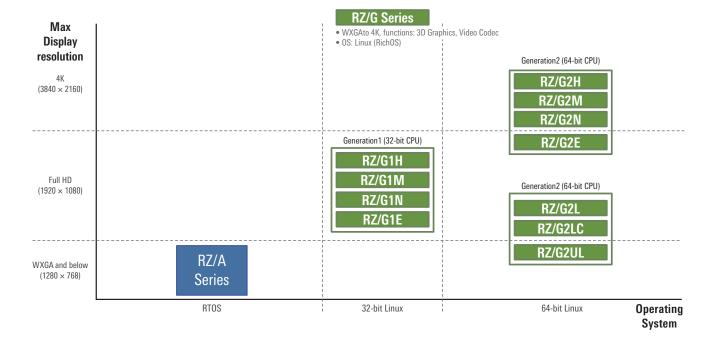
■ RZ/Five [RISC-V] Group Block Diagram

System	CPU	Interfaces
Debugger	Application Core Domain	1.6/1.3GT/s × 16
16ch DMAC	AX45MP Single (1GHz) With SIMD / FPU	DDR4/DDR3L (inline ECC)
Interrupt Controller	I-L1\$: 32KB (Parity), D-L1\$: 32KB (ECC)	1 × SPI Multi I/O (4-bit DDR)
PLL/SSCG	TCM (ILM/DLM): Total 128KB (ECC)	2 × SDHI(UHS-I)/MMC
	L2\$: 128KB (ECC)	1 × USB2.0 Host
	224. 125/15 (255)	1 × USB2.0 Host / Function
Timers	Internal Memory	2 × 100/1000
1 × 32-bit MTU3	SRAM: 128KB (ECC)	Ether MAC
8 × 16-bit MTU3	0	4 × I ² C
1 × WDT	Security Secure Boot	2 × SCI 8/9-bit (incl. IrDA)
		5 × SCIF (UART)
A l	Crypto Engine	3 × RSPI
Analog	Secure JTAG	4 × SSIF2
2 input 12-bit ADC (1 unit)	TRNG	2 × CAN-FD
Thermal Sensor	OTP 1Kbit	GPI0

[HMI Application] The HMI can be made more expressive by making full use of the 3D graphics and video capabilities.



HMI Solutions





RZ/G2L Group

CPU core

- Arm® Cortex®-A55, dual-core or single-core
 Max. operating frequency: 1.2GHz
- Arm® Cortex®-M33, single-core Max. operating frequency: 200MHz

Cache memory (Cortex®-A55)

- L1 instruction cache: 32KB
- L1 data cache: 32KB
- L3 cache: 256KB

External memory

- Ability to connect DDR4-SDRAM / DDR3L-SDRAM via DDR dedicated bus
- Data bus width: 16 bits × 1 channel 3D graphics
- Arm Mali™-G31 GPU

Video functions

- Video display interface:
 MIPI DSI × 1 channel or Digital parallel output × 1 channel
- Video input interface:
 MIPI CSI-2 × 1 channel or Digital parallel input × 1 channel
- Video codec module: VCPL4 × 1 channel
- Video image processing functions (Resizer and Color Space / Color Format Conversion)

Audio functions

- Serial sound interface × 4 channels Storage interfaces
- USB 2.0 × 2 channels (Host only 1 channel/Host-Function 1 channel)
- SD host interface × 2 channels
- Multimedia card interface x 1 channel (Shared with SDHI)

Other peripheral functions

- 32-bit timer × 1 channel
- 16-bit timer × 8 channels
- PWM timer × 8 channels
- I²C bus interface × 4 channels
- Serial communication interface with FIFO (SCIF) × 5 channels
- Serial communication interface (SCI) × 2 channels
- SPI Multi I/O Bus Controller× 1 channel (8bit Double data rate)
- Serial Peripheral Interface (RSPI) × 3channels
- Gigabit Ethernet controller × 2 channels
- Controller area network (CAN) interface
 × 2 channels (support CAN FD)
- 12-bit A/D converter × 8 channels
- Interrupt controller
- Clock generator (CPG): on-chip PLL
- On-chip debug function

■ RZ/G2L Group Block Diagram

System		CPU		Interfaces
Arm® Debugger	Cortex®-A55 (Cortex®-A55(#)		1.6/1.3GT/s × 16
(CoreSight™)	1.2GHz	1.2GHz		DDR4/DDR3L (inline ECC)
Arm® TrustZone®	Neon™/VFP I-L1\$: 32KB (Parity) I-			1 × SPI Multi I/0
16ch DMAC	D-L1\$: 32KB (ECC) D			(8-bit DDR)
Interrupt Controller	L2\$: 0KB	L2\$: 0KB	Cortex®-M33 @200MHz	1 × SDHI (UHS-I)/MMC
PLL/SSCG	L3\$(Shared) : 2	256KB (ECC)	@Z00IVII1Z	1 × SDHI (UHS-I)
		B/Lower and		1 × USB2.0 Host
	D.A	Memory	2)	1 × USB2.0
	RA	M 128KB (EC	3)	Host / Function
Timers	Video & Graphics		2 × 100/1000Mbps	
1 × 32-bit MTU3			Camera In	Ether MAC
8 × 16-bit MTU3	3D GPU Arm® Mali™-G	(MAIDLOC	SI-2 4-lane, Parallel)	2 × I ² C, 2 × I ² C
8 × 32-bit PWM	Allii ividii -U	-	isplay Out	
3 × WDT	H.264 Enc/De		SI 4-lane, Parallel)	2 × SCI 8/9-bit
3 × Wb1	1920 × 1080 @3	Ofne	a Caalina Hait	5 × SCIF (UART)
		· imag	e Scaling Unit	3 × RSPI
	Se	curity (option	1)	2 × CAN-FD
Analog	Secure Boot	t Devi	ice Unique ID	GPI0
8 × 12-bit ADC	Crypto Engin	e JT	AG Disable	Audio
	TRNG		OTP 4Kbit	
				4 × SSI (I ² S)

RZ/G2LC Group

CPU core

- Arm® Cortex®-A55, dual-core or single-core
 Max. operating frequency: 1.2GHz
- Arm® Cortex®-M33, single-core
 Max. operating frequency: 200MHz

Cache memory (Cortex®-A55)

- L1 instruction cache: 32KB
- L1 data cache: 32KB
- L3 cache: 256KB

External memory

- Ability to connect DDR4-SDRAM / DDR3L-SDRAM via DDR dedicated bus
- Data bus width: 16 bits × 1 channel 3D graphics
- Arm Mali[™]-G31 GPU

Video functions

- Video display interface: MIPI DSI × 1 channel
- Video input interface: MIPI CSI-2 × 1 channel
- Video image processing functions (Resizer and Color Space / Color Format Conversion)

Audio functions

- Serial sound interface × 2 channels Storage interfaces
- USB 2.0 × 2 channels (Host only 1 channel/Host-Function 1 channel)
- SD host interface × 2 channels
- Multimedia card interface × 1 channel (Shared with SDHI)

Other peripheral functions

- 32-bit timer × 1 channel
- 16-bit timer × 5 channels
- PWM timer × 4 channels
- I²C bus interface × 4 channels
 Social communication interface with
- Serial communication interface with FIFO (SCIF) × 3 channels
- Serial communication interface (SCI) × 2 channels
- SPI Multi I/O Bus Controller× 1 channel (4bit Double data rate)
- Serial Peripheral Interface (RSPI) × 3channels
- Gigabit Ethernet controller × 1 channel
- Controller area network (CAN) interface
 × 2 channels (support CAN FD)
- Interrupt controller
- Clock generator (CPG): on-chip PLL
- On-chip debug function

RZ/G2LC Group Block Diagram

RZ/GZLG Group Bio	ock Diagrar	n				
System		CF	υ			Interfaces
Arm® Debugger (CoreSight™)	Cortex®-A55 1.2GHz Neon™/VFP	Cortex ⁰ 1.20 Neon ¹	GHz			1.6/1.3GT/s × 16 DDR4/DDR3L (inline ECC)
Arm® TrustZone®	I-L1\$: 32KB (Parity)	I-L1\$: 32K	(B (Parity)		Ш	1 × SPI Multi I/O
16ch DMAC	D-L1\$: 32KB (ECC) L2\$: 0KB	D-L1\$: 32 L2\$:		Cortex®-M33	Н	(4-bit DDR)
Interrupt Controller				@200MHz	Ш	1 × SDHI (UHS-I)/MMC 1 × SDHI (UHS-I)
PLL/SSCG	L3\$(Shared) :	256KB	ECC)		H	
		Men	norv		ıŀ	1 × USB2.0 Host
	RAM 128KB (ECC)				1 × USB2.0 Host / Function	
Timers	Graphics		П	1 × 100/1000Mbps		
1 × 32-bit MTU3	3D GPU Camera In Eth			Ether MAC		
5 × 16-bit MTU3	Arm® Mali™-G31 (MIPI CSI-	(MIPI CSI-2 4-lane)		П	$2 \times I^2C$, $2 \times I^2C$	
6 × 32-bit PWM	Imana Caslina	. Hais	Display Out		П	2 × SCI 8/9-bit
3 × WDT	Image Scaling	JUIIL	(IVII)	PI DSI 4-lane)	П	4 × SCIF (UART)
					П	3 × RSPI
	5	Security	(option)		2 × CAN-FD
	Secure Bo	ot	Devi	ce Unique ID		GPI0
	Crypto Eng	ine	JT	AG Disable	П	Audio
	TRNG		(TP 4Kbit		3 × SSI (I ² S)
	TRNG		(TP 4Kbit		

RZ/G2UL Group

CPU core

- Arm® Cortex®-A55, single-core Max. operating frequency: 1.0GHz
- Arm® Cortex®-M33, single-core
 Max. operating frequency: 200MHz

Cache memory (Cortex®-A55)

- L1 instruction cache: 32KB
- L1 data cache: 32KB
- L3 cache: 256KB
- External memory
- Ability to connect DDR4-SDRAM / DDR3L-SDRAM via DDR dedicated bus
- Data bus width: 16 bits × 1 channel Video functions
- Video display interface:
 Digital parallel output × 1 channel
- Video input interface:
 MIPI CSI-2 × 1 channel
- Video image processing functions (Resizer and Color Space / Color Format Conversion)

Audio functions

- Serial sound interface × 4 channels Storage interfaces
- USB 2.0 × 2 channels (Host only 1 channel/Host-Function 1 channel)
- SD host interface × 2 channels
- Multimedia card interface x 1 channel (Shared with SDHI)

Other peripheral functions

- 16-bit timer × 8 channels
- I^2C bus interface × 4 channels
- Serial communication interface with FIFO (SCIF) × 5 channels
- Serial communication interface (SCI) × 2 channels
- SPI Multi I/O Bus Controller× 1 channel (4bit Double data rate)
- Serial Peripheral Interface (RSPI) × 3channels
- Gigabit Ethernet controller × 2 channels
- Controller area network (CAN) interface
 × 2 channels (support CAN FD)
- 12-bit A/D converter × 2 channels
- Interrupt controller
- Clock generator (CPG): on-chip PLL
- On-chip debug function

■ RZ/G2UL Group Block Diagram

System	СР	U		Interfaces
Arm® Debugger (CoreSight™)	Cortex®-A55 1.0GHz			1.6/1.3GT/s × 16 DDR4/DDR3L (inline ECC)
Arm® TrustZone®	Neon™/VFP I-L1\$: 32KB (Parity) D-L1\$: 32KB (ECC)			1 × SPI Multi I/O (4-bit DDR)
16ch DMAC Interrupt Controller	L2\$: OKB		Cortex®-M33 @200MHz	1 × SDHI (UHS-I)/MMC
PLL/SSCG	L3\$ (Shared): 256KB (I	ECC)	@ZUUIVII IZ	1 × SDHI (UHS-I)
	D/L a ser			1 × USB2.0 Host
	RAM 128		:)	1 × USB2.0 Host / Function
Timers	Graphics Image Scaling Unit Display Out (Parallel-IF)			2 × 100/1000Mbps Ether MAC
8 × 16-bit MTU3 (#)				2 × I ² C, 2 × I ² C
2 × WDT				2 × SCI 8/9-bit
	Camera In (MIPI CSI-2 4-lane)			5 × SCIF (UART)
	Camera III (IVIII	3 × RSPI		
Analog	Security	(option))	2 × CAN-FD
2 × 12-bit ADC	Secure Boot	Devi	ce Unique ID	GPI0
	Crypto Engine		AG Disable	Audio
	TRNG	C	TP 1Kbit	4 × SSI (I ² S)

RZ/G2H Group

CPU core

- Arm® Cortex®-A57, quad-core Max. operating frequency: 1.5GHz
- Arm® Cortex®-A53, quad-core Max. operating frequency: 1.2GHz
- Arm® Cortex®-R7, single-core Max. operating frequency: 800MHz

Cache memory (Cortex®-A57)

- L1 instruction cache: 48KB
- L1 data cache: 32KB
- L2 cache: 2MB

Cache memory (Cortex®-A53)

- L1 instruction cache: 32KB
- L1 data cache: 32KB
- L2 cache: 512KB

Cache memory (Cortex®-R7)

- L1 instruction cache: 32KB
- L1 data cache: 32KB
- I-TCM: 32KB
- D-TCM: 32KB

External memory

- Ability to connect LPDDR4-SDRAM via DDR dedicated bus
- Data bus width: 32 bits × 2 channels External expansion
- Ability to connect flash ROM or SRAM directly
- Data bus width: 8/16 bits
- PCI Express 2.0 : 1 Lane × 2 channels (one of PHY is shared with Serial ATA)
 3D graphics
- PowerVR[™] GX6650

Video functions

- Video display interface × 3 channels (1 channel: HDMI(option), 1 channel: LVDS, 1 channel: RGB888)
- Video input interface x 4 channels (2 channels: MIPI CSI-2, 2 channels: Digital(RGB/YCbCr))

- Video codec module: VCP4 x 1 channel
- IP converter module
- Video image processing functions (color conversion, image enlargement/reduction, filtering)

Audio functions

- Sampling rate converter × 10 channels
- Serial sound interface × 10 channels Storage interfaces
- USB 3.0 DRD × 1 channel
- USB 2.0 × 2 channels (Host only 1 channel/Host-Function 1 channel)
- SD host interface × 4 channels
- Multimedia card interface × 2 channels
- Serial ATA interface × 1 channel Other peripheral functions
- 32-bit timer × 15 channels
- PWM timer × 7 channels
- I²C bus interface × 7 channels
- Serial communication interface (SCIF)
 × 6 channels
- Quad serial peripheral interface (QSPI)
 × 2 channels (boot support)
- Clock-synchronous serial interface (MSIOF) × 4 channels (SPI/IIS support)
- Ethernet controller with AVB support (support for IEEE 802.1BA, IEEE 802.1AS, IEEE 802.1Qav, and IEEE 1722)
- Controller area network (CAN) interface × 2 channels
- Interrupt controller (INTC)
- Clock generator (CPG): on-chip PLL
- On-chip debug function

■ RZ/G2H Group Block Diagram

RZ/G2H Group Blo	ck Diagram	
System	CPU	Connectivity
System controller	4 × Cortex®-A57 1.5GHz 4 × Cortex®-A53 1.2GHz 1 × Cortex®-R7 800MHz	2 × PCle2.0 (1Lane)
System RAM: 384KB	L1 I\$ 48KB L1 I\$ 32KB L1 I\$ 32KB	SATA (Rev.3.2) (shared)
Thermal Sensor	L1 D\$ 32KB L1 D\$ 32KB L1 D\$ 32KB	USB3.0/2.0 (DRD)
JTAG Debug	NEON/VFPv4 NEON/VFPv4 VFPv3-D16	4 × USB2.0 (2H, 2H/F/OTG)
(CoreSight™)	L2 cache: 2MB with ECC L2 cache: 512KB with ECC I-TCM 32KB, D-TCM 32KB with ECC	Ethernet AVB (1Gbps)
Timers	3D Graphics	2 × CAN2.0B / 2 × CAN-FD
26 × 32-bit Timer	PowerVR GX6650	6 × UART, 5 × H-UART
15 × 32-bit Interval	2D/3D tile based 600MHz	4 × SPI
WDT	Video Codec	7 × I ² C; 1 × DVFS ctrl
7 × PWM out	Up to 4K resolution	Memory I/F
Audio IPs	(2 channels)	32-bit × 2ch LPDDR4-3200 access cache
Audio router w/10 ASRC,	Video IP	16-bit ExtBus/SRAM
mixer, 10 I ² S (6ch TDM), 90ch Audio DMA	3 × Display out 1 × Digital out, 1 × LVDS	
Secure IP	1 × HDMI 2 × Fine Display Processor 8 × Video in	1 × QSPI (4/8-bit selectable) or 1 × Hyperflash
Crypto engine	2 × MIPI CSI-2	4 × SDIO (SDR104)
(AES, DES, Hash, RSA, TRNG)	(1 × 4L, 1 × 2L) 2 × Digital	2 × eMMC (5.0, HS400)

FC-BGA: 29 × 29mm² 1022-pins, 0.8mm pitch



RZ/G2M Group

CPU core

- Arm® Cortex®-A57, dual-core Max. operating frequency: 1.5GHz
- Arm® Cortex®-A53, quad-core Max. operating frequency: 1.2GHz
- Arm® Cortex®-R7, single-core Max. operating frequency: 800MHz

Cache memory (Cortex®-A57)

- L1 instruction cache: 48KB
- L1 data cache: 32KB
- L2 cache: 2MB

Cache memory (Cortex®-A53)

- L1 instruction cache: 32KB
- L1 data cache: 32KB
- L2 cache: 512KB

Cache memory (Cortex®-R7)

- L1 instruction cache: 32KB
- L1 data cache: 32KB
- I-TCM: 32KB
- D-TCM: 32KB

External memory

- Ability to connect LPDDR4-SDRAM via DDR dedicated bus
- Data bus width: 32 bits × 2 channels External expansion
- Ability to connect flash ROM or SRAM directly
- Data bus width: 8/16 bits
- PCI Express 2.0 : 1 Lane \times 2 channels (one of PHY is shared with Serial ATA)
- 3D graphics ■ PowerVR[™] GX6250

Video functions

- Video display interface × 3 channels (1 channel: HDMI(option), 1 channel: LVDS, 1 channel: RGB888)
- Video input interface × 4 channels (2 channels: MIPI CSI-2, 2 channels: Digital(RGB/YCbCr))

■ Video codec module: VCP4 × 1 channel

- IP converter module
- Video image processing functions (color conversion, image enlargement/ reduction, filtering)

Audio functions

- Sampling rate converter × 10 channels
- Serial sound interface × 10 channels Storage interfaces
- USB 3.0 DRD × 1 channel
- USB 2.0×2 channels (Host only 1 channel/Host-Function 1 channel)
- SD host interface \times 4 channels
- Multimedia card interface × 2 channels Other peripheral functions
- 32-bit timer × 15 channels
- PWM timer × 7 channels
- I²C bus interface × 7 channels
- Serial communication interface (SCIF) × 6 channels
- Quad serial peripheral interface (QSPI) × 2 channels (boot support)
- Clock-synchronous serial interface (MSIOF) × 4 channels (SPI/IIS support)
- Ethernet controller with AVB support (support for IEEE 802.1BA, IEEE 802.1AS, IEEE 802.10av, and IEEE 1722, GMII/MII interface, PHY device connection
- Ethernet controller with AVB support (support for IEEE 802.1BA, IEEE 802.1AS, IEEE 802.10av, and IEEE 1722)
- Controller area network (CAN) interface × 2 channels
- Interrupt controller (INTC)
- Clock generator (CPG): on-chip PLL
- On-chip debug function

■ RZ/G2M Group Block Diagram

System	СРИ
System controller	2 × Cortex®-A57 1.5GHz 4 × Cortex®-A53 1.2GHz 1 × Cortex®-R7 800MHz
System RAM: 384KB	L1 I\$ 48KB L1 I\$ 32KB L1 I\$ 32KB
Thermal Sensor	L1 D\$ 32KB L1 D\$ 32KB L1 D\$ 32KB
JTAG Debug	NEON/VFPv4 NEON/VFPv4 VFPv3-D16
(CoreSight™)	L2 cache: 2MB with ECC L2 cache: 512KB with ECC I-TCM 32KB, D-TCM 32KB with ECC

26 × 32-bit Timer 15 × 32-bit Interval WDT

7 × PWM out

Audio IPs Audio router w/10 ASRC, mixer, 10 I2S (6ch TDM). 90ch Audio DMA

Secure IP Crypto engine (AES, DES, Hash, RSA, TRNG)

3D Graphic

PowerVR GX6250 2D/3D tile based 600MHz

Video Codec

Up to 4K resolution (2 channels)

Video IP

3 × Display Out × Digital out, 1 × LVDS 1 × HDMI 8 × Video in 4 × Video Signal Processor 2 × MIPI CSI-2 (1 × 4L, 1 × 2L) 2 × Digital

FC-BGA: 29 × 29mm² 1022-pins, 0.8mm pitch

Connectivity
2 × PCle2.0 (1Lane)
USB3.0/2.0 (DRD)
2 × USB2.0 (1H, 1H/F/0TG)
Ethernet AVB (1Gbps)
$2 \times \text{CAN2.0B} / 2 \times \text{CAN-FD}$
$6 \times \text{UART}$, $5 \times \text{H-UART}$ $4 \times \text{SPI}$ $7 \times \text{I}^2\text{C}$; $1 \times \text{DVFS ctrl}$

Memory I/F

32-bit × 2ch LPDDR4-3200 access cache Raw NAND

(8/16-bit, ONFI 1.x, ECC 1-8-bits)

16-bit ExtBus/SRAM 1 × QSPI (4/8-bit selectable)

or 1 × Hyperflash 4 × SDIO (SDR104)

2 × eMMC (5.0, HS400)

RZ/G2N Group

CPU core

- Arm® Cortex®-A57, quad-core Max. operating frequency: 1.5GHz
- Arm® Cortex®-R7, single-core Max. operating frequency: 800MHz

Cache memory (Cortex®-A57)

- L1 instruction cache: 48KB
- L1 data cache: 32KB
- L2 cache: 2MB

Cache memory (Cortex®-R7)

- L1 instruction cache: 32KB L1 data cache: 32KB
- I-TCM: 32KB
- D-TCM: 32KB

External memory

- Ability to connect LPDDR4-SDRAM via DDR dedicated bus
- Data bus width: 32 bits × 1 channel External expansion
- Ability to connect flash ROM or SRAM directly
- Data bus width: 8/16 bits
- PCI Express 2.0 : 1 Lane \times 2 channels (one of PHY is shared with Serial ATA)

3D graphics

■ PowerVR[™] GE7800

Video functions

- Video display interface × 3 channels (1 channel: HDMI(option), 1 channel: LVDS, 1 channel: RGB888)
- Video input interface × 4 channels (2 channels: MIPI CSI-2, 2 channels: Digital(RGB/YCbCr))

- Video codec module: VCP4 × 1 channel
- IP converter module
- Video image processing functions (color conversion, image enlargement/ reduction, filtering)

Audio functions

- Sampling rate converter × 10 channels
- Serial sound interface × 10 channels Storage interfaces
- USB 3.0 DRD × 1 channel USB 2.0×2 channels (Host only 1
- channel/Host-Function 1 channel) ■ SD host interface × 4 channels
- Multimedia card interface × 2 channels
- Serial ATA interface × 1 channel
- Other peripheral functions
- 32-bit timer x 15 channels
- PWM timer × 7 channels
- I^2C bus interface \times 7 channels Serial communication interface (SCIF) ×
- 6 channels Quad serial peripheral interface (QSPI) × 2 channels (boot support)
- Clock-synchronous serial interface (MSIOF) × 4 channels (SPI/IIS support)
- Ethernet controller with AVB support (support for IEEE 802.1BA, IEEE 802.1AS, IEEE 802.10av, and IEEE 1722)
- Controller area network (CAN) interface × 2 channels
- Interrupt controller (INTC)
- Clock generator (CPG): on-chip PLL
- On-chip debug function

■ RZ/G2N Group Block Diagram

System	CI	PU
System controller	2 × Cortex®-A57 1.5GHz	1 × Cortex®-R7 800MHz
System RAM: 384KB	L1 I\$ 48KB	L1 I\$ 32KB
Thermal Sensor	L1 D\$ 32KB	L1 D\$ 32KB
JTAG Debug	NEON/VFPv4	VFPv3-D16
(CoreSight™)	L2 cache: 1MB with ECC	I-TCM 32KB, D-TCM 32KB with ECC
Timoro	3D C*	anhiaa

26 × 32-bit Timer 15 × 32-bit Interval WDT Video Codec

Audio IPs Audio router w/10 ASRC, mixer, 10 I²S (6ch TDM), 90ch Audio DMA

7 × PWM out

	5	Secure	IP	
	Cry	/pto er	ngine	
IVEC	DEC	Hach	DC V	TRNC

cache: 1MB with ECC I-TCM 32KB, D-TCM 32KB with
3D Graphics
PowerVR GE7800 2D/3D tile based 600MHz
ZD/OD the based oppivitiz

Up to 4K resolution (2 channels) Video IP 3 × Display out × Digital out, 1 × LVDS 1 × HDMI 2 × Video Signal Processor 1 x Fine Display Processor

I × HUIVII	1 × 11110 Biopidy 110000001
8 × Video in 2 × MIPI CSI-2 (1 × 4L, 1 × 2L) 2 × Digital	
FC-BGA: 29 × 29mm ²	1022-pins, 0.8mm pitch

Connectivity
2 × PCle2.0 (1Lane)
SATA (Rev.3.2) (shared)
USB3.0/2.0 (DRD)
2 × USB2.0 (1H, 1H/F/0TG)
Ethernet AVB (1Gbps)
2 × CAN2.0B / 2 × CAN-FD
$6 \times \text{UART}$, $5 \times \text{H-UART}$ $4 \times \text{SPI}$ $7 \times \text{I}^2\text{C}$; $1 \times \text{DVFS ctrl}$
Memory I/F

IVIGILIOTY 1/1
32-bit × 1ch LPDDR4-3200 access cache
Raw NAND (8/16-bit, ONFI 1.x, ECC 1-8-bits)
16-bit ExtBus/SRAM
$\begin{array}{c} 1 \times \text{QSPI (4/8-bit selectable)} \\ \text{or } 1 \times \text{Hyperflash} \end{array}$
4 × SDIO (SDR104)
2 × eMMC (5.0, HS400)

RZ/G2E Group

CPU core

- Arm® Cortex®-A53, quad-core Max. operating frequency: 1.2GHz
- Arm® Cortex®-R7, single-core
 Max. operating frequency: 800MHz

Cache memory (Cortex®-A53)

- L1 instruction cache: 32KB
- L1 data cache: 32KB
- L2 cache: 256KB
- Cache memory (Cortex®-R7)
- L1 instruction cache: 32KB
- L1 data cache: 32KB
- I-TCM: 32KB
- D-TCM: 32KB

External memory

- Ability to connect DDR3L-SDRAM via DDR dedicated bus
- Data bus width: 32 bits × 1 channel External expansion
- Ability to connect flash ROM or SRAM directly
- Data bus width: 8/16 bits
- PCI Express 2.0 : 1 Lane × 1 channel 3D graphics
- PowerVR[™] GE8300

Video functions

- Video display interface × 2 channels (2 channels: LVDS, 1 channel: RGB888)
- Video input interface x 3 channels (1 channels: MIPI CSI-2, 2 channels: Digital(RGB/YCbCr))

- Video codec module: VCP4 × 1 channel
- IP converter module
- Video image processing functions (color conversion, image enlargement/ reduction, filtering)

Audio functions

- Sampling rate converter × 10 channels
- Serial sound interface × 10 channels
 Storage interfaces
- USB 3.0 DRD × 1 channel
- USB 2.0 × 1 channel (Host-Function 1 channel)
- SD host interface × 3 channels
- Multimedia card interface x 1 channel Other peripheral functions
- 32-bit timer × 15 channels
- PWM timer × 7 channels
- I^2C bus interface \times 8 channels
- Serial communication interface (SCIF) × 6 channels
- Quad serial peripheral interface (QSPI)
 × 2 channels (boot support)
- Clock-synchronous serial interface (MSIOF) × 4 channels (SPI/IIS support)
- Ethernet controller with AVB support (support for IEEE 802.1BA, IEEE 802.1AS, IEEE 802.1Qav, and IEEE 1722)
- Controller area network (CAN) interface × 2 channels
- Interrupt controller (INTC)
- Clock generator (CPG): on-chip PLL
- On-chip debug function

■ RZ/G2E Group Block Diagram

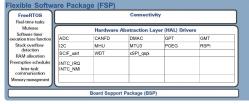
System	CI	Connectivity	
System controller	2 × Cortex®-A53 1.2GHz	2 × Cortex®-A53 1.2GHz 1 × Cortex®-R7 800MHz	1 × PCle2.0 (1Lane)
System RAM: 128KB	L1 I\$ 32KB	L1 I\$ 32KB	
Thermal Sensor	L1 D\$ 32KB	L1 D\$ 32KB	USB3.0/2.0 (DRD)
JTAG Debug	NEON/VFPv4	VFPv3-D16	USB2.0 (1H/F)
(CoreSight™)	L2 cache: 256KB with ECC	I-TCM 32KB, D-TCM 32KB with ECC	Ethernet AVB (1Gbps)
Timers	3D Gr	2 × CAN2.0B / 2 × CAN-FD	
26 × 32-bit Timer	PowerVR GE8300 2D/3D tile based 600MHz		6 × UART, 5 × H-UART
15 × 32-bit Interval			4 × SPI
WDT		8 × I ² C; 1 × DVFS ctrl	
WDI	Video	Codec	
7 × PWM out		Codec	Memory I/F
7 × PWM out		resolution	Memory I/F 32-bit DDR3L-1856
7 × PWM out	Up to FHD		32-bit DDR3L-1856
7 × PWM out Audio IPs Audio router w/10 ASRC, mixer, 10 I ² S (6ch TDM),	Up to FHD Vide 2 × Display out:	resolution	32-bit DDR3L-1856 access cache
7 × PWM out Audio IPs Audio router w/10 ASRC,	Up to FHD Vide 2 × Display out: (2 × LVDS or	resolution	32-bit DDR3L-1856 access cache Raw NAND
7 × PWM out Audio IPs Audio router w/10 ASRC, mixer, 10 I ² S (6ch TDM),	Up to FHD Vide 2 × Display out: (2 × LVDS or 1 × LVDS + 1 × DRGB)	resolution eo IP 2 × Video Signal Processor	32-bit DDR3L-1856 access cache Raw NAND (8-bit, ONFI 1.x,
7 × PWM out Audio IPs Audio router w/10 ASRC, mixer, 10 I°S (6ch TDM), 45ch Audio DMA Secure IP	Up to FHD Vide 2 × Display out: (2 × LVDS or 1 × LVDS + 1 × DRGB) 2 × Video in	resolution 2 v Video Signal Processor 1 × Fine Display Processor	32-bit DDR3L-1856 access cache Raw NAND (8-bit, ONFI 1.x, ECC 1-8-bits) 16-bit ExtBus/SRAM 1 × QSPI (4/8-bit selectable)
7 × PWM out Audio IPs Audio router w/10 ASRC, mixer, 10 I°S (6ch TDM), 45ch Audio DMA	Up to FHD Vide 2 × Display out: (2 × LVDS or 1 × LVDS + 1 × DRGB)	resolution 2 v Video Signal Processor 1 × Fine Display Processor	32-bit DDR3L-1856 access cache Raw NAND (8-bit, DNFI 1.x, ECC 1-8-bits)
7 × PWM out Audio IPs Audio router w/10 ASRC, mixer, 10 I'S (6ch TDM), 45ch Audio DMA Secure IP Crypto engine	Vide 2 × Display out: (2 × LVDS or 1 × LVDS + 1 × DRGB) 2 × Video in 1 × MIPI CSI-2 (1 × 2L) 1 × Digital	resolution 2 v Video Signal Processor 1 × Fine Display Processor	32-bit DDR3L-1856 access cache Raw NAND (8-bit, ONFI 1.x, ECC 1-8-bits) 16-bit ExtBus/SRAM 1 × QSPI (4/8-bit selectable)

Code Generation Support: Flexible Software Package (FSP) + Smart Configurator (SC)

(Supported products: RZ/G2L, RZ/G2LC, RZ/G2UL, RZ/G3S)

The FSP includes everything you'll need to start developing software: board-dependent programs, peripheral function drivers, middleware, and documentation on how to use them.

Smart Configurator is a utility based on the concept of "combining software components freely." The intuitive GUI makes it easy to configure pins and FSP driver settings and to generate source code customized for your use case. It works together with integrated development environments such as e^2 studio.







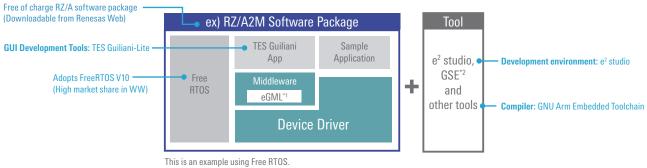
RZ/A Series

RZ/A Series Application



Benefits of RZ/A Series — Develop like MCUs

RZ/A series MPUs retain the ease-of-use of Renesas MCUs due to rich integrated development environments, and deliver higher performance than MCUs.



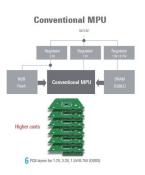
^{*1} embedded Graphics Multiplatform Library *2 Guiliani Streaming Editor

Benefits of RZ/A3UL

- 64bit CPU@1GHz RTOS MPU
- Choice of two memory I/Fs for different applications
 - Octal-SPI Flash/Octal-SPI RAM: For simple and low cost PCB design
 - DDR3L/DDR4: For high resolution HMI and camera use cases
- Pin-compatible RZ/A3UL (RTOS) and RZ/G2UL (Linux) for easy migration
- The 361-pin package is pin-compatible between RZ/A3UL and RZ/G2UL

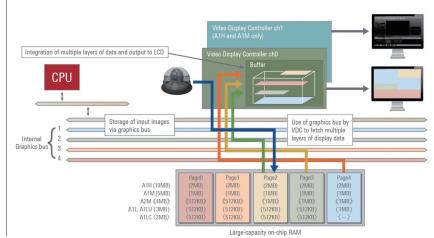
Benefits of RZ/A1 Group, and RZ/A2M MPUs

- Eliminate the need to design a high-speed interface
- Reduced mounting area
- Reduced PCB cost
- No DRAM procurement issues
- Reduced EMI noise





Include on-chip graphics display and camera input capabilities



DRP Library

- RZ/A2M MPUs with DRP improve image processing performance by 10X over RZ/A1 MPUs
 - $\, {\sf Dynamically \, Reconfigurable \, Processor \, (DRP) \, technology \, accelerates \, image \, processing}$
 - Enables hybrid e-Al solutions with DRP for image processing + CPU for inference

The RZ/A2M is designed around e-AI for smart appliances, network cameras, service robots, scanner products, and industrial equipment requiring high-speed image processing. The RZ/A2M combines a general-purpose MPU with Renesas' proprietary DRP technology for unique hybrid processing for image recognition and machine vision (MV), and AI processing works in conjunction with the Cortex®-A9, which preprocesses image data at high speed and extracts features for recognition target.



RZ/A3UL Group

- 64-bit Arm® Cortex®-A55 (1 GHz, single core)
- 16bit DDR3L/DDR4-1600 (in line ECC)
- Octal-SPI Flash/RAM IF
- Camera IF; MIPI CSI-2 (4-lane)
- Display IF; Parallel RGB888/RGB666
- 2x Gigabit Ethernet
- 2x CAN (CAN-FD)
- 2x USB2.0 (Host, Host/Peripheral)
- 2x SDHI (UHS-I, UHS-I/MMC)

■ RZ/A3UL Group Block Diagram

	0		
System	CF	Interfaces	
Arm Debugger	Cortex®-A55 1.0GHz NEON/VFP		DDR4/DDR3L (In line ECC) 16bit × 1.6/1.3Gbps
(CoreSight™)	I -L1\$: 32k	(B w/Parity	SPI Multi I/O or Octa IF
16 ch DMAC	D-L1\$: 32k L2\$: 0Kl		(4/8bit × 200Mbps)
Interrupt Controller			(Cache: 64bit line x 32 entries)
PLL/SSCG	L3\$ (Shared) :	256KB w/ECC	1 × SDHI (UHS-I)/MMC
Standby	Memory		1 × SDHI (UHS-I)
(Sleep/Module)	RAM128KB w/ECC		1 × USB2.0 Host
Timers	LCD Controller + Resize		1 × USB2.0 Host / Function
1 × 32bit MTU3	Image Scaling Unit		2 × 100/1000Mbps Ether MAC
8 × 16bit MTU3	Display Out (Parallel-IF)		4×1 ² C
1×WDT	Camera In (MIPI CSI-2 4-lane)		
			2 × SCI 8/9bit
	Analog	Audio	5 × SCIF (UART)
	2×12bit ADC	4 × SSI (I ² S)	3×RSPI
			2 × CAN-FD
			GPIO

RZ/A2M Group

CPU (Arm® Cortex®-A9)

- Operating frequency: 528MHz
- Single-precision/double-precision FPU
 Arm® NEON™

On-chip memory

Main graphics and camera input functions

- Video display controller (VDC6): 1 channel LCD output: Max. WXGA Screen superimposition: 3 layers Video input: Max. XGA
- CMOS camera input (CEU): 1 channel
 MIPI CSI-2 interface: 1 channel
- Distortion compensation unit (IMR): 1 channel
- 2D graphics engine: 1 channel
- Sprite engine: 1 channel
- JPEG coding engine: 1 channel

- Main memory interface functions

 NOR flash, SDRAM, NAND flash

 Serial flash: 1-bit/4-bit/8-bit: 1 channel, 8-bit: 1 channel (ability to run stored programs directly)
- SD/MMC host interface: 2 channels

Main communication functions

- USB 2.0 High Speed: 2 channels (Host/Function switchable)
- 10M/100M EtherMAC: 2 channels
- SCIF: 5 channels
- I²C: 4 channels SSI: 4 channels
- RSPI: 3 channels
- CAN-FD: 2 channels
- Optional functions

■ DRP (Dynamically Reconfigurable Processor)

Package

- 176-LFBGA (13mm×13mm, 0.8mm pitch)
- 256-LFBGA (11mm×11mm, 0.5mm pitch)
- 272-FBGA (17mm×17mm, 0.8mm pitch)
- 324-FBGA (19mm×19mm, 0.8mm pitch)

WDT RTC

DRP (option)

RZ/A2M Group Block	Dia	agram	
System		CF	υ
DMAC 16ch		Cortex®-A	9 528 MHz
Interrupt Controller PLL/SSCG		NEON	FPU
On-chip Debug			nory
Standby	١.	SRAM: 4MB	
(Sleep/Software/Deep/Module)		I CACHE: 32KB	D Cache: 32KB
(***)	L2 Cache: 128KB		e: 128KB
Timers OSTM		Grap	hics
32-bit × 3ch		VDC6 (LCDC)	LVDS
MTU3		Timing Controller	IMR-LS2
32-bit × 1ch		Digital Input	Sprite Engine
MTU3 16-bit × 8cb		CMOS Camera I/F	2D Graphics Engine
PWM 32-bit × 8ch	L	MIPI Camera I/F	JPEG Codec Engine
JZ-DIL X OUII			

Security (option)	
Secure Boot	
Crypto Engine	
TRNG	
Device Unique ID	
JTAG Disable	

I ² C
4ch
SCI
2ch
SCIF (UART)
5ch
RSPI 3ch
CAN-FD
2ch
Ethernet MAC
(100M: IEEE1588 v2)
2ch
IrDA
SSI (I ² S)
4ch
SPDIF
1ch
BSC (E×t. Bus I/F)
$HyperFlash^{\scriptscriptstyleTM}/HyperRAM^{\scriptscriptstyleTM}$
OctaFlash™ / OctaRAM™
SPI Multi I/O (DDR)
(1,4 or 8bit width)
NAND Flash I/F
(ONFI1.0, ECC)
USB2.0
HS 2ch Host/Peripheral/OTG SDHI (UHS-I)/MMC
SDHI (UHS-I)/IVIIVIC 2ch
GPI0

Interfaces

Analog ADC 12-bit × 8ch

RZ/A1H Group and RZ/A1M Group (Pin Compatible)

CPU (Arm® Cortex®-A9)

- Operating frequency: 400MHz
- Single-precision/double-precision FPU
- Arm® NEON™

On-chip memory

- RZ/A1H: 10MB
- RZ/A1M: 5MB

Main graphics and camera input functions

Video display controller (VDC5): 2 channels LCD output: Max. WXGA

Screen superimposition: 4 layers

Video input: Max. XGA (CVBS analog input supported)

- CMOS camera input (CEU): 1 channel
- PAL/NTSC decoder (DVDEC): 2 channels
- Distortion compensation unit (IMR): 1 channel
- Open VG accelerator: 1 channel
- JPEG coding engine: 1 channel

Main memory interface functions

- NOR flash, SDRAM, NAND flash
- QSPI serial flash: 2 channels (ability to run stored programs directly)
- SD host interface: 2 channels
- MMC host interface: 1 channel

Main communication functions

- USB 2.0 High Speed: 2 channels (Host/Function switchable)
- 10M/100M EtherMAC: 1channel
- SCIF: 8 channels
- I²C: 4 channels
- SSI: 6 channels
- RSPI: 5 channels
- Ethernet AVB: 1 channel
- CAN: 5 channels

Package

- 256-LFBGA (11mm × 11mm, 0.5mm pitch)
- 256-LFQFP (28mm × 28mm, 0.4mm pitch)
- 324-FBGA (19mm × 19mm, 0.8mm pitch)

■ RZ/A1H,and RZ/A1M Group Block Diagram

Memory
SRAM
A1H: 10MB/A1M: 5MB
SRAM L2 Cache
128 KB
Cache
32 KB + 32 KB

System

DMAC 16ch

Interrupt Controller

Clock Generation with SSCG

JTAG Debug

SCUX 4ch ASRC
CDROM DEC
Sound Generator

Analog ADC 12-bit × 8ch CPU

Cortex®-A9 400MHz

NEON FPU

Timers

MTU2

16-bit × 5ch

WDT

8-bit × 1ch

OS Timer

32-bit × 2ch

PWM Timer

16ch

Real-Time CLK

Graphics
Video Display Controller
2ch
OpenVG 1.1
Enhanced eng.
PAL/NTSC
dec. 2ch
CMOS Camera I/F
1ch
Fish Eye Correction
2ch
JPEG Engine

Interfaces 10/100 Ether MAC USB2.0 HS 2ch Host/Func NAND Flash External Bus 32-bit ROM, SRAM SDRAM, PCMCIA SPI Multi SCIF RSPI 8ch I^2C **IEBus** 1ch SSI (I2S) SPDIF SDHI MMC CAN MOST50 5ch 1ch Smart Card I/F LIN Master IrDA 2ch Ethernet AVB

RZ/A1LU Group

CPU (Arm® Cortex®-A9)

- Operating frequency: 400MHz
- Single-precision/double-precision FPU
- Arm® NEON™

On-chip memory

■ 3MB

Main graphics and camera input functions

- LCD controller (VDC5): 1 channel LCD output: Max. WXGA Screen superimposition: 3 layers Video input: Max. XGA
- CMOS camera input (CEU): 1 channel
- JPEG coding engine: 1 channel

Main memory interface functions

- NOR flash, SDRAM
- QSPI serial flash: 1 channel (ability to run stored programs directly)
- SD host interface: 2 channels
- MMC host interface: 1 channel

Main communication functions

- USB 2.0 High Speed: 2 channels (Host/Function switchable)
- 10M/100M EtherMAC: 1channel
- SCIF: 5 channels
- I²C: 4 channels
- SSI: 4 channels
- RSPI: 3 channels
- Ethernet AVB: 1 channel
- CAN: 2 channels

Package

- 176-LFBGA (8mm × 8mm,0.5mm pitch)
- 176-LFQFP (24mm × 24mm, 0.5mm pitch)
- 208-LFQFP (28mm × 28mm,0.5mm pitch)

■ RZ/A1LU Group Block Diagram

Memory
SRAM 3MB
SRAML2 Cache 128 KB
Cache 32 KB + 32 KB
System
System DMAC 16ch
,
DMAC 16ch

Audio
SCUX 4ch ASRC

Analog

ADC 12-bit × 8ch 8-bit x 1ch
OS Timer
32-bit x 2ch
Real-Time CLK

Graphics

Video Display Controller
1ch
CMOS Camera I/F
1ch
JPEG Engine
1ch

CPU

Cortex®-A9 400MHz

Timers

MTU2 16-bit × 5ch

WDT

NEON

	Inter	faces	
П	10/100 Ether MAC		
	CA		
ı	USE HS 2ch H	32.0	
		Bus 32-bit SRAM,	
	SPI Multi		
	SCIF 5ch	RSPI 3ch	
	2 40	-	
	SSI (I ² S)	SPDIF 1ch	
	SDHI 2ch	MMC	
	Smart Card I/F		
	IrE)A	
	Ethernet AVB		



RZ/A1L, RZ/A1LC Group

CPU (Arm® Cortex®-A9)

- Operating frequency: 400MHz
- Single-precision/double-precision FPU
- Arm® NEON™

On-chip memory

- RZ/A1L: 3MB
- RZ/A1LC: 2MB

Main graphics and camera input functions

- LCD controller (VDC5): 1 channel LCD output: Max. WXGA Screen superimposition: 3 layers Video input: Max. XGA
- CMOS camera input (CEU): 1 channel

Main memory interface functions

NOR flash, SDRAM, NAND flash

- QSPI serial flash: 1 channel (ability to run stored programs directly)
- SD host interface: 2 channels
- MMC host interface: 1 channel

Main communication functions

- USB 2.0 High Speed: 2 channels (Host/Function switchable)
- 10M/100M EtherMAC: 1 channel
- SCIF: 5 channels
- I²C: 4 channels
- SSI: 4 channels
- RSPI: 3 channels
- CAN: 2 channels
- Package
- 176-LFBGA (8mm × 8mm,0.5mm pitch)
- 176-LFQFP (24mm × 24mm,0.5mm pitch)
- 208-LFQFP (28mm × 28mm,0.5mm pitch)
- 233-FBGA (15mm × 15mm, 0.8mm pitch)

■ RZ/A1L, RZ/A1LC Group Block Diagram

	Memory
Г	SRAM
١.	A1L: 3 MB/A1LC: 2 MB
	SRAM L2 Cache
١.	128 KB
Г	Cache
L	32 KB + 32 KB

System
DMAC 16ch
Interrupt Controller
Clock Generation with SSCG
JTAG Debug

Audio	
SCUX 4ch ASRC	
CDROM DEC*	

Analog
ADC
12-bit × 8ch

^{*} RZ/A1L Group specification only.

CPU				
Cortex®-A9 400MHz				
NEON	FPU			

Timers		
	MTU2	
	16-bit × 5ch	
	WDT	
	8-bit × 1ch	
	OS Timer	
	32-bit × 2ch	
	Real-Time CLK	

Graphics		
Video Display Controller		
1ch		
CMOS Camera I/F		
1ch		

Interfaces		
10/100 Ether MAC		
USB2.0		
HS 2ch Host/Func		
External Bus 32-bit		
ROM, SRAM,		
SDRAM, PCMCIA		
SPI Multi		
1ch		
SCIF	RSPI	
5ch	3ch	
I ² C	IEBus*	
4ch	1ch	
SSI (I ² S)	SPDIF	
4ch	1ch	
SDHI	MMC	
2ch	1ch	
CAN	MOST50*	
2ch	1ch	
Smart Card I/F		
2ch		
IrDA	LIN Master*	
1ch	1ch	

RZ/A Series: Development Environments (Integrated Development Environments)

	RENESAS	arm	iar
Development environments	• e² studio*1 e² studio e² studio	• Arm® DS	• IAR Embedded Workbench® for Arm®
Compilers	GNU Arm Embedded Toolchain	Arm Compiler	• IAR C/C++ compiler*3
ICEs	• J-Link LITE from Segger • J-Link series from Segger*2	DSTREAM™ ULINKpro™ ULINKproD™ ULINK2™	I-jet™/I-jet Trace™ for Arm® Cortex®-A/R/M JTAGjet-Trace
Supported products	RZ/A1 Group, RZ/A2M, RZ/A3UL	RZ/A2M	RZ/A1 Group, RZ/A2M

- *1: Eclipse-based development environment from Renesas (https://www.renesas.com/e2studio)
- *2: Renesas does not handle ICEs from Segger. Contact a sales agent for details.
- *3: A free evaluation license is available provided the 14-day time-limited evaluation or the code size-limited evaluation.

RZ/A Series: Development Tools (Debuggers, ICEs)

	Kyoto Microcomputer Co., Ltd.	SEGGER	LAUTERBACH DEVELOPMENT TOOLS
Debuggers	• PARTNER-Jet2	Ozone e² studio ozone ozone	• PowerView
ICEs		• J-Link Series	• PowerDebug
Supported compilers	exeGCC from Kyoto Microcomputer GNU Arm Embedded Toolchain Arm compiler IAR C/C++ compiler, etc.	GNU Arm Embedded Toolchain Arm compiler IAR C/C++ compiler, etc.	GNU Arm Embedded Toolchain Arm compiler IAR C/C++ compiler, etc.
Supported products	RZ/A1 Group, RZ/A2M, RZ/A3UL		

Code Generation Support: Flexible Software Package (FSP) + Smart Configurator (SC)

(Supported product: RZ/A3UL)

The FSP includes everything you'll need to start developing software: board-dependent programs, peripheral function drivers, middleware, and documentation on how to use them.

Smart Configurator is a utility based on the concept of "combining software components freely." The intuitive GUI makes it easy to configure pins and FSP driver settings and to generate source code customized for your use case. It works together with integrated development environments such as ${\rm e}^2$ studio.











RZ Family Ecosystem Partners

Renesas is enabling a comprehensive partner ecosystem to deliver an array of software and hardware building blocks that will work out-of-the-box with Renesas RZ Family MPUs. The Renesas RZ ecosystem will help accelerate the development of IoT applications, including core technologies such as security, safety, connectivity, and HMI among others.



Expansive Third Party Solutions Portfolio

- 200+ partners, 300+ solutions and growing
- Coverage across all key IoT technologies
- Robust GTM and strong digital drumbeat



Commercial Grade Building Block Solutions

- Commercial grade software
- Work out-of-box with Renesas products
- Bundling options for select solutions



Problem Solving at Heart

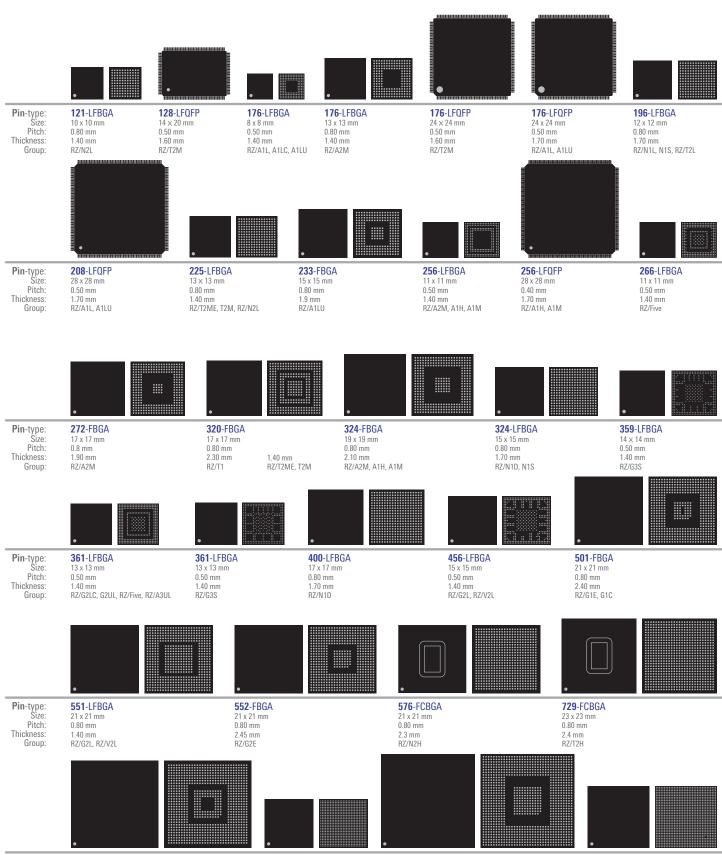
- Address specific design problems
- Address specific skill-set gaps
- Customer-centric approach

Partner Overview

The partner overview shown might not be complete since the partner network is extending almost daily. For best reference and latest data, we recommend checking our webpage at: RZ Partner Ecosystem Solutions



RZ Family Package Lineup



Pin-type: Size: Pitch: Thickness: Group:

27 x 27 mm 0.80 mm 2.40 mm RZ/G1H, G1M, G1N

831-FBGA

841-FCBGA 15 x 15 mm 0.50 mm

1.90 mm ± 0.2 mm RZ/V2M, V2MA

1022-FBGA 29 x 29 mm 0.80 mm 2.5 mm RZ/G2M, G2N

3.15 mm RZ/G2H

1368-HFBGA

19 x 19 mm 0.50 mm 2.65 mm RZ/V2H



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