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SH7080 Group

×16-Bit SDRAM Interface

Introduction

This application note describes how to connect and use an SDRAM (×16 bits). You can use this application note as reference information for designing user software.

Target Device

SH7085 (R5F7085)

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1. Connecting an SDRAM

Applicable Conditions:

- Microcomputer: SH7085 (R5F7085)
- Operating frequency: Internal clock 80 MHz
  Bus clock 40 MHz
  Peripheral clock 40 MHz
  MTU2 clock 40 MHz
  MTU2S clock 80 MHz
- C compiler: V.9.00.02 manufactured by Renesas Technology Corp.

The SH7080 Group MCU can directly connect an SDRAM satisfying the following conditions to area 2 (CS2 space) or area 3 (CS3 space):

- Row address: 11/12/13 bits
- Column address: 8/9/10 bits
- Number of banks: 4 or less banks
- The A10 pin of the SDRAM is used for setting the precharge mode.

Note: If you are using only one SDRAM chip, connect it to the CS3 space.

The operating modes supported by the SH7080 Group MCU are burst read/single write (burst length 1) and burst read/burst write (burst length 1).

In this sample task, a K4S641632H-TC75 (1 Mword × 16 bits × 4 banks; manufactured by Samsung Electronics Co., Ltd.) is connected to the CS3 space of the SH7085. Figure 1 shows connections between the SH7085 and the SDRAM.

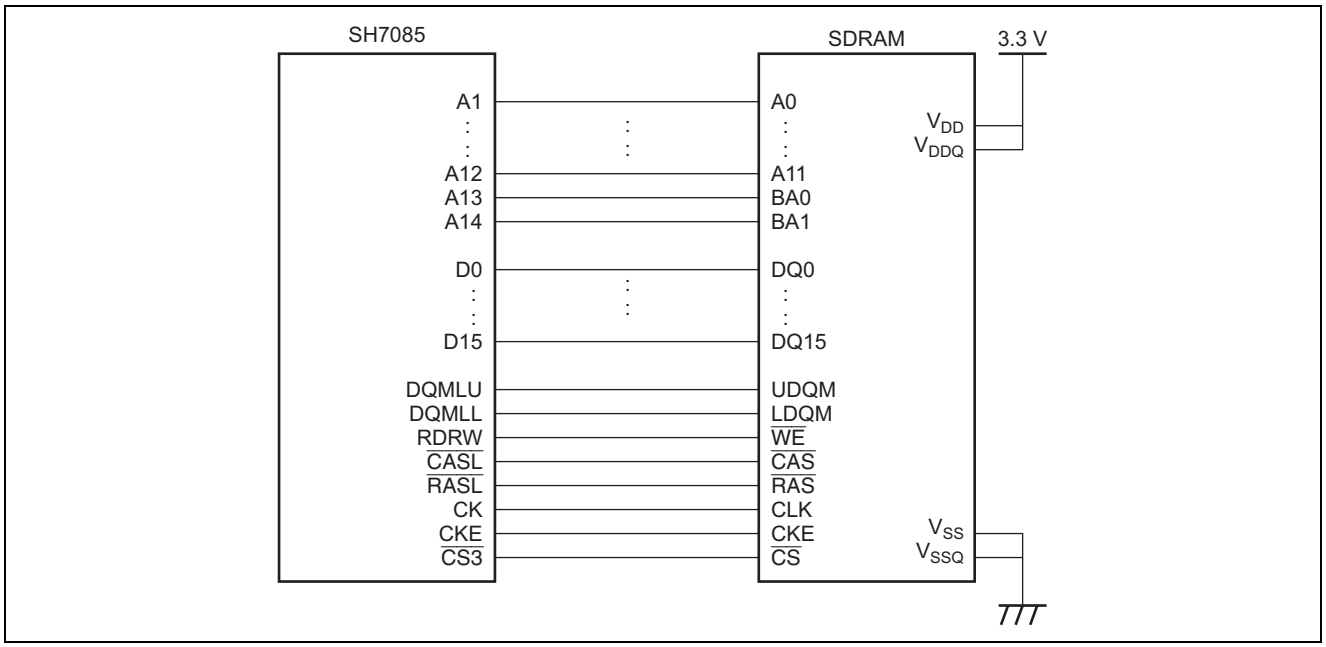


Figure 1 Connection Example of SDRAM

The SH7080 Group issues the following commands to the SDRAM.

- NOP: No operation
- Auto-refresh (REF): Request for refreshing the SDRAM
- Self-refresh (SELF): Execution of self-refreshing
- Precharge all banks (PALL): Precharging of all banks (transition to the idle state)
- Precharge specified bank (PRE): Precharging of the specified bank (transition to the idle state)
- Bank active (ACTV): Selection of the bank to be accessed
- Read (READ): Execution of read operation
- Read with precharge (READA): Issuing of the precharge command after a read operation
- Write (WRIT): Execution of a write operation
- Write with precharge (WRITA): Issuing of the precharge command after a write operation
- Write to the mode register (MRS): Setting of an SADRAM operating mode

2. Power-On Sequence

The following MCU internal modules must be set after power-on before the SDRAM can be used:

- Pin function controller (PFC)
- Bus state controller (BSC)
- SDRAM mode register

Setting of the individual registers assumes that the SDRAM is allocated in the CS3 space.

2.1 Setting the Pin Function Controller (PFC)

The PFC must be set so that the SDRAM pins can be used.

(1) Port A Control Register L2 (PACRL2)

This register selects the functions of multiplexed pins in port A (PA4 - PA7).
Setting value: H'2000

Bit	Bit Name	Setting Value	Function
15	—	0	Reserved
14-12	PA7MD[2:0]	010	010: $\overline{CS3}$ (Chip Select 3) output
11	—	0	Reserved
10-8	PA6MD[2:0]	000	000: PA6 input/output
7	—	0	Reserved
6-4	PA5MD[2:0]	000	000: PA5 input/output
3	—	0	Reserved
2-0	PA4MD[2:0]	000	000: PA4 input/output

(2) Port A Control Register L3 (PACRL3)

This register selects the functions of multiplexed pins in port A (PA8 - PA11).
Setting value: H'0055

Bit	Bit Name	Setting Value	Function
15	—	0	Reserved
14-12	PA11MD[2:0]	000	000: PA11 input/output
11	—	0	Reserved
10-8	PA10MD[2:0]	000	000: PA10 input/output
7	—	0	Reserved
6-4	PA9MD[2:0]	101	101: CKE (Clock Enable) output
3	—	0	Reserved
2-0	PA8MD[2:0]	101	101: RDWR (Read/Write) output

(3) Port A Control Register L4 (PACRL4)

This register selects the functions of multiplexed pins in port A (PA12 - PA15).
Setting value: H'1011

Bit	Bit Name	Setting Value	Function
15	—	0	Reserved
14-12	PA15MD[2:0]	001	001: CK (system clock) output
11	—	0	Reserved
10-8	PA14MD[2:0]	000	000: PA14 input/output
7	—	0	Reserved
6-4	PA13MD[2:0]	001	001: DQMLU (upper side selected) output
3	—	0	Reserved
2-0	PA12MD[2:0]	001	001: DQMLL (lower side selected) output

(4) Port B Control Register L2 (PBCRL2)

This register selects the functions of multiplexed pins in port B (PB4 - PB7).
Setting value: H'0044

Bit	Bit Name	Setting Value	Function
15	—	0	Reserved
14-12	PB7MD[2:0]	000	000: PB7 input/output
11	—	0	Reserved
10-8	PB6MD[2:0]	000	000: PB6 input/output
7	—	0	Reserved
6-4	PB5MD[2:0]	100	100: $\overline{\text{CASL}}$ (CAS) output
3	—	0	Reserved
2-0	PB4MD[2:0]	100	100: $\overline{\text{RASL}}$ (RAS) output

(5) Port C Control Register L1 (PCCRL1)

This register selects the functions of multiplexed pins in port C (PC0 - PC3).
Setting value: H'1111

Bit	Bit Name	Setting Value	Function
15-13	—	000	Reserved
12	PC3MD0	1	1: A3 output
11-9	—	000	Reserved
8	PC2MD0	1	1: A2 output
7-5	—	000	Reserved
4	PC1MD0	1	1: A1 output
3-1	—	000	Reserved
0	PC0MD0	1	1: A0 output (not connected)

(6) Port C Control Register L2 (PCCRL2)

This register selects the functions of multiplexed pins in port C (PC4 - PC7).
Setting value: H'1111

Bit	Bit Name	Setting Value	Function
15-13	—	000	Reserved
12	PC7MD0	1	1: A7 output
11-9	—	000	Reserved
8	PC6MD0	1	1: A6 output
7-5	—	000	Reserved
4	PC5MD0	1	1: A5 output
3-1	—	000	Reserved
0	PC4MD0	1	1: A4 output

(7) Port C Control Register L3 (PCCRL3)

This register selects the functions of multiplexed pins in port C (PC8 - PC11).
Setting value: H'1111

Bit	Bit Name	Setting Value	Function
15-13	—	000	Reserved
12	PC11MD0	1	1: A11 output
11-9	—	000	Reserved
8	PC10MD0	1	1: A10 output
7-5	—	000	Reserved
4	PC9MD0	1	1: A9 output
3-1	—	000	Reserved
0	PC8MD0	1	1: A8 output

(8) Port C Control Register L4 (PCCRL4)

This register selects the functions of multiplexed pins in port C (PC12 - PC15).
Setting value: H'1111

Bit	Bit Name	Setting Value	Function
15-13	—	000	Reserved
12	PC15MD0	1	1: A15 output
11-9	—	000	Reserved
8	PC14MD0	1	1: A14 output
7-5	—	000	Reserved
4	PC13MD0	1	1: A13 output
3-1	—	000	Reserved
0	PC12MD0	1	1: A12 output

(9) Port D Control Register L1 (PDCRL1)

This register selects the functions of multiplexed pins in port D (PD0 - PD3).
Setting value: H'1111

Bit	Bit Name	Setting Value	Function
15	—	0	Reserved
14-12	PD3MD[2:0]	001	001: D3 input/output
11	—	0	Reserved
10-8	PD2MD[2:0]	001	001: D2 input/output
7	—	0	Reserved
6-4	PD1MD[2:0]	001	001: D1 input/output
3	—	0	Reserved
2-0	PD0MD[2:0]	001	001: D0 input/output

(10) Port D Control Register L2 (PDCRL2)

This register selects the functions of multiplexed pins in port D (PD4 - PD7).
Setting value: H'1111

Bit	Bit Name	Setting Value	Function
15	—	0	Reserved
14-12	PD7MD[2:0]	001	001: D7 input/output
11	—	0	Reserved
10-8	PD6MD[2:0]	001	001: D6 input/output
7	—	0	Reserved
6-4	PD5MD[2:0]	001	001: D5 input/output
3	—	00	Reserved
2-0	PD4MD[2:0]	001	001: D4 input/output

(11) Port D Control Register L3 (PDCRL3)

This register selects the functions of multiplexed pins in port D (PD8 - PD11).
Setting value: H'1111

Bit	Bit Name	Setting Value	Function
15-14	—	00	Reserved
13-12	PD11MD[1:0]	01	001: D11 input/output
11	—	0	Reserved
10-8	PD10MD[2:0]	001	001: D10 input/output
7	—	0	Reserved
6-4	PD9MD[2:0]	001	001: D9 input/output
3	—	0	Reserved
2-0	PD8MD[2:0]	001	001: D8 input/output

(12) Port D Control Register L4 (PDCRL4)

This register selects the functions of multiplexed pins in port D (PD12 - PD15).
Setting value: H'1111

Bit	Bit Name	Setting Value	Function
15-14	—	00	Reserved
13-12	PD15MD[1:0]	01	01: D15 input/output
11-10	—	00	Reserved
9-8	PD14MD[1:0]	01	01: D14 input/output
7-6	—	00	Reserved
5-4	PD13MD[1:0]	01	01: D13 input/output
3-2	—	00	Reserved
1-0	PD12MD[1:0]	01	01: D12 input/output

2.2 Setting the Bus State Controller (BSC)

(1) CS3 Space Bus Control Register (CS3BCR)

This register selects the type of memory to be connected to the CS3 space, the data bus width, and the number of wait cycles.

Setting value: H'36DB4400

Bit	Bit Name	Setting Value	Function
31-30	—	00	Reserved
29-28	IWW[1:0]	11	11: Inserts 4 idle cycles between write-read or write-write cycles.
27	—	0	Reserved
26-25	IWRWD[1:0]	11	11: Inserts 4 idle cycles between read-write cycles in a different space.
24	—	0	Reserved
23-22	IWRWS[1:0]	11	11: Inserts 4 idle cycles between read-write cycles in the same space.
21	—	0	Reserved
20-19	IWRRD[1:0]	11	11: Inserts 4 idle cycles between read-read cycles in a different space.
18	—	0	Reserved
17-16	IWRRS[1:0]	11	11: Inserts 4 idle cycles between read-read cycles in the same space.
15	—	0	Reserved
14-12	TYPE[2:0]	100	100: Connects the SDRAM.
11	—	0	Reserved
10-9	BSZ[1:0]	10	10: 16-bit data bus width
8-0	—	0-0	Reserved

(2) CS3 Space Wait Control Register (CS3WCR)

This register selects varying number of wait cycles related to memory located in the CS3 space.

Setting value: H'00000480

Bit	Bit Name	Setting Value	Function
31-15	—	0-0	Reserved
14-13	TRP[1:0]	00	00: Inserts 1 idle cycle between issuing of the auto-precharge or PRE command and issuing of the ACTV command to the same bank.
12	—	0	Reserved
11-10	TRCD[1:0]	01	01: Inserts 2 idle cycles between issuing of the ACTV command and issuing of the READ(A) or WRIT(A) command.
9	—	0	Reserved
8-7	A3CL[1:0]	01	01: Sets the CAS latency to 2 cycles.
6-5	—	00	Reserved
4-3	TRWL[1:0]	00	00: No idle cycles are inserted between issuing of the WRITA or WRIT command and issuing of the auto-precharge or PRE command.
2	—	0	Reserved
1-0	TRC[1:0]	00	00: Inserts 3 idle cycles between cancellation of the REF command or self-refresh command and issuing of the ACTV command.

(3) Refresh Time Constant Register (RTCOR)

This register issues a refresh request when the values of RTCNT and RTCOR match.

Setting value: H'A55A009C

Bit	Bit Name	Setting Value	Function
31-8	—	0-0	Reserved
7-0		1001 1100	H'9C: Sets the refresh interval to 15.6 µs.

Note: When writing data to this register, make the upper two bytes H'A55A. If this is not done, written data will be protected.

(4) Refresh Timer Counter (RTCNT)

This register counts up until the value of RTCNT matches the value of RTCOR. The clock selected by the RTCSR register is used for counting up.

Setting value: H'A55A0000

Bit	Bit Name	Setting Value	Function
31-8	—	0-0	Reserved
7-0		0000 0000	H'00: Clears the counter.

Note: When writing data to this register, set the upper two bytes to H'A55A. Otherwise, write protection will not be cleared.

(5) SDRAM Control Register (SDCR)

This register selects how to refresh and access the SDRAM, and the type of the SDRAM.

Setting value: H'00000808

Bit	Bit Name	Setting Value	Function
31-21	—	0-0	Reserved
20-19	A2ROW[1:0]	00	00: Sets the row address of area 2 to 11 bits.
18	—	0	Reserved
17-16	A2COL[1:0]	00	00: Sets the column address of area 2 to 8 bits.
15-12	—	0000	Reserved
11	RFSH	1	1: Refreshes the SDRAM.
10	RMODE	0	0: Auto-refreshing is performed.
9	—	0	Reserved
8	BACTV	0	0: Accesses the SDRAM in the auto-precharge mode.
7-5	—	000	Reserved
4-3	A3ROW[1:0]	01	01: Sets the row address of area 3 to 12 bits
2	—	0	Reserved
1-0	A3COL[1:0]	00	00: Sets the column address of area 3 to 8 bits

(6) Refresh Timer Control/Status Register (RTCSR)

This register selects various items related to refreshing of the SDRAM.

Setting value: H'A55A0008

Bit	Bit Name	Setting Value	Function
31-8	—	0-0	Reserved
7	CMF	0	Compare match flag
6	CMIE	0	0: Disables interrupt requests by the CMF bit.
5-3	CKS[2:0]	001	001: Counts up RTCNT with a Bϕ/4 clock.
2-0	RRC[2:0]	000	000: Refreshes the SDRAM one time when the values of RTCNT and RTCOR match.

Note: To write data to this register, set the upper two bytes to H'A55A. Otherwise, write protection will not be cleared.

2.3 Setting the SDRAM Mode Register

The SDRAM mode register is set by inputting a specific address signal to the SDRAM. The SDRAM mode register sets the CAS latency, burst length, and similar items.

The SH7080 Group MCU supports burst read/single write, burst read/burst write, burst length 1, wrap type (burst type) - sequential, and CAS latency 2 or 3.

If the value to be set for the mode address is X, writing to the SDRAM mode register allocated in area 3 would be accomplished with a word-write to the <X + H'FFF85000> address. If the register is allocated in area 2, the data would be written to the <X + H'FFF84000> address. Table 1 is a list of access addresses and the corresponding SDRAM operating modes available when the SDRAM mode register is set.

Table 1 Access Addresses and Operating Modes When the SDRAM Mode Register Is Set

(1) Area 2 setting

- Burst read/single write (burst length 1)

Data Bus Width	CAS Latency	Access Address
16	2	H'FFF84440
	3	H'FFF84460
32	2	H'FFF84880
	3	H'FFF848C0

- Burst read/burst write (burst length 1)

Data Bus Width	CAS Latency	Access Address
16	2	H'FFF84040
	3	H'FFF84060
32	2	H'FFF84080
	3	H'FFF840C0

(2) Area 3 setting

- Burst read/single write (burst length 1)

Data Bus Width	CAS Latency	Access Address
16	2	H'FFF85440*
	3	H'FFF85460
32	2	H'FFF85880
	3	H'FFF858C0

*These are the settings in this sample task.

- Burst read/burst write (burst length 1)

Data Bus Width	CAS Latency	Access Address
16	2	H'FFF85040
	3	H'FFF85060
32	2	H'FFF85080
	3	H'FFF850C0

When the SDRAM mode register is set (that is, a word-write to the addresses described above is performed), a low level (0) is output to bit A12 and above of the address bus. In a 16-bit connection, the A0 pin is not used because a word address is specified. (In a 32-bit connection, the A0 and A1 pins are not used). Accordingly, the value X to be set in the mode register is a value shifted to the left 1 bit from the value set in the SDRAM mode register.

Example: Value in the SDRAM mode register → Value of X
H'0020 → H'0040
H'0030 → H'0060

Table 2 is a list of SH7085 address pins used when the SDRAM mode register is set, the SDRAM address pins, and the function of the settings.

Table 2 Address Pins and SDRAM Mode Register Settings

SH7085 Address Pins	SDRAM Address Pins	Function
A1-A3	A0-A2	Burst length
A4	A3	Wrap type (burst type)
A5-A7	A4-A6	CAS latency
A8-A11	A7-A10	Operating mode
A12 and above	A11 and above	Reserved

The SH7080 Group MCU issues the following commands in the order given to set the SDRAM mode register (word-write to the address indicated in table 1).

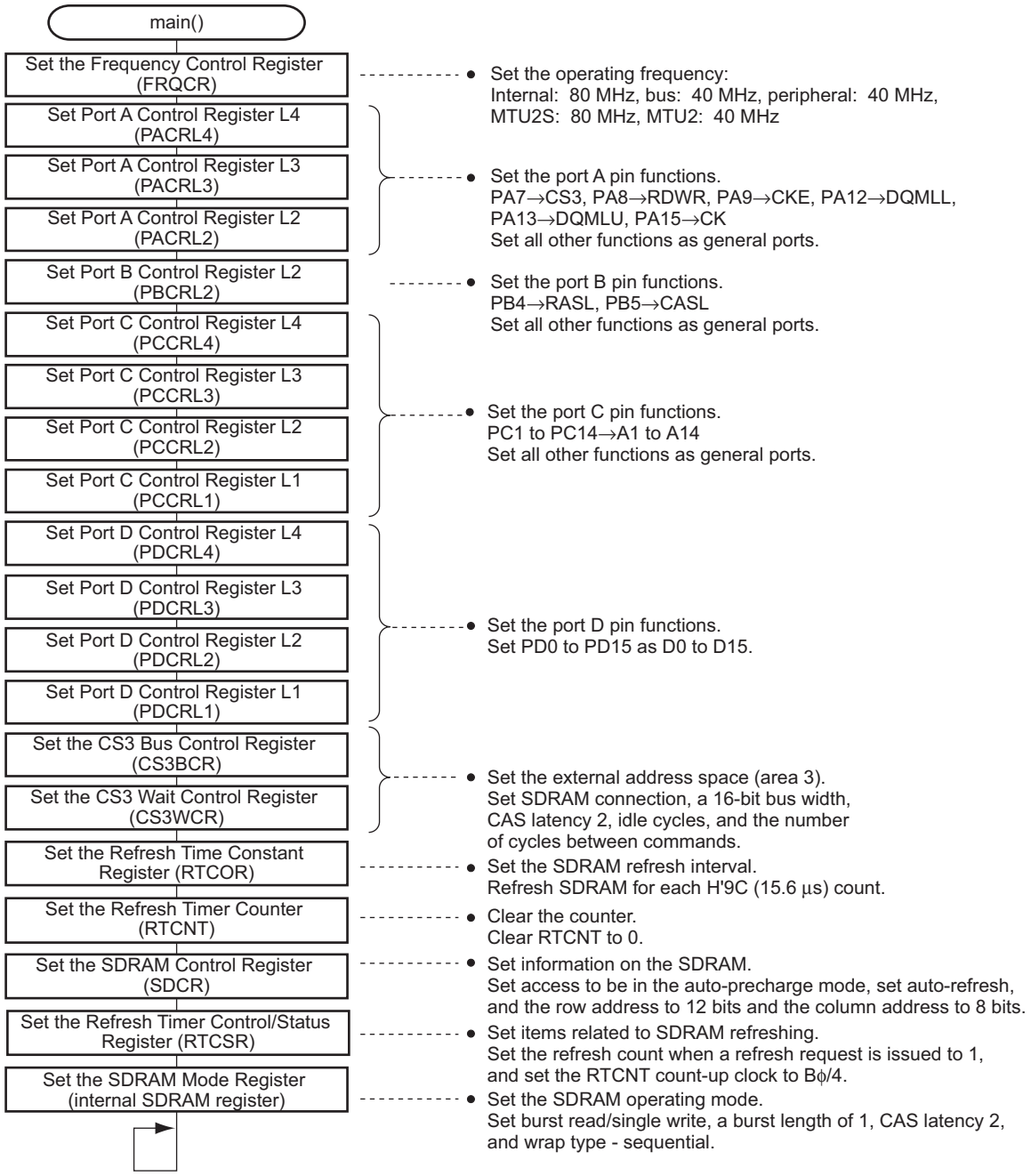
- Precharge all banks command
- Auto-refresh command (8 times)
- Write to the mode register command

When the mode register has been set, the SDRAM is usable.

The SDRAM requires a certain amount of idle time between power-on and execution of the precharge all banks command. For information on the required idle time, see the manual for the SDRAM you are using.

3. Flowchart

3.1 Main Routine



Note: RTCNT starts counting when the CKS bit of RTCSR is set. Accordingly, be sure to set RTCSR after all other settings are complete.

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Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Sep.14.05	—	First edition issued

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