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M16C/64 Group

Using the Voltage-Down Detection Interrupt to Enter Wait Mode

1. Abstract

This document describes an application example for the voltage-down detection interrupt of the microcomputer.
The sample program shows how to use the voltage-down detection interrupt to enter wait mode when the VCC1 input voltage drops below Vdet2, and to return from wait mode when the voltage rises above Vdet2.

2. Introduction

The application example presented in this document applies to the microcomputers listed below.

- Microcomputers: M16C/64 group
- Power supply voltage: 5.0 V (when voltage stabilized)

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Description of the Application Example

3.1 System Configuration

The application example presented here consists of the following system.

- Main clock: 6 MHz
- CPU clock source: PLL clock (XIN multiplied by 4 [24 MHz])
- Power control: Normal operating mode and wait mode used
- Peripheral function clock operation during wait mode: Turned off (CM02 bit = 1)
- Voltage-down detection interrupt: Enabled (VCR2 register VC27 bit = 1 (voltage-down detection circuit enabled)
  (D4INT register D40 bit = 1 (interrupt enabled)
- Hardware reset 2: Enabled (VCR2 register VC25 bit = 1 (voltage detection 0 circuit enabled)
  (VW0C register VW0C0 bit = 1 (reset enabled)
- Cold start/warm start determination function used
  - When cold started: Internal RAM is cleared to 0.
  - When warm started: Internal RAM is not cleared to 0. (The values stored in memory immediately before reset are retained.)
- Port P0: Time-of-day counter output during normal operation
  - Counts up every 1 sec.
- Port P1_0: VCC1 input voltage up/down determination output (When voltage is down: It outputs a logic 1.)
- Timer A0 timer mode: 50-ms cycle timer produced
  - Purpose of use: 1-sec timer (It counts down each time a timer interrupt is generated.)
  - Count source: f32TIMAB (PLL clock (24 MHz) divided by 32)
  - Timer A0 set value: 37,499 (50 ms × 24 MHz/f32TIMAB – 1)

3.2 Description of the Peripheral Function

The peripheral function used in the application example here is as follows:

(1) Voltage-down detection interrupt

The voltage-down detection interrupt is an interrupt enabled by setting the VC27 bit to 1 (voltage-down detection circuit enabled) and the D40 bit to 1 (voltage-down detection interrupt enabled).

- When the input voltage on VCC1 pin is detected to have risen or dropped past Vdet2, the D42 bit (voltage change detection flag) changes from 0 to 1, generating a voltage-down detection interrupt request. The D42 bit should be cleared to 0 by a program.
- The cause of voltage-down detection interrupt (VCC1 < Vdet2 or VCC1 ≥ Vdet2) can be determined by the VC13 bit (voltage-down monitor flag). (This interrupt request is not generated until the sampling time elapses after the value of the VC13 bit has changed.) Table 1 shows the sampling time. Figure 1 shows the manner of how a voltage-down detection interrupt request is generated.
- The interrupt vector for the voltage-down detection interrupt is shared with the watchdog timer interrupt and oscillation stop/reoscillation detected interrupt vectors.

Table 1. Sampling Time

CPU clock (MHz)	Sampling time (µs)			
	DF1–DF0 = 00b (CPU clock divided by 8)	DF1–DF0 = 01b (CPU clock divided by 16)	DF1–DF0 = 10b (CPU clock divided by 32)	DF1–DF0 = 11b (CPU clock divided by 64)
16	3.0	6.0	12.0	24.0
24	2.0	4.0	8.0	16.0

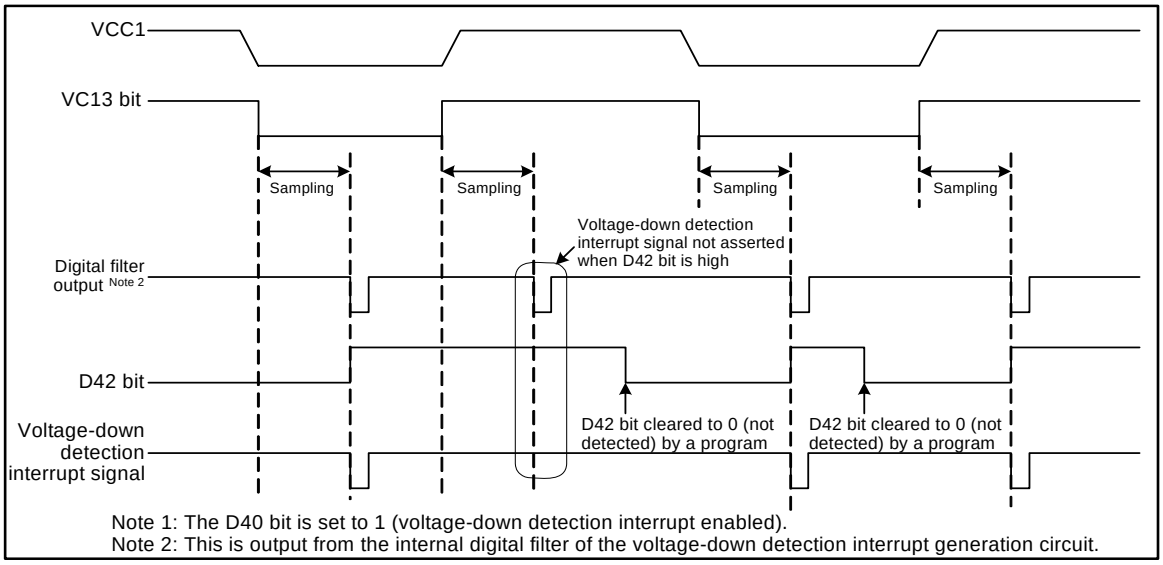


Figure 1. Typical Operation of the Voltage-Down Detection Interrupt Generation Circuit

Note: In the sample program, the CM02 bit is set to 1 (peripheral function clock, f1, turned off when in wait mode). Therefore, if the WAIT instruction is executed while VCC1 ≥ Vdet2, because wait mode constraint applies, a voltage-down detection interrupt is generated immediately and control returns from wait mode.

[Wait mode constraint]

If the WAIT instruction is executed while all of the following five conditions are met, a voltage-down detection interrupt is generated immediately and control returns from wait mode.

- The CM0 register's CM02 bit = 1 (peripheral function clock turned off)
- VCR2 register's VC27 bit = 1 (voltage-down detection circuit enabled)
- D4INT register's D40 bit = 1 (voltage-down detection interrupt enabled)
- D4INT register's D41 bit = 1 (voltage-down detection interrupt used for return from wait mode)
- VCC1 input voltage greater than Vdet2 (VCR1 register's VC13 bit = 1)

(2) Hardware reset 2

Hardware reset 2 is a reset asserted by the microcomputer's internal voltage detection 0 circuit. This circuit monitors the input voltage on VCC1 pin and when the input voltage drops below Vdet0, it resets the microcomputer.

Hardware reset 2 is enabled by setting the VCR2 register's VC25 bit to 1 (voltage detection 0 circuit enabled) and the VW0C register's VW0C0 bit to 1 (hardware reset 2 enabled).

Table 2 shows the procedure for setting the register bits associated with hardware reset 2. Figure 2 shows the manner of how hardware reset 2 works. The sample program does not use the digital filter.

Table 2. Hardware Reset 2 Related Bit Setup Procedure

Step	When digital filter is used	When digital filter is not used
1	Set the VCR2 register's VC25 bit to 1 (voltage detection 0 circuit enabled).	
2	Wait a while equal to td(E-A)	
3	Use the VW0C register's VW0F0–VW0F1 bits to select the sampling clock of the digital filter. Also, set the VW0C1 bit to 0 (digital filter enabled) and bits 6 and 7 to 1.	Set the VW0C register's VW0C1 bit to 1 (digital filter disabled) and bits 6 and 7 to 1.
4	Set the VW0C register bit 2 to 0. (After step 3, set bit 2 to 0 over again.)	
5	Set the CM1 register's CM14 bit to 0 (125 kHz on-chip oscillator oscillating).	—
6	Wait a while equal to the digital filter sampling clock × 4 cycles.	— (No wait time)
7	Set the VW0C register's VW0C0 bit to 1 (hardware reset 2 enabled).	

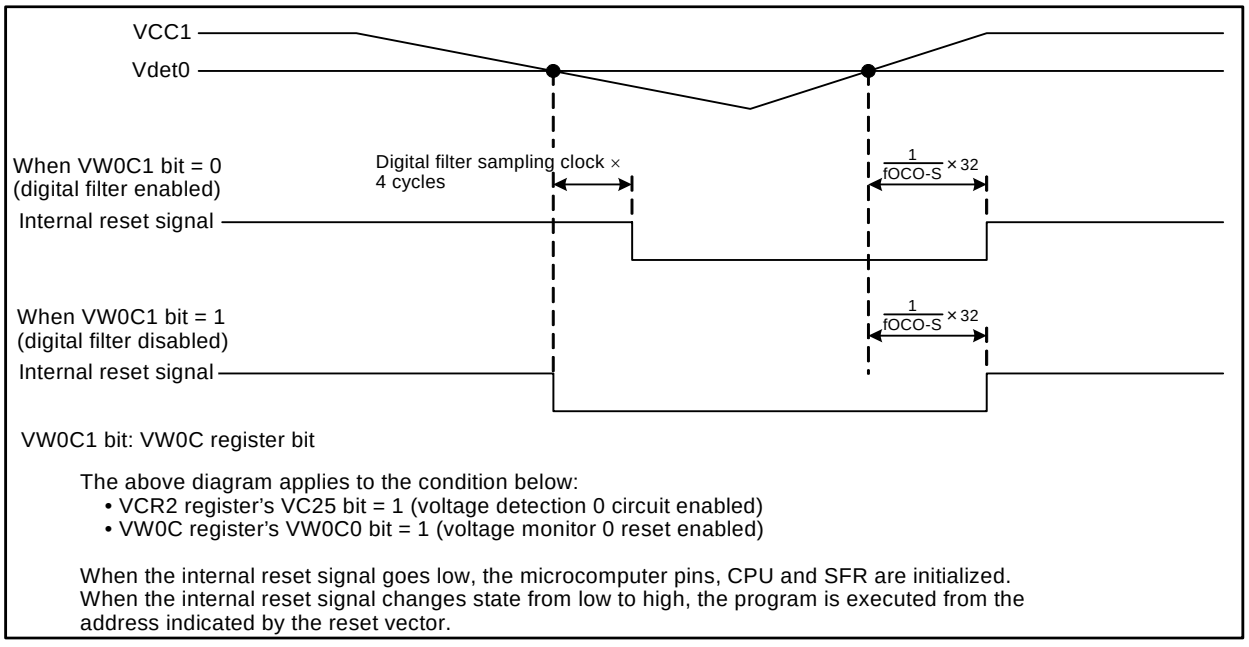


Figure 2. Hardware Reset 2 Operation Example

(3) Cold start/warm start determination function

- Cold start: When powered on, hardware reset 2
- Warm start: Hardware reset 1, software reset, watchdog timer reset, or oscillation stop detection reset

- Cold start/warm start determination is made by checking the RSTFR register's CWR bit (cold start/warm start determination flag). To enable the CWR bit, set the VCR2 register's VC25 bit to 1 (voltage detection 0 circuit enabled) and the VW0C register's VW0C0 bit to 1 (hardware reset 2 enabled).
- The CWR bit is cleared to 0 (cold start) when the device is powered on or hardware reset 2 is asserted. The CWR bit is set to 1 by writing 1 in a program. The value of this bit is unaffected by hardware reset 1, software reset, watchdog timer reset, and oscillation stop detection reset.
- When warm started, the value of the internal RAM is retained. However, if the RESET pin goes low while a write to the internal RAM is in progress, the value of the RAM being written becomes indeterminate.

Figure 3 shows the manner of how the cold start/warm start determination function works.

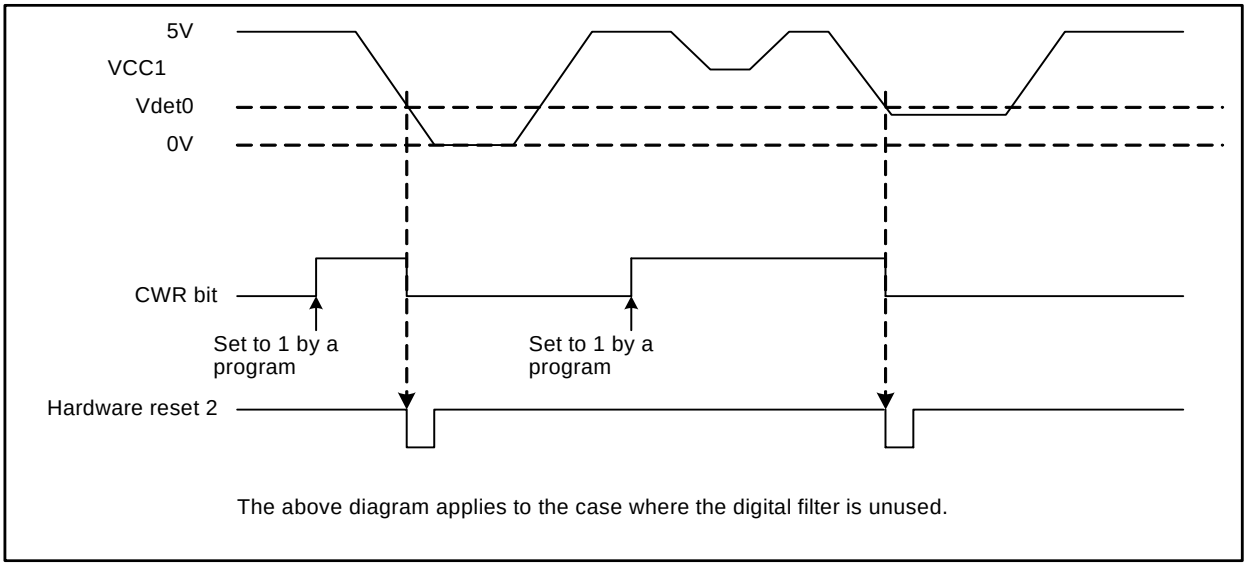


Figure 3. Operation Example of the Cold Start/Warm Start Determination Function

3.3 Description of Software Operation

(1) During normal operation
1-1) Count down the 1-sec timer each time a timer A0 interrupt request is generated (at 50-ms intervals).
1-2) Count up WATCH_CNT when the 1-sec timer underflows and output the count to port P0.

(2) When VCC1 < Vdet2 (when the VCC1 input voltage dropped)
2-1) Set the D42 bit to 1 (dropping past Vdet2 detected) at the same time a voltage-down detection interrupt is generated.
2-2) In a voltage-down detection interrupt handler, check the VC13 bit (voltage-down monitor flag) to determine whether VCC1 < Vdet2.
2-3) When the VCC1 < Vdet2 condition is confirmed, switch the CPU clock source from the PLL clock to the main clock.
2-4) Turn the PLL off to reduce the amount of power consumed in the chip.
2-5) Execute the WAIT instruction to enter wait mode.

(3) When VCC1 < Vdet0 (when the VCC1 input voltage dropped)
3-1) The internal reset signal is pulled low by action of hardware reset 2, causing the microcomputer pins, CPU and SFR to be initialized.

(4) When VCC1 ≥ Vdet0 (when the VCC1 input voltage rose)
4-1) The internal reset signal is released high by action of hardware reset 2, causing the device to enter a reset sequence.

(5) When VCC1 < Vdet2 (when the VCC1 input voltage dropped)
Perform the same operation as in (2).

(6) When VCC1 ≥ Vdet2 (when the VCC1 input voltage rose)
6-1) A voltage-down detection interrupt is generated. After returning from wait mode, execute the voltage-down detection interrupt handler again (multiple interrupts).
6-2) In a voltage-down detection process within the voltage-down detection interrupt handler, check the VC13 bit (voltage-down monitor flag) to determine whether VCC1 ≥ Vdet2.
6-3) When the VCC1 ≥ Vdet2 condition is confirmed, switch the CPU clock source from the main clock to the PLL clock.

Figure 4 shows VCC1 voltage changes and sample program state transitions.

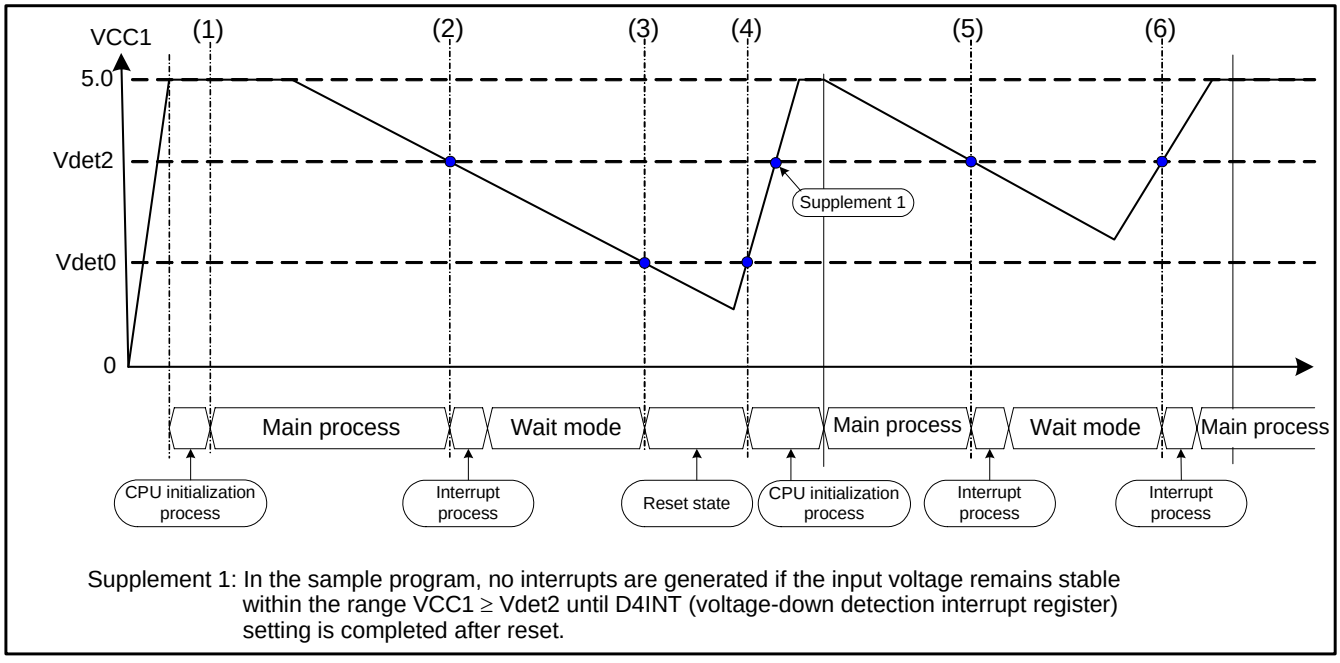


Figure 4. VCC1 Voltage Changes and Sample Program State Transitions

3.4 Description of the Voltage-Down Detection Interrupt Handling

The content and processing flow of voltage-down detection interrupt handling is described below.
The rise/fall of VCC1 input voltage is determined by reading the VC13 bit (voltage-down monitor flag) several times. The method for determining whether the VC13 bit is set or reset is described in Section 3.4.1, "VC13 Bit (Voltage-Down Monitor Flag) Check Example."

(1) If VCC1 < Vdet2 (when the VCC1 input voltage drops → Wait mode is entered)
  (1) Switch the CPU clock source from the PLL clock to the main clock.
    In the sample program, since the PLL clock is selected for the CPU clock source, the CPU clock source must be switched to the main clock before wait mode is entered.
  (2) Turn the PLL off to reduce the amount of power consumed in the chip.
  (3) Set the output counter port for input.
  (4) Set the D42 bit to 0 (Vdet2 undetected).
  (5) Execute the WAIT instruction to enter wait mode.
    In the sample program, the option "peripheral function clock, f1, turned off when in wait mode" (CM02 bit = 1) is selected to reduce the amount of power consumed in the chip.

(2) If VCC1 ≥ Vdet2 (when the VCC1 input voltage rises → Wait mode is exited)
  Return from wait mode when a voltage-down detection interrupt is generated during wait mode, and then enter voltage-down detection interrupt handling. In this case, there are multiple occurrences of voltage-down detection interrupts, i.e., another interrupt while an interrupt being processed.

(3) If VCC1 ≥ Vdet2 (multiple occurrences of voltage-down detection interrupts)
  (1) Switch the CPU clock source from the main clock to the PLL clock.
    Because the PLL was turned off before entering wait mode, it is turned back on.
  (2) Set the output counter port for output. (The counter data that was latched immediately before entering wait mode is output.)
  (3) Set the D41 to 0 temporarily and then set it to 1 (voltage-down detection interrupts used to return from stop mode).
  (4) Set the D42 bit to 0 (Vdet2 undetected).
    The D42 bit is set to 1 when the VCC1 input voltage is detected to have risen or dropped past Vdet2. When the D42 bit = 1, no voltage-down detection interrupt signals are output, so the D42 bit must be set to 0.

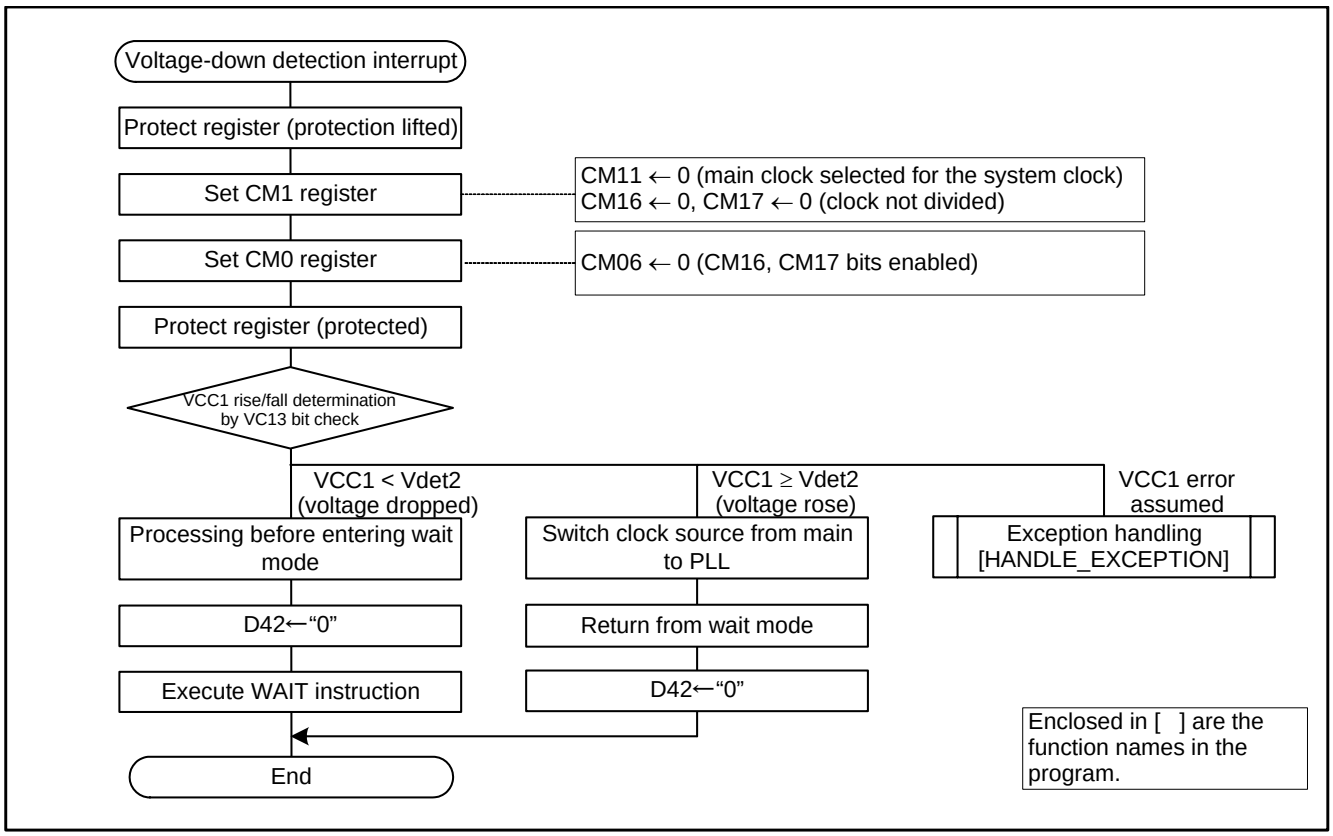


Figure 5. Voltage-Down Detection Interrupt Processing Flowchart

3.4.1 VC13 Bit (Voltage-Down Monitor Flag) Check Example

(1) The VC13 bit (voltage-down monitor flag) is checked in a fixed cycle. (The fixed cycle is produced by a loop process.)
(2) If the VC13 bit is sampled as 0 CNT_UNDER_VDET2 times (8 times) consecutively, a determination of VCC1 < Vdet2 is made.
(3) If the VC13 bit is sampled as 1 CNT_UNDER_VDET2 times (8 times) consecutively, a determination of VCC1 ≥ Vdet2 is made.
(4) If the number of times the VC13 bit is checked exceeds CNT_LOOP_MAX times (20 times), occurrence of an exception is assumed.

Figure 6 shows a VC13 bit (voltage-down monitor flag) check flowchart.

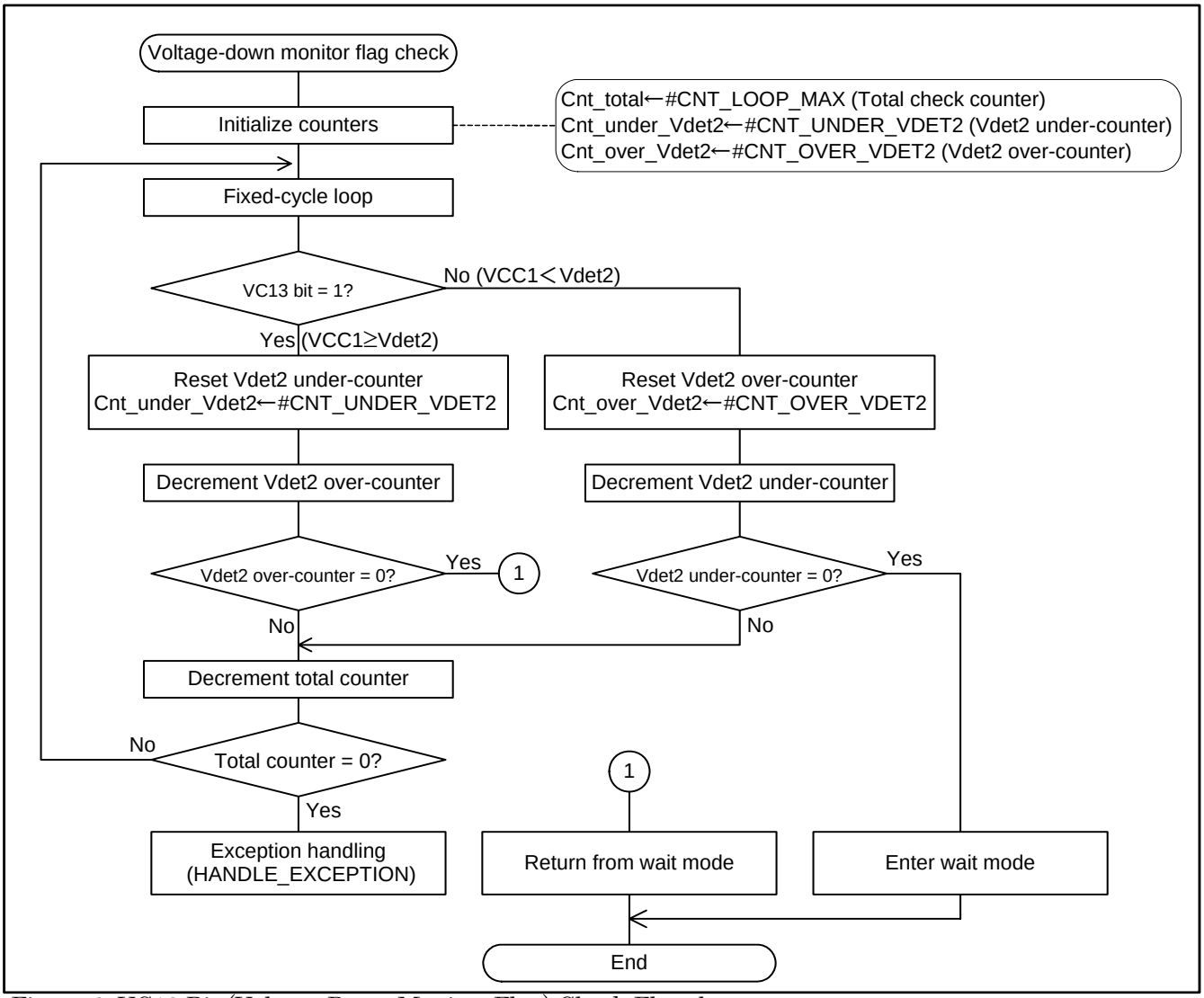


Figure 6. VC13 Bit (Voltage-Down Monitor Flag) Check Flowchart

3.4.2 Exception Handling (HANDLE_EXCEPTION)

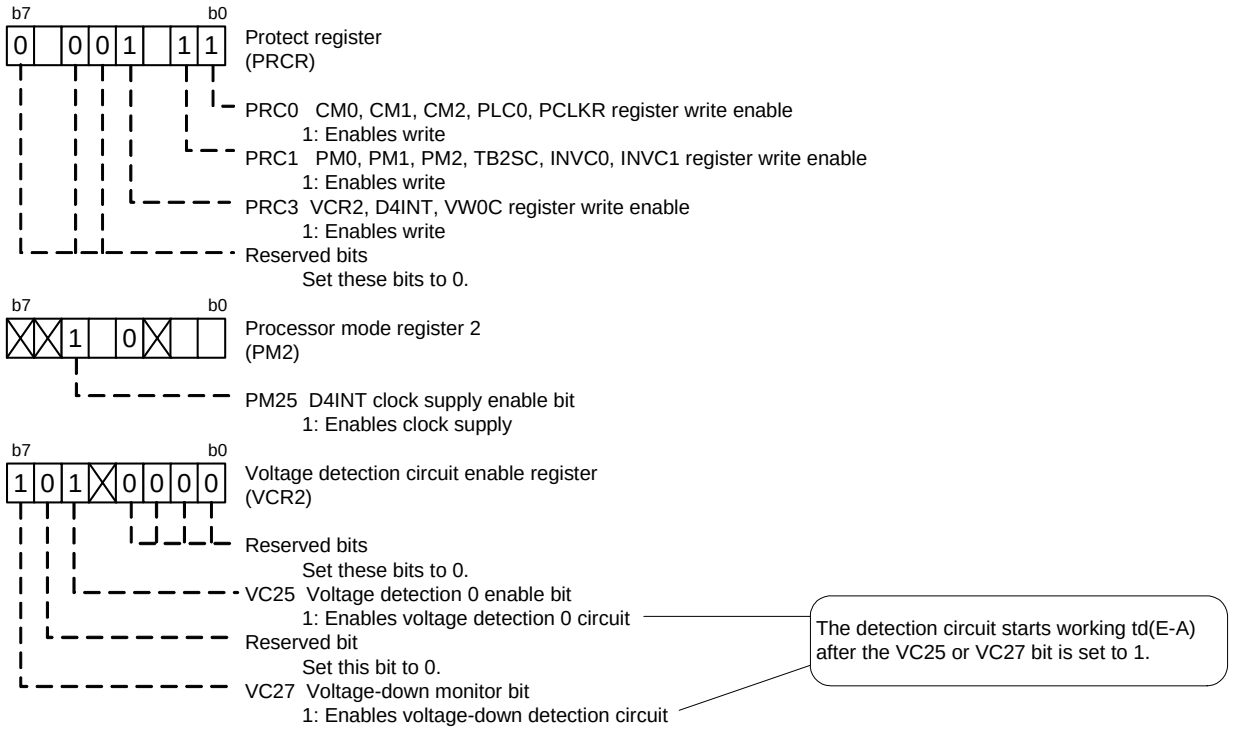
In the sample program, unless the VC13 bit (voltage-down monitor flag) is sampled 0 or 1 a number of times consecutively within a total check count (CNT_LOOP_MAX (20 times)), an exception condition is assumed.
In exception handling, the voltage-down detection interrupt is disabled before wait mode is entered and then the program is halted thereafter.

- Since the voltage-down detection interrupt is disabled before wait mode is entered, control does not return from wait mode even when the VCC1 input voltage rises to VCC1 ≥ Vdet2 after an exception occurs.
- A logic 1 is set in the output latch of port P1_0 as information that an exception has occurred.

4. How to Set Up

The following shows how to set up the registers to accomplish the operation described in Section 3.3, "Description of Software Operation." For details about each register, see the hardware manual of the M16C/64 group.

(1) Set the D4INT clock supply enable bit (PM25) and the voltage detection circuit enable register (VCR2).



(2) Wait until the voltage-down detection interrupt enable bit (D40) is set.

Here, a wait for sampling time is inserted to allow for the voltage-down detection interrupt enable bit to be set.
The time in which the voltage-down signal is sampled depends on how the DF1 and DF0 bits (sampling clock setting bits) are set. The maximum sampling time that can be set is (DF1, DF0 bits = 11 (CPU clock divided by 64)).

● Wait time = CPU clock × 1/64 × 6 clock cycles (see the table shown to the right)

CPU clock	Wait time
16MHz	24 μs
24MHz	16 μs
125 kHz on-chip oscillator divided by 8	25ms

Figure 7. Procedure for Setting Up the Registers to Use a Voltage-Down Interrupt Application (1)

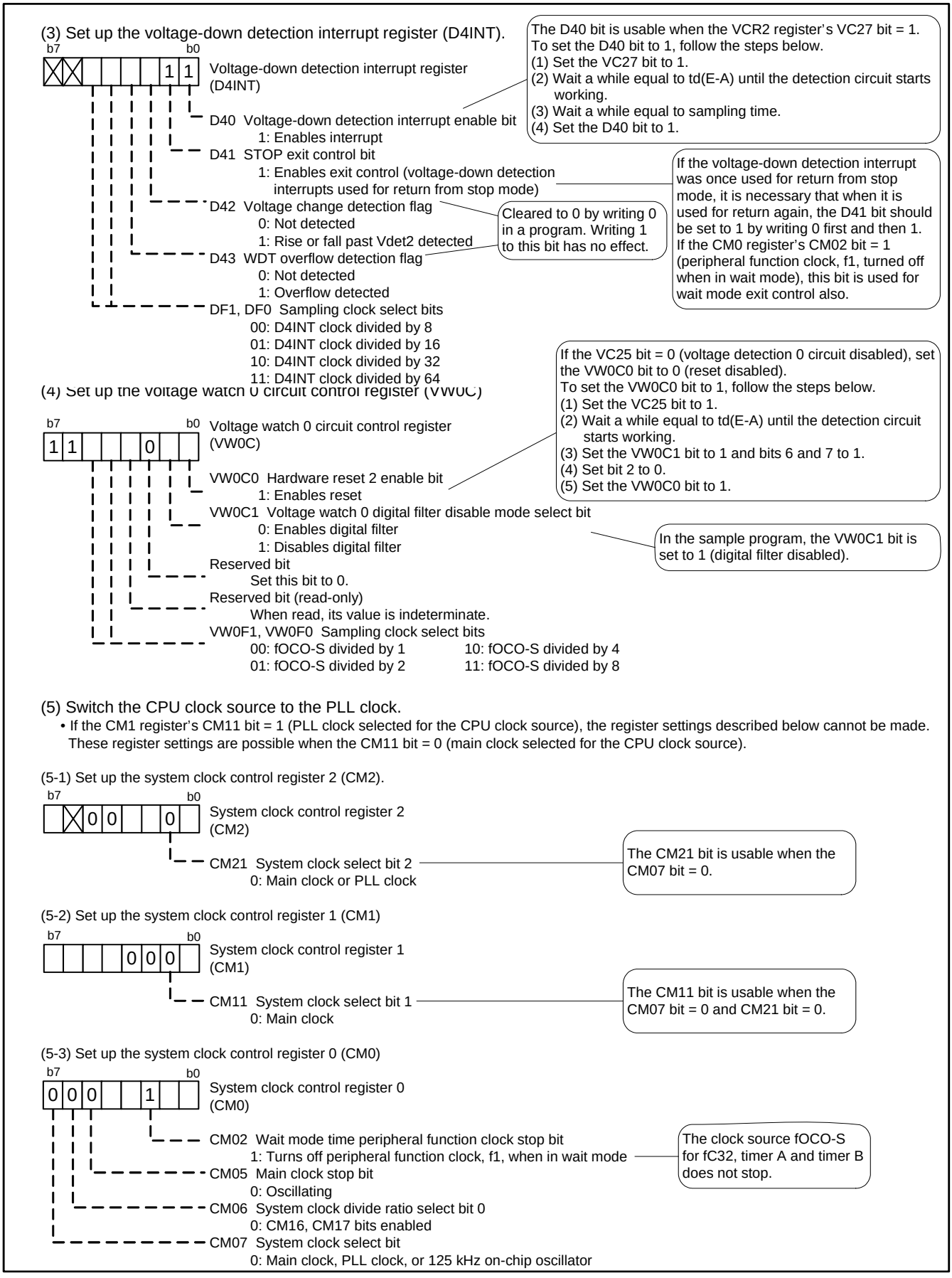
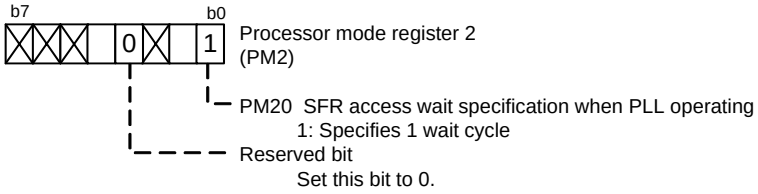
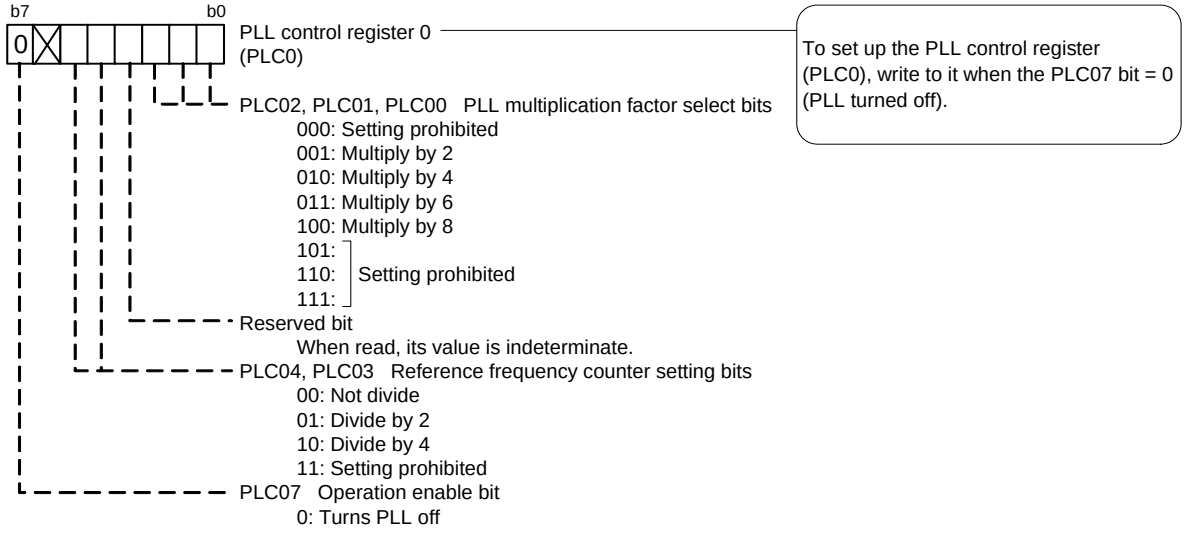


Figure 8. Procedure for Setting Up the Registers to Use a Voltage-Down Interrupt Application (2)

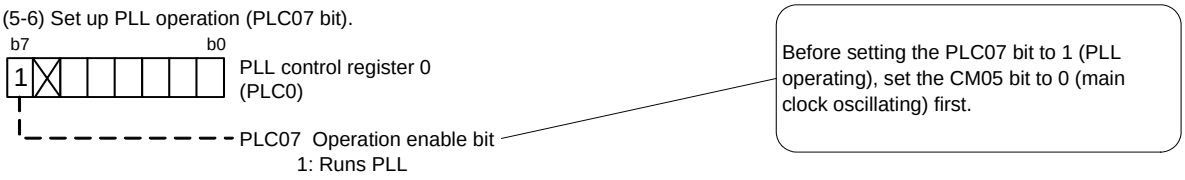
(5-4) Set up the processor mode register 2 (PM2).



(5-5) Set PLC04 and PLC03 (reference frequency counter setting bits) and PLC02, PLC01 and PLC00 (PLL multiplication factor select bits).

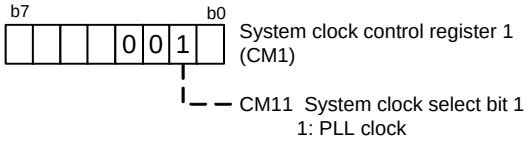


(5-6) Set up PLL operation (PLC07 bit).



(5-7) Wait a while (t_{su}(PLL)) until the PLL oscillation stabilizes.

(5-8) Switch the system clock from the main clock to the PLL clock.



(6) Set up the protect register (PRCR).

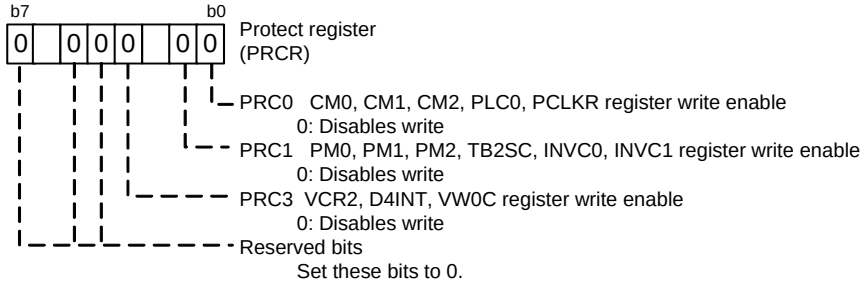


Figure 9. Procedure for Setting Up the Registers to Use a Voltage-Down Interrupt Application (3)

5. Sample Programs

Download a sample program from the Renesas Technology website. Click the screen menu “Application Note” on the left side of the M16C family’s top web page.

6. Reference Documents

Hardware manual

M16C/64 Group Hardware Manual
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