SH7455 Group, SH7456 Group

Using the DRI in Special Mode

R01AN1337EJ0100
Rev.1.00
Mar. 4, 2013

Abstract

This document describes the sample code using Direct RAM Input Interface (hereinafter, DRI) of the SH7455 Group and SH7456 Group (hereinafter, the SH7455).

The feature of the sample code is described below.

- Use DRI in special mode to acquire video data output from a camera module.

Products

SH7455 Group, SH7456 Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

Use DRI in special mode to acquire video data output from a camera module. The required image data is acquired by specifying the target data area. Table 1.1 lists the Peripheral Function and Its Application, Figure 1.1 shows a Waveform of a Camera Module, and Figure 1.2 shows a Target Area for Acquiring Image Data.

Table 1.1 Peripheral Function and Its Application

Peripheral Function	Application
DRI	Acquire video data (parallel data) output from a camera module without stopping CPU operation to write to SHwyRAM integrated in the SH7455.

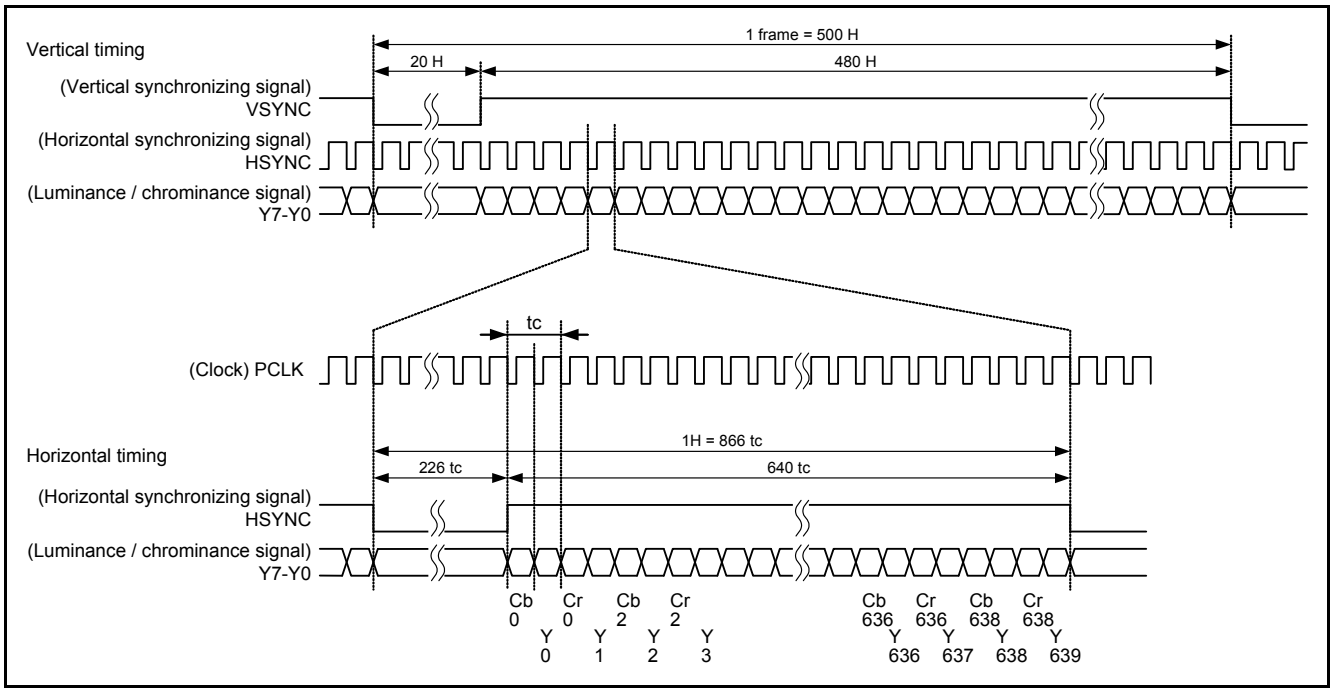
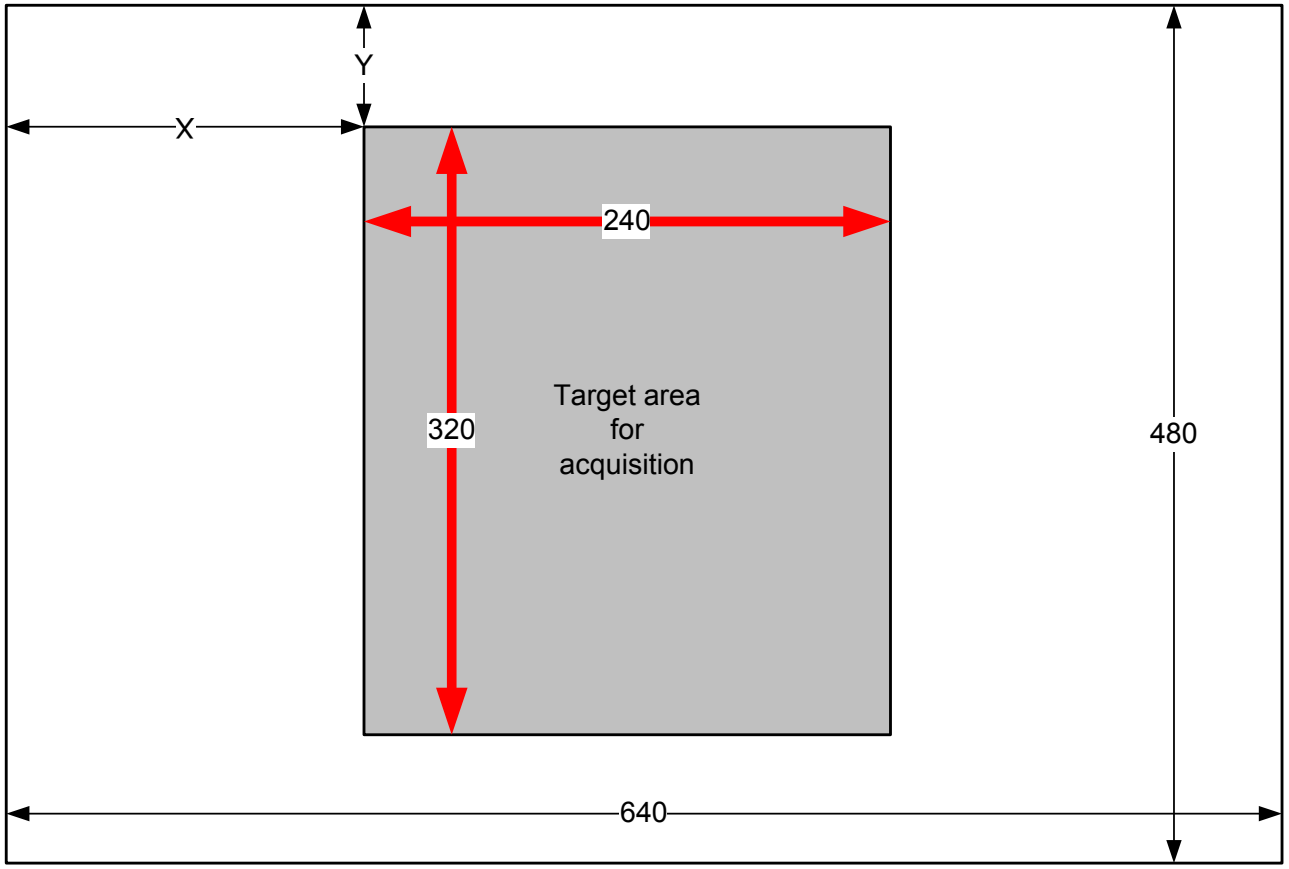


Figure 1.1 Waveform of a Camera Module



From one frame of video data (640 × 480 dots) from a camera module, acquire a 240 × 320 dot image data.
Acquisition beginning points X and Y are specified in the sample code.

Figure 1.2 Target Area for Acquiring Image Data

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	SH7455 Group, SH7456 Group
Operating frequencies	• Input clock frequency: 20 MHz • CPU clock (Ick): 160 MHz • SHwy clock (SHck): 80 MHz • Peripheral clock (Pck): 40 MHz • Peripheral A clock (PAck): 80 MHz
Operating voltages	Vcc = PLLVcc = AVcc = 3.3 V, Vdd = 1.5 V
Integrated development environment	Renesas Electronics Corporation High-performance Embedded Workshop Version 4.09.01.007 (HEW)
C compiler	Renesas Electronics Corporation C/C++ Compiler Package for SuperH RISC engine Family V.9.04 Release 01
	Compile options -cpu=sh4a -object="$(CONFIGDIR)\$(FILELEAF).obj" -debug -gbr=auto -chgincpath -errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 -nologo (Default setting is used in the integrated development environment.)
Operating mode	Single-chip mode
Sample code version	Version 1.00
Board used	SH7455 evaluation board (Product Nos. :R0K474552C000BR/R0K474552C010BR)
Device used	AR camera board (product No.: M3T-M32RUT-ARV2)*

Note: This product is no longer in production.

3. Reference Application Notes

For additional information associated with this document, refer to the following application notes.

- SH7455 Group, SH7456 Group, Register Definition Header File (R01AN0355EJ)
- SH7455 Group, SH7456 Group, Data Communication Using the DRO and DRI (R01AN0588EJ)

4. Hardware

4.1 Hardware Configuration

Figure 4.1 shows an Example of Connecting a Camera Module to the MCU.

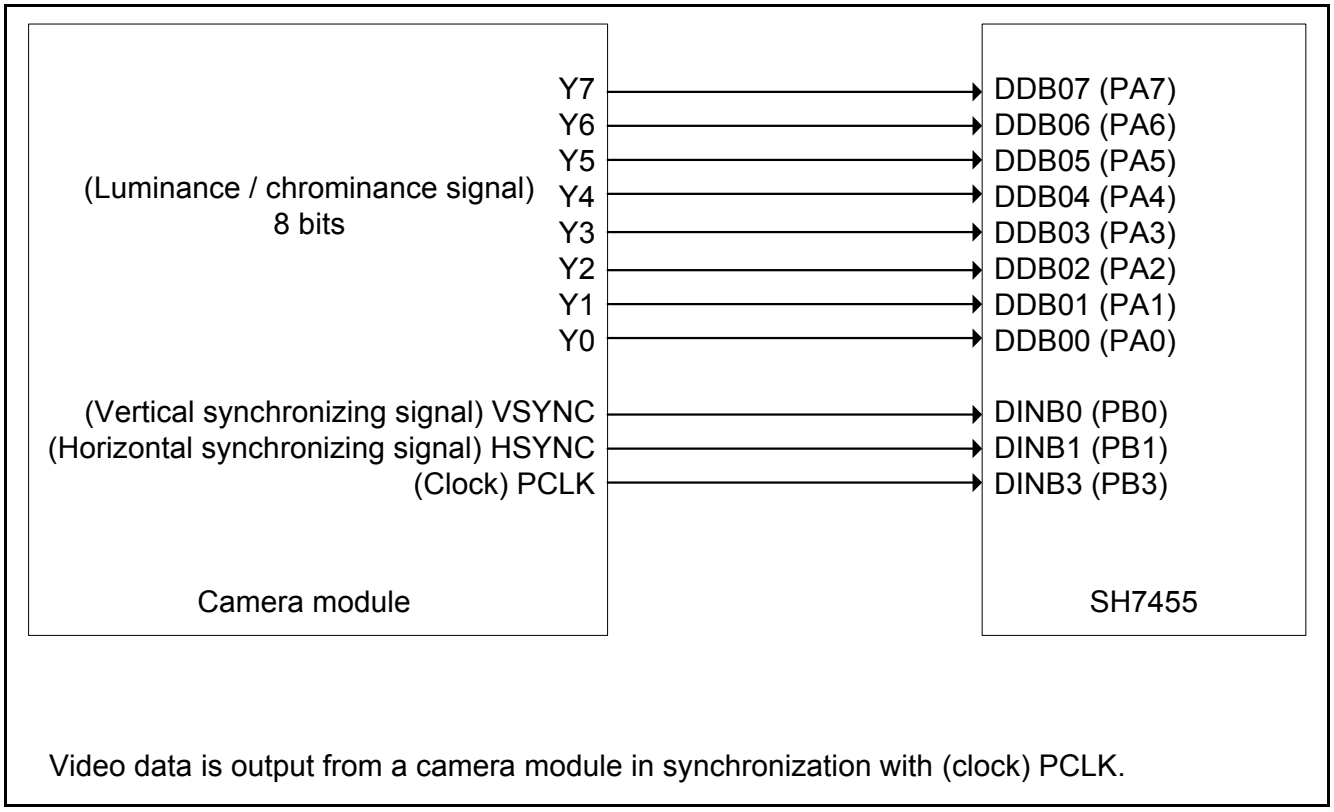


Figure 4.1 Example of Connecting a Camera Module to the MCU

4.2 Pins Used

Table 4.1 lists the Pins Used and Their Functions.

Table 4.1 Pins Used and Their Functions

Pin Name	I/O	Function
PA7/DDB07 to PA0/DDB00	Input	Image data
PB3/DINB3	Input	Data synchronizing signal (clock)
PB1/DINB1	Input	Horizontal synchronizing signal
PB0/DINB0	Input	Vertical synchronizing signal

5. Software

5.1 Operation Overview

In the sample code, the DRI operates in special mode which allows faster data acquisition. The minimum data acquisition period is 25 ns when special mode is on and 43.75 ns when the mode is off. An area of image data specified in the sample code is acquired from one frame of video data using decimation control function of the DEC counter. The function thin out unnecessary data to allow selective data acquisition. Figure 5.1 shows an Operation Timing Diagram.

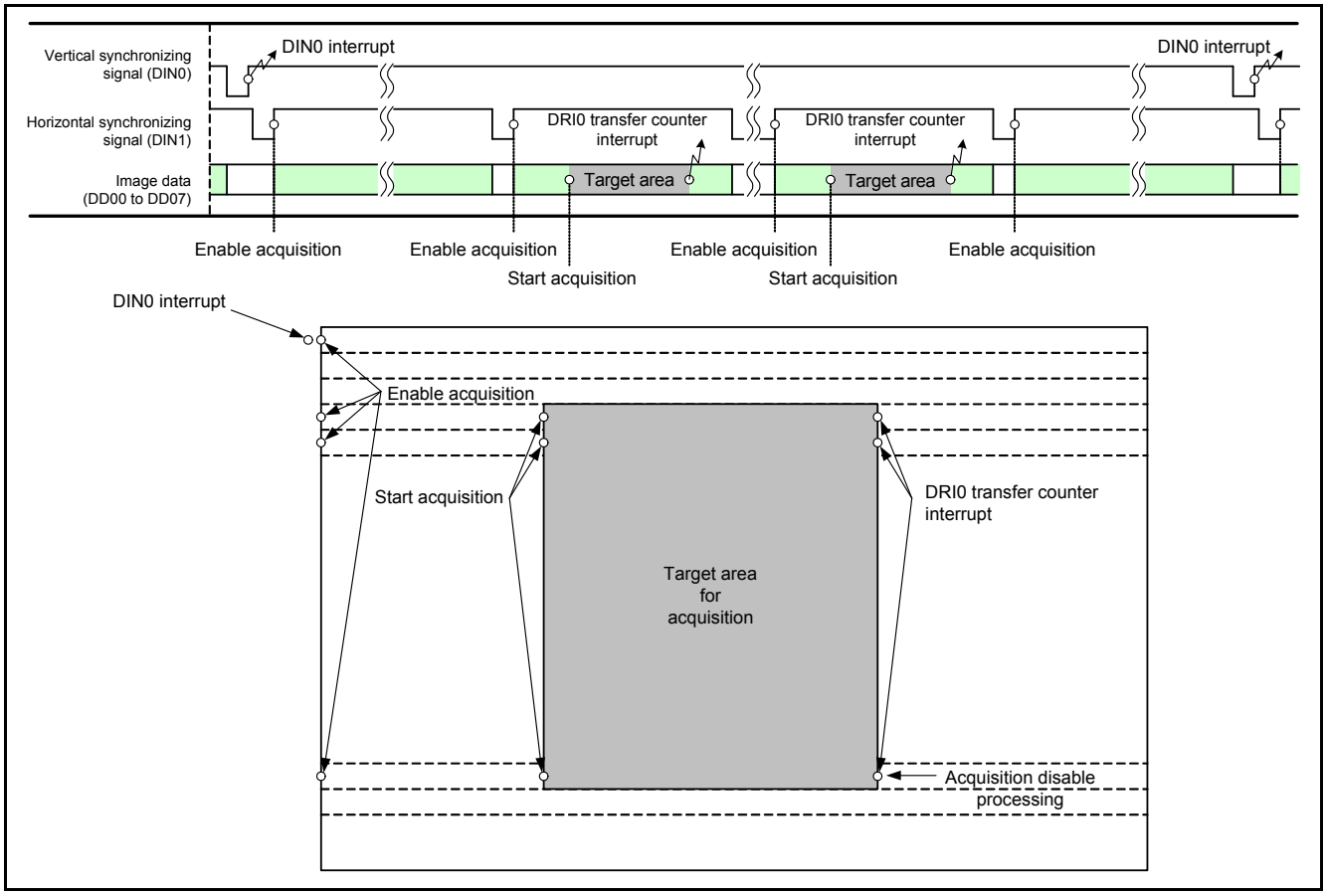


Figure 5.1 Operation Timing Diagram

Table 5.1 describes the Event Counter Settings and Operation Overview.

Table 5.1 Event Counter Settings and Operation Overview

	DEC0	DEC1	DEC2	DEC3
Count enable factor	DIN0 (vertical synchronizing signal)	DIN1 (horizontal synchronizing signal)	DIN1 (horizontal synchronizing signal)	DEC2 underflow
Count event	DIN1 (horizontal synchronizing signal)	DIN3 (data synchronizing signal)	Acquisition event*	DIN3 (data synchronizing signal)
Counter initial value	Unnecessary line count beginning at the vertical synchronizing signal	Unnecessary pixel count beginning at the horizontal synchronizing signal	Effective pixel count in one line	Underflow value (H'ffff)
Reload value				Unnecessary pixel count in one line after effective pixels are acquired
Operation overview	Counts DIN1 event (horizontal synchronizing signal: line count) from the beginning of one frame and underflows at the data acquisition start line.	Counts DIN3 event (data synchronizing signal: pixel count) from the beginning of one line and underflows at the pixel before the data acquisition start point.	Counts acquisition event (effective pixel count) when such event is generated and underflows at data acquisition end point.	Counts DIN3 event (data synchronizing signal: pixel count) from the pixel after data acquisition end point and underflows at the end of one line.

Note: This is an internal event signal of the SH7455. It is generated from DIN3 (data synchronizing signal) to output to an event detection block when acquisition condition is satisfied.

Figure 5.2 shows a Timing Diagram of DRI Data Acquisition (one frame is simplified to a four-line configuration). In this example, the target areas for acquisition are set in the second and third lines of one frame with four lines. In the sample code, the decimation control function enables acquisition only when counters DEC0, DEC1, and DEC3 all underflow. Under these circumstances, the next DIN3 (data synchronizing signal) event detected is effective as an acquisition event. In the diagram, the underflow state of each counter is highlighted in red.

Data acquisition operations are described below.

(1) The rising edge of DIN0 (vertical synchronizing signal) generates a DIN0 interrupt request and the DEC0 counter is enabled. The DRI0 transfer counter interrupt request is enabled during DIN0 interrupt processing.

(2) With the rising edge of DIN1 (horizontal synchronizing signal), counters DEC1 and DEC2 are enabled and data acquisition is enabled. However, data acquisition does not begin at this point since the condition required to execute decimation control for data acquisition is not yet satisfied.

(3) The DEC0 counter counts DIN1 (horizontal synchronizing signal) inputs and underflows at the data acquisition start line. The DEC1 counter counts DIN3 (data synchronizing signal) inputs, i.e., pixels until the acquisition start point and underflows at the pixel before that point. The underflow value for the DEC3 counter is determined at the initial setting.

(4) Data acquisition using the decimation control function is enabled when counters DEC0, DEC1, and DEC3 all underflow. Under these circumstances, the next DIN3 (data synchronizing signal) event detected is effective as an acquisition event which triggers the DEC2 counter to acquire data.

(5) The DEC2 counter counts pixels in the target area of one line. The DEC2 counter and the DRI transfer counter underflow at the end of the target area and a DRI0 transfer counter interrupt is generated. The DEC3 counter is enabled when the DEC2 counter underflows.

(6) The DEC3 counter counts unnecessary pixels in one line and underflows at the end of the line.

(7) The remaining effective lines are counted during DRI0 transfer counter interrupt processing. After acquisition of all data in the target area, DRI data acquisition is disabled to complete the acquisition process.

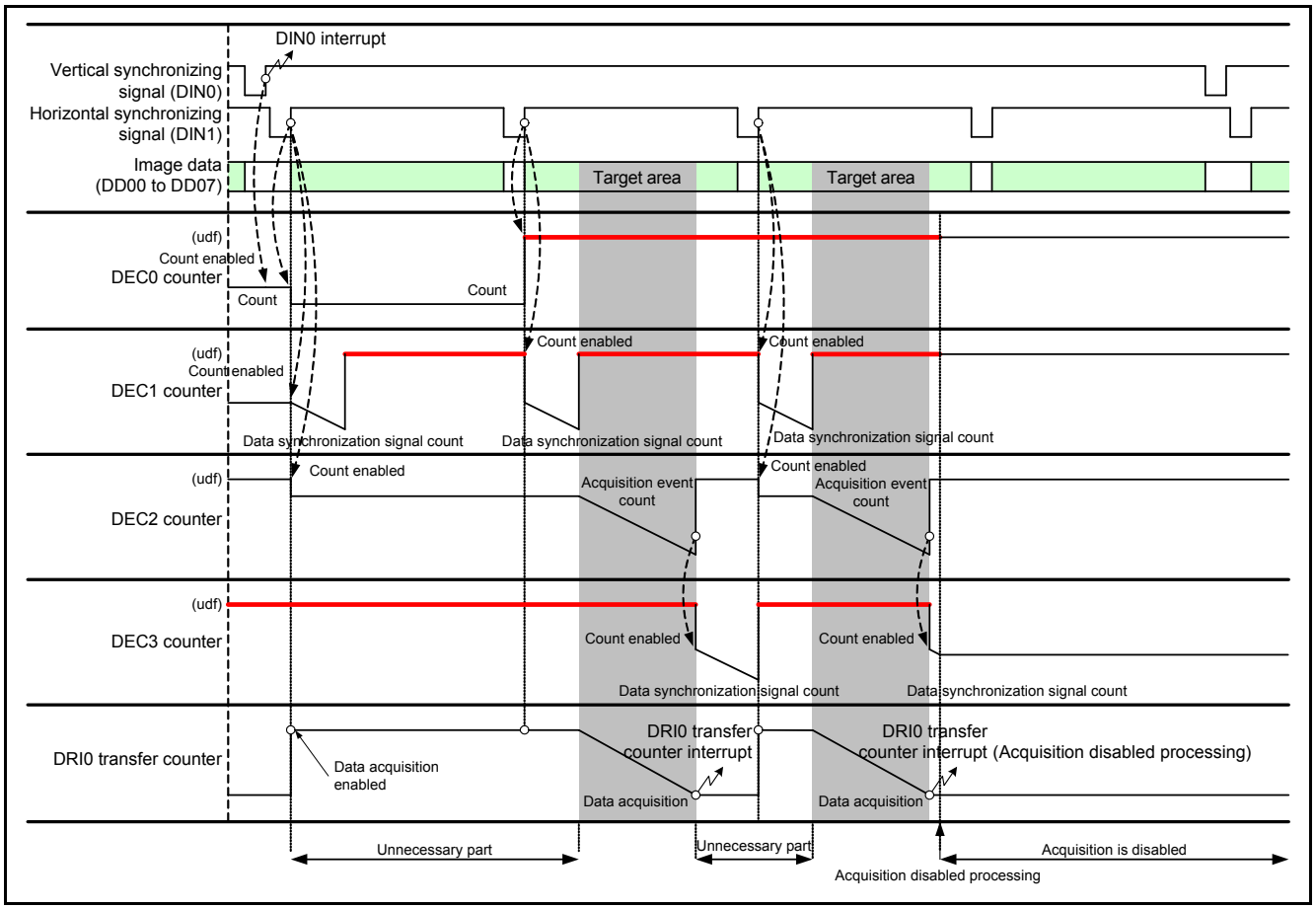


Figure 5.2 Timing Diagram of DRI Data Acquisition (one frame is simplified to a four-line configuration)

Figure 5.3 shows the Event Counters, Variable, and Their Count Values Used to Specify the Target Area. Note that the actual count values are decremented by one because the event counters DEC increment the setting values by one.

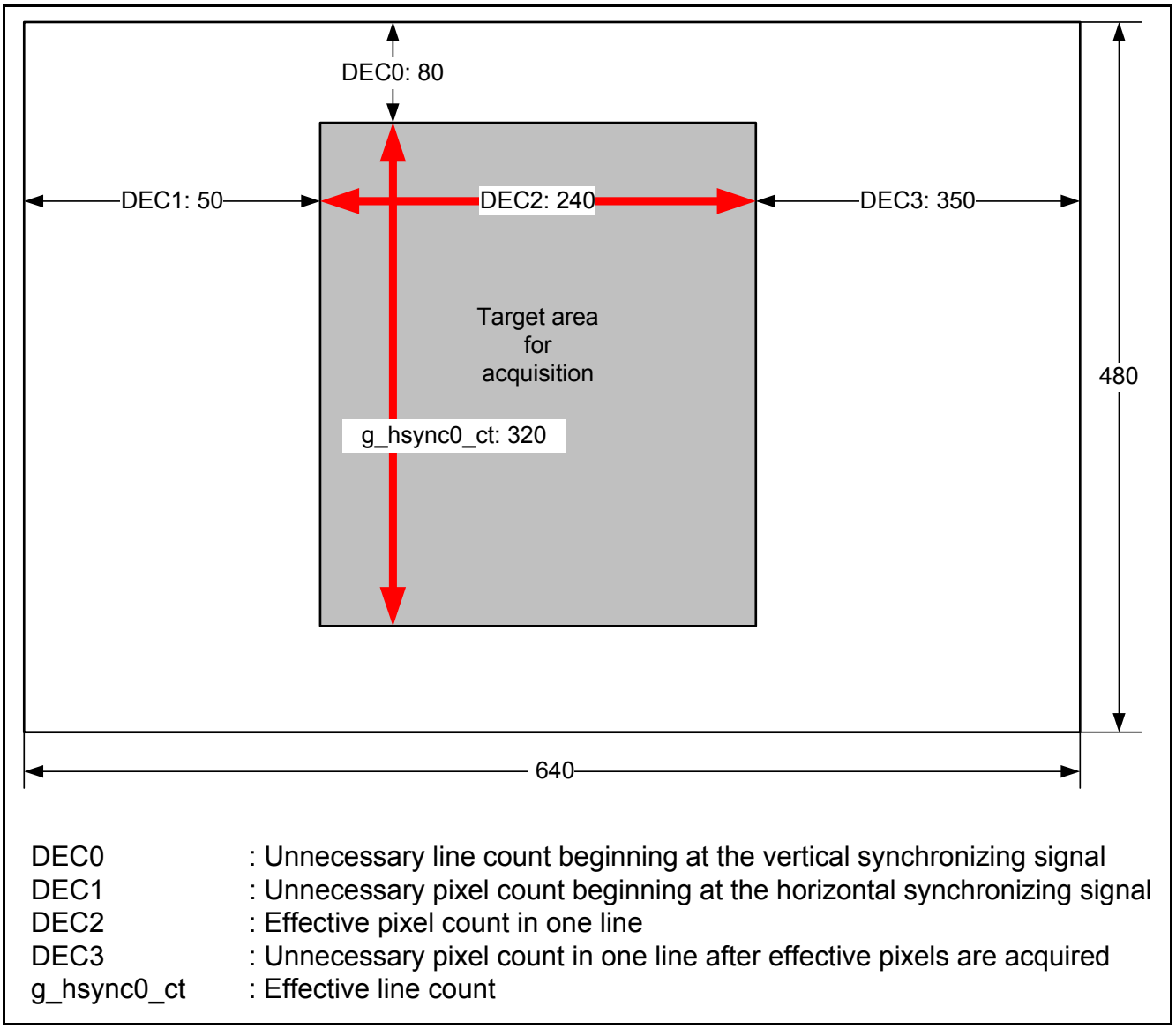


Figure 5.3 Event Counters, Variable, and Their Count Values Used to Specify the Target Area

5.2 Constants

Table 5.2 lists the Constants Used in the Sample Code.

Table 5.2 Constants Used in the Sample Code

Constant Name	Setting Value	Contents
SENSOR_WIDTH	640	Pixel count of the video data output from a camera module
SENSOR_HEIGHT	480	Line count of the video data output from a camera module
PICT_WIDTH	240	Effective pixel count to be acquired by the DRI
PICT_HEIGHT	320	Effective line count to be acquired by the DRI
V_START_POS	80	The line where acquisition by the DRI begins
H_START_POS	50	The pixel where acquisition by the DRI begins
CAP_NOT_END	0	Data acquisition not completed
CAP_END	1	Data acquisition completed

5.3 Variables

Table 5.3 lists the Global Variables.

Table 5.3 Global Variables

Type	Variable Name	Contents	Function Used
unsigned short	g_hsync0_ct	HSYNC counter. Indicates remaining effective line count.	dri0_start, dri0_tr_counter_int
signed long	g_dri0_cap_eflag	Indicates acquisition state as 0: Acquisition not completed 1: Acquisition completed	main, dri0_start, dri0_tr_counter_int

5.4 Functions

Table 5.4 lists the Functions.

Table 5.4 Functions

Function Name	Outline
main	Main processing
dri0_init	DRI0 initial setting
dri0_start	Start data acquisition by DRI0
dri0_vsync_int	Processing executed at DIN0 event (vertical synchronizing signal) detection interrupt
dri0_tr_counter_int	Processing executed at DRI0 transfer counter interrupt

5.5 Function Specifications

The following tables list the sample code function specifications.

Main	
Outline	Main processing
Header	dri.h, typedefine.h
Declaration	void main(void)
Description	Acquire video data (parallel data) output from a camera module without stopping CPU operation using DRI0 to write data to SHwyRAM.
Arguments	None
Returned Value	None

dri0_init	
Outline	DRI0 initial setting
Header	machine.h, typedefine.h, iodefine.h
Declaration	void dri0_init(void)
Description	Set the ports and interrupt controller (INTC) and initialize the DRI0 register.
Arguments	None
Returned Value	None

dri0_start	
Outline	Start data acquisition by DRI0
Header	dri.h, typedefine.h, iodefine.h
Declaration	void dri0_start(unsigned long *dst, unsigned short offset_x, unsigned short offset_y)
Description	Set DRI0 to acquire video data output from a camera module selectively. Set event detection method for DRI0 to start data acquisition.
Arguments	• unsigned long *dst : SHwyRAM address for storing DRI0 output data • unsigned short offset_x : Unnecessary pixel count beginning at the horizontal synchronizing signal • unsigned short offset_y : Unnecessary line count beginning at the vertical synchronizing signal
Returned Value	None

dri0_vsync_int	
Outline	Interrupt function: Processing executed at DIN0 event (vertical synchronizing signal) detection interrupt
Header	iodefine.h
Declaration	void dri0_vsync_int(void)
Description	Clear the DRI0 interrupt request status. Enable the DRI0 transfer counter interrupt request.
Arguments	None
Returned Value	None

dri0_tr_counter_int

Outline	Interrupt function: Processing executed at DRI transfer counter interrupt
Header	typedefine.h, iodefine.h
Declaration	void dri0_tr_counter_int(void)
Description	Clear the DRI0 transfer interrupt request status and decrement the HSYNC counter by one. When the HSYNC counter is 0, DRI0 is set to event detection “input disabled”, data acquisition “disabled”, interrupt request “masked”, and acquisition status “acquisition completed”.
Arguments	None
Returned Value	None

5.6 Flowcharts

5.6.1 Main Processing

Figure 5.4 shows the Main Processing.

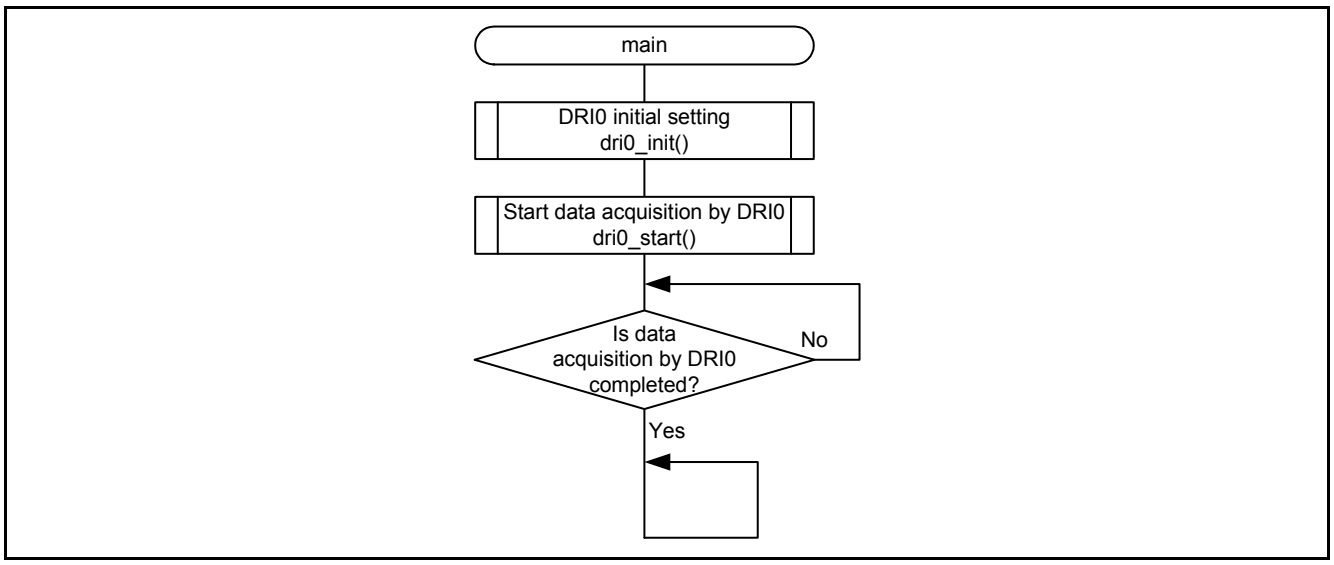


Figure 5.4 Main Processing

5.6.2 DRI0 Initial Setting

Figure 5.5 shows the DRI0 Initial Setting.

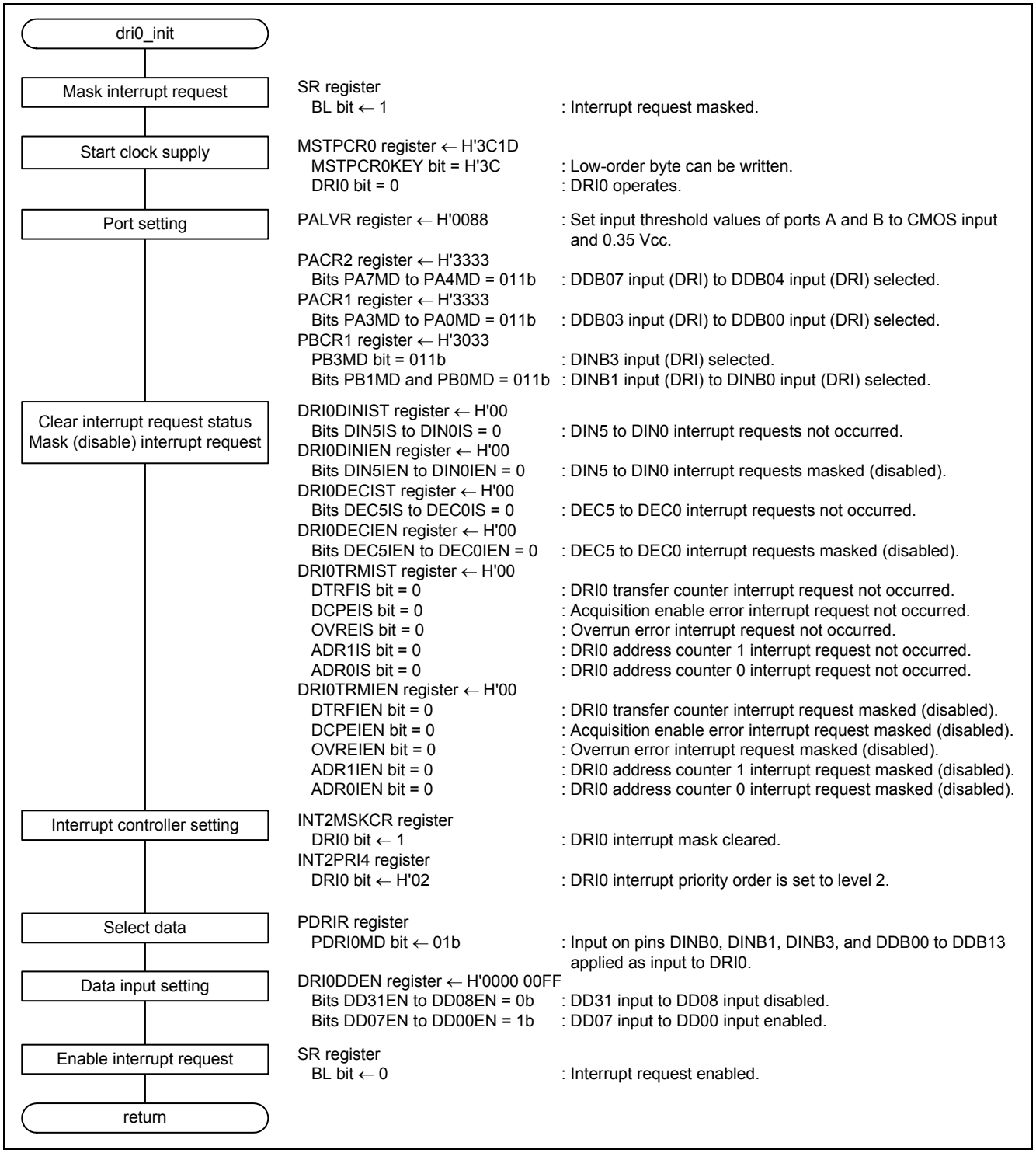


Figure 5.5 DRI0 Initial Setting

5.6.3 DRI0 Data Acquisition Start

Figure 5.6 and Figure 5.7 show the DRI0 Data Acquisition Start.

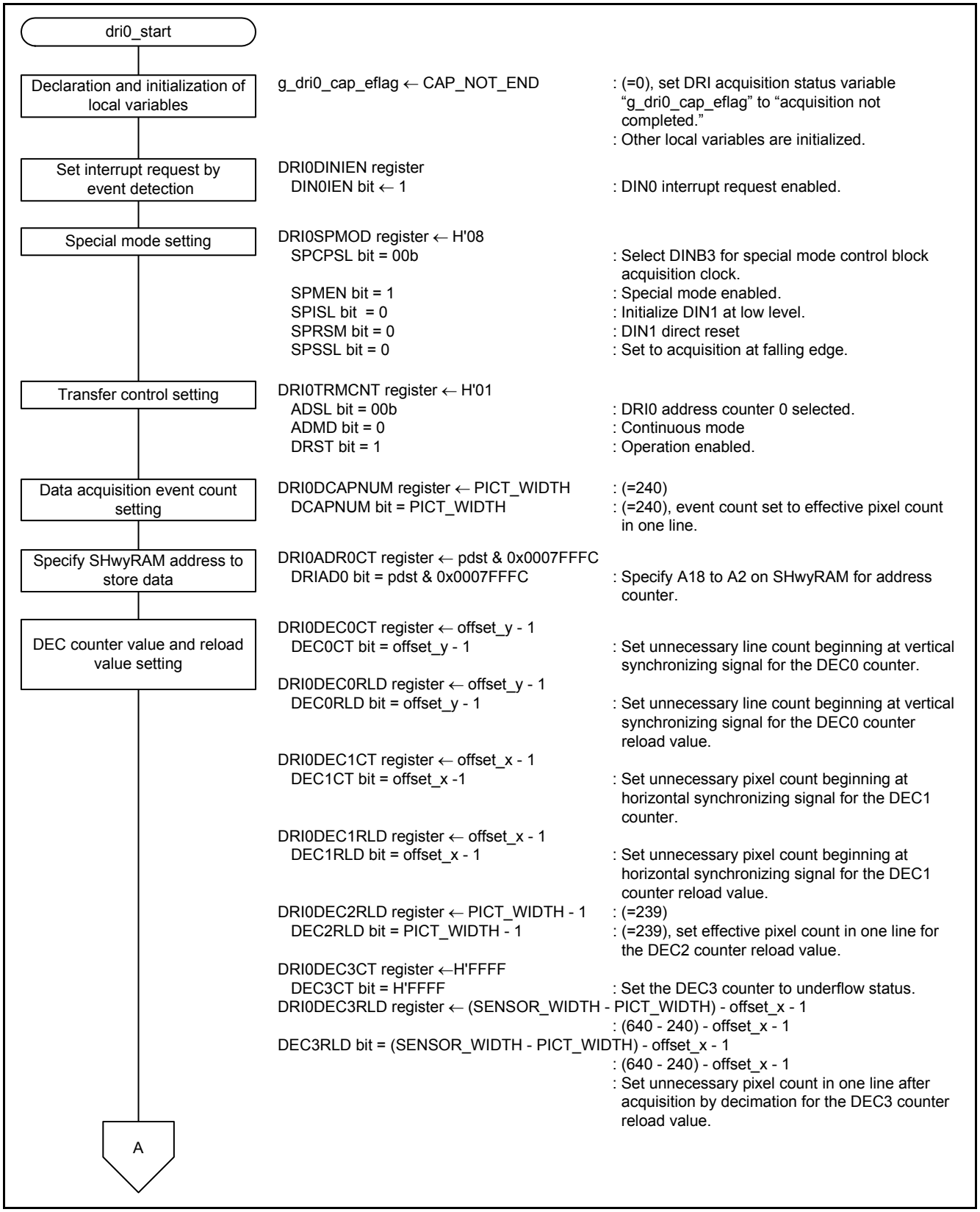


Figure 5.6 DRI0 Data Acquisition Start (1/2)

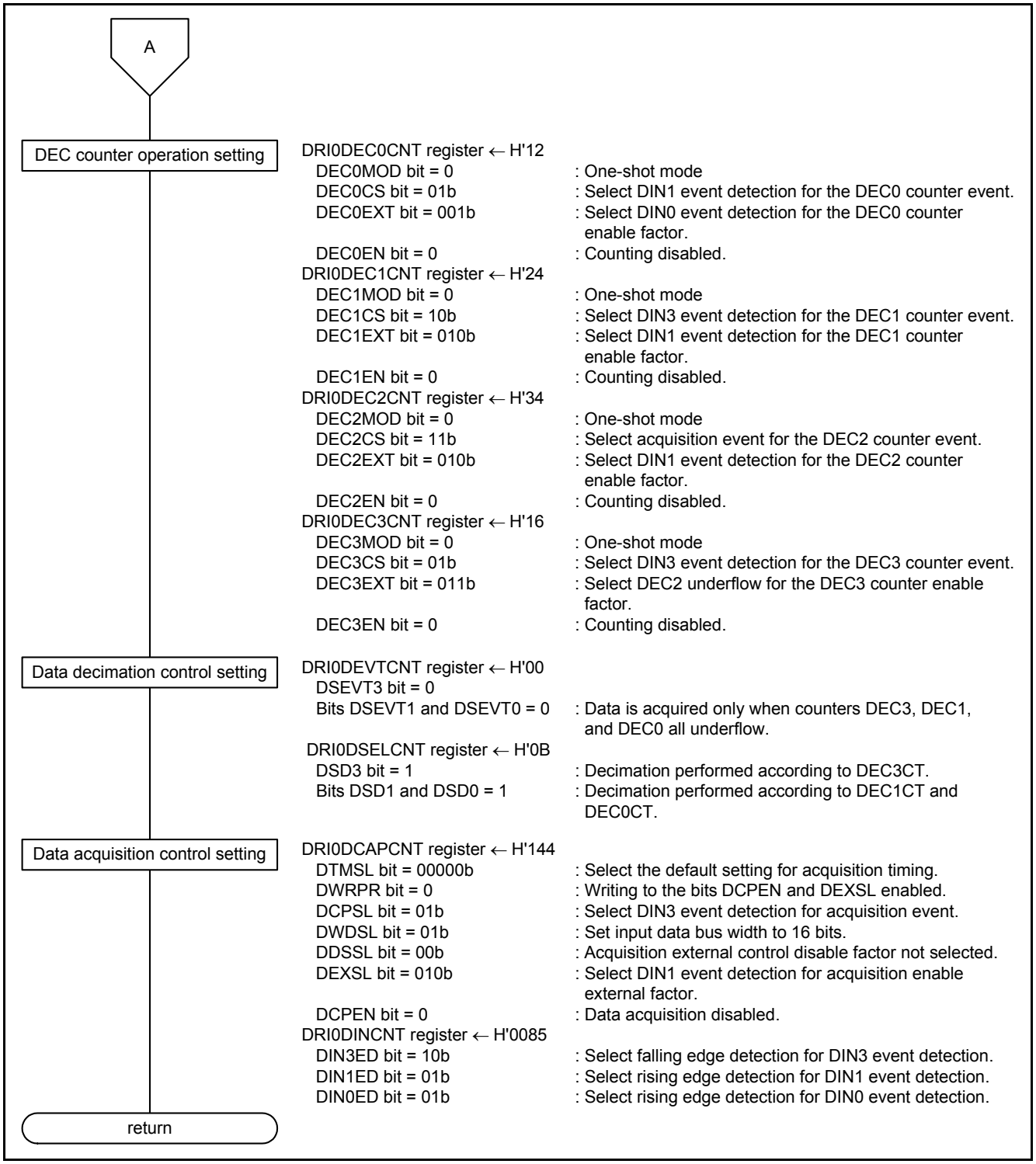


Figure 5.7 DRI0 Data Acquisition Start (2/2)

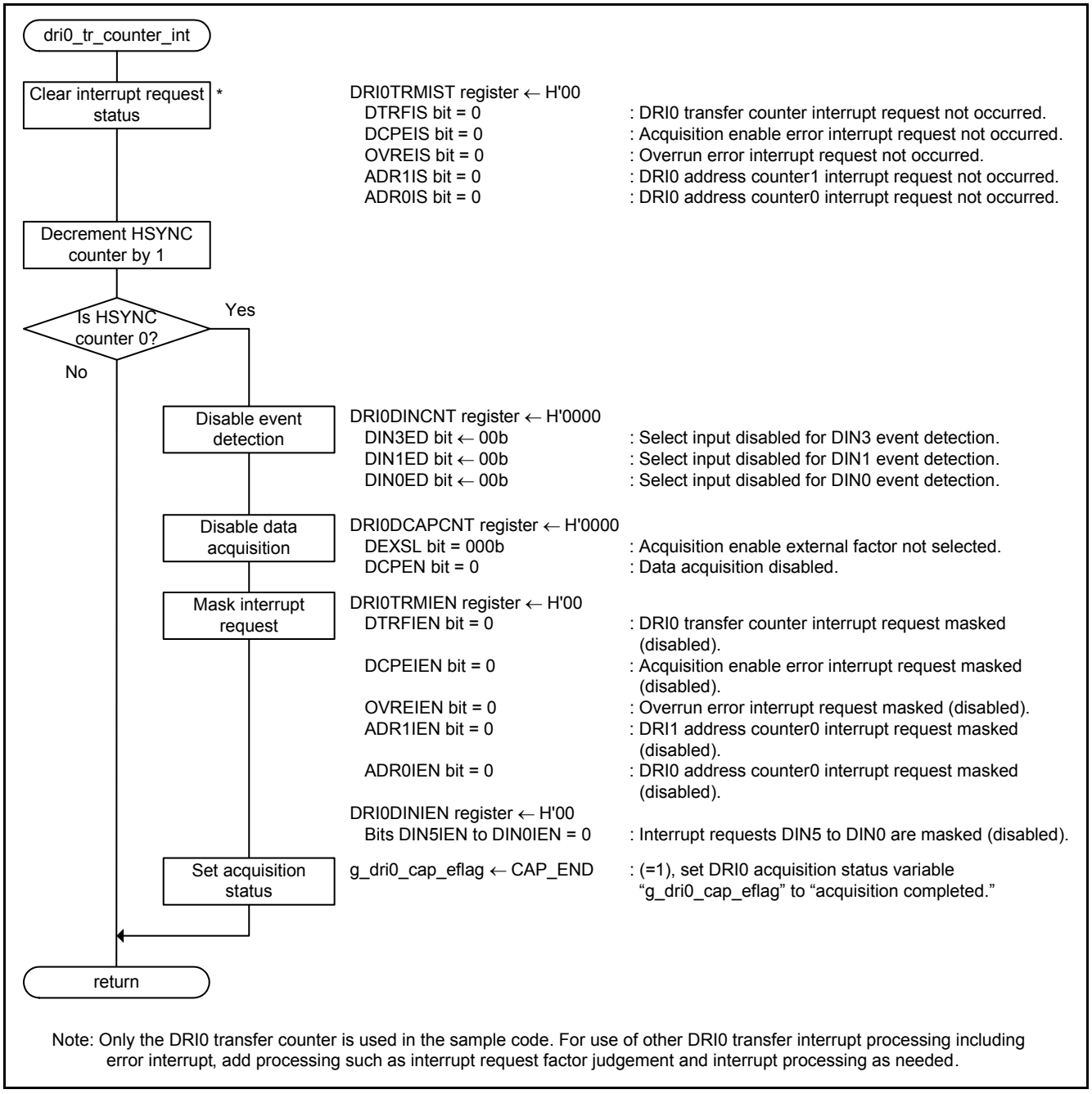
5.6.4 Processing Executed at DIN0 Event (Vertical Synchronizing Signal) Detection Interrupt

Figure 5.8 shows the Processing Executed at DIN0 Event (Vertical Synchronizing Signal) Detection Interrupt.

Figure 5.8 Processing Executed at DIN0 Event (Vertical Synchronizing Signal) Detection Interrupt

5.6.5 Processing at DRI0 Transfer Counter Interrupt

Figure 5.9 shows the Processing at DRI0 Transfer Counter Interrupt.



Note: Only the DRI0 transfer counter is used in the sample code. For use of other DRI0 transfer interrupt processing including error interrupt, add processing such as interrupt request factor judgement and interrupt processing as needed.

Figure 5.9 Processing at DRI0 Transfer Counter Interrupt

6. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

7. Reference Documents

User's Manual: Hardware
SH7455 Group, SH7456 Group User's Manual: Hardware Rev.1.10
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

User's Manual: Development Tools
SuperH™ RISC engine C/C++ Compiler, Assembler, Optimizing Linkage Editor
Compiler Package V.9.04 User's Manual Rev.1.01
The latest version can be downloaded from the Renesas Electronics website.

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REVISION HISTORY	SH7455 Group, SH7456 Group Application Note Using the DRI in Special Mode

Rev.	Date	Description	
		Page	Summary
1.00	Mar. 4, 2013	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
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