To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

SH7262/SH7264 Group

Serial Communication Interface with FIFO, Configuration to Receive Strings in Asynchronous Mode

Summary

This application note describes the configuration example to receive strings using the SH7264 Serial Communication Interface with FIFO (SCIF) in asynchronous mode.

Target Device

SH7262/7264 MCU (In this document, SH7262/SH7264 are described as "SH7264".)

Contents

1. Introduction 2
2. Applications 3
3. Sample Program Listing 11
4. References 18

1. Introduction

1.1 Specifications

- Uses the Serial Communication Interface with FIFO (SCIF) channel 0
- Initializes the SH7264 MCU as the receiver in asynchronous mode, and stores the received data in buffer

1.2 Modules Used

- Serial Communication Interface with FIFO (SCIF)

1.3 Applicable Conditions

MCU	SH7262/SH7264
Operating Frequencies	Internal clock: 144 MHz Bus clock: 72 MHz Peripheral clock: 36 MHz
Integrated Development Environment	Renesas Technology Corp. High-performance Embedded Workshop Ver.4.07.00
C Compiler	Renesas Technology SuperH RISC engine Family C/C++ Compiler Package Ver.9.03 Release 00
Compiler Options	Default setting in the High-performance Embedded Workshop (-cpu=sh2afpu -fpu=single -object="$(CONFIGDIR)\$(FILELEAF).obj" -debug -gbr=auto -chgincpath -errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 –nologo)

1.4 Related Application Notes

For more information, refer to the following application notes:

- SH7262/SH7264 Group Example of Initialization
- SH7262/SH7264 Group Serial Communication Interface with FIFO, Configuration to Transmit Strings in Asynchronous Mode
- SH7262/SH7264 Group Serial Communication Interface with FIFO, Configuring the Serial Communication in Clock Synchronous Mode (Full-duplex)

1.5 About Active-low Pins (Signals)

The symbol "#" suffixed to the pin (or signal) names indicates that the pins (or signals) are active-low.

2. Applications

This application note uses the Serial Communication Interface with FIFO (SCIF).

2.1 SCIF Overview

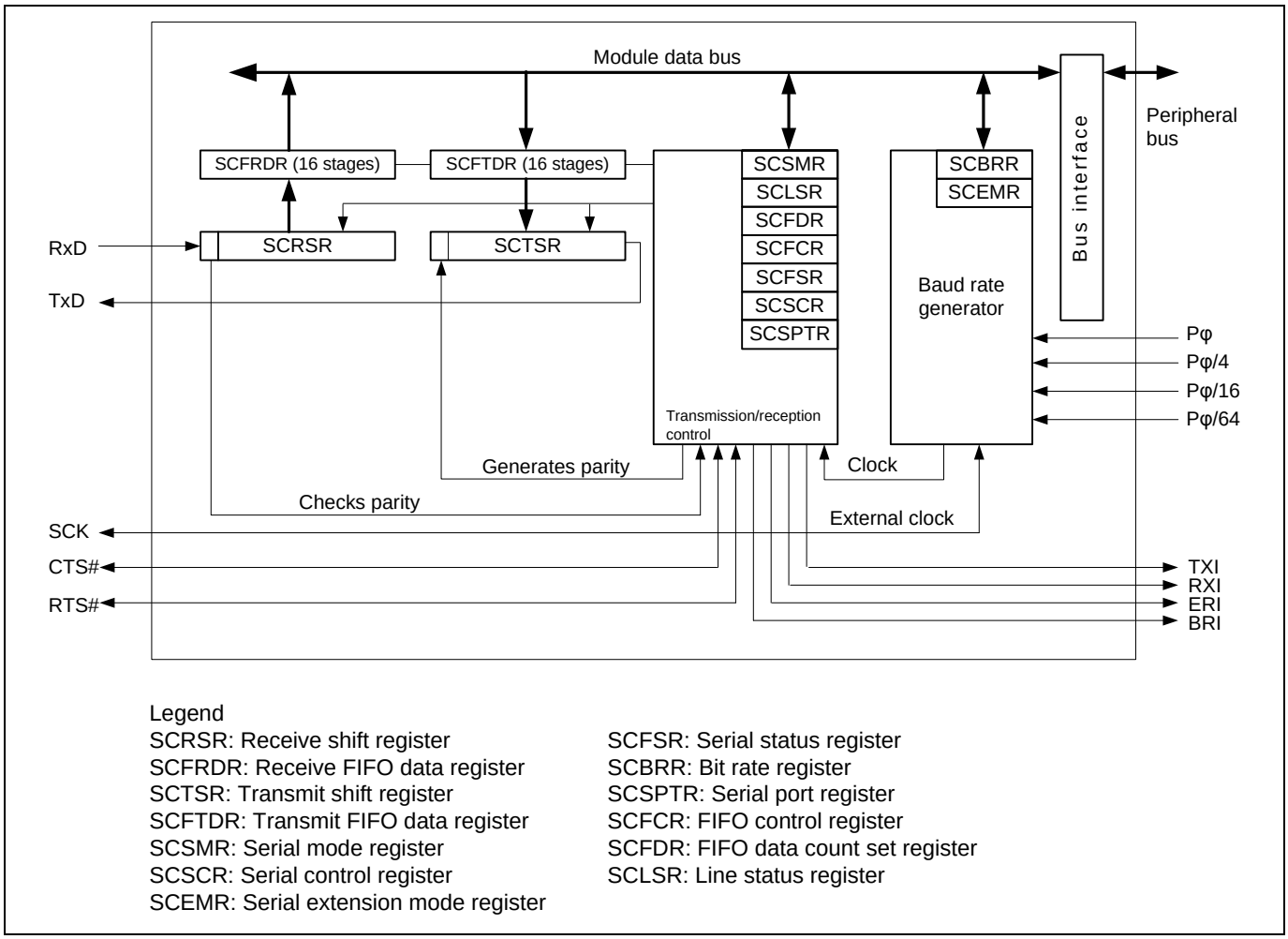
The SH7264 SCIF transmits or receives a "character", appending a start bit which indicates the initiation of the communication, and a stop bit which indicates the end of the communication to data. Then, the SH7264 SCIF handles communication in sync per character. The internal clock or external clock from the SCK pin can be specified as the clock source. Transfer data format and baud rate can be set in the SCIF.

Table 1 lists the overview of the asynchronous mode. Figure 1 shows the SCIF block diagram.

Table 1 SCIF (Asynchronous mode) Overview

Item	Description
Number of channels	8 (SCIF0 to SCIF7)
Clock source	Internal clock: Pφ, Pφ/4, Pφ/16, Pφ/64 Pφ: internal peripheral clock External clock: SCK0 to SCK3 pin input clock (The pin input divided by 16 or 8 is selected as the SCIF operating clock.)
Data format	Transfer data length: 7-bit or 8-bit Order of transfer: LSB first fixed Start bit: 1-bit fixed Stop bit: 1-bit or 2-bit Parity bit: even parity, odd parity, or no parity
Baud rate	When specifying the internal clock: 68.66 bps to 4500 kbps (Pφ is at 36 MHz) When specifying the external clock: up to 1125 kbps (Pφ is at 36 MHz, external clock is at 9 MHz)
Error detection	Parity error, framing error, overrun error
Interrupt request	Transmit-FIFO-data-empty interrupt (TXI) by the transmit FIFO data empty (TDFE) Break interrupt (BRI) by the break (BRK) or overrun error (ORER) Receive FIFO data full (RXI) by the Receive FIFO data full (RDF) or data ready (DR) Receive-error interrupt (ERI) by the receive error (ER)
Other	• Break can be detected • Supplying clock unused channels can be stopped to reduce power consumption • Includes the modem control functions (RTS and CTS), (Only channels 1 and 3. Only channel 1 for the SH7262) • The number of valid data stored in the Transmit and Receive FIFO data registers, and the number of receive errors stored in the Receive FIFO data register can be detected • Time out error (DR) on reception can be detected • Base clock frequency can be either 16 or 8 times the bit rate • Double-speed mode can be specified for the baud rate generator (When not using the SCK pin)

Note: For more information about the SCIF, refer to the Serial Communication Interface with FIFO chapter in the SH7262 Group, SH7264 Group Hardware Manual.



Legend

SCRSR: Receive shift register
SCFRDR: Receive FIFO data register
SCTSR: Transmit shift register
SCFTDR: Transmit FIFO data register
SCSMR: Serial mode register
SCSCR: Serial control register
SCEMR: Serial extension mode register
SCFSR: Serial status register
SCBRR: Bit rate register
SCSPTR: Serial port register
SCFCR: FIFO control register
SCFDR: FIFO data count set register
SCLSR: Line status register

Figure 1 SCIF Block Diagram

2.2 Configuration Procedure

This section describes how to configure the SH7264 SCIF in asynchronous mode. Figure 2 and Figure 3 show flow charts of configuring the reception in asynchronous mode. Figure 4 shows the flow chart of reception in asynchronous mode.

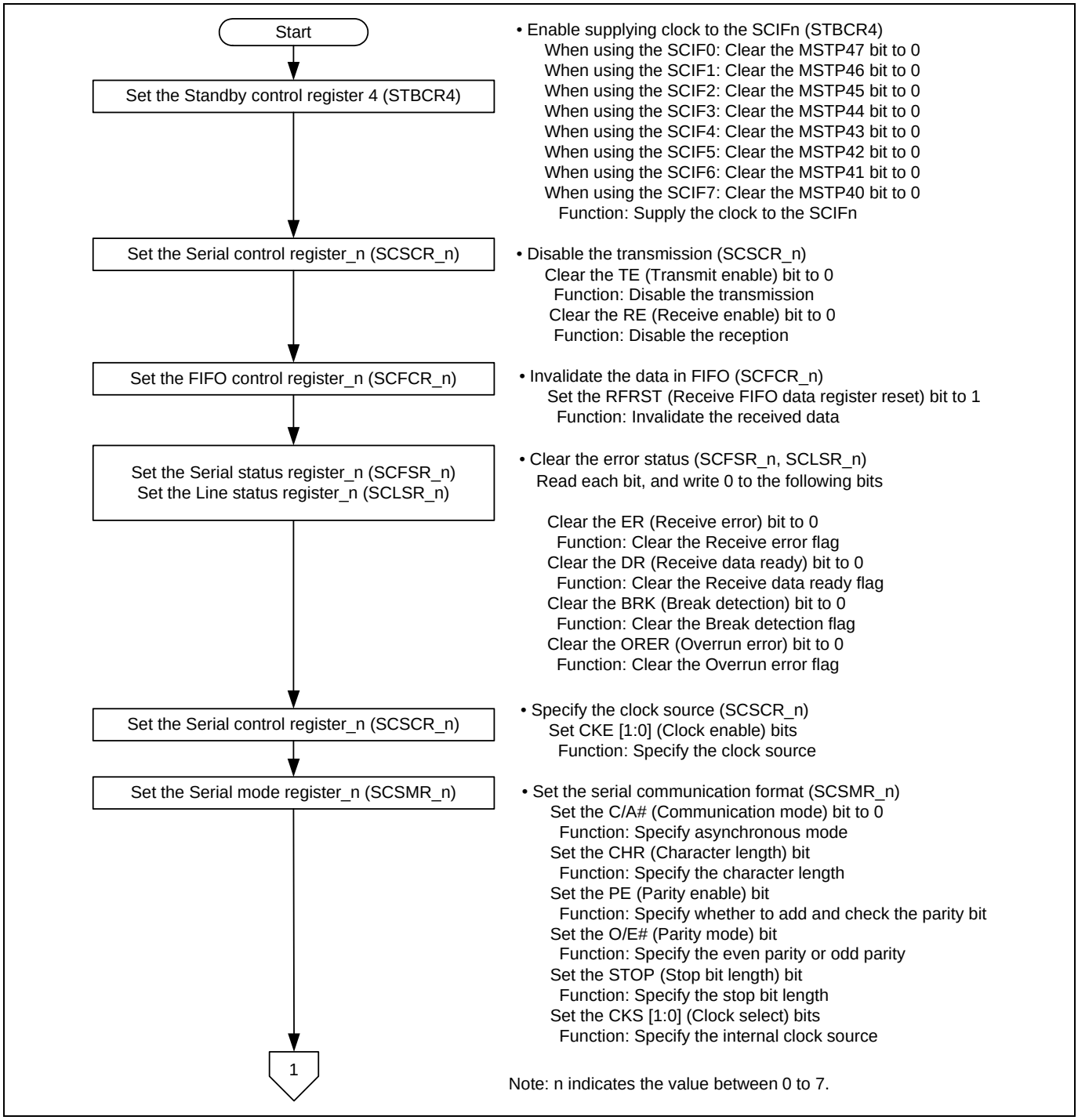
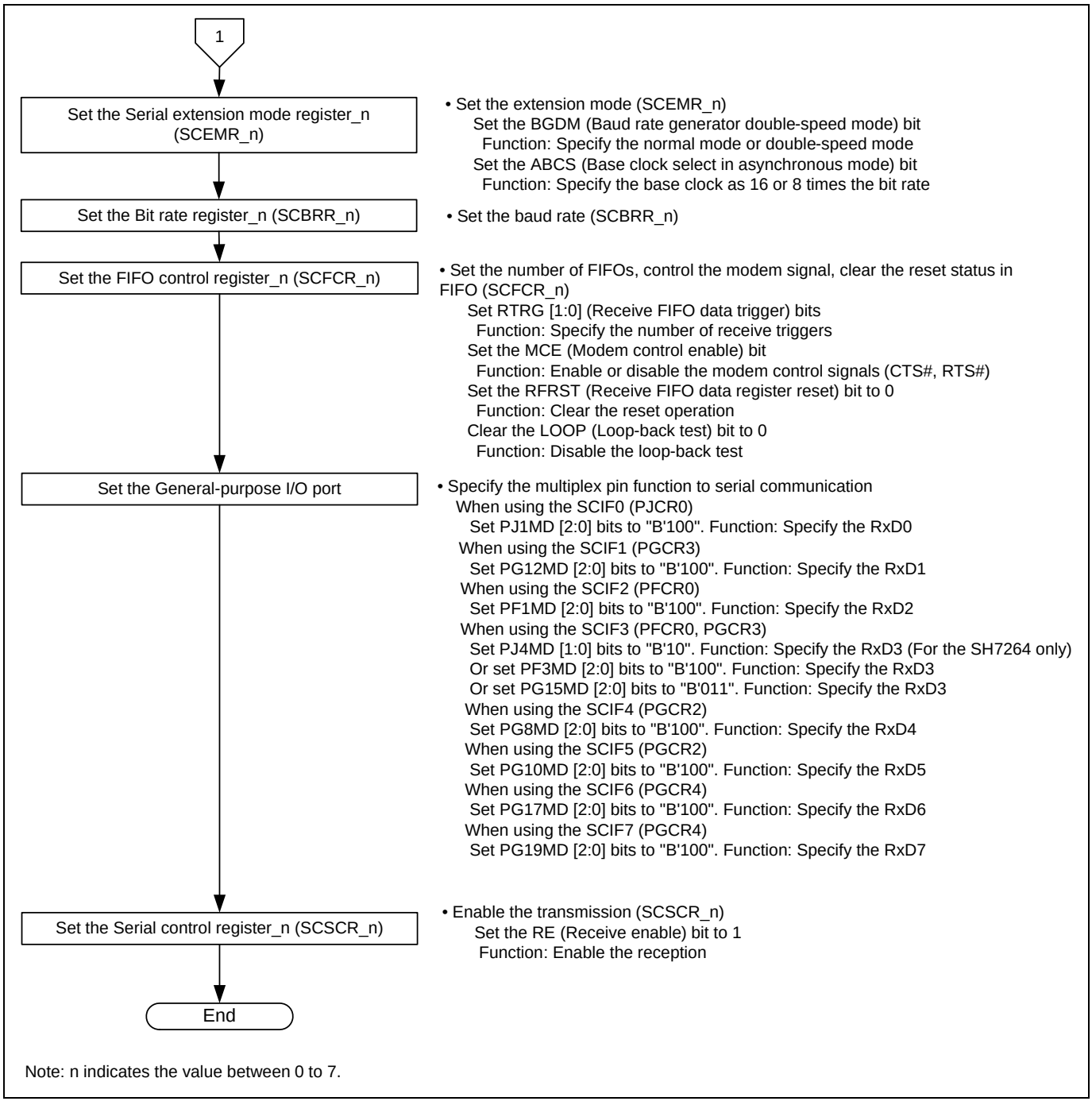


Figure 2 Flow Chart for Configuring the Reception in Asynchronous Mode (1/2)



Note: n indicates the value between 0 to 7.

Figure 3 Flow Chart for Configuring the Reception in Asynchronous Mode (2/2)

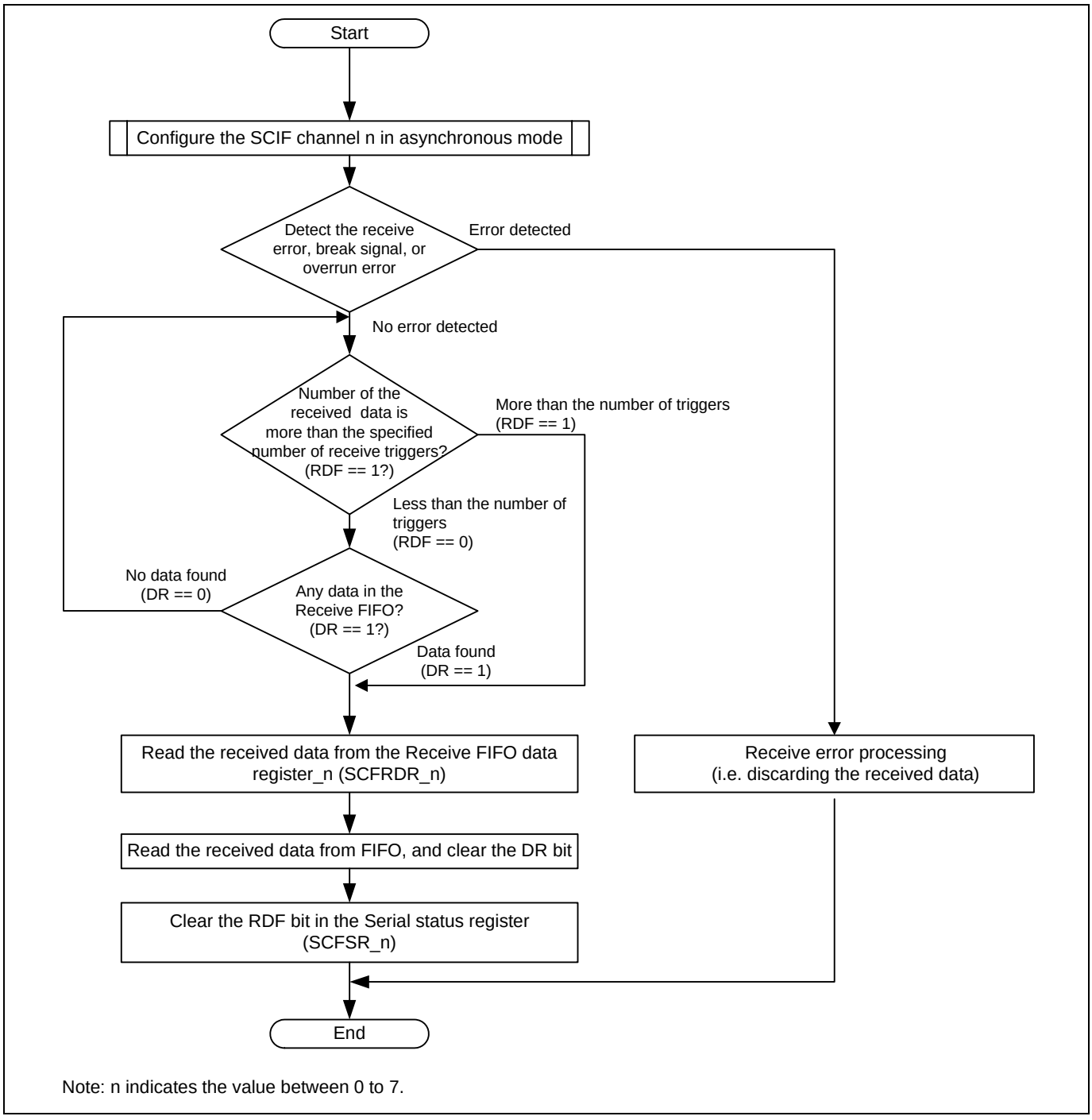


Figure 4 Flow Chart of the Reception in Asynchronous Mode

2.3 Sample Program Operation

This sample program uses the SCIF channel 0 in asynchronous mode, and receives character strings. When the Receive FIFO data full flag (RDF bit) is set to 1, it reads the received data from the Receive FIFO data register. Then, it clears the RDF bit. When the RDF bit is not set, it checks the Receive data ready bit (DR bit) if there is any data in the receive FIFO. If there is data in the receive FIFO, the sample program reads the received data, and then clears the DR bit.

Table 2 lists the reception settings for the sample program. Figure 5 shows the operation timing of the sample program.

Table 2 Sample Program Reception Settings

Communication Format	Setting
Communication mode	Asynchronous mode
Number of channel to use	Channel 0
Interrupt	Not used
Baud rate	19,200 bps
Data length	8-bit
Parity	No parity
Stop bit	1 stop bit
Modem control	RTS/CTS functions are disabled
Bit order	LSB first
Number of FIFO data triggers	14

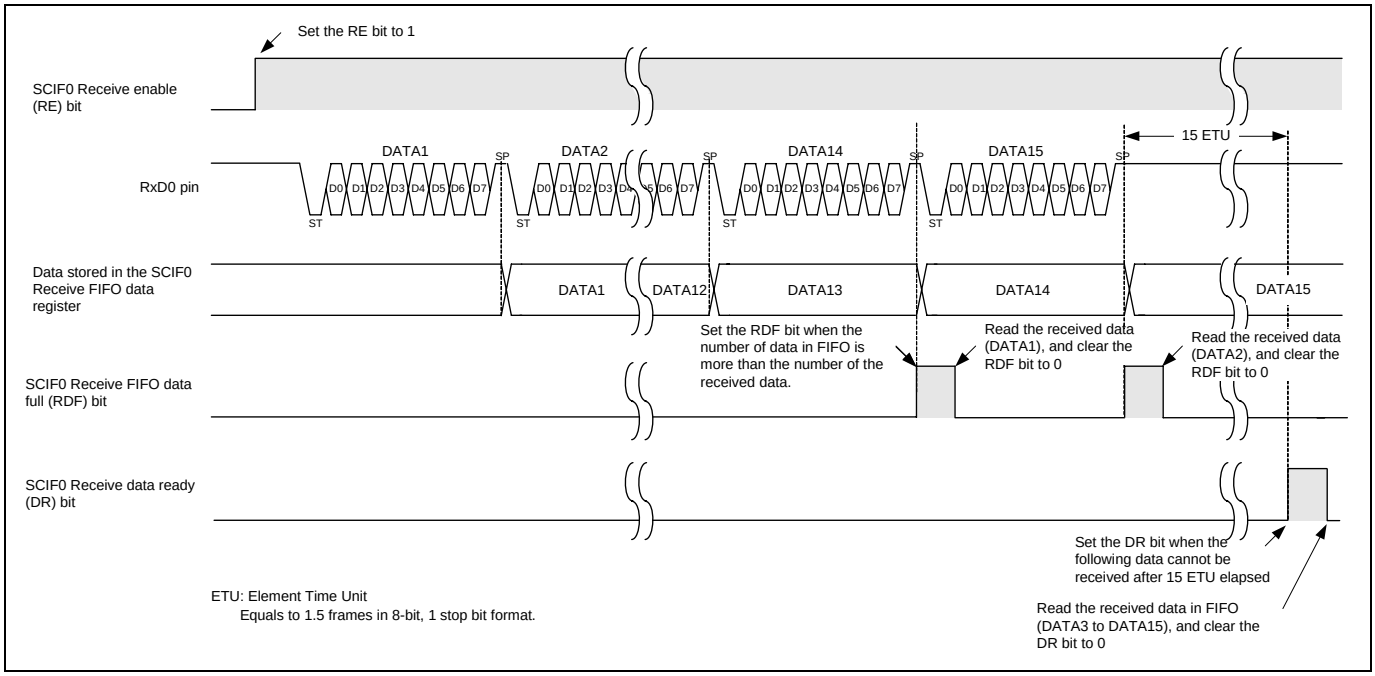


Figure 5 Sample Program Operation Timing

2.4 Sample Program Procedure

The sample program initializes the SCIF channel 0 in asynchronous mode, and checks the Receive FIFO data full (RDF bit) in the Serial status register (SCFSR_0). When the Receive FIFO is full, (RDF = "1"), it receives the data.

Table 3 lists register settings related to the SCIF channel 0 in the sample program. Figure 6 shows the flow chart of the sample program.

Table 3 Sample Program Register Settings

Register Name	Address	Setting	Description
Standby control register 4 (STBCR4)	H'FFFE 040C	H'7F	• MSTP47 = "0": SCIF0 is operating (Supplies the clock)
Port J control register 0 (PJCR0)	H'FFFE 390E	H'0040	• PJ1MD [2:0] = "B'100": RxD0 output (SCIF0)
Serial mode register_0 (SCSMR_0)	H'FFFE 8000	H'0000	• C/A# = "0": Asynchronous mode • CHR = "0": 8-bit data • PE = "0": Disable to add the parity bit • STOP = "0": 1 stop bit • CKS [1:0] = "0": Peripheral clock
Serial control register (SCSCR_0)	H'FFFE 8008	H'0000	• TE = "0": Disable the transmission • RE = "0": Disable the reception • CKE [1:0] = "B'00": Internal clock/SCK pin is an input pin
		H'0010	• RE = "1": Enable the reception
FIFO control register_0 (SCFCR_0)	H'FFFE 8018	H'0002	• RFRST = "1": Enable to reset the Receive FIFO data register
		H'00C0	• RFRST = "0": Disable to reset the Receive FIFO data register • RTRG [1:0] = "B'11": Set the RDF flag when the number of data in the Receive FIFO is equal to or less than 14
Serial extension mode register_0 (SCEMR_0)	H'FFFF 8028	H'0000	• BGDM = "0": Normal mode • ABCS = "0": Base clock is 16 times the bit rate
Bit rate register_0 (SCBRR_0)	H'FFFE 8004	H'3A	Specifies the bit rate as 19,200 bps (Error: −0.69% when Pφ is at 36 MHz)
Serial status register (SCFSR_0)	H'FFFE 8010	H'FF6E	• ER = "0": Receive error • BRK = "0": Break detected • DR = "0": Receive data ready Read bits before clearing to 0.
Line status register_0 (SCLSR_0)	H'FFFE 8024	H'0000	• ORER = "0": Overrun error Read the bit before clearing to 0.

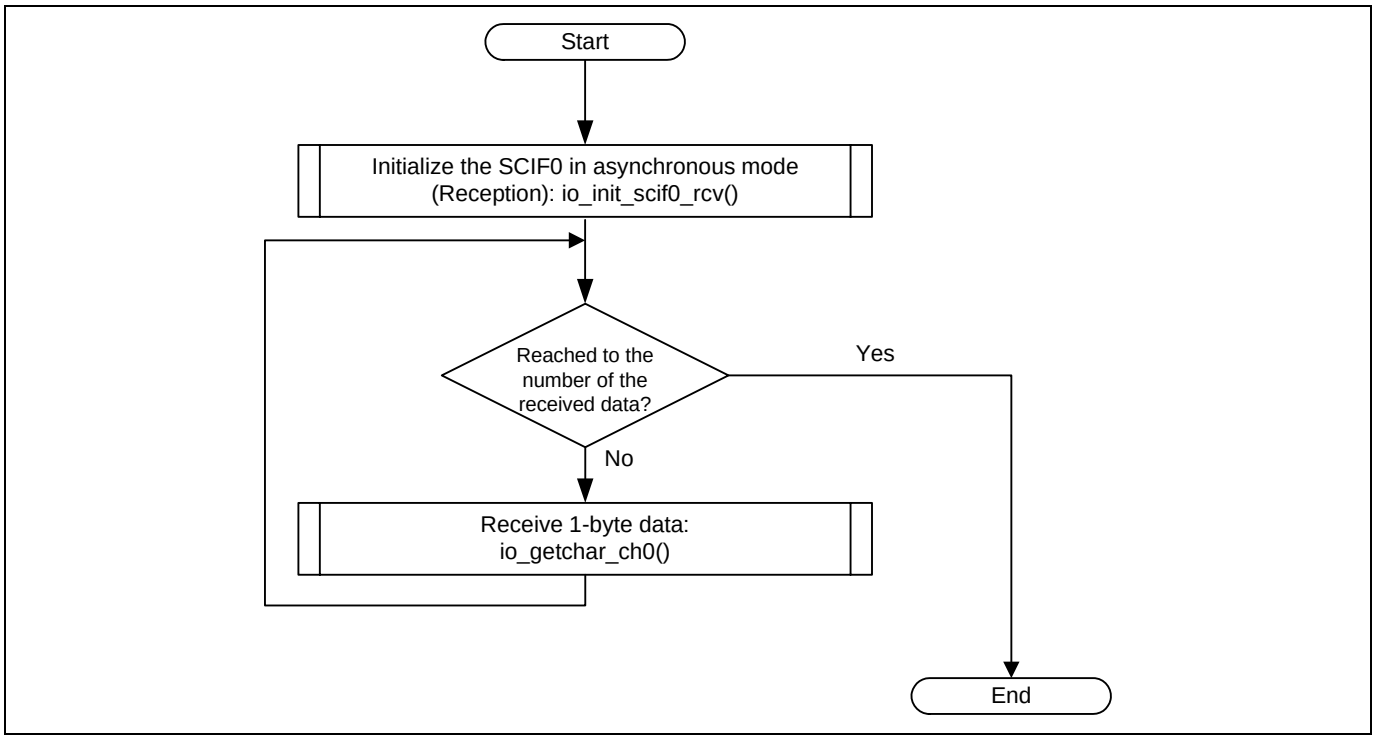


Figure 6 Sample Program Flow Chart

3. Sample Program Listing

3.1 Supplement to the Sample Program

As the capacity of the SH7264 large-capacity internal RAM varies as 1 MB or 640 KB, depending on the MCU type, the section alignment and register setting must be partly altered. To support both MCU types, this application note provides two types of sample programs (workspaces) for 1-MB RAM and 640-KB RAM.

As the MCU with 640-KB RAM must be write-enabled before writing data in the data-retention RAM, the System control register 5 (SYSCR5) is set to write-enable the RAM in the sample program for 640-KB RAM.

Review your product and use the appropriate workspace.

3.2 Sample Program Listing "main.c" (1/6)

```
1       /***********************************************************************
2       *   DISCLAIMER
3       *
4       *   This software is supplied by Renesas Technology Corp. and is only
5       *   intended for use with Renesas products. No other uses are authorized.
6       *
7       *   This software is owned by Renesas Technology Corp. and is protected under
8       *   all applicable laws, including copyright laws.
9       *
10      *   THIS SOFTWARE IS PROVIDED "AS IS" AND RENESAS MAKES NO WARRANTIES
11      *   REGARDING THIS SOFTWARE, WHETHER EXPRESS, IMPLIED OR STATUTORY,
12      *   INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, FITNESS FOR A
13      *   PARTICULAR PURPOSE AND NON-INFRINGEMENT.  ALL SUCH WARRANTIES ARE EXPRESSLY
14      *   DISCLAIMED.
15      *
16      *   TO THE MAXIMUM EXTENT PERMITTED NOT PROHIBITED BY LAW, NEITHER RENESAS
17      *   TECHNOLOGY CORP. NOR ANY OF ITS AFFILIATED COMPANIES SHALL BE LIABLE
18      *   FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL OR CONSEQUENTIAL DAMAGES
19      *   FOR ANY REASON RELATED TO THIS SOFTWARE, EVEN IF RENESAS OR ITS
20      *   AFFILIATES HAVE BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.
21      *
22      *   Renesas reserves the right, without notice, to make changes to this
23      *   software and to discontinue the availability of this software.
24      *   By using this software, you agree to the additional terms and
25      *   conditions found by accessing the following link:
26      *   http://www.renesas.com/disclaimer
27      ***********************************************************************
28      *   Copyright (C) 2009. Renesas Technology Corp., All Rights Reserved.
29      *""FILE COMMENT""*********** Technical reference data *************************
30      *   System Name : SH7264 Sample Program
31      *   File Name   : main.c
32      *   Abstract    : Serial communication interface with FIFO (SCIF).
33      *               : Reception in asynchronous mode sample program
34      *   Version     : 1.00.00
35      *   Device      : SH7262/SH7264
36      *   Tool-Chain  : High-performance Embedded Workshop (Ver.4.07.00).
37      *               : C/C++ compiler package for the SuperH RISC engine family
38      *               :                              (Ver.9.03 Release00).
39      *   OS          : None
40      *   H/W Platform: M3A-HS64G50 (CPU board)
41      *   Description :
42      ***********************************************************************
43      *   History     : Dec.03,2009 ver.1.00.00
44      *""FILE COMMENT END""*****************************************************/
45      #include "iodefine.h"       /* SH7264 iodefine  */
46
```

3.3 Sample Program Listing "main.c" (2/6)

```
47    /* ==== Prototype declaration ==== */
48    void main(void);
49    void io_init_scif0_rcv(int);
50    unsigned char io_getchar_ch0(void);
51
52    /* ==== Type definition ==== */
53    /* SCIF baud rate setting */
54    typedef struct  {
55      unsigned char scbrr;    /* SCBRR register setting */
56      unsigned short scsmr;       /* SCSMR register setting */
57    } SH7264_BAUD_SET;
58
59    /* ---- Baud rate specified value ---- */
60    enum{
61      CBR_1200,
62      CBR_2400,
63      CBR_4800,
64      CBR_9600,
65      CBR_19200,
66      CBR_31250,
67      CBR_38400,
68      CBR_57600,
69      CBR_115200
70    };
71
72    /* ==== Register setting table (P clock = 36 MHz) ==== */
73    static SH7264_BAUD_SET scif_baud[] = {
74      {233, 1},    /*  1200 bps (error: 0.16%) */
75      {116, 1},    /*  2400 bps (error: 0.16%) */
76      {233, 0},    /*  4800 bps (error: 0.16%) */
77      {116, 0},    /*  9600 bps (error: 0.16%) */
78      { 58, 0},    /* 19200 bps (error: -0.69%) */
79      { 35, 0},    /* 31250 bps (error: 0.00%) */
80      { 28, 0},    /* 38400 bps (error: 1.02%) */
81      { 19, 0},    /* 57600 bps (error: -2.34%) */
82      {  9, 0}     /*115200 bps (error: -2.34%) */
83    };
84
85    /* ==== Receive data buffer ==== */
86    unsigned char rcv_data[16];
87
88
```

3.4 Sample Program Listing "main.c" (3/6)

```
89    /*""FUNC COMMENT""*****************************************************************
90     * ID            :
91     * Outline       : Sample program main (Asynchronous serial I/O reception).
92     *-------------------------------------------------------------------------------
93     * Include       : "iodefine.h"
94     *-------------------------------------------------------------------------------
95     * Declaration   : void main(void);
96     *-------------------------------------------------------------------------------
97     * Description   : Initializes the SCIF0 to receive data in asynchronous mode,
98     *               : and stores 16-byte received data in buffer.
99     *-------------------------------------------------------------------------------
100    * Argument      : void
101    *-------------------------------------------------------------------------------
102    * Return Value  : void
103    *-------------------------------------------------------------------------------
104    * Note          :
105    *""FUNC COMMENT END""*************************************************************/
106   void main(void)
107   {
108     int i;
109
110     /* ==== Initializes the SCIF0 in asynchronous mode (reception) ==== */
111     io_init_scif0_rcv(CBR_19200);   /* Specifies the bit rate as 19200 bps */
112
113     /* ==== Receives data ==== */
114     for(i=0; i < sizeof(rcv_data); i++){
115       /* ---- Receives 1-byte data ---- */
116        rcv_data[i] = io_getchar_ch0();
117     }
118
119     while(1){
120       /* Program end */
121     }
122   }
123
```

3.5 Sample Program Listing "main.c" (4/6)

```
/*""FUNC COMMENT""*****************************************************************
 * ID            :
 * Outline       : Configure the SCIF0 as the receiver in asynchronous mode
 *-----------------------------------------------------------------------------
 * Include       : "iodefine.h"
 *-----------------------------------------------------------------------------
 * Declaration   : void io_init_scif0_rcv(int bps);
 *-----------------------------------------------------------------------------
 * Description   : Configures the SCIF0 as the receiver in asynchronous mode.
 *               : Sets it in asynchronous mode, 8-bit, no parity,
 *               : 1 stop bit, and RTS/CTS disabled.
 *               : Specify the baud rate by the argument "bps".
 *-----------------------------------------------------------------------------
 * Argument      : int bps ; I : Baud rate specified value (Table index)
 *-----------------------------------------------------------------------------
 * Return Value  : void
 *-----------------------------------------------------------------------------
 * Note          : The above baud rate specified value is applicable when using
 *               : the peripheral clock (operating frequency for the peripheral
 *               : module using the internal clock) is 36 MHz. Alter the baud rate
 *               : setting when using other clocks.
 *""FUNC COMMENT END""*************************************************************/
void io_init_scif0_rcv(int bps)
{
  /* ==== Wakes up the MCU from power-down mode ==== */
  /* ---- Sets the Standby control register 4 (STBCR4) ---- */
  CPG.STBCR4.BIT.MSTP47 = 0;      /* Starts to supplying clock to the SCIF0 */

  /* ==== Configures the SCIF0  ==== */
  /* ---- Sets the Serial control register (SCSCRi) ---- */
  SCIF0.SCSCR.WORD = 0x0000;      /* SCIF0 stops transmission/reception */

  /* ---- Sets the FIFO control register (SCFCRi) ---- */
  SCIF0.SCFCR.BIT.TFRST = 1;      /* Resets the transmit FIFO */

  /* ---- Sets the Serial status register (SCFSRi) ---- */
  SCIF0.SCFSR.WORD &= 0xff6eu;/* Clears bits ER, BRK, and DR */

  /* ---- Sets the Line status register (SCLSRi) ---- */
  SCIF0.SCLSR.BIT.ORER = 0;       /* Clears ORER */

  /* ---- Sets the Serial control register (SCSCRi) ---- */
  SCIF0.SCSCR.BIT.CKE = 0x0;      /* B'00: internal clock */

```

3.6 Sample Program Listing "main.c" (5/6)

```
168     /* ---- Sets the Serial mode register (SCSMRi) ---- */
169     SCIF0.SCSMR.WORD = scif_baud[bps].scsmr;
170                                /*  Communication mode, 0: Asynchronous mode  */
171                                /*  Character length, 0: 8-bit data   */
172                                /*  Parity enable, 0: Disables to add and check parity */
173                                /*  Parity mode, 0: Even parity */
174                                /*  Stop bit length, 0: 1 stop bit */
175                                /*  Clock select: Setting in table */
176
177     /* ---- Sets the Serial extension mode register (SCEMRi) ---- */
178     SCIF0.SCEMR.WORD = 0x0000;      /* Baud rate generator double-speed mode, 0: Normal mode */
179                                /* Base clock select in asynchronous mode, */
180                                /*   0: Base clock is 16 times the bit rate */
181
182     /* ---- Sets the Bit rate register (SCBRRi) ---- */
183     SCIF0.SCBRR.BYTE = scif_baud[bps].scbrr;
184
185     /* ---- Sets the FIFO control register (SCFCRi) ---- */
186     SCIF0.SCFCR.WORD = 0x00C0;      /* RTS output active trigger: Default */
187                                /* Number of the receive FIFO data trigger: 14 */
188                                /* Modem control enable: Disabled */
189                                /* Receive FIFO data register reset: Disabled */
190                                /* Loop-back test: Disabled */
191
192     /* ==== Sets the General-purpose I/O port ==== */
193     PORT.PJCR0.BIT.PJ1MD = 4;       /* Specifies the RxD0 pin */
194
195     /* ---- Sets the Serial control register (SCSCRi) ---- */
196     SCIF0.SCSCR.BIT.RE = 1;         /* Enables the SCIF0 to receive data */
197   }
198
199   /*""FUNC COMMENT""*****************************************************************
200    * ID            :
201    * Outline       : SCIF0 1 character reception
202    *-----------------------------------------------------------------------------
203    * Include       : "iodefine.h"
204    *-----------------------------------------------------------------------------
205    * Declaration   : unsigned char io_getchar_ch0(void);
206    *-----------------------------------------------------------------------------
207    * Description   : Reads the received data from the Receive FIFO data register.
208    *               : When it detects a framing error, parity error, overrun error,
209    *               : or break signal, it returns 0.
210    *-----------------------------------------------------------------------------
211    * Argument      : void
212    *-----------------------------------------------------------------------------
213    * Return Value  : Received data
214    *-----------------------------------------------------------------------------
215    * Note          :
216    *""FUNC COMMENT END""*************************************************************/
```

3.7 Sample Program Listing "main.c" (6/6)

```
217   unsigned char io_getchar_ch0(void)
218   {
219     unsigned char data;
220
221     /* ==== Detects the receive error, break signal, or overrun error ==== */
222     if((SCIF0.SCFSR.WORD & 0x0090u ) || (SCIF0.SCLSR.BIT.ORER == 1)) {
223       /* Receive error processing (discarding the received data) */
224       SCIF0.SCSCR.BIT.RE = 0;       /* Disables to receive data */
225       SCIF0.SCFCR.BIT.RFRST = 1; /* Resets the receive FIFO */
226       SCIF0.SCFCR.BIT.RFRST = 0; /* Enables the receive FIFO */
227       SCIF0.SCFSR.WORD &= ~0x0091u; /* Clears bits ER, BRK, and DR */
228
229       SCIF0.SCLSR.BIT.ORER = 0;     /* Clears the ORER bit */
230       SCIF0.SCFSR.BIT.RDF = 0;   /* Clears the RDF bit */
231
232       SCIF0.SCSCR.BIT.RE = 1;       /* Enables to receive data */
233       return 0;
234     }
235
236     /* ==== Number of the received data is more than the specified number
237               of receive triggers? (RDF == 1?) ==== */
238     while(SCIF0.SCFSR.BIT.RDF == 0){
239       /* After receiving data, certain period of time elapsed? (DR == 1?) */
240       if(SCIF0.SCFSR.BIT.DR == 1){
241           /* Stops to wait for the RDF flag because FIFO is not empty */
242           break;
243       }
244     }
245
246     /* ==== Reads the received data from the Receive FIFO data register (SCFRDR0) ==== */
247     data = SCIF0.SCFRDR.BYTE;
248
249     /* ==== Clears the DR bit after reading the received data from FIFO ==== */
250     SCIF0.SCFSR.BIT.DR = 0;     /* When FIFO is empty, the DR bit is cleared */
251
252     /* ==== Clears the RDF bit in the Serial status register (SCFSR0) ==== */
253     SCIF0.SCFSR.BIT.RDF = 0;/* Clears the RDF bit */
254
255     return data;
256   }
257
258   /* End of File */
```

4. References

- Software Manual
  SH-2A/SH2A-FPU Software Manual Rev. 3.00
  The latest version of the software manual can be downloaded from the Renesas website.

- Hardware Manual
  SH7262 Group, SH7264 Group Hardware Manual Rev. 2.00
  The latest version of the hardware manual can be downloaded from the Renesas website.

Website and Support

Renesas Technology Website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry
csc@renesas.com

Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Mar. 12, 2010	—	First edition issued

Notes regarding these materials

1. This document is provided for reference purposes only so that Renesas customers may select the appropriate Renesas products for their use. Renesas neither makes warranties or representations with respect to the accuracy or completeness of the information contained in this document nor grants any license to any intellectual property rights or any other rights of Renesas or any third party with respect to the information in this document.
2. Renesas shall have no liability for damages or infringement of any intellectual property or other rights arising out of the use of any information in this document, including, but not limited to, product data, diagrams, charts, programs, algorithms, and application circuit examples.
3. You should not use the products or the technology described in this document for the purpose of military applications such as the development of weapons of mass destruction or for the purpose of any other military use. When exporting the products or technology described herein, you should follow the applicable export control laws and regulations, and procedures required by such laws and regulations.
4. All information included in this document such as product data, diagrams, charts, programs, algorithms, and application circuit examples, is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas products listed in this document, please confirm the latest product information with a Renesas sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas such as that disclosed through our website. (http://www.renesas.com)
5. Renesas has used reasonable care in compiling the information included in this document, but Renesas assumes no liability whatsoever for any damages incurred as a result of errors or omissions in the information included in this document.
6. When using or otherwise relying on the information in this document, you should evaluate the information in light of the total system before deciding about the applicability of such information to the intended application. Renesas makes no representations, warranties or guaranties regarding the suitability of its products for any particular application and specifically disclaims any liability arising out of the application and use of the information in this document or Renesas products.
7. With the exception of products specified by Renesas as suitable for automobile applications, Renesas products are not designed, manufactured or tested for applications or otherwise in systems the failure or malfunction of which may cause a direct threat to human life or create a risk of human injury or which require especially high quality and reliability such as safety systems, or equipment or systems for transportation and traffic, healthcare, combustion control, aerospace and aeronautics, nuclear power, or undersea communication transmission. If you are considering the use of our products for such purposes, please contact a Renesas sales office beforehand. Renesas shall have no liability for damages arising out of the uses set forth above.
8. Notwithstanding the preceding paragraph, you should not use Renesas products for the purposes listed below:
   (1) artificial life support devices or systems
   (2) surgical implantations
   (3) healthcare intervention (e.g., excision, administration of medication, etc.)
   (4) any other purposes that pose a direct threat to human life
   Renesas shall have no liability for damages arising out of the uses set forth in the above and purchasers who elect to use Renesas products in any of the foregoing applications shall indemnify and hold harmless Renesas Technology Corp., its affiliated companies and their officers, directors, and employees against any and all damages arising out of such applications.
9. You should use the products described herein within the range specified by Renesas, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas shall have no liability for malfunctions or damages arising out of the use of Renesas products beyond such specified ranges.
10. Although Renesas endeavors to improve the quality and reliability of its products, IC products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Please be sure to implement safety measures to guard against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other applicable measures. Among others, since the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
11. In case Renesas products listed in this document are detached from the products to which the Renesas products are attached or affixed, the risk of accident such as swallowing by infants and small children is very high. You should implement safety measures so that Renesas products may not be easily detached from your products. Renesas shall have no liability for damages arising out of such detachment.
12. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written approval from Renesas.
13. Please contact a Renesas sales office if you have any questions regarding the information contained in this document, Renesas semiconductor products, or if you have any other inquiries.