SH7216

IEEE1588 PTP Clock Synchronization over Ethernet

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Introduction

The purpose of this application note is to demonstrate the ability to synchronize clocks on two boards using the IEEE1588 protocol. Each board has a clock and each board puts out a pulse once every second on a GPIO pin. The analysis uses an oscilloscope with two channels so the pulses from each board can be viewed together. The scope is set up to trigger on the pulses form the master (IXXAT) board. The object of the demo is to show the two clock pulses quickly synchronize and then stay locked during operation to within 10's of nanoseconds.

NOTE: This is not a training session on IEEE1588, we will leave that to the experts and refer readers to some of the references listed in the back of this document.

Target Device

SH7216

Contents

1. Setup for Analysis

The following items are required in order to build and run this demonstration.

1.1 Renesas Development Tools (software)

The following tools and their versions were used for building the code for this analysis. Evaluation editions of these tools are all available for download from our website.

- High-performance Embedded Workshop (HEW) Version 4.07.xx.xx (or later)
  http://www.renesas.com/download

  Web Search Keyword: “High-performance Embedded Workshop”

- Renesas SuperH RISC Engine Standard Toolchain Version 9.3. Release 00 (or later)
  http://www.renesas.com/download

  Web Search Keyword: “SuperH Compiler”

1.2 Hardware used for Analysis

The following items are needed for the demo below.

- Renesas RSK board for SH7216
  http://america.renesas.com/products/tools/introductory_evaluation_tools/renesas_demo_kits/yrdksh7216/yrdksh7216.jsp
- IXXAT PTP Master Clock board
- SMSC Evaluation LAN board
- MII Evaluation Adapter board
- Oscilloscope with at least two channels
- Serial Cable, Null Modem
- Two Cat5 Ethernet cables

1.3 Anaylsis Software

The software consisted of a HEW workspace. This workspace can be built and downloaded to the Renesas RSK board using the E10A. Software for the Grand Master node is pre-loaded into the flash on the IXXAT board. The IXXAT software is supplied as a pre-built library. More detailed documentation on the RSK hardware is included with the kit or can be downloaded from the Renesas Web site.

NOTE: The PTP Stack and the Micrium TCP/IP stack source codes are restricted to IXXAT and Micrium licensees. Please contact the appropriate vendor for software licensing.

2. Hardware Set-up Description

The demonstration is used to show clock Synchronization between the Grand Master (IXXAT demo board) and Slave Node (Renesas RSK) boards. The Hardware should be setup as shown in Figure 1. The connections to the PC provide further methods for analyzing the IEEE1588 operation as follows:

- RS232 – Status message from the PTP Application/Stack. Outputs clock drift information
- CAT5 Ethernet – Used with Wireshark can observe and decode IEEE1588 packets.

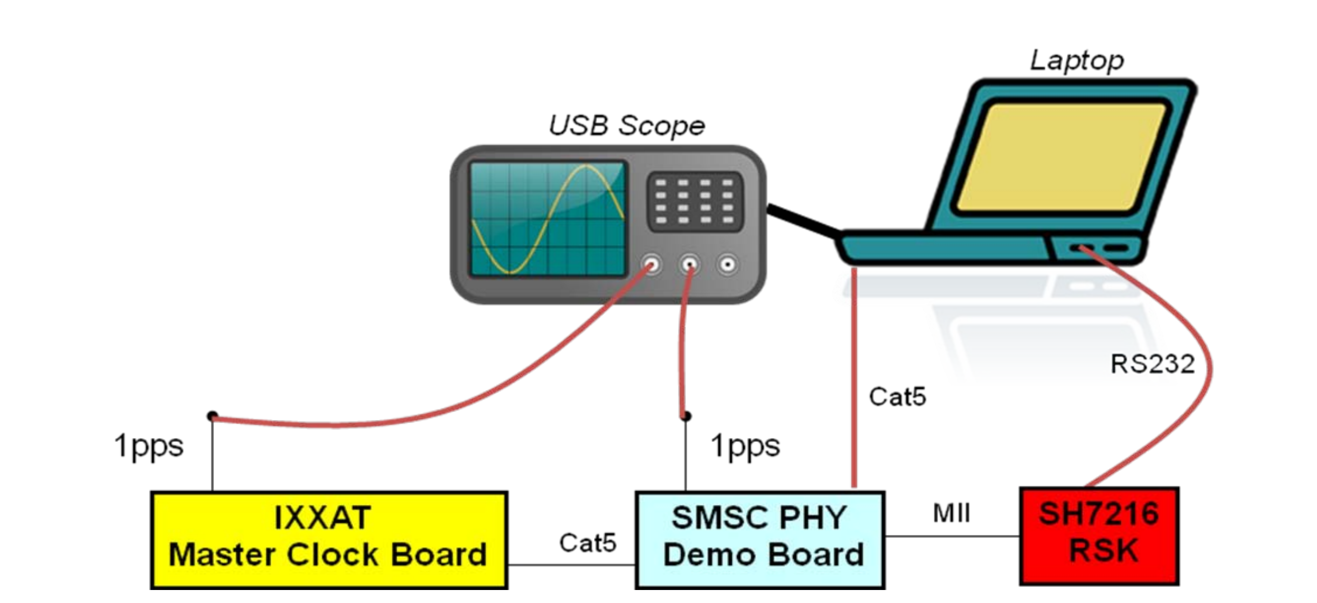

Figure 1: Diagram of IEEE1588 Demo

2.1 Scope connections

The scope was connected to the 1 PPS of both the IXXAT Master clock board and the 1PPS from SMSC Demo board, pin 1 of J5 .

The IXXAT test point is on X205 pin 1.

2.2 Ethernet Settings

The PC connection should be set for IP address of 192.168.1.11 and subnet mask of 255.255.255.0.

2.3 RS232 Settings

The serial port on the PC should be set to 115.2K baud, no parity, 1 stop bit, no handshaking.

3. IEEE1588 Overview

The Precision Time Protocol (PTP) is implemented in accordance with IEEE1588, “Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems” (see references for NIST website for further details and history). The basic premise of this protocol is, *not* to guarantee timely delivery of Ethernet packets as some might think, but rather to keep the clocks within a PTP domain in Sync so that they can operate in harmony so to speak. Some the many applications for this are:

- Motion control
- Telecommunications
- Measurement equipment
- Any industrial application requiring precise synchronized operation of many nodes.

An over-simplified example might be a robotic machine that must move product by “handing” it from one robot to another. Without precise timing, the motion profiles must operate at reduced speeds so that product is not “Dropped”. With precision clocks, the master control can set up motion profiles where the product can be moved at the fastest possible rate, since everyone knows within microseconds or even nanoseconds when the “hand-off” must a occur and run their motion profiles to meet this requirement.

In general, a node joining the PTP domain can synchronize to the Master clock in less than a minute. Once synchronized, operations across nodes will happen in perfect time synchronization. Synchronization accuracies will be dependant on the Clock and Timestamp implementation. Typical numbers are given in Table 1.

Timer Stamp Generation Point	Range of Accuracy
Within Application (PTP Stack level)	milliseconds
ISR level	1-100 Microseconds
Hardware assisted Timestamp	10's of nanoseconds

Table 1: Clock Accuracy Range

In this demo we provide Hardware assisted timestamp through the use of an Ethernet PHY containing a hardware time stamping unit containing a high accuracy, adjustable clock.

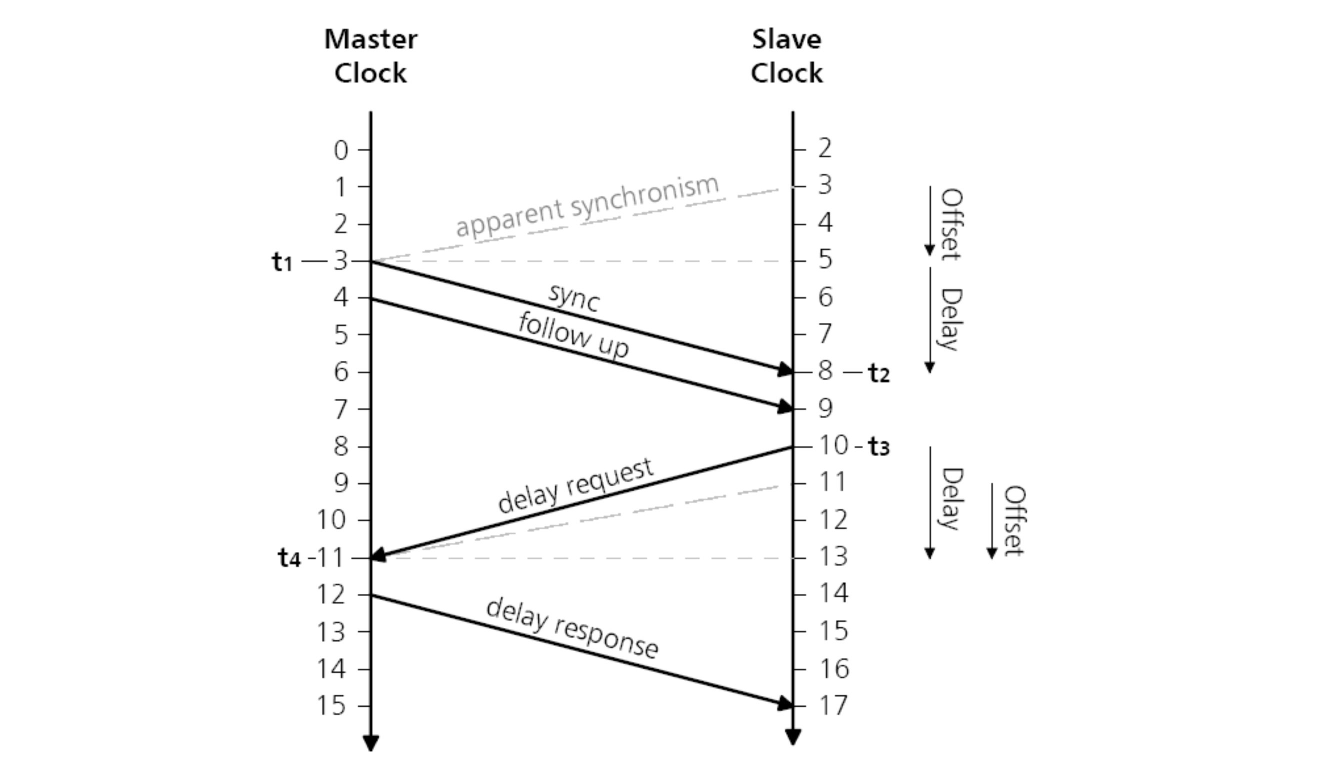

Figure 2: PTP Basic Sync Operation

3.1 Announce Message

The Announce message is sent by the master (IXXAT board) to all attached boards. This packet contains information about the master clock. It tells all nodes that a master has been established and the master clock is a crystal controlled oscillator. This information could be used by new nodes attached to the system to determine if the master should be replaced by a new master. For the purpose of this demo the master clock is accurate so there is no need for a new master to be established so any new nodes attached to the system will be slaves.

3.2 Join Message

When a new node is attached to the system it is neither in master or slave mode. It is said to be in the listening state. When the new node receives an announce message form an established master it will determine if it should become a slave or whether it should try to become a new master. In this demo the new node is the Renesas RSK board. Renesas RSK board will always receive the announce message and go into slave mode. Once a new node goes into slave mode it will send out a broadcast Join Message. The Join message is sent by a new node when it is attached to the system in response to the masters announce message. This informs the system that a new node has attached and has gone into slave mode.

3.3 Sync Message

Sync messages are sent by the IXXAT Demo Master at 4 times a second. This rate is defined by the System requirements and is fast enough to keep the clocks in sync to meet these requirements. The sync message contains a sequence number that is used to pair it with a follow up message. The master sends a follow-up message immediately after each sync message. The IEEE 1588 hardware on the master board records a copy of the master's clock at the time the sync message is sent. When a slave receives a sync message the IEEE 1588 hardware on the slave board will save a copy of the slaves clock when the sync message arrives.

3.4 Follow-up Message

The master sends a follow-up message after every sync message. The follow-up message contains a sequence number that pairs it with the previous sync message. The follow-up message also contains the hardware time stamp that was saved by the master when the sync message was sent. When the slave receives a follow-up message it compares the time stamp in the follow-up message with the time stamp it saved when the sync message was received. This comparison allows the slave to determine the differences between its clock and the masters clock ignoring any time it took for the messages to be sent over the network. With this information the slave can adjust its clock to be close to the masters clock. In order for the slave to precisely synchronize to the master it must determine the time delay of sending a message over the network. It then uses this information to adjust the clock on the hardware timestamp unit to go either faster or slower depending on the delay information. The PTP stack actually runs a PID control loop for calculating the required adjustment.

3.5 Delay Request Message

Once the slave has received a sync and a follow-up message and adjusted its clock to the master the next step is to determine the time delay of sending a message over the network. In order to start this process the slave sends a delay request message. The delay request message contains a sequence number that will allow it to me paired with a delay response message. When the slave sends out a delay request, the hardware on the slave board saves a copy of the slaves clock at the exact time the message was sent. When the delay request message is received by the master the hardware on the master's board saves a copy of the master's clock at the time the delay request was received.

3.6 Delay Response Message

When the master receives a Delay Request message it responds by sending a Delay Response message. The Delay Response message contains a sequence number that allows it to be paired with the Delay Request. The master recalls the time stamp that was saved by hardware when the delay request was received and places it in the Delay Response Message. When the slave receives a Delay Response Message it compares this time stamp with the time stamp that was saved by its hardware when it sent the Delay Request message. The difference between the two time stamps is the amount of time it takes to send a message over the network. The slave uses this information to further adjust its clock to match the masters clock.

4. Synchronization Analysis

The synchronization can be observed two ways. The first is the based on debug print messages from the ptp stack. The second is by observation of the physical 1 PPS signals coming from the two boards.

4.1 Analyzing using Debug prints

The PTP stack outputs various debug messages to the STDOUT (console) while it is running. One of these messages is the "drift analysis" message in the following form:

ofm (msrd/filt); 0,000000035; 0,000000035;pcr;11677400 ;

where ofm (Offset message) is the raw offset from Master, followed by the filtered offset, the phase change return value.

The pcr (phase change return) number is in picoseconds/second of adjustment required to keep the clocks in sync.

Offset values (ofm) are in nanoseconds and represent the absolute different in the clocks.

The results as displayed on the Terminal can be cut and paste into a file for importing into Excel. Figure 3 and 4 show the results of this analysis.

A sample output from the code is show in Figure 3. You can see that on power up, the clocks are clearly out of sync (large offset), but quickly come into synchronization (about 11 - 13 samples times). The Master report rate in this code is 250mS so this sync time is about 13*250mS = 3.25 seconds after stack started.

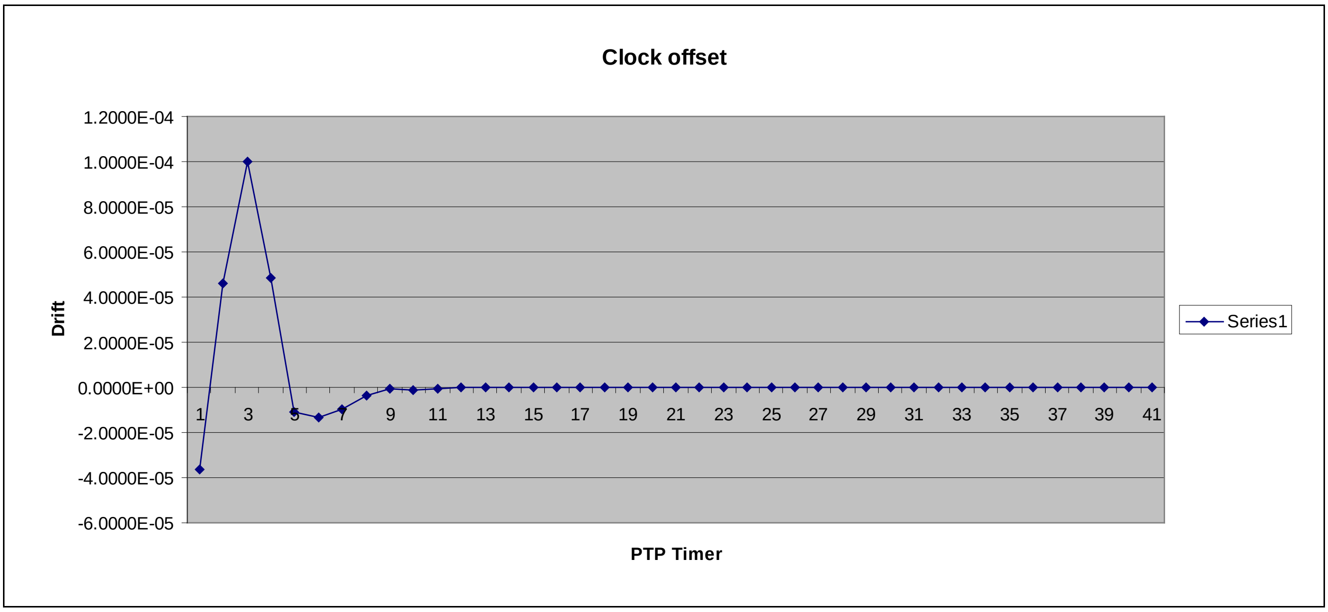

Figure 3: Clock Drift Chart

If we look a small section of the data as shown in Figure 4, we can see the clock is drifting about ±80nS worst case.

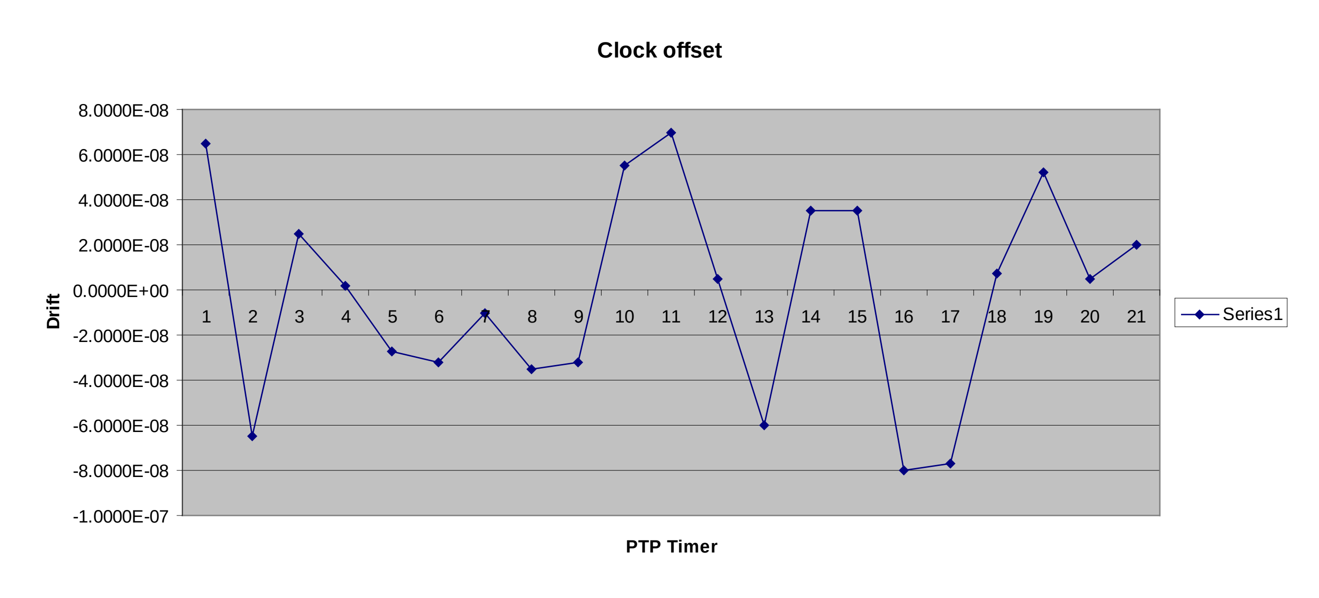

Figure 4: Clock drift, narrow sample

4.2 Viewing Clock Synchronization on the Oscilloscope

The 1 PPS signals are set to come out on the 1 second boundarires (i.e. no sub-second times involved). When the two test point are connected to the scope, and the trigger is set to the Master Clock (probe connected to the IXXAT board), the 1 PPS signal can be observed to be in sync with the Master 1 PPS and will "jitter" within the drift time of the accuracy maintained by the clock. See Figure 5.

NOTE: the latency is a function of the target.h file and must be analyzed and must be set for the specific configuration of the system to reduce it.

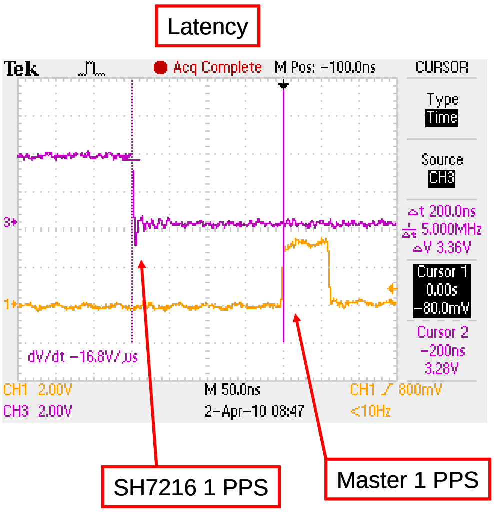

Figure 5: PPS Sync Observation

5. Limitations of Testing

5.1 This software port on this project has only been tested as a SLAVE ONLY device on the IEEE1588 Ethernet protocol. The PTP stack can act as Master, but a clock source would need to be implemented (RTC, GPS, etc.) and the engineer is referred to the IXXAT manual for details.

5.2 This software only runs a limited application that synchronizes the Clocks in the MASTER and SLAVE. No other applications are included.

5.3 Module Sized Estimates. Note, that the size may vary based on the features enabled in the OS, the TCP/IP stack and the PTP stack. The Micrium OS and TCP/IP stack were built with larger Ethernet buffers and Memory pool and could possibly be trimmed in size for control type application where there is not a lot of large packets being transferred (no streaming video, etc.)

PTP Stack - ~60K bytes of code

OS + TCP/IP - ~125k bytes of code

Memory Pool for Network – 25k Bytes of RAM

Total Linker Sizes:

PROGRAM: ~200k bytes

ROMDATA: ~23k bytes

RAMDATA: ~100kBytes

6. Building Your own application

The modules included in this application were for analysis only. If you are ready to build you own IEEE1588 for use in your product, you need to contact the following companies for licensing:

PTP Stack – IXXAT (see link in References section)

uCOS-II and TCP/IP stack Middleware – Micrium (see link in References section)

7. References

RSK+SH7216 Quick Start Guide

RSK+SH7216 Schematics

RSK+SH7216

SHC Compiler Package V9.01 User's Manual, rej10J1571-0101

IXXAT 1588-2008 Protocol Software Manual, 4.02.0314.20000, Version 1.4

SMSC LAN9313 Data Sheet

IXXAT Website: www.ixxat.com

Micrium Website: www.micrium.com

NIST: http://ieee1588.nist.gov/

8. Glossary

GPIO – General Purpose Input/Output

IEEE 1588 – IEEE standard for PTP

PTP – Precision Time Protocol

RSK – Renesas Starter Kit

Website and Support

Renesas Electronics Website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Aug 16.11	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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