SH7216 Group

MTU2 Positive/Negative Three-Phase PWM Output Function (Reset-Synchronized PWM Mode)

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Introduction

This application note describes example settings for three-phase PWM waveform output using the reset-synchronized PWM mode of the SH7216's multi-function timer pulse unit 2 (MTU2).

Target Device

SH7216

Contents

1. Introduction

1.1 Specifications

This application note presents an example in which three-phase (positive and negative) PWM waveforms are output using channels 3 and 4 of multi-function timer pulse unit 2 (MTU2) in reset-synchronized PWM mode and the I/O port set to general output. Figure 1 illustrates the configuration.

- Channels 3 and 4 of MTU2 are set to reset-synchronized PWM mode.
- The positive PWM output pins are TIOC3B/PE9, TIOC4A/PE12, and TIOC4B/PE13. Corresponding to the positive output pins are the negative output pins TIOC3D/PE11, TIOC4C/PE14, and TIOC4D/PE15.
- The PWM output level is low-active.
- The PWM carrier cycle is set to 400 µs.
- The three-phase PWM duty is updated during interrupt handling each PWM carrier cycle. The register buffer function is used to update the PWM duty.
- The pins used for PWM output switch to general output when the PWM duty is 0% or 100%. Pin function switching is performed in the interrupt handling for MTU2 channel 0 (normal mode). (For details, see 2.2.2 (2) Setting the PWM Duty to 0% and 100%.)
- A toggle waveform synchronized with the PWM carrier cycle is output from pin TIOC3A.

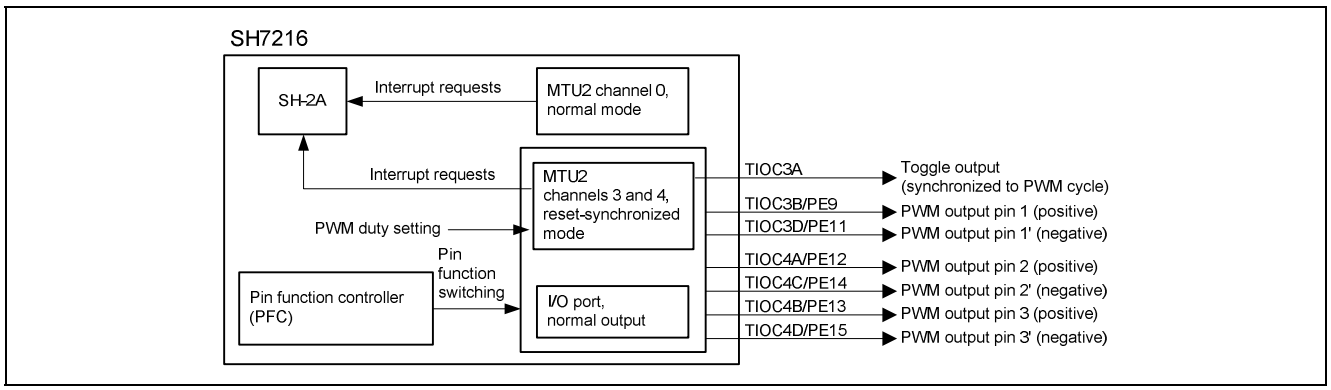

Figure 1 Three-Phase PWM Output (Reset-Synchronized PWM Mode)

1.2 Functions Used

Multi-function timer pulse unit 2 (MTU2) channels 3 and 4

1.3 Applicable Conditions

MCU	SH7216 [R5F72167]	
Operating frequencies	Internal clock	: Iϕ = 200 MHz
	bus clock	: Bϕ = 50 MHz
	Peripheral clock	: Pϕ = 25 MHz
	MTU2S clock	: Mϕ = 100 MHz
	AD clock	: Aϕ = 50 MHz
MCU operating mode	Single-chip mode	
Integrated development environment	Renesas Electronics High-performance Embedded Workshop, Ver. 4.07.00.007	
C compiler	Renesas Electronics SuperH RISC Engine Family C/C++ Compiler Package, Ver. 9.03, Release 02	
Compile options	High-performance Embedded Workshop default settings (-cpu = sh2afpu -include = "$(WORKSPDIR)\inc" -object = "$(CONFIGDIR)\$(FILELEAF).obj" -debug -gbr = auto -chgincpath - errorpath -global_volatile = 0 -opt_range = all -infinite_loop = 0 - del_vacant_loop = 0 -struct_alloc = 1 - nologo)	

2. Description of Application Example

This application note describes using the reset-synchronized PWM mode of multi-function timer pulse unit 2 (MTU2).

2.1 Overview of Functions Used

2.1.1 Multi-Function Timer Pulse Unit 2 (MTU2)

Multi-function timer pulse unit 2 (MTU2) comprises six 16-bit timer channels. Each channel has a variety of settings, including a compare-match function and input-capture function. By setting channels 3 and 4 to complementary PWM mode or reset-synchronized mode, six-line PWM output control is possible.

For details of MTU2, see the Multi-Function Timer Pulse Unit 2 (MTU2) section in the *SH7216 Group Hardware Manual* (REJ09B0543).

Table 1 shows an overview of multi-function timer pulse unit 2 (MTU2). Figure 2 is a block diagram of MTU2.

Table 1 Overview of Multi-Function Timer Pulse Unit 2 (MTU2)

Item	Description
Number of channels	16-bit timer × 6 channels (channels 0 to 5)
Counter clocks	8 counter input clocks selectable per channel (4 clocks for channel 5)
Operation of channels 0 to 4	• Compare-match based waveform output, input-capture function, counter clear operation, simultaneous writing to multiple timer counters (TCNT), compare-match/input-capture based simultaneous clearing • Register input/output synchronized with counter, max. 12-phase PWM output by combining synchronous operation modes
A/D converter triggers	• Ability to generate conversion start trigger for A/D converter • In complementary PWM mode, ability to skip counter peak/trough interrupts or A/D converter conversion start triggers
Buffer operation	Ability to specify register buffer operation for channels 0, 3, and 4
Operating modes	• Ability to specify PWM mode for channels 0 to 4 • Ability to specify phase counting mode independently for channels 1 and 2 • Ability to specify a total of 6 lines of PWM waveform output, three-phase positive and negative output using complementary PWM mode and reset-synchronized PWM mode, by using linked operation of channels 3 and 4
Interrupt requests	28 interrupt sources (compare-match, input-capture interrupt, etc.)
Other	• Cascade connection operation • High-speed access using internal 16-bit bus • Support for automatic transfer of register data • Ability to specify module standby mode • Support for dead time compensation counter function using channel 5

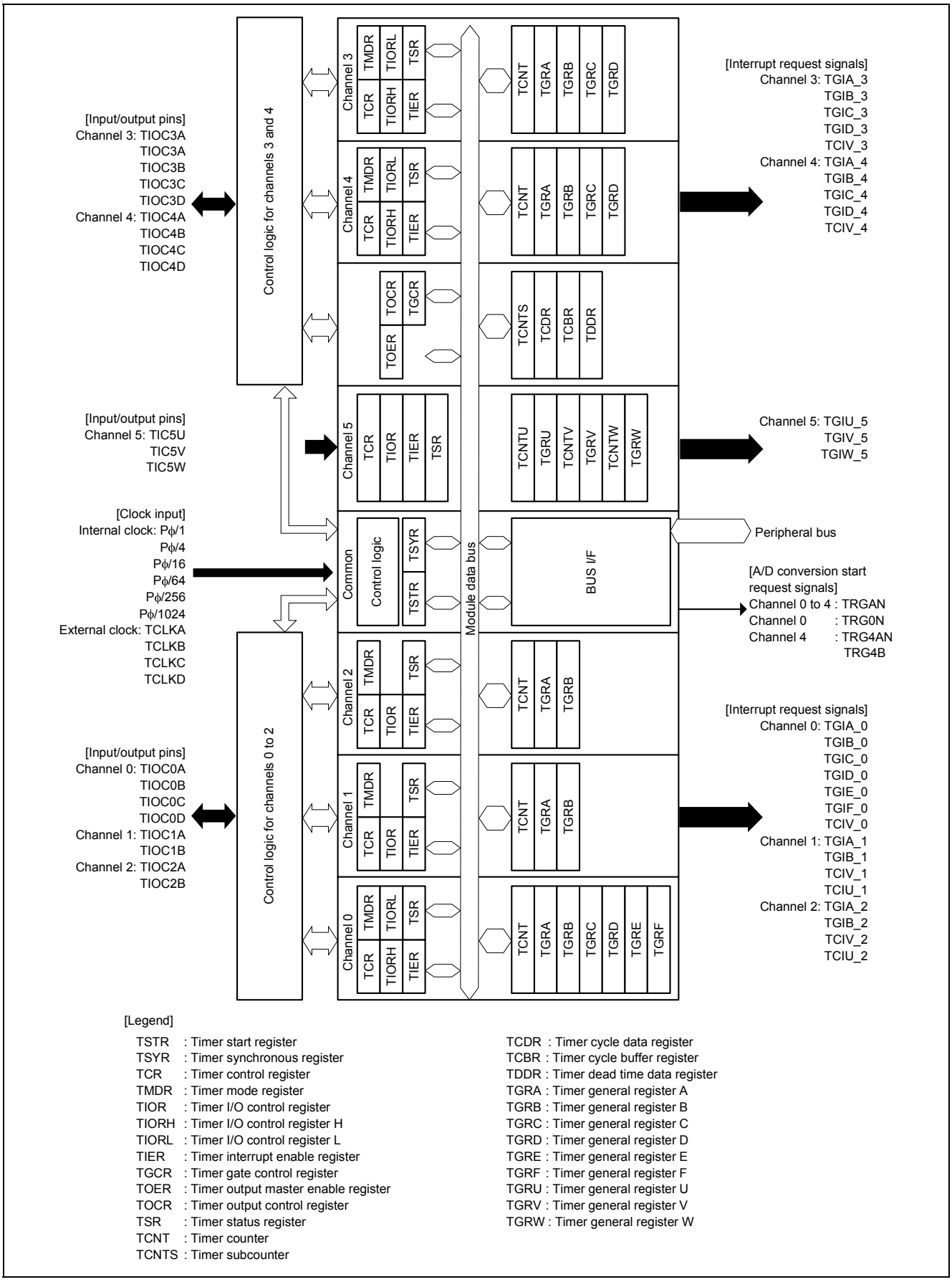

Figure 2 Block Diagram of MTU2

2.1.2 Reset-Synchronized PWM Mode

In reset-synchronized PWM mode, three-phase output of PWM waveforms (positive and negative) that share a common wave transition point is obtained by combining channels 3 and 4.

In reset-synchronized PWM mode, pins TIOC3B, TIOC4A, and TIOC4B are set as positive PWM outputs. Corresponding to the positive outputs are negative PWM outputs on pins TIOC3D, TIOC4C, and TIOC4D. Timer counter 3 (TCNT_3) functions as an up-counter. When a compare-match occurs between TCNT_3 and the TGRA_3 (period) register, the counter is cleared and begins to count up from H'0000 again. The outputs of the PWM output pins toggle at each compare-match with the TGRB_3, TGRA_4, and TGRB_4 registers, respectively, and each time the counter is cleared.

Figure 3 shows an example of reset-synchronized PWM mode operation. In this operation example, both the positive and negative PWM outputs are high-level active.

Table 2 lists the PWM output pins used in reset-synchronized PWM mode. Table 3 lists the register functions.

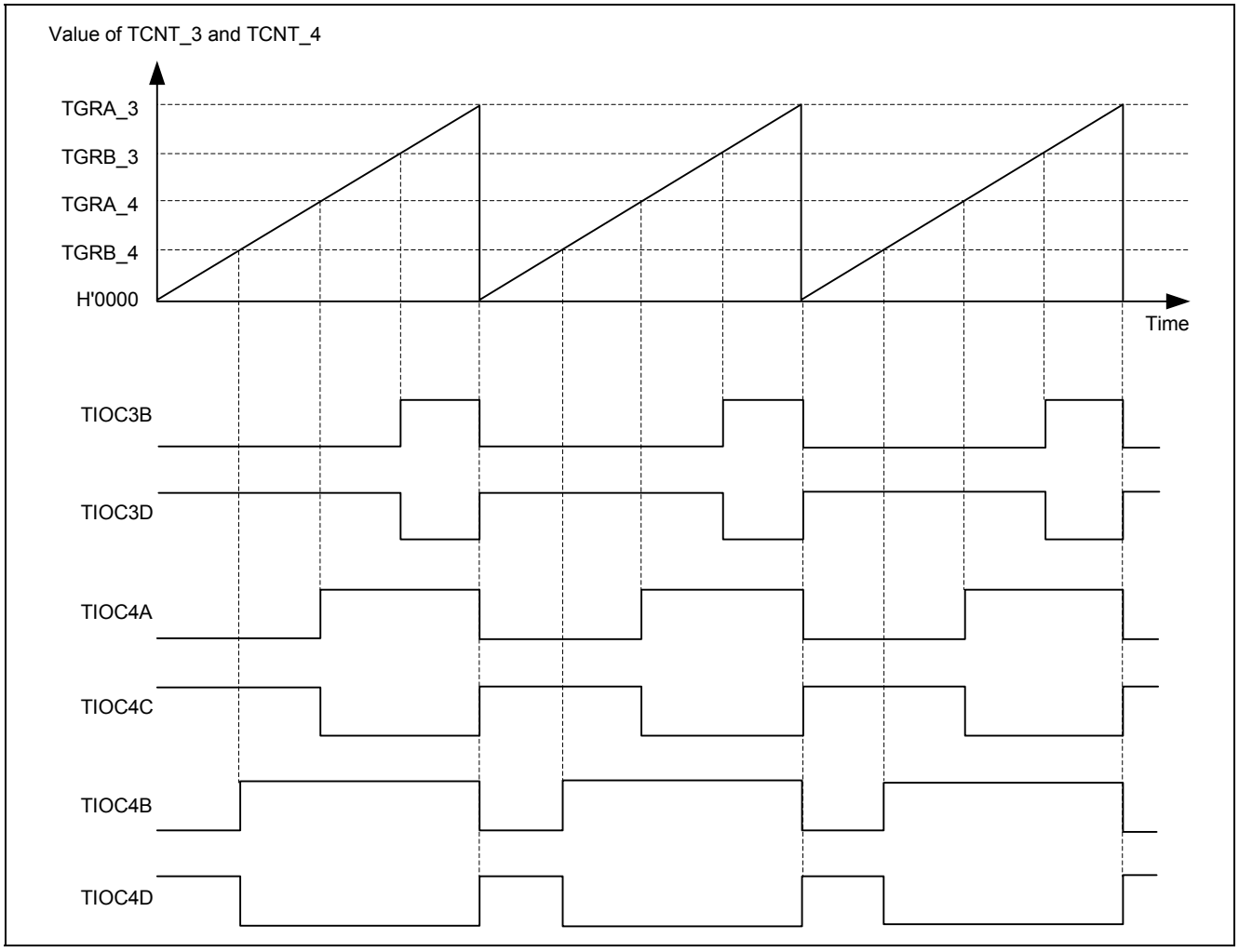

Figure 3 Operation Example of Reset-Synchronized PWM Mode (OLSN = 1 and OLSP = 1 in TOCR)

Table 2 Output Pins in Reset-Synchronized PWM Mode

Channel	Output pin	Description
Channel 3	TIOC3A	Toggle output synchronized with PWM period (Can also be used as an I/O port if toggle output is not used.)
	TIOC3B	PWM output pin 1
	TIOC3D	PWM output pin 1' (PWM output 1 negative waveform)
Channel 4	TIOC4A	PWM output pin 2
	TIOC4C	PWM output pin 2' (PWM output 2 negative waveform)
	TIOC4B	PWM output pin 3
	TIOC4D	PWM output pin 3' (PWM output 3 negative waveform)

Table 3 Registers Used in Reset-Synchronized PWM Mode

Register	Description
TCNT_3	Channel 3 timer counter Initial setting is H'0000.
TCNT_4	Channel 4 timer counter Initial setting is H'0000.
TGRA_3	TCNT_3 count period setting (PWM period) Set value in buffer register to update the PWM period.
TGRB_3	Compare-match register Sets the PWM wave transition point (duty) for output on pins TIOC3B and TIOC3D. Set value in buffer register to update duty.
TGRA_4	Compare-match register Sets the PWM wave transition point (duty) for output on pins TIOC4A and TIOC4C. Set value in buffer register to update duty.
TGRB_4	Compare-match register Sets the PWM wave transition point (duty) for output on pins TIOC4B and TIOC4D. Set value in buffer register to update duty.
TGRC_3	TGRA_3 buffer register (When using buffer function)
TGRD_3	TGRB_3 buffer register (When using buffer function)
TGRC_4	TGRA_4 buffer register (When using buffer function)
TGRD_4	TGRB_4 buffer register (When using buffer function)

2.2 Operation of Reference Program

2.2.1 Reference Program Operation Settings

The program described in this application note sets channel 3 of multi-function timer pulse unit 2 (MTU2) to reset-synchronized PWM mode and outputs a three-phase PWM waveform. For PWM output with a PWM duty of 0% or 100%, the PWM output pins are switched to general output in the handling of the MTU2 channel 0 (normal mode) compare-match interrupt. (For details, see 2.2.2 (2) Setting the PWM Duty to 0% and 100%.)

Table 4 lists the setting conditions for reset-synchronized PWM mode, table 5 lists the setting conditions for general output, and table 6 lists the setting conditions for MTU2 channel 0.

Table 4 Settings for Reset-Synchronized PWM Mode Operation

Item	Description
Channels used	Channels 3 and 4
Operating mode	Reset-synchronized PWM mode
Pin functions	TIOC3A pin: Toggle output synchronized with PWM period TIOC3B pin: PWM output 1 (positive waveform) TIOC3D pin: PWM output 1' (PWM output 1 negative waveform) TIOC4A pin: PWM output 2 (positive waveform) TIOC4C pin: PWM output 2' (PWM output 2 negative waveform) TIOC4B pin: PWM output 3 (positive waveform) TIOC4D pin: PWM output 3' (PWM output 3 negative waveform)
Active level	Positive output: Active-low output Negative output: Active-low output
Counter clock	6.25 MHz (Pϕ clock divided by 4)
PWM carrier cycle	400 μs (carrier frequency: 2.5 kHz)
PWM duty	The phase of the waveforms output from PWM outputs 1, 2, and 3 are each shifted by 2π/3 relative to the one preceding, and the initial PWM duty values are 0.04%, 66.68%, and 66.68%, respectively (increase, decrease, and increase, respectively). During the handling of each TGRA_3 compare-match interrupt, the PWM duty setting is updated (incremented or decremented) in the buffer register. The function of the PWM output pins switches to I/O port for output when the duty is 0% or 100 %.
Interrupt	TGRA_3 compare-match interrupt A TGRA_3 interrupt is generated once each PWM carrier cycle.

Table 5 General Output Settings

Item	Description
Port used	Port E
Pin functions	PE9 pin: General output corresponding to TIOC3B pin (PWM output 1) PE11 pin: General output corresponding to TIOC3D pin (PWM output 1') PE12 pin: General output corresponding to TIOC4A pin (PWM output 2) PE14 pin: General output corresponding to TIOC4C pin (PWM output 2') PE13 pin: General output corresponding to TIOC4B pin (PWM output 3) PE15 pin: General output corresponding to TIOC4D pin (PWM output 3')
PWM duty and output level	Low output for PWM duty 0%, high output for 100%.

Table 6 MTU2 Channel 0 (Normal Mode) Settings

Item	Description
Channel used	Channel 0
Operating mode	Normal mode
Counter clock	6.25 MHz (Pϕ clock divided by 4)
Clearing source	Compare-match with TGRA_0
Period	400 μs (frequency: 2.5 kHz)
Interrupt	TGRA_0 compare-match interrupt Used to switch the pin function for positive duty 100 % PWM output. TGRB_0 compare-match interrupt Used to switch the pin function for positive duty 0 % PWM output.

2.2.2 Description of Reference Program Operation

Figure 4 illustrates the basic operation of the reference program. Channel 3 of multi-function timer pulse unit 2 (MTU2) is set to reset-synchronized PWM mode. The registers for specifying the period and PWM duty are set by means of buffer operation. Buffer operation in reset-synchronized PWM mode involves setting the BFA and BFB bits in the TMDR_3 register. Setting the BFA and BFB bits in TMDR_3 to 1 causes TGRC_3 to function as the buffer register for TGRA_3 and TGRD_3 to function as the buffer register for TGRB_3, respectively, for channel 3. At the same time, TGRC_4 functions as the buffer register for TGRA_4, and TGRD_4 as the buffer register for TGRB_4, for channel 4.

The three-phase PWM duty is updated in the handling of the TGRA_3 compare-match interrupt, which is generated each PWM carrier cycle. The PWM duty update values are set in the buffer registers (TGRD_3, TGRC_4, and TGRD_4). The buffer register values are transferred to the compare registers when a TGRA_3 compare-match occurs once each period. Using buffer operation makes it possible to update the registers at a user-defined compare-match timing.

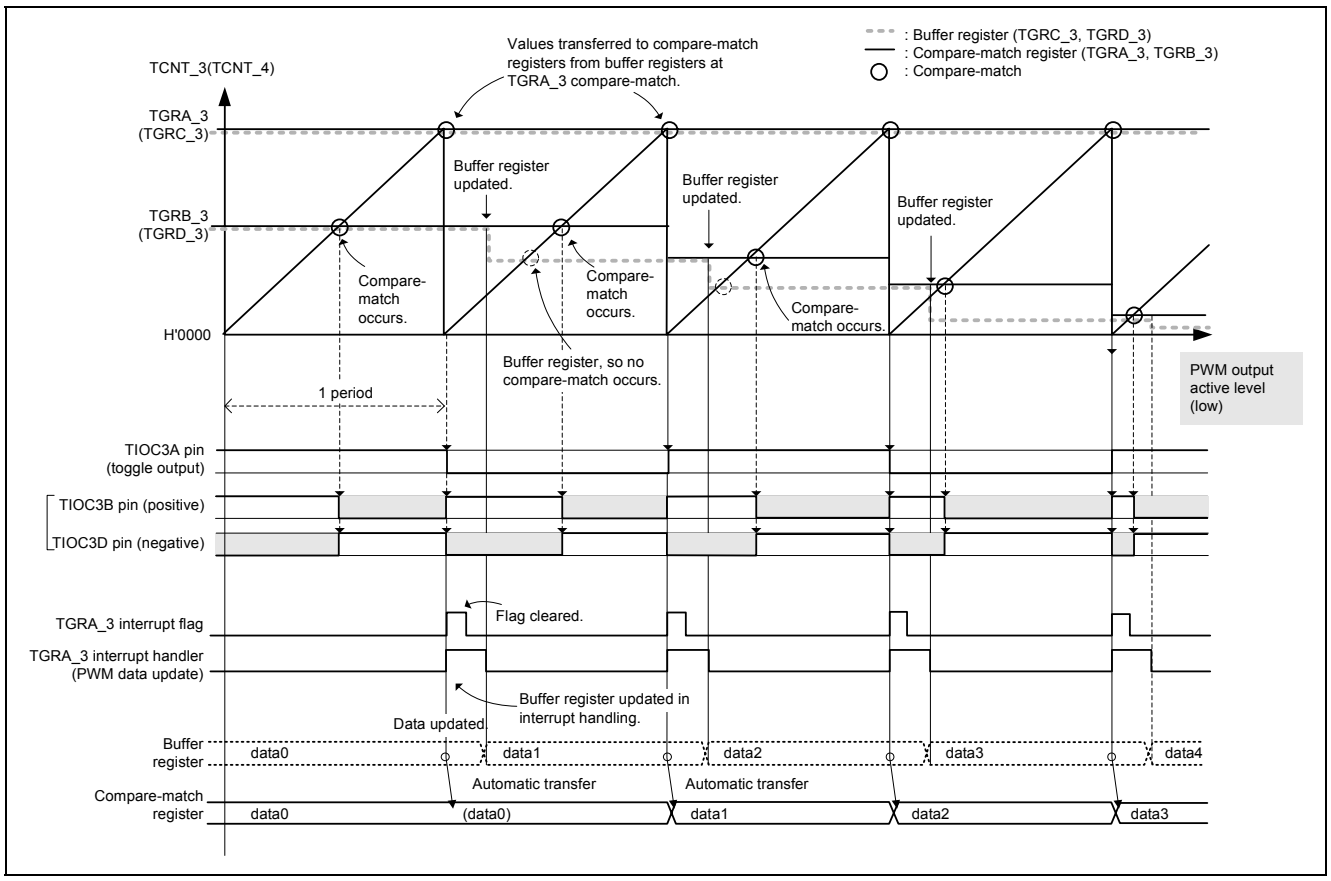

Figure 4 Reset-Synchronized PWM Mode Operation (Buffer Operation)

(1) Period Register Setting Values

When counter clearing is set to occur at a compare-match with the TGRA_3 period register, the TCNT timer counter is cleared at the last state in which the TGR value matches (the timing when the count value matched by TCNT is updated). Therefore, the setting value of the period register (TGRA_3 register) can be calculated with the following equation.

TGRA_3 register setting value = (PWM period duration / single count duration) – 1

- PWM period duration: The desired PWM carrier cycle duration
- Single count duration: The duration of one count of timer counter TCNT

For a PWM carrier cycle is 400 [µs], set the period register (TGRA_3 register) to the following value.

TGRA_3 register setting value = 400 [µs] / 160 [ns] – 1
= D'2499

- Timer counter TCNT count clock: 6.25 MHz (Pϕ/4: Pϕ is the on-chip peripheral clock.)
- Single count duration: 160 [ns]

(2) Setting the PWM Duty to 0% and 100%

Figure 5 shows the PWM output waveform in reset-synchronized PWM mode when the setting value of PWM duty register TGRB_3 is H'0000 or the same value as that set in period register TGRA_3.

When the setting value of duty register TGRB_3 is H'0000 in reset-synchronized PWM mode, the PWM output is a pulse waveform lasting for one count of timer counter TCNT. Also, when the setting value of duty register TGRB_3 is the same or greater as that of period register TGRA_3, the PWM output toggles between high- and low-level each PWM period.

It is not possible to set the output to PWM duty 0% or 100%, in which the PWM output level is fixed high- or low-level, by changing the PWM duty register setting value. To obtain high- or low-level fixed PWM output, it is necessary to change the pin function setting from MTU2 output (PWM output) to port output by using the pin function controller (PFC). In addition, the timing of pin function switching is controlled by the MTU2 channel 0 (normal mode) compare-match interrupt. Figure 6 shows the operation timing for duty 0% PWM output and figure 7 for duty 100% PWM output.

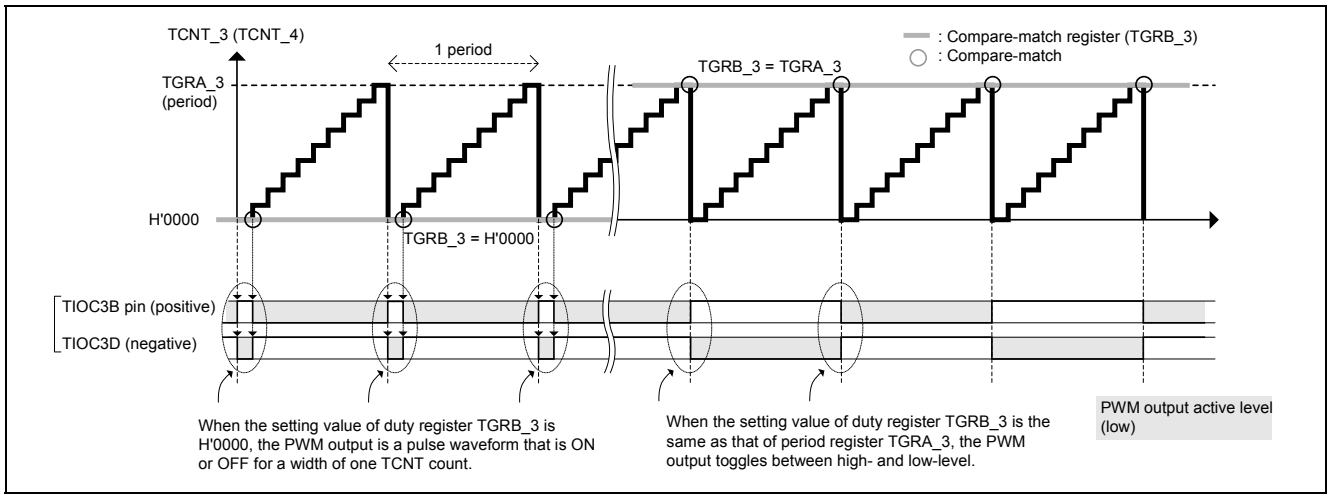

Figure 5 Duty Register Setting Values and PWM Output Waveform

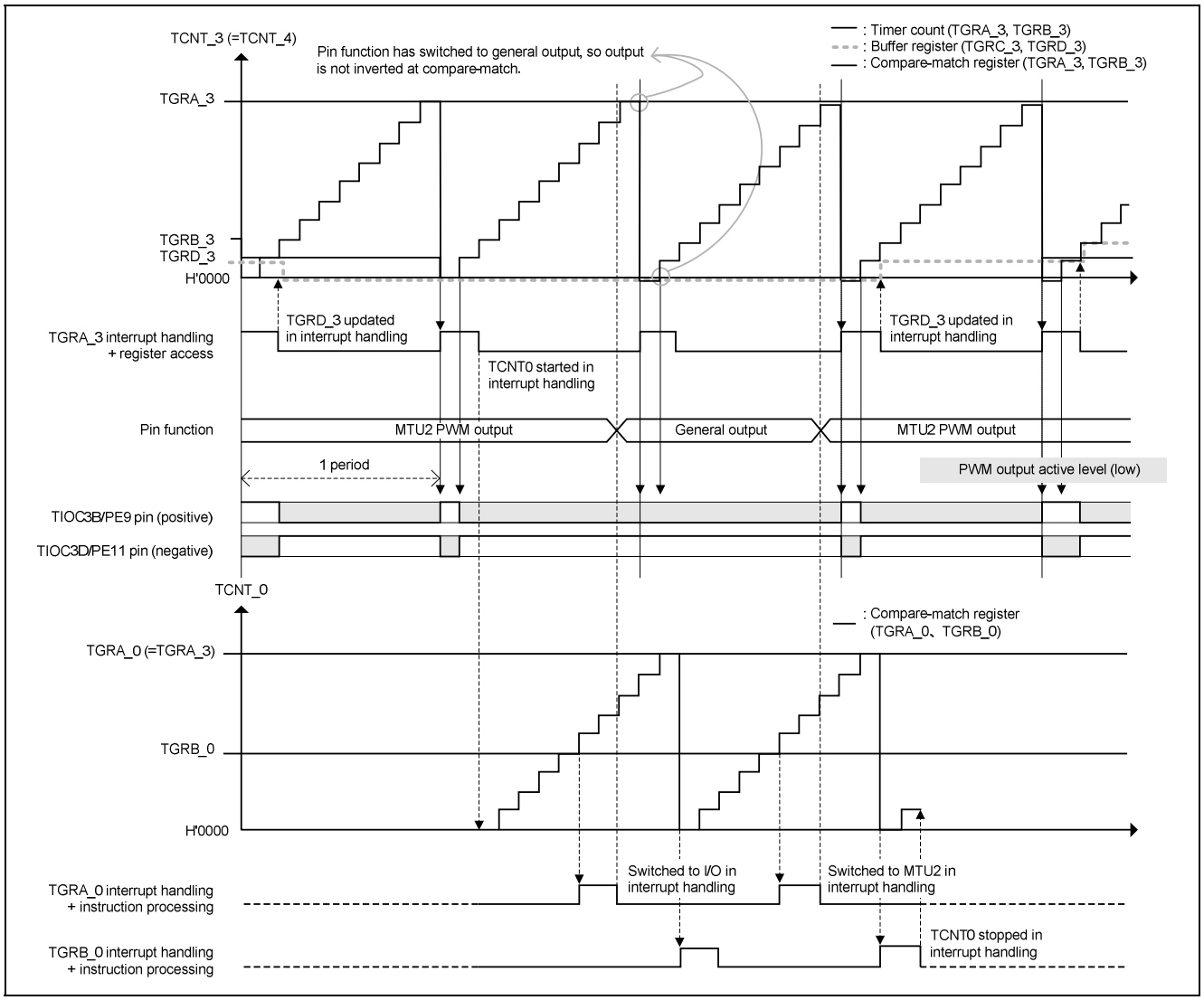

Figure 6 Operation Timing For Duty 0% PWM Output

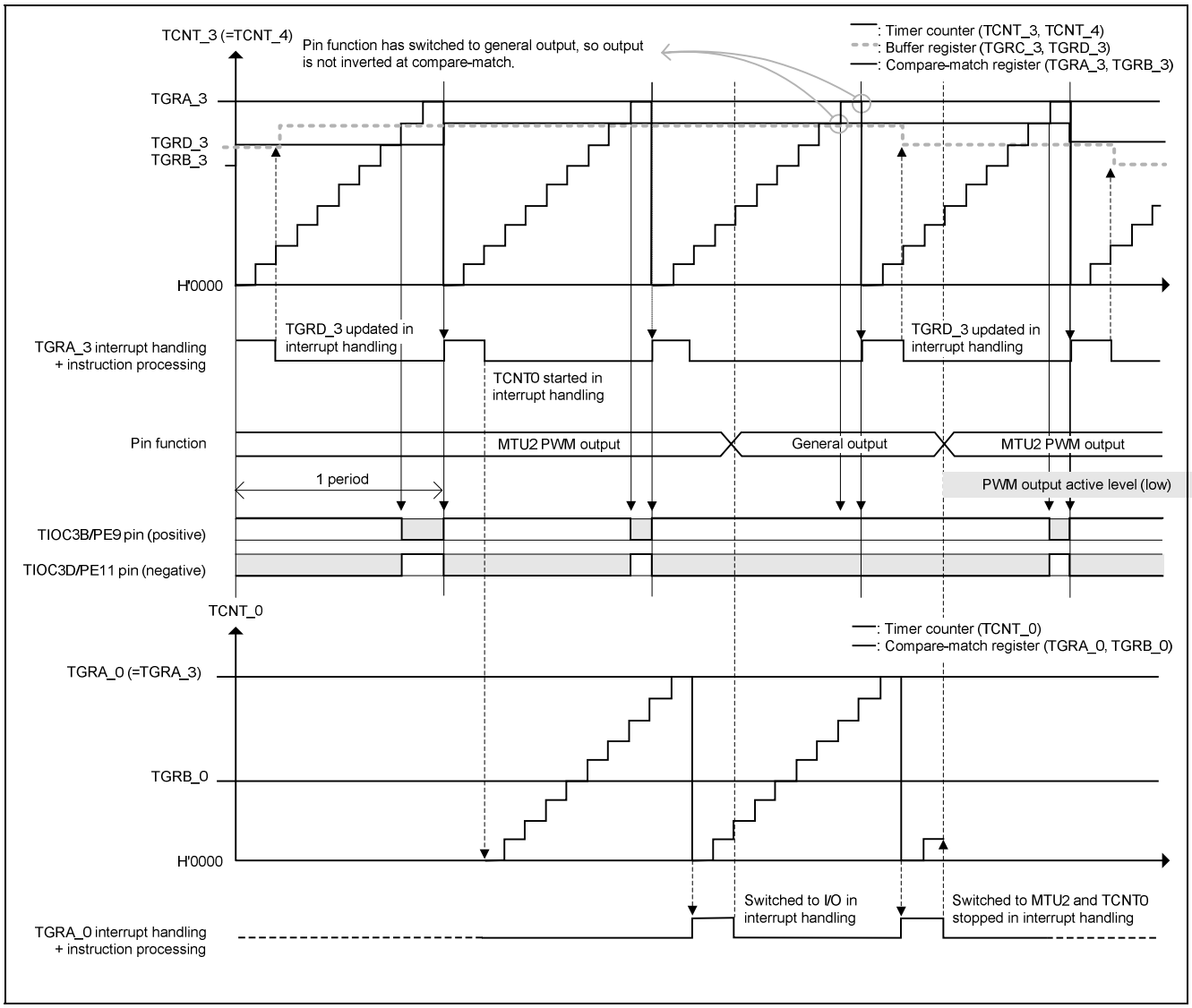

Figure 7 Operation Timing For Duty 100% PWM Output

2.3 Reference Program Configuration

2.3.1 Functions

Table 7 lists the principal functions used by the reference program.

Table 7 Description of Functions

Label	Description
main()	Main function Calls the initial settings functions for the various modules. Starts MTU2 channel 3 (reset-synchronized mode) timer count operation.
stbcr_init()	Standby setting Releases MTU2 from module standby.
mtu2_ch3_ch_4_init()	MTU2 (channels 3 and 4) initial settings Sets MTU2 channels 3 and 4 to reset-synchronized mode.
mtu2_ch0_init()	MTU2 (channel 0) initial settings Set MTU2 channel 0 to normal mode.
pfc_init()	PFC initial settings Sets MTU2-related pins to timer pin function.
int_mtu2_tgia3()	MTU2 channel 3 TGRA_3 compare-match interrupt handler Updates PWM duty setting values. Starts MTU2 channel 0 timer counter operation.
int_mtu2_tgia0()	MTU2 channel 3 TGRA_0 compare-match interrupt handler Calls a function for positive duty 100% PWM output. Also stops of MTU2 channel 0 timer counter operation.
int_mtu2_tgib0()	MTU2 channel 3 TGRB_0 compare-match interrupt handler Calls a function for positive duty 0% PWM output.
port_output_data_duty 0()	General output data settings (PWM duty 0%) Sets general output data for positive duty 0% PWM output.
port_output_data_duty 100()	General output data settings (PWM duty 100 %) Sets general output data for positive duty 100% PWM output.
pfc_port_output()	Pin switching (I/O port) Switches pin functions to I/O port for duty 0% and 100 % PWM output.
pfc_mtu2_output()	Pin switching (MTU2) Switches pin functions to MTU2 for other than duty 0% and 100 % PWM output.

2.3.2 Variables

Table 8 lists the variables used in the reference program.

Table 8 Description of Variable

Variable Name	Description	Functions Used
pul_ pwm_duty[]	PWM duty setting value. Each element corresponds to a pin, as indicated below. [0] PWM1 output (pins TIOC3B and TIOC3D) (Stored in TGRD_3 register.) [1] PWM2 output (pins TIOC4A and TIOC4C (Stored in TGRC_4 register.) [2] PWM3 output (pins TIOC4B and TIOC4D) (Stored in TGRD_4 register.)	mtu2_init() int_mtu2_tgia3() int_mtu2
duty_select[]	Flag that determines if the PWM duty setting value is incremented, decremented, or maintained (duty 0% or 100 % PWM output) at a TGRA_3 compare-match interrupt. Each element corresponds to a pin, as indicated below. [0] PWM1 output and the PE9 and PE11 general output pins corresponding to it. [1] PWM2 output and the PE12 and PE14 general output pins corresponding to it. [2] PWM3 output and the PE13 and PE15 general output pins corresponding to it.	int_mtu2_tgia3()

2.4 Function Setting Procedures

The processing sequences of the reference program are shown below.

2.4.1 Main Function

Figure 8 shows the processing sequence of the main function.

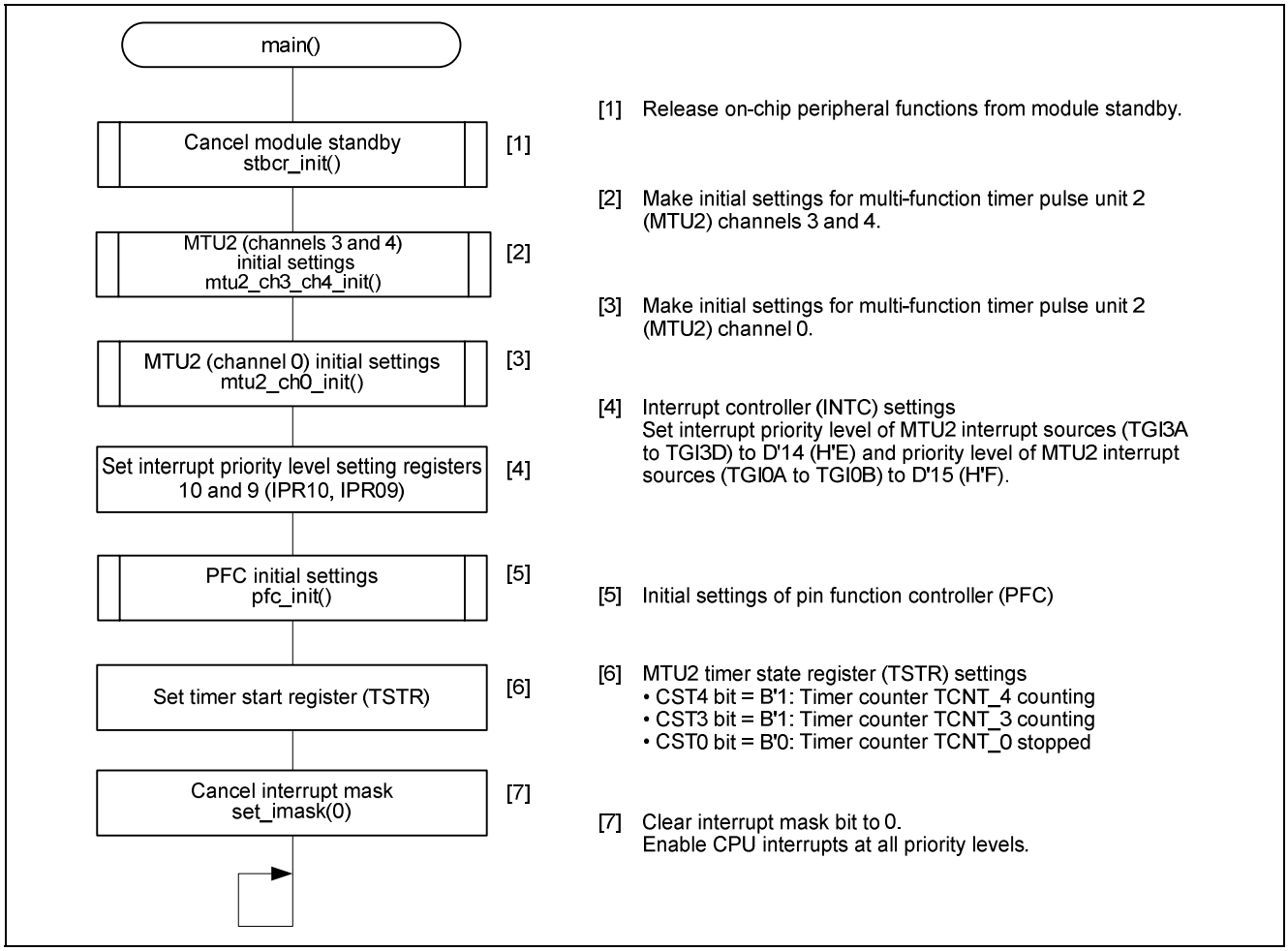

Figure 8 Processing of Main Function

2.4.2 Canceling Module Standby

Figure 9 shows the processing sequence for canceling module standby.

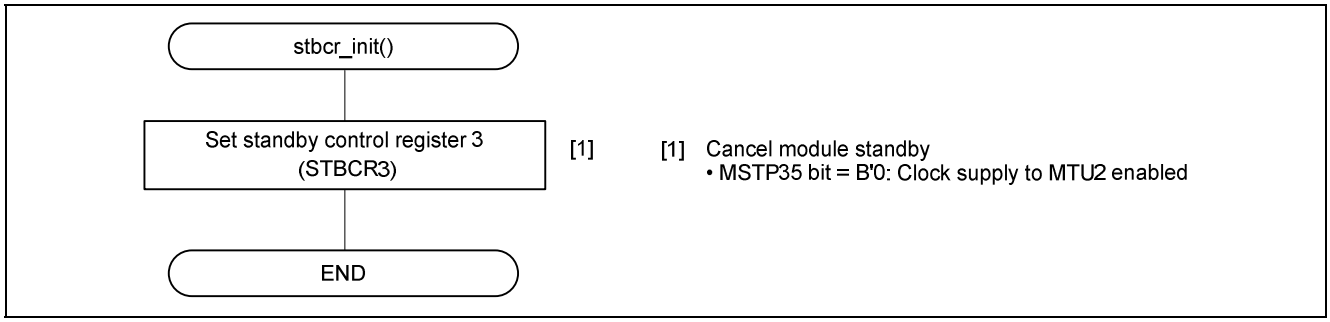

Figure 9 Canceling Module Standby

2.4.3 Multi-Function Timer Pulse Unit 2 (MTU2) Settings

Figure 10 shows the processing sequence for making initial settings for channels 3 and 4 of multi-function timer pulse unit 2 (MTU2), and figure 11 shows the processing sequence for making initial settings for channel 0. Channels 3 and 4 are set to reset-synchronized PWM mode and channel 0 to normal mode.

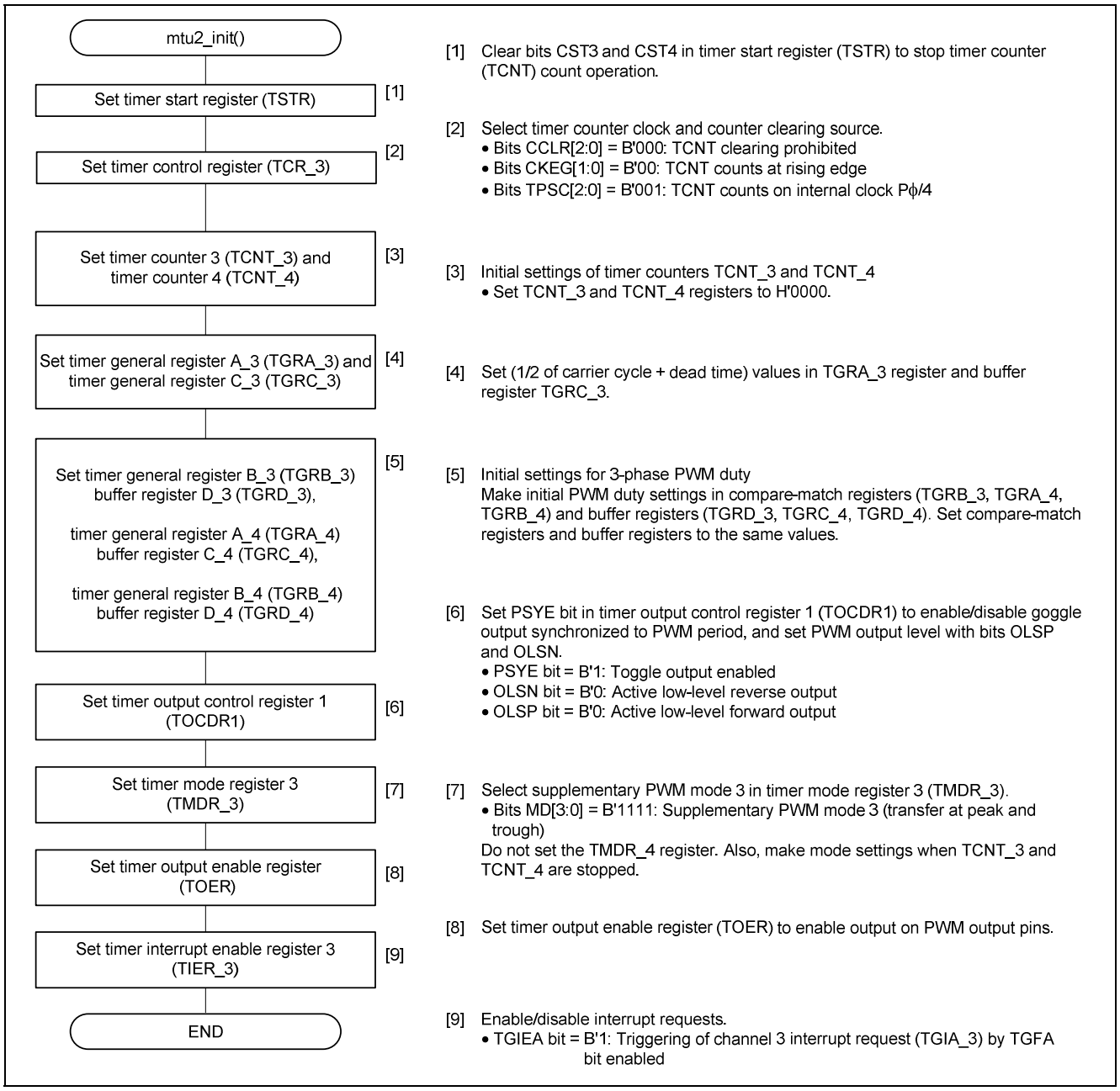

Figure 10 Initial Settings for Channels 3 and 4 of Multi-Function Timer Pulse Unit 2 (MTU2)

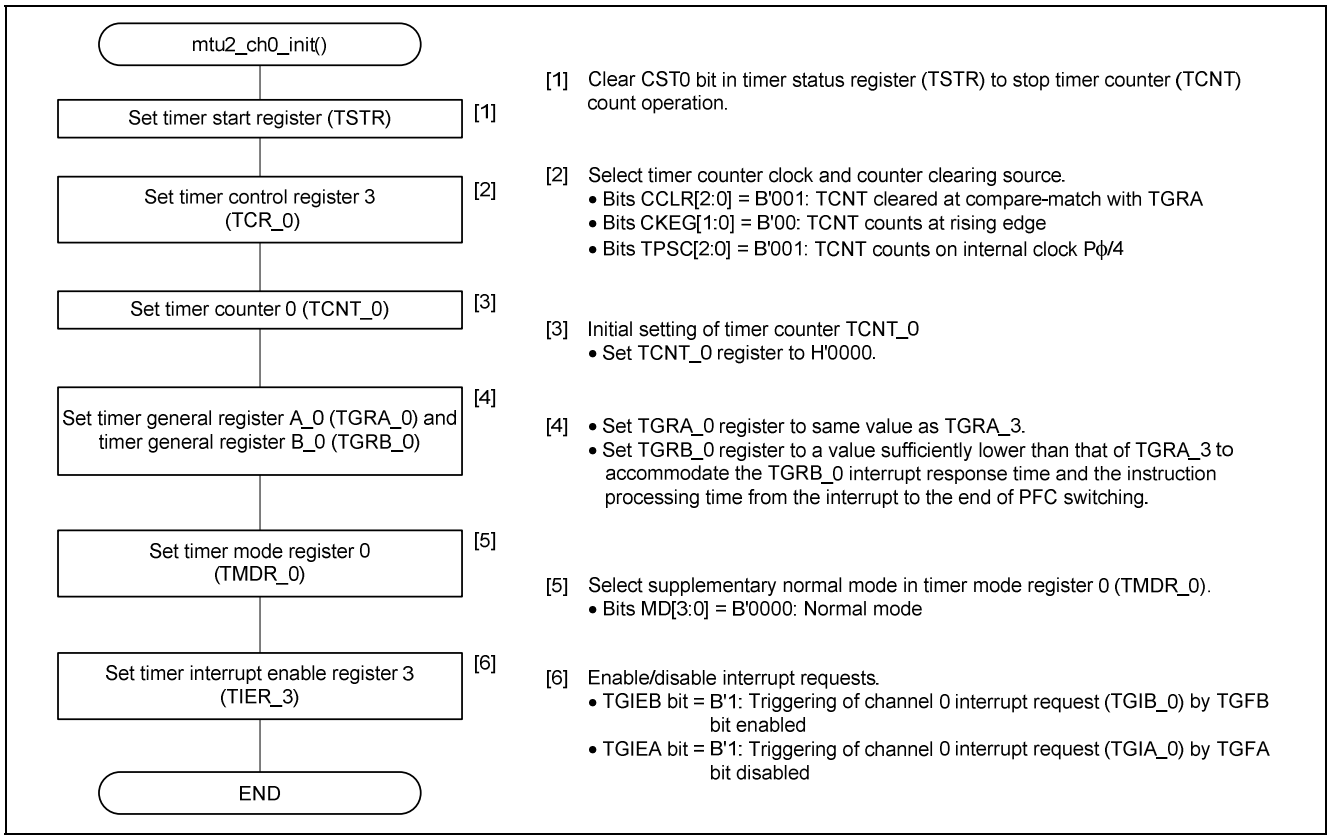

Figure 11 Initial Settings for Channel 0 of Multi-Function Timer Pulse Unit 2 (MTU2)

2.4.4 Pin Function Controller (PFC) Settings

Figure 12 shows the processing sequence for making pin function controller (PFC) settings.

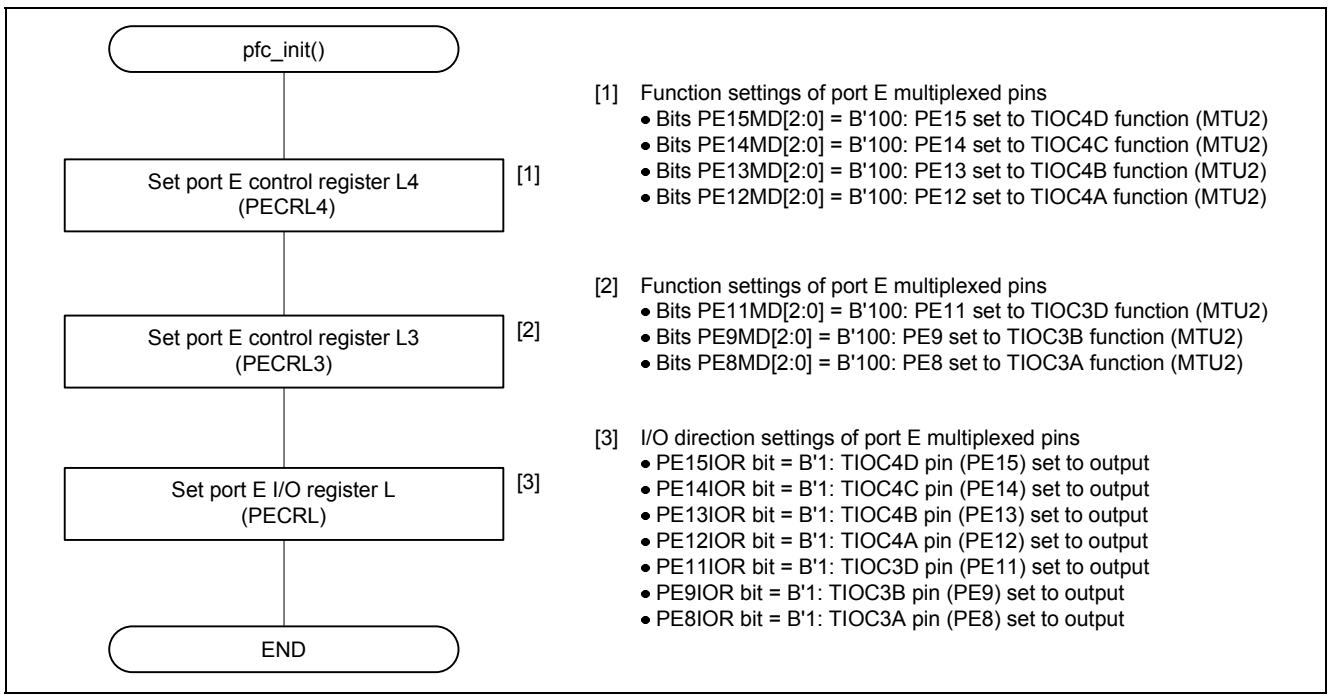

Figure 12 Pin Function Controller (PFC) Settings

2.4.5 Channel 3 Compare-Match (TGRA_3) Interrupt Handler

Figure 13 shows the processing sequence of the MTU2 channel 3 compare-match (TGRA_3) interrupt handler. An interrupt is generated once each PWM carrier cycle.

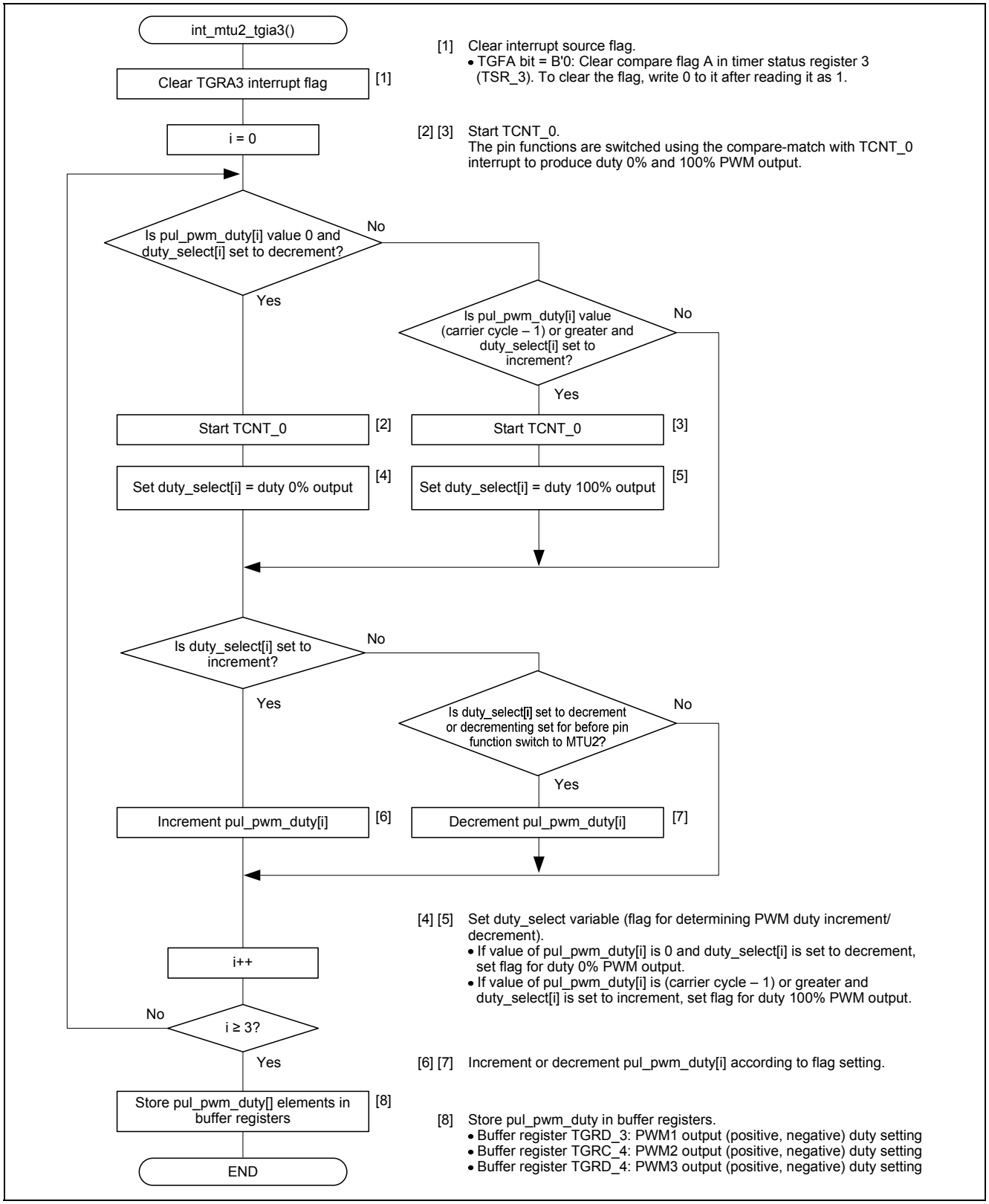

Figure 13 MTU2 Channel 3 Compare-Match (TGRA_3) Interrupt Handler

2.4.6 Channel 0 Compare-Match (TGRA_0) Interrupt Handler

Figure 14 shows the processing sequence of the MTU2 channel 0 compare-match (TGRA_0) interrupt handler.

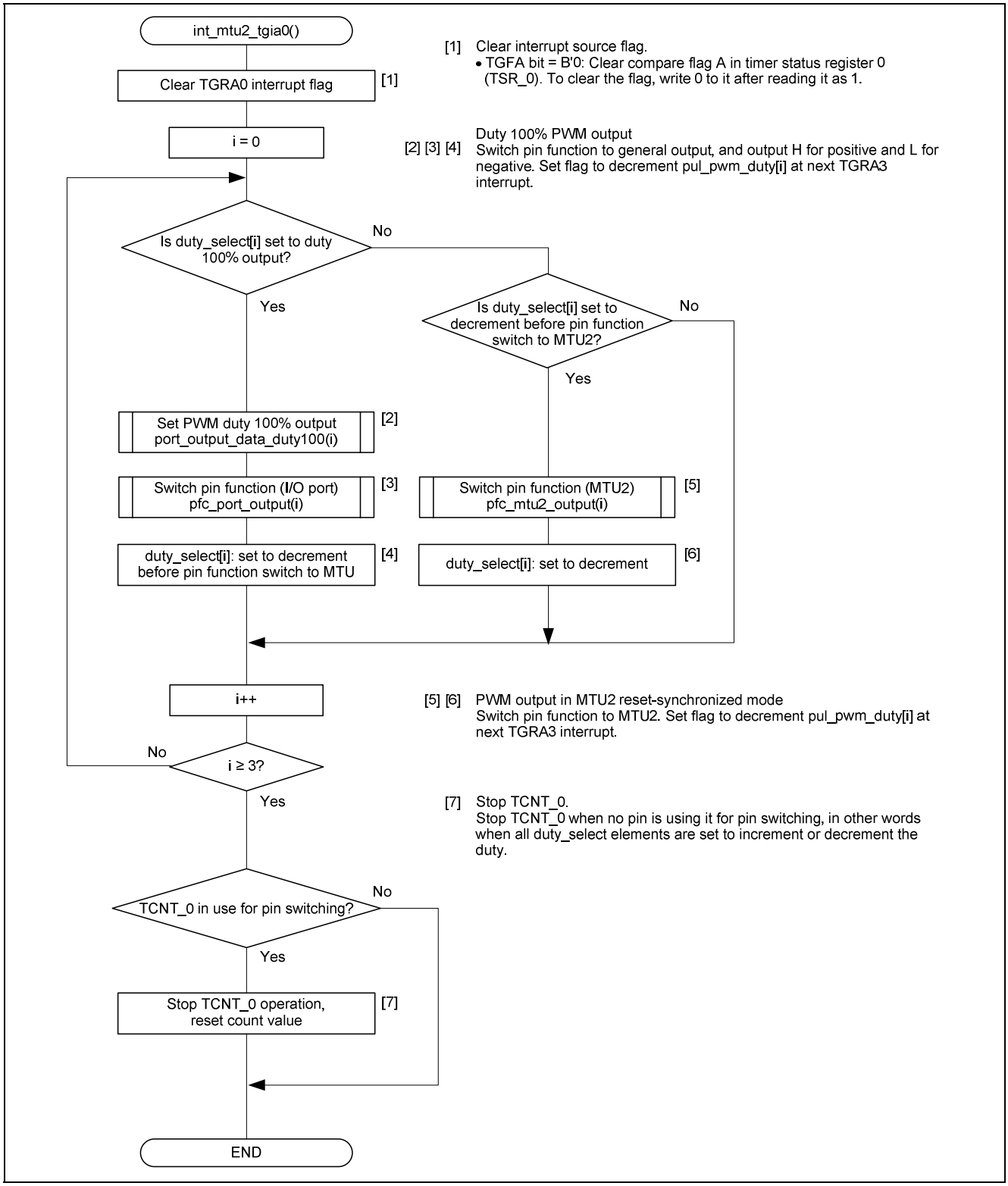

Figure 14 MTU2 Channel 0 Compare-Match (TGRA_0) Interrupt Handler

2.4.7 Channel 0 Compare-Match (TGRB_0) Interrupt Handler

Figure 15 shows the processing sequence of the MTU2 channel 0 compare-match (TGRB_0) interrupt handler.

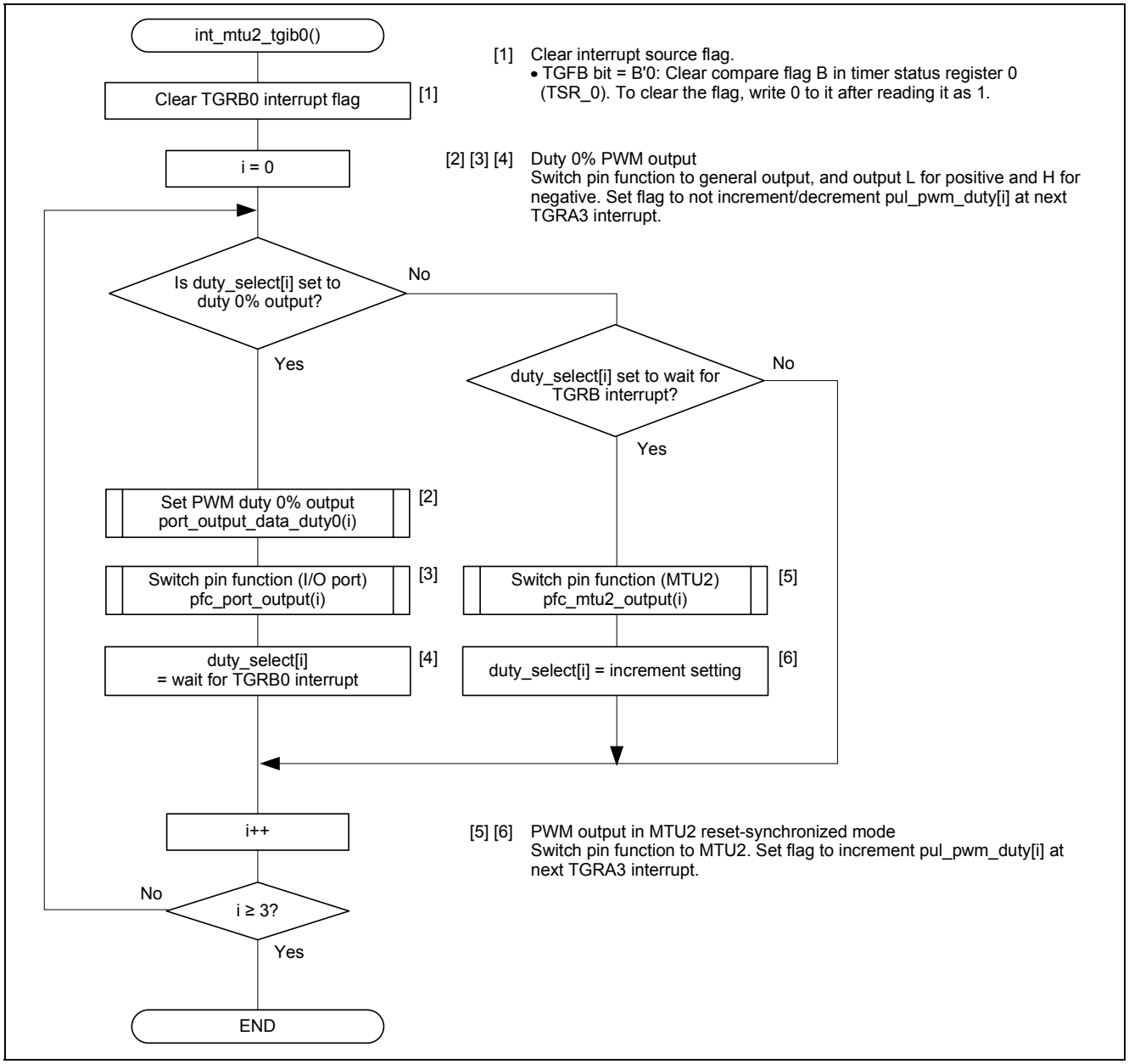

Figure 15 MTU2 Channel 0 Compare-Match (TGRB_0) Interrupt Handler

2.4.8 General Output Settings (PWM Duty 0%)

Figure 16 shows the processing sequence for general output settings to produce duty 0% PWM output for positive.

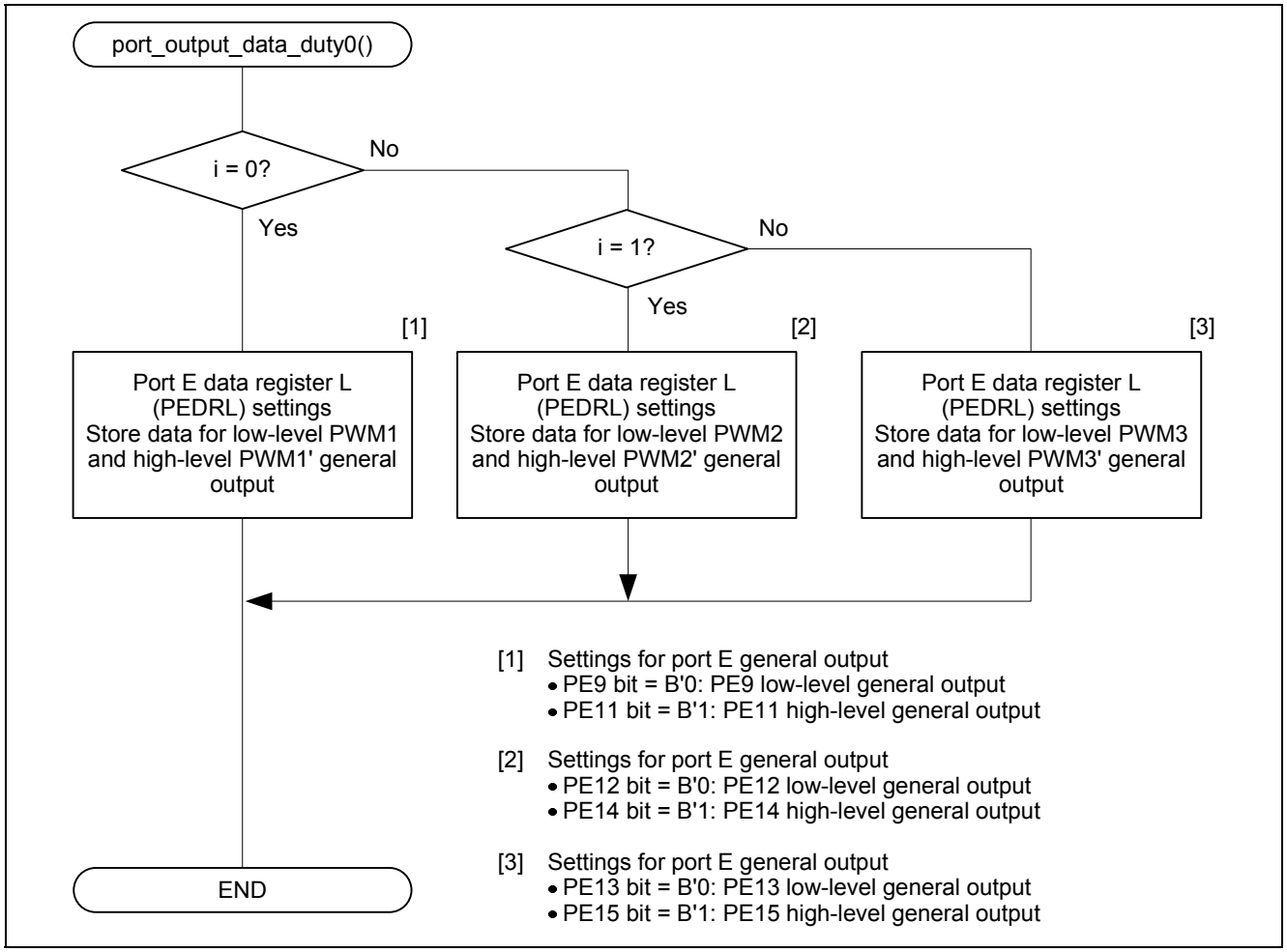

Figure 16 General Output Settings (PWM Duty 0%)

2.4.9 General Output Settings (PWM Duty 100%)

Figure 17 shows the processing sequence for general output settings to produce duty 100% PWM output for positive.

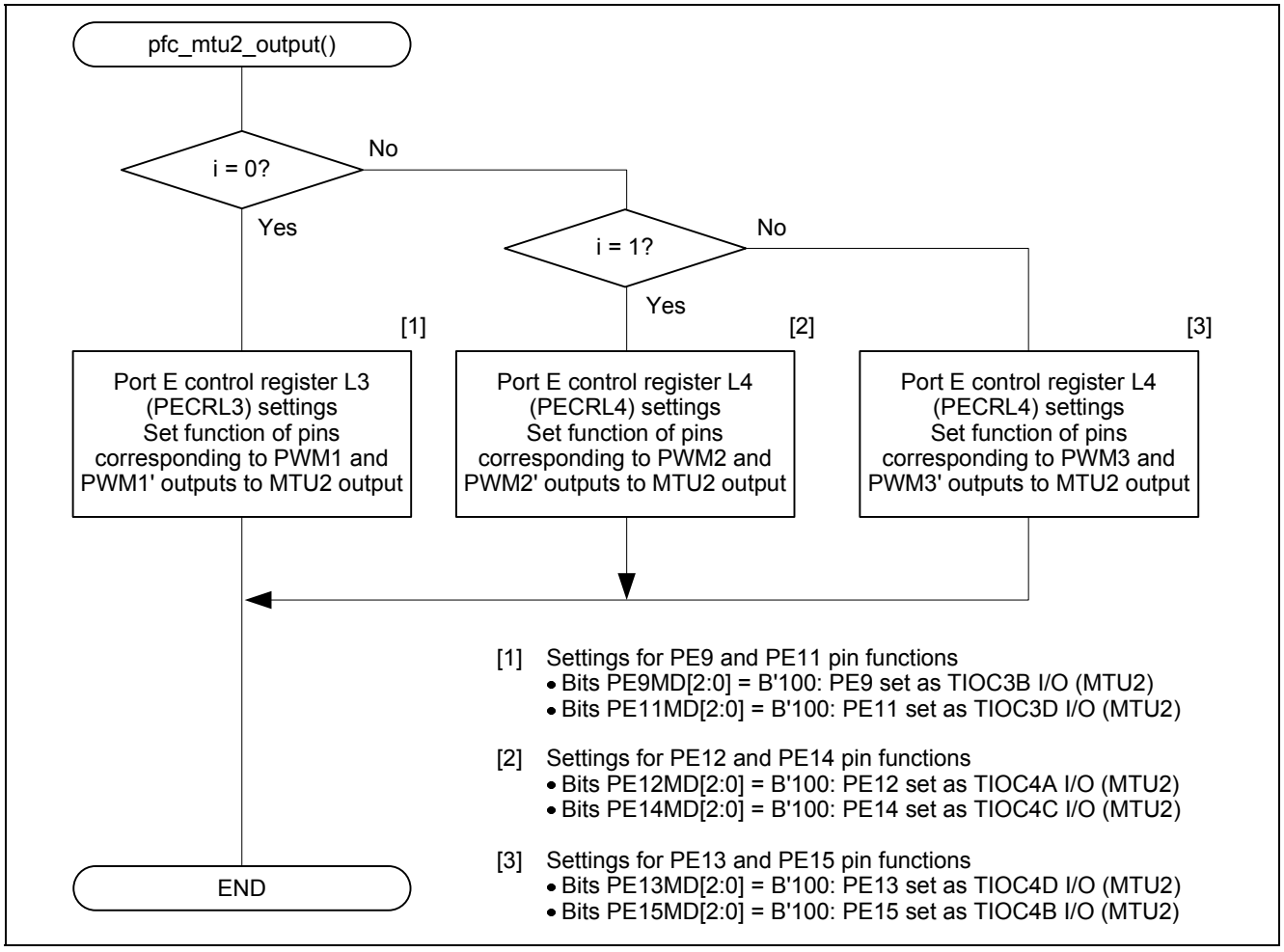

Figure 17 General Output Settings (PWM Duty 100%)

2.4.10 Pin Function Switching (I/O Port)

Figure 18 shows the processing sequence for switching the pin function to I/O port for duty 0% and 100% PWM output.

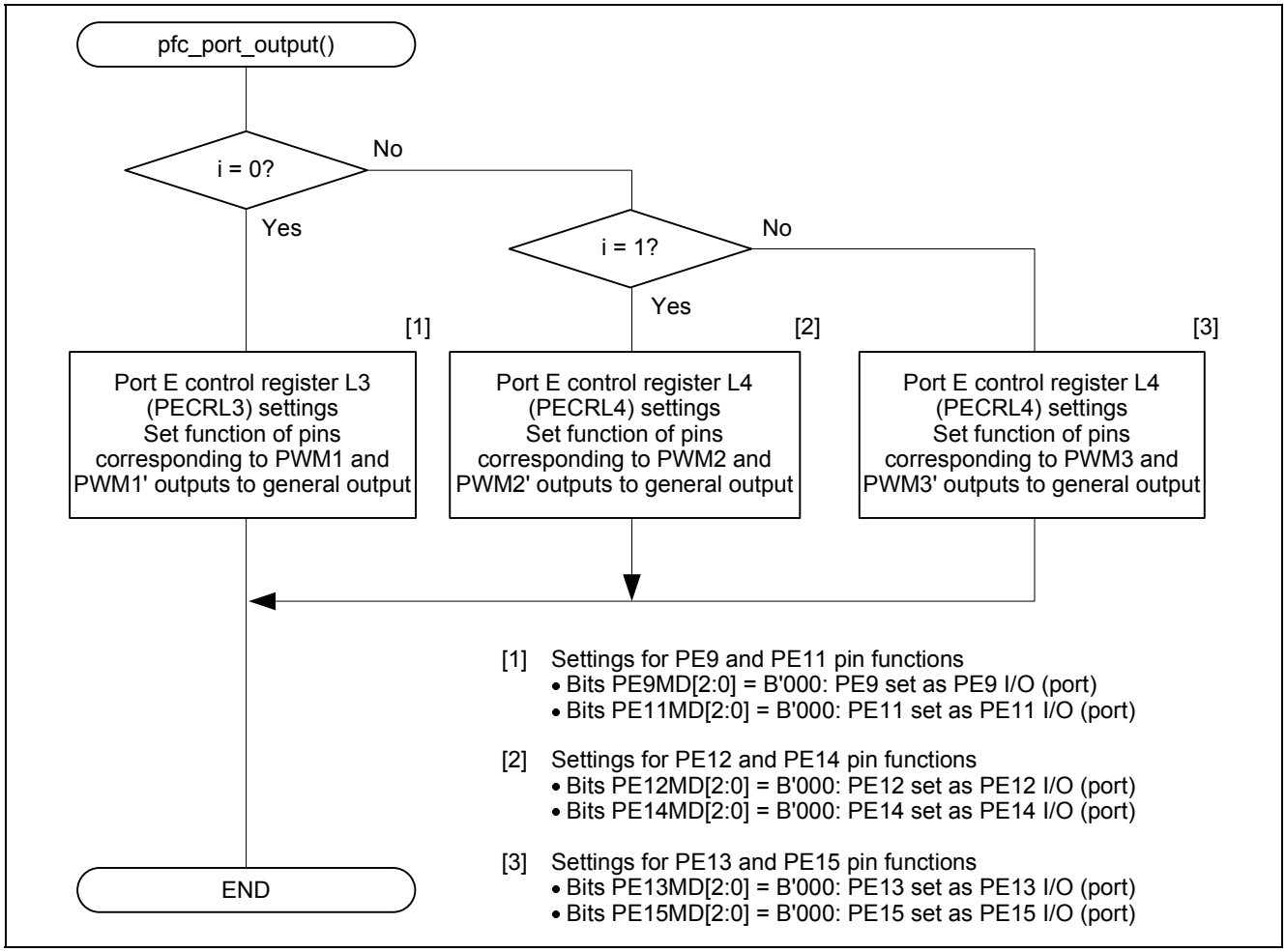

Figure 18 Pin Function Switching (I/O Port)

2.4.11 Pin Function Switching (MTU2)

Figure 19 shows the processing sequence for switching the pin function to MTU2 for other than duty 0% and 100% PWM output.

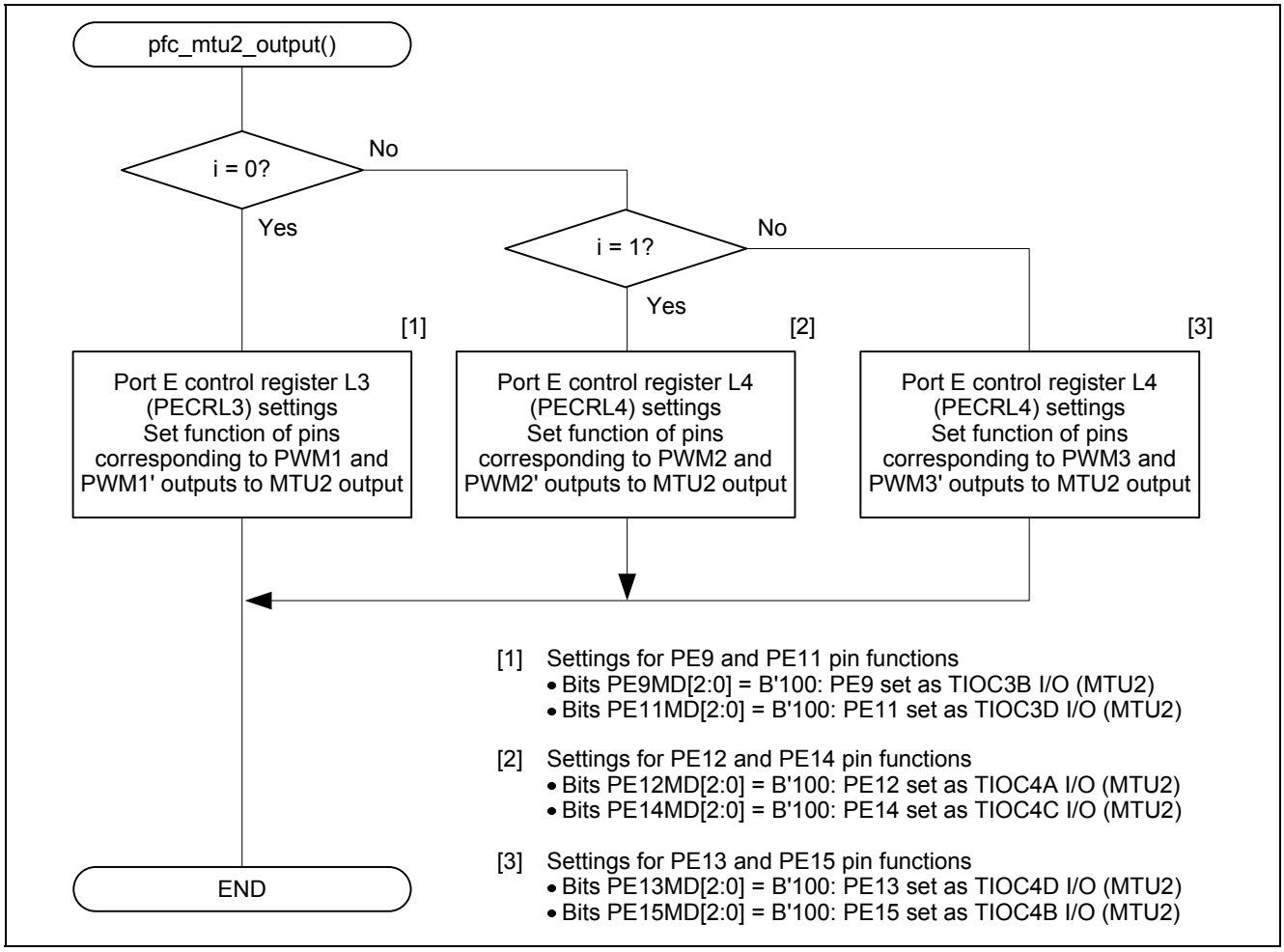

Figure 19 Pin Function Switching (MTU2)

2.5 Reference Program Settings

The register setting values used in the reference program are described below.

2.5.1 Clock Pulse Generator (CPG)

Table 9 lists the register settings of the clock pulse generator.

Table 9 Clock Pulse Generator (CPG)

Register	Address	Setting Value	Description
Frequency control register (FRQCR)	H'FFFE0010	H'0305	Specifies clock output settings and operation frequency division ratios. STC[1:0] = B'11: ×1/4, bus clock (Bϕ) IFC[2:0] = B'000: ×1, internal clock (Iϕ) PFC[2:0] = B'101: ×1/8, peripheral clock (Pϕ)

2.5.2 Power-Down Modes

Table 10 lists the register settings related to the power-down modes.

Table 10 Power-Down Modes

Register	Address	Setting Value	Description
Standby control register 3 (STBCR3)	H'FFFE0408	H'5E	Operation settings for individual modules HIZ = B'0: Pin states maintained in software standby MSTP36 = B'1: Clock supply to MTU2S stopped MSTP35 = B'0: MTU2 operating MSTP34 = B'1: Clock supply to POE2 stopped MSTP33 = B'1: Clock supply to IIC3 stopped MSTP32 = B'1: Clock supply to ADC0 stopped MSTP31 = B'1: Reserved bit MSTP30 = B'0: Flash memory operating

2.5.3 Multi-Function Timer Pulse Unit 2 (MTU2)

Table 11 lists the register settings of the multi-function timer pulse unit 2 (MTU2).

Table 11 Multi-Function Timer Pulse Unit 2 (MTU2)

Register	Address	Setting Value	Description
Timer control register 3 (TCR_3)	H'FFFE4200	H'21	TCNT control settings CCLR[2:0] = B'001: Clear TCNT at TGRA compare-match. CKEG[1:0] = B'00: Count at rising edge. TPSC[2:0] = B'001: TCNT counts on internal clock Pϕ/4.
Timer control register 4 (TCR_4)	H'FFFE4201	—	TCNT control settings When channel 3 is set to reset-synchronized PWM mode, the settings for channel 4 are ignored and the channel 3 settings are followed automatically. Make no settings to this register; simply leave the default values unchanged.
Timer counter 3 (TCNT_3)	H'FFFE4210	H'0000	16-bit counter Set to initial value of 0.
Timer counter 4 (TCNT_4)	H'FFFE4212	H'0000	16-bit counter Set to initial value of 0.
Timer general register A_3 (TGRA_3)	H'FFFE4218	D'2499	TCNT_3 upper limit value setting Sets the PWM carrier cycle. The buffer register is used to update the cycle (period) during operation.
Timer general register C_3 (TGRC_3)	H'FFFE4224		TGRA_3 buffer register Set to the same values as the TGRA_3 register as the initial setting.
Timer general register B_3 (TGRB_3)	H'FFFE421A	D'0 to D'2498	PWM output 1 compare register PWM duty setting. The initial setting is D'0. The buffer register is used to update the PWM duty during operation.
Timer general register D_3 (TGRD_3)	H'FFFE4226		TGRB_3 buffer register Set to the same values as the TGRB_3 register as the initial setting.
Timer general register A_4 (TGRA_4)	H'FFFE421C	D'0 to D'2498	PWM output 2 compare register PWM duty setting. The initial setting is D'1666. The buffer register is used to update the PWM duty during operation.
Timer general register C_4 (TGRC_4)	H'FFFE4228		TGRA_4 buffer register Set to the same values as the TGRA_4 register as the initial setting.
Timer general register B_4 (TGRB_4)	H'FFFE421E	D'0 to D'2498	PWM output 3 compare register PWM duty setting. The initial setting is D'1666. The buffer register is used to update the PWM duty during operation.
Timer general register D_4 (TGRD_4)	H'FFFE422A		TGRA_4 buffer register Set to the same values as the TGRA_4 register as the initial setting.

Register	Address	Setting Value	Description
Timer output control register 1 (TOCR1)	H'FFFE420E	H'43	Reset-synchronized PWM mode output control PSYE = B'1: Toggle output synchronized with PWM period enabled TOCL = B'0: Writing to TOCS, OLSN, and OLSP bits enabled TOCS = B'0: TOCR1 setting enabled OLSN = B'1: Reset-synchronized PWM mode negative output level selection Initial output = low, active level = high OLSP = B'1: Reset-synchronized PWM mode positive output level selection Initial output = low, active level = high
Timer mode register 3 (TMDR_3)	H'FFFE4202	H'38	Operating mode settings (channel 3) BFB = B'1: Buffer operation by TGRB and TGRD BFA = B'1: Buffer operation by TGRA and TGRC MD3 to MD0 = B'1000: Reset-synchronized PWM mode
Timer mode register 4 (TMDR_4)	H'FFFE4203	H'00 (Initial Value)	Operating mode settings (channel 4) When channel 3 is set to reset-synchronized PWM mode, the settings for channel 4 are ignored and the channel 3 settings are followed automatically. Leave the initial values unchanged. To enable buffer operation, leave bits BFA and BFB in TMDR_4 cleared to 0.
Timer output master enable register (TOER)	H'FFFE420A	H'FF	MTU2 output pin output setting enable/disable OE4D = B'1: MTU2 output on TIOC4D pin enabled OE4C = B'1: MTU2 output on TIOC4C pin enabled OE3D = B'1: MTU2 output on TIOC3D pin enabled OE4B = B'1: MTU2 output on TIOC4B pin enabled OE4A = B'1: MTU2 output on TIOC4A pin enabled OE3B = B'1: MTU2 output on TIOC3B pin enabled
Timer interrupt enable register 3 (TIER_3)	H'FFFE4208	H'01	Interrupt request enable/disable control TGIEA = B'1: Triggering of interrupt request (TGIA) by TGFA bit enabled
Timer start register (TSTR)	H'FFFE4280	H'40, H'41	Channel 0 to 4 TCNT operation/stop selection CST3 = B'1: TCNT_3 performs count operation. Note: In reset-synchronized PWM mode, setting the CST3 bit in TSTR to 1 causes TCNT_3 of channel 3 and TCNT_4 of channel 4 to start count operation. Do not set TCNT_4 of channel to perform count operation (CST4 = B'1). The initial setting of TCNT_0 is count stopped (CST0 = B'0). While the program is running, operation is started (CST0 = B'1) and stopped. TCNT_2 and TCNT_1 count operation is stopped.
Timer control register 0 (TCR_0)	H'FFFE4300	H'21	TCNT control settings CCLR[2:0] = B'001: Clear TCNT at TGRA compare-match. CKEG[1:0] = B'00: Count at rising edge. TPSC[2:0] = B'001: TCNT counts on internal clock Pϕ/4.
Timer counter 0 (TCNT_0)	H'FFFE4306	H'0000	16-bit counter Set to initial value of 0.

Register	Address	Setting Value	Description
Timer general register A_0 (TGRA_0)	H'FFFE4308	D'2499	Channel 0 reset source compare register Set to same value as TGRA_3.
Timer general register B_0 (TGRB_0)	H'FFFE430A	D'2469	This compare register sets the timing of pin function switching. Select a setting that takes into account the interrupt response time, necessary number of instruction cycles, and number of cycles needed to access the peripheral module register.
Timer mode register 0 (TMDR_0)	H'FFFE4301	H'00	Operating mode settings (channel 0) BFB = B'0: Normal operation of TGRB and TGRD BFA = B'0: Normal operation of TGRA and TGRC MD3 to MD0 = B'0000: Normal mode
Timer interrupt enable register 0 (TIER_0)	H'FFFE4304	H'03	Interrupt request enable/disable control TGIEB = B'1: Triggering of interrupt request (TGIB) by TGFB bit enabled TGIEA = B'1: Triggering of interrupt request (TGIA) by TGFA bit enabled

2.5.4 Interrupt Controller (INTC)

Table 12 lists the register settings of the interrupt controller (INTC).

Table 12 Interrupt Controller (INTC)

Register	Address	Setting Value	Description
Interrupt priority register 9 (IPR09)	H'FFFE0C08	H'F000	Interrupt priority (level 0 to 15) setting Bits 15 to 12 = B'1111: MTU2 (TGIA_0 to TGID_0) interrupt level = 15 Bits 11 to 8 = B'0000: MTU2 (TCIV_0, TGIE_0, and TGIF_0) interrupt level = 0 Bits 7 to 4 = B'0000: MTU2 (TGIA_1 and TGIB_1) interrupt level = 0 Bits 3 to 0 = B'0000: MTU2 (TCIV_1 and TGIU_1) interrupt level = 0
Interrupt priority register 10 (IPR10)	H'FFFE0C08	H'00E0	Interrupt priority (level 0 to 15) setting Bits 15 to 12 = B'0000: MTU2 (TGIA_0 and TGIB_2) interrupt level = 0 Bits 11 to 8 = B'0000: MTU2 (TCIV_2, and TGIU_2) interrupt level = 0 Bits 7 to 4 = B'1110: MTU2 (TGIA_3 to TGID_3) interrupt level = 14 Bits 3 to 0 = B'0000: MTU2 (TCIV_3) interrupt level = 0

2.5.5 Pin Function Controller (PFC)

Table 13 lists the register settings of the pin function controller (PFC).

Table 13 Pin Function Controller (PFC)

Register	Address	Setting Value	Description
Port E control register L4 (PECRL4)	H'FFFE3A10	H'xxxx	Port E multiplex pin function settings The initial setting values are as follows. • PE15MD[2:0] = B'100: PE15 functions as TIOC4D I/O (MTU2). • PE14MD[2:0] = B'100: PE14 functions as TIOC4C I/O (MTU2). • PE13MD[2:0] = B'100: PE13 functions as TIOC4B I/O (MTU2). • PE12MD[2:0] = B'100: PE12 functions as TIOC4A I/O (MTU2). While the program is running, the settings of the various bits change between their initial values and the following values. • PE15MD[2:0] = B'000: PE15 functions as PE15 I/O (Port). • PE14MD[2:0] = B'000: PE14 functions as PE14 I/O (Port). • PE13MD[2:0] = B'000: PE13 functions as PE13 I/O (Port). • PE12MD[2:0] = B'000: PE12 functions as PE12 I/O (Port).
Port E control register L3 (PECRL3)	H'FFFE3A12	H'x0x4	Port E multiplex pin function settings The initial setting values are as follows. • PE11MD[2:0] = B'100: PE11 functions as TIOC3D I/O (MTU2). • PE10MD[2:0] = B'000: PE10 functions as PE10 I/O (Port). • PE9MD[2:0] = B'100: PE9 functions as TIOC3B I/O (MTU2). • PE8MD[2:0] = B'100: PE8 functions as TIOC3A I/O (MTU2). While the program is running, the settings of the various bits change between their initial values and the following values. • PE11MD[2:0] = B'100: PE11 functions as PE11 I/O (Port). • PE10MD[2:0] = B'100: PE10 functions as PE10 I/O (Port).
Port E IO register L (PEIORL)	H'FFFE3886	H'FB00	Port E pin I/O direction settings • PE15IOR = B'1: PE15 functions as an output pin. • PE14IOR = B'1: PE14 functions as an output pin. • PE13IOR = B'1: PE13 functions as an output pin. • PE12IOR = B'1: PE12 functions as an output pin. • PE11IOR = B'1: PE11 functions as an output pin. • PE9IOR = B'1: PE9 functions as an output pin. • PE8IOR = B'1: PE8 functions as an output pin. All other bits set to B'0: All function as input pins.

2.5.6 I/O Port

Table 14 lists the I/O port-related register settings.

Table 14 I/O Port

Register	Address	Setting Value	Description
Port B data register L (PBDRL)	H'FFFE3882	H'xx00	Port B general output pin output value settings When PWM1 output duty is 0% • PE11DR = B'1: H output on PE11 • PE9DR = B'0: L output on PE9 When PWM1 output duty is 100% • PE11DR = B'0: L output on PE11 • PE9DR = B'1: H output on PE9 When PWM2 output duty is 0% • PE11DR = B'1: H output on PE14 • PE9DR = B'0: L output on PE12 When PWM2 output duty is 100% • PE11DR = B'0: L output on PE14 • PE9DR = B'1: H output on PE12 When PWM3 output duty is 0% • PE11DR = B'1: H output on PE15 • PE9DR = B'0: L output on PE13 When PWM3 output duty is 100% • PE11DR = B'0: L output on PE15 • PE9DR = B'1: H output on PE13

3. Documents for Reference

- Hardware Manual
  SH7216 Group Hardware Manual [REJ09B0543]
  (The latest version can be downloaded from the Renesas Electronics Web site.)
- Software Manual
  SH-2A/SH2A-FPU Software Manual [REJ09B0051]
  (The latest version can be downloaded from the Renesas Electronics Web site.)

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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Sep.07.10	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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