SH7216 Series

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Digital Power Control for PFC

Introduction

This application note describes the design of a Power Factor Correction(PFC) based on the Renesas SH7216 microcontrollers.

This PFC provide a reference design using Renesas SH7216 MCU, which has the fast processing core and I/O port for the controller needs.

Target Device

SuperH RISC engine Family SH7216 Series

Contents

1. System Architecture

The following is online UPS platform composed of PFC, Intverter, Boot, PFC and SH7216 CPU board. UPS function is controlled fully by SH7216. This document only describes PFC how controlled by SH7216 CPU board.

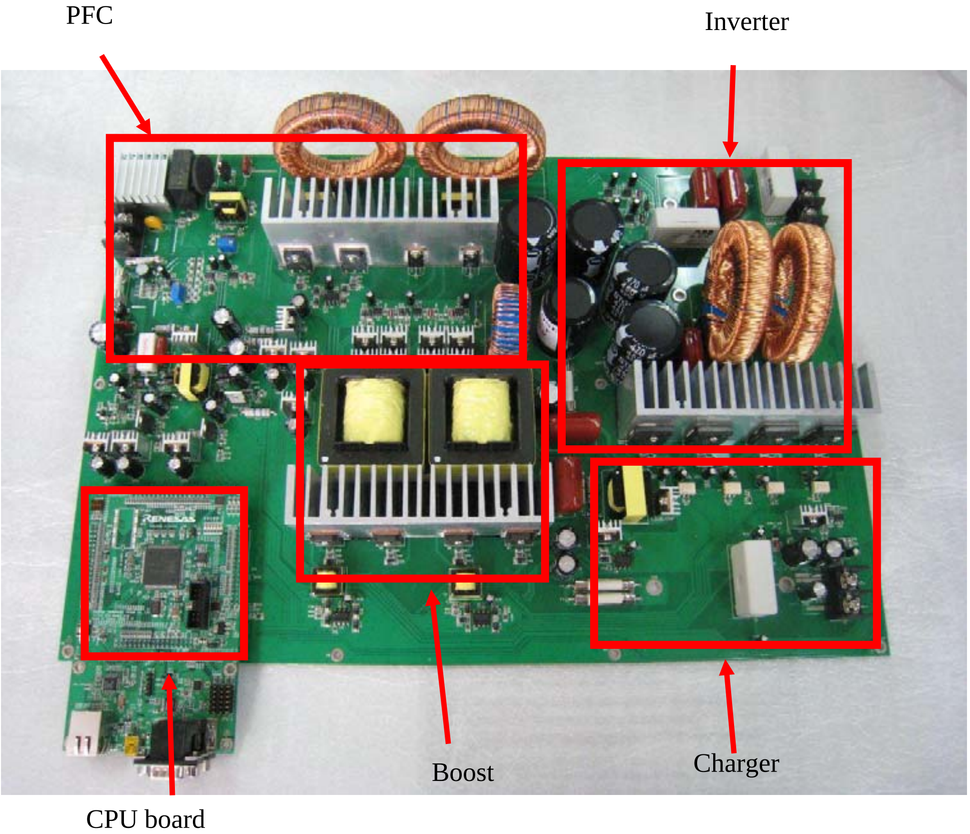


Figure 1-1 Online UPS platform

The PFC system consists of two main portions. These are:

- CPU Board
- PFC Board

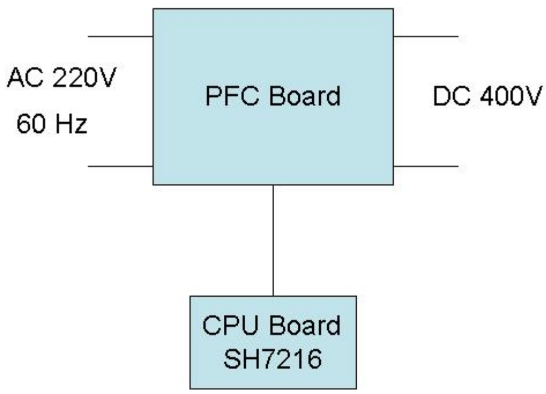


Figure 1-2 Block diagram

2. Specifications

The detail designed specifications of the power stage board are shown in Table 2-1.

Table 2-1 System specifications

	PFC
Input Voltage	AC 220 V
Output Voltage	DC 400 V
Output Waveform	DC
Type/Topology	Boost type
Max. Input Current	AC 6.364 A
Max. Output Current	DC 3.5 A
Max. Output Power	1.4 kW

CPU Board:

- Renesas Microcontroller: SH7216

NOTE:

The use of high voltage power supplies is extremely dangerous. Only authorized personnel working in a controlled environment are allowed to change the system configuration, at their own risk.

The voltage supply in the standard configuration is 220Vac.

Renesas does not assume any responsibility for any voluntary modification of the standard demonstration hardware as well as over any misuse of the proposed system.

2.1 CPU Board

The CPU board can be used to control the online UPS for PFC, Boost, Charger and Inverter. The microcontroller responsible for the following tasks for PFC :
1) PFC and close loop regulation algorithm
2) Relay management
3) MOSFETs management.

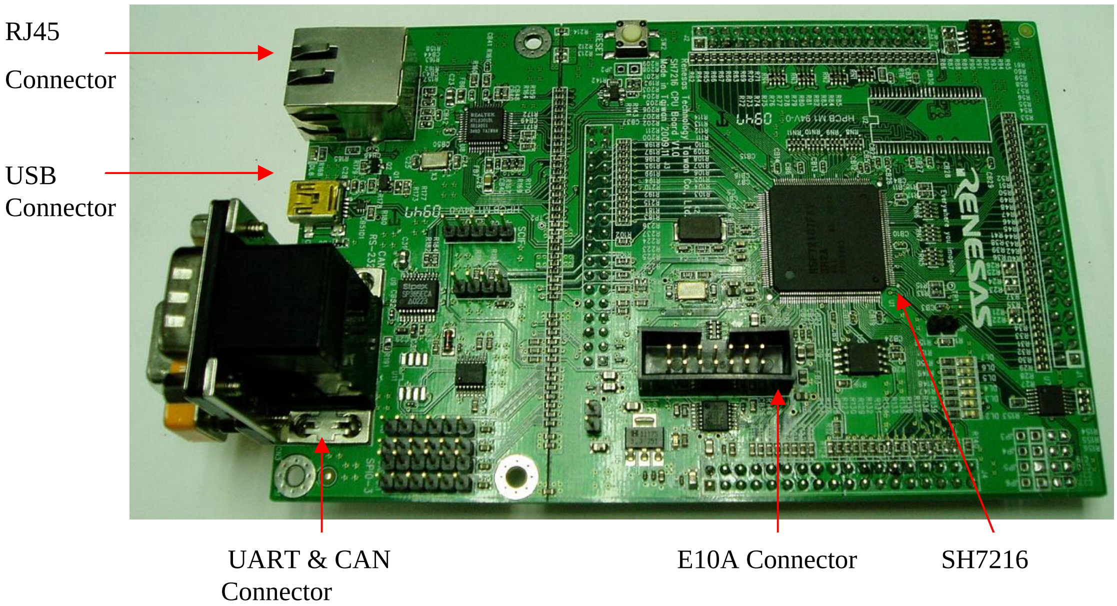


Figure 2-0-1 CPU Board

3. System Configuration / Control Block Diagram

Figure 3-1 is to show control diagram of PFC, it consists of PI control, ADC and PWM.

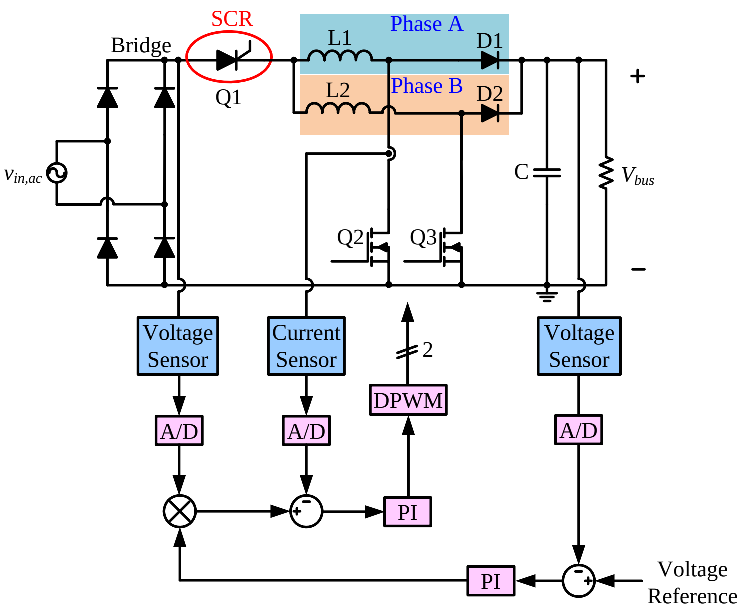


Figure 3-1 Control diagram for PFC

4. Hardware block diagram analysis

The purpose of PFC is to let input current following in same phase with input voltage waveform. The circuit of PFC used in this system is shown in Figure 4-1. The basic topology is an interleave PFC. The input side of PFC circuit is diode bridge-rectifier. The MOSFET controls the input current waveform. The output of PFC is 400V DC.

Soft-start function for PFC is used to avoid inrush current caused by output capacitor. During UPS power on, the filter capacitors are completely discharged and act as short circuit, which will cause a high inrush current. Therefore this current may damage the power devices. With soft-start function the capacitor voltage will increase gradually. Therefore dv/dt is low and inrush current can be significantly decreased. PFC soft-start function is implemented by Silicon Controlled Rectifier (SCR). The schematic is shown in Fig. 4-1 and operational waveforms are shown in Fig. 4-2.

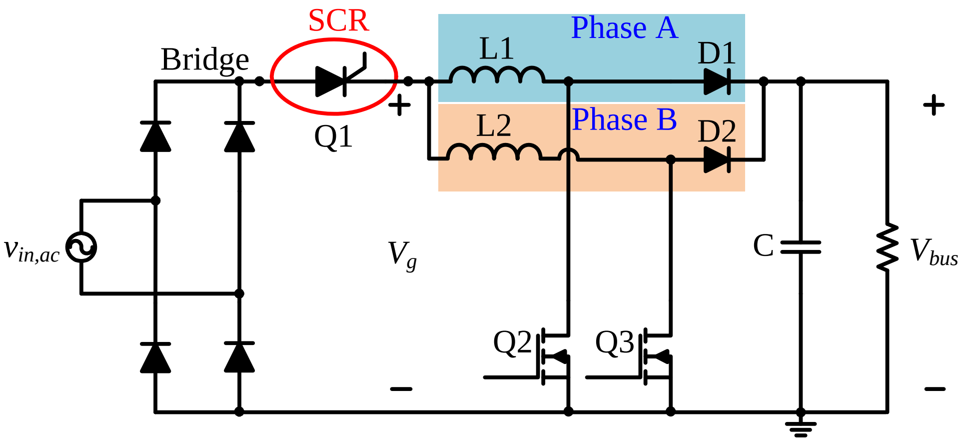


Figure 4-1 PFC circuit

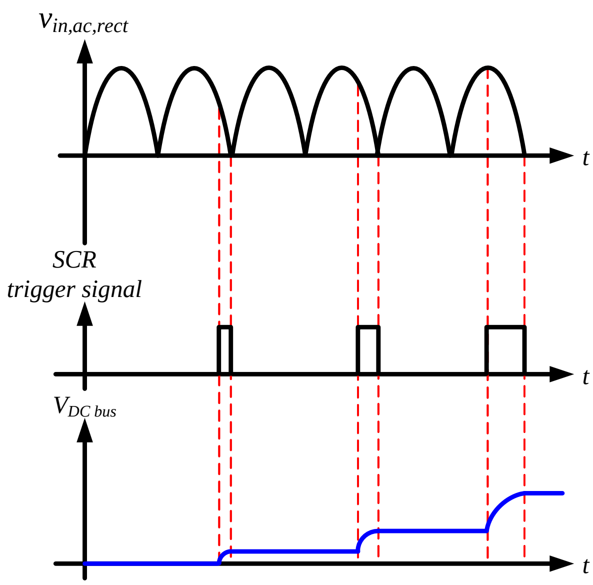
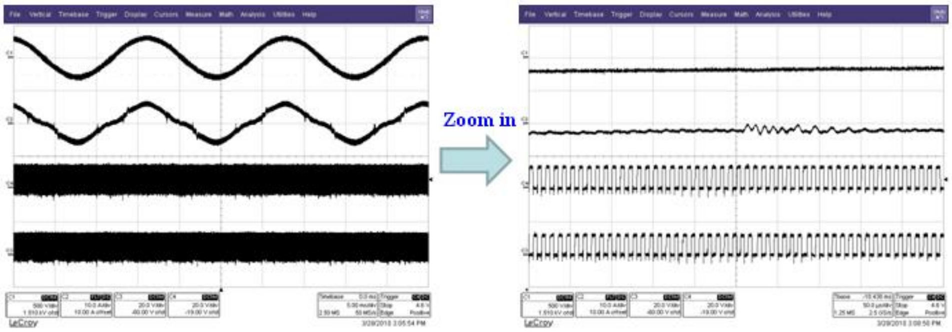


Figure 4-2 Software start operational waveform

The carrier frequency is 50KHz for PWM to control two power MOSFETs.



Ch1: Input Voltage (500V/div)

Ch2: Input Current (10A/div)

Ch3: Phase A PWM (20V/div)

Ch4: Phase B PWM (20V/div)

Figure 4-3 Phase A and B PWM control signal

The following table is measurement for efficiency of PFC.

Table 4-1 Efficiency table of PFC

Power	**PF**	**Input power**	**Output power**	**Efficiency**	**Output voltage**
100	0.856	113	105	0.929	397
200	0.914	215	207	0.962	397
300	0.931	317	308	0.971	397
400	0.949	418	405	0.968	397
500	0.966	520	505	0.971	397
600	0.976	625	605	0.968	397
700	0.984	729	707	0.970	397
800	0.988	828	805	0.972	397
900	0.990	932	906	0.972	397
1000	0.991	1036	1005	0.970	397
1100	0.992	1142	1104	0.966	397
1200	0.992	1245	1204	0.967	397
1300	0.992	1345	1305	0.970	396
1400	0.991	1451	1406	0.968	396

5. Software description

List and description of the software modules and functions

The main settings are:

io_set_cpg: performs the PLL initialization

```
WDT.WRITE.WTCSR = 0xa51e;          => WDT stop, WDT count clock setting
                                   => 1/4096 x P-clock (50MHz; 20.97msec)
WDT.WRITE.WTCNT = 0x5a85;          => Counter initial setting 10msec
CPG.FRQCR.WORD  = 0x0303;          => Clockin = 12.5MHz
                                   => I Clock = 200MHz, B Clock = 50MHz
                                   => P Clock = 50MHz
CPG.MCLKCR.BIT.MSDIVS = 1;         => MTU2S = 100MHz
CPG.ACLKCR.BIT.ASDIVS = 3;         => AD   =  50MHz
STB.CR3.BYTE = 0x02;               => Module Standby Clear
                                   => HIZ,MTU2S,MTU2,POE2,IIC3,ADC0,Reserve(1),FLASH
STB.CR4.BYTE = 0xE2;               => Module Standby Clear
                                   => SCIF3,Reserve(0),CMT,Reserve(1),EtherC
STB.CR5.BYTE = 0x12;               => Module Standby Clear
                                   => SCI0,SCI1,SCI2,SCI4,ADC1
```

pfc_init: performs the MTU2 initialization

```
ADC0.ADCR.BIT.ADCS = 0x0;          => AD0 initialization
ADC0.ADANSR.BIT.ANS0 = 0x1;
ADC0.ADANSR.BIT.ANS1 = 0x1;
ADC0.ADANSR.BIT.ANS2 = 0x1;
ADC0.ADANSR.BIT.ANS3 = 0x1;
ADC0.ADBYPSCR.BIT.SH = 0x1;
ADC1.ADCR.BIT.ADCS = 0x0;          =>  AD1 initialization
ADC1.ADANSR.BIT.ANS0 = 0x1;
ADC1.ADANSR.BIT.ANS1 = 0x1;
ADC1.ADANSR.BIT.ANS2 = 0x1;
ADC1.ADANSR.BIT.ANS3 = 0x1;

MTU2S.TSTR.BYTE = 0x0;             => Clear MTU2S counter

MTU2S3.TCR.BIT.TPSC = 0x0;         => MTU2S3 TCNT clearing disabled
MTU2S3.TCR.BIT.CKEG = 0x0;         => MTU2S3 Count at rising edge
MTU2S4.TCR.BIT.TPSC = 0x0;         => MTU2S4 TCNT clearing disabled
MTU2S4.TCR.BIT.CKEG = 0x0;         => MTU2S4 Count at rising edge

MTU2S.TDDR = 1;                    => MTU2S dead time

MTU2S3.TGRB = 495;
MTU2S3.TGRD = 495;
MTU2S4.TGRA = 300;                 => PFC output
MTU2S4.TGRC = 300;                 => PFC output
MTU2S4.TGRB = 200;                 => PFC output
MTU2S4.TGRD = 200;                 => PFC output
MTU2S.TCDR = 500;                  => triangle waveform setting 100K
MTU2S.TCBR = 500;                  => triangle waveform setting 100K
MTU2S3.TGRA = 501;                 => triangle waveform setting 100K
MTU2S3.TGRC = 501;                 => triangle waveform setting 100K

MTU2S.TOCR1.BIT.PSYE = 0x1;        => toggle output
MTU2S.TOCR1.BIT.TOCS = 0x1;
MTU2S.TOCR2.BIT.OLS3N = 0x0;       => TIOC4D
MTU2S.TOCR2.BIT.OLS3P = 0x1;       => TIOC4B

MTU2S.TOCR2.BIT.OLS2N = 0x1;       => TIOC4C
MTU2S.TOCR2.BIT.OLS2P = 0x0;       =>  TIOC4A
MTU2S.TOCR2.BIT.OLS1N = 0x0;       =>  TIOC3D
MTU2S.TOCR2.BIT.OLS1P = 0x1;       =>  TIOC3B
MTU2S3.TMDR.BIT.MD = 0xF;          => output high at peak value
MTU2S.TOER.BIT.OE3B = 0x1;         =>  TIOC3B Pin output
MTU2S.TOER.BIT.OE3D = 0x1;         =>  TIOC3D Pin output
```

```
MTU2S.TOER.BIT.OE4A = 0x1;          =>  TIOC4A Pin output
MTU2S.TOER.BIT.OE4C = 0x1;          =>  TIOC4C Pin output
MTU2S.TOER.BIT.OE4B = 0x1;          =>  TIOC4B Pin output
MTU2S.TOER.BIT.OE4D = 0x1;          =>  TIOC4D Pin output

INTC.IPR12.WORD = 0xF000;           =>  Interrupt Priority of MTU2S3
INTC.IPR13.WORD = 0xF000;           =>  Interrupt Priority of MTU2S5
MTU2S3.TIER.BIT.TGIEA = 0x1;        =>  Active MTU2S3 interrupt
MTU2S5.TIER.BIT.TGIEU = 0x1;        =>  Active MTU2S5 interrupt
MTU2S5.TCNTCMPCLR.BIT.CLRU = 0x1;       => compare match clear
MTU2S5.TIORU.BIT.IOC = 0x0;         => compare match
MTU2S5.TGRU = 1000;                 =>  output high at lower value

PFC.PDCRL3.BIT.PD10MD = 0x5;        => TIOC3BS
PFC.PDIORL.BIT.B10 = 0x1;
PFC.PDCRL3.BIT.PD11MD = 0x5;        => TIOC3DS
PFC.PDIORL.BIT.B11 = 0x1;
PFC.PDCRL4.BIT.PD12MD = 0x5;        => TIOC4AS
PFC.PDIORL.BIT.B12 = 0x1;
PFC.PDCRL4.BIT.PD13MD = 0x5;        => TIOC4BS PFC output A phase (Left side)
PFC.PDIORL.BIT.B13 = 0x1;
PFC.PDCRL4.BIT.PD14MD = 0x5;        => TIOC4CS PFC output B phase (Right side)
PFC.PDIORL.BIT.B14 = 0x1;
PFC.PDCRL4.BIT.PD15MD = 0x5;        => TIOC4DS
PFC.PDIORL.BIT.B15 = 0x1;
PFC.PECRL3.BIT.PE10MD = 0x0;        => Active relay
PFC.PEIORL.BIT.B10      = 0x1;
PFC.PECRL3.BIT.PE11MD = 0x0;        => Active relay
PFC.PEIORL.BIT.B11      = 0x1;

MTU2S.TSTR.BYTE = 0xC0;             => MTU2S3/MTU2S4 performs count operation
MTU2S5.TSTR.BYTE = 0x4;             => MTU2S5 performs count operation

PE.DR.BIT.B10 = 0x1;
```

The figure 6 shows the flow chart of the operations performed by the software.

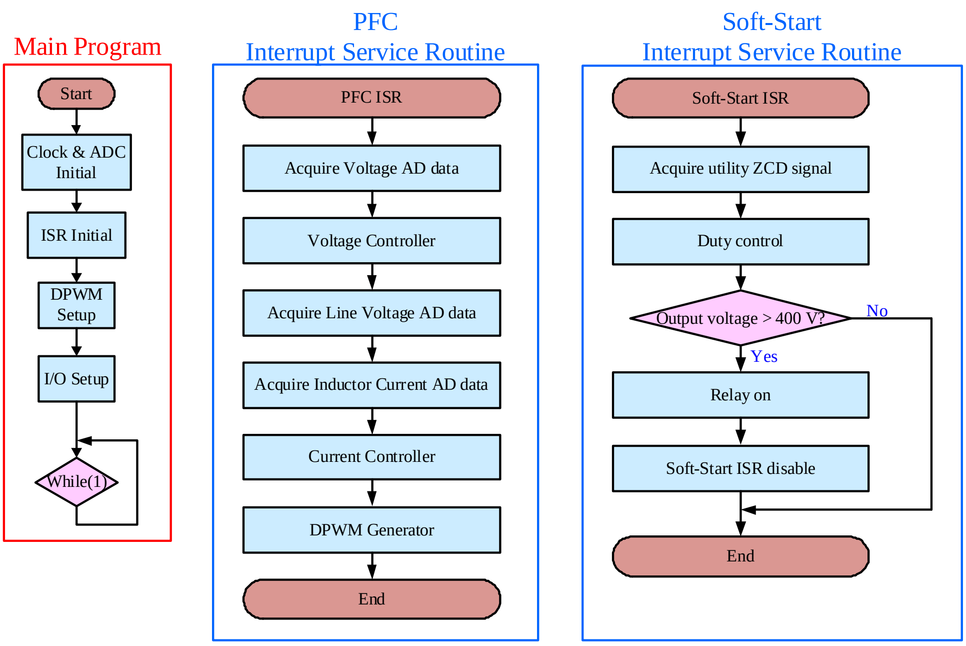
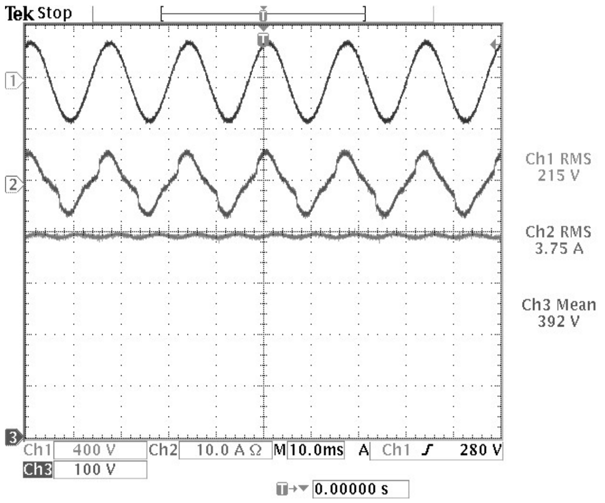


Figure 5-1 Flow Chart for PFC

6. Experimental Result

Pout = 700Watt



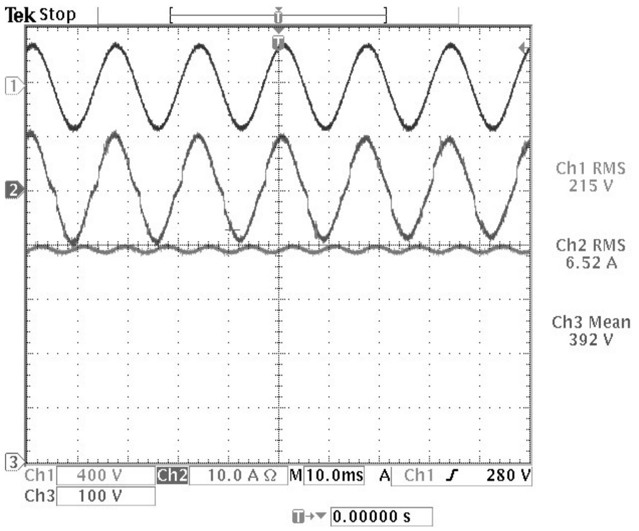
Ch1 : Input Voltage (400 V/div)

Ch2 : Input current (10 A/div)

Ch3 : Output voltage (100 V/div)

Figure 6-1 Pout=700Watt

Pout = 1400Watt



Ch1 : Input Voltage (400 V/div)

Ch2 : Input current (10 A/div)

Ch3 : Output voltage (100 V/div)

Figure 6-2 Pout=1400Watt

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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Sep.30.10	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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