SH7216 Series

R01AN0060ET0100
Rev.1.00
Sep 30, 2010

Digital Power Control for Inverter

Introduction

This application note describes the design of a sine wave inverter based on the Renesas SH7216 microcontrollers.

This Sine Wave Inverter provides a reference design using Renesas SH7216 MCU, which has the fast processing core and I/O port for the controller needs.

Target Device

SuperH RISC engine Family SH7216 Series

Contents

1. System Architecture

The inverter system consists of two main sections. These are:

- CPU Board.
- Inverter Board

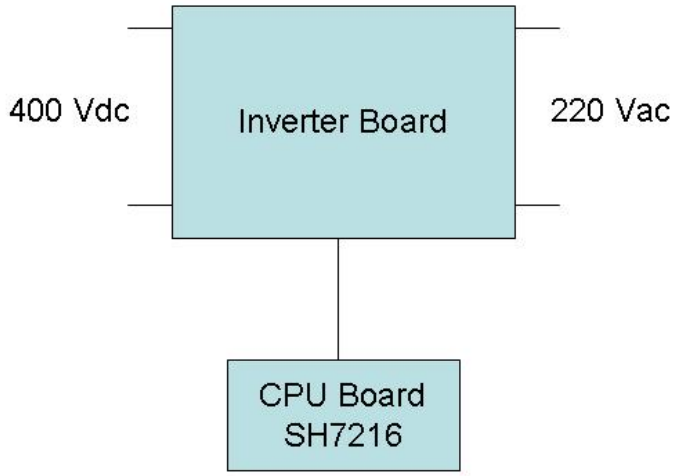


Figure 1 Block diagram

2. Specifications

The detail designed specifications of the power stage board are shown in Table 1.

Table 1 System specifications

	Inverter
Input Voltage	DC 400 V
Output Voltage	AC 220 V
Output Waveform	Sinusoidal
Type/Topology	H-Bridge
Max. Input Current	DC 3.5 A
Max. Output Current	AC 9.1A
Max. Output Power	1.4 kW

CPU Board:

- Renesas Microcontroller: SH7216

NOTE:

The use of high voltage power supplies is extremely dangerous. Only authorized personnel working in a controlled environment are allowed to change the system configuration, at their own risk.
The voltage supply in the standard configuration is 400Vdc.
Renesas does not assume any responsibility for any voluntary modification of the standard demonstration hardware as well as over any misuse of the proposed system.

2.1 CPU Boards

The CPU boards can be used to control the inverter board. The microcontroller responsible for the following tasks:
1) Regulation Close Loop algorithm
2) Inverter control
4) Relay control management for soft start
5) MOSFETs management.

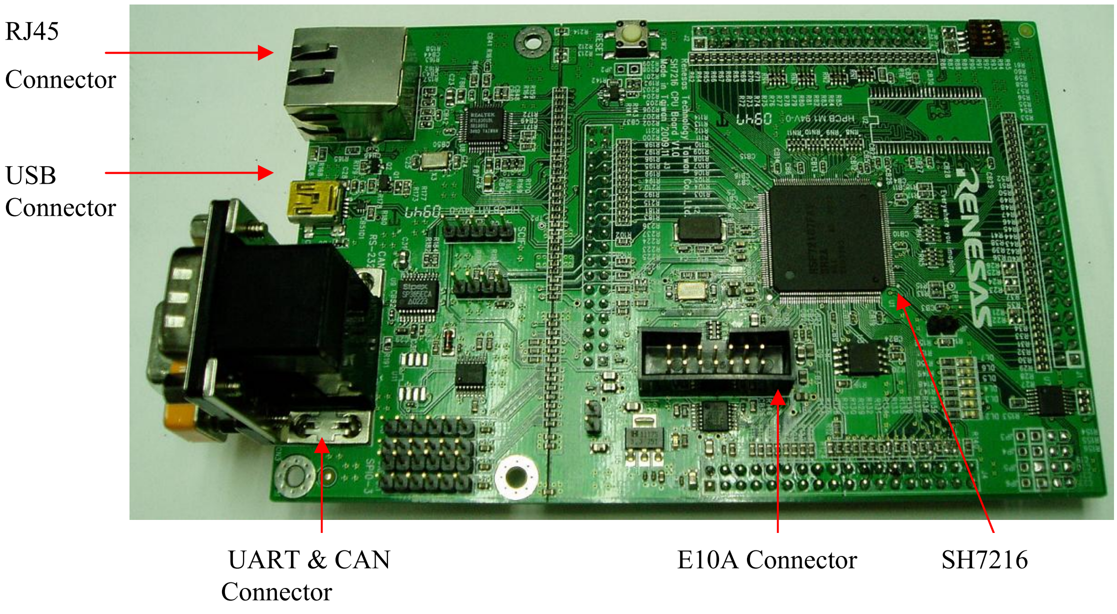


Figure 2 CPU Board

3. System Configuration / Control Block Diagram

The Regulation Close Loop algorithm method is shown in Figure 3. The output voltage of inverter is regulated at AC 220 V sine wave with 0.7 A current limit to prevent damaging of Loading. There are two close loops. The inner loop is current loop. The current loop is to control the output current to provide a stable current to load. The outer loop is voltage loop. The voltage loop is to control the output voltage to provide a pure sine wave voltage to load.

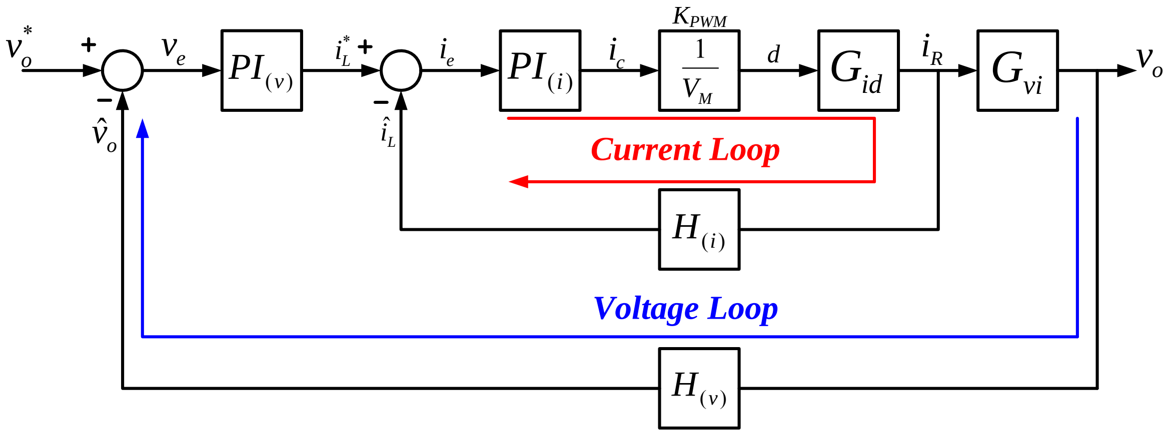


Figure 3 Close Loop algorithm for inverter

4. Hardware Block Diagram Analysis

The purpose of H-Bridge inverter is to produce single phase sine wave. The circuit of H-Bridge inverter used in this system is shown in Figure 4. The basic topology is an H-Bridge inverter with LC filter.

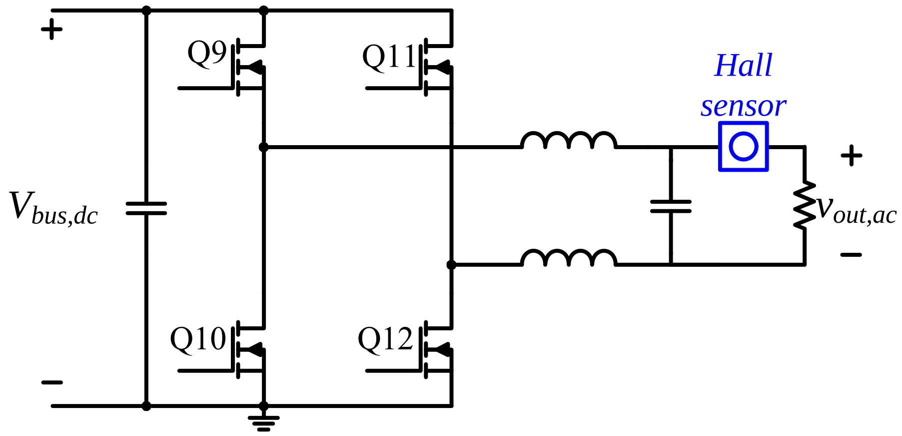
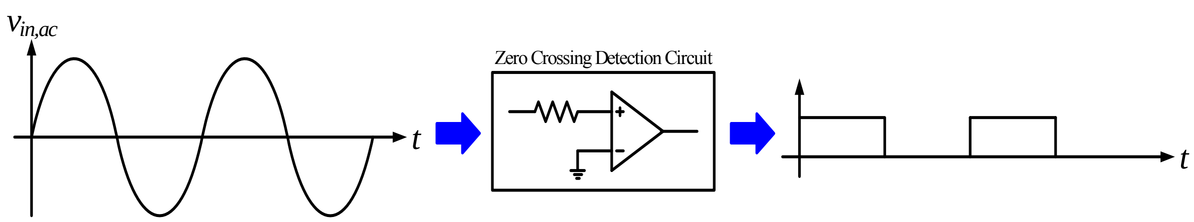


Figure 4 Inverter circuit

PLL(Phase Loop Lock)

The purpose for Phase Lock Loop (PLL) for UPS application is to synchronous the frequency and phase of the input/output voltage. This function is implemented by controlling the sine table acquiring period, therefore the output of inverter sinusoidal frequency can increase/decrease according to input sinusoidal voltage. To determine the phase of input/output voltage a zero-crossing detection (ZCD) circuit shown in the following picture



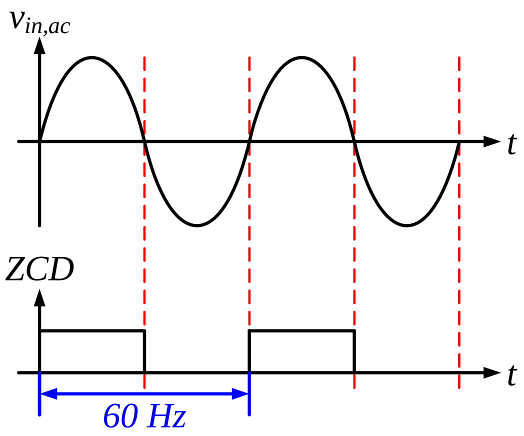


Figure 5 ZCD function

Using the capture function in SH7216, the phase difference can be derived. As shown in the below figure, the capture counter is synchronized with input voltage, by acquiring the output voltage ZCD, the phase lead and lag can be determined.

- Capture counter value (t_d) > $T_C/2$
  - Phase lead
- Capture counter value (t_d) < $T_C/2$
  - Phase lag

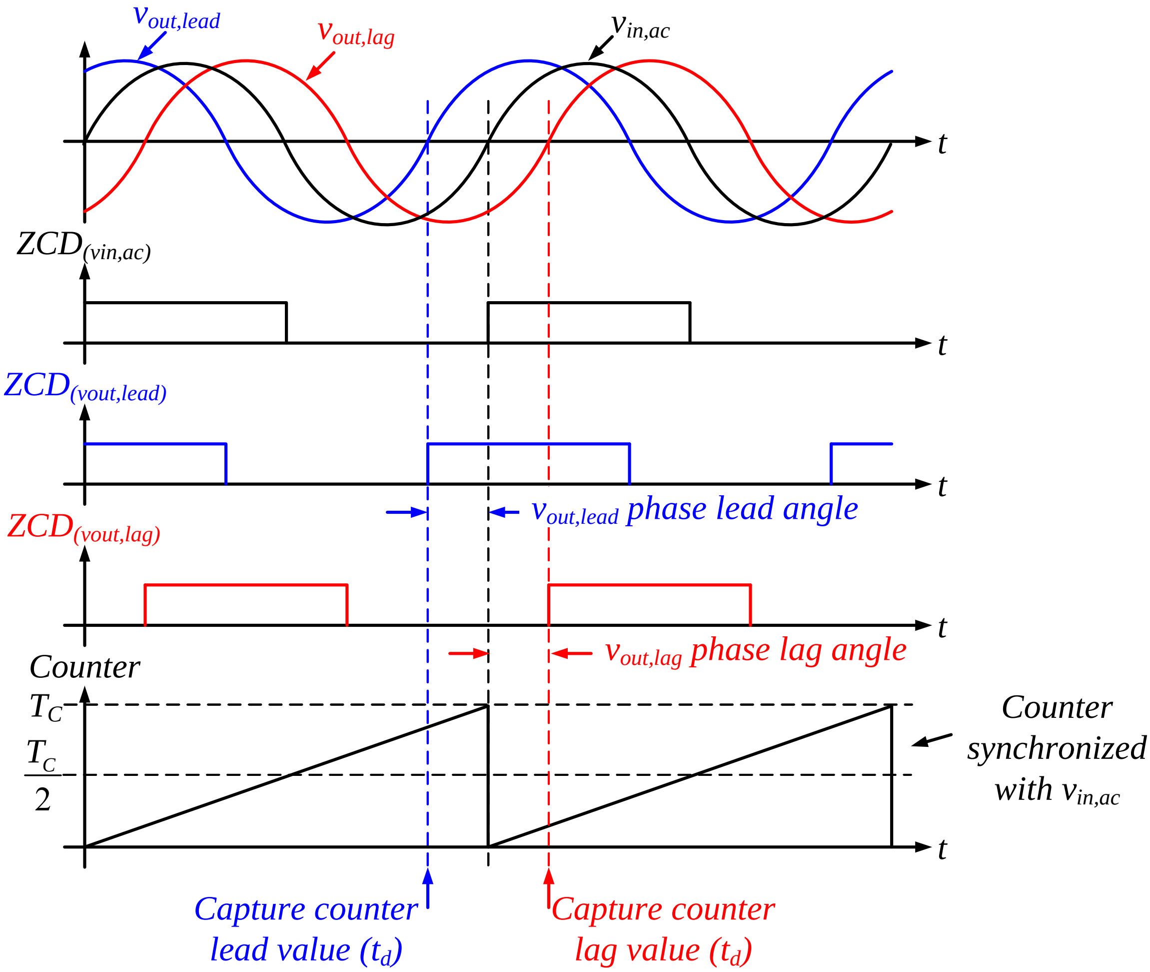


Figure 6 ZCD control

For phase lag, sine table acquire time will decrease, therefore the output sine wave frequency will increase, vice versa.

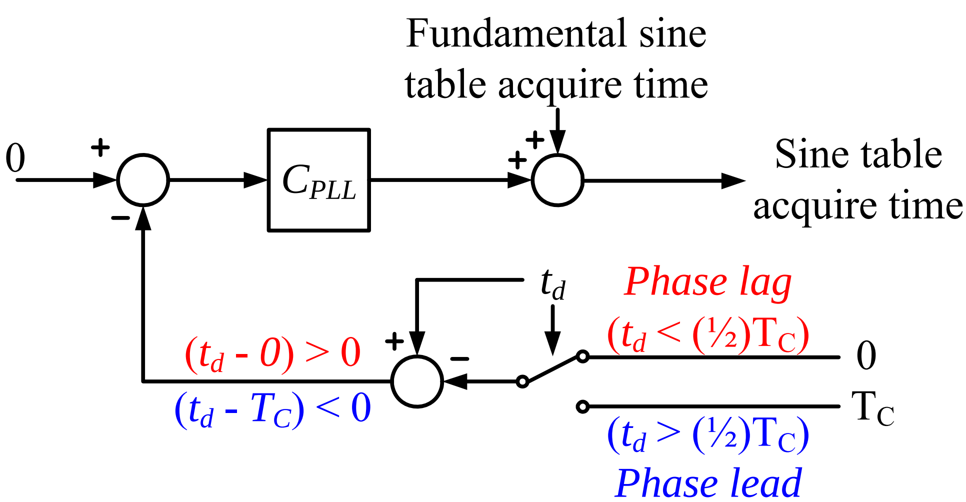


Figure 7 ZCD difference calculation

5. Software Description

List and description of the software modules and functions

The main settings are:

io_set_cpg: performs the PLL initialization

```
WDT.WRITE.WTCSR = 0xa51e;           => WDT stop, WDT count clock setting
                                     => 1/4096 x P-clock (50MHz; 20.97msec)
WDT.WRITE.WTCNT = 0x5a85;           => Counter initial setting 10msec
CPG.FRQCR.WORD  = 0x0303;           => Clockin = 12.5MHz
                                     => I Clock = 200MHz, B Clock = 50MHz
                                     => P Clock = 50MHz
CPG.MCLKCR.BIT.MSDIVS = 1;          => MTU2S = 100MHz
CPG.ACLKCR.BIT.ASDIVS = 3;          => AD   =  50MHz
STB.CR3.BYTE = 0x02;                => Module Standby Clear
                                     => HIZ,MTU2S,MTU2,POE2,IIC3,ADC0,Reserve(1),FLASH
STB.CR4.BYTE = 0xE2;                => Module Standby Clear
                                     => SCIF3,Reserve(0),CMT,Reserve(1),EtherC
STB.CR5.BYTE = 0x12;                => Module Standby Clear
                                     => SCI0,SCI1,SCI2,SCI4,ADC1
```

inverter_init: performs the MTU2 initialization

```
MTU2.TSTR.BYTE = 0x00 ;             => Count operation is stopped
MTU23.TCR.BIT.TPSC = 0x0 ;          => MTU23 TCNT clearing disabled
MTU23.TCR.BIT.CKEG = 0x0 ;          => MTU23 Count at rising edge
MTU24.TCR.BIT.TPSC = 0x0 ;          => MTU24 TCNT clearing disabled
MTU24.TCR.BIT.CKEG = 0x0 ;          => MTU24 Count at rising edge

MTU2.TDDR = 0x32;                   => Timer Dead Time
MTU2.TCDR = 0x09C4 ;
MTU2.TCBR = 0x09C4 ;
MTU23.TGRA = 0x09F6 ;
MTU23.TGRC = 0x09F6 ;

MTU2.TOCR1.BIT.PSYE = 0x1;          => 1: Toggle output is enabled
MTU2.TOCR1.BIT.TOCS = 0x1;          => 1: TOCR2 setting is selected

MTU2.TOCR2.BIT.OLS2N = 0x1;         => Output Level Select Function
MTU2.TOCR2.BIT.OLS2P = 0x1;
MTU2.TOCR2.BIT.OLS1N = 0x1;         => Output Level Select Function
MTU2.TOCR2.BIT.OLS1P = 0x1;

MTU23.TMDR.BIT.MD = 0xF ;           => Complementary PWM mode 2

MTU2.TOER.BIT.OE3B = 0x1;           => enables  the TIOC3B pin MTU2 output
MTU2.TOER.BIT.OE3D = 0x1;           => enables  the TIOC3D pin MTU2 output
MTU2.TOER.BIT.OE4A = 0x1;           => enables  the TIOC4A pin MTU2 output
MTU2.TOER.BIT.OE4C = 0x1;           => enables  the TIOC4B pin MTU2 output

MTU22.TCR.BIT.CCLR = 0x1;           => TCNT cleared by TGRA compare match
MTU22.TCR.BIT.CKEG = 0x0;           => Count at rising edge
MTU22.TCR.BIT.TPSC = 0x2;           => Internal clock: counts on Pφ/16

MTU22.TMDR.BIT.MD = 0x0;            => Normal operation

MTU22.TIOR.BIT.IOA = 0x8;           => Input capture at rising edge
MTU22.TIOR.BIT.IOB = 0x8;           => Input capture at rising edge

ADC1.ADCR.BIT.ADCS=0x0;             => 0: Single-cycle scan
ADC1.ADANSR.BIT.ANS0=0x1;           => AN7
ADC1.ADANSR.BIT.ANS1=0x1;
ADC1.ADANSR.BIT.ANS2=0x1;
```

```
ADC1.ADANSR.BIT.ANS3=0x1;

INTC.IPR10.WORD= 0xF0E0;
MTU23.TIER.BIT.TGIEA = 0x1;          => Interrupt enable for Inverter

MTU22.TIER.BIT.TGIEB = 0x1;          => Interrupt enable for PLL function


PFC.PECRL3.BIT.PE9MD  = 0x4;         => GPIO Pin setting
PFC.PECRL3.BIT.PE11MD  = 0x4;
PFC.PECRL4.BIT.PE14MD  = 0x4;
PFC.PECRL4.BIT.PE12MD  = 0x4;
PFC.PEIORL.BIT.B9       = 0x1;
PFC.PEIORL.BIT.B11      = 0x1;
PFC.PEIORL.BIT.B14      = 0x1;
PFC.PEIORL.BIT.B12      = 0x1;

PFC.PEIORL.BIT.B7       = 0x0;
PFC.PECRL2.BIT.PE7MD = 0x4;

PFC.PEIORL.BIT.B6       = 0x0;
PFC.PECRL2.BIT.PE6MD = 0x4;

MTU2.TSTR.BIT.CST3 = 0x1;            => Enable timer for PWM module for Inverter
MTU2.TSTR.BIT.CST4 = 0x1;            => Enable timer for PWM module for Inverter
MTU2.TSTR.BIT.CST2 = 0x1;            => Enable timer for PWM module for PLL
```

The figure 8 shows the flow chart of the operations performed by the software.

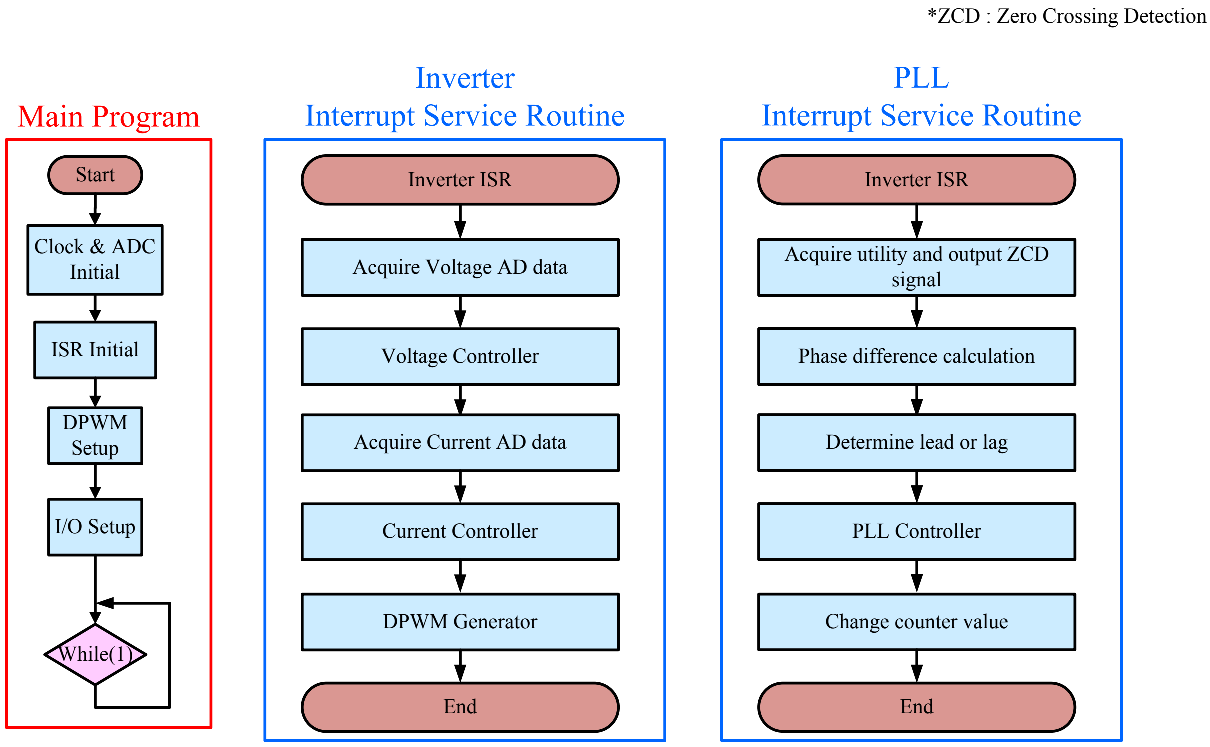


Figure 8 Flow chart for Inverter

6. Experimental Result

Line mode :

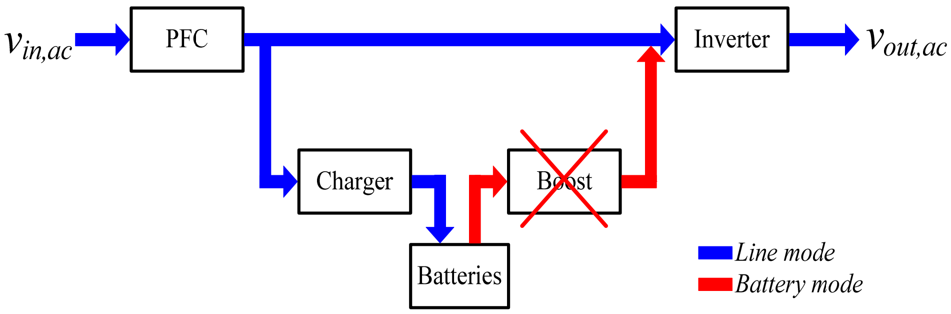


Figure 9 Block diagram of Online UPS in line mode

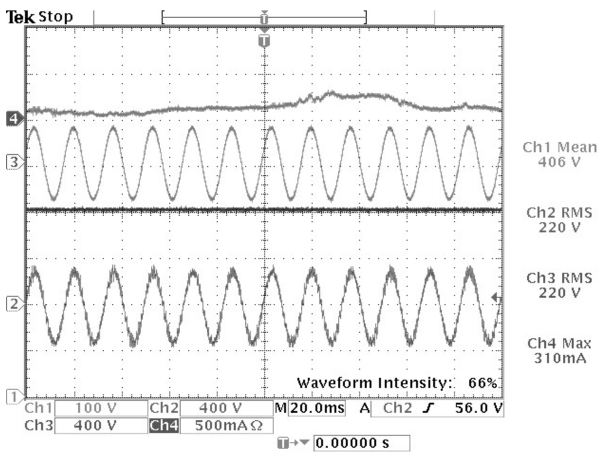


Figure 10 Waveform of line mode

Ch1 : PFC output voltage (100 V/div)

Ch2 : Inverter output voltage (400 V/div)

Ch3 : PFC input voltage (400 V/div)

Ch4 : Battery charge current (500 mA/div)

Battery mode :

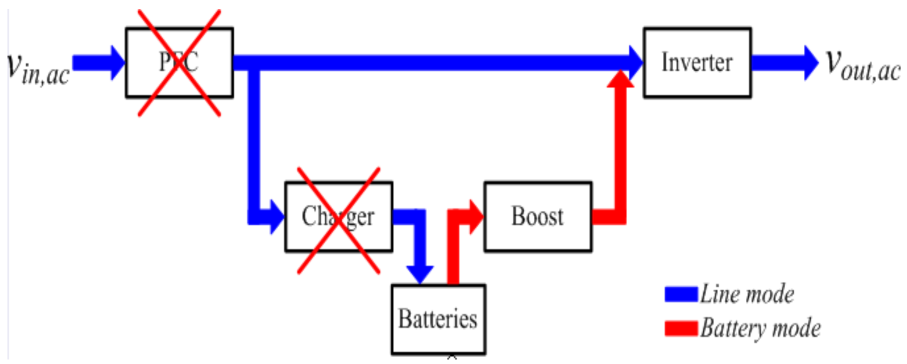


Figure11 Block diagram of Online UPS in battery mode

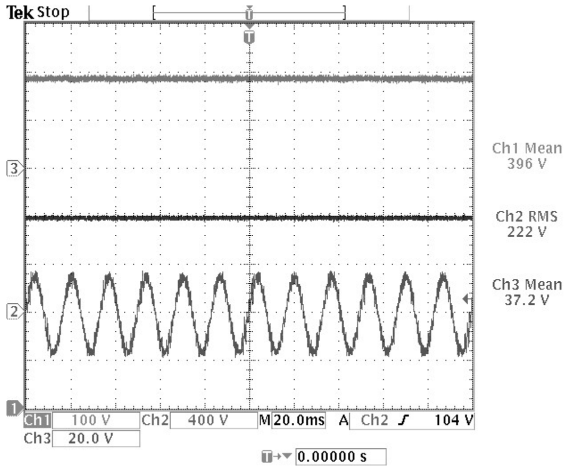


Figure 12 Waveform of line mode

Ch1 : Boost output voltage (100 V/div)
Ch2 : Inverter output voltage (400 V/div)
Ch3 : Battery voltage (20 V/div)

Website and Support

Renesas Electronics Website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Sep.30.10	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

RENESAS

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
7F, No. 363 Fu Shing North Road Taipei, Taiwan, R.O.C.
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141