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SH7211 Group

SCIF Clocked Synchronous Serial Data Transmit and Receive

Introduction

This application note describes an example of setting up serial data transmit and receive using the transmit FIFO data empty interrupt source and receive FIFO data full interrupt source of the serial communication interface with FIFO (SCIF) built into the SH7211.

Target Device

SH7211

Contents

1. Preface

1.1 Specifications

This application note describes the use of clocked synchronous serial transfer with FIFO to transmit and receive 256 bytes of data. Figure 1 shows an overview.

- Channel 1 of the SCIF is used.
- The transfer format of the transmit and receive data has a fixed 8-bit data length.
- The bit rate is 100 kilobits per second.
- There are eight receive triggers, and the receive FIFO data full interrupt source is used to receive 256 bytes of data.
- There are eight transmit triggers, and the transmit FIFO data empty interrupt source is used to transmit 256 bytes of data.
- Transmit and receive operation stops when transmission and reception of 256 bytes of data completes.

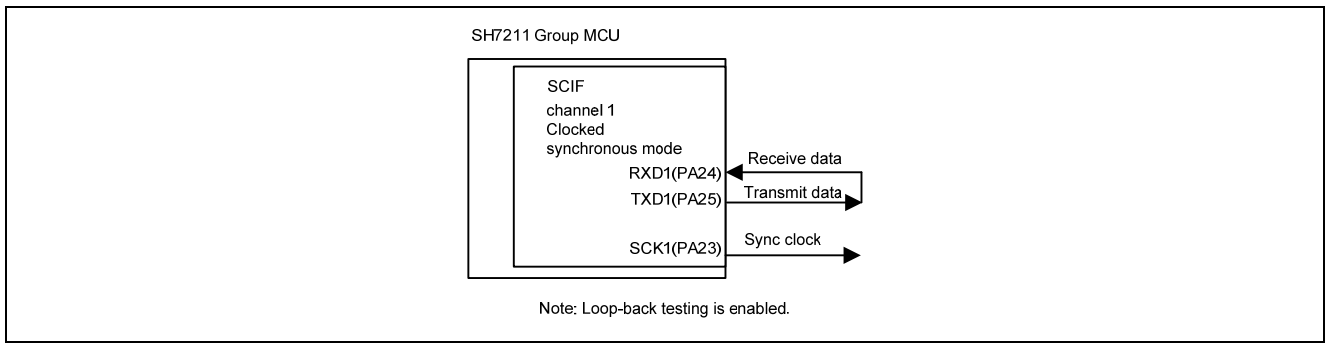

Figure 1 Clocked Synchronous Serial Data Transmit and Receive Operation with FIFO

1.2 Module Used

Serial communication interface with FIFO (SCIF channel 1)

1.3 Applicable Conditions

MCU	SH7211
Operating frequency	Internal clock: Iϕ = 160 MHz Bus clock: Bϕ = 40 MHz Peripheral clock: Pϕ = 40 MHz MTU2S clock: Mϕ = 80 MHz AD clock: Aϕ = 40 MHz
MCU operating mode	Single-chip
Integrated development environment	High-performance Embedded Workshop Ver. 4.05.01.001 from Renesas Technology
C compiler	SuperH RISC Engine Family C/C++ Compiler Package Ver. 9.03 Release 00 from Renesas Technology
Compiler options	Default settings of High-performance Embedded Workshop (-cpu=sh2a -include="$(WORKSPDIR)¥inc" -object="$(CONFIGDIR) ¥$(FILELEAF).obj" -debug -gbr=auto -chgincpath -errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 –nologo)

2. Description of the Sample Application

In this sample application, the transmit FIFO data empty interrupt source and receive FIFO data full interrupt source of the serial communication interface with FIFO (SCIF) are used to transmit and receive serial data in clocked synchronous mode.

2.1 Operational Overview of Module Used

In clocked synchronous mode, the SCIF transmits and receives data in synchronization with clock pulses. This mode is suitable for high-speed serial communication. Within the SCIF, and transmitter and receiver blocks are independent, so full-duplex communication is possible while sharing the same clock. The transmitter and receiver are also buffered by 16-stage FIFOs, so continuous transmitting or receiving is possible by reading or writing data while transmitting or receiving is in progress. In clocked synchronous serial communication, each data bit is output on the communication line from one falling edge of the sync clock to the next. Data is guaranteed valid at the rising edge of the sync clock. In each character, the serial data bits are transmitted in order from the LSB (first) to the MSB (last). After output of the MSB, the communication line remains in the state of the MSB. In clocked synchronous mode, the SCIF receives data by synchronizing with the rising edge of the sync clock.

For details on the SCIF, see the Serial Communication Interface with FIFO (SCIF) section in the *SH7211 Group Hardware Manual* (RJJ09B0338).

Table 1 gives an overview of the serial communication interface with FIFO (SCIF). Figure 2 is a block diagram of the SCIF.

Table 1 Clocked Synchronous Serial Communication

Item	Description
Number of channels	3 channels (channels 0 to 3)
Clock sources	Internal/external clock selection supported Internal clock: Clock produced by baud rate generator External clock: Clock input on SCK pin
Data format	Transfer data length: 8 bits, fixed No parity bit may be affixed.
Bit rate	Internal clock selected: 500 bps to 2 Mbps (when Pϕ = 40 MHz) External clock selected: Max. 3.3 Mbps (when Pϕ = 40 MHz and external clock input frequency is 3.3 MHz)
Error detection	Overrun error
Interrupt request	Transmit FIFO empty interrupt (TXI) Receive FIFO data full interrupt (RXI) Receive error interrupt (ERI) Break interrupt (BRI)

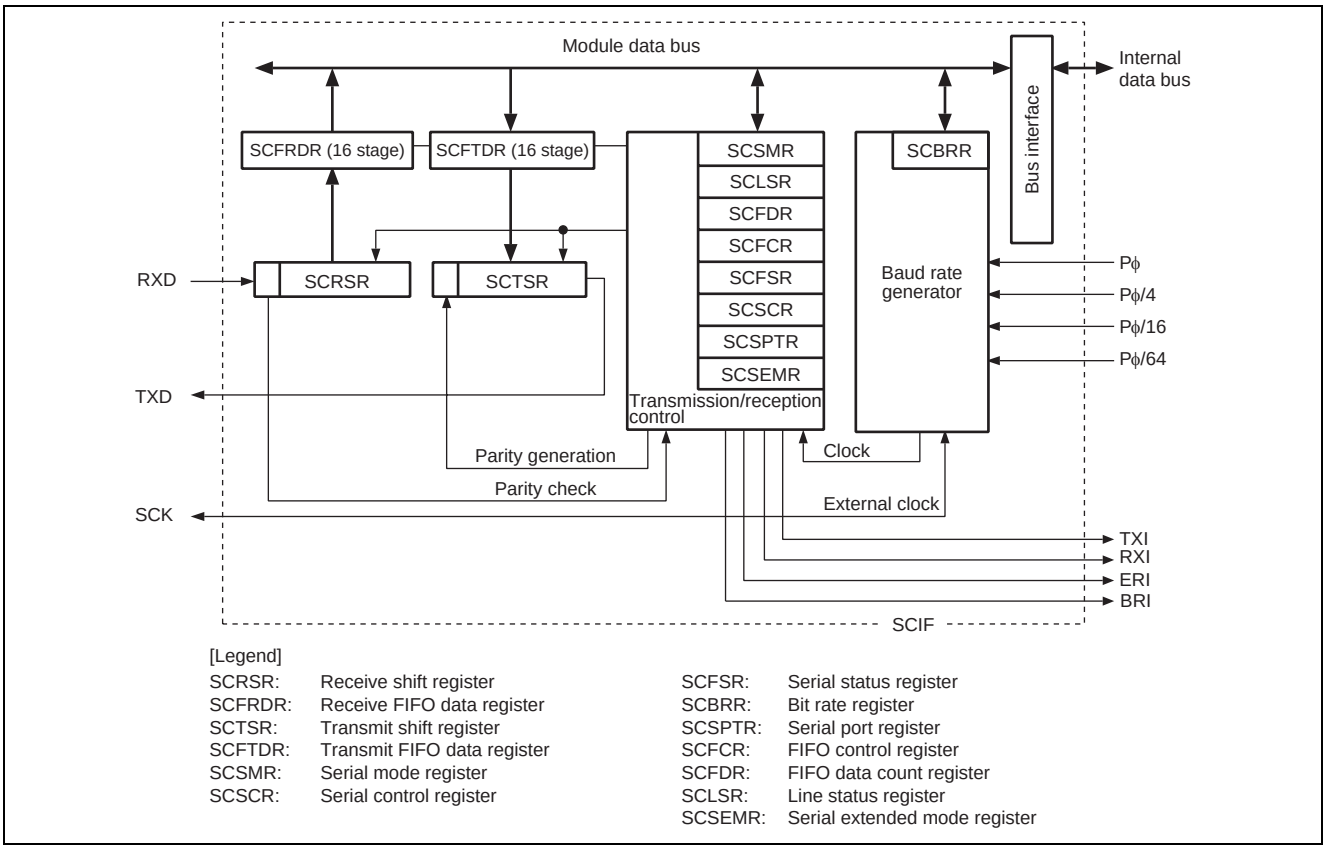

Figure 2 Block Diagram of SCIF

The register functions of the serial communication interface with FIFO (SCIF) are as follows.

- The receive shift register (SCRSR) is a register for receiving serial data. The SCIF sets in SCRSR the serial data bit values input on the RXD pin in the order received, starting from the LSB (bit 0), and the data is then converted into parallel format. When reception of one byte of data completes, the data is transferred automatically to the receive FIFO data register (SCFRDR). The CPU cannot perform direct read or write access to SCRSR.
- The receive FIFO data register (SCFRDR) is an 8-bit, 16-stage FIFO register that stores received serial data. When reception of one byte of serial data finishes, the received serial data is transferred from the receive shift register (SCRSR) to SCFRDR, completing the receive operation. Receive operation can proceed continuously until 16 bytes of data have been stored. The CPU can read from SCFRDR but cannot write to it. Reading the receive FIFO data register when it contains no receive data returns an undefined value. When the SCFRDR register is full of receive data, subsequently received serial data is lost.
- The transmit shift register (SCTSR) is a register for transmitting serial data. The SCIF first transfers transmit data from the transmit FIFO data register (SCFTDR) into SCTSR, then transmits the data serially from the TXD pin, LSB (bit 0) first. After transmitting one byte of data, the SCIF automatically transfers the next byte of transmit data from SCFTDR into SCTSR and starts transmitting again. The CPU cannot perform direct read or write access to SCTSR.
- The transmit FIFO data register (SCFTDR) is an 8-bit, 16-stage FIFO register that stores data for serial transmission. When the SCIF detects that the transmit shift register (SCTSR) is empty, it moves transmit data written to SCFTDR into SCTSR and starts serial transmission. Continuous serial transmission is performed until there is no transmit data left in SCFTDR. The CPU can write to SCFTDR at all times. When SCFTDR is full of transmit data (16 bytes), no more data can be written to it. If writing of new data is attempted, the data is ignored.
- The serial mode register (SCSMR) is a 16-bit register that specifies the SCIF serial communication format and selects the clock source for the baud rate generator. The CPU can always read and write to SCSMR.
- The serial control register (SCSCR) is a 16-bit register that operates the SCIF transmitter and receiver, enables and disables interrupt requests, and selects the transmit and receive clock source. The CPU can always read and write to SCSCR.
- The serial status register (SCFSR) is a 16-bit register. The upper 8 bits indicate the receive error count for the receive FIFO data register, and the lower 8 bits are status flags indicating SCIF operating state. The CPU can always read and write to SCFSR, but cannot write 1 to the status flags ER, TEND, TDFE, BRK, RDF, and DR. These flags can be cleared to 0 only if they have first been read as 1. The FER and PER flags are read-only bits that cannot be written to.
- The bit rate register (SCBRR) is an 8-bit register that together with the baud rate generator clock source selected by bits CKS1 and CKS0 in the serial mode register (SCSMR), determines the serial transmit/receive bit rate. The CPU can always read and write to SCBRR. SCBRR is initialized to H'FF by a power-on reset.
- The FIFO control register (SCFCR) is a 16-bit register that resets the data count of the transmit and receive FIFO data registers and sets the trigger data count. It also contains an enable bit for loop-back testing. SCFCR can always be read and written to by the CPU.
- The FIFO data count register (SCFDR) is a 16-bit register that indicates the quantity of data stored in the transmit FIFO data register (SCFTDR) and the receive FIFO data register (SCFRDR). The upper 8 bits indicate the transmit data count in SCFTDR, and the lower 8 bits indicate the receive data count in SCFRDR. SCFDR can always be read by the CPU.
- The line status register (SCLSR) is a 16-bit register that can always be read and written to by the CPU, but the CPU cannot write 1 to the ORER flag. This flag can be cleared to 0 only if it has first been read as 1.

2.2 Operation of the Sample Program

Table 2 gives the setting conditions for transmit and receive operation in clocked synchronous mode.

Table 2 Settings for Transmit and Receive Operation in Clocked Synchronous Mode

Item	Description
Channel in use	SCIF channel 1
Pins in use	RXD1 (PA24): Receive data input pin TXD1 (PA25): Transmit data output pin SCK1 (PA23): Sync clock output pin
Communication mode	Clocked synchronous mode
Communication speed	100 kbps
Transmit and receive data	256 bytes
Data length	8 bits
Bit order	LSB first
Sync clock	Internal clock/SCK pin used for sync clock output
Receive trigger	8
Transmit trigger	8
Interrupts	Transmit FIFO data empty interrupt (TXI) Receive FIFO data full interrupt (RXI) Break interrupt (BRI)
Loop-back testing	Enabled (TXD1 and RXD1 pins connected internally)

Figure 3 shows transmit and receive operation. The sample program transmits 256 bytes of transmit data. The loop-back testing function is enabled, so the transmit data is received unmodified. Transmit and receive operation ends after transmission and reception of the 256 bytes completes.

When transmit and receive operation starts, a transmit FIFO empty interrupt is generated, indicating that the amount of data stored in the transmit FIFO data register (SCFTDR) is less than 8 bytes. The handler for this interrupt writes transmit data to SCFTDR. The transmit data is transferred to the transmit shift register (SCTSR), after which it is converted into serial data and output by TXD1.

The serial data is received via RXD1, converted into parallel data by the receive shift register (SCRSR), and transferred to the receive FIFO data register (SCFRDR) one byte at a time. When 8 bytes of data are stored in SCFRDR, a receive FIFO data full interrupt is generated. The handler for this interrupt moves the receive data from SCFRDR to the receive buffer.

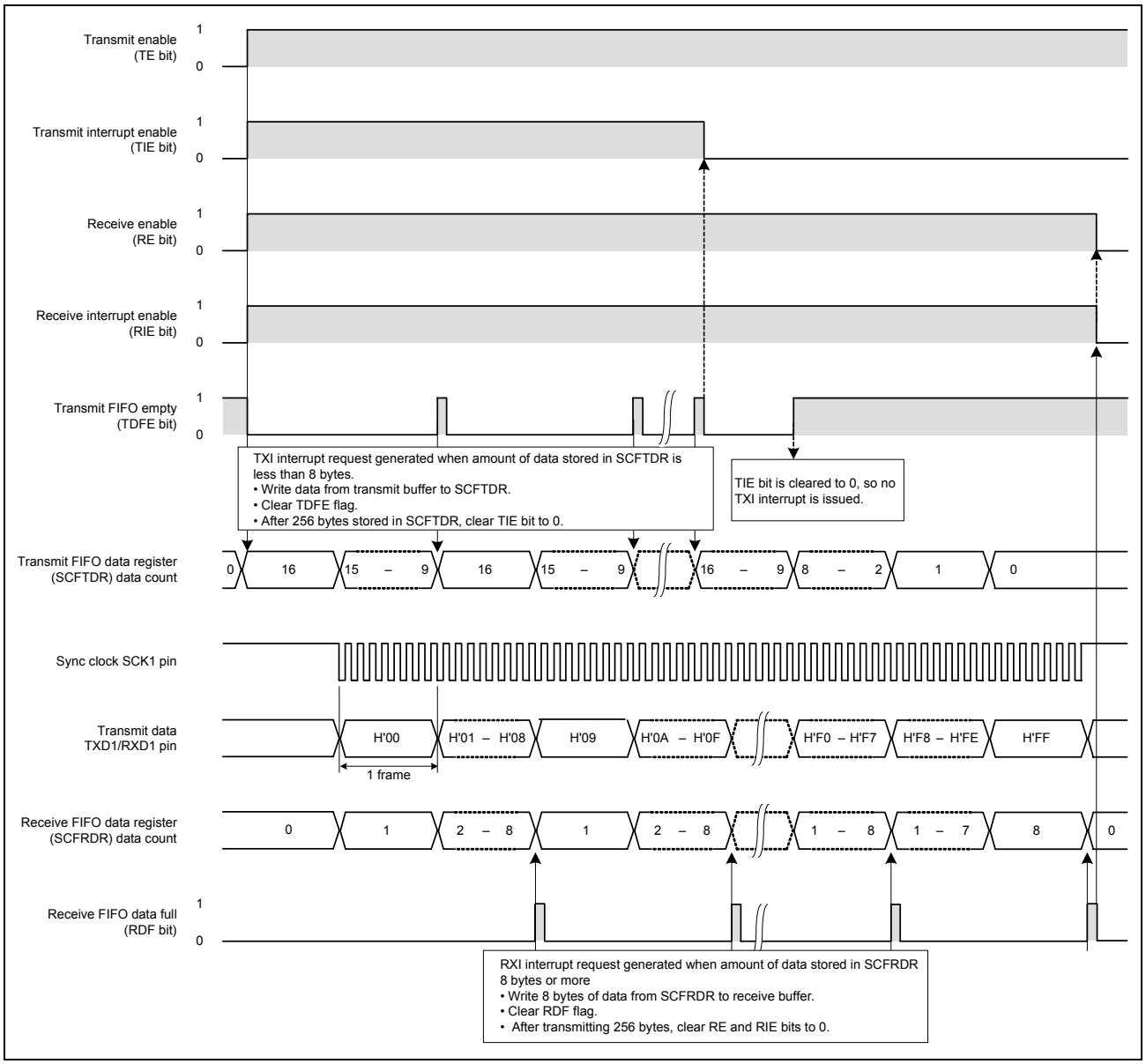

Figure 3 Transmit and Receive Operation

2.3 Configuration of the Sample Program

2.3.1 Description of Functions

Table 3 lists the functions used in this sample program.

Table 3 Functions Used

Function Name	Label	Description
Main	main ()	Initializes other modules Initializes serial communication interface with FIFO (SCIF) Enables SCIF transmit and receive operation
Standby setting	stbcr_init ()	Makes setting to release SCIF from standby
Initialization of PFC	pfc_init ()	Initializes the pin function controller (PFC) Selects SCIF pin functions
Initialization of SCIF	scif_init()	Initializes the SCIF
SCIF transmit FIFO data empty interrupt	Int_scif_txif()	Handles the SCIF transmit FIFO data empty interrupt
SCIF receive FIFO data full interrupt	Int_scif_rxif ()	Handles the SCIF receive FIFO data full interrupt
SCIF break interrupt	Int_scif_brif ()	Handles the SCIF break interrupt (overrun error handler)

2.3.2 Variable Usage

Table 4 lists the variables used in the sample program.

Table 4 Variable Usage

Label Name	Description	Name of Employing Module
unsigned int DataNum	Transmit data count	Int_scif_txif()
unsigned long Trns_Count	Transmit completed data count	
unsigned char Trns _Data[256]	Transmit buffer	
unsigned long Txif_Count	Transmit FIFO data empty interrupt count	
unsigned long Rcv_Count	Receive completed data count	Int_scif_rxif ()
unsigned char Rcv_Data[256]	Receive buffer	
unsigned long Rxif_Count	Receive FIFO data full interrupt count	
unsigned long Brif_Count	Break interrupt count	Int_scif_brif ()

2.4 Procedure for Setting the Modules Used

The following subsections describe the flow of processing by the sample program.

2.4.1 Main Function

Figure 4 shows the flow of processing by the main function.

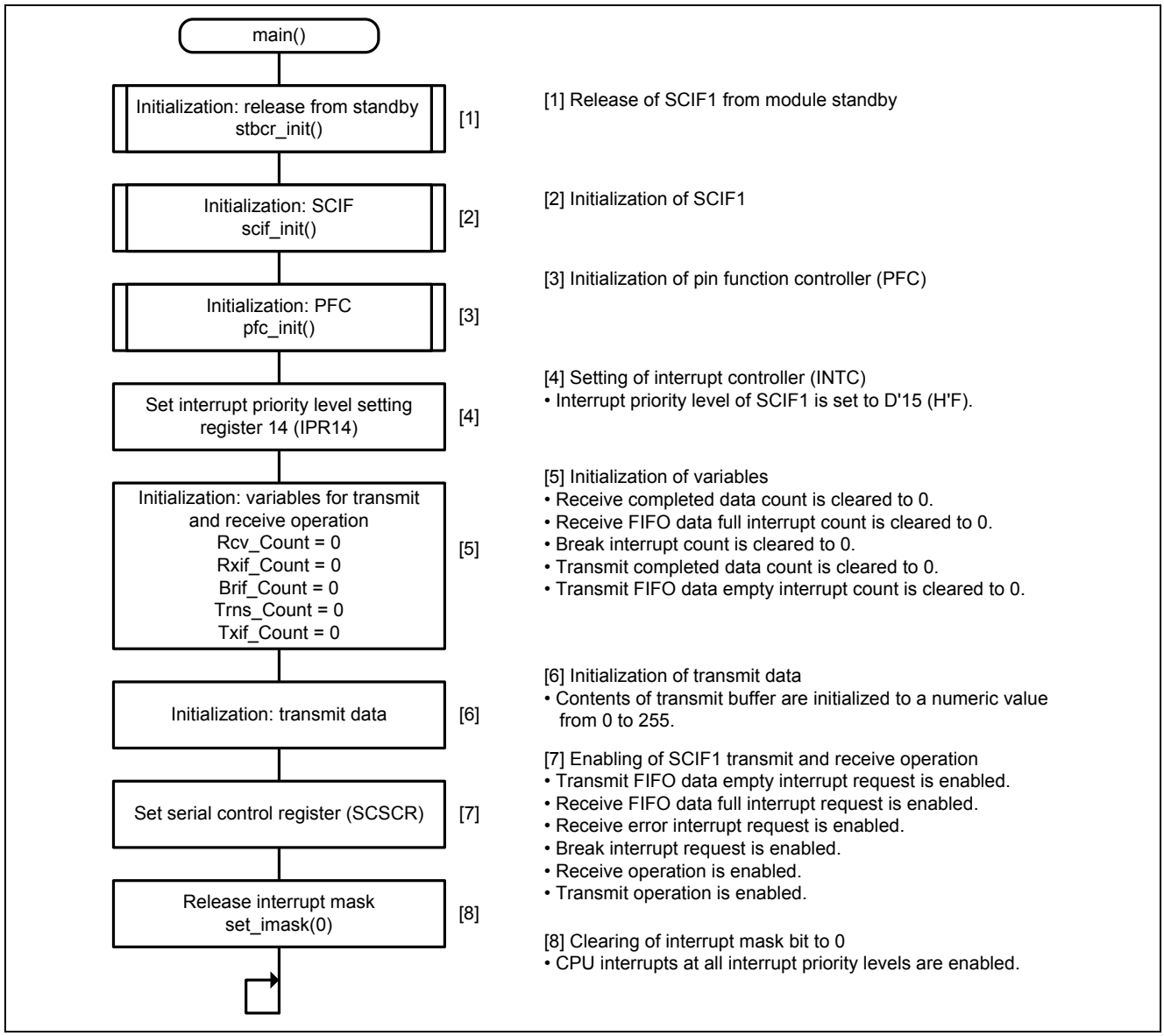

Figure 4 Processing by Function main

2.4.2 Initialization for Standby

Figure 5 shows the flow of processing for release from standby.

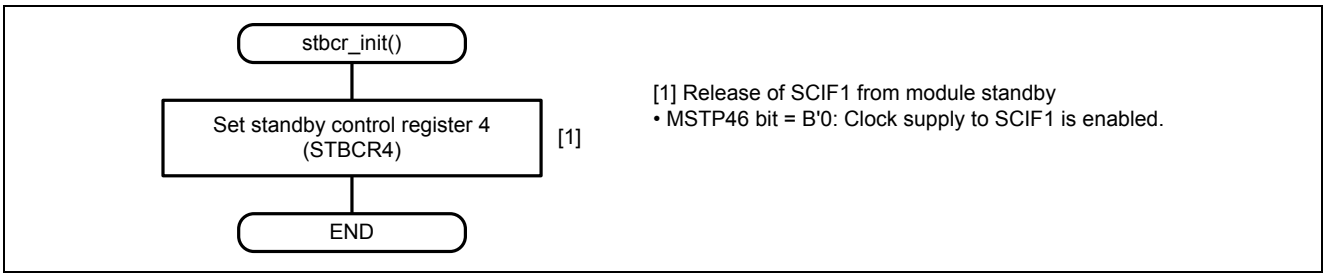

Figure 5 Initialization: Release from Standby

2.4.3 Initialization of Pin Function Controller (PFC)

Figure 6 shows the flow for initialization of the pin function controller (PFC).

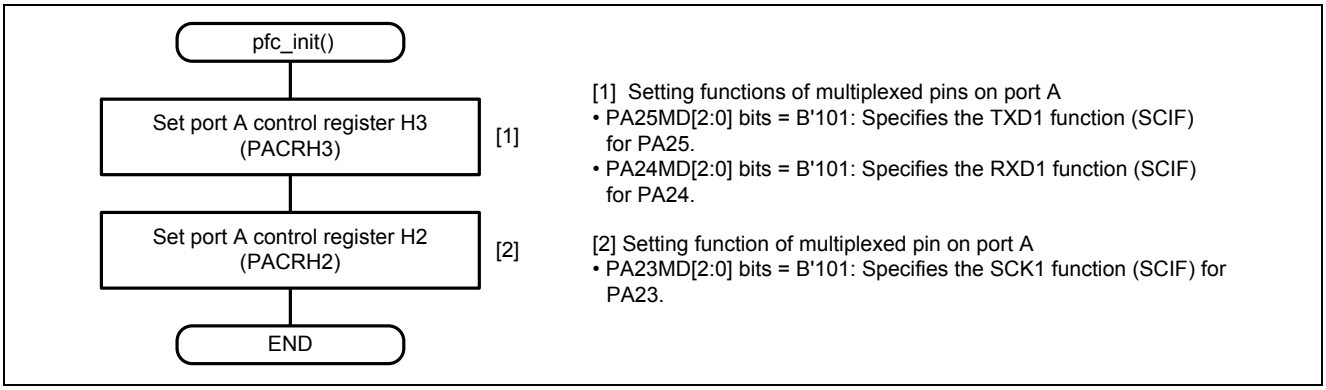

Figure 6 Initialization of Pin Function Controller (PFC)

2.4.4 Initialization of SCIF

Figure 7 shows the flow for initialization of the SCIF.

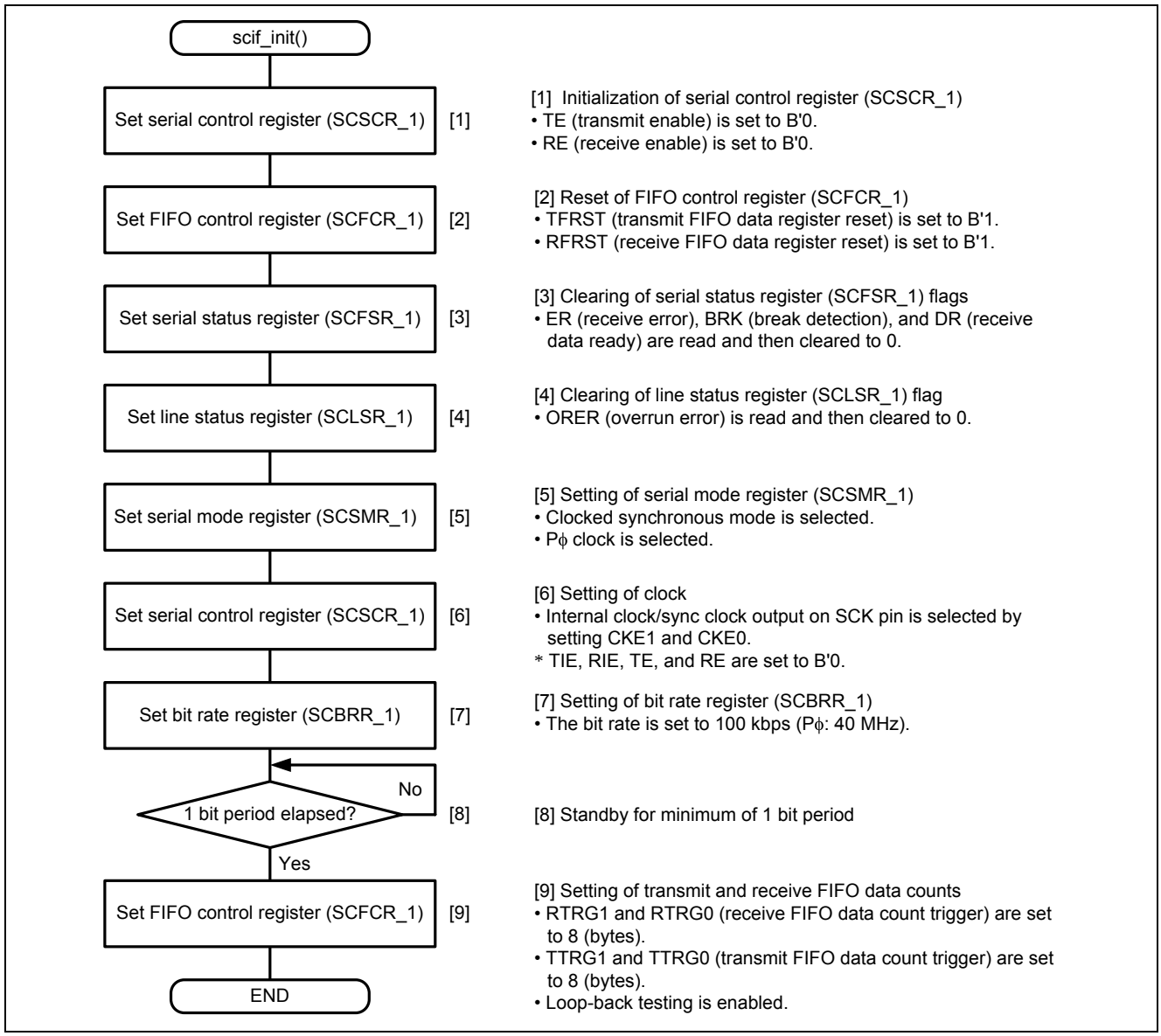

Figure 7 Initialization of SCIF

2.4.5 Handling of the SCIF Receive FIFO Data Full Interrupt

Figure 8 shows the flow for handling the SCIF receive FIFO data full interrupt.

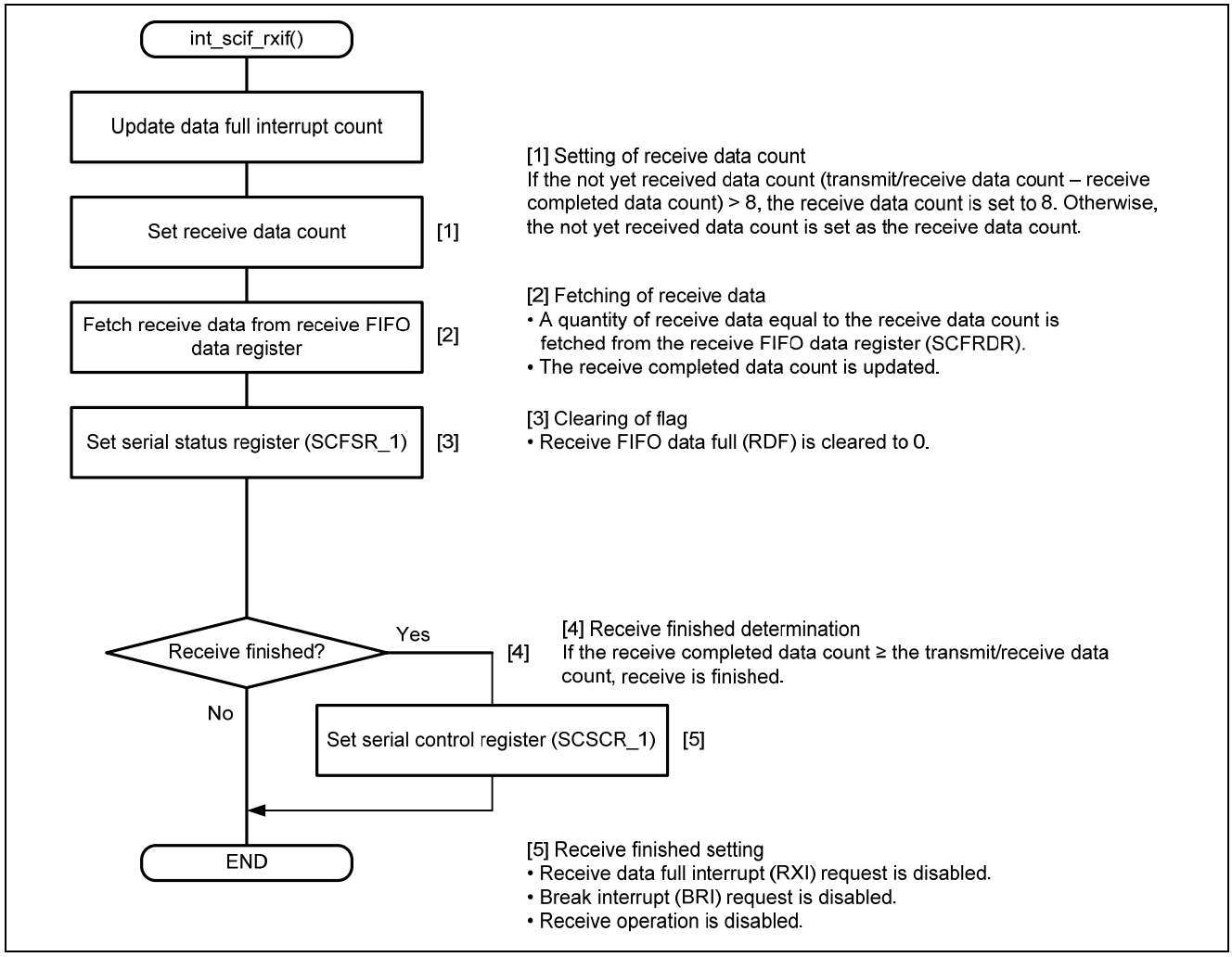

Figure 8 Handling of the SCIF Receive FIFO Data Full Interrupt SCIF

2.4.6 Handling of the SCIF Break Interrupt (Overrun Error Handler)

Figure 9 shows the flow for handling the SCIF break interrupt (overrun error handler).

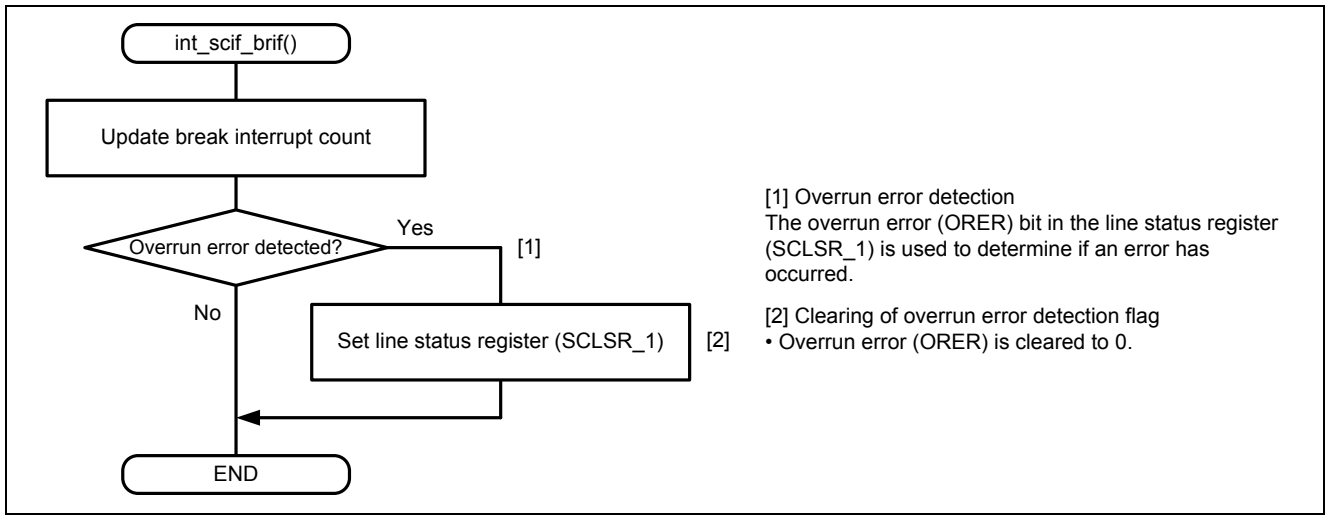

Figure 9 Handling of the SCIF Break Interrupt (Overrun Error Handler)

2.4.7 Handling of the SCIF Transmit FIFO Data Empty Interrupt

Figure 10 shows the flow for handling the SCIF transmit FIFO data empty interrupt.

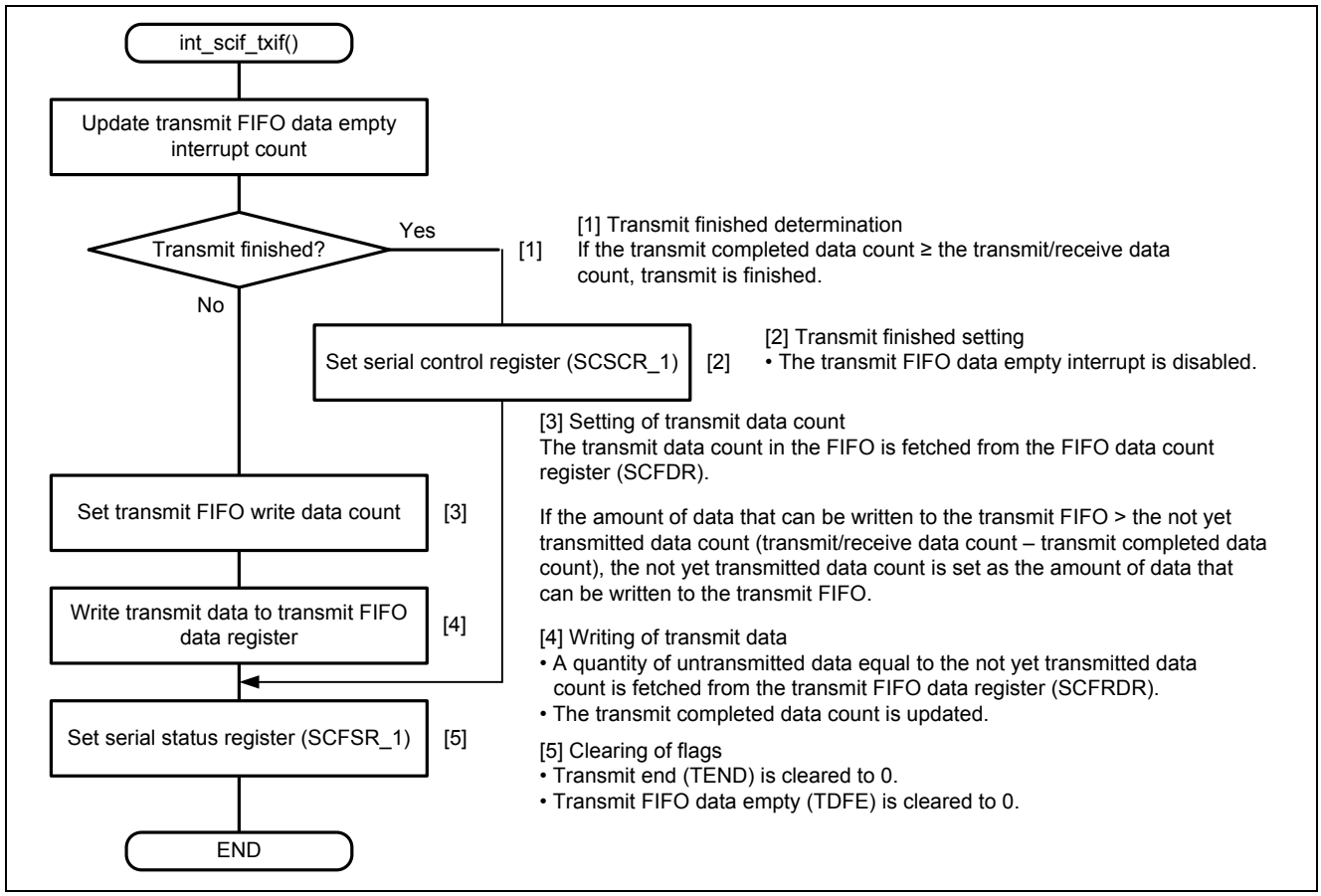

Figure 10 Handling of the SCIF Transmit FIFO Data Empty Interrupt

2.5 Settings of Registers in the Sample Program

The following describes the settings of registers used in the sample program.

2.5.1 Clock Pulse Generator (CPG)

Table 5 gives a list of settings for registers of the clock pulse generator (CPG).

Table 5 Clock Pulse Generator (CPG)

Register Name	Address	Setting	Description
Frequency control register (FRQCR)	H'FFFE0010	H'1303	Specifies clock output settings and operating frequency division ratios • CKOEN = B'1: CK pin fixed low level • STC[1:0] = B'11: ×2, PLL circuit 1 • IFC[2:0] = B'000: ×1, internal clock (Iϕ) • RNGS = B'0: High-frequency mode • PFC[2:0] = B'011: ×1/4, peripheral clock (Pϕ)

2.5.2 Power-Down Modes

Table 6 gives register settings related to low-power modes.

Table 6 Power-Down Modes

Register Name	Address	Setting	Description
Standby control register 4 (STBCR4)	H'FFFE040C	H'B6	Settings for the operation of various modules • MSTP47 = B'1: Clock supply to SCIF0 halted. • MSTP46 = B'0: SCIF1 runs. • MSTP45 = B'1: Clock supply to SCIF2 halted. • MSTP44 = B'1: Clock supply to SCIF3 halted. • MSTP42 = B'1: Clock supply to CMT halted. • MSTP41 = B'1: Clock supply to WAVEIF halted.

2.5.3 Serial Communication Interface with FIFO (SCIF)

Table 7 gives a list of settings for registers of the serial communication interface with FIFO (SCIF).

Table 7 Serial Communication Interface with FIFO (SCIF)

Register Name	Address	Setting	Description
Serial mode register_1 (SCSMR_1)	H'FFFE8800	H'0080	Sets operating mode of SCIF_1. • C/A = B'1: Clocked synchronous mode • CHR = B'0: 8-bit data • PE = B'0: Parity bit affixed and checking disabled • STOP = B'0: 1 stop bit • CKS[1:0] = B'00: Pϕ clock
Bit rate register_1 (SCBRR_1)	H'FFFE8804	H'61	Bit rate: 100 kbps
Serial control register_1 (SCSCR_1)	H'FFFE8808	H'00F0	Initial settings • TIE = B'1: Transmit FIFO data empty interrupt (TXI) request enabled • RIE = B'1: Receive FIFO data full interrupt request (RXI), receive error interrupt request (ERI), and break interrupt request (BRI) request enabled • TE = B'1: Send operation enabled • RE = B'1: Receive operation enabled • REIE = B'0: Receive error interrupt request (ERI) and break interrupt request (BRI) request disabled • CKE[1:0] = B'00: Internal clock/SCK pin sync clock output
Serial status register_1 (SCFSR_1)	H'FFFE8810	H'0060	Initial values • PER[3:0] = Parity error count • FER[3:0] = Framing error count • ER = B'0: Receive in progress, or normal receive end • TEND = B'1: Transmit end • TDFE = B'1: Data count written to SCFTDR is smaller than specified transmit trigger. • BRK = B'0: No break signal • FER = B'0: No framing error • PER = B'0: No parity error • RDF = B'0: SCFRDR receive data count is smaller than specified trigger count. • DR = B'0: Receive in progress, or no receive data remains in SCFRDR after successful receive end.
FIFO control register_1 (SCFCR_1)	H'FFFE8818	H'0081	• RTRG[1:0] = B'10: Receive FIFO data trigger count = 8 • TTRG[1:0] = B'00: Transmit FIFO data trigger count = 8 • TFRST = B'0: Transmit FIFO data register reset disabled • RFRST = B'0: Receive FIFO data register reset disabled • LOOP = B'1: Loop-back testing enabled

2.5.4 Interrupt Controller (INTC)

Table 8 gives a list of settings for registers of the interrupt controller (INTC).

Table 8 Interrupt Controller (INTC)

Register Name	Address	Setting	Description
Interrupt priority level setting register 14 (IPR14)	H'FFFE0C10	H'0F00	Selects interrupt priority (level 0 to 15). • Bits 15 to 12 = B'0000: SCIF_0 interrupt level = 0 • Bits 11 to 8 = B'1111: SCIF_1 interrupt level = 15 • Bits 7 to 4 = B'0000: SCIF_2 interrupt level = 0 • Bits 3 to 0 = B'0000: SCIF_3 interrupt level = 0

2.5.5 Pin Function Controller (PFC)

Table 9 gives a list of settings for registers of the pin function controller (PFC).

Table 9 Pin Function Controller (PFC)

Register Name	Address	Setting	Description
Port A control register H3 (PACRH3)	H'FFFE380A	H'0055	Specifies functions of multiplexed pins on port A. • PA25MD[2:0] = B'101: Specifies TXD1 output (SCIF) for PA25. • PA24MD[2:0] = B'101: Specifies RXD1 input (SCIF) for PA24.
Port A control register H2 (PACRH2)	H'FFFE380C	H'5000	Specifies functions of multiplexed pins on port A. • PA23MD[2:0] = B'101: Specifies SCK1 output (SCIF) for PA23.

3. Documents for Reference

- Hardware Manual
  SH7211Group Hardware Manual (RJJ09B0338)
  The most up-to-date version of this document is available on the Renesas Technology Website.
- Software Manual
  SH-2A/SH2A-FPU Software Manual (RJJ09B0086)
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