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# SH7211 Group

## BSC SDRAM Interface Settings Examples

### Introduction

This application note introduces the SDRAM interface functions of the SH7211 bus state controller (BSC) SDRAM interface and presents a connection example.

### Target Devices

SH7211

### Contents

# 1. Preface

## 1.1 Specifications

- This application uses a 16 MB (8M words × 16 bits) SDRAM, and connects to it with a 16-bit bus width.
- This application uses the SH7211 SDRAM interface functions and initializes the SDRAM.

## 1.2 Functions Used

- Bus state controller (BSC)

## 1.3 Application Conditions

- Microcontroller: SH7211
- Operating frequency: Internal clock - 160 MHz
  Bus clock - 40 MHz
  Peripheral clock - 40 MHz
  MTU2S clock - 80 MHz
  A/D converter clock - 40 MHz
- C compiler: Renesas Technology Corp.
  SuperH RISC Engine Family C/C++ Compiler Package Version 9.01, Release 01
- Compiler options: The default settings in the HEW file (-cpu=sh2a -debug -gbr=auto -chgincpath -global_volatile=0 -opt_range=all -infinite_loop=0 -struct_alloc=1 -nologo)

## 1.4 Related Application Notes

- The sample program in this document has been verified under the setting conditions in the SH7211 Initial Settings Application Note. Refer to that document in conjunction with this application note.

# 2. The Application Example

## 2.1 Operational Overview of the Functions Used

This application uses the SH7211's bus state controller (BSC) to control externally connected SDRAM. Table 1 lists the specifications of the SDRAM used in this application and figure 1 shows the memory map.

**Table 1 SDRAM Specifications**

| Item | SDRAM specification |
|---|---|
| Product No. | EDS1216AATA-75E |
| Bus width | 16 bits |
| Capacity | 2 MB (16 bits × 1 Mword) × 1 |
| Package | 48 pin TSOP (20 × 12mm) |

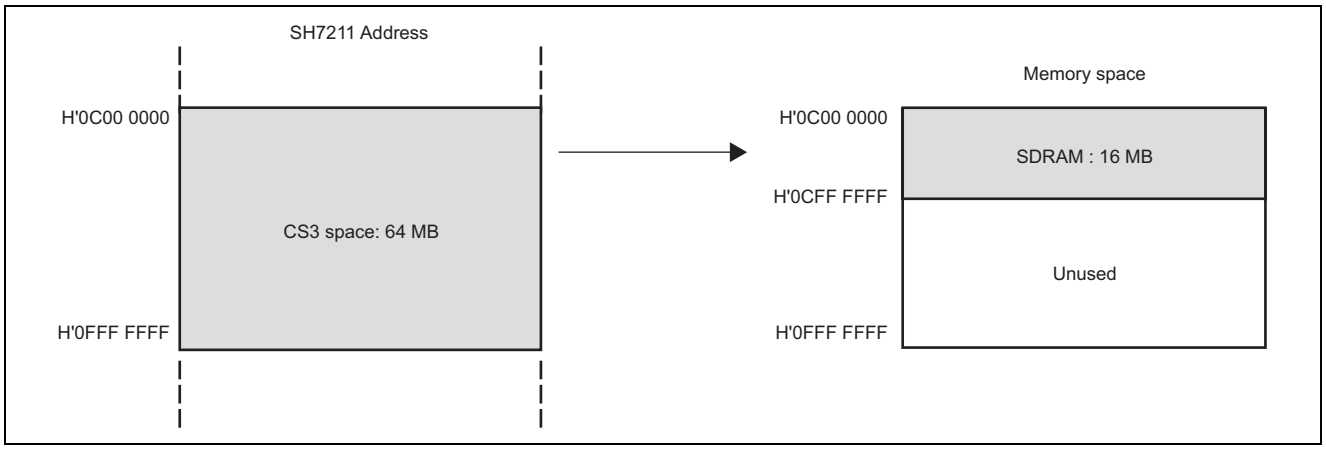



**Figure 1 SDRAM Related Memory Map**

Figure 2 shows a sample SDRAM connection circuit and table 2 lists the SH7211 pin functions. Since all pins are set to I/O port operation as the initial pin function, applications must use the pin function controller (PFC) to switch the pin functions as required.

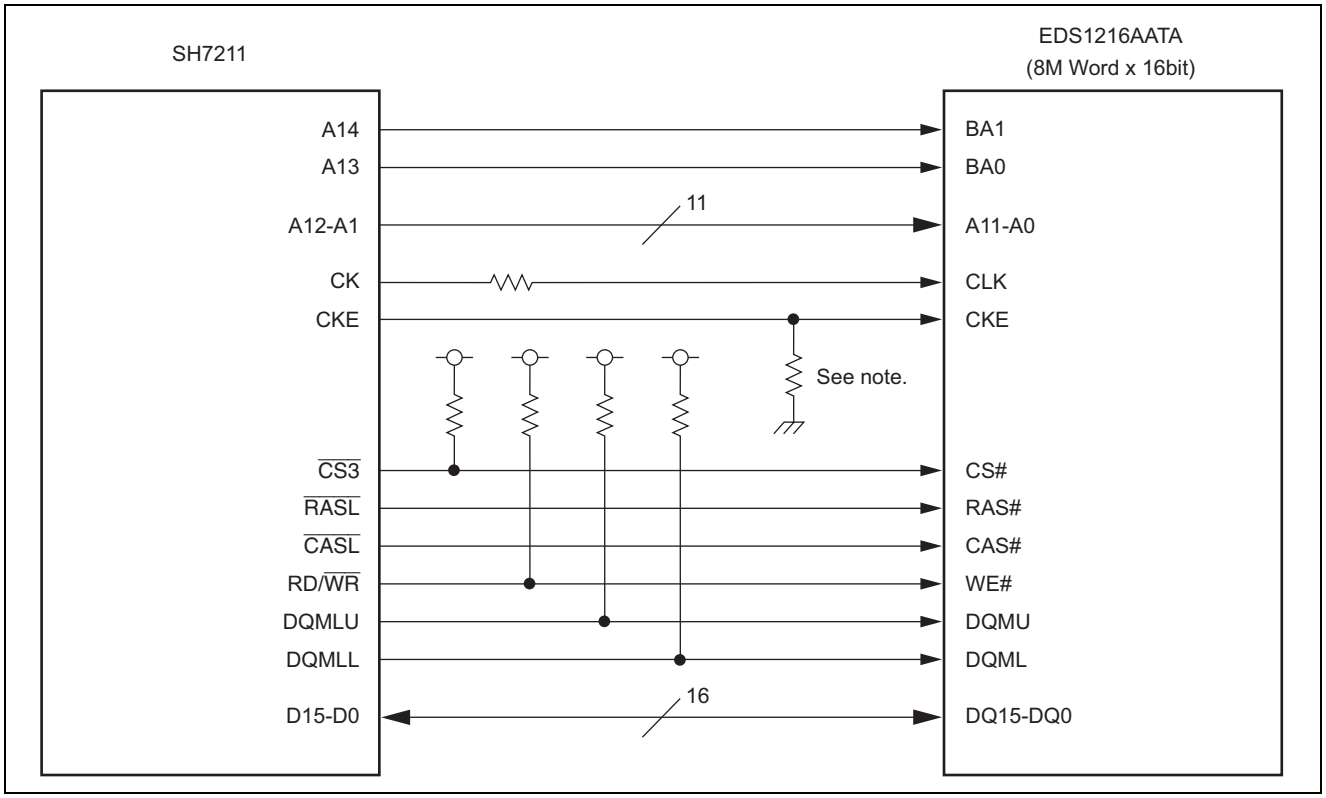



**Figure 2 SDRAM Connection Circuit Example**

**Table 2 SH7211 Pin Functions**

| SH7211 pin | I/O | Initial pin function | Function |
|---|---|---|---|
| A14 to A1 | Output | PA14 to PA1 | Address bus |
| D15 to D0 | I/O | PD15 to PD0 | Data bus |
| CK | Output | PB3 | Clock output |
| CKE | Output | PB4 | Clock enable (See note.) |
| $\overline{CS3}$ | Output | PB17 | Chip reset |
| $\overline{RASL}$ | Output | PB5 | RAS signal |
| $\overline{CASL}$ | Output | PB6 | CAS signal |
| $\overline{RD/WR}$ | Output | PB1 | Read or write signal |
| $\overline{DQMLU}$ | Output | PB9 | Byte write command for D15 to D8 |
| $\overline{DQMLL}$ | Output | PB8 | Byte write command for D7 to D0 |

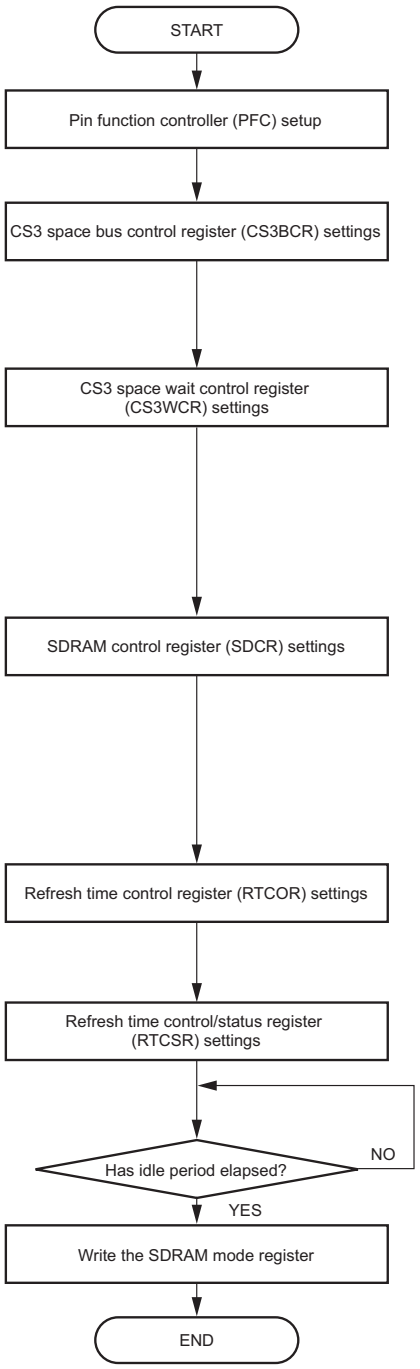
Note: The pin handling for the CKE pin differs depending on the SDRAM used.
This pin should be either pulled up or pulled down as required by the SDRAM actually used.

## 2.2 Setup Procedure for the Functions Used

Table 3 lists sample settings for the bus state controller. See chapter 8, Bus State Controller, in the SH7211 Group Hardware Manual for details on the BSC module. Figure 3 shows a bus state controller setup procedure example.

**Table 3 Sample Bus State Controller Settings**

| Register | Address | Value | Function |
|---|---|---|---|
| CS3 space bus control register (CS3BCR) | H'FFFC 0010 | H'1000 4400 | • IWW[2:0] = B'001<br>Inserts 1 idle cycle as the write-read/write-write interval idle<br>• TYPE[2:0]="B'100": SDRAM<br>• BSZ[1:0] = B'01: Bus width: 16 bits |
| CS3 space wait control register (CS3WCR) | H'FFFC 0034 | H'0000 0091 | • WTRP[1:0] = B'00<br>Precharge complete wait cycle count: No wait cycles<br>• WTRCD[1:0] = B'00<br>ACTV command -> READ/WRIT command interval wait cycle count: No wait cycles<br>• A3CL[1:0] = B'01<br>Area 3 CAS latency: 2 cycles<br>• TRWL[1:0] = B'10<br>WRIT(A) command -> auto precharge/PRE command cycle count: 2 cycles<br>• WRTC[1:0] = B'01<br>REF command/self refresh clear -> ACTV command cycle count: 3 cycles |
| SDRAM control register (SDCR) | H'FFFC 004C | H'0000 0809 | • RFSH = 1<br>Refresh control: Perform refresh operations<br>• RMODE = 0<br>Refresh control: Perform auto refresh operations<br>• BACTV = 0<br>Bank active mode: auto precharge mode<br>• A3ROW[1:0] = B'01<br>Area 3 row address bit length: 12 bits<br>• A3COL[1:0] = B'01<br>Area 3 column address bit length: 9 bits |
| Refresh time control/status register (RTCSR) | H'FFFC 0050 | H'A55A 0010 | • CKS[2:0] = B'010<br>Clock select: Bø/16<br>• RRC[2:0] = B'000<br>Refresh count: 1 |
| Refresh time constant register (RTCOR) | H'FFFC 0058 | H'A55A 0027 | *: The refresh request interval will be as follows when clock select is set to Bϕ/16.<br>1 cycle: 400 ns (400 MHz/16 = 2.5 MHz)<br>Refresh refresh interval for this SDRAM: 15.625 µs per operation (4096 refresh cycles every 64 ms)<br>15.625 µs/400 ns = 39 cycles/refresh count |




- PACRL4 to 1 :A14 to A1
- PDCRL4 to 1 :D15 to D0
- PBCRH1 :CS3
- PBCRL3 :DQMLL, DQMLU
- PBCRL2 :CKE, CASL, RASL
- PBCRL1 :RD/WR, CK

  Function: Multiplexed pin selection
- CS3BCR settings

  Functions
  - Inter-cycle idle insertion setting
  - Memory type: SDRAM
  - Endian specification
  - Data bus width setting
- CS3WCR settings

  Functions
  - Precharge complete wait cycle count setting
  - ACTV command -> READ(A)/WRIT(A) command interval wait cycle insertion setting
  - Area 3 CAS latency setting
  - Precharge activation wait cycle count setting
  - REF command/self precharge clear -> ACTV/REF/MRS command interval idle cycle count setting
- SDCR settings

  Functions
  - Deep power down mode setting for low-power SDRAMs
  - Refresh enable and execute method setting
  - Power down mode
  - Area 3 row address bit count
  - Area 3 column address bit count
- RTCOR settings *: There register is write protected (the upper 16 bits must be 0xa55a)

  Functions
  - Setting the refresh request interval for the SDRAM
  - Refresh count
- RTCSR settings *: There register is write protected (the upper 16 bits must be 0xa55a)

  Functions
  - Interrupt enable/disable setting during timer counting
  - Selection of the clock that increments the refresh timer counter (RTCNT)
  - Refresh count selection
- SDRAM requires certain amount of idle time when power is first applied.
- Write to the SDRAM mode register *: The set value is specified with the address value.

  Functions
  - Burst length setting
  - Wrap type setting
  - CAS latency setting

**Figure 3 Bus State Controller Setup Procedure (CS3 space)**

Figure 4 shows an SDRAM single read/write timing example when the bus clock is 40 MHz.

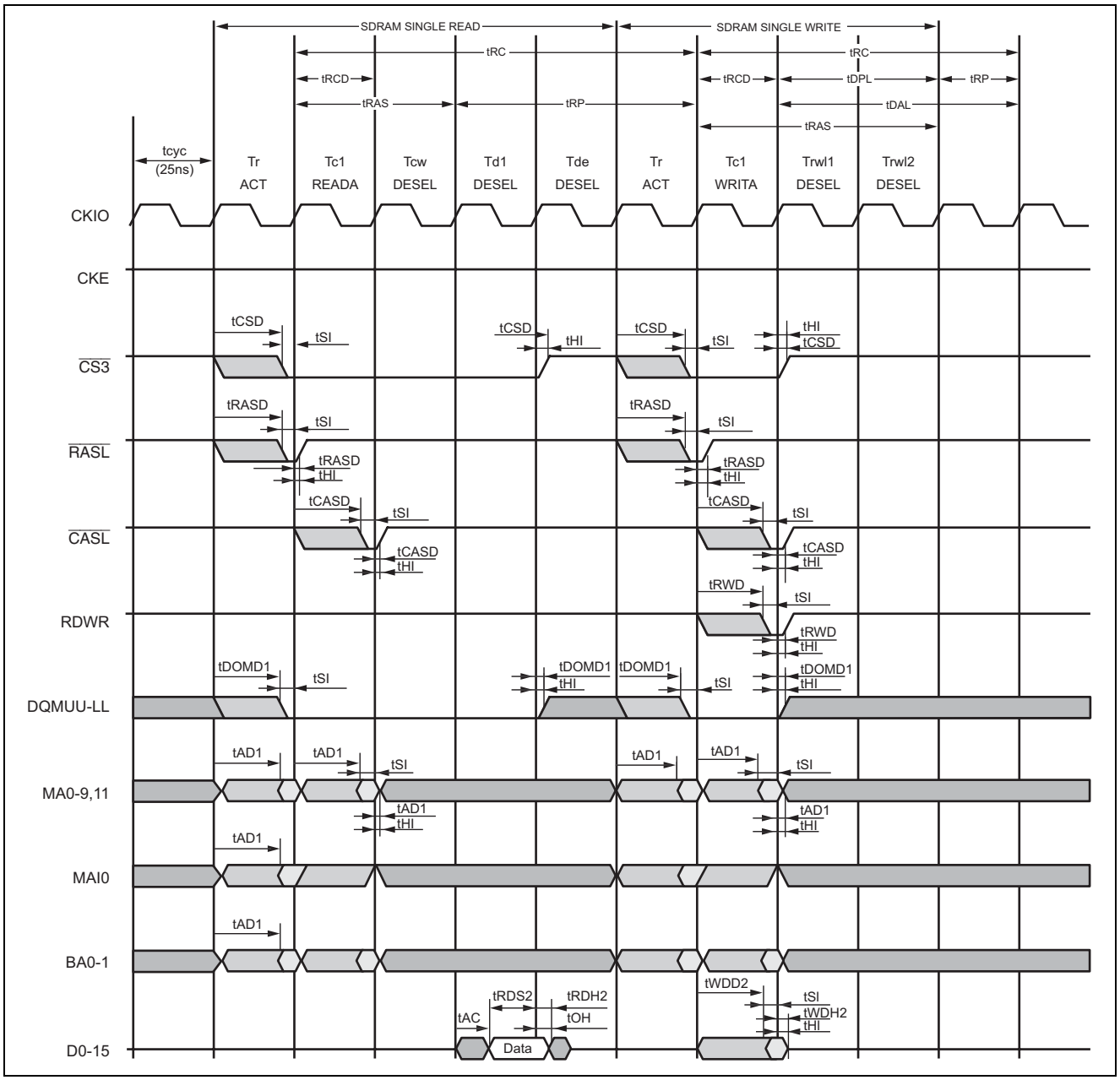



**Figure 4 SDRAM Single Read/Write Timing Example**

## 3. Sample Program

```
1       /*""FILE COMMENT""*****************************************************************
2       *
3       *       System Name : SH7211 Sample Program
4       *       File Name   : bsc_sdram.c
5       *       Version     : 1.00.02
6       *       Contents    : SH7211 SDRAM Initial Setting
7       *       Model       : M3A-HS11
8       *       CPU         : SH7211
9       *       Compiler    : SHC9.1.1.0
10      *       OS          : none
11      *
12      *       note        : <Notes>
13      *                     This sample program is provided for reference
14      *                     purposes; its operation is not guaranteed.
15      *                     This sample program may be used for reference
16      *                     purposes when developing user applications.
17      *
18      *                     <Caution>
19      *                     This sample programs are all reference,
20      *                     and no one to guarantee the operation.
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22      *                     reference when customers develop softwares.
23      *
24      *       Copyright (C) 2008 Renesas Technology Corp. All Rights Reserved
25      *       AND Renesas Solutions Corp. All Rights Reserved
26      *
27      *       history   : 2005.04.21 ver.1.00.00
28      *                 : 2005.06.01 ver.1.00.01
29      *                 : 2008.04.04 ver.1.00.02
30      *""FILE COMMENT END""*************************************************************/
31      #include "iodefine.h"
32
33      /* ==== Macro name definition ==== */
34
35      /* The address when writing in a SDRAM mode register */
36      #define SDRAM_MODE  (*(volatile unsigned short *)(0xfffc5440))
37
38      /* ==== Prototype declaration ==== */
39      void io_init_sdram(void);
40
```

**Figure 5 Sample Program Listing: bsc_sram.c (1)**

```
41      /*""FUNC COMMENT""*************************************************************
42      * ID                :
43      * Module outline    : SDRAM 16-bit bus width connection settings
44      *-----------------------------------------------------------------------------
45      * Include           : #include "iodefine.h"
46      *-----------------------------------------------------------------------------
47      * Declaration       : void io_init_sdram(void)
48      *-----------------------------------------------------------------------------
49      * Function          : The pin function controller (PFC) and
50      *                   : bus state controller (BSC) are set up to
51      *                   : enable access to the CS3 space SDRAM.
52      *-----------------------------------------------------------------------------
53      * Parameters        : None
54      *-----------------------------------------------------------------------------
55      * Return Values     : None
56      *-----------------------------------------------------------------------------
57      * Precaution        : Bit manipulations are used to set PFC so that
58      *                   : the PFC settings from other processes are not changed.
59      *""FUNC COMMENT END""*********************************************************/
60      void io_init_sdram(void)
61      {
62        volatile int j = 32000;     /* 200usec wait count @160MHz */
63
64        /* ==== PFC settings ==== */
65        PFC.PACRL4.BIT.PA14MD = 0x1;    /* Set A14 */
66        PFC.PACRL4.BIT.PA13MD = 0x1;    /* Set A13 */
67        PFC.PACRL4.BIT.PA12MD = 0x1;    /* Set A12 */
68        PFC.PACRL3.WORD = 0x1111;       /* Set A11-A8 */
69        PFC.PACRL2.WORD = 0x1111;       /* Set A7-A4 */
70        PFC.PACRL1.BIT.PA3MD = 0x1;     /* Set A3 */
71        PFC.PACRL1.BIT.PA2MD = 0x1;     /* Set A2 */
72        PFC.PACRL1.BIT.PA1MD = 0x1;     /* Set A1 */
73
74        PFC.PDCRL4.WORD = 0x1111;       /* Set D15-D12 */
75        PFC.PDCRL3.WORD = 0x1111;       /* Set D11-D8 */
76        PFC.PDCRL2.WORD = 0x1111;       /* Set D7-D4 */
77        PFC.PDCRL1.WORD = 0x1111;       /* Set D3-D0 */
78
79        PFC.PBCRL1.BIT.PB1MD  = 0x1;    /* Set RDWR */
80        PFC.PBCRL1.BIT.PB3MD  = 0x1;    /* Set CK */
81        PFC.PBCRL2.BIT.PB4MD  = 0x1;    /* Set CKE */
82        PFC.PBCRL2.BIT.PB5MD  = 0x1;    /* Set RASL */
83        PFC.PBCRL2.BIT.PB6MD  = 0x1;    /* Set CASL */
84        PFC.PBCRL3.BIT.PB8MD  = 0x1;    /* Set DQMLL */
85        PFC.PBCRL3.BIT.PB9MD  = 0x1;    /* Set DQMLU */
86        PFC.PBCRH1.BIT.PB17MD = 0x1;    /* Set CS3# */
87
```

**Figure 6 Sample Program Listing: bsc_sram.c (2)**

```
88        /* ==== CS3BCR Setting ==== */
89        BSC.CS3BCR.LONG = 0x10004400ul;
90                        /* Idle cycles between Raed-Write/Write-Write
91                           :1 Idle cycle */
92                        /* Memory type :SDRAM */
93                        /* Data bus size :16-bit size */
94
95        /* ==== CS3WCR setting ==== */
96        BSC.CS3WCR = 0x00000091ul;
97      /* Precharge completion wait cycles:0cycle */
98      /* Wait cycles between ACTV command and READ/WRIT command :0cycle */
99      /* CAS latency for area3 :2cycles */
100     /* Auto-precharge startup wait cycles:2cycles */
101     /* Idle cycles from REF command/self-refresh relese to ACTV/REF/MRS command :3cycles */
102
103       /* ==== SDCR setting ==== */
104       BSC.SDCR.LONG = 0x00000809ul;   /*
105                         Refresh Control :Refresh
106                         RMODE :Auto-refresh is performed
107                         BACTV :Auto-precharge mode
108                         Row address for Area3 :12-bits
109                         Column Address for Area3 :9-bits
110                       */
111       /* ==== RTCOR setting ==== */
112       BSC.RTCOR = 0xa55a0027ul;       /*
113                         15.625usec /400nsec = 39(0x27)cycles/refresh
114                       */
115       /* ==== RTCSR setting ==== */
116       BSC.RTCSR.LONG = 0xa55a0010ul;  /*
117                         Initialize sequence start
118                         Clock select B-clock/16 = 400nsec
119                         Refresh count :Once
120                       */
121       /* ====  200usec interval elapsed   ==== */
122       while(j-- > 0){
123         /* wait */
124       }
125
126       /* ==== Written in SDRAM Mode Register ==== */
127       SDRAM_MODE = 0;         /*
128                         CS3 area/16bit bus size
129                         Burst read/Single write
130                       */
131     }
132     /* End of File */
```

**Figure 7 Sample Program Listing: bsc_sram.c (3)**

## 4. Reference Documents

- Software Manual
  SH-2A, SH2A-FPU Software Manual, Rev. 3.00
  (The latest version can be downloaded from the Renesas Technology Web site.)
- Hardware Manual
  SH7211 Group Hardware Manual, Rev. 2.00
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