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SH7147

Control Area Network (RCAN-ET) Communication

1. Abstract

This application note is organized based on sample communication using RCAN-ET, which is mounted on SH7147, and is aimed to provide information users may need during software and hardware design.

Although the operation of each program in this application note has been checked, make sure that you conduct your own operation checks before actually using.

2. Introduction

2.1 Specification

1 byte data transmission/reception is performed with standard format, using two SH7147 (Figure 1.)

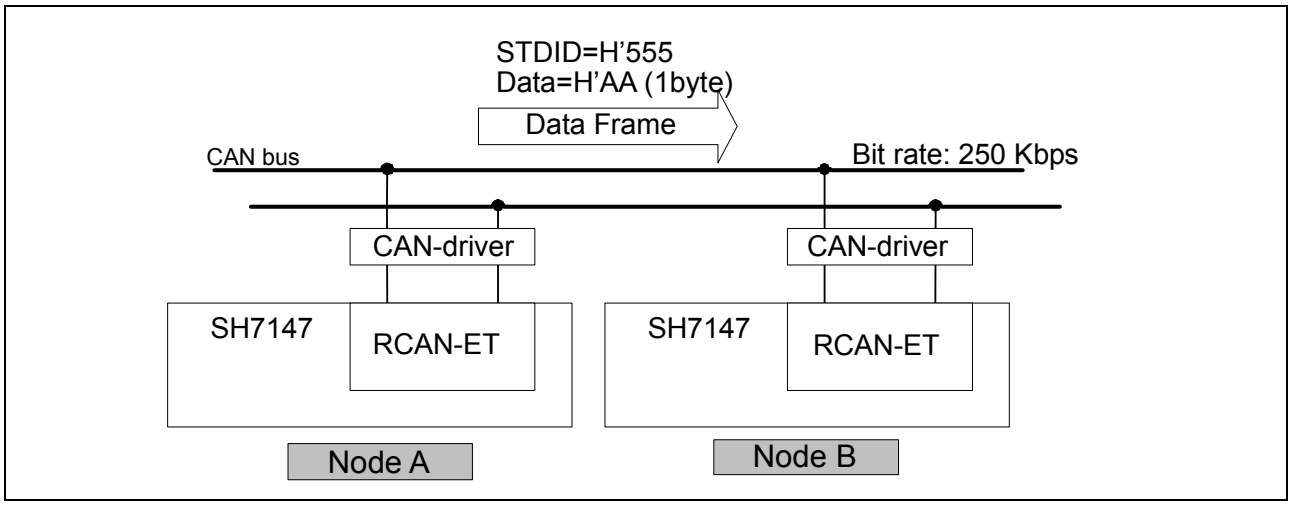

Figure 1 Communication Specification

(1) Transmission/Reception Common Specification

- Communication speed is 250Kbps (when PΦ=32MHz).
- Identifier is H'555

(2) Transmission Specification

- Uses mailbox1.
- Data length is 1byte. Transmit data is H'AA.
- Transmission end flag is polled during transmission.
- After confirming that transmission end flag is set, the flag is cleared and transmission process ends.

(3) Reception Specification

- Uses mailbox2.
- Data is received if Identifier matches.
- Data frame reception end flag is polled.
- Data frame reception end flag is cleared after confirming that the flag is set.
- Reception data is transmitted to RAM and ends reception process.

2.2 Function Used

- RCAN-ET

2.3 Applicable Conditions

- MCU : SH7147 (R5F71474AK64FPV)
- Operation Frequency : Internal Clock 64MHz
  : Bus Clock 32MHz
  : Peripheral Clock 32MHz
  : MTU2S Clock 64MHz
  : MTU2 Clock 32MHz
- C Compiler : Renesas Technology product Ver. V.9.00.02.001
  SuperH RISC engine Family C/C++ compiler package
- Compile Option : Default setting by HEW

3. Description of Sample Task

This sample task performs 1 byte data transmission/reception with standard format, using two SH7147.

3.1 Overview of Functions Used

- Comply with CAN standard 2.0B and ISO-11898 standard
- Sixteen mailboxes (15 mailboxes for transmission/reception, 1 mailbox for reception-only)
- Reception filter mask (LAFM) is supported for all mailboxes
- Test function implemented
- Similar registers with HCAN-II

3.2 Register Description

Table 1 shows descriptions of RCAN-ET registers.

Table 1 RCAN-ET Register Descriptions

Register Name	Abbreviation	Function
Message Control 0	MB[x].CONTROL0	Monitors enable/disable of RCAN-ET transmission/reception pin, transmission stop control of transmission pin, and pin status of transmission/reception pin.
Local Acceptance Filter	MB[x].LAFM	Performs filter mask setting for IDE bit, standard ID, and extended ID
Message Data	MB[x].MSG_DATA[n] (n=0 to 7)	Performs transmission/reception data setting
Message Control 1	MB[x].CONTROL1	Sets new-message control, automatic data frame transmit, disabling automatic retransmit, mailbox configuration, and data length.
Master Control Register	MCR	Controls RCAN-ET operation.
General Status Register	GSR	Indicates RCAN-ET status.
Bit Timing Configuration Register	BCR1/BCR0	Sets RCAN-ET baud rate and bit timing
Interrupt Request Register	IRR	Status flag of various interrupts
Interrupt Mask Register	IMR	Enables interrupt request by IRR's interrupt flag
Error Counter	TEC/REC	A counter that indicates the number of transmitting/receiving message errors.
Transmission Wait Register	TXPR	Sets a message stored in mailbox to transmission wait status.
Transmission Cancel Register	TXCR	Cancels transmission of a transmission waiting message in a mailbox
Transmission Acknowledge Register	TXACK	A status register, indicating that a transmission message in a mailbox have been transmitted properly
Abort Acknowledge Register	ABACK	A status register, indicating that a transmission message in a mailbox have been cancelled properly
Data Frame Reception End Register	RXPR	A status register, indicating that a mailbox have received data frame properly
Remote Frame Reception End Register	RFPR	A status register, indicating that a mailbox have received remote frame properly
Mailbox Interrupt Mask Register	MBIMR	Enables interrupt request of each mailbox
Unread Message Status Register	UMSR	A status register, indicating that overwrite/ overrun have occurred because a mailbox, which has unread message, have received a new message.

[Note] x: Mailbox number (0 to 15)

3.3 Sample Program Procedure

(1) Transmitter side Procedure

Table 2 shows description of registers, been used for transmission. Figure 2 to Figure 4 describes procedure flow.

Table 2 Setting of Registers Used by Transmitter side

Register Name	Function	Set Value
CPG.FRQCR.BIT.IFC	Sets IΦ (internal clock) to 64MHz	0
CPG.FRQCR.BIT.BFC	Sets BΦ (bus clock) to 32MHz	1
CPG.FRQCR.BIT._PFC	Sets PΦ (peripheral clock) to 32MHz	1
CPG.FRQCR.BIT.MIFC	Sets MIΦ (MTU2S clock) to 64MHz	0
CPG.FRQCR.BIT.MPFC	Sets MPΦ (MTU2 clock) to 32MHz	1
STB.CR3.BIT._RCANET	Releases RCAN-ET module stop	0
PFC.PBCR2.BIT.PB7MD	Sets PB7 (41pin) as RCAN-ET reception pin (CRx0)	6
PFC.PBCR2.BIT.PB6MD	Sets PB6 (42pin) as RCAN-ET transmission pin (CTx0)	6
PFC.PBIORL.BIT.B7	Sets PB7 (41pin · CRx0) to input	0
PFC.PBIORL.BIT.B6	Sets PB6 (42pin · CTx0) to output	1
RCANET.MCR.WORD	Sets reset request bit (Sets MCR0 to “1” and ignores other bits) * Automatically set, only by hardware reset	0x0001
RCANET.GSR.WORD	Confirms that RCAN-ET is in reset state (Confirms GSR3=1)	—
RCANET.IRR.WORD	Confirms that RCAN-ET have transited to reset mode (Confirms IRR0=1)	—
RCANET.IRR.WORD	Clears reset/ halt/ sleep interrupt flag (IRR0) (Clear condition: 1 write)	0x0001
RCANET.MCR.WORD	Sets different ID order with HCAN2 (Sets MCR15 to “1” and ignores other bits)	0x8000
RCANET.MB[i].CTRL0.WORD.H RCANET.MB[i].CTRL0.WORD.L RCANET.MB[i].LAFM.WORD.H RCANET.MB[i].LAFM.WORD.L RCANET.MB[i].MSG_DATA[j] (i=0 to 15 , j=0 to 7)	Initializes mailboxes (RAM area)	—
RCANET.MB[1].CTRL0.WORD.H	Sets mailbox 1 to standard format and data frame. Also sets ID(H’555).	0x1544
RCANET.MB[1].CTRL1.WORD	Sets mailbox 1 for transmission and data length (1byte)	0x0001
RCANET.MB[1].MSG_DATA[0]	Sets H’AA as transmit data	0xAA
RCANET.BCR1.WORD	Sets 250kbps when PΦ=40MHz	0xA300
RCANET.BCR0.WORD	(TSEG1=10(11tq), TSEG2=3(4tq), SJW=0, BSP=0, BRP=3)	0x0003
RCANET.MCR.WORD	Clears reset request bit (Clears MCR0 and ignores other bits)	0xFFFE
RCANET.GSR.WORD	Confirms that RCAN-ET have been reset released (Confirms GSR3=0)	—
RCANET.TXPR0.LONG	Sets mailbox 1 to transmission wait status	0x00000002
RCANET.TXACK0.WORD	Waits Mailbox 1 transmission end (Flag polling until bit1 of TXACK0 is set to “1”)	—
RCANET.TXACK0.WORD	Clears transmission end flag of mailbox1 (Clear condition: 1 write)	0x0002

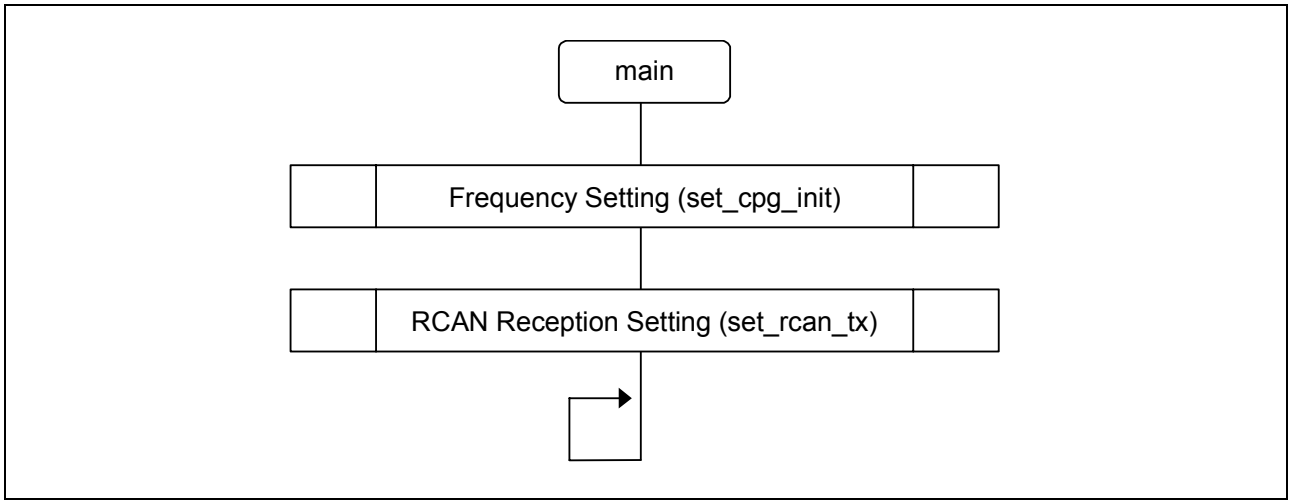

Figure 2 Transmitter side Main Function Flow

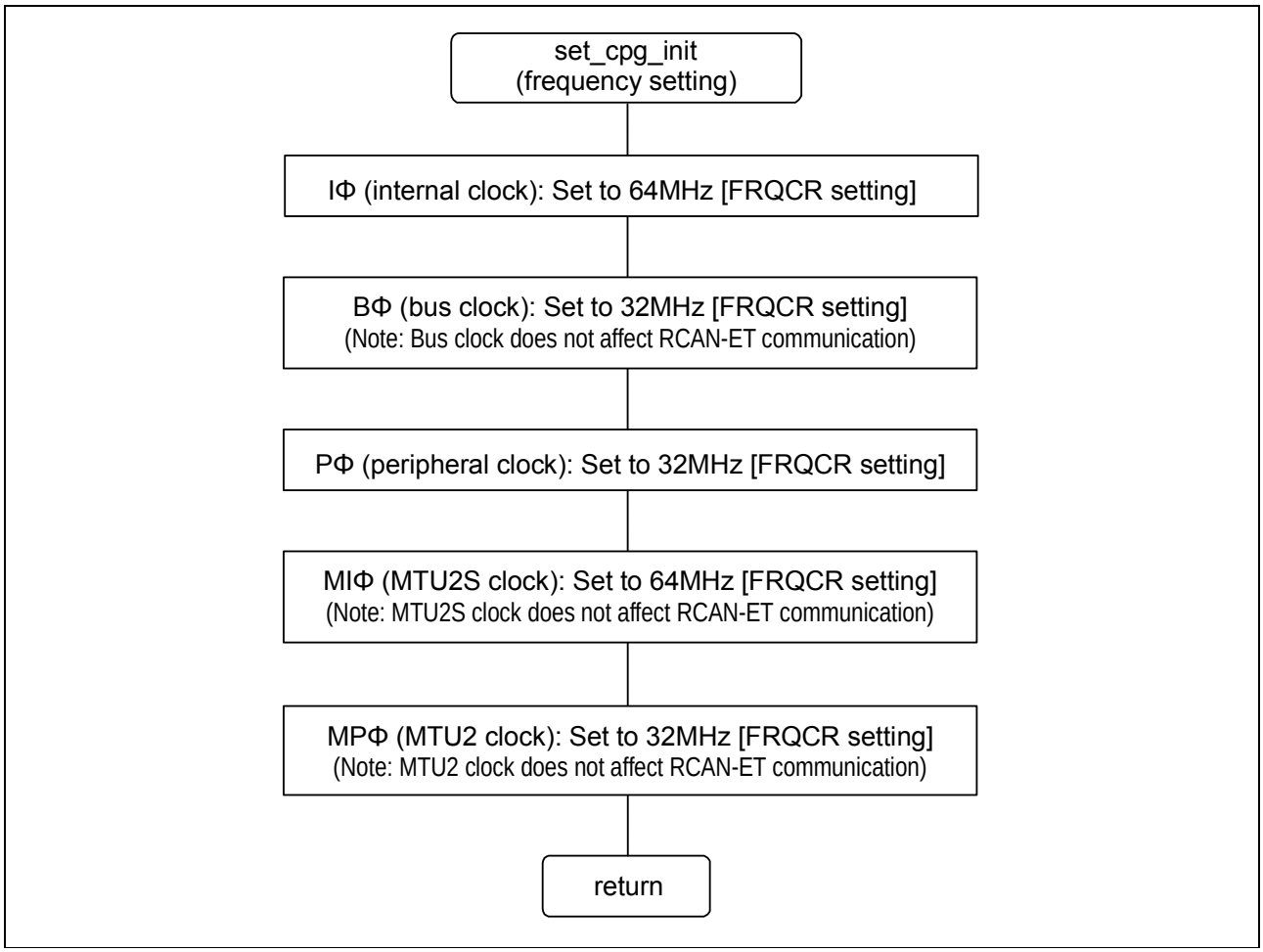

Figure 3 Frequency Setting Flow

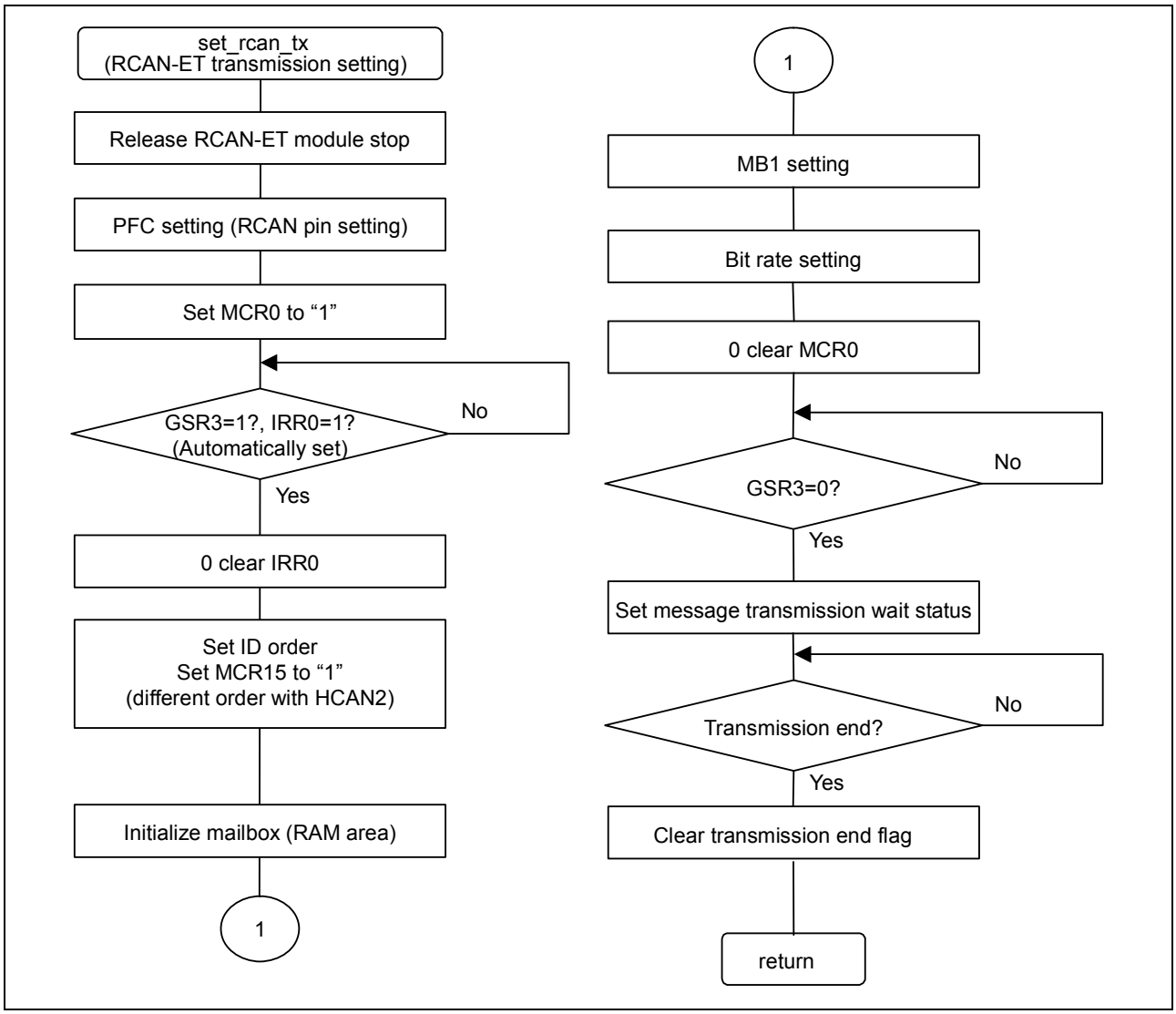

Figure 4 Transmission Setting Flow

(2) Receiver side Procedure

Table 3 shows description of registers, been used in reception. Figure 5 to Figure 7 describes procedure flow.

Table 3 Setting of Registers been Used by Receiver side

Register Name	Function	Set Value
CPG.FRQCR.BIT.IFC	Sets IΦ (internal clock) to 64MHz	0
CPG.FRQCR.BIT.BFC	Sets BΦ (bus clock) to 32MHz	1
CPG.FRQCR.BIT._PFC	Sets PΦ (peripheral clock) to 32MHz	1
CPG.FRQCR.BIT.MIFC	Sets MIΦ (MTU2S clock) to 64MHz	0
CPG.FRQCR.BIT.MPFC	Sets MPΦ (MTU2 clock) to 32MHz	1
STB.CR3.BIT._RCANET	Releases RCAN-ET module stop	0
PFC.PBCR2.BIT.PB7MD	Sets PB7 (41pin) as RCAN-ET reception pin (CRx0)	6
PFC.PBCR2.BIT.PB6MD	Sets PB6 (42pin) as RCAN-ET transmission pin (CTx0)	6
PFC.PBIORL.BIT.B7	Sets PB7 (41pin · CRx0) to input	0
PFC.PBIORL.BIT.B6	Sets PB6 (42pin · CTx0) to output	1
RCANET.MCR.WORD	Sets reset request bit (Sets MCR0 to “1” and ignores other bits) * Automatically set, only by hardware reset	0x0001
RCANET.GSR.WORD	Confirms that RCAN-ET is in reset state (Confirms GSR3=1)	—
RCANET.IRR.WORD	Confirms that RCAN-ET have transited to reset mode (Confirms IRR0=1)	—
RCANET.IRR.WORD	Clears reset/ halt/ sleep interrupt flag (IRR0) (Clear condition: 1 write)	0x0001
RCANET.MCR.WORD	Sets different ID order with HCAN2 (Sets MCR15 to “1” and ignores other bits)	0x8000
RCANET.MB[i].CTRL0.WORD.H RCANET.MB[i].CTRL0.WORD.L RCANET.MB[i].LAFM.WORD.H RCANET.MB[i].LAFM.WORD.L RCANET.MB[i].MSG_DATA[j] (i=0 to 15 , j=0 to 7)	Initializes mailboxes (RAM area)	—
RCANET.MB[2].CTRL0.WORD.H	Sets mailbox 2 as standard format and data frame. Also sets ID(H’555).	0x1544
RCANET.MB[2].LAFM.WORD.H	Sets filter mask of mailbox 2 standard ID, IDE bits	0x0000
RCANET.MB[2].CTRL1.WORD	Sets mailbox 2 for reception	0x0200
RCANET.BCR1.WORD	Sets 250kbps when PΦ=32MHz (TSEG1=10(11tq), TSEG2=3(4tq), SJW=0, BSP=0, BRP=3)	0xA300
RCANET.BCR0.WORD		0x0003
RCANET.MCR.WORD	Clears reset request bit (Clears MCR0 and ignores other bits)	0xFFFE
RCANET.GSR.WORD	Confirms that RCAN-ET has been reset released (Confirm GSR3=0)	—
RCANET.RXPR0.WORD	Waits mailbox 2 reception end (Flag polling until bit0 of RXPR0 is set to “1”)	—
RCANET.RXPR0.WORD	Clears reception end flag of mailbox2 (Clear condition: 1 write)	0x0004

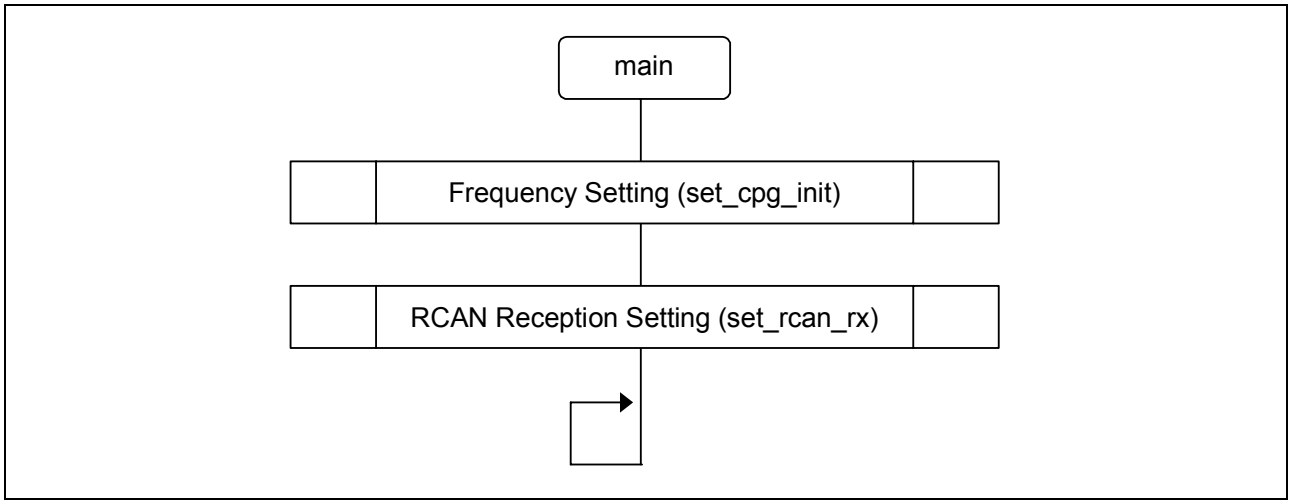

Figure 5 Receiver side Main Function Flow

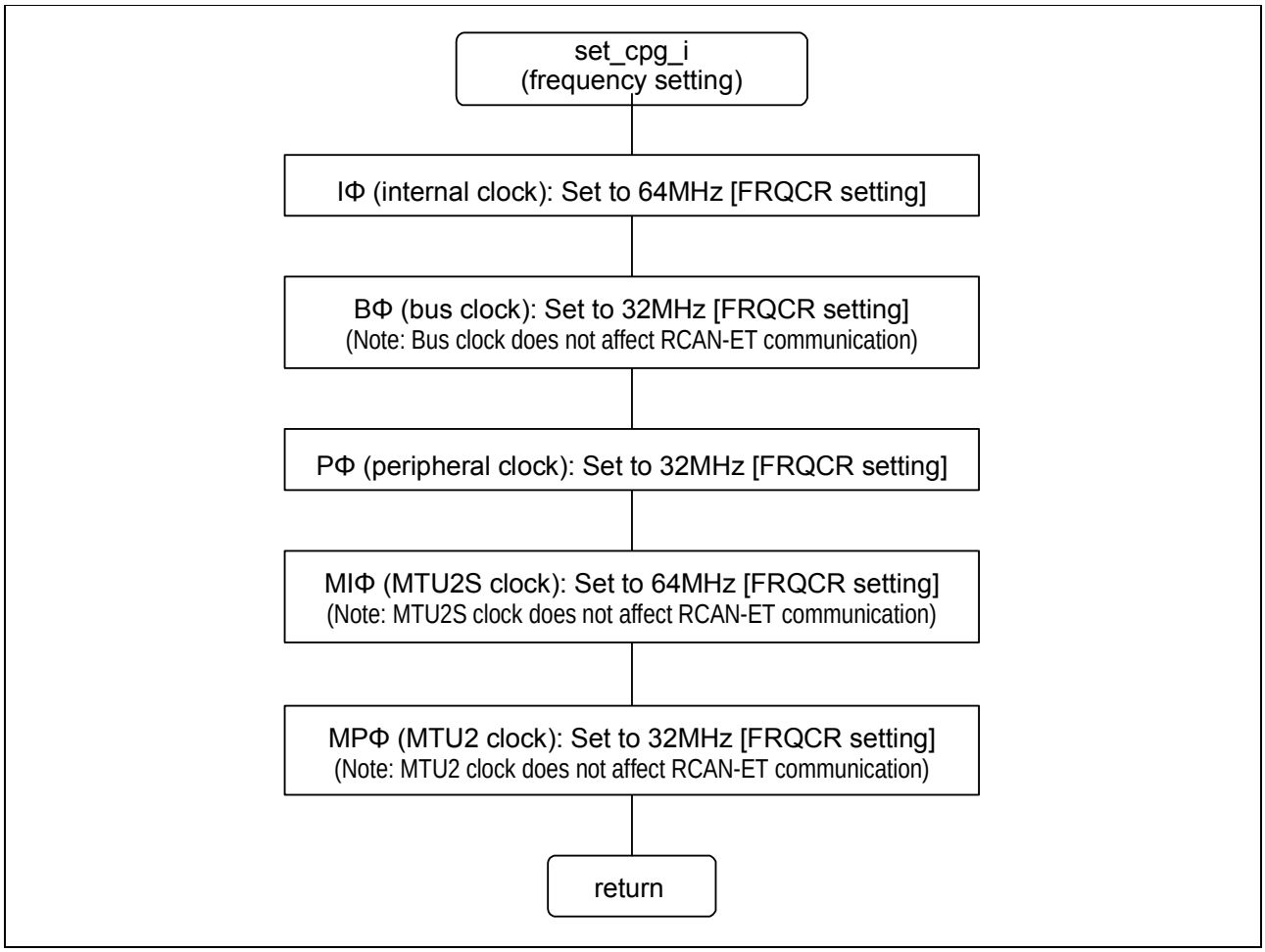

Figure 6 Frequency Setting Flow

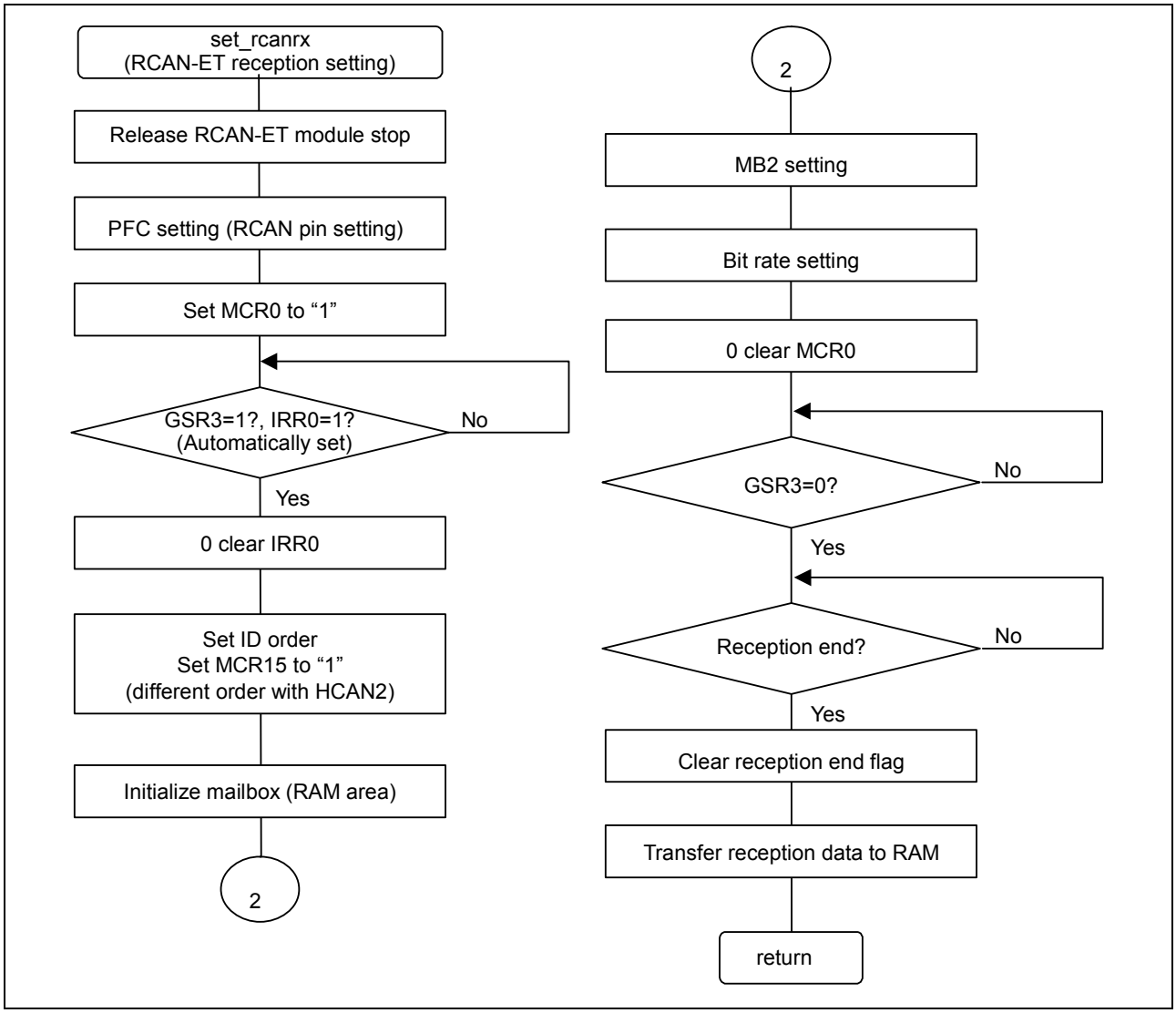

Figure 7 Reception Setting Flow

4. Sample program

(1) Transmitter side Program

```
/*********************************************************************/
/* SH7147                                                            */
/* RCAN-ET Communication Transmitter Side                            */
/*********************************************************************/

/*------------ Include File-------------------------------------------*/
#include <machine.h>
#include"iodefine.h"

/*********************************************************************/
/*    Function Declaration                                           */
/*********************************************************************/
void main(void);              /* Main Routine */
void set_cpg_init(void);      /* Each Clock Setting */
void set_rcan_tx(void);       /* RCAN-ET Transmission Setting */

/*********************************************************************/
/*    Main Routine                                                   */
/*********************************************************************/
void main(void){

   set_cpg_init();          /* Each Clock Setting */
   set_rcan_tx();           /* RCAN-ET Transmission Setting */

  while(1);

}

/*********************************************************************/
/*    Each Clock Setting                                             */
/*    IΦ:BΦ:PΦ:MIΦ:MPΦ = 64MHz:32MHz:32MHz:64MHz:32MHz               */
/*********************************************************************/
void set_cpg_init(void){
```

```
   CPG.FRQCR.BIT.IFC = 0;      /* IΦ=64MHz */
   CPG.FRQCR.BIT.BFC = 1;      /* BΦ=32MHz */
   CPG.FRQCR.BIT._PFC = 1;     /* PΦ=32MHz */
   CPG.FRQCR.BIT.MIFC = 0;     /* MIΦ=64MHz */
   CPG.FRQCR.BIT.MPFC = 1;     /* MPΦ=32MHz */
}

/************************************************************************/
/*    RCAN-ET Transmission Setting Routine                              */
/************************************************************************/
void set_rcan_tx(void){

   unsigned short i,j;

   /** RCCAN-ET Module Stop Release **/
   STB.CR3.BIT._RCANET = 0;    /* RCAN-ET 0:active 1:standby */

   /** Port Setting **/
   PFC.PBCR2.BIT.PB7MD = 6;    /* PB7=CRX0 */
   PFC.PBCR2.BIT.PB6MD = 6;    /* PB6=TRX0 */
   PFC.PBIORL.BIT.B7 = 0;      /* PB7(CRX0) Input */
   PFC.PBIORL.BIT.B6 = 1;      /* PB6(CTX0) Output */

   /** RCCAN-ET Initialization **/
   RCANET.MCR.WORD |= 0x0001;    /* Reset Request (Automatically set by HW reset) */
   while((RCANET.GSR.WORD & 0x0008) != 0x0008);
/* GSR3=1?(RCAN-ET reset state) */
   while((RCANET.IRR.WORD & 0x0001) != 0x0001);
                               /* IRR0=1?(Reset/Halt/Sleep interrupt) */
   RCANET.IRR.WORD = 0x0001;   /* IRR0 Clear (clear condition:1 write) */
   RCANET.MCR.WORD |= 0x8000;  /* Rearrange ID order: Set MCR15=1(initial value) */

   /* Mailbox(RAM area) Initialization */
   for(i = 0;i < 16;i++){
      RCANET.MB[i].CTRL0.WORD.H = 0;
```

```
        RCANET.MB[i].CTRL0.WORD.L = 0;
        RCANET.MB[i].LAFM.WORD.H = 0;
        RCANET.MB[i].LAFM.WORD.L = 0;
        for(j = 0;j < 8;j++){
           RCANET.MB[i].MSG_DATA[j] = 0;
        }
    }

    /* MB1 Setting */
    RCANET.MB[1].CTRL0.WORD.H = 0x1554;   /* ID:H'555, Standard Format, Data Frame */
    RCANET.MB[1].CTRL1.WORD = 0x0001;     /* Set MB[1] for transmission */
    RCANET.MB[1].MSG_DATA[0] = 0xAA;      /* Transmission Data:0xAA */

    /* Bit Rate Setting */
    /* pΦ=32MHz , 250kbps */
    RCANET.BCR1.WORD = 0xA300;        /* TSEG1=10(11tq),TSEG2=3(4tq),SJW=0,BSP=0 */
    RCANET.BCR0.WORD = 0x0003;        /* BRP = 3 */

   /* Reset State Releasing */
    RCANET.MCR.WORD &= 0xFFFE;        /* MCR0 Clear (Clear reset request bit)*/
    while ((RCANET.GSR.WORD & 0x0008) != 0x0000);
                                      /* GSR3=0?(RCAN-ET reset state released?)*/

   /* Transmission Setting */
    RCANET.TXPR0.LONG = 0x00000002;       /* Set MB1 to transmission wait status */
    while ((RCANET.TXACK0.WORD & 0x0002) != 0x0002);      /* Transmission End? */
    RCANET.TXACK0.WORD = 0x0002;
                    /* Transmission End Flag Clear (clear condition:1 write) */

}
```

(2) Receiver Side Program

```
/*****************************************************************************/
/*  SH7147                                                                   */
/*  RCAN-ET Communication Receiver Side                                      */
/*****************************************************************************/

/*------------ Include File-------------------------------------------*/
#include <machine.h>
#include"iodefine.h"

/*------------ Function Definition ------------------------------------*/
void main(void);                  /* Main Routine */
void set_cpg_init(void);          /* Each Clock Setting */
void set_rcan_rx(void);           /* RCAN-ET Reception Setting */

/*****************************************************************************/
/*    Function Declaration                                                   */
/*****************************************************************************/
unsigned short rcan_data;         /* RCAN reception data storing RAM */

/*****************************************************************************/
/*    Main routine                                                           */
/*****************************************************************************/
void main(void)
{

   set_cpg_init();                /* Each Clock Setting */
   set_rcan_rx();                 /* RCAN-ET Reception Setting */

   while(1);

}
```

```
/**********************************************************************/
/*    Each Clock Setting                                              */
/*    IΦ:BΦ:PΦ:MIΦ:MPΦ = 64MHz:32MHz:32MHz:64MHz:32MHz                */
/**********************************************************************/
void set_cpg_init(void){

   CPG.FRQCR.BIT.IFC = 0;          /* IΦ=64MHz */
   CPG.FRQCR.BIT.BFC = 1;          /* BΦ=32MHz */
   CPG.FRQCR.BIT._PFC = 1;         /* PΦ=32MHz */
   CPG.FRQCR.BIT.MIFC = 0;         /* MIΦ=64MHz */
   CPG.FRQCR.BIT.MPFC = 1;         /* MPΦ=32MHz */

}

/**********************************************************************/
/*    RCAN-ET Initial Setting Routine                                 */
/**********************************************************************/
void set_rcan_rx(void){

   unsigned short i,j;

   /** Module Stop Releasing **/
   STB.CR3.BIT._RCANET = 0;        /* RCAN-ET 0:active 1:standby */


   /** Port Setting **/
   PFC.PBCR2.BIT.PB7MD = 6;        /* PB7=CRX0 */
   PFC.PBCR2.BIT.PB6MD = 6;        /* PB6=TRX0 */
   PFC.PBIORL.BIT.B7 = 0;          /* Input PB7(CRX0) */
   PFC.PBIORL.BIT.B6 = 1;          /* Output PB6(CTX0) */

   /** RCAN-ET Reception Setting **/
   RCANET.MCR.WORD |= 0x0001;      /* Reset Request (Automatically set by HW reset) */
   while((RCANET.GSR.WORD & 0x0008) != 0x0008);   /* GSR3=1?(RCAN-ET reset state) */
   while((RCANET.IRR.WORD & 0x0001) != 0x0001);
                               /* IRR0=1?(reset/halt/sleep interrupt) */
```

```
    RCANET.IRR.WORD = 0x0001;      /* IRR0 Clear (Clear condition:1 write) */
    RCANET.MCR.WORD |= 0x8000;    /* Rearrange ID order: Set MCR15=1(initial value) */

    /* Mailbox Initialization */
    for(i = 0;i < 16;i++){
       RCANET.MB[i].CTRL0.WORD.H = 0;
       RCANET.MB[i].CTRL0.WORD.L = 0;
       RCANET.MB[i].LAFM.WORD.H = 0;
       RCANET.MB[i].LAFM.WORD.L = 0;
       for(j = 0;j < 8;j++){
          RCANET.MB[i].MSG_DATA[j] = 0;
       }
    }

    /* MB2 Setting */
    RCANET.MB[2].CTRL0.WORD.H =  0x1554;      /* standard ID , data flam ,ID=555 */
    RCANET.MB[2].LAFM.WORD.H = 0x0000;           /* Set STD_LAFM,IDE_LAFM */
    RCANET.MB[2].CTRL1.WORD = 0x0200;            /* Set Mailbox2 for reception */

    /* Bit Rate Setting */
    /* pΦ=32MHz , 250kbps */
    RCANET.BCR1.WORD = 0xA300;     /* TSEG1=10(11tq),TSEG2=3(4tq),SJW=0,BSP=0 */
    RCANET.BCR0.WORD = 0x0003;      /* BRP = 3 */

   /* Reset State Releasing */
    RCANET.MCR.WORD &= 0xFFFE;      /* MCR0 Clear (Clear reset request bit) */
    while ((RCANET.GSR.WORD & 0x0008) != 0x0000);
                                          /* GSR3=0?(RCAN-ET reset state released?) */

   /* Reception Setting */
   while ((RCANET.RXPR0.WORD & 0x0004) != 0x0004);  /* Reception End? */
   RCANET.TXACK0.WORD = 0x0004;
                        /* Transmission End Flag Clear(Clear condition:1 write) */
   rcan_data = RCANET.MB[2].MSG_DATA[0];           /* Store reception data to RAM */

}
```

5. Reference

Hardware Manual

SH7147 Group Hardware Manual

6. Web-site and contact for support

Renesas Web-site

http://www.renesas.com/

Revision History	RCAN-ET Communication Application Note

Rev.	Date	Description	
		Page	Summary
Rev.1.00	2006.10.12	-	First edition issued

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