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April 1st, 2010
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SH7145 Group

A/D Conversion in Single-cycle Scan Mode

Introduction

The A/D converter of the SH7145 is used to perform A/D conversion in single-cycle scan mode. A/D conversion is performed three times using analog input channels 0 to 3 (AN0 to AN3), and the converted data are stored to RAM.

Target Device

SH7145F

Contents

1. Specifications

The A/D converter of the SH7145 is used to perform A/D conversion in single-cycle scan mode.

As shown in figure 1, A/D conversion is performed three times using analog input channels 0 to 3 (AN0 to AN3), and the converted data are stored to RAM.

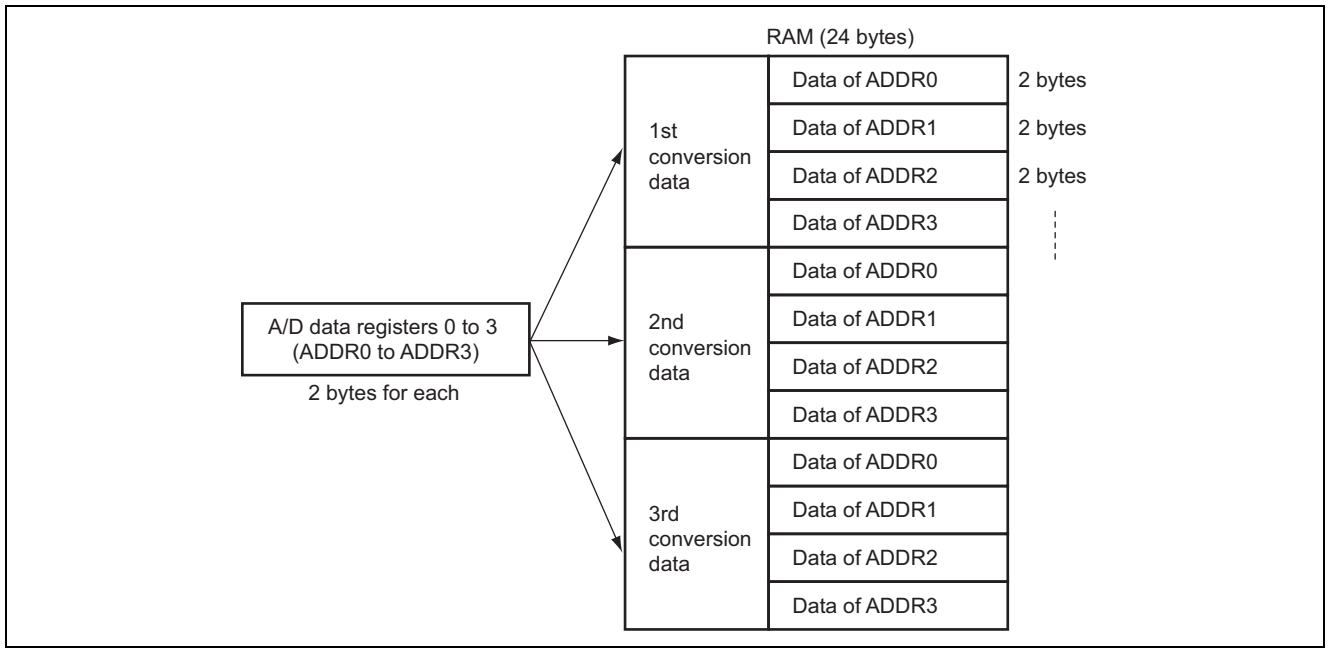


Figure 1 Storage of A/D-Converted Data

2. Description of Functions

In this sample task, channels 0 to 3 (ch0 to ch3) of the A/D converter are used to perform A/D conversion.

2.1 A/D Converter

This is a 10-bit successive approximation A/D converter. Figure 2 shows a block diagram of the A/D converter; below, the converter functions are explained.

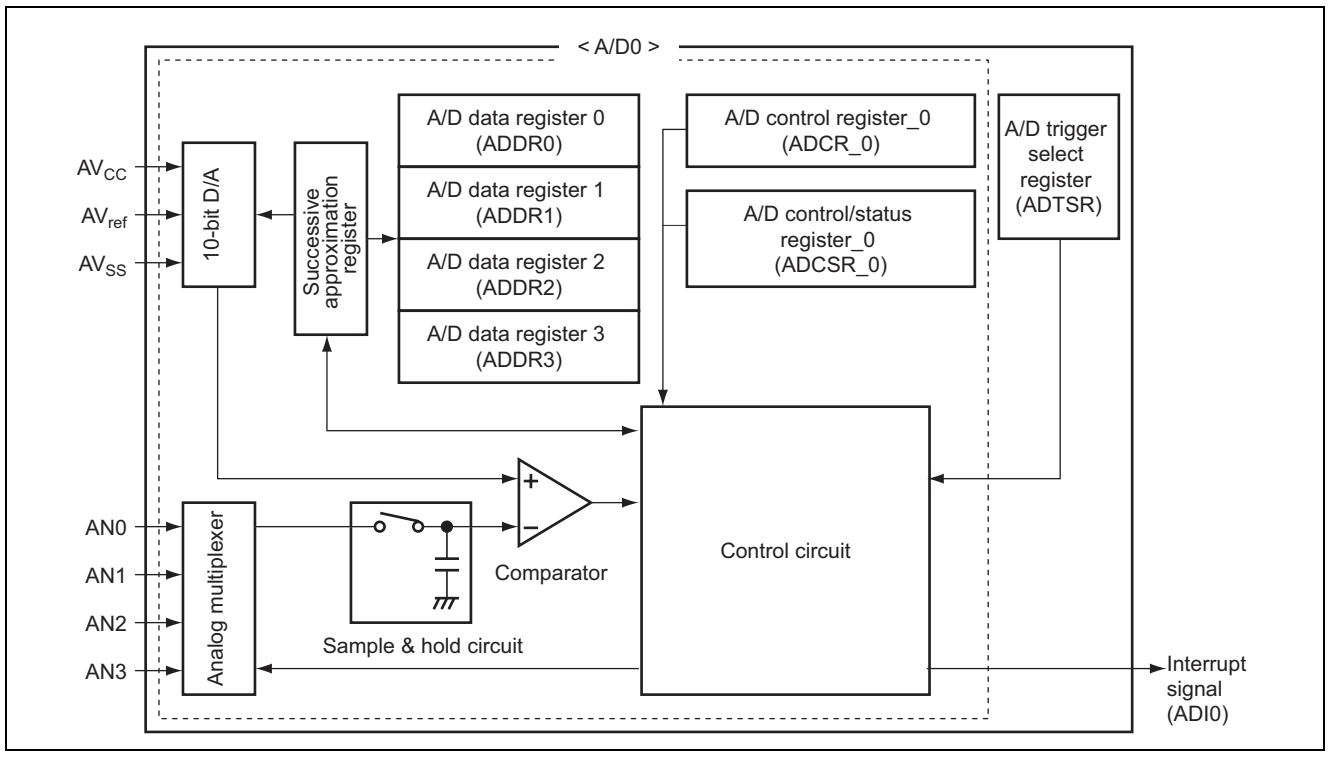


Figure 2 Block Diagram of A/D Converter (ch0 to ch3)

- The A/D data registers (ADDR0 to ADDR3) are 16-bit read-only registers which store the results of conversion for the corresponding analog input channels. The converted data is stored in bits 15 to 6 of ADDR, and the lowermost 6 bits are always 0.
- The A/D control register_0 (ADCR_0) controls starting of A/D conversion and selects the operating clock.
- The A/D control/status register_0 (ADCSR_0) controls A/D conversion operation.
- The A/D trigger select register (ADTSR) enables starting of A/D conversion by an external trigger.

3. Principles of Operation

Figure 3 shows an example of operation in single-cycle scan mode. Table 1 describes the software and hardware processing performed for the operation of figure 3.

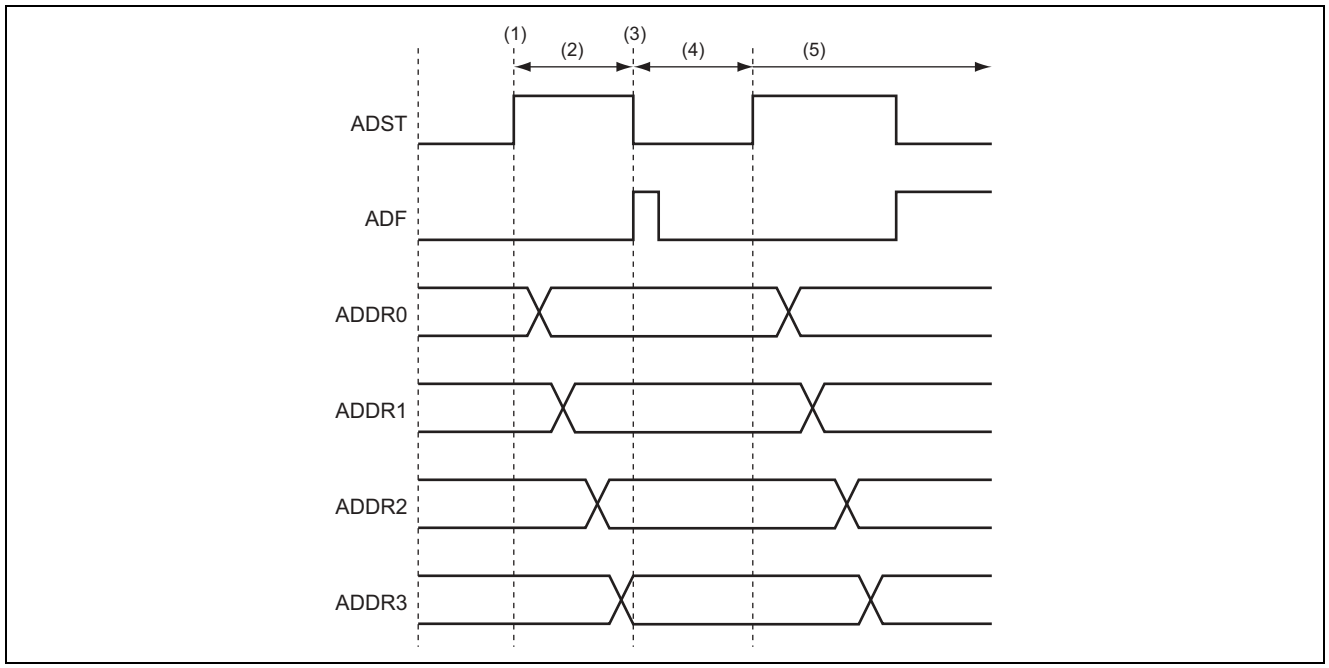


Figure 3 Example of Operation in Single-Cycle Scan Mode

Table 1 Description of Processing

	Software Processing	Hardware Processing
(1)	Set the ADST bit in ADCR_0 to 1.	Start A/D conversion on analog input channels 0, 1, 2, 3 in this order.
(2)	—	Store A/D-converted data to ADDR registers.
(3)	—	When A/D conversion for all channels is completed, set the ADF flag to 1 and clear the ADST bit to 0.
(4)	Clear the ADF flag to 0 and store the data in ADDR registers to RAM.	—
(5)	Repeat steps (1) through (4) above.	Repeat steps (1) through (4) above.

4. Description of Software

4.1 Modules

Table 2 describes the modules used in this sample task.

Table 2 Description of Modules

Module Name	Label Name	Functions
Main routine	main	Initializes A/D0 and calls A/D conversion routine.
A/D conversion routine	ad_conv	Starts A/D conversion and stores the results of conversion to RAM.

4.2 Internal Registers

Tables 3 and 4 describe the internal registers used in this sample task. The settings are values used in this sample task and differ from the initial values.

Table 3 Description of Internal Registers (1)

Register Name	Bit	Bit Name	Setting	Function
MSTCR2				Module standby control register 2
	4	MSTP4	0	A/D0 Standby Control When MSTP4 = 0, the standby state of A/D0 is cancelled.
ADCSR_0				A/D control/status register_0
	7	ADF	*	A/D End Flag Set to 1 when A/D conversion ends.
	6	ADIE	0	A/D Interrupt Enable When ADIE = 1, A/D conversion end interrupt is enabled.
	5	—	0	Reserved
	4	ADM	1	A/D Mode Select When ADM = 1, A/D converter operates in scan mode.
	3	—	1	Reserved
	2	—	0	Reserved
	1	CH1	1	Channel Select 1, 0 These bits select analog input channels for A/D conversion.
	0	CH0	1	

Note: * Only 0 can be written to this bit for clearing; this bit is automatically set by hardware.

Table 4 Description of Internal Registers (2)

Register Name	Bit	Bit Name	Setting	Function
ADCR_0				A/D control register 0
	7	TRGE	0	Trigger Enable When TRGE = 0, A/D conversion triggering is disabled.
	6	CKS1	0	Clock Select 1, 0
	5	CKS0	0	Set A/D conversion time (in this sample task, Pϕ/32).
	4	ADST	*	A/D Start Setting ADST to 1 starts A/D conversion. Automatically cleared when A/D conversion on the selected channel is completed.
	3	ADCS	1	A/D Continuous Scan When ADCS = 0, A/D converter operates in single-cycle scan mode.
	2	—	1	Reserved
	1		1	
	0		1	
ADDR0			—	A/D data register 0 Stores the results of A/D conversion for analog input pin 0 (AN0).
ADDR1			—	A/D data register 1 Stores the results of A/D conversion for analog input pin 1 (AN1).
ADDR2			—	A/D data register 2 Stores the results of A/D conversion for analog input pin 2 (AN2).
ADDR3			—	A/D data register 3 Stores the results of A/D conversion for analog input pin 3 (AN3).

Note: * Clear this bit to 0 to stop A/D conversion.

4.3 RAM Usage

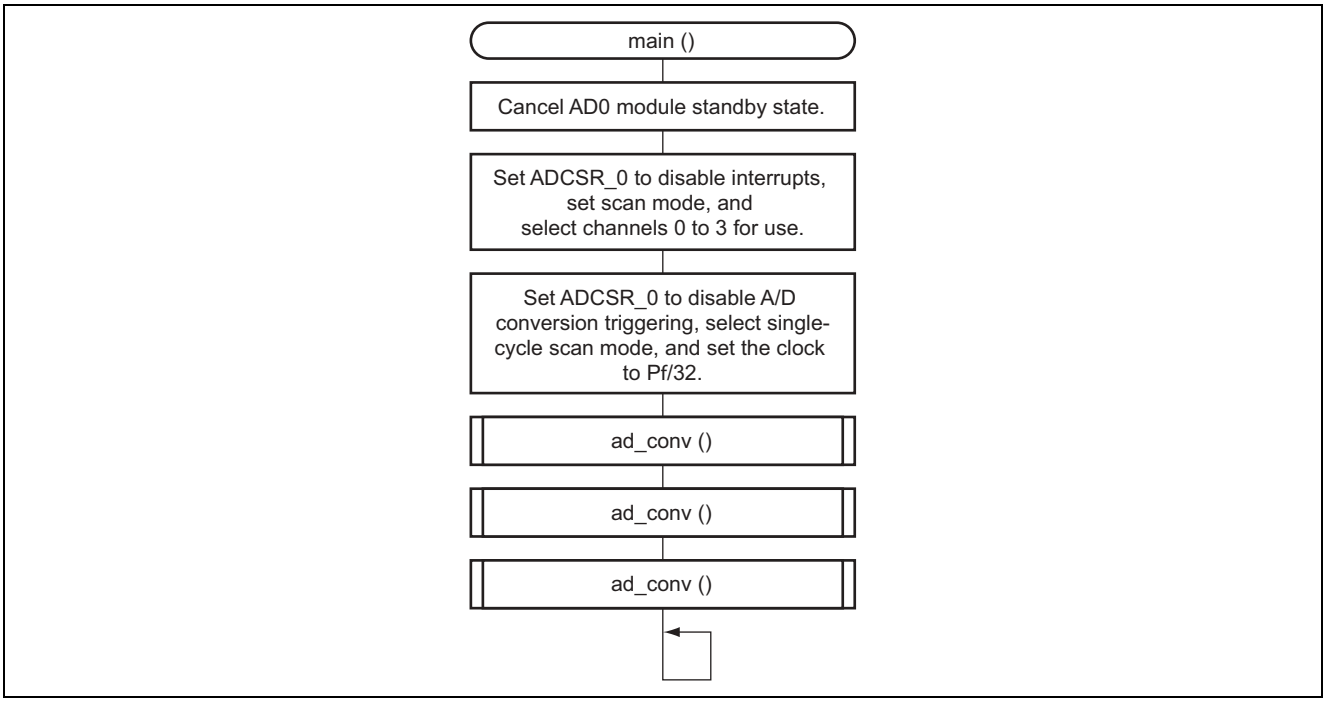
Table 5 describes the RAM usage in this sample task.

Table 5 Description of RAM

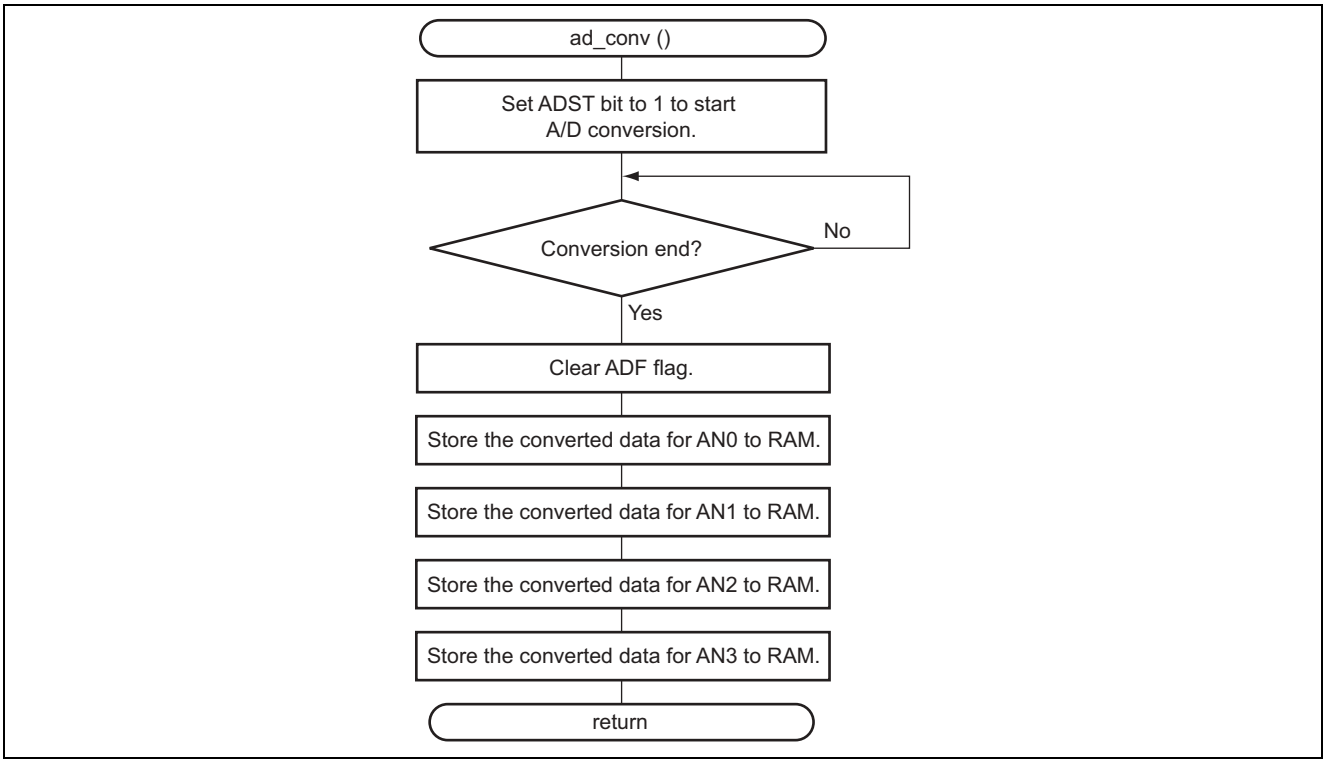
Label Name	Function	Address	Used in
Ad_data[0-2][0-3]	Array for storing A/D converted data (2 bytes/data)	On-chip RAM	A/D conversion routine

5. Flowchart

5.1 Main Routine



5.2 A/D Conversion Routine



6. Program Listing

```
/************************************************************************************************/
/* SH7145F Application Note                                                                     */
/*                                                                                              */
/* Function                                                                                     */
/*    :AD0(1 Cycle Scan Mode)                                                                   */
/*                                                                                              */
/* External input clock         :12.5MHz                                                        */
/* Internal CPU clock           :50MHz                                                          */
/* Internal peripheral clock    :25MHz                                                          */
/*                                                                                              */
/* Written        :2003/10       Rev.1.0                                                       */
/************************************************************************************************/

#include "iodefine.h"
#include <machine.h>

/************************************************************************************************/
/*  Symbol Definition                                                                           */
/************************************************************************************************/
#define AD 3
#define CH 4

/************************************************************************************************/
/*  Function Define                                                                             */
/************************************************************************************************/
void main(void);
void ad_conv(void);

void dummy_f(void);

/************************************************************************************************/
/*  RAM Allocation Definition                                                                   */
/************************************************************************************************/
unsigned short Ad_data[AD][CH];

unsigned char ad_count;
unsigned char ch_count;
```

```
/*****************************************************************************************************/
/* Main Program                                                                                      */
/*****************************************************************************************************/
void main( void )
{
    ad_count = 0;
    ch_count = 0;

    P_STBY.MSTCR2.BIT.MSTP4 = 0;                    /* Disable AD0 standby mode                 */

    P_AD.ADCSR_0.BYTE = 0x1B;                       /* Set ADCSR_0                              */
                //[7] = 0;ADF
                //[6] = 0;A/D interrupt disable
                //[5] = 0;reserve
                //[4] = 1;scan mode
                //[3] = 1;reserve
                //[2] = 0;reserve
                //[1] = 1
                //[0] = 1;channel select AN0-3

    P_AD.ADCR_0.BYTE = 0x07;                        /* Set ADCR_0                               */
                //[7] = 0;trigger disable
                //[6] = 0
                //[5] = 0;clock P phi/32
                //[4] = 0;wait conversion
                //[3] = 0;1 cycle scan
                //[2] = 1;reserve
                //[1] = 1;reserve
                //[0] = 1;reserve
    ad_conv();
    ad_conv();
    ad_conv();

    while(1);                                       /* LOOP                                     */
}
```

```
/*****************************************************************************************************/
/*  ad_conv                                                                                          */
/*****************************************************************************************************/
void ad_conv(void)
{
    P_AD.ADCR_0.BIT.ADST = 1;                       /* Start AD converter                       */

    while(P_AD.ADCSR_0.BIT.ADF==0);                 /* Waits till a conversion end              */

    P_AD.ADCSR_0.BIT.ADF = 0;                       /* Clear ADF flag                           */

    Ad_data[ad_count][ch_count] = P_AD.ADDR0.WORD; /* Store AD(AN0) data                        */
    ch_count++;

    Ad_data[ad_count][ch_count] = P_AD.ADDR1.WORD; /* Store AD(AN1) data                        */
    ch_count++;

    Ad_data[ad_count][ch_count] = P_AD.ADDR2.WORD; /* Store AD(AN3) data                        */
    ch_count++;

    Ad_data[ad_count][ch_count] = P_AD.ADDR3.WORD; /* Store AD(AN4) data                        */
    ch_count = 0;
    ad_count++;
}

/*****************************************************************************************************/
/*  Interruption Program                                                                             */
/*****************************************************************************************************/
#pragma interrupt(dummy_f)
void dummy_f(void)
{
    /* Other Interrupt */
}
```

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Sep.16.04	—	First edition issued

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