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Renesas Electronics Corporation

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SH7144/45 Group

Pulse Output

1. Specifications

Using MTU ch0, a 50% duty pulse with a period set in RAM is output as shown in figure 1.

When operating with on-chip peripheral clock Pϕ = 40.0 MHz, the output pulse width can be set arbitrarily in the range 50.0 ns to 1.63 ms.

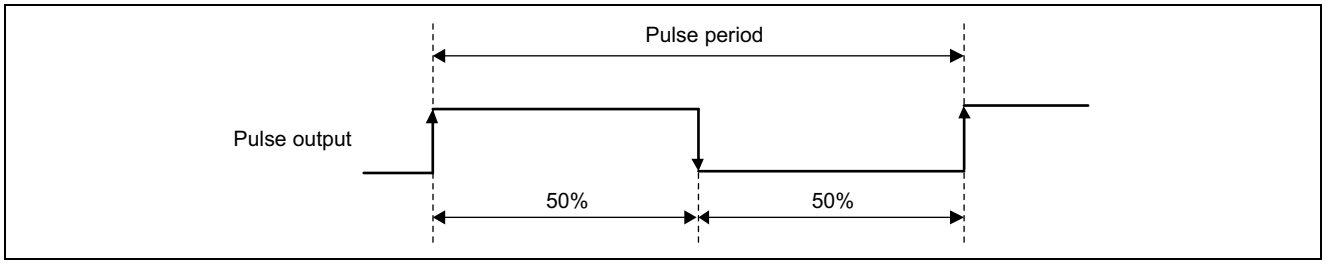


Figure 1 Pulse Output

2. Functions Used

In this sample task, a pulse with a 50% duty cycle is output using MTU channel 0 (ch0).

Figure 2 shows a block diagram of MTU/ch0 as used in this task. The following ch0 functions are used.

- A function that outputs pulses automatically by hardware without software intervention (output compare)
- A function that clears a counter when a compare match occurs (counter clearing)
- A function that reverses output each time a compare match occurs (toggle output)

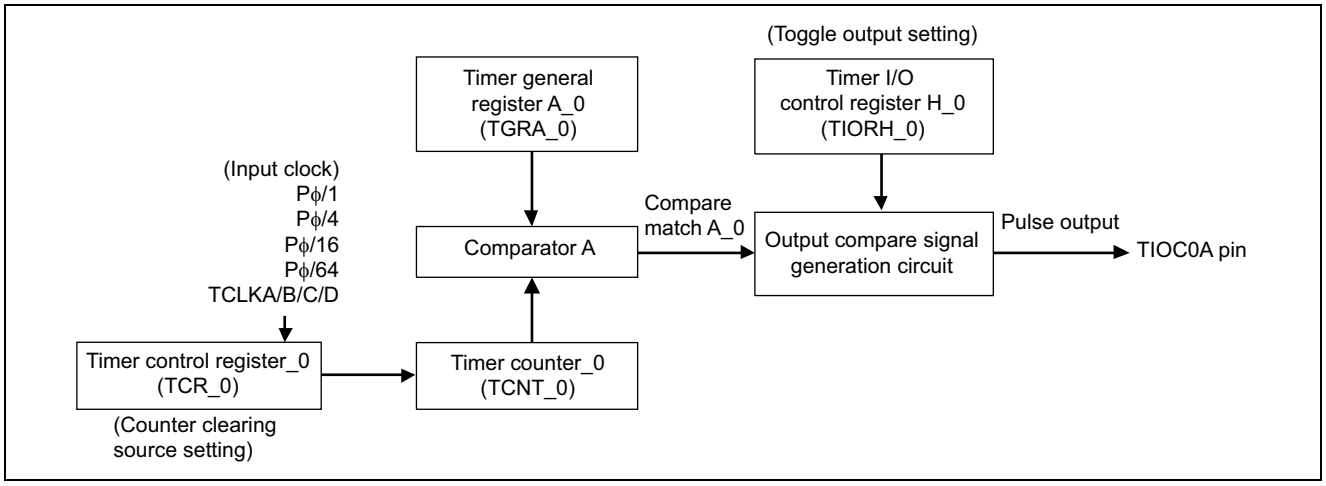


Figure 2 Block Diagram of MTU/ch0

Table 1 shows the function assignments used in this sample task. Pulses are output by assigning MTU functions as shown in the table.

Table 1 Function Assignments

Pin or Register Name	Function Assignment
TIOC0A	Pulse output pin
TCR_0	Selection of counter clearing source and input clock
TIORH_0	Pulse output level setting
TGRA_0	Pulse 1/2 period setting

3. Principles of Operation

Figure 3 illustrates the principles of operation of this sample task. Pulses are output by SH7145 hardware and software processing as shown in the figure.

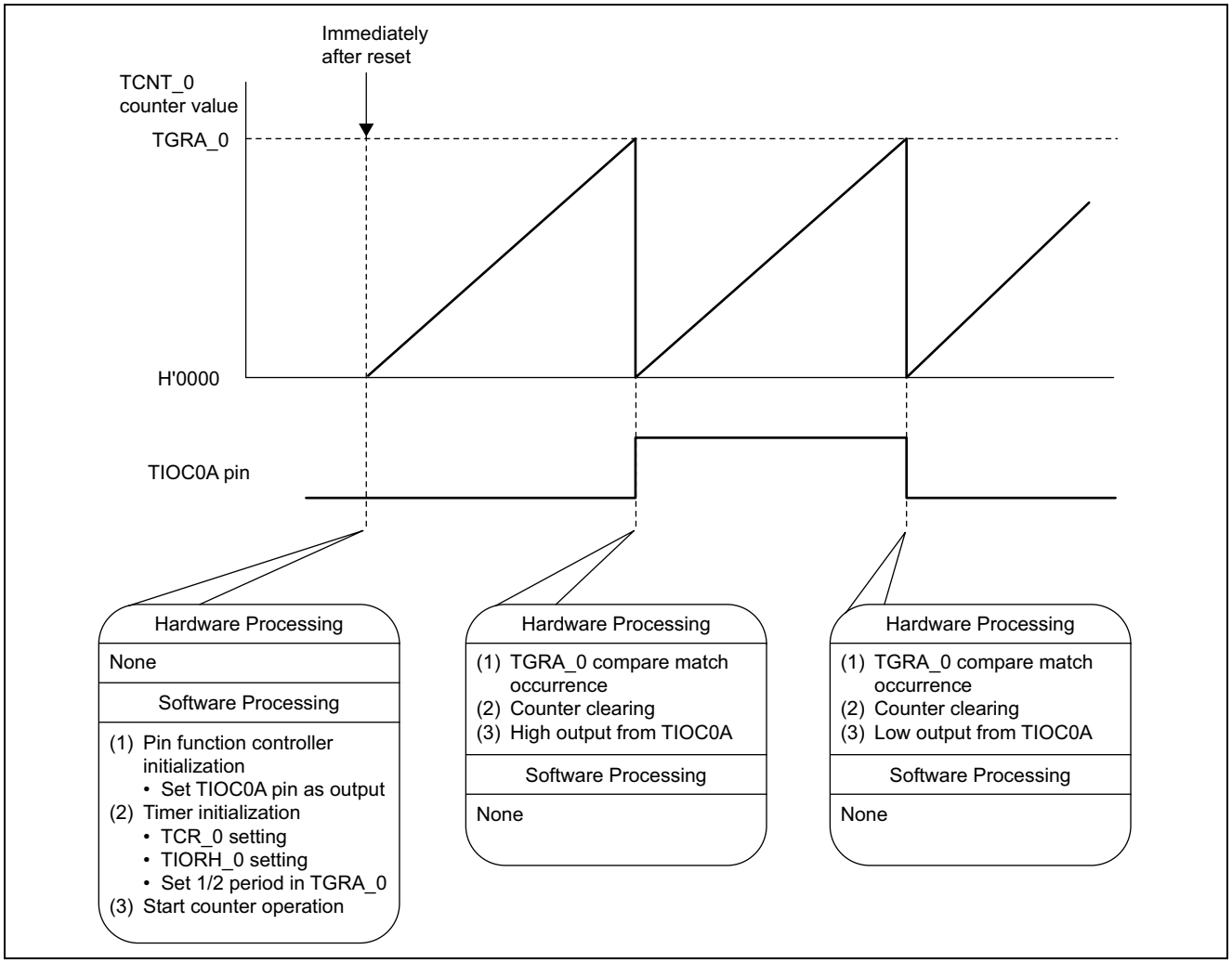


Figure 3 Principles of Operation of Pulse Output

4. Software

(1) Modules

Module Name	Label	Function Assignment
Main routine	puls_out	PFC and pulse output setting

(2) Arguments

Label or Register Name	Function Assignment	Data Length	Module	Input/Output
pul_cyc	Used to set timer value for pulse 1/2 period Pulse period is calculated using following equation: Pulse period (ns) = timer value × ϕ period (25 ns at 40.0 MHz)	1 word	Main routine	Input

(3) Internal Registers Used

Register Name	Function	Address	Set Value
P_PORTE.PECRL2	Sets PE0 as TIOC0A output	H'FFFF83BA	H'0001
P_MTU0.TCR_0	Sets TGRA_0 compare match as counter clearing source Sets Pϕ/1 as input clock	H'FFFF8260	H'20
P_MTU0.TIORH_0	TIOC0A initial output 0, output toggled on compare match	H'FFFF8262	H'03
P_MTU0.TGRA_0	Output pulse 1/2 period setting	H'FFFF8268	pul_cyc
P_MTU0.TMDR_0	Sets ch0 to normal mode	H'FFFF8261	H'c0
P_STBY.MSTCR2	MTU module standby mode clearing	H'FFFF861E	H'd0fd

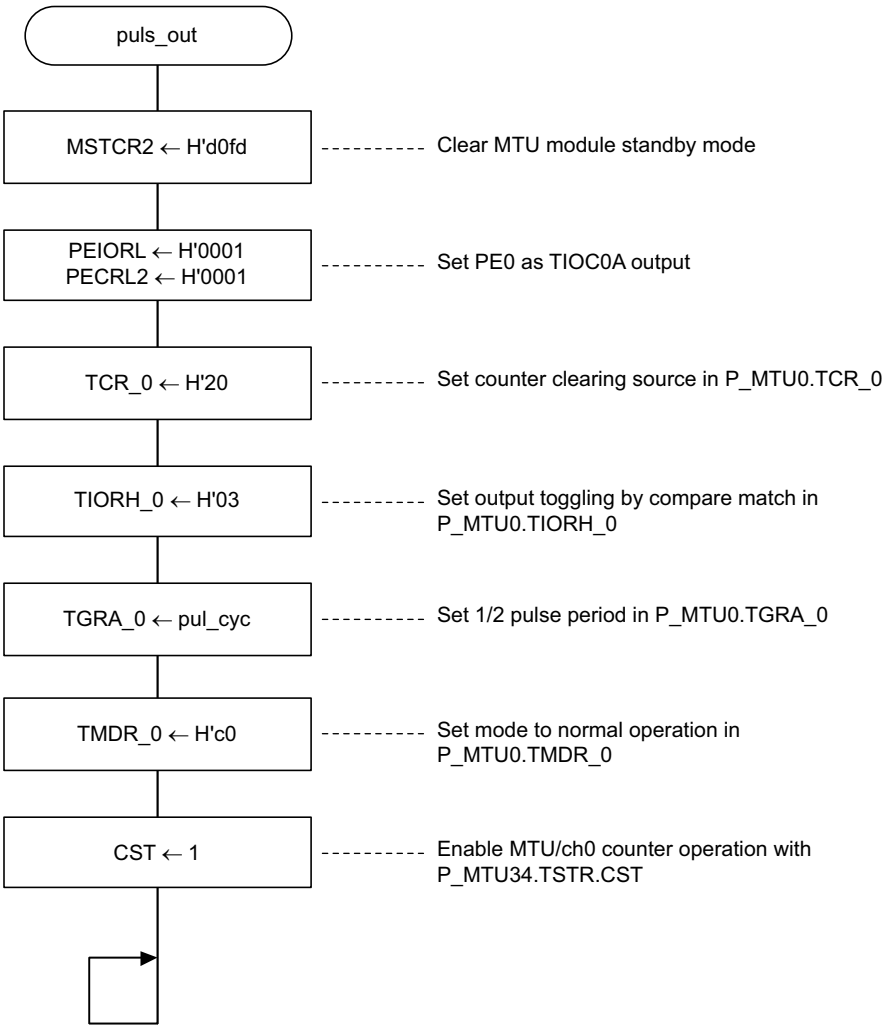
(4) RAM Used

This sample task does not use any RAM apart from the arguments.

Note: SH7145 header file names are used for register label names.

5. Flowcharts

(1) Main routine



6. Program Listing

```
/************************************************************************/
/*                                INCLUDE FILE                          */
/************************************************************************/
#include<machine.h>
#include"iodefine_7145F.h"
/************************************************************************/
/*                                  PROTOTYPE                           */
/************************************************************************/
void puls_out(void);
/************************************************************************/
/*                                RAM ALLOCATION                        */
/************************************************************************/
#define  pul_cyc   (*(unsigned short *)0xffffe000)
/************************************************************************/
/*                                MAIN PROGRAM                          */
/************************************************************************/
void puls_out(void)
 {
  P_STBY.MSTCR2.WORD = 0xd0fd;   /* MTU module standby mode clear */
  P_PORTE.PEIORL.WORD = 0x0001;  /* TIOC0A = output */
  P_PORTE.PECRL2.WORD = 0x0001;  /* PE0 function = TIOC0A */

  P_MTU0.TCR_0.BYTE = 0x20;      /* Counter clear by TGRA_0 */
  P_MTU0.TIORH_0.BYTE = 0x03;    /* toggle output */
  P_MTU0.TGRA_0 = pul_cyc;       /* set 1/2 period */
  P_MTU0.TCNT_0 = 0x0000;        /* Clear timer counter */
  P_MTU0.TMDR_0.BYTE = 0xc0;     /* Set operation mode */
  P_MTU34.TSTR.CST.BIT = 1;      /* Start timer counter */
  while(1);
 }
```

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