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SH7080/SH7146/SH7125/SH7200 Series

Three-Phase Complementary PWM Output

Introduction

This application note discusses the generation of three-phase complementary PWM (Pulse Width Modulation) waveforms that include dead time, during which the positive and negative phases will not both be active at the same time.

Target Device

- Microcomputer: SH7085 (R5F7085)
- Operating frequency:

Internal clock	80 MHz
Bus clock	40 MHz
Peripheral clock	40 MHz
MTU2 clock	40 MHz
MTU2S clock	80 MHz

- C compiler: Ver. 7.1.04 of Renesas C compiler

Contents

1. Specifications

(1) In this sample task, PWM waveforms are generated by using the MTU2*.
(2) As shown in figure 1, three phases of PWM waveforms, each phase comprising a pair of positive and negative phases, are output.
(3) The PWM waveform includes the time intervals (dead time) during which the positive and negative phases will not both be active at the same time.
(4) The dead time may be set to any desired length (no dead time can also be specified).
(5) The duty cycle may be set to any value between 0 and 100%.

$$\text{Duty cycle} = \frac{\text{Active pulse period}}{\text{Pulse period}} \times 100\ (\%)$$

(6) A toggle waveform is output in synchronization with the PWM period.

Note: * The settings and operations are the same when the MTU2S is used instead. With the MTU2S, a maximum of 80-MHz operation is possible.

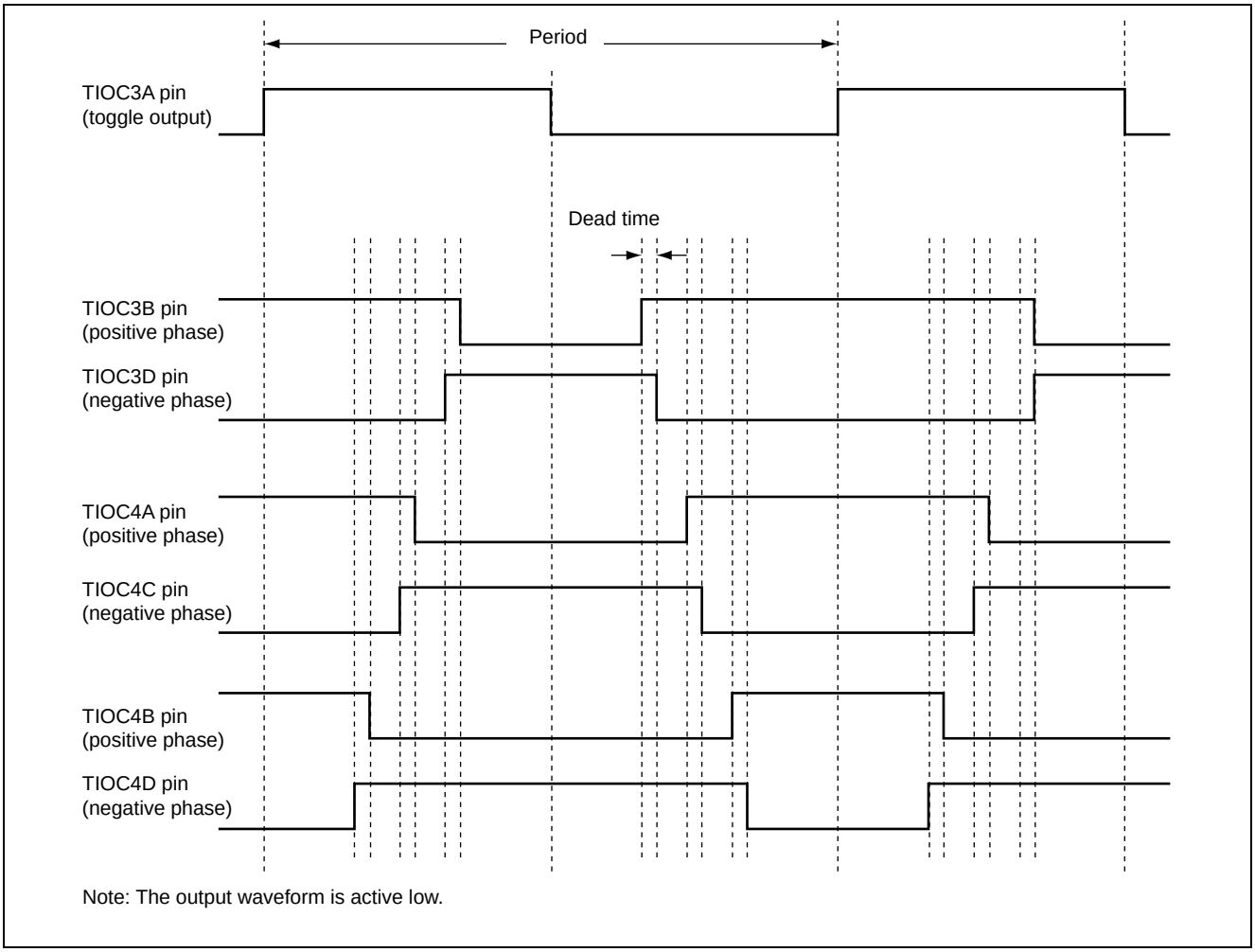
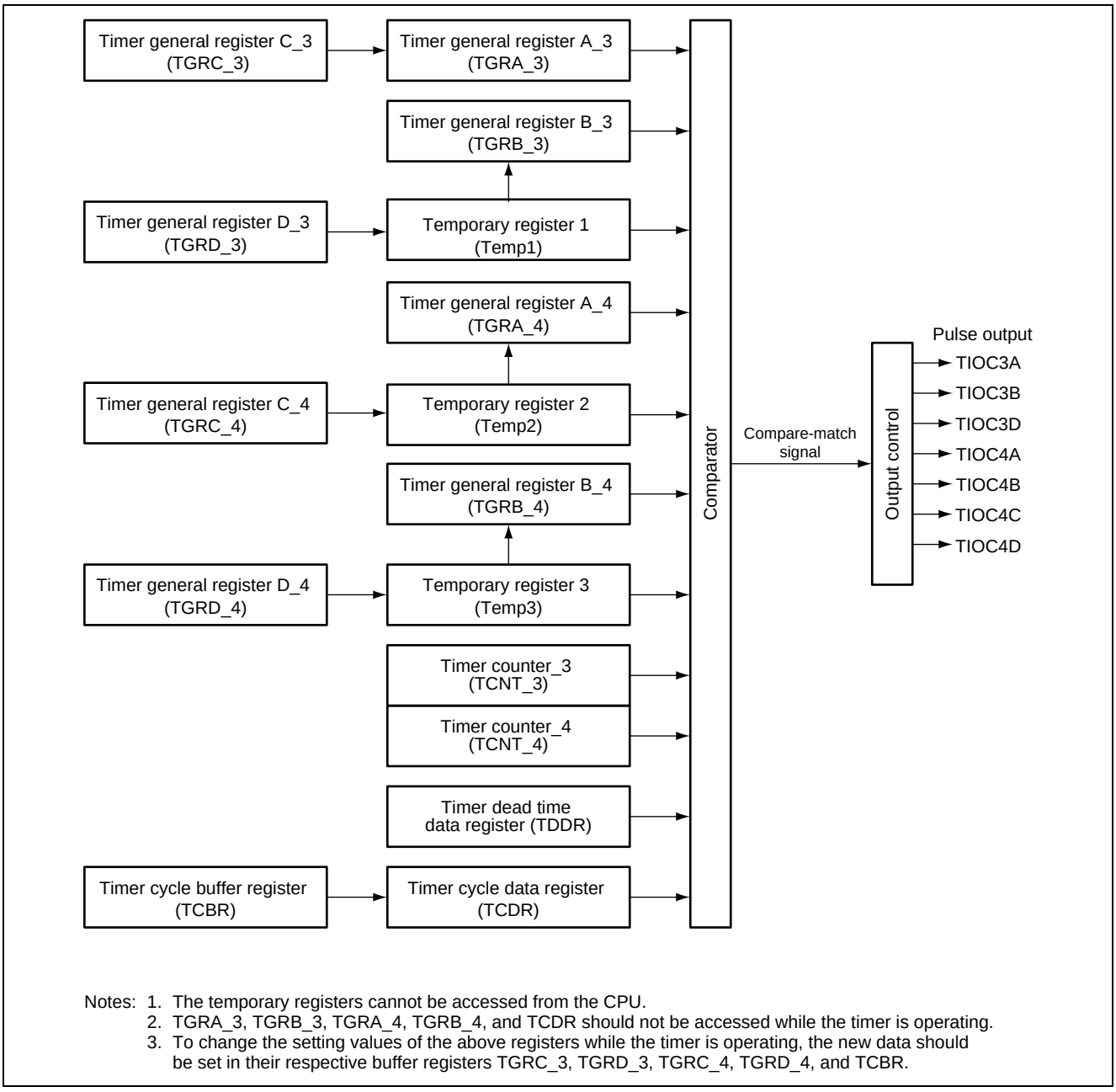


Figure 1 Three-Phase Complementary PWM Output Waveforms

2. Description of Functions

In this sample task, channel 3 (ch3) and channel 4 (ch4) of the MTU2 are used to output three-phase complementary PWM waveforms. The operating mode of the MTU2 is complementary PWM mode.

Figure 2 shows a block diagram of the MTU2 (ch3 and ch4) in complementary PWM mode, with a description of the functions noted below.



Notes: 1. The temporary registers cannot be accessed from the CPU.
2. TGRA_3, TGRB_3, TGRA_4, TGRB_4, and TCDR should not be accessed while the timer is operating.
3. To change the setting values of the above registers while the timer is operating, the new data should be set in their respective buffer registers TGRC_3, TGRD_3, TGRC_4, TGRD_4, and TCBR.

Figure 2 Block Diagram of MTU2 (ch3 and ch4) in Complementary PWM Mode

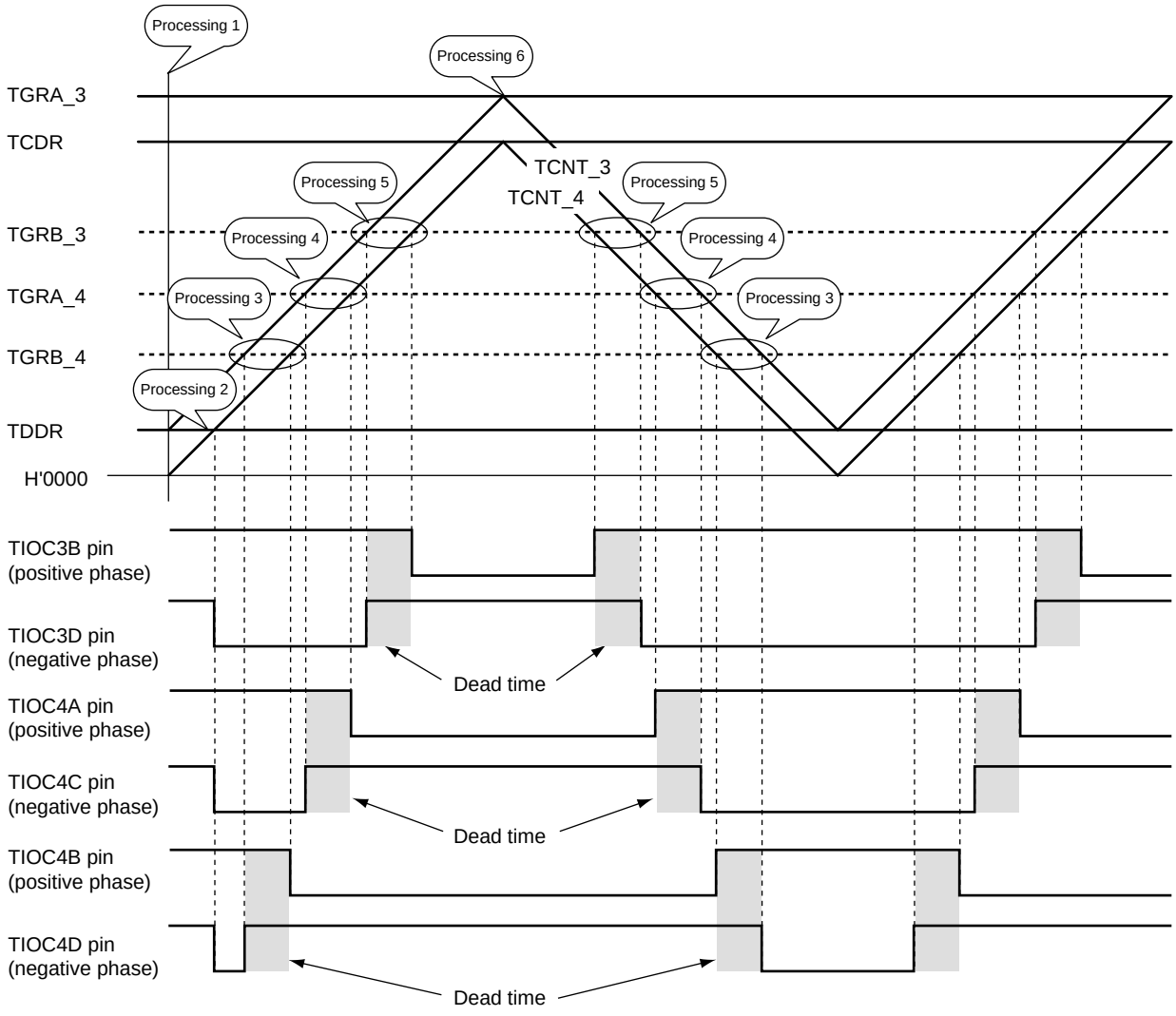
- The timer general register A_3 (TGRA_3) operates as a compare register. A value that corresponds to half the PWM pulse period should be set in TGRA_3. To change the setting value during timer operation, a new value should be set in the timer general register C_3 (TRGC_3).
- The timer general register B_3 (TGRB_3) operates as a compare register. The duty cycle of the PWM waveforms output from the TIOC3B and TIOC3D pins should be set in TGRB_3. To change the setting value during timer operation, a new value should be set to the timer general register D_3 (TRGD_3).
- The timer general register C_3 (TGRC_3) operates as the buffer register for TGRA_3. While the timer is operating, the TGRC_3 value is reflected to TGRA_3.
- The timer general register D_3 (TGRD_3) operates as the buffer register for TGRB_3. If the value of TGRD_3 is changed during timer operation, a new value will be transferred to the temporary register 1 (TEMP1) and reflected to TGRB_3.
- The timer general register A_4 (TGRA_4) operates as a compare register. The duty cycle of the PWM waveforms output from the TIOC4A and TIOC4C pins should be set in TGRA_4. To change the setting value during timer operation, a new value should be set in the timer general register C_4 (TRGC_4).
- The timer general register B_4 (TGRB_4) operates as a compare register. The duty cycle of the PWM waveforms output from the TIOC4B and TIOC4D pins should be set in TGRB_4. To change the setting value during timer operation, a new value should be set in the timer general register D_4 (TRGD_4).
- The timer general register C_4 (TGRC_4) operates as the buffer register for TGRA_4. While the timer is operating, the TGRC_4 value is reflected to TGRA_4.
- The timer general register D_4 (TGRD_4) operates as the buffer register for TGRB_4. While the timer is operating, the TGRD_4 value is reflected to TGRB_4.
- The temporary registers 1 to 3 (TEMP1 to TEMP3) are located between the buffer registers and compare registers. Data written to the buffer register is transferred to the corresponding temporary register, and then transferred to the compare register. The temporary registers cannot be accessed from the CPU.
- The timer counter_3 (TCNT_3) is a 16-bit readable/writable counter. TCNT_3 counts downward after a compare-match with TGRA_3, and counts upward after a compare-match with the timer dead time data register (TDDR).
- The timer counter_4 (TCNT_4) is a 16-bit readable/writable counter. TCNT_4 counts downward after a compare-match with the timer cycle data register (TCDR), and counts upward after it reaches H'0000.
- The timer dead time data register (TDDR) is a 16-bit readable/writable register. Dead time of PWM waveforms should be set in TDDR.
- The timer cycle data register (TCDR) is a 16-bit readable/writable register. A value that corresponds to half the PWM carrier period should be set in TCDR.
- The timer cycle buffer register (TCBR) operates as the buffer register for TCDR. While the timer is operating, the TCBR value is reflected to TCDR.

3. Principles of Operation

3.1 Three-Phase Complementary PWM Output

Figure 3 illustrates the operation during three-phase complementary PWM output, and table 1 shows the operation contents.

The TIOC3B pin is paired with the TIOC3D pin, the TIOC4A pin with the TIOC4C pin, and the TIOC4B pin with the TIOC4D pin. PWM waveforms with dead time are output from these pins to produce three-phase output (it is also possible to specify no dead time).



Note: For each pin, the initial output is high level and the active level is low level.

Figure 3 Operation of Three-Phase Complementary PWM Waveform Output

Table 1 Operation of Three-Phase Complementary PWM Waveform Output

	Hardware Processing	Software Processing
Processing 1	—	• Set MTU2 registers. • Select the pin functions for use. • Start the timer counter.
Processing 2	Output a low level from the TIOC3D, TIOC4C and TIOC4D pins on compare match between TCNT_4 and TDDR.	—
Processing 3	• Invert TIOC4D pin output on compare match between TCNT_3 and TGRB_4. • Invert TIOC4B pin output on compare match between TCNT_4 and TGRB_4.	—
Processing 4	• Invert TIOC4C pin output on compare match between TCNT_3 and TGRA_4. • Invert TIOC4A pin output on compare match between TCNT_4 and TGRA_4.	—
Processing 5	• Invert TIOC3D pin output on compare match between TCNT_3 and TGRB_3. • Invert TIOC3B pin output on compare match between TCNT_4 and TGRB_3.	—
Processing 6	Generate an interrupt (TGIA_3) on compare match between TCNT_3 and TGRA_3.	Update the duty cycle*.

Note: When changing the duty cycle, always set TGRD_4 last. TGRD_4 must be set even if the value of TGRD_4 needs not be changed.

3.2 Timer Counter Operation

Figure 4 illustrates the timer counter operation.

The timer counters are started after loading TCNT_3 with the same value as TDDR and loading TCNT_4 with H'0000.

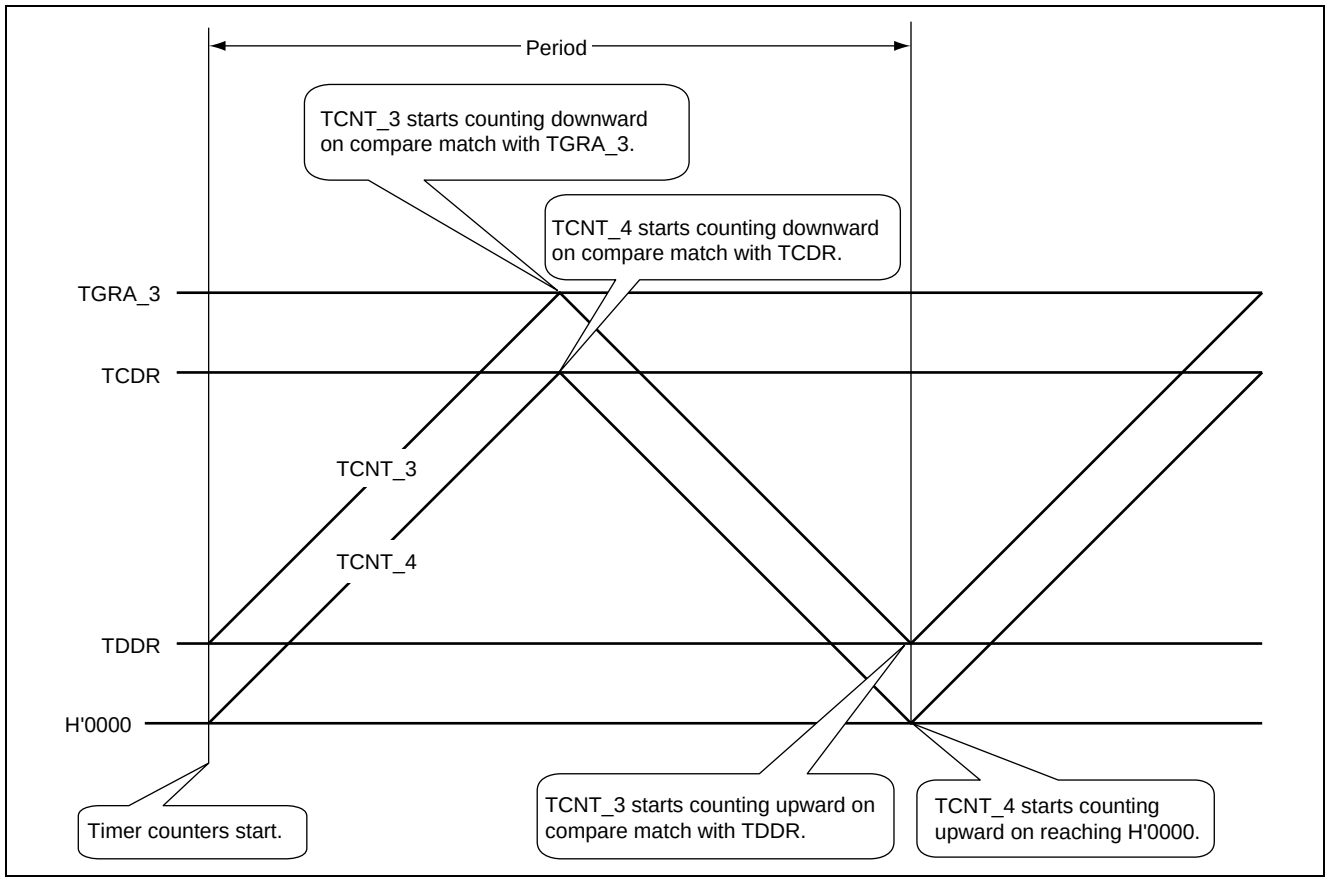
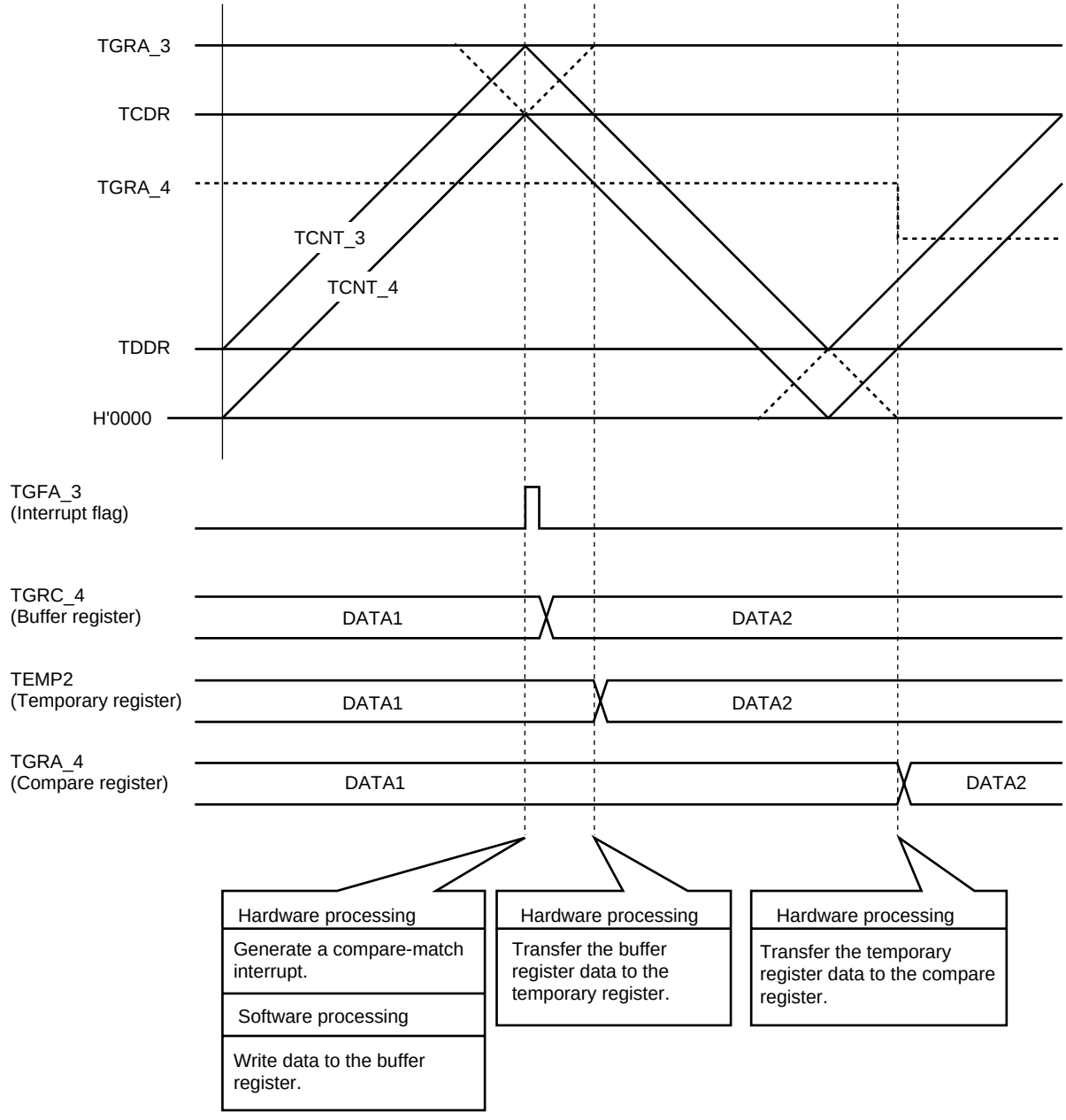


Figure 4 Timer Counter Operation

3.3 Changing the Duty Cycle

The PWM duty cycle is changed with the timing shown in figure 5.

The duty cycle is changed using compare-match interrupts. To change the duty cycle, the buffer register value should be changed. The value of the compare register must not be changed directly because this causes unstable operation.



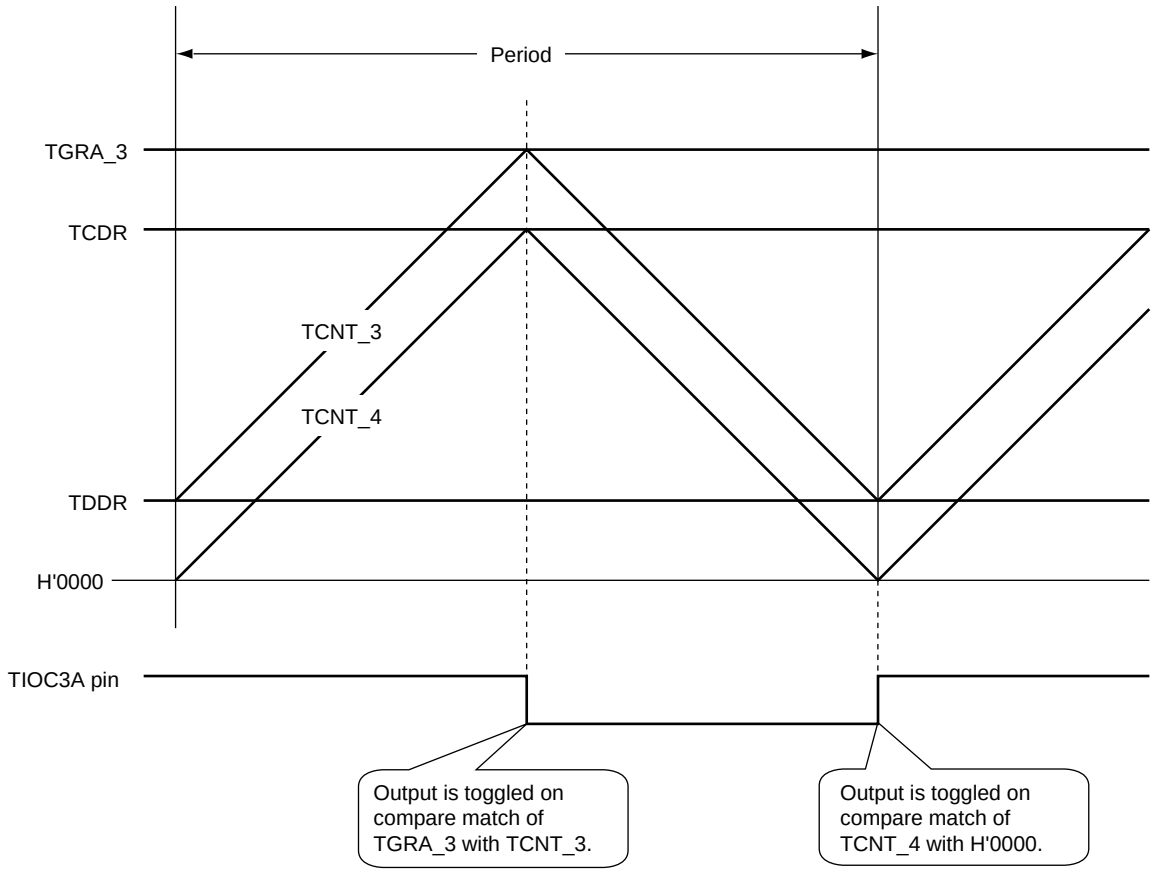
Note: When changing the duty cycle, always set TGRD_4 last.
TGRD_4 must be set even if the TGRD_4 setting does not need to be changed.

Figure 5 Timing of Duty Cycle Changing

3.4 Toggle Output Synchronized with the PWM Period

Figure 6 shows the operation of the toggle output synchronized with the PWM period.

The output on the TIOC3A pin is toggled, forming a 50% duty cycle waveform with the same period as the PWM pulses. The duty cycle of this waveform cannot be changed.



Note: When toggle output is enabled, the output pin is TIOC3A and the initial output level is high.

Figure 6 Toggle Output Operation Synchronized with the PWM Period

4. Description of Software

4.1 Modules

Table 2 describes the modules of this sample task.

Table 2 Description of Modules

Module Name	Label Name	Functions
Main routine	main()	Makes initial settings of MTU2 and starts the timer counters.
TGRA_3 compare-match interrupt routine	int_tgia3()	Changes the duty cycle.

4.2 Internal Registers

Table 3 shows the registers used in this sample task. Note that the settings in the tables are the values used in this sample task, and are different from the initial values.

Table 3 Description of Internal Registers

Register	Bit	Bit Name	Function	Setting
FRQCR			Frequency Control Register Specifies the ratios for dividing the output frequency of the PLL circuit to generate operating clocks. FRQCR = H'0241 sets the division ratios as follows. Internal clock: ×1 Bus clock: ×1/2 Peripheral clock: ×1/2 MTU2S clock: ×1 MTU2 clock: ×1/2	H'0241
STBCR4			Standby Control Register 4	H'BF
	6	MSTP22	Module Stop bit 22 Clock is supplied to MTU2 when MSTP22 = b'0.	0
IPRE			Interrupt Priority Register E Sets the interrupt level of MPU2 to 15.	H'00F0
PEIORL			Port E I/O Register L Sets up the pins for PWM output (TIOC3A, TIOC3B, TIOC3D, TIOC4A, TIOC4B, TIOC4C and TIOC4D pins) as output pins.	H'FB00

Register	Bit	Bit Name	Function	Setting
PECRL3			Port E Control Register L3	H'1011
	15	—	Reserved	0
	14	PE11MD2	PE11 Mode	0
	13	PE11MD1	Selects TIOC3D as the pin function when PE11MD2 to	0
	12	PE11MD0	PE11MD0 = b'001.	1
	11	—	Reserved	0
	10	PE10MD2	PE10 Mode	0
	9	PE10MD1	Selects PE10 (general I/O) as the pin function when	0
	8	PE10MD0	PE10MD2 to PE10MD0 = b'000	0
	7	—	Reserved	0
	6	PE9MD2	PE9 Mode	0
	5	PE9MD1	Selects TIOC3B as the pin function when PE9MD2 to	0
	4	PE9MD0	PE9MD0 = b'001.	1
PECRL3	3	—	Reserved	0
	2	PE8MD2	PE8 Mode	0
	1	PE8MD1	Selects TIOC3A as the pin function when PE8MD2 to	0
	0	PE8MD0	PE8MD0 = b'001.	1
PECRL4			Port E Control Register L4	H'1111
	15	—	Reserved	0
	14	PE15MD2	PE15 Mode	0
	13	PE15MD1	Selects TIOC4D as the pin function when PE15MD2 to	0
	12	PE15MD0	PE15MD0 = b'001.	1
	11	—	Reserved	0
	10	PE14MD2	PE14 Mode	0
	9	PE14MD1	Selects TIOC4C as the pin function when PE14MD2 to	0
	8	PE14MD0	PE14MD0 = b'001.	1
	7	—	Reserved	0
	6	—	Reserved	0
	5	PE13MD1	PE13 Mode	0
	4	PE13MD0	Selects TIOC4B as the pin function when PE13MD1 and PE13MD0 = b'01.	1
	3	—	Reserved	0
	2	PE12MD2	PE12 Mode	0
	1	PE12MD1	Selects TIOC4A as the pin function when PE12MD2 to	0
	0	PE12MD0	PE12MD0 = b'001.	1

Register	Bit	Bit Name	Function	Setting
TCR_3			Timer Control Register_3	H'01
	7	CCLR2	Counter Clear 2,1,0	0
	6	CCLR1	Disables clearing of TCNT_3 when CCLR2 to CCLR0 = b'000.	0
	5	CCLR0		0
	4	CKEG1	Clock Edge 1,0	0
	3	CKEG0	When CKEG1 and CKEG0 = b'00, TCNT_3 counts rising edges of the internal clock.	0
	2	TPSC2	Timer Prescaler 2, 1, 0	0
	1	TPSC1	When TPSC2 to TPSC0 = b'001, the clock source for TCNT_3 is MPϕ/4.	0
	0	TPSC0		1
TCR_4			Timer Control Register_4	H'01
	7	CCLR2	Counter Clear 2, 1, 0	0
	6	CCLR1	Disables clearing of TCNT_4 when CCLR2 to CCLR0 = b'000.	0
	5	CCLR0		0
	4	CKEG1	Clock Edge 1,0	0
	3	CKEG0	When CKEG1 and CKEG0 = b'00, TCNT_4 counts rising edges of the internal clock.	0
	2	TPSC2	Timer Prescaler 2, 1, 0	0
	1	TPSC1	When TPSC2 to TPSC0 = b'001, the clock source for TCNT_4 is MPϕ/4.	0
	0	TPSC0		1
TCNT_3			Timer Counter_3 The timer counter for channel 3 The same value as the timer dead time data register (TDDR) value is set.	Dead_time
TCNT_4			Timer Counter_4 The timer counter for channel 4 H'0000 is set.	H'0000
TGRA_3			Timer General Register A_3 TCNT_3 starts counting downward on compare-match with TGRA_3. Used to set carrier period / 2 + dead time.	Pul_cycle
TGRB_3			Timer General Register B_3 Used to set the duty cycle of PWM waveforms output from the TIOC3B and TIOC3D pins.	Pul_duty3d
TGRC_3			Timer General Register C_3 Buffer register for TGRA_3 To change the TGRA_3 value during timer operation, a new value should be set in this register. The same value as TGRA_3 is set as the initial value.	Pul_cycle

Register	Bit	Bit Name	Function	Setting
TGRD_3			Timer General Register D_3 Buffer register for TGRB_3 To change the TGRB_3 value during timer operation, a new value should be set in this register. The same value as TGRB_3 is set as the initial value.	Pul_duty3d
TGRA_4			Timer General Register A_4 Used to set the duty cycle of PWM waveforms output from the TIOC4A and TIOC4C pins.	Pul_duty4c
TGRB_4			Timer General Register B_4 Used to set the duty cycle of PWM waveforms output from the TIOC4B and TIOC4D pins.	Pul_duty4d
TGRC_4			Timer General Register C_4 Buffer register for TGRA_4 To change the TGRA_4 value during timer operation, a new value should be set in this register. The same value as TGRA_4 is set as the initial value.	Pul_duty4c
TGRD_4			Timer General Register D_4 Buffer register for TGRB_4 To change the TGRB_4 value during timer operation, a new value should be set in this register. The same value as TGRB_4 is set as the initial value.	Pul_duty4d
TDDR			Timer Dead Time Data Register Sets the dead time.	Dead_time
TCDR			Timer Cycle Data Register Sets half the carrier period.	C_cycle
TCBR			Timer Cycle Buffer Register Buffer register for the timer cycle data register To change the TCDR value during timer operation, a new value must be set in this register.	C_cycle

Register	Bit	Bit Name	Function	Setting
TOCR1			Timer Output Control Register 1	H'40
	7	—	Reserved	0
	6	PSYE	PWM Synchronous Output Enable Enables toggle output synchronized with the period of the PWM pulses on the TIOC3A pin when PSYE = b'1.	1
	5	—	Reserved	0
	4	—	Reserved	0
	3	TOCL	TOC Register Write Protect Enables writing to the TOCS, OLSN and OLSP bits in TOCR1 when TOCL = b'0.	0
	2	TOCS	TOC Select Validates TOCR1 setting when TOCS = b'0.	0
	1	OLSN	Output Level Select N Selects output level of the negative phase.	0
	0	OLSP	Output Level Select P Selects output level of the positive phase.	0
TMDR_3			Timer Mode Register_3	H'3F
	7	—	Reserved	0
	6	BFR	Buffer Operation E Reserved with channel 3.	0
	5	BFB	Buffer Operation B Selects buffer operation of TGRB_3 and TGRD_3 when BFB = b'1.	1
	4	BFA	Buffer Operation A Selects buffer operation of TGRA_3 and TGRC_3 when BFA = b'1.	1
	3	MD3	Mode 3, 2, 1, 0 Sets the timer operating mode. When MD3 to MD0 = b'1111, the timer operates in complementary PWM mode 3.	1
	2	MD2		1
	1	MD1		1
	0	MD0		1
TOER			Timer Output Enable Register	H'FF
	7	—	Reserved	1
	6	—	Reserved	1
	5	OE4D	Timer Enable TIOC4D Enables output from the TIOC4D pin when OE4D = b'1.	1
	4	OE4C	Timer Enable TIOC4C Enables output from the TIOC4C pin when OE4C = b'1.	1
	3	OE3D	Timer Enable TIOC3D Enables output from the TIOC3D pin when OE3D = b'1.	1
	2	OE4B	Timer Enable TIOC4B Enables output from the TIOC4B pin when OE4B = b'1.	1

Register	Bit	Bit Name	Function	Setting
TOER	1	OE4A	Timer Enable TIOC4A Enables output from the TIOC4A pin when OE4A = b'1.	1
	0	OE3B	Timer Enable TIOC3B Enables output from the TIOC3B pin when OE3B = b'1.	1
TIER_3			Timer Interrupt Enable register_3	H'01
	7	TTGE	A/D Conversion Start Request Enable Disables A/D conversion start request generation by TGRA when TTGE = b'0.	0
	6	TTGE2	A/D Conversion Start Request Enable 2 Reserved with channel 3.	0
	5	TCIEU	Underflow Interrupt Enable Reserved with channel 3.	0
	4	TCIEV	Overflow Interrupt Enable Disables interrupt requests by the TCFV flag when TCIEV = b'0.	0
	3	TGIED	TGR Interrupt Enable D Disables interrupt requests by the TGFD bit when TGIED = b'0.	0
	2	TGIEC	TGR Interrupt Enable C Disables interrupt requests by the TGFC bit when TGIEC = b'0.	0
	1	TGIEB	TGR Interrupt Enable B Disables interrupt requests by the TGFB bit when TGIEB = b'0.	0
	0	TGIEA	TGR Interrupt Enable A Enables interrupt requests by the TGFA bit when TGIEA = b'1.	1
TSTR			Timer Start Register	H'C0
	7	CTS4	Counter Start 4 When CTS4 = b'1, TCNT_4 starts counting.	1
	6	CTS3	Counter Start 3 When CTS3 = b'1, TCNT_3 starts counting.	1
	5	—	Reserved	0
	4	—		0
	3	—		0
	2	CTS2	Counter Start 2 When CTS2 = b'0, TCNT_2 stops counting.	0
	1	CTS1	Counter Start 1 When CTS1 = b'0, TCNT_1 stops counting.	0
	0	CTS0	Counter Start 0 When CTS0 = b'0, TCNT_0 stops counting.	0

4.3 Arguments

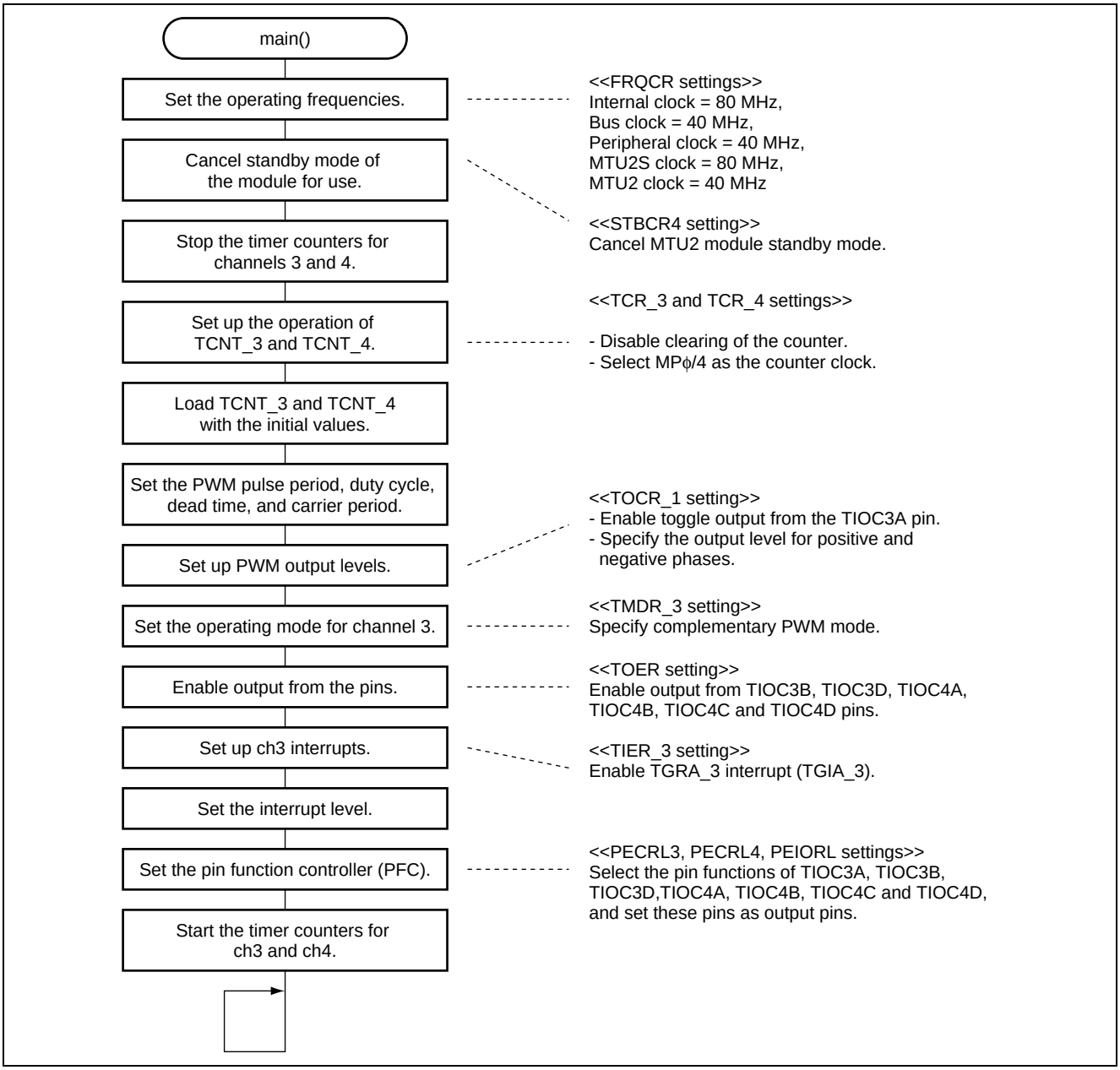
Table 4 describes the arguments used in this sample task.

Table 4 Description of Arguments

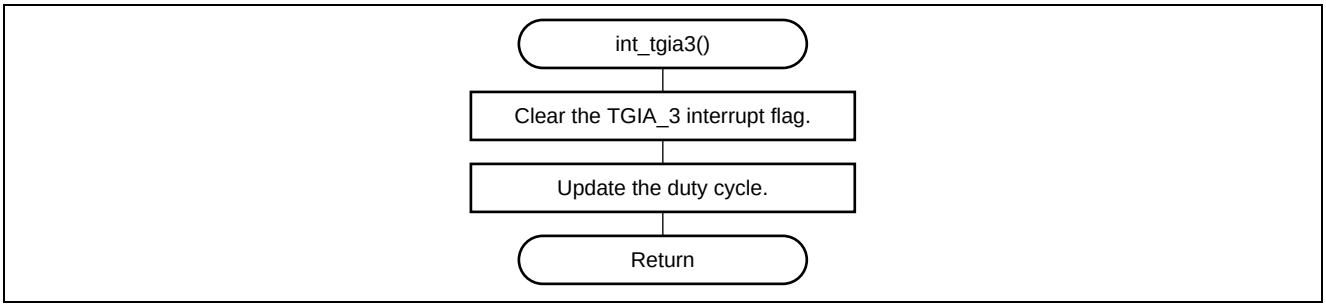
Label	Description	Used in
Pul_duty3d	Duty cycle of the PWM waveforms output from the TIOC3D pin (set in TGRD_3)	Main routine, TGRA_3 compare-match interrupt routine
Pul_duty4c	Duty cycle of the PWM waveforms output from the TIOC4C pin (set in TGRC_4)	
Pul_duty4d	Duty cycle of the PWM waveforms output from the TIOC4D pin (set in TGRD_4)	
Dead_time	Dead time (set in TDDR)	Main routine
C_cycle	PWM carrier period / 2 (set in TCBR)	
Pul_cycle	Pulse period / 2 + dead time (set in TGRC_3)	

5. Flowchart

5.1 Main Routine



5.2 TGRA_3 Compare-Match Interrupt Routine



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Customer Support Center:

Please email the following address for information on products of Renesas Technology, Corp.

csc@renesas.com

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Mar.04.05	—	First edition issued

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