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Renesas Electronics Corporation

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SH7000 Series

32 Bit × 32 Bit = 64 Bit (Unsigned)

Label: MULU32

Functions Used: MULU Instruction
SWAP Instruction

Contents

1. Function

Multiplies the multiplicand (unsigned 32 bits) by the multiplier (unsigned 32 bits) and determines the product (unsigned 64 bits).

2. Arguments

Description		Storage Location	Data Length (Bytes)
Input	Multiplicand (unsigned 32 bits)	R0	4
	Multiplier (unsigned 32 bits)	R1	4
Output	Upper 32 bits of product (unsigned 64 bits)	R2	4
	Lower 32 bits of product (unsigned 64 bits)	R3	4

3. Internal Register Changes and Flag Changes

	(Before Execution) → (After Execution)
R0	Multiplicand (unsigned 32 bits) → No change
R1	Multiplier (unsigned 32 bits) → No change
R2	Undefined → Product (upper 32 bits)
R3	Undefined → Product (lower 32 bits)
R4	Work
R5	Work
R6	Work
R7	
R8	
R9	
R10	
R11	
R12	
R13	
R14	
R15	(SP)

T bit | * |

— : No change
* : Change
0 : Fixed 0
1 : Fixed 1

4. Programming Specifications

Program memory (bytes)
76
Data memory (bytes)
0
Stack (bytes)
24
Number of states
35
Reentrant
Yes
Relocation
Yes
Intermediate interrupt
Yes

5. Notes

The number of states indicated in the programming specifications is the value when H'FFFFFFFF × H'FFFFFFFF is calculated.

6. Description

(1) Function

Details of the arguments are as follows.

R0: Set the multiplicand (unsigned 32 bits) as the input argument.
R1: Set the multiplier (unsigned 32 bits) as the input argument.
R2: Holds the upper 32 bits of the product (unsigned 64 bits) as the output argument.
R3: Holds the lower 32 bits of the product (unsigned 64 bits) as the output argument.

Figure 1 shows a software MULU32 execution example.

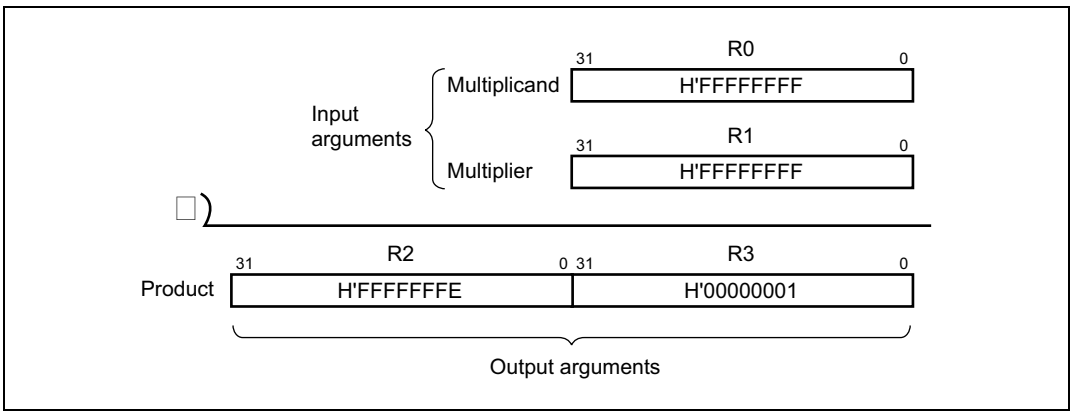


Figure 1 Software MULU32 Execution Example

(2) Usage Notes

There are no particular precautions for the software MULU32 instruction.

(3) RAM Used

No RAM is used by the software MULU32 instruction.

(4) Usage Example

After the multiplicand and multiplier are set, the software instruction MULU32 is executed by a subroutine call.

```
          MOV.L   DATA1,R0      .... Sets multiplicand in input argument (R0)
          BSR     MULU32        .... Subroutine call to software instruction MULU32
          MOV.L   DATA2,R1      .... Sets multiplier in input argument (R1)
                 .
                 .
                 .
                 .
        .align    4
DATA1   .data.l   H'FFFFFFFF
DATA2   .data.l   H'FFFFFFFF
```

(5) Operating Principle

As shown in figure 2, multiplication is performed in 16 bit units. Partial products (1–4) are determined, and these are added to get the final product (64 bits). The 16-bit unsigned multiplication instruction (MULU) is used to multiply the partial products.

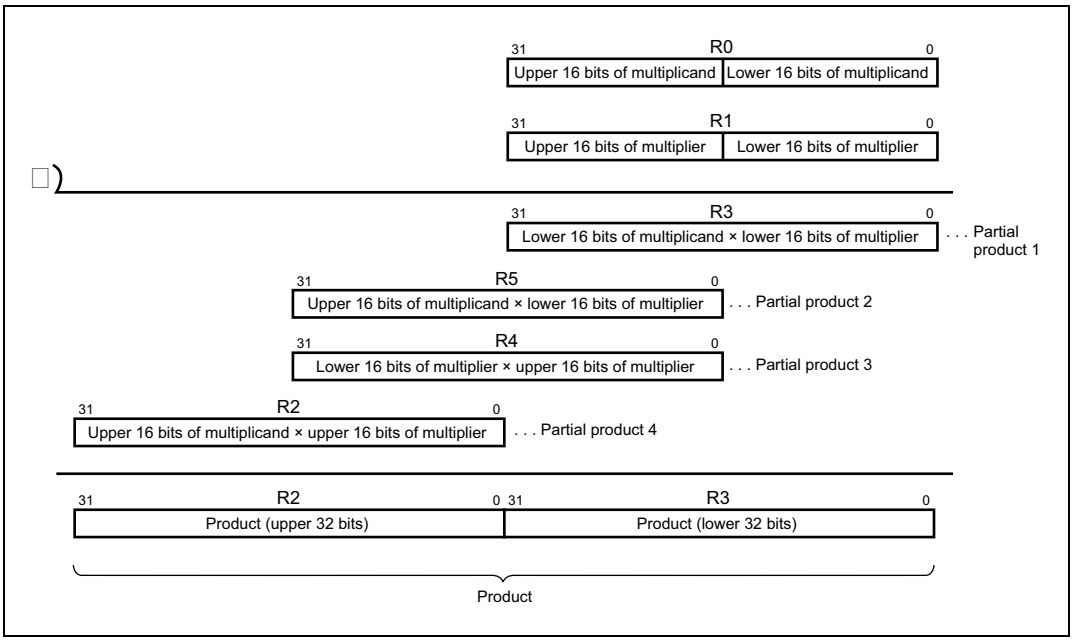
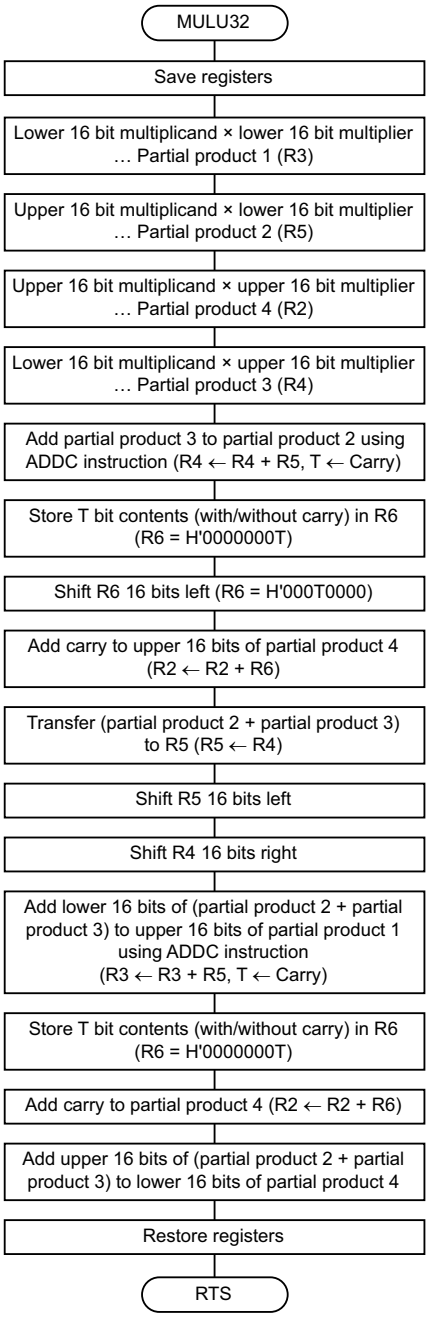


Figure 2 Multiplication

7. Flowchart


MULU32
Save registers
Lower 16 bit multiplicand × lower 16 bit multiplier … Partial product 1 (R3)
Upper 16 bit multiplicand × lower 16 bit multiplier … Partial product 2 (R5)
Upper 16 bit multiplicand × upper 16 bit multiplier … Partial product 4 (R2)
Lower 16 bit multiplicand × upper 16 bit multiplier … Partial product 3 (R4)
Add partial product 3 to partial product 2 using ADDC instruction (R4 ← R4 + R5, T ← Carry)
Store T bit contents (with/without carry) in R6 (R6 = H'0000000T)
Shift R6 16 bits left (R6 = H'000T0000)
Add carry to upper 16 bits of partial product 4 (R2 ← R2 + R6)
Transfer (partial product 2 + partial product 3) to R5 (R5 ← R4)
Shift R5 16 bits left
Shift R4 16 bits right
Add lower 16 bits of (partial product 2 + partial product 3) to upper 16 bits of partial product 1 using ADDC instruction (R3 ← R3 + R5, T ← Carry)
Store T bit contents (with/without carry) in R6 (R6 = H'0000000T)
Add carry to partial product 4 (R2 ← R2 + R6)
Add upper 16 bits of (partial product 2 + partial product 3) to lower 16 bits of partial product 4
Restore registers
RTS

8. Program Listing

```
 1                          1  ;*************************************************************
 2                          2  ;*                                                           *
 3                          3  ;*        NAME ; 32 BIT UNSIGNED MULTIPLATION (MULU32)       *
 4                          4  ;*                                                           *
 5                          5  ;*************************************************************
 6                          6  ;*                                                           *
 7                          7  ;*      ENTRY : R0 (MULTIPLICAND)                            *
 8                          8  ;*              R1 (MULTIPLIER)                              *
 9                          9  ;*    RETURNS : R2 (UPPER 32 BIT PRODUCT)                    *
10                         10  ;*              R3 (LOWER 32 BIT PRODUCT)                    *
11                         11  ;*                                                           *
12                         12  ;*************************************************************
13 00001000                13          .SECTION A,CODE,LOCATE=H'1000
14          00001000       14  MULU32  .EQU    $           ; Entry point
15 00001000 4F12           15          STS.L   MACL,@-R15  ; Escape register
16 00001002 2F46           16          MOV.L   R4,@-R15    ;
17 00001004 2F56           17          MOV.L   R5,@-R15    ;
18 00001006 2F66           18          MOV.L   R6,@-R15    ;
19                         19                              ;
20 00001008 201E           20          MULU    R1,R0       ; Lower 16 bit + lower 16 bit -> R3
21 0000100A 6009           21          SWAP.W  R0,R0       ;
22 0000100C 031A           22          STS     MACL,R3     ;
23 0000100E 201E           23          MULU    R1,R0       ; Upper 16 bit + lower 16 bit -> R5
24 00001010 6119           24          SWAP.W  R1,R1       ;
25 00001012 051A           25          STS     MACL,R5     ;
26 00001014 201E           26          MULU    R1,R0       ; Upper 16 bit + upper 16 bit -> R2
27 00001016 6009           27          SWAP.W  R0,R0       ;
28 00001018 021A           28          STS     MACL,R2     ;
29 0000101A 201E           29          MULU    R1,R0       ; Lower 16 bit + upper 16 bit -> R4
30 0000101C 6119           30          SWAP.W  R1,R1       ;
31 0000101E 041A           31          STS     MACL,R4     ;
32                         32                              ;
33 00001020 0008           33          CLRT                ;
34 00001022 345E           34          ADDC    R5,R4       ;
35 00001024 0629           35          MOVT    R6          ; R6 <- Carry
36 00001026 4628           36          SHLL16  R6          ;
37 00001028 326C           37          ADD     R6,R2       ; Carry = 1  R2 <- R2 + H'0001000
38                         38                              ; Carry = 0  R2 <- R2 + H'0000000
39 0000102A 6543           39          MOV     R4,R5       ;
40 0000102C 4528           40          SHLL16  R5          ;
41 0000102E 4429           41          SHLR16  R4          ;
42                         42                              ;
43 00001030 0008           43          CLRT                ;
44 00001032 335E           44          ADDC    R5,R3       ;
45 00001034 0629           45          MOVT    R6          ; R6 <- Carry
46 00001036 326C           46          ADD     R6,R2       ; Carry = 1  R2 <- + H'00000001
47                         47                              ; Carry = 0  R2 <- + H'00000000
48 00001038 324C           48          ADD     R4,R2       ;
49                         49                              ;
```

```
 50 0000103A 66F6          50          MOV.L   @R15+,R6    ; Return register
 51 0000103C 65F6          51          MOV.L   @R15+,R5    ;
 52 0000103E 64F6          52          MOV.L   @R15+,R4    ;
 53 00001040 000B          53          RTS                 ;
 54 00001042 4F16          54          LDS.L   @R15+,MACL  ;
 55                        55          .END
*****TOTAL ERRORS    0
*****TOTAL WARNINGS  0
```

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