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H8S Family

SDRAM Control

Introduction

This sample task connects the SDRAM to the H8S microcomputer by using the SDRAM control function of the bus controller.

Target Device

H8S/2377R

Contents

1. Overview

This sample task connects the SDRAM to the H8S microcomputer by using the SDRAM control function of the bus controller.

2. Configuration

Table 1 shows the configuration of this sample task.

Table 1 Configuration of This Sample Task

Part	Specification
H8S/2377 CPU board (CPU mounted: H8S/2377R) Product code: HSB8S2377F (Manufactured by Hokuto Denshi Co., Ltd.)	Board power supply input: 3.3 V DC Operating frequency: 19.6608 MHz MCU operating mode: 4
SYNCRONOUS DRAM Product code: MT48LC4M16A2 (manufactured by Micron Technology Inc.)	Power supply for operation: 3.3 V DC Capacity: 1 Mwords × 16 bits × 4 banks Refresh cycle: 64 ms/4,096 cycles
Debugger High-performance Embedded Workshop	Version 4.03.00.001
Compiler H8S, H8/300,C/C++ Complier	Version 6.2.0.0
On-chip debugging emulator E10A-USB Type No.: HS0005KCU02H	

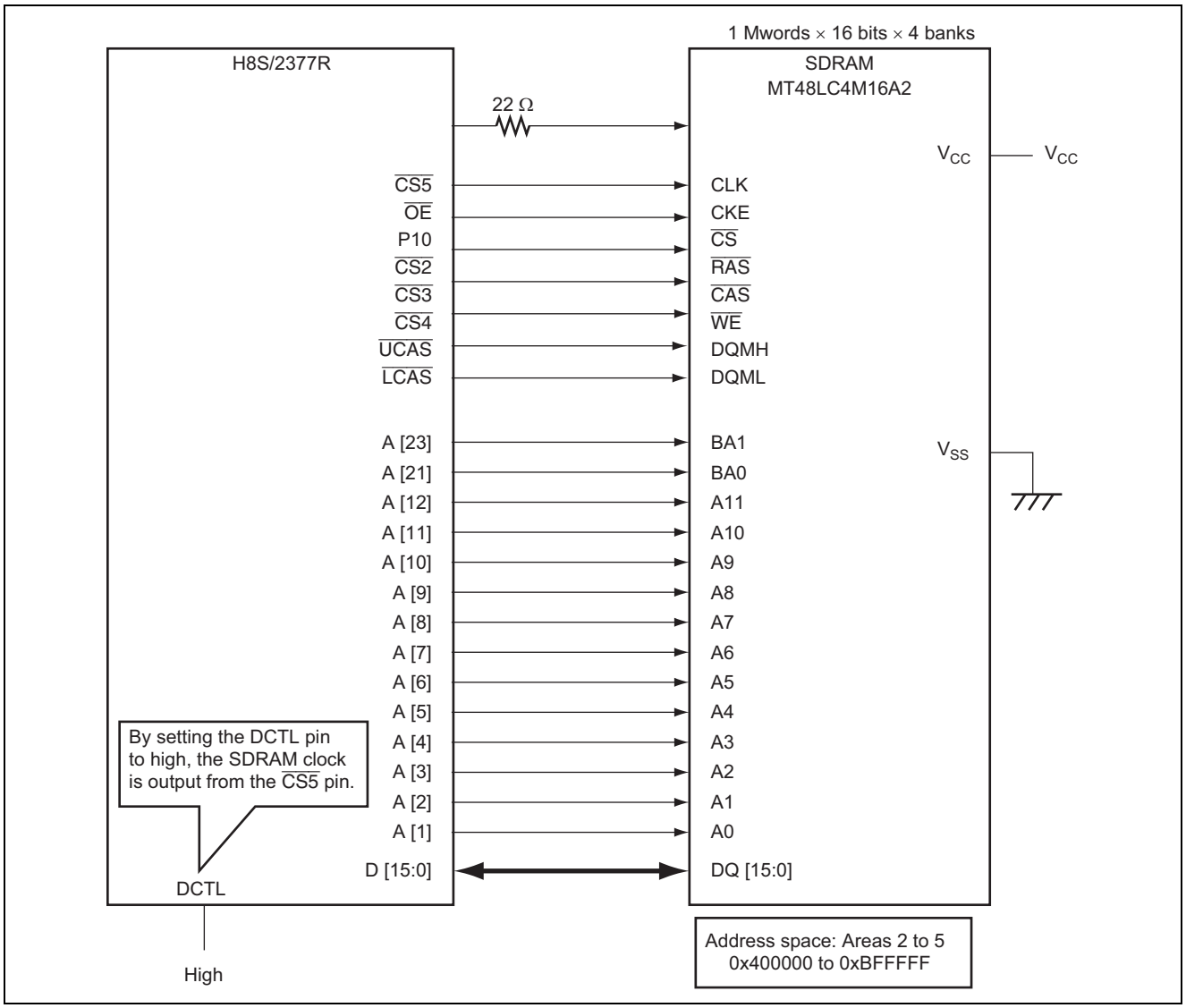

Figure 1 Connections between H8S/2377R and SDRAM

3. Description of Functions

By using the SDRAM control function of the bus controller, this sample task directly links the SDRAM to the H8S microcomputer, writes the fixed value 0x12345678 to address 0x400000, reads the address, and stores it in the on-chip RAM area read_data.

Table 2 Description of Functions

On-Chip RAM Area Name	Data Size	Function
read_data	unsigned long	Area to store data read from the SDRAM

4. Description of Operation

4.1 SDRAM Commands

The SDRAM is controlled by commands which consist of combinations of high and low levels of the control signals. The following shows the commands supported by the H8S microcomputer and the high and low combinations for each command. The command abbreviations shown in the table are also used in the following descriptions.

Command Name	Abbreviation	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	ADDR	DQ
COMMAND INHIBIT	DESL	H	×	×	×	×	×	×
NO OPERATION	NOP	L	H	H	H	H	×	×
ACTIVE (Selects a bank and activates a row)	ACTV	L	L	H	H	×	Bank/row	×
READ (Selects a bank and a column, and reads)	READ	L	H	L	H	L	Bank/column	×
WRITE (Selects a bank and a column, and writes)	WRITE	L	H	L	L	L	Bank/column	×
PRECHARGE SELECT BANK	PRE	L	L	H	L	×	Bank, A10 = low	×
PRECHARGE ALL BANK	PAL	L	L	H	L	×	A10 = high	×
AUTO-/SELF-REFRESH	REF	L	L	L	H	×	×	×
LOAD-MODE REGISTER	MRS	L	L	L	L	×	Setting value	×

4.2 Initialization Processing

4.2.1 Processing Procedure

Before the SDRAM can be accessed, appropriate settings must be performed in order to enable use of the SDRAM.

(1) COMMAND INHIBIT (DESL) State Setting

After power-on, the following initialization must be performed and the SDRAM interface must be placed in the COMMAND INHIBIT (DESL) state for 100 µs or more.

Register Name	Bit	Name	Value	Description	Reference Section
P1DDR	7 to 0	—	0x01	Sets the CS pin to high to set the SDRAM interface to COMMAND INHIBIT (DESL) state.	—
P1DR	0	P10DR	1		

(2) SDRAM-Related Register Setting

After the SDRAM-related registers are set, CS is fixed to low and the SDRAM interface is set to the NO OPERATION (NOP) state for 100 µs or more.

Register Name	Bit	Name	Value	Description	Reference Section
DRAMCR	10 to 8	RMT2 to RMT0	4	SDRAM Space Setting Areas 2 to 5: SDRAM space	4.2.2 (1)
DRAMCR	2, 1	MXC2 to MXC0	4	Address Multiplexing Setting (Sets the amount of row address shift.) Sets to 8 bits.	4.2.2 (2)
PADDR	7 to 0	—	0xA0	Address Bus Setting Sets address output for A23, A21 and A12 to A1	4.2.2 (3)
PBDDR	7 to 0	—	0x1F		
PCDDR	7 to 0	—	0xFE		
ABWCR	2	ABW2	0	Data Bus Width Setting Sets to 16 bits.	4.2.2 (4)
PFCR0	3	CS3E	1	RAS and CAS Pin Settings Sets the PG3 pin as the CAS pin.	—
PFCR0	2	CS2E	1	Sets the PG2 pin as the RAS pin	
PFCR0	4	CS4E	1	WE Pin Setting Sets the PH0 pin as the WE pin.	—
PFCR2	1	OES	1	CKE Pin Setting Sets the PH3 pin as the CKE pin.	—
DRAMCR	15	OEE	1		
DRACCR	11	SDWCD	0	Sets the CAS latency to 3	4.2.2 (5)
WTCRH	10 to 8	W22 to W20	2		
DRACCR	9, 8	RCD1, RCD0	0	Row Address Output State Setting (Controls wait between ACTV and READ/WRITE) Sets to no wait.	
DRACCR	13, 12	TPC1, TPC0	0	Precharge State Count Setting Sets to 1 state between PAL and ACTV	
DRAMCR	7	BE	1	Burst Access Mode Setting Enables burst mode.	4.2.2 (6)
REFCR	13, 12	RCW1, RCW0	0	Refresh Control Wait State Insertion Between PAL and REF: 1 state with no wait state insertion	4.2.2 (5)
REFCR	5,4	RLW1, RLW0	0	Between REF and ACTV: 3 states with no wait state insertion	
P1DR	0	P10DR	0	Pulls the CS pin to low and places the SDRAM interface in NO-OPERATION (NOP) state.	—

(3) Precharge and Auto-Refresh Command Execution

PRECHARGE and AUTO-REFRESH commands are activated with the following settings. After activation, a short loop is performed for around 1 ms, and the AUTO-REFRESH command (REF) is executed eight times or more to reset the SDRAM control circuit.

A refresh is enabled at this time to reset the SDRAM control circuit. Therefore, the refresh cycle is set to a short period.

Register Name	Bit	Name	Value	Description	Reference Section
RTCNT	7 to 0	—	0x00	Resets the refresh counter.	4.2.2 (7)
RTCOR	7 to 0	—	4	Sets refresh interval to 510 ns. ϕ (19.6608 MHz) / 2 × 5 = 510 ns	
REFCR	7	RFSHE	1	Enables refresh.	
REFCR	10 to 8	RTCK2 to RTCK0	1	The refresh counter starts counting with input of ϕ/2 to issue REF commands.	
REFCR	7	RFSHE	0	Disables refresh.	
REFCR	10 to 8	RTCK2 to RTCK0	0	Stops counting	

(4) Initial Setting of SDRAM Mode Register

The SDRAM internal registers are set in the following procedure. Note that these register settings must match the timing of the signals issued by the H8S microcomputer for operation.

To enable the mode register setting of the SDRAM, the RMTS2 to RMTS0 bits in DRAMCR must be set to H'5. If value X needs to be set to the SDRAM mode register, a write to address H'400000 + X is required for the 8-bit SDRAM and a write to address H'400000 + 2X for the 16-bit bus SDRAM.

The SDRAM mode register is set by an address signal value at the time of MRS command issuance.

The H8S microcomputer does not support the SDRAM burst-read / burst-write mode. Only the burst-read / single-write mode can be selected and the burst length should be set to 1.

The following shows the mode setting values:

Bit	Name	Description	Setting Value: 0x230
11, 10	Reserved		00
9	WB	Write Burst Mode	1
8, 7	Op Mode	Operating Mode	00

M9	Write Burst Mode
0	Programmed Burst Length
1	Single Location Access

M8	M7	M6-0	Operating Mode
0	0	Defined	Standard Operation
—	—		All other states reserved

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th><th>Setting Value: 0x230</th></tr>
<tr><td>6 to 4</td><td>CAS latency</td><td>CAS Latency
<table>
<tr><th>M6</th><th>M5</th><th>M4</th><th>CAS Latency</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Reserved</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Reserved</td></tr>
</table></td><td>011</td></tr>
<tr><td>3</td><td>BT</td><td>Burst Type
<table>
<tr><th>M3</th><th>Burst Type</th></tr>
<tr><td>0</td><td>Sequential</td></tr>
<tr><td>1</td><td>Interleaved</td></tr>
</table></td><td>0</td></tr>
<tr><td>2 to 0</td><td>Burst Length</td><td>Burst Length
<table>
<tr><th></th><th></th><th></th><th colspan="2">Burst Length</th></tr>
<tr><th>M2</th><th>M1</th><th>M0</th><th>M3 = 0</th><th>M3 = 1</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>2</td><td>2</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>4</td><td>4</td></tr>
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<tr><td>1</td><td>1</td><td>1</td><td>Full Page</td><td>Reserved</td></tr>
</table></td><td>000</td></tr>
</table>

(5) Restart of AUTO-REFRESH Command

The AUTO-REFRESH command is activated with the following settings.

A refresh is enabled at this time to precharge (re-charge) for operation. Therefore, the refresh interval should be set as long as possible within the SDRAM specifications.

Register Name	Bit	Name	Value	Description	Reference Section
RTCNT	7 to 0	—	0x00	Resets the refresh counter.	4.2.2 (7)
RTCOR	7 to 0	—	152	Sets refresh interval within 64 ms/4,096 cycles.	
REFCR	7	RFSHE	1	Enables refresh.	
REFCR	10 to 8	RTCK2 to RTCK0	1	The refresh counter starts counting with input of ϕ/2 to issue REF commands.	

(6) Continuous SDRAM Space Setting

Lastly, the following settings will complete SDRAM initialization.

Register Name	Bit	Name	Value	Description	Reference Section
DRAMCR	10 to 8	RMT2 to RMT0	4	Continuous SDRAM Space Setting Areas 2 to 5: SDRAM space	4.2.2 (1)

The above settings enable reading or writing to the SDRAM.

4.2.2 Supplement

The following gives additional explanation for each processing described in section 4.2.1.

(1) SDRAM Space Setting

The address space for the H8S microcomputer is divided into eight areas in units of 2 Mbytes. A bus can be set for each area. The SDRAM can occupy consecutive areas 2 to 5. This sample task uses 8-Mbyte SDRAM (1 Mwords × 16 bits × 4 banks) with an available address range of 0x400000 to 0xBFFFFF.

(2) Address Multiplexing Setting

The SDRAM space is multiplexed in terms of row and column addresses. Therefore, the amount of a row-address shift needs to be set according to the address width (memory capacity) of the SDRAM to be used. Because the SDRAM used in this application note has the column address width of 8 bits, the row-address shift amount is also set to 8 bits.

(3) Address Bus Setting

To use as an address bus, the output mode must be set using the DDR register of the I/O port.

(4) Data Bus Setting

The data width (16 bits) for the SDRAM used in the application note must be set. Note that because access is made in units of 16 bits, the least significant bit of an address is not connected, and that connections are shifted by 1 bit. (See the connection diagram in section 2, Configuration.)

(5) Signal Timing Adjustment

Appropriate settings must be provided according to the AC characteristic of the SDRAM to be connected and the operating frequency of the microcomputer.

The figure below shows fundamental access timing in the SDRAM READ/WRITE and REF (auto-refresh).

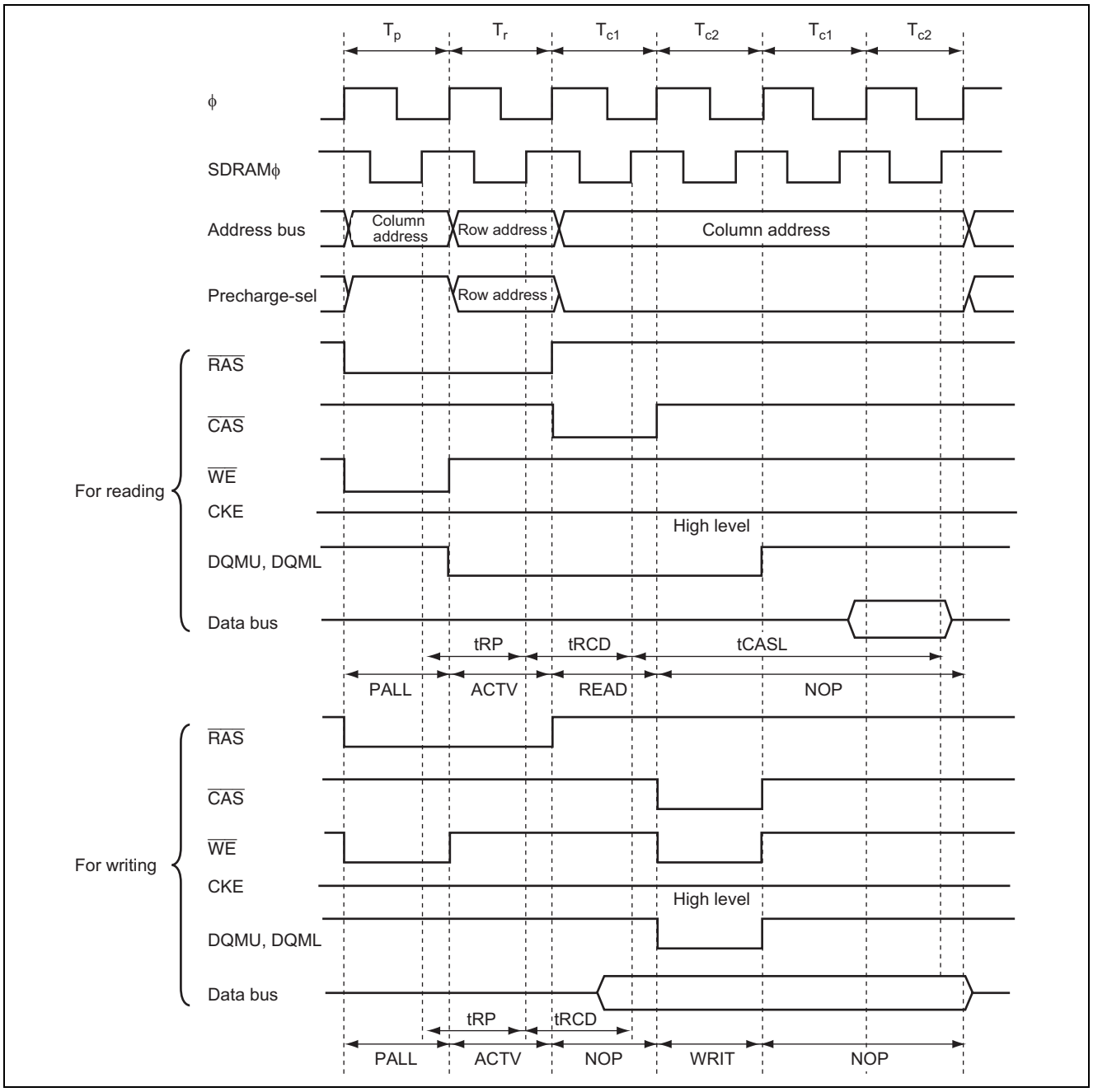


Figure 2 Fundamental Access Timing of SDRAM (1)

Table 3 Fundamental Access Timing of SDRAM (1)

Symbol	Description	SDRAM Specification	Microcomputer Access Timing	Register to Adjust Timing
ϕ	Access cycle	—	19.6608 MHz, 50.86 ns	—
tCASL	CAS latency: 0	2 or 3 cycles	3 cycles	WCR (W2)
tRCD	Wait cycle between ACTV and READ/WRITE	Min. 20 ns	ϕ = 50.86 ns	DRACCR (RCD)
tRP	Wait cycle between PALL and ACTV	Min. 20 ns	ϕ = 50.86 ns	DRACCR (TPC)

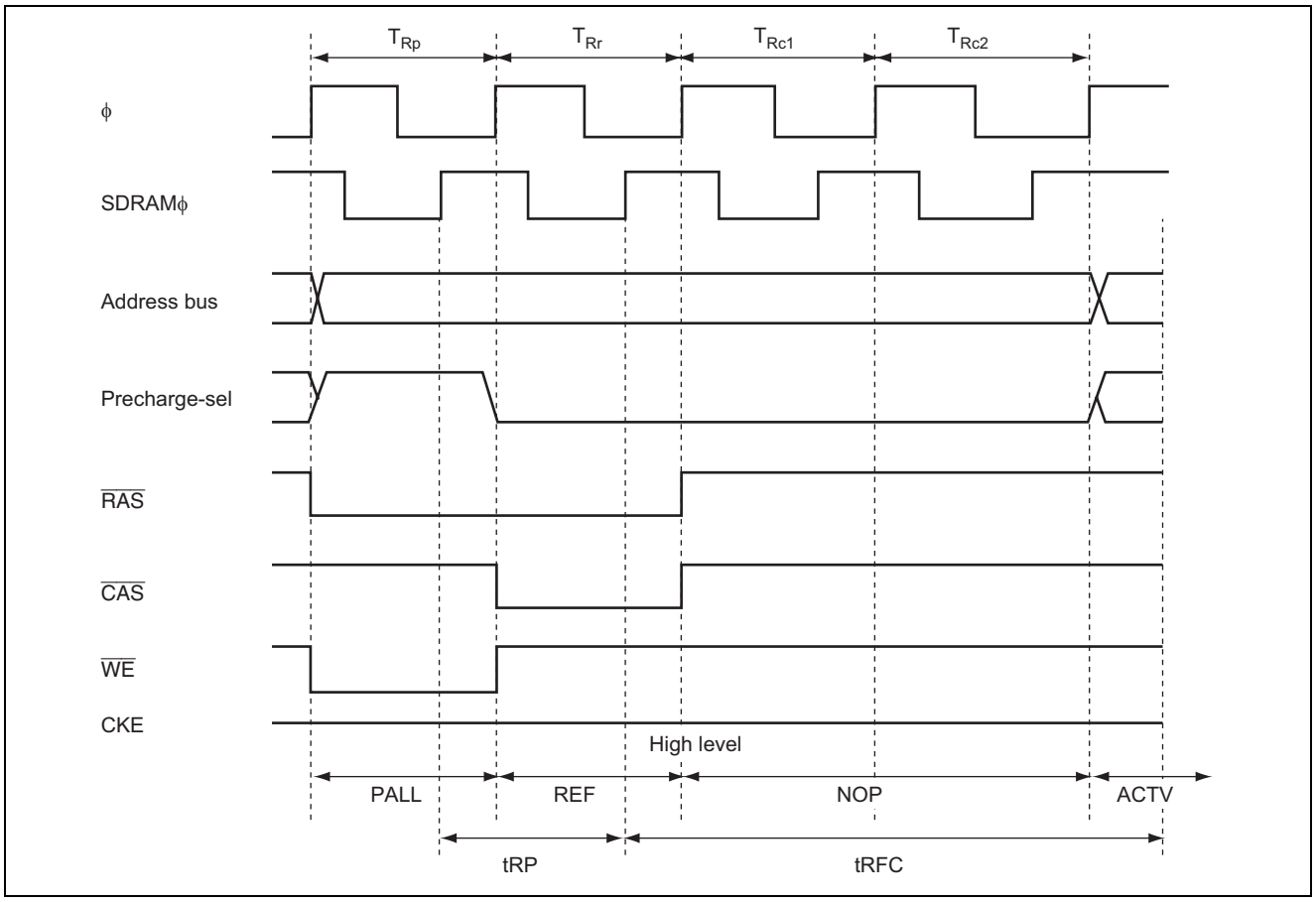


Figure 2 Fundamental Access Timing of SDRAM (2)

Table 3 Fundamental Access Timing of SDRAM (2)

Symbol	Description	SDRAM Specification	Microcomputer Access Timing	Register to Adjust Timing
tRP	Wait cycle between PALL and REF	Min. 20 ns	ϕ = 50.86 ns	REFCR (RCW)
tRFC	Wait cycle between REF and ACTV	Min. 66 ns	3ϕ = 152.58 ns	REFCR (RLW)

As indicated in the above table, the SDRAM used in the application note can be accessed at fundamental access timing. If a given access timing cannot meet the SDRAM specifications, it can be modified using the timing adjustment register. For details, refer to the hardware manual.

(6) Burst Access Mode Setting

The burst mode refers to a mode that permits high-speed data access when identical row addresses are encountered in succession, by simply changing column addresses after the row address is output. When row addresses are identical, even if access to other space is provided, the SDRAM can be accessed without issuing the ACTV command, simply by changing the column addresses (issuing the READ or WRITE command).

(7) Refresh Control Setting

In accordance with SDRAM specifications, an auto- refresh can be issued at fixed intervals.

In this application note, 15.563 µs is set so that refresh is executed.

SDRAM Refresh

64 ms/4,096 cycles = 15.625µs

Refresh Timing of This Application

Operating frequency 19.6608 MHz = 50.86 ns

Counting at ϕ/2, 15.625 µs / (50.86 ns $\times$ 2) $\approx$ 153

50.86 ns $\times$ 2 $\times$ 153 $\approx$ 15.563 µs

For 15.563 µs < 15.625 µs, 152 (153 – 1) is set in the RTCOR register.

4.3 SDRAM Access

The above settings enable access to the SDRAM.

For this application, the SDRAM space is 0x400000 to 0xBFFFFF, with an access unit of 2 bytes.

5. Description of Sample Program

5.1 File Configuration

The sample program is provided as a project of the HEW (High-performance Embedded Workshop).

By executing H8S_2377_2.hws, the High-performance Embedded Workshop starts up and source program can be referenced or updated. If the user has no High-performance Embedded Workshop, refer to the following source files directly using editors.

Table 4 File Configuration

File Name	Specification
resetprg.c	Executed from reset vector address 0 if the MCU is reset.
intprg.c	Executed if an interrupt other than a reset occurs.
dbsct.c	Sets start and end addresses of the section used by _INITSCT function in resetprg.c to section initialization table. For details, refer to sections 9 and 10 in the H8S, H8/300H Series C/C++ Compiler, Assembler, and Optimization Linkage Editor User's Manual.
H8S_2377_2.c	Main routine of this sample task.
iodefine.h	Configuration definition file of internal registers.
stacksct.h	Defines stack size.

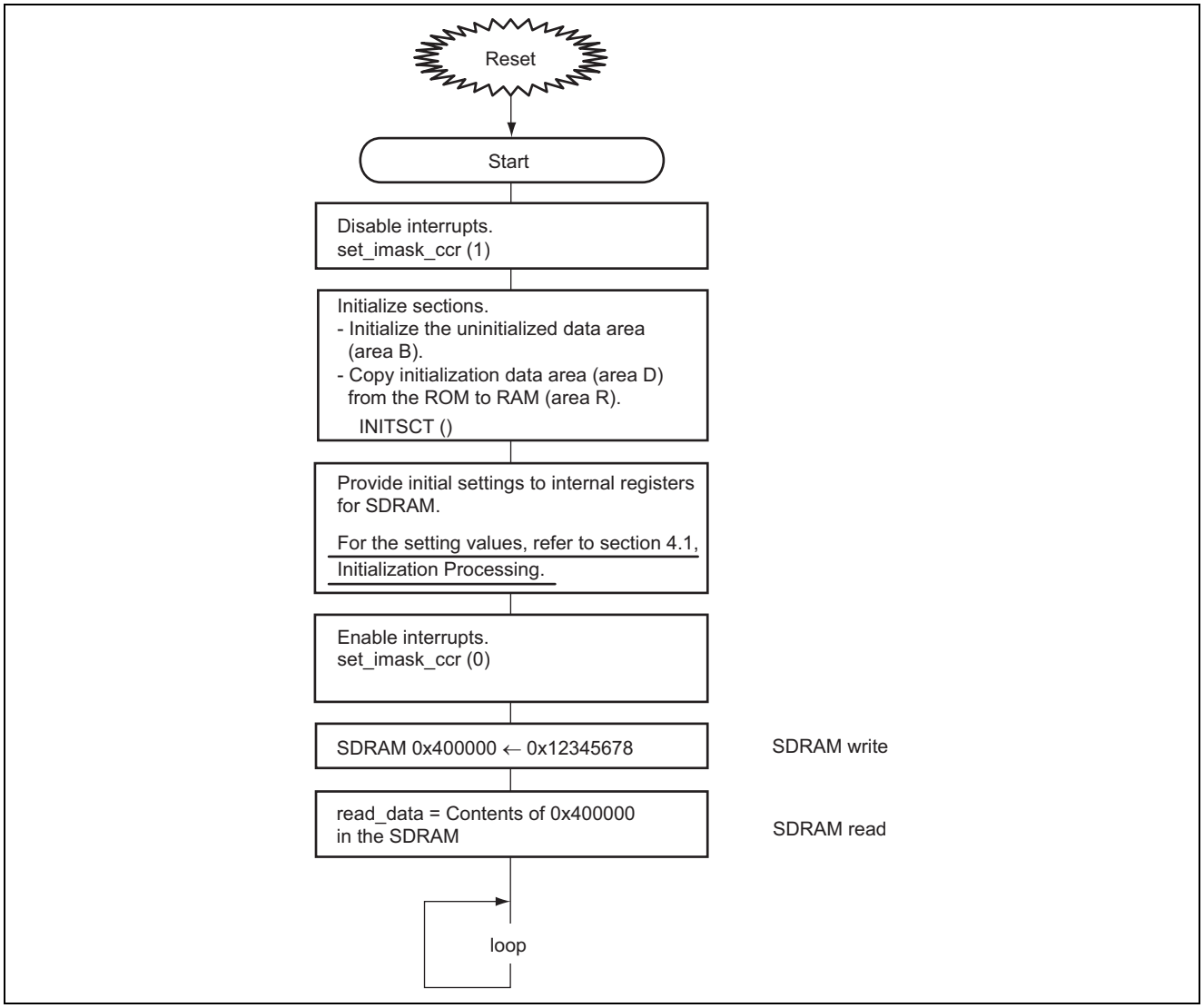
5.2 Linkage

The linkage addresses of each section are as follows.

In the HEW project files, the linkage addresses can be referenced and set by Category: section of Link/librarq tab in option –Standard Toolchain.

Section	Start Address
PResetPRG	0x000400
PIntPRG	
P	0x000800
C$DSEC	
C$BSEC	
D	
B	0xFF6000
R	
S	0xFFBDF0

6. Flowchart



References

Document Name	How to Get the Document
H8S/2378, H8S/2378R Group Hardware Manual	Download from the website of Renesas Technology Corp.
SDRAM MT48LC4M16A2 Data Sheet	Download from the website of Micron Technology Inc.
Usage of SDRAM	Download from the website of Elpida Memory Inc.

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Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Mar.09.05	—	First edition issued
2.00	Dec.12.07	—	Correction on refresh timing

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