RYZ024A

Module Integration Guide

Introduction

This application note is intended to help customers who want to deviate from the Renesas' reference designs to successfully integrate and test their product based on an RYZ024A module.

This document presents Integration Guidelines for:

- All RYZ024A interface requirements
- Tips and "how-to"s for troubleshooting

Development of the hardware should follow a process that ensures the solution will be optimum and it is the purpose and goal of this document to reach this. For this to occur, we recommend that these processes are followed in order. This document is delivered as three sections:

1. System Overview
2. Hardware and software design guidelines
3. Bring-up verification and test

Caution: It is highly recommended that Renesas support teams are involved during all processes to ensure the very best can be achieved for the alternative design.

Who Should Read this Document

This Application Note is for hardware designers of user applications based on the Renesas RYZ024A module.

Important: **-** Reference design source files are based on the application PADS® from Mentor Graphics® (www.mentor.com). Customers using the other CAD applications can use schematics translators and viewers, such as Elgris® (www.elgris.com). Such translators may save time and prevent mistakes during manual PADs conversion.
- The reference design uses the RYZ024A-EVK. Please note that the RYZ024A-EVK is used for performance evaluation within Renesas and cannot be provided to users and customers.

Contents

1. Introduction

1.1 System Architecture

Figure 1 provides an overview of the Host to RYZ024A interfacing relationship. The various interfaces are explained in detail later in this document.

It provides summary details of:

- Digital interfaces between the RYZ024A and the host platform
- Power supply requirement (V_{BAT}).

Note: V_{BAT} range is 2.2 V to 5.5 V.

It does **not** show the RYZ024A local terminations.

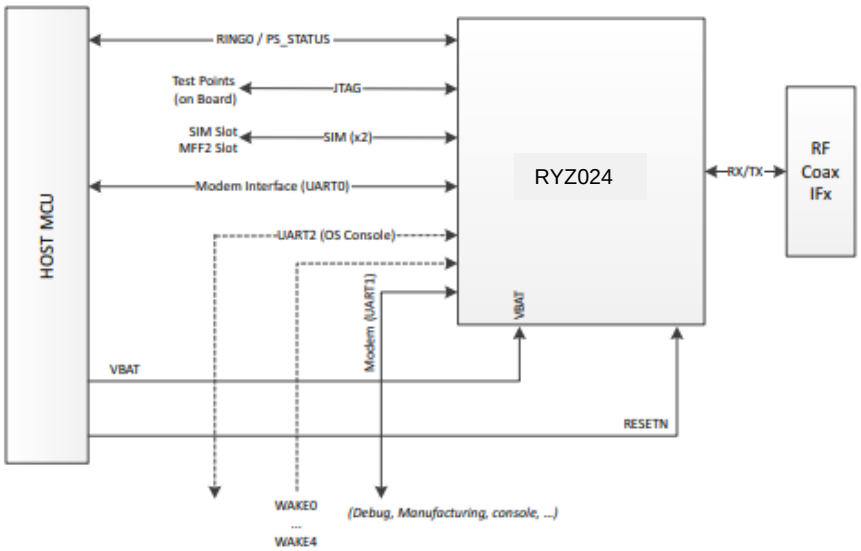

Figure 1. RYZ024A-Based System Architecture

An example of design is shown in Figure 2.

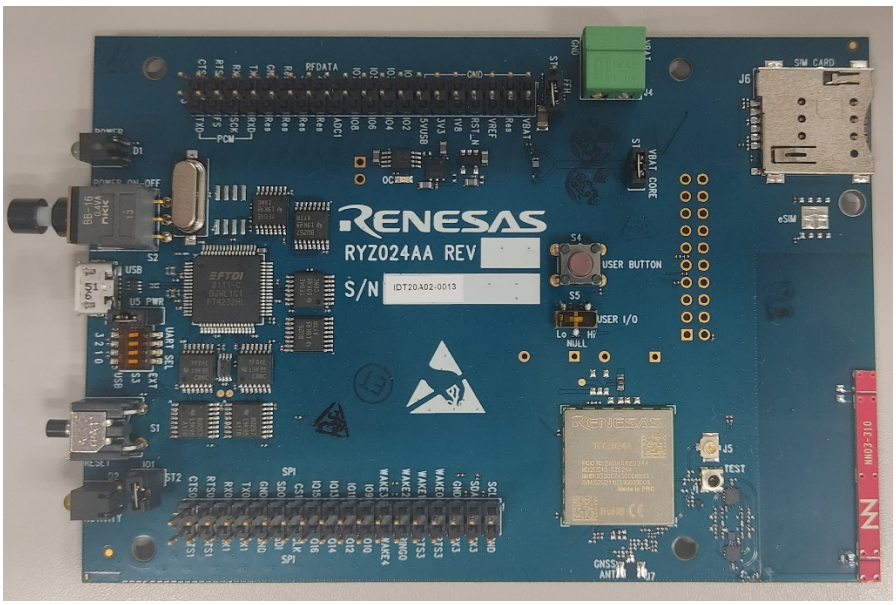

Figure 2. Module Mounted on RYZ024A-EVK Evaluation Kit

Note: The hardware design package of RYZ024A reference design is available from your Renesas local contact.

1.2 Recommended Design Flow

To ensure that the customer benefits from the details of this document we recommend carefully taking the following information into account during the design process.

1.2.1 Schematics Review

Ensure that the circuit design by analysis will be compliant with the Renesas chipset. It is recommended to follow Renesas's schematics checklist .

1.2.2 PCB Placement and Layout Review

To ensure that the PCB layout is compliant, it is recommended that the review of this CAD activity includes Renesas Schematics Checklist at several iterative steps such as the component placement, RF and digital routing, and final layout levels. This might avoid later rework.

1.2.3 Optimization

When the design returns from manufacture, it might be the case that improvements have to be made to the circuits. It is also recommended to communicate such results to Renesas who can help to verify the implementation.

1.2.4 Functional Validation

The test of the design performance should be done in thorough detail. This will ensure compliance with the test standard as the final design will be subjected to a formal qualification. It is the designer's responsibility to meet this goal. Sharing the results with Renesas will help identify any particular problem that could be fixed at an early stage to ensure strong confidence of qualification. This should be done for all the tests that involve Renesas chipsets.

Appendix: Hardware Test Preparation on page 30 provides you with the hardware setup required to proceed with test phases.

2. Hardware Integration Recommendations

This chapter provides the information necessary to understand the various interface requirements to interconnect with the RYZ024A, associated software-configurable items for the respective interface and, more generally, good practices for board design when considering the various interface types. Table 1 describes the requirements for trace characteristics.

Important: Different signals require different special treatment. Please carefully consider the interfacing requirements of each relevant connection.

Table 1. Requirements Overview: Trace Characteristics

Trace Characteristics	Description
Digital	Generic digital trace if reasonable high impedance.
Supply	Broader trace routing based on the power needs of the load.
50 Ohm	Conventionally used for RF routing. Track must be retained to this impedance.
Quiet	Intention is to keep away from digital signals and as short as possible, possibly burying the signal.
Ground	Shortest RYZ024A Ground to Host Ground possible, best possible lowest impedance path.

2.1 Power Supply

Note: More information on Power Supply dimensioning can be found in the *RYZ024A Datasheet*.

2.1.1 Synthesis of the Power Supplies

Table 2 provides a synthesis of the power supplies and their characteristics. Please see typical voltage values in the *RYZ024A Datasheet*.

Note: Each output reference voltage (pad 8) can be either running or powered off depending on the internal software configuration. They should not be used to power external IC or parts that require permanent supply.

Table 2. Power Supply Signals

Pin Name	Pin Number	Trace Style	Direction	Notes
1V8	8	Supply	Out	Reference voltage. See the note above.
SIM_VCC	73	Supply	Out	
VBAT	60, 62, 63	Supply	In	Voltage used is 2.5 V to 5.5 V for operations and 2.2 V to 5.5 V for functional behavior with possible degradation of RF performances.

2.1.2 Power Supply Circuit Example

2.1.2.1 Test Points and Measurement Access

Test point access is recommended on all supply nets so that the supply voltages can be measured.

Tracked through 0-Ohm links are recommended to be fitted on all supply nets and these can be cut (and re-fitted with 0-Ohm link later) to facilitate metering of the load currents on each supply rail. Appropriate sizing of the tracks and 0-Ohm links is advised based on the load current.

2.1.2.2 Battery Considerations

RYZ024A's voltage range allows use of a wide range of rechargeable and non-rechargeable batteries without the need of any external power supply. This is the case for Li-Po, Li-Ion, Li-MnO2 (typically coming in CR2 or CR123A format) with a nominal supply voltage above 2.5 V. In these cases, the battery can be connected directly to the module's VBAT input as shown on Figure 3.

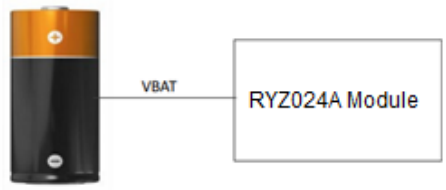

Figure 3. Direct Battery Connection

For batteries with a normal voltage lower than 2.5 V (such as single alkaline AA battery), RYZ024A recommends using a low leakage voltage booster.

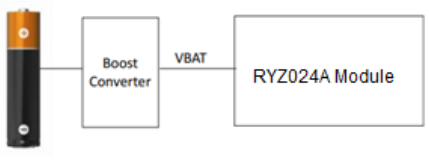

Figure 4. Battery with Boost Converter

Note: RYZ024A is still functional between 2.2 V and 2.5 V. This can be used to extract last energy out of a battery or to trigger a last gasp mechanic. But, selecting a battery whose nominal operating voltage is below 2.5 V should be avoided since, in this range, the compliance to 3GPP RF requirements is not guaranteed.

Please refer also to section 2.7.3.2, Power Supply Traces on page 20.

2.2 SIM Interface

2.2.1 Interface Description

Table 3 and Table 4 list the RYZ024A pins related to the SIM interface. SIM0 is the main external SIM interface. SIM1 can be used as a second SIM interface, typically for soldered SIM chips. If the design only has one SIM, then, it is preferred to use the main SIM0 interface.

Table 3. SIM0 Interface Signals

Pin Name	Pin Number	Trace Style	Direction	Power Group
SIM0_CLK	42	Digital	Output from Module	PVDD_1V8
SIM0_DETECT[1]	45	Digital	Input to Module	PMU_5V
SIM0_IO	44	Digital	Input or Output to/from Module	PVDD_1V8
SIM0_RESETN	43	Digital	Output from Module	PVDD_1V8
SIM0_VCC	73	Digital	Output from Module	PVDD_1V8

Note: 1. SIM0_DETECT=1 signals that a card is present. SIM0_DETECT=0 signals that no card is present.

Table 4. SIM1 Interface Signals

Pin Name	Pin Number	Trace Style	Direction	Power Group
GPIO26/SIM1_CLK	40	Digital	Output from Module	PVDD_1V8
GPIO25/SIM1_IO	39	Digital	Input or Output to/from Module	PVDD_1V8
GPIO27/SIM1_RESETN	41	Digital	Output from Module	PVDD_1V8

Note: When using SIM1, the SIM needs to be powered with external 1V8 source as the module does not supply the SIM through this interface. It is therefore recommended to use SIM0 unless a dual SIM solution is required. Please refer to the *RYZ024A AT Commands Reference Manual* to know how to enable each SIM interface and switch between SIM interfaces.

2.2.2 Other Hardware Considerations

- Use a 100 nF decoupling capacitor on SIM_VCC.
- Use a 4.7 kOhm resistor between SIM_VCC and SIM_IO.
- When considering the placement of the SIM connector and RYZ024A SIM interface, try to keep the distance between them as small as possible.
- Ensure that a good ground return exists between the SIM card and the RYZ024A.
- If the application requires the support of hot insertion or removal of SIM card, then the SIM card handler must include a removal/insertion pad detector in order to allow the software to process the event immediately. Default software configuration is to support SIM_DETECT.
- This bullet describes an option which is NOT recommended by Renesas. Renesas recommends using a SIM card socket with SIM_DETECT support.
  If the SIM card socket does not support SIM_DETECT signal, then keep the SIM_DETECT tied high (1V8) to avoid it floating and configure the platform accordingly (SIM card detection in polling mode).

2.3 Host Communications Signals

2.3.1 Introduction to UART Interfaces

The communication between the RYZ024A and the host platform is supported as follows by three UART interfaces, named UART0, UART1 and UART2. They all support flow control.

The two usages of the UART interfaces are:

- Host-Modem interface, also named “AT Commands mode”, provides an interface to modem configuration with AT commands, and application traffic data. This interface requires preferably a high-speed UART port with flow control.
- Modem Console interface, to get console logs from the LTE modem.
- Debug interface (also referred to as DCP) interface is usable for upgrade with SFU.

Table 5. UART Interfaces Usage Synthesis

UART Port	Available Usage of Port	Power Group
UART0	AT Commands	Host-Modem interface
UART1	AT Commands	Manufacturing, debug, and upgrade
UART2	Modem Console	Modem Console
UART3	Reserved, do not use	Reserved, do not use

1. UART1 is configured by default to AT Commands, but it is required that this UART is set to DCP mode at product manufacturing.

The default configuration is set as shown in Table 5 and is configurable by software.

Important: We recommend that a design based on RYZ024A provides an easy access to UART1 with hardware flow control in order to allow debugging and upgrades during the development of the product. This can be achieved with a simple UART connector or, more conveniently, with a dedicated UART-to-USB converter chip and a USB connector.

Various UART-to-USB converters were tested with platforms based on RYZ024A modules, including Exar XR21V1410™, FTDI FT234XD™, or FTDI FT4232H™. Implementation examples are available in Renesas’.

The following sections detail these interfaces.

2.3.2 UART Electrical Characteristics

Caution: The PCB designer must ensure that the voltage on these pads never exceeds V_{IH}.

Table 6. UART Pads DC Characteristics

Symbol	Minimum	Maximum	Unit
VIH Input HIGH level	1.26	3.3	V
VIL Input LOW level	0	0.54	V
VOH Output HIGH voltage	1.44	1.8	V
VOL Output LOW voltage	0	0.36	V

2.3.3 General Notes on UART Connections

RYZ024A uses the DCE-DTE convention for UART lines. It is designed for use as DCE (Data Communication Equipment).

The output from the device at one end of the link connects to the input at the other end of the link and vice versa. Figure 5 represents the typical implementation for the UART connection (including hardware flow control in case of high-speed UART).

The DCE (Data Communication Equipment) device will communicate with the customer application (DTE) using the following signals:

- Port TXD on Application sends data to the RYZ024A's TXD signal line.
- Port RXD on Application receives data from the RYZ024A's RXD signal line.

Caution: If the Host does not support flow control, then connect RTS pin to ground through 1KOhm resistor, leave CTS pin unconnected, disable flow control on the UART by using AT+SQNHWCFG command.

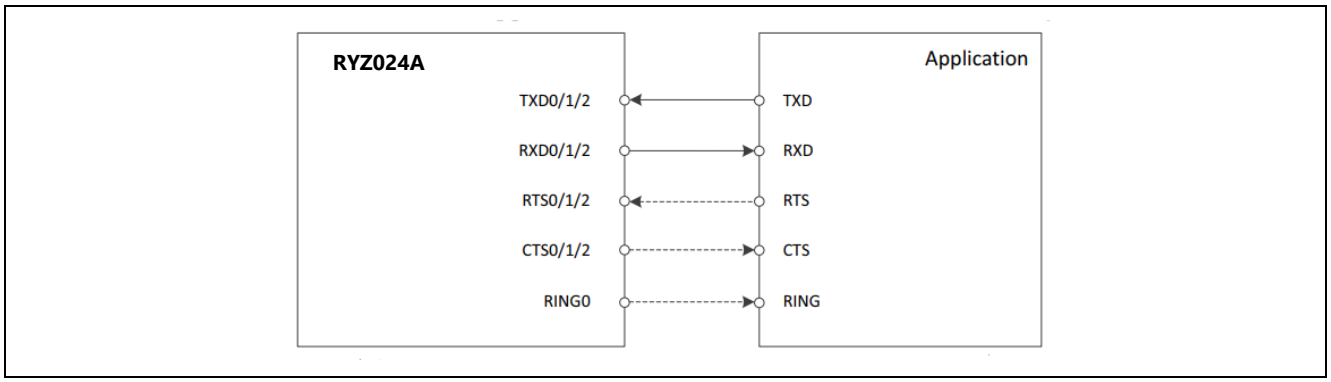

Figure 5. UART0, UART1, UART2 Connection Implementation (with hardware flow control)

Note: Refer to *RYZ024A Module System Integration Guide* for more information on the possible implementation.

2.3.4 UART0 Interface

2.3.4.1 Interface Description

Important:

- See the Section 2.3.3 General Notes on UART Connections on page 9 for usage of UART0.
- If not used, the UART0 signals should be connected to test points.
- A pull-up is recommended in UART0 RTS and CTS signals.
- It is recommended that UART0 tracks be buried inside the PCB to improve security by reducing attack surface possibility.

Table 7 lists the RYZ024A pins related to the UART0 interface.

Table 7. UART Interface Signals

Pin Name	Pin Number	Trace Style	Direction	Power Group	Notes
GPIO13/RXD0	34	Digital	Out	PVDD_1V8	UART0 RXD
GPIO12/TXD0	36	Digital	In	PVDD_1V8	UART0 TXD
RTS0	33	Digital	In	PMU_5V	UART0 RTS. A pull-up is recommended.
GPIO14/CTS0	35	Digital	Out	PVDD_1V8	UART0 CTS. A pull-up is recommended.

2.3.4.2 Default Configuration

The default software configuration of UART0 is AT Commands mode.

Important: UART0 is configured with hardware flow control (RTS0, CTS0) by default.

The serial link settings are as follows:

- Baud rate: 115200
- Data: 8 bits
- Parity: None
- Stop: 1 bit
- Flow control: Hardware (RTS/CTS)

2.3.4.3 Behavior in Low Power Mode

- The module power mode selection is internally managed by the module software.
- RTS0 signal is an input to the module. It is used by the Host to wake the module up. A pull-up is recommended on this signal either internal to the host or in the PCB. This will avoid the module waken up if the host goes in low power and does not drive RTS0.
- CTS0 is an output of the module. It signals when the module is ready to receive characters. But the modem does not drive this signal when it is in Deep Sleep. Therefore it is recommended to pull-up to this signal either internal to the host or in the PCB.

2.3.5 UART1 Interface

2.3.5.1 Interface Description

Important:

- See the Section 2.3.3 General Notes on UART Connections on page 9 for usage of UART1.
- If not used, the UART1 signals should be connected to test points.
- All pull-up is recommended in UART1 RTS signal.

Table 8 lists the RYZ024A pins related to the UART1 interface.

Table 8. UART1 Interface Signals

Pin Name	Pin Number	Trace Style	Direction	Power Group	Notes
RXD1	30	Digital	Out	PVDD_1V8	UART1 RXD.
TXD1	32	Digital	In	PVDD_1V8	UART1 TXD.
RTS1	29	Digital	In	PMU_5V	UART1 RTS. A pull-up is recommended.
CTS1	31	Digital	Out	PVDD_1V8	UART` CTS. A pull-up is recommended.

2.3.5.2 Default Configuration

The default software configuration of UART1 is debug mode. Boot traces are sent on this interface as shown on section 3.4.2 Confirm Module Power-Up Operation (UART2) on page 28.

The serial link settings are as follows:

- Baud rate: 921600
- Data: 8 bits
- Parity: None
- Stop : 1 bit
- Flow control: Hardware (RTS/CTS)

2.3.5.3 Behavior in Low Power Mode

- The module power mode selection is internally managed by the module software.
- RTS1 signal is used by the host to wake up the module.

2.3.6 UART2 Interface

2.3.6.1 Interface Description

Important:

- See the section 2.3.3 General Notes on UART Connections on page 9 for usage of UART2.
- If not used, the UART2 signals should be connected to test points.

Table 9 lists the RYZ024A pins related to the UART2 interface.

Table 9. UART2 Interface Signals

Pin Name	Pin Number	Trace Style	Direction	Power Group	Notes
GPIO16/RXD2	26	Digital	Out	1.8 V	UART2 RXD
GPIO15/TXD2	28	Digital	In	1.8 V	UART2 TXD
GPIO18/RTS2/DSR0	25	Digital	In	1.8 V	UART2 RTS
GPIO17/CTS2/DCD0	27	Digital	Out	1.8 V	UART2 CTS

2.3.6.2 Default Configuration

The default software configuration of UART2 is console mode.

The serial link settings are as follows:

- Baud rate: 115200
- Data: 8 bits
- Parity: None
- Stop : 1 bit
- Flow control: None

2.3.6.3 Behavior in Low Power Mode

UART2 cannot be used for wake from low power mode operations.

2.4 RF Interface

2.4.1 RF Signals

2.4.1.1 RF Interface Signals

Table 10. RF Interface Signals

Pin Name	Pin Number	Trace Style	Direction	Power Group	Notes
LTE_ANT	90	RF	In/Out	RF	LTE antenna. Special RF routing conditions

2.4.2 Circuit Diagram Example

Important: Figure 6 should be strictly followed as a topology reference. It is recommended not to deviate from this circuit from your application. More information is provided in this document on the layout constraint which are too very important to abide by.

The RF inter-connect called P1 is for example purposes only. Depending on the antenna, interfacing system will dictate the RF interconnect.

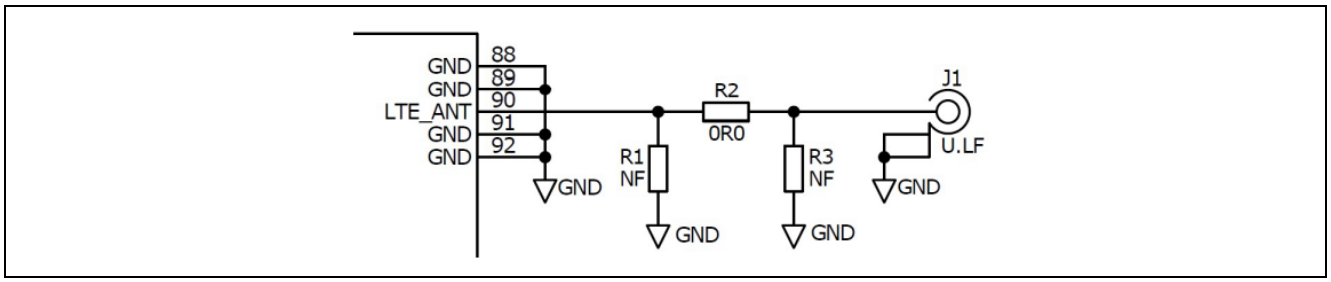

Figure 6. RF Typical Circuit

LTE_ANT is the primary (main) antenna pin and carries TX and RX signals.

Connect 50-Ohm transmission lines from this pin to the 50-Ohm Primary Antenna/Antenna-connector.

Figure 6 shows, included in the connection between LTE_ANT and the antenna connectors, Pi-type network for matching.

See Section 2.4.4 Antennas and RF Design Considerations on page 12 for more detail on connecting to these pins and for information on the Pi-type matching network and ESD protection.

2.4.3 Test Points and Measurement Access

50-Ohm termination points, for example P1 in Figure 6, are needed for Engineering and Production teams for the validation of the RF performance.

There may be a potential need to measure the RF path (as per 3.3.2.1 Test Procedure on page 27) and optimize the Pi-type matching network in it.

This requires measurement from the LTE_ANT0 pin#90 to the 50-Ohm RF connector. As there is, by design, no RF connector at the pin 90 directly, a coaxial cable (usually 1.25-mm diameter semi-rigid) can be manually attached to it for precision impedance measurements. Critically, a sufficient area of GND metal on the top layer adjacent to this pin is required (GND pads are typically sufficient) to make quality RF ground connection and provide robust physical attachment of the coaxial cable itself.

Please refer to section 2.4.4, Antennas and RF Design Considerations on page 12 for more detail on managing RF Trace Design.

2.4.4 Antennas and RF Design Considerations

Antennas require special interfacing for optimum RX and TX Performance.

2.4.4.1 Pi-Type Matching

We recommend fitting a 3-component T-type matching network. The purpose of the T-type matching network is to transform the impedance of the RF-path that extends beyond 50 Ohms if needed. The three components in this matching network should be as close together as possible to minimize the interconnecting track lengths.

By default, the component pads should be for a 0201-size capacitor which can be a No Fit by default. There should be a short low-impedance connection connecting the GND node of this component.

The series matching element should be connected at the junction where first shunt component. By default a 0-Ohm 0201-size resistor should be fitted but if matching is needed the pads must be able to take a 0201-size inductor.

The final shunt matching element should be connected from the node where the series matching component ends to the signal ground connection. By default, the component pads should be for a 0201-size capacitor which can be a No Fit by default. There should be a short low-impedance connection connecting the GND node of this component to the GND node of the first shunt component. There should be a short low-impedance connection connecting the GND node of this component to the GND reference of the 50-Ohm transmission line that continues beyond to the Antenna/Antenna-connector.

2.4.4.2 ESD Protection

ESD protection is a discretionary requirement and only required if necessary for higher ESD specifications than those provided by the RYZ024A.

We recommend selecting an ESD device with very low capacitance and small size (0201) to prevent further RF matching compensation.

2.4.4.3 Standard Impedance Transmission Lines

There are two possible methods to design 50-Ohm transmission lines:

1. With the RF track on the outer metal layer both micro-strip and coplanar types can be implemented.
2. With the RF track on an inner metal layer embedded micro-strip and strip-line topologies can be used.

Irrespective of which one is selected, the following guidelines are recommended:

- Design the transmission line tracks appropriately wide to minimize the RF insertion loss between the Antenna/Antenna-connector and RYZ024A. The maximum insertion loss of the conducted path should be < 0.5 dB.
- Transmission line EM fields will couple to adjacent metal layers.
  For microstrip implementation, make sure that a minimum of twice the spacing exists between transmission-line and associated GND. This clearance to adjacent metal layers will ensure that the designed transmission line impedance is not affected.
  For co-planar design, the spacing helps to define the controlled impedance. Take special care to make the calculations correctly.
  Whether these are microstrip or co-planar designed transmission lines, make sure that the adjacent metal GND areas are connected to the GND reference plane using periodic via connections, as to effectively terminate these leakage EM fields.

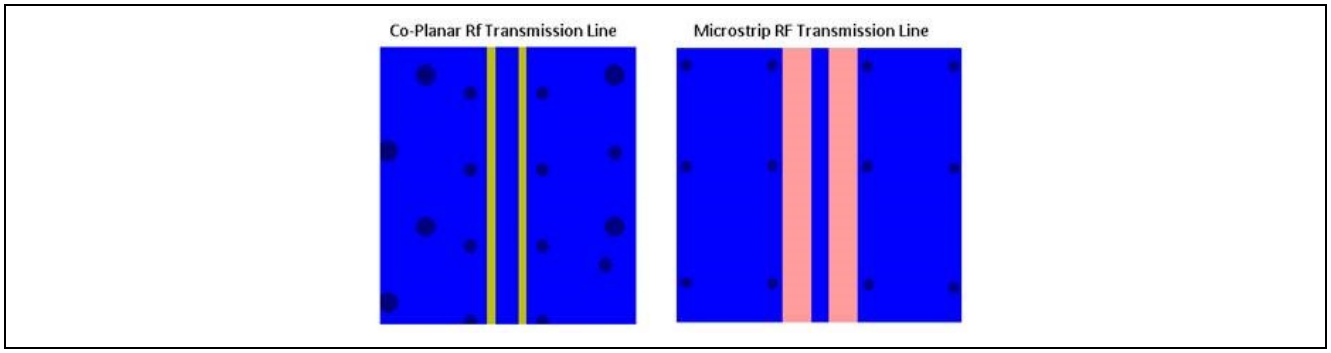

Figure 7. Transmission Line Implementation Examples

Figure 7 provides examples of both transmission line implementations, specifically showing:

a) The clearance from the transmission line to adjacent metal on layer 1.
b) The periodic via connections connecting metal-1 layer through to the reference GND layer for the transmission line.

- Avoid routing of noisy signal tracks adjacent to RF transmission lines to minimize interference coupling into RYZ024A RF ports.
- The component pads for the SMD terminals of the matching components used in the 3-component T-type matching circuit are effectively very short transmission lines. To minimize the RF insertion loss caused by the discontinuity in width differences, the ideal width of the 50-Ohm track should be as close as possible to the width of the component pads.
- If connectors are used in-line on antenna paths, design the PCB interface tracking and cut-out carefully to these connectors to keep the transmission line impedance to 50 Ohms.

2.4.5 Antenna Matching Circuitry

RYZ024A supports antenna matching. An example implementation is provided in NEKTAR reference design that uses two switches and an inverter to manage the antenna switching circuitry. The signals ANT_TUNE0 and ANT_TUNE1 are used for this purpose as shown in the following figure.

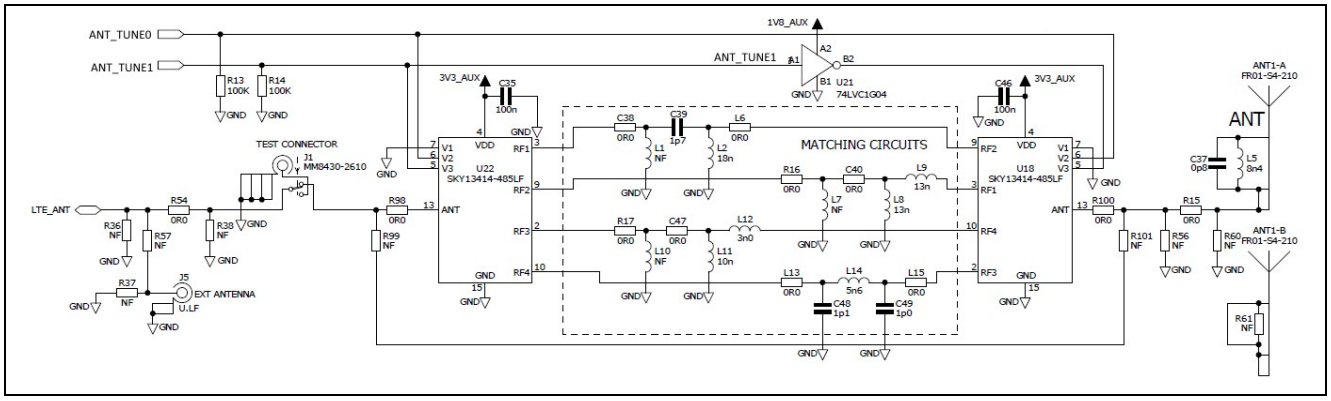

Figure 8. Antenna Matching in Reference Design Schematics

This implementation has the switches and the inverter always-on. An improvement to reduce the leakage can be done by using PS_STATUS to control the power enable of both switches and the inverter, as illustrated in the following figure. By doing this, they will only be powered when the module is not in low power mode.

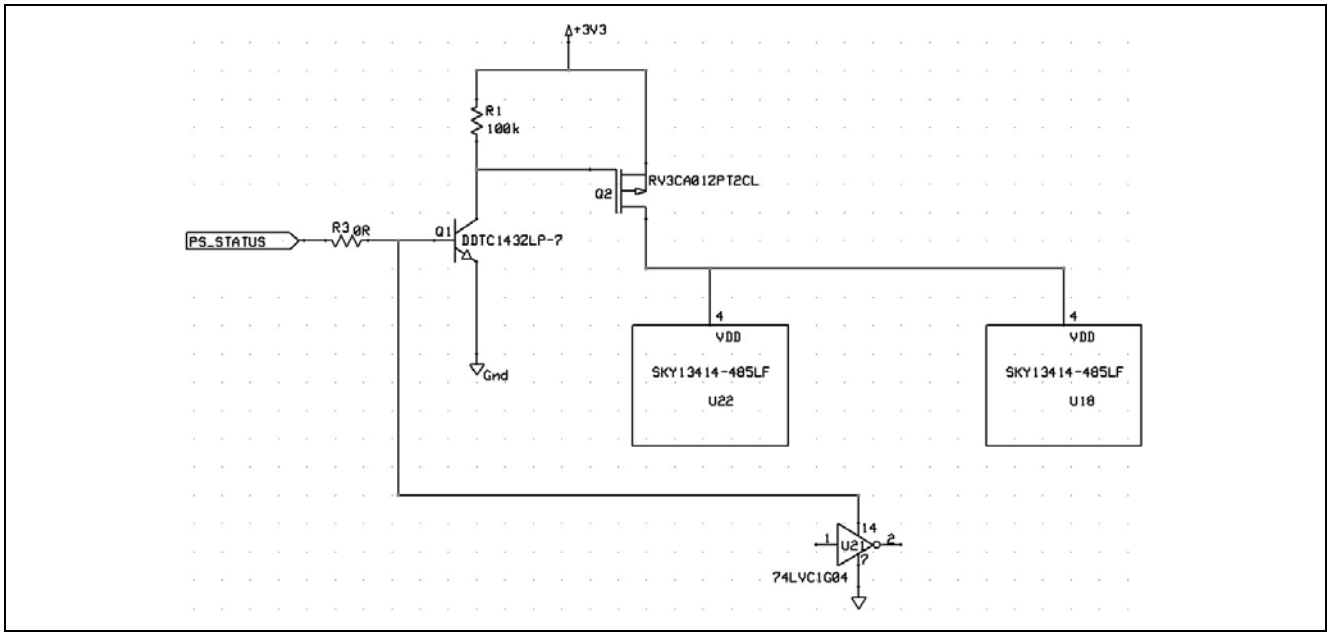

Figure 9. Power Enable Control for Switched and Inverter

2.5 Reset and Environmental Signals

Table 11 lists the Reset and other environmental signals and the following subsections describe their purpose and termination requirements.

Table 11. Non-Interfacing Signals

Pin Name	Pin Number	Trace Style	Direction	Power Group	Notes
72	ADC1	Digital	In	PVDD_1V8	An external switch should be connected to the ADC pin to prevent current leakage in low power modes. See section 2.6,

Pin Name	Pin Number	Trace Style	Direction	Power Group	Notes
					Analog to Digital Converter on page 18.
13	GPIO2/PS_STATUS	Digital	Out	PVDD_1V8	Default function: PS_STATUS (Enabled by default). Should be connected to a test point for debug purpose. - Function : Power Saving status. High level: module is active Low level: module is in Low Power Mode This signal can be used by the host to know when the modem is in low power mode and therefore requires to be woken-up via a WAKE signal such as RTS0, RTS1 or a dedicated WAKE. This signal can also be used to enable external circuits (such as RF switches on antenna path) that need to be active only when the module is not in low-power mode. A 100 kOhm pull-down resistor is required on PS_STATUS if this signal can be used by the Host.
14	GPIO28/ DTR0	Digital	In/Out	PVDD_1V8	
12	GPIO1/ STATUS_LED	Digital	In/Out	PVDD_1V8	Default function: STATUS_LED (Disabled by default). A persistent AT command is needed to set it active high (1.8V). Please see details on LED behavior in the *RYZ024A AT Commands Reference Manual*. It is recommended to add a pull down resistor and an inverter or a MOSFET-N to avoid extra power consumption in the

Pin Name	Pin Number	Trace Style	Direction	Power Group	Notes
					deepest power saving mode.
19	GPIO31/PWM0/PULSE0/19M2_OUT	Digital	In/Out	PVDD_1V8	
18	GPIO32/ PWM1/ PULSE1	Digital	In/Out	PVDD_1V8	
9	GPIO33/ TX_IND	Digital	In/Out	PVDD_1V8	
10	GPIO34/ ANT_TUNE0	Digital	In/Out	PVDD_1V8	ANT_TUNE0 (1.8V output) can be used to drive an antenna tuning circuit, as described in section 2.4.5, Antenna Matching Circuitry on page 14. See also Antenna Tuning description in RYZ024A Manufacturing Guidelines.
11	GPIO35/ ANT_TUNE1	Digital	In/Out	PVDD_1V8	ANT_TUNE1 (1.8V output) can be used to drive an antenna tuning circuit, as described in section 2.4.5, Antenna Matching Circuitry on page 14. See also Antenna Tuning description in RYZ024A Manufacturing Guidelines.
69	JTAG_TCK	Digital	In		JTAG interface. Each signal should be connected to a test point. Note that it is helpful to add a 1.8V and GND test points to ease the connection (or even better, a not fitted test pin header).
67	JTAG_TDI	Digital	In		
68	JTAG_TDO	Digital	Out		
66	JTAG_TMS	Digital	In		
70	JTAG_TRSTN	Digital	In		
20	RESERVED/FFF_FFH	Digital	In	PVDD_1V8	Reserved pad: it must be pull-down and connected to a Test Point.

Pin Name	Pin Number	Trace Style	Direction	Power Group	Notes
46	RESETN	Digital	In	PMU_5V	It is recommended to add an optional, not-fitted pull-up.
16	RING0	Digital	In/Out	PVDD_1V8	Enabled by default and active low. Used to signal the host when there is data or URC pending on the UART line. A 100 kOhm pull-up (either on the host input or external on the PCB) is recommended as this signal will become HighZ when the modem goes in deep sleep or shuts down.
48	WAKE0	Digital	In	PMU_5V	WAKE input. Disabled by default. When enabled, active level HIGH will wake up the modem if the modem is in Deep Sleep mode. Note: When a low level is applied to this pin, there is no leakage.
47	WAKE1	Digital	In	PMU_5V	WAKE input. Disabled by default. When enabled, active level HIGH will wake up the modem if the modem is in Deep Sleep mode. Note: When a low level is applied to this pin, there is no leakage.
49	WAKE2	Digital	In	PMU_5V	WAKE input. Disabled by default. When enabled, active level HIGH will wake up the modem if the modem is in Deep Sleep mode. Note: When a low level is applied to this pin, there is no leakage.
55	WAKE3	Digital	In	PMU_5V	WAKE input. Disabled by default. When enabled, active level HIGH will wake up the

Pin Name	Pin Number	Trace Style	Direction	Power Group	Notes
					modem if the modem is in deep sleep mode. Note: When a low level is applied to this pin, there is no leakage.
57	WAKE4	Digital	In	PMU_5V	WAKE input. Disabled by default. When enabled, active level HIGH will wake up the modem if the modem is in Deep Sleep mode. Note: When a low level is applied to this pin, there is no leakage.

2.6 Analog to Digital Converter

- It is recommended to leave the ADC pin #72 floating if not used.
- For Low Power mode conditions, it is best to consider having an inline FET switch connected between the ADC pin and the analog source as per the configuration of Figure 10.

This is intended to further minimize the power consumption in the Low Power mode operation.

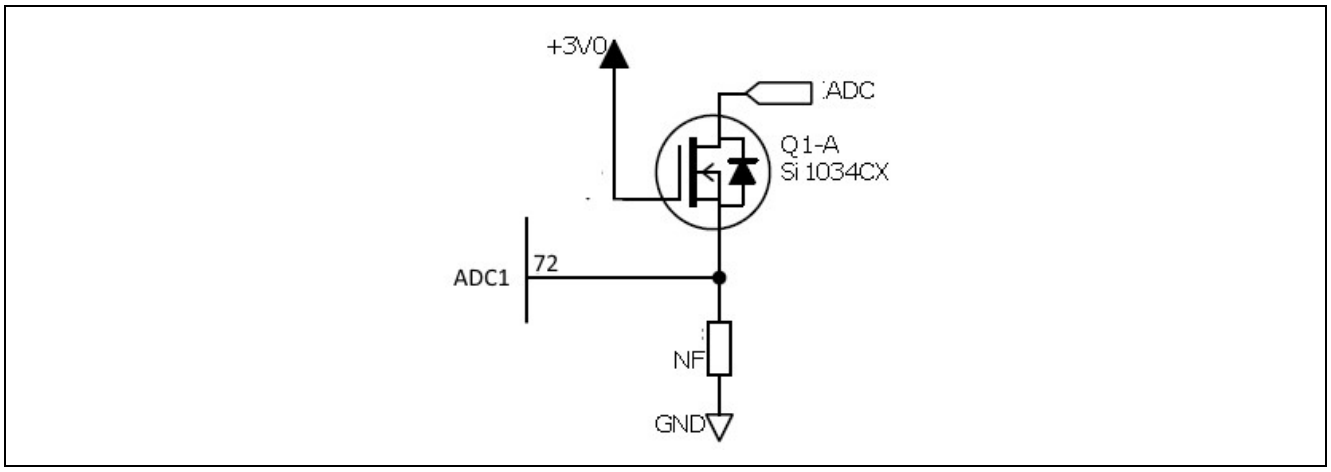

Figure 10. FET Implementation for ADC

2.7 PCB Layout Rules

This section provides general good practices in defining a PCB layout.

2.7.1 Placement

It is good to perform the placement of all the major components blocks before routing any section of the PCB design. The considerations here are:

- RYZ024A module
- RF interface

Initial placement of these parts allows assessment of the PCB floor plan usage and avoids any significant changes to final routed areas of the design if a placement issue is found. This also provides an opportunity for Renesas to review the placement.

The following information presents considerations when performing this placement:

1. Keep them in a similar quadrant to the interface they connect to.
2. Consider orientation to avoid crossing traces when routing.
3. Keep them as close as possible to the RYZ024A module where possible.

2.7.2 PCB Layers

It is recommended to use more layers, for example 6 instead of 4, to have more flexibility on burying and shielding RF traces and noisy signals. A 6-layer PCB design fits well for an evaluation board that contains many signals, as shown in Figure 11. A design on 4-layer PCB on the contrary shall implement a minimal set of signals as shown on Figure 12.

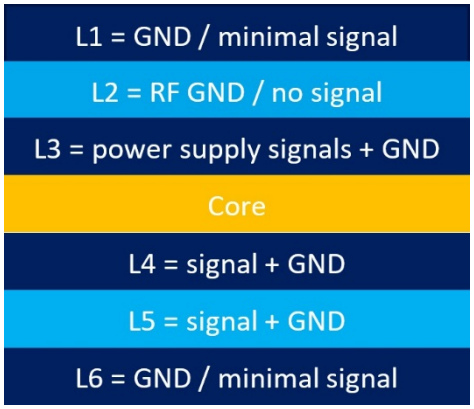

Figure 11. 6-Layer PCB Example

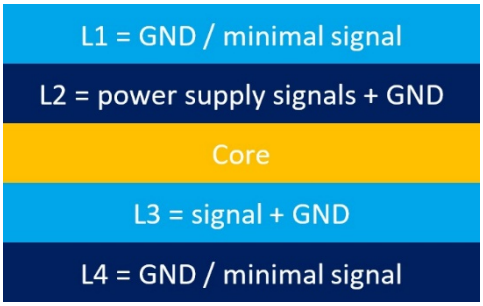

Figure 12. 4-Layer PCB Example

2.7.3 Trace Characteristic Design

This section explains some standard design rules when considering different types of signals involved (digital, power supply, RF).

2.7.3.1 Digital Traces

1. Careful and logical placement of digital signals is required to ensure separation of digital interference between each other and unrelated traces.
2. Consider the flow of ground currents during routing. Make sure that the grounding surrounding the traces (from source to load) remains continuous, with no cut or breaks. This will avoid long convoluted ground return currents which can create EMI-type problems.
3. Ensure the steps provided in section 2.7.3.4 Controlled Impedance Traces are considered for digital traces requiring specific impedance.
4. For those with no impedance requirements, be practical with the trace thickness. Keep them thin to avoid a buildup of capacitance, but make sure they are suitable for manufacture.
5. If routing traces on alternate layers, avoid running them parallel and keep them orthogonal. Good practice is to run traces on alternative layer from vertical to horizontal. This avoids traces directly coupling.
6. Important recommendations related to SIM connector placement can be found in section 2.2.2, Other Hardware Considerations on page 7.
7. Apply via shielding around clock signal traces.
8. Top/bottom layers are flooded with ground plan with minimal traces.
9. As many traces as possible shall be buried. Priority should be put on burying data (UART, and so forth) and clock traces. If not possible to bury everything, leave static signals (such as reset) on external layers.
10. Extra filtering provision could be added on some lines. It is typically not necessary but could be provisioned just in case.
    - PI filter on 1V8_LTE. Default BOM is a 0R series resistor
    - Decoupling caps on all SIM signals as close as possible to SIM connector (NF by default)
    - RC filters on the RFDATA lines controlling the antenna switches. Default BOM is a series 0R resistor.
11. Traces between SIM connector and RYZ024A should be kept as short as possible, and away from the antenna.
12. Data and clock should be as far as possible from the antenna area.

2.7.3.2 Power Supply Traces

1. Size the power supply traces appropriately for low impedance source. Pay attention to the number of vias used when routing traces across multiple layers. This is especially true for high current signals such as PA supply voltage.
2. For each power supply output, the decoupling capacitors ground pad must be connected to the ground return of the power supply source.
3. Make sure that the digital traces remain well away from the power supply traces.
4. Appropriate dimensioning of the width and length of each supply track and the number of any interlayer connecting vias is needed to minimize the resistive losses in each supply track.
5. Renesas does not recommend the usage of power planes for this design.

2.7.3.3 RF Traces

1. Avoid burying these traces as much as possible, because it increases RF losses compared with routing on the top.
2. Keep as short as possible to help reduce RF losses.
3. Design the impedance of the trace keeping in mind that the footprint of the RF components should be of similar width. This helps avoid impedance discontinuities.
4. Ensure the steps provided in Section 2.7.3.4 Controlled Impedance Traces are considered when determining the trace width.

2.7.3.4 Controlled Impedance Traces

- Calculation of traces width and spacing:
  Use simple RF design tools to calculate the copper trace thicknesses based upon:
  a) Thickness of the dielectric substrate that is used between the RF copper trace and the ground plane
  b) Spacing between the copper trace and the adjacent ground plane (on the same layer)
  c) Dielectric constant of the substrate material being used for manufacture. Sometimes, the required trace width is impossible to manufacture. It must be reconsidered until feasible. In this case, consider implementation of one of the following:
     - Thicker substrate
     - Moving the ground plane reference to the next layer down by removing the ground plane under the transmission line of interest
- General good practice guidelines
  a) Careful placement is required to keep RF traces short and kink-free.
  b) Do not route RF traces on intermediate layers.
  c) Ground planes beneath RF traces should be continuous.
  d) The ground fill around RF traces should have sufficient clearance to maintain the desired impedance.
- RF matching component footprints
  Depending on the substrate thickness and the size of the components' pads used can deviate the desired transmission impedance from the wanted (nominally 50 Ohms).
  For RF devices, if any copper pad in relation to RF signals is significantly larger than the transmission line width, then the ground reference could be moved to the next layer down.

2.7.3.5 Grounding

1. Stitch ground areas together with vias where flooded ground remains unterminated.
2. Stitch ground areas together in general to keep common ground impedance the same across the region.
3. RF ground planes should be as large and continuous as possible and not be cut into small islands. Check that strings of vias do not inadvertently create slots in ground or power planes.
4. Apply ground plane flooding on all layers.
5. Apply extensive via stitching.
6. Use extra vias around sensitive areas such as RF traces and noisy lines.
7. Make sure to apply an even distribution of vias on ground planes.
8. Tight stitching all along board edges to create Faraday cage.
9. On the 4-layer PCB, use blind vias and micro vias instead of through-hole vias only, and avoid via stubs.

2.7.4 Example of 6-Layer PCB Design

This section details an example of a 6-layer PCB design.

1. Layer 1
   — Minimal signal traces (in blue)
   — Ground plane flooding with a lot of ground stitching (in green)
   — Vias are evenly distributed across the surface
   — Tight stitching around the board edges (Faraday cage)

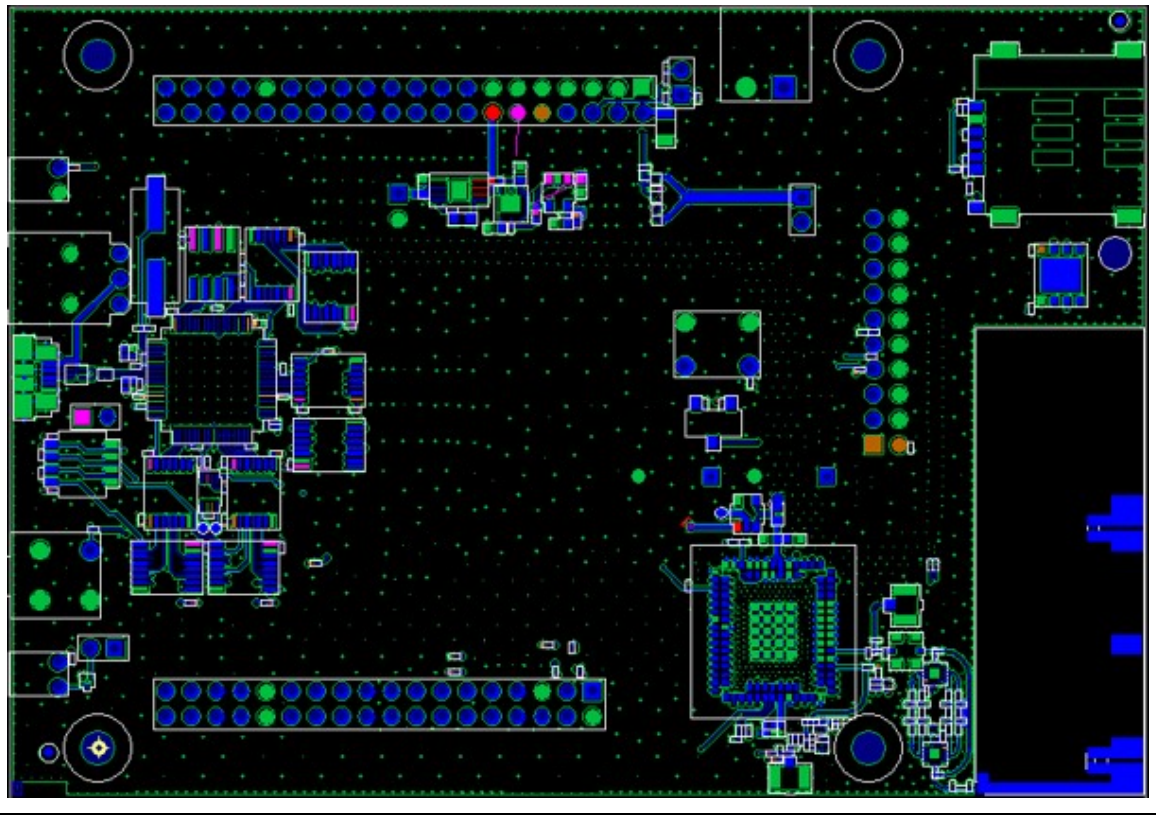

Figure 13. Layer 1 View

2. Layer 2
   - Ground plane, no signal
   - Vias are evenly distributed across the surface

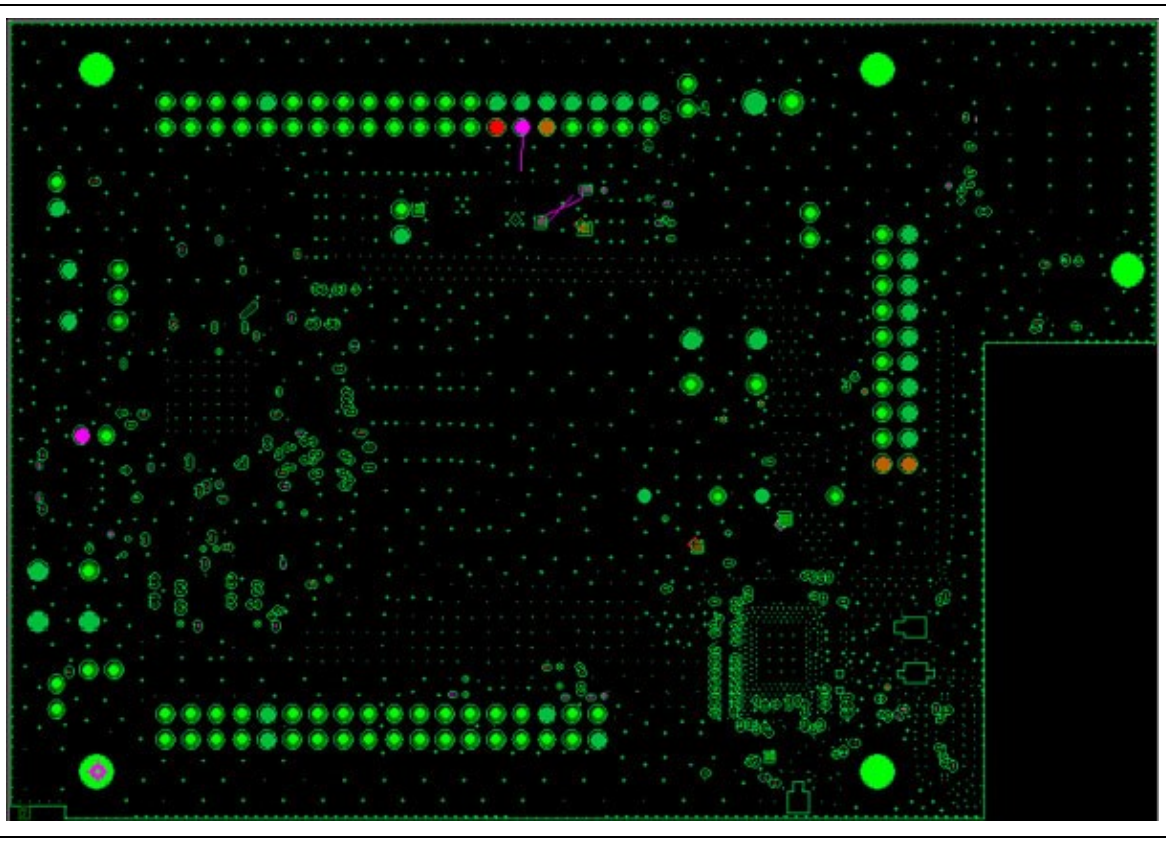

Figure 14. Layer 2 View

3. Layer 3
   - Power traces (in pink)
   - The remaining surface is flooded with ground with proper stitching and even via distribution.

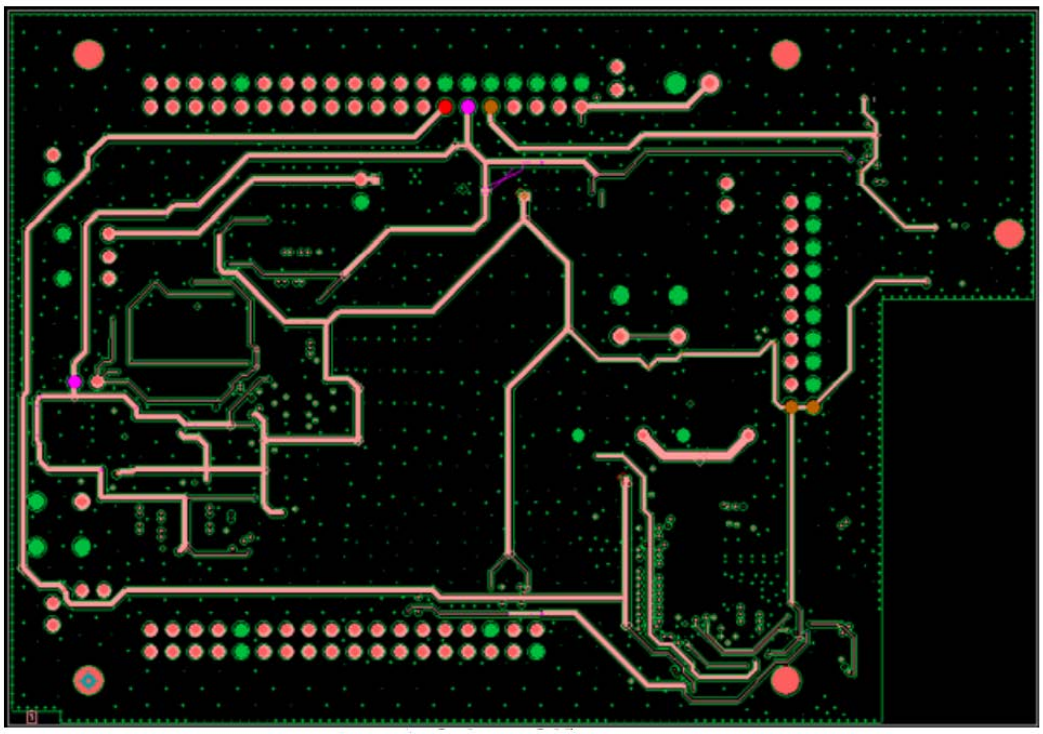

Figure 15. Layer 3 View

4. Layer 4
   - Signal layer (in pink)
   - The remaining surface is flooded with ground with proper stitching and even via distribution.

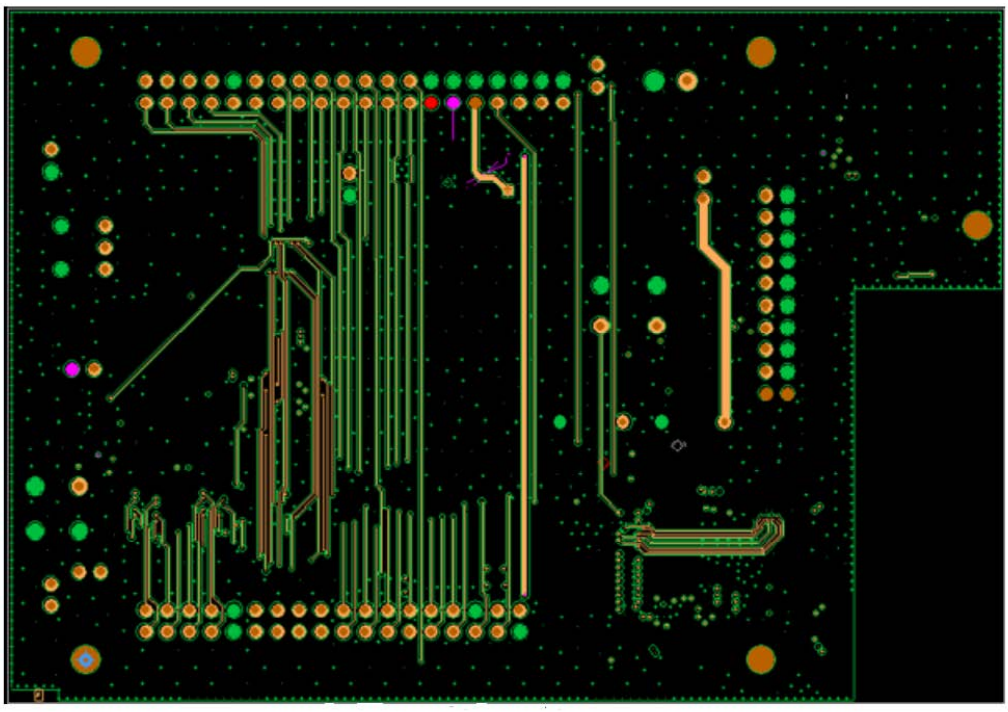

Figure 16. Layer 4 View

5. Layer 5
   - Signal layer (in pink)
   - The remaining surface is flooded with ground with proper stitching and even via distribution.

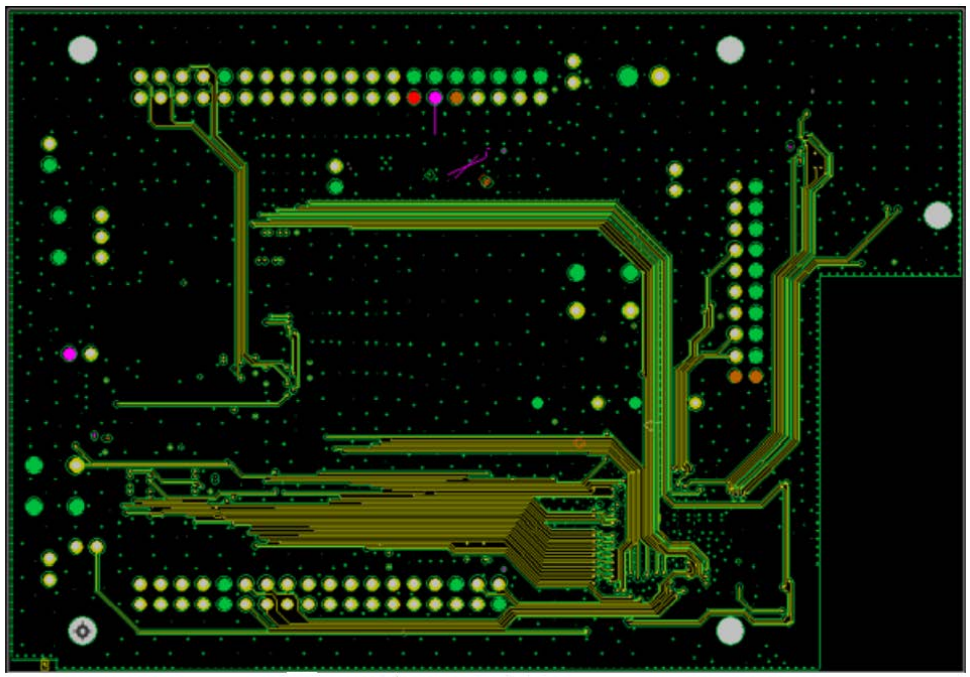

Figure 17. Layer 5 View

6. Layer 6
   - Minimal signal traces (in blue)
   - Ground plane flooding with a lot of ground stitching (in green)
   - Vias are evenly distributed across the surface
   - Tight stitching around the board edges (Faraday cage)

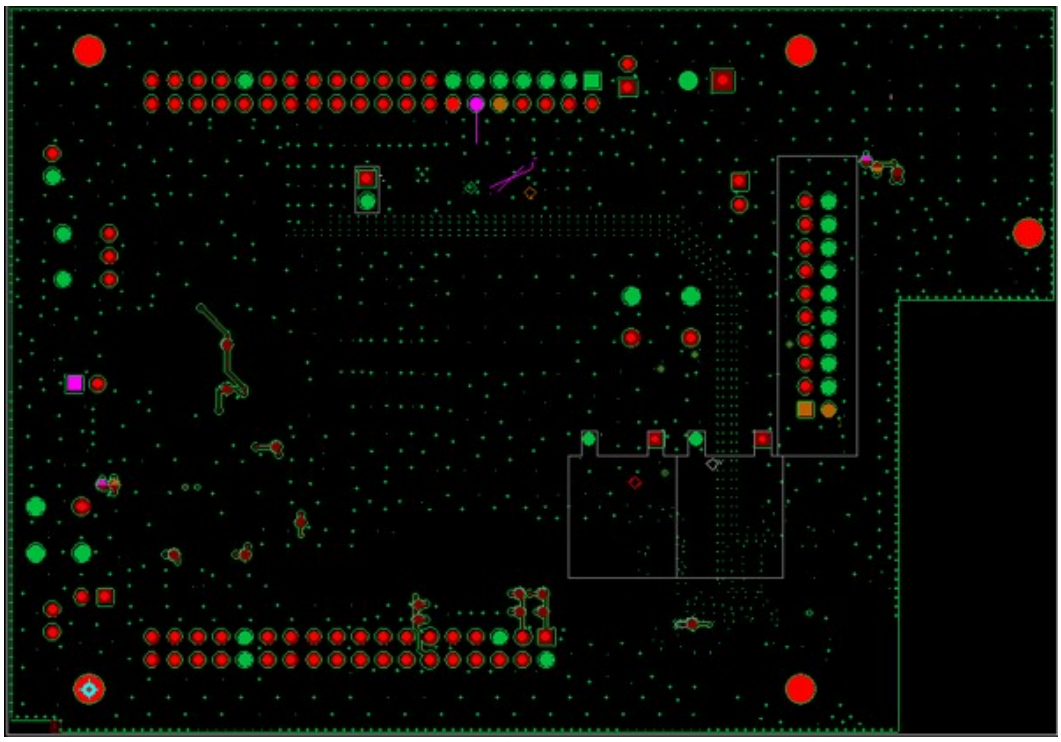

Figure 18. Layer 6 View

Signals are brought from module pads (L1/blue) to internal layer (L4/yellow) as soon as possible using blind and buried vias. Many ground vias are used below the module and around the module to ensure a proper return path to the main ground plane on L2.

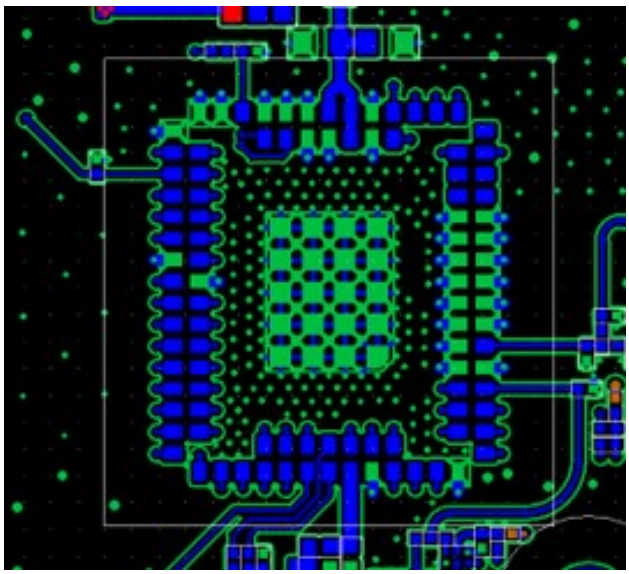

Figure 19. Module Pads (in blue) on Layer 1

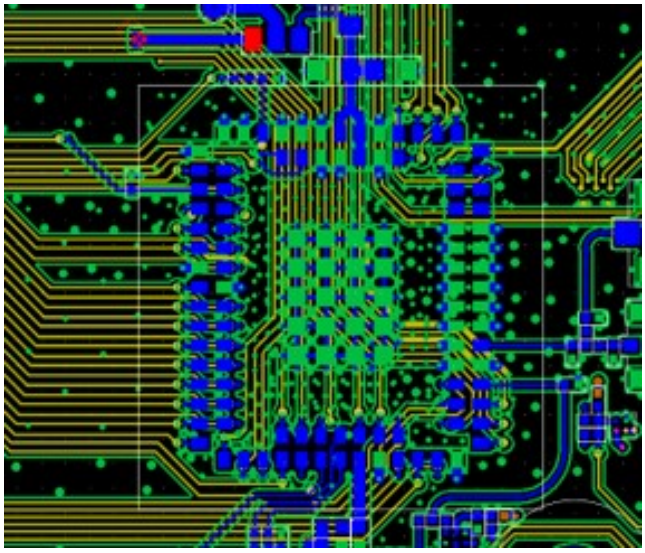

Figure 20. Internal Signals (in Yellow) on Layer 4

Even if all traces are buried between ground planes, clock signals are also shielded with the ground strip. This can be seen on layer 5 as represented on Figure 21.

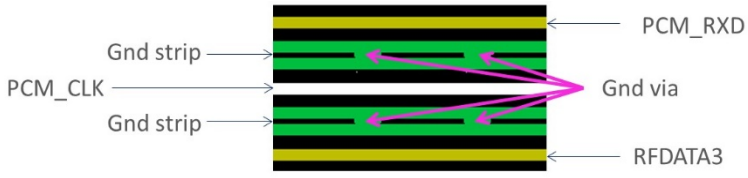

Figure 21. Shielding Clock Signals with Ground Strips

3. Bring-Up and Testing

3.1 Introduction

The purpose of this chapter is to describe what has to be done for board bring-up, test and qualification.

The expectations at this stage of the product's life are:

1. Consider any inconsistent and potentially hazardous manufacturing faults to be eliminated.
2. Confirm that it is safe to proceed to further detailed calibration and measurement steps.
3. Evaluate board performances.

3.2 Prerequisites

The following lists the necessary tools to perform all aspects of the Hardware Qualification.

1. Device under test
   a) Without RYZ024A assembled:
      - to check RF extra loss between the RYZ024A RF ports and product RF output
      - to perform sanity check of connection with RYZ024A
      - for debugging if necessary
   b) With RYZ024A assembled: to do hardware qualification
2. External Host PC/Laptop for UART1 interface
   Note: Detailed information will be provided in a future revision of this document.
3. LTE RF test equipment setup
   a) Shielding box to avoid any RF performance results degradation due to environment
   b) RF components such as: cable, splitter, 50 Ohm loads corresponding to the RF working band
4. Power supply with current measuring ability

3.3 Functional Verification without Assembled Module

Attention: If a fault is discovered, consider the impact of the issue observed on all the manufactured samples.

The purpose of this section is to establish a sanity check on the board before soldering the module, in order to avoid any damage due to a manufacturing issue.

This test covers VBAT power supply.

3.3.1 Power Supply

3.3.1.1 Test Procedure

Figure 22 presents the equipment necessary to perform the next following test steps and the required configuration for test.

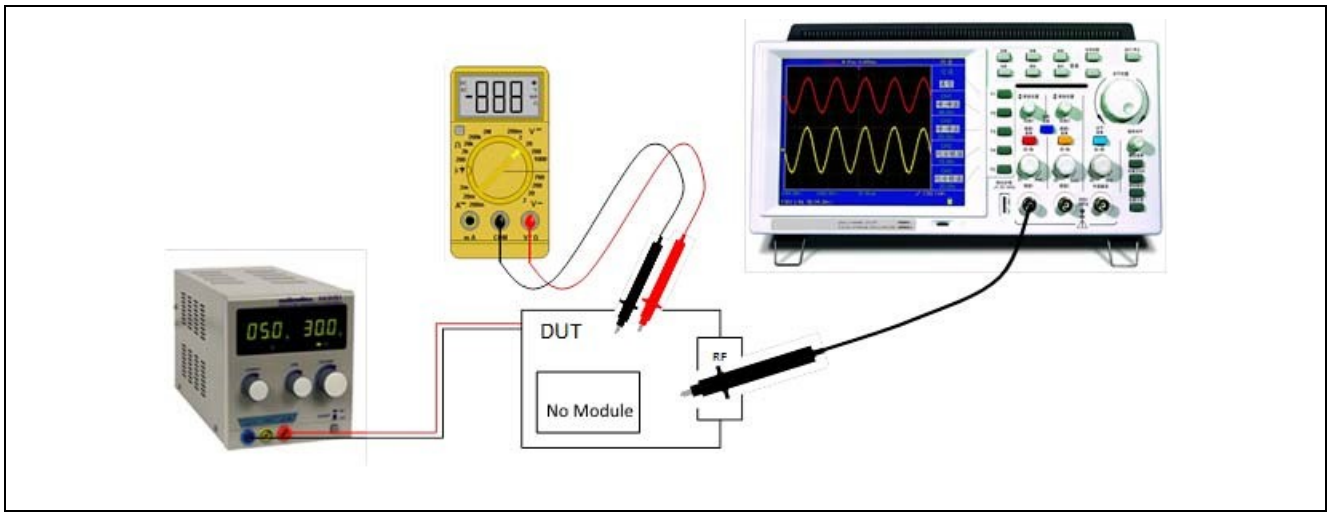

Figure 22. Pre-Test Configuration (No Module on Board)

- Test voltage values
  Test the DC nature of the voltage delivered by the power supply with an oscilloscope before connecting the DUT. Confirm that the voltage level is correct and stable. Once the power supply is confirmed, you can power the DUT and accurately measure the test points voltage with a multimeter. At this stage, only VBAT1 can be tested.
  Check at each voltage test point, as illustrated on Figure 23, that the voltage value corresponds to what is expected. The value of VBAT1 must be in the range specified in the *RYZ024A Datasheet*, section *Electrical Operating Conditions*.

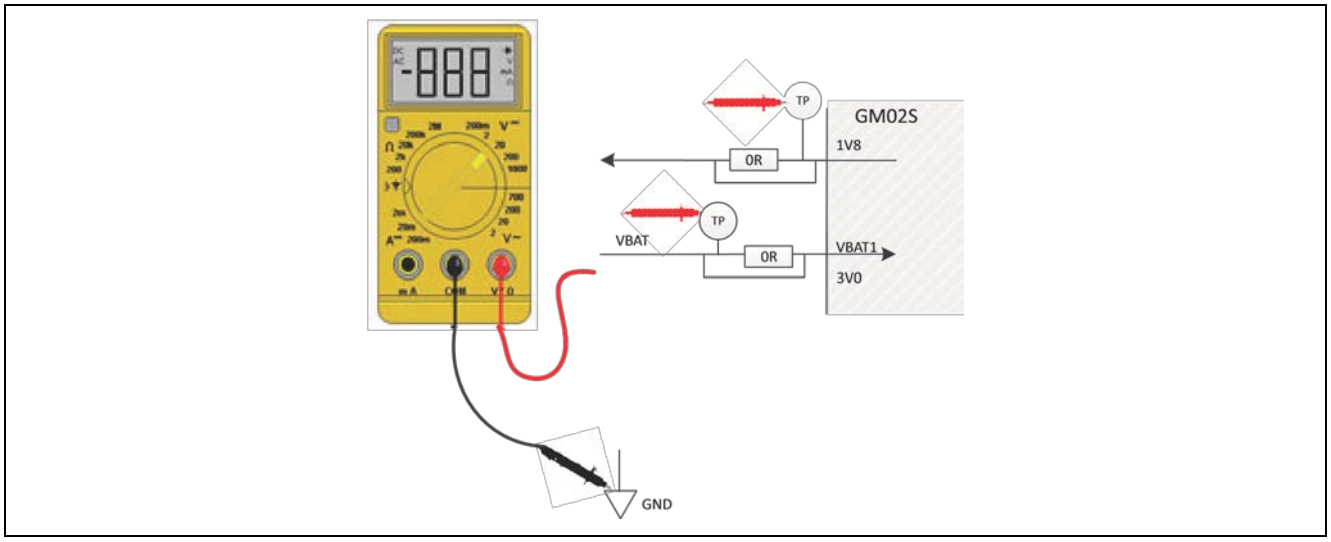

Figure 23. Measuring Voltage Value (RYZ024A)

3.3.1.2 Troubleshooting

- One power supply is incorrect
  - If the VBAT1 voltage is incorrect
    - Check any resistor link to detect unexpected short or open circuits.

3.3.2 RF Path

3.3.2.1 Test Procedure

Important: Those tests should be run or supervised by engineers with RF measurement preparation and test experience.

- RF path check

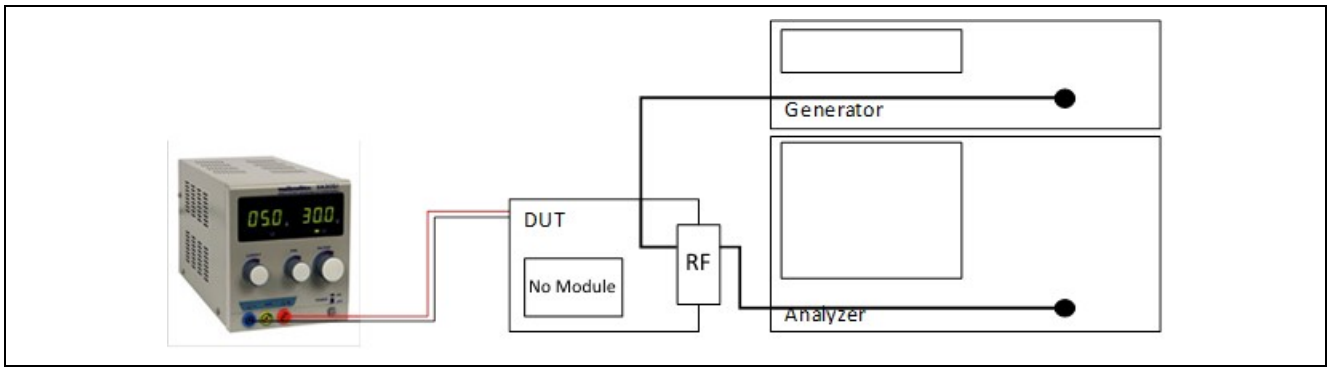

Figure 24. RF Path Check Setup

a) Measure and record the insertion loss on all the supported LTE bands for the antenna from pin 54 of the RYZ024A to LTE port antenna
b) By design, the extra RF path loss must be lower than 0.5 dB, to assume having good RF performance.

3.3.2.2 Troubleshooting

- In case of unexpected RF losses:
  a) Ensure that the assembly of the coaxial connectors are correct:
     - No dry joints.
     - The right way around.
  b) Ensure that the soldered SMA is not a short circuit or open circuit:
     - Test with digital voltmeter.
  c) Verify the RF equipment calibration, including coaxial cable used to connect to the RYZ024A pin 54 and LTE port antenna.
  d) Verify that the RF matching is good.

3.4 Functional Verification with Assembled Module

Attention: If a fault is discovered, consider the impact of the issue observed on all manufactured samples.

The purpose of this section is to validate the assembly process of the module.

This test covers:

1. RYZ024A pins and features:
   a) Power supply
   b) UART1 console output during power-up operation
   c) SIM Interface
   d) GPIOs
   e) ADC
2. Nominal power consumption
3. RYZ024A boot

3.4.1 Power Supply

3.4.1.1 Procedure

1. Turn on the device under test.
2. Confirm voltages of the power supplies remain in line with the specifications from the datasheet. See the test points involved on Figure 23.
   Caution: If, at this point, the voltages are incorrect, **stop immediately** to diagnose the cause of the issue.
3. Confirm that the current is nominal from the Host power supply.
   Observe the current drawn and ensure it is in line with expectations.

3.4.1.2 Troubleshooting

- Excessive current draw
  Check all RYZ024A voltage supplies. Confirm that there are no RYZ024A supply short circuits. Voltage should read according to the nominal requirement.
- No current draw or current less than expected
  a) Check the external power supply wiring
  b) Check for dry joints between adjacent RYZ024A pin(s) and the power supply source.

3.4.2 Confirm Module Power-Up Operation (UART2)

An extract of the output of the OS console on UART2 port is provided below (boot in FFF mode):

```
[0000000000] boot: Switched to flash, timeout 10000, proto thp
[0000000000] Running on Windbond flash sector 0x1C030000
[0000000000] RBBombyx 11.11@50892 '8.0.0.0 [50892]'
[0000000004] Reset cause 'BUTTON'(real 'BUTTON' )
(bootWDG : '0') [rawRst '0x00000001']
[0000000012] regConfig 0x1BBB0BA3@1
[0000000015] boot: Current flash, timeout 10000, proto thp
```

```
[0000000020] boot: FFF mode
[0000000179] elf: ELF format selected
[0000000183] elf: Header finished
[0000000186] elf: Waiting for 480 bytes
[0000000189] elf: PH 0x00333DE0, 28 bytes [0000000193] elf: Note 0x63727A04
[0000000196] elf: PH 0x00000000, 20 bytes [0000000200] elf: Note 0x4D415000
[0000000203] elf: PH 0x00001000, 86 bytes
[0000000207] elf: PH 0x00001060, 1920 bytes
[0000000210] elf: PH 0x000017E0, 119824 bytes
[0000000218] elf: PH 0x0001EBF0, 8 bytes
[0000000221] elf: PH 0x0001EBF8, 56 bytes
[0000000225] elf: PH 0x0001EC30, 100 bytes
[0000000229] elf: PH 0x0001EC94, 624 bytes
[0000000233] elf: PH 0x0001EF04, 2676 bytes
[0000000237] elf: PH 0x00336000, 32 bytes
[0000000240] elf: PH 0x00710000, 196656 bytes
[0000000249] elf: PH 0x00750000, 129576 bytes
[0000000257] elf: PH 0x007A0000, 325728 bytes
[0000000269] elf: PH 0x00334000, 8192 bytes
[0000000273] elf: Program Header finished
[0000000277] sbp: no ACPU found
[0000000280] sbp: MCPU Booting at 0x1C1002F0... fs: Mounting /flash0...done
fs: Overlay filesystem mounted on /fs
[USIM] PSI USIM rev = 2
[USIM] Default slot=0 itf=0 OK
[USIM] ITF(0) slot(0) enabled(1) polling(0)
[USIM] ITF(1) slot(0) enabled(0) polling(0)
[USIM] ITF(2) slot(0) enabled(0) polling(0)
>INFO> DCP : Init over='serial' eem: Memory initialized
#WARN# ATF : can't find device related to id=4!
[PSP] initializing fs: Mounting upgrade filesystem ...
fs: Mounting done
QKI pools init...done rrcInitCallbacks 440
RrcPersistEco - error: 'rootFsDir' is unresolved feeds: 510 Configure enter
EAPPS feeds: 520  Configure leave EAPPS feeds: 520  Configure enter MQTT
feeds: 520  Configure leave MQTT feeds: 530  Init enter EAPPS feeds: 560  Init
leave EAPPS feeds: 560  Init enter LWM2M feeds: 560  Init leave LWM2M feeds:
560  Init enter MQTT feeds: 560  Init leave MQTT feeds: 560  Init enter SQNSMS
feeds: 570  Init leave SQNSMS
[PSP] initialized [PSP] starting reserved room 7/150 ::hell terminal::
-> [ZSP0] started after 2 ms, version 261.6 [ZSP1] started after 1 ms, version
261.1 ue: Waiting for LCPU IRQ...done xpc (mcpu): Initalized xpc (lcpu):
Initalized done ue: Waiting for LCPU DLP to start...dLPU boot confirmation
done ue: Waiting for LCPU to run...[L1P] started hp: Started feeds: 960  Start
enter EAPPS feeds: 1180  Start leave EAPPS feeds: 1180  Start enter LWM2M
feeds: 1190  Start leave LWM2M feeds: 1190  Start enter MQTT feeds: 1190
Start leave MQTT feeds: 1190  Start enter SQNSMS feeds: 1200  Start leave
SQNSMS
[PSP] started
```

3.4.3 GPIOs

3.4.3.1 Procedure

This section helps to confirm a GPIO's behavior.

Use the manufacturing AT command AT+SMGT.

The first 32-bit triplet of parameters is a bitmask to address the GPIO, the second 32-bit triplet of parameters is the bitmask of the value to drive on the GPIO, and the third 32-bit triplet provides the expected polarity

setting for the GPIO. Refer to *Manufacturing AT Commands Reference Manual* for more detail on this command.

The following command tests SQN3330_GPIO_22 (GPIO[22]) setting to 1, active high. Value 22 is represented by bitmask 0x400000, coded as triplet 0,0,0x400000.

```
AT+SMGT=0,0,0x400000,0,0,0x400000,0,0,0
```

The following command tests SQN3330_GPIO_38 (GPIO[38]) setting to 1, active low. Value 38 is represented by bitmask 0x4000000000, coded as triplet 0,0x40,0.

```
AT+SMGT=0,0x40,0,0,0x40,0,0,0x40,0
```

Test the expected behavior as needed by your implementation.

3.4.3.2 Troubleshooting

- Unexpected AT command error
  - Make sure that you activated the Manufacturing mode with AT+CFUN=5 before trying to use the AT+SMGT command.
  - Make sure that the version of Firmware used is the correct version.
- Unexpected GPIO behavior
  - Ensure that there are no short or open circuits between the test point and the RYZ024A.

3.4.4 SIM Communication

3.4.4.1 Procedure

Confirmation of SIM behavior:

Insert the following command to verify the SIM is working properly.

1. Send AT+CMEE=2 to activate error logs.
2. Send AT+CFUN=4 to start reading the SIM card.
3. Wait for 10 seconds.
4. Send AT+CIMI. It will answer one of the following:
   - +CME ERROR: SIM not inserted: no SIM card was detected
   - +CME ERROR: SIM busy: wait for a few more seconds and check if the IMSI is returned. If not, please refer to Section 3.4.4.2 Troubleshooting on page 50.
   - <IMSI value>: test completed successfully

3.4.4.2 Troubleshooting

- Unexpected AT command error
  - Make sure that the correct version of firmware is used.
- Unexpected SIM behavior
  - Check all the connections between the SIM housing and the RYZ024A module are done according to Section 2.2 SIM Interface on page 6.
  - Ensure that there exists no short or open circuit between the SIM housing and the RYZ024A.

4. Appendix: Hardware Test Preparation

4.1 RF Interfaces Preparation

4.1.1 LTE RF Test Preparation

To ensure that the RF test platform will provide the most reliable interface for testing. The following setup is proposed when measuring RF characteristics of the RYZ024A System.

The shield box cavity is configured as shown on Figure 25:

- The DUT is connected to the computer by UART1.
- The DUT is also connected by one RF cable.

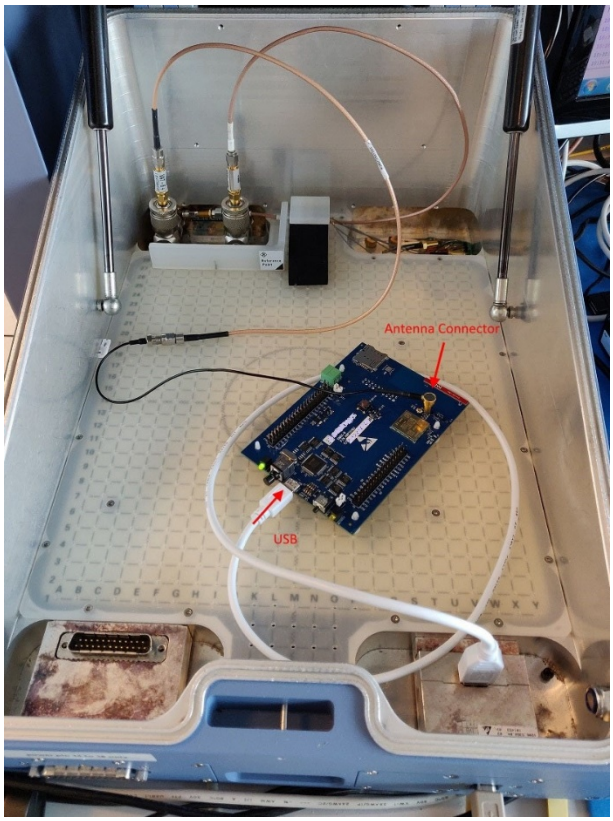

Figure 25. Shield Box Cavity View

Figure 26 shows the required configuration for calibration and screening. It consists of:

- 1 x ZN2PD2-50-S + power splitter if the signal analyzer and the signal generator are two distinct devices. R&S® CMW100 or CMW500 for instance allows the use of a single bidirectional RF port and prevents the need of a power splitter.
- 1 x RF cable to the MXA (if needed)
- 1 x RF cable to the MXG (if needed)
- 1 x RF cable to the DUT (in the shield box)

Figure 26. Configuration for Calibration and Screening

5. Appendix: Abbreviations

AC	Alternate Current
ADC	Analog to Digital Converter
LTE_ANT0	Antenna 0 for LTE
AT Command	Modem-type commands prefixed with AT characters
BOM	Bill of Material
COM	Communication
CPU	Central Processing Unit
dB	decibel
DC	Direct Current
DCP	Data Communication Protocol
DM Tool	Diagnosis and Monitoring tool
DUT	Device Under Test
DV Tool	Diagnostic and Validation Tool
EM	Electromagnetic
EMI	Electromagnetic interference
FFF	Firmware from Flash module boot mode
FFH	Firmware from Host module boot mode
FS	File System
FW	Firmware
GND	Ground
GPIO	General Purpose Input/Output
HW	Hardware
IC	Integrated Circuit
IMEI	International Mobile Equipment Identity
IT	Interrupt
LTE	Long-Term Evolution. See also www.3gpp.org/.
MXA	Signal Analyzer
MXG	Signal Generator
PA	Power amplifier
PCB	Printed Circuit Board
PS	Power Supply
PSI	Platform Specification Interface
R	Short notation for Ohm
RF	Radio Frequency
RX	Reception
S/N	Serial Number
SIM	Subscriber Identity Module
SMA	RF connector type
SMD	Storage Module Device
SW	Software
TX	Transmission or Emission
UART	Universal Asynchronous Receiver Transmitter
UE	User Equipment
UL	Uplink
USB	Universal Serial Bus
USIM	Universal SIM.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Sep.29.22	—	First release document

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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