RX72N Group

Initial Settings Example

Introduction

This application note describes the settings that must be made after a reset of a RX72N Group microcontroller, including clock settings, disabling of peripheral functions still running after a reset, and nonexistent port settings.

Target Devices

- RX72N Group 224-pin version, ROM capacity: 2 MB to 4 MB
- RX72N Group 176-pin version, ROM capacity: 2 MB to 4 MB
- RX72N Group 145 and 144-pin-version, ROM capacity: 2 MB to 4 MB
- RX72N Group 100-pin version, ROM capacity: 2 MB to 4 MB

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

The sample code makes settings to disable peripheral functions still running after a reset, nonexistent port settings, and clock settings. The description in this application note applies to the processing that occurs following power-on (cold start).

1.1 Disabling Peripheral Functions Still Running After a Reset

Some peripheral functions start operating immediately after power-on, and some have the module stop function disabled. The processing covered under this item disables the following functions:

EXDMAC, DMAC/DTC, standby RAM, ECCRAM, RAM, and Expansion RAM

Note that the above processing is not performed by the sample code. As necessary, overwrite the corresponding constants to execute the processing.

1.2 Nonexistent Port Settings

The sample code performs initial settings suitable for 224-pin products. On products with pin counts under 224 pins, it is necessary to set the pins for ports that exist on 224-pin products but not on the target device to output mode.

Overwrite the constants as necessary to accommodate the actual target device.

1.3 Clock Settings

1.3.1 Overview

The procedure for making clock settings is as follows:

1. Sub-clock settings
2. Main clock settings
3. HOCO clock settings
4. PLL clock settings
5. PPLL clock settings
6. System clock switching settings

By making changes to the constants defined in r_init_clock.h, the sample code described in this application note can be used to change the various clock settings.

The sample code sets the PLL clock as the system clock and does not use a sub-clock. Overwrite the constants as necessary to match the clocks you wish to use.

1.3.2 Clock Specifications Assumed in Sample Code

Table 1.1 lists the clock specifications assumed in sample code.

Table 1.1 Clock Specifications Assumed in Sample Code

Clock	Oscillation Frequency	Oscillation Stabilization Time	Remarks
Main clock oscillator	24 MHz	4.2 ms*2	Crystal
Sub-clock oscillator	32.768 kHz*1	1.3 s*2	Standard LC
PLL clock	240 MHz (main clock × 1/1 × 10)	—*3	—
PPLL clock	200 MHz (main clock × 1/3 × 25)	—*3	—
HOCO clock	20 MHz*1	—*3	—

Notes: 1. Oscillation disabled by the sample code.
2. The actual oscillation stabilization time of the oscillator may differ due to conditions such as the system's wiring pattern and the oscillation constant. To determine the correct oscillation stabilization time, request an evaluation of the system you are actually using from the oscillator manufacturer.
3. Refer to section 63, Electrical Characteristics, in RX72N Group User's Manual: Hardware.

1.3.3 Clock Selection

By making changes to the constants defined in r_init_clock.h, the sample code described in this application note can be used to select settings such as the clock source of the system clock and whether each clock is oscillating or stopped. Table 1.2 lists clock selection examples.

Table 1.2 Clock Selection Examples

No.	1	2	3
System clock	PLL (MAIN)		
RTC (sub-clock)	Stopped	Oscillating	Stopped
MAIN	Oscillating	Oscillating	Oscillating
HOCO	Stopped	Stopped	Stopped
PLL	Operating	Operating	Operating
PPLL	Stopped	Stopped	Operating
CLKOUT	Stopped	Stopped	Operating
Operating mode	High-speed operating mode		
Memory wait cycles*1	1 wait cycle		
Constants			
SEL_SYSCLK	CLK_PLL	CLK_PLL	CLK_PLL
SEL_PLL	B_USE	B_USE	B_USE
SEL_MAIN	B_USE	B_USE	B_USE
SEL_HOCO	B_NOT_USE	B_NOT_USE	B_NOT_USE
SEL_SUB*2	B_NOT_USE	B_NOT_USE	B_NOT_USE
SEL_RTC*2	B_NOT_USE	B_USE	B_NOT_USE
SEL_PPLL	B_NOT_USE	B_NOT_USE	B_USE
REG_CLKOUT	CKOUT_NOT_USE	CKOUT_NOT_USE	CKOUT_USE
REG_OPCCR	OPCM_HIGH	OPCM_HIGH	OPCM_HIGH
REG_MEMWAIT	MEMWAIT_1WAIT	MEMWAIT_1WAIT	MEMWAIT_1WAIT

No.	4	5	6
System clock	HOCO		
RTC (sub-clock)	Stopped	Oscillating	Stopped
MAIN	Stopped	Stopped	Stopped
HOCO	Oscillating	Oscillating	Oscillating
PLL	Stopped	Stopped	Stopped
PPLL	Stopped	Stopped	Operating
CLKOUT	Stopped	Stopped	Operating
Operating mode	High-speed operating mode		
Memory wait cycles*1	0 wait cycles		
Constants			
SEL_SYSCLK	CLK_HOCO	CLK_HOCO	CLK_HOCO
SEL_PLL	B_NOT_USE	B_NOT_USE	B_NOT_USE
SEL_MAIN	B_NOT_USE	B_NOT_USE	B_NOT_USE
SEL_HOCO	B_USE	B_USE	B_USE
SEL_SUB*2	B_NOT_USE	B_NOT_USE	B_NOT_USE
SEL_RTC*2	B_NOT_USE	B_USE	B_NOT_USE
SEL_PPLL	B_NOT_USE	B_NOT_USE	B_USE
REG_CLKOUT	CKOUT_NOT_USE	CKOUT_NOT_USE	CKOUT_USE
REG_OPCCR	OPCM_HIGH	OPCM_HIGH	OPCM_HIGH
REG_MEMWAIT	MEMWAIT_0WAIT	MEMWAIT_0WAIT	MEMWAIT_0WAIT

No.	7	8	9
System clock	MAIN		
RTC (sub-clock)	Stopped	Oscillating	Stopped
MAIN	Oscillating	Oscillating	Oscillating
HOCO	Stopped	Stopped	Stopped
PLL	Stopped	Stopped	Stopped
PPLL	Stopped	Stopped	Stopped
CLKOUT	Stopped	Stopped	Operating
Operating mode	Low-speed operating mode 1		
Memory wait cycles*1	0 wait cycles		
Constants			
SEL_SYSCLK	CLK_MAIN	CLK_MAIN	CLK_MAIN
SEL_PLL	B_NOT_USE	B_NOT_USE	B_NOT_USE
SEL_MAIN	B_USE	B_USE	B_USE
SEL_HOCO	B_NOT_USE	B_NOT_USE	B_NOT_USE
SEL_SUB*2	B_NOT_USE	B_NOT_USE	B_NOT_USE
SEL_RTC*2	B_NOT_USE	B_USE	B_NOT_USE
SEL_PPLL	B_NOT_USE	B_NOT_USE	B_NOT_USE
REG_CLKOUT	CKOUT_NOT_USE	CKOUT_NOT_USE	CKOUT_USE
REG_OPCCR	OPCM_LOW_1	OPCM_LOW_1	OPCM_LOW_1
REG_MEMWAIT	MEMWAIT_0WAIT	MEMWAIT_0WAIT	MEMWAIT_0WAIT

Notes: 1. Do not clear the MEMWAIT bit to 0 if the ICLK frequency is 120 MHz or higher. Do not set the MEMWAIT bit to 1 when the operating power control mode is low-speed operating mode 2.
2. Set SEL_SUB to B_USE (use) when the sub-clock is used as the system clock, and set SEL_RTC to B_USE when the sub-clock is used as the RTC count source.
The sub-clock oscillates when either SEL_SUB or SEL_RTC, or both of them, are set to B_USE.

2. Operation Confirmation Conditions

The operation of the sample code referenced in this application note (Nos. 1 to 9 in Table 1.2) has been confirmed under the following conditions.

Table 2.1 Operation Confirmation Conditions

Item		Contents
MCU used		R5F572NNHDBD (RX72N Group)
Operating frequency	PLL clock selected as system clock (Nos. 1 and 2 in Table 1.2)	Main clock: 24 MHz PLL: 240 MHz (main clock × 1/1 × 10) System clock (ICLK): 240 MHz (PLL × 1/1) Peripheral module clock A (PCLKA): 120 MHz (PLL × 1/2) Peripheral module clocks B to D (PCLKB to PCLKD): 60 MHz (PLL × 1/4) FlashIF clock (FCLK): 60 MHz (PLL × 1/4) External bus clock (BCLK): 80 MHz (PLL × 1/3)
	PLL clock selected as system clock, PPLL and CLKOUT used (No. 3 in Table 1.2)	Main clock: 24 MHz PLL: 240 MHz (main clock × 1/1 × 10) System clock (ICLK): 240 MHz (PLL × 1/1) Peripheral module clock A (PCLKA): 120 MHz (PLL × 1/2) Peripheral module clocks B to D (PCLKB to PCLKD): 60 MHz (PLL × 1/4) FlashIF clock (FCLK): 60 MHz (PLL × 1/4) External bus clock (BCLK): 80 MHz (PLL × 1/3) PPLL: 200 MHz (main clock × 1/3 × 25) Ethernet-PHY External Clock (CLKOUT25M): 25 MHz (PPLL × 1/8) CLKOUT: 240 kHz (HOCO × 1/1)
	HOCO clock selected as system clock (Nos. 4 and 5 in Table 1.2)	HOCO: 20 MHz System clock (ICLK): 20 MHz (HOCO × 1/1) Peripheral module clock A (PCLKA): 20 MHz (HOCO × 1/1) Peripheral module clocks B to D (PCLKB to PCLKD): 10 MHz (HOCO × 1/2) FlashIF clock (FCLK):10 MHz (HOCO × 1/2) External bus clock (BCLK):10 MHz (HOCO × 1/2)
	HOCO clock selected as system clock, PLL and CLKOUT used (No. 6 in Table 1.2)	HOCO: 20 MHz System clock (ICLK): 20 MHz (HOCO × 1/1) Peripheral module clock A (PCLKA): 20 MHz (HOCO × 1/1) Peripheral module clocks B to D (PCLKB to PCLKD): 10 MHz (HOCO × 1/2) FlashIF clock (FCLK):10 MHz (HOCO × 1/2) External bus clock (BCLK):10 MHz (HOCO × 1/2) PPLL: 200 MHz (HOCO × 1/1 × 10) Ethernet-PHY External Clock (CLKOUT25M): 25 MHz (PPLL × 1/8) CLKOUT: 240 kHz (HOCO × 1/1)
	Main clock selected as system clock (Nos. 7 and 8 in Table 1.2)	Main clock: 24 MHz System clock (ICLK): 750 kHz (main clock × 1/32) Peripheral module clock A (PCLKA):750 kHz (main clock × 1/32) Peripheral module clocks B to D (PCLKB to PCLKD): 750 kHz (main clock × 1/32) FlashIF clock (FCLK):750 kHz (main clock × 1/32) External bus clock (BCLK):750 kHz (main clock × 1/32)

Item		Contents
Operating frequency	Main clock selected as system clock, CLKOUT used (No. 9 in Table 1.2)	Main clock: 24 MHz System clock (ICLK): 750 kHz (main clock × 1/32) Peripheral module clock A (PCLKA):750 kHz (main clock × 1/32) Peripheral module clocks B to D (PCLKB to PCLKD): 750 kHz (main clock × 1/32) FlashIF clock (FCLK):750 kHz (main clock × 1/32) External bus clock (BCLK):750 kHz (main clock × 1/32) CLKOUT: 240 kHz (HOCO × 1/1)
Operating voltage		3.3 V
Integrated development environment		Renesas Electronics e^2 studio Version: 2021-01
C compiler		Renesas Electronics C/C++ Compiler Package for RX Family V 3.02
		Compiler option The integrated development environment default settings are used.
iodefine.h version		V 1.00C
Endian order		Little endian or big endian
Operating mode		Single-chip mode
Processor mode		Supervisor mode
Sample code version		Version 1.01
Board used		Renesas Starter Kit+ for RX72N (Product No. RTK5572NNHSxxxxxBE)

3. Software

After disabling peripheral functions still running after a reset and making nonexistent port settings, the sample code makes clock settings.

3.1 Disabling Peripheral Functions Still Running After a Reset

The sample code disables peripheral functions still running after a reset.

Only the peripheral modules listed below are not in the module stop state after a reset is canceled. To transition a module to the module stop state, set the corresponding module stop bit to 1 (transition to module stop state). Putting modules into the module stop state can reduce the power consumption of the device.

In the sample code the value of the constant MSTP_STATE_<target module name> is 0 (MODULE_STOP_DISABLE), so the target module does not transition to the module stop state. To transition one or more modules to the module stop state on the target system, set the corresponding constant(s) to 1 (MODULE_STOP_ENABLE) in r_init_stop_module.h.

Table 3.1 lists the peripheral modules that are not in the module stop state after a reset.

Table 3.1 Peripheral Modules Not in Module Stop State After a Reset

Peripheral Module	**Module Stop Setting Bit**	**Value After Reset Setting When**	Not Using Module
EXDMAC	MSTPCRA.MSTPA29 bit	0 (module stop state canceled)	1 (transition to module stop state)
DMAC/DTC	MSTPCRA.MSTPA28 bit		
Standby RAM	MSTPCRC.MSTPC7 bit	0 (RAM operating)	1 (RAM stopped)
ECCRAM	MSTPCRC.MSTPC6 bit		
RAM	MSTPCRC.MSTPC0 bit		
Expansion RAM	MSTPCRC.MSTPC2 bit		

3.2 Nonexistent Port Settings

3.2.1 Processing Overview

The sample code sets the bits in the PDR registers corresponding to nonexistent ports to 1 (output). When writing in byte units to PDR or PODR registers containing nonexistent ports after this function has been called, set the direction control bits corresponding to the nonexistent ports to 1 and the port output data storage bits corresponding to the nonexistent ports to 0.

Table 3.2 lists the nonexistent ports.

Table 3.2 Nonexistent Ports

Port Symbol	224-Pin Products	Pins	176-Pin Products	Pins
PORT0	P04, P06	2	P04, P06	2
PORT1	—	—	—	—
PORT2	—	—	—	—
PORT3	—	—	—	—
PORT4	—	—	—	—
PORT5	—	—	—	—
PORT6	—	—	—	—
PORT7	—	—	—	—
PORT8	—	—	—	—
PORT9	—	—	—	—
PORTA	—	—	—	—
PORTB	—	—	—	—
PORTC	—	—	—	—
PORTD	—	—	—	—
PORTE	—	—	—	—
PORTF	PF6, PF7	2	PF6, PF7	2
PORTG	—	—	—	—
PORTH	—	—	PH0 to PH7	8
PORTJ	PJ4, PJ6, PJ7	3	PJ4, PJ6, PJ7	3
PORTK	—	—	PK0 to PK7	8
PORTL	—	—	PL0 to PL7	8
PORTM	—	—	PM0 to PM7	8
PORTN	PN6, PN7	2	PN0 to PN7	8
PORTQ	—	—	PQ0 to PQ7	8

Table 3.3 Nonexistent Ports

Port Symbol	145 and 144-Pin Products	Pins	100-Pin Products	Pins
PORT0	P04, P06	2	P00 to P04, P06	6
PORT1	P10, P11	2	P10, P11	2
PORT2	—	—	—	—
PORT3	—	—	—	—
PORT4	—	—	—	—
PORT5	P57	1	P56, P57	2
PORT6	—	—	P60 to P67	8
PORT7	—	—	P70 to P77	8
PORT8	P84, P85	2	P80 to P87	8
PORT9	P94 to P97	4	P90 to P97	8
PORTA	—	—	—	—
PORTB	—	—	—	—
PORTC	—	—	—	—
PORTD	—	—	—	—
PORTE	—	—	—	—
PORTF	PF0 to PF4, PF6, PF7	7	PF0 to PF7	8
PORTG	PG0 to PG7	8	PG0 to PG7	8
PORTH	PH0 to PH7	8	PH0 to PH7	8
PORTJ	PJ0 to PJ2, PJ4, PJ6, PJ7	6	PJ0 to PJ2, PJ4 to PJ7	7
PORTK	PK0 to PK7	8	PK0 to PK7	8
PORTL	PL0 to PL7	8	PL0 to PL7	8
PORTM	PM0 to PM7	8	PM0 to PM7	8
PORTN	PN0 to PN7	8	PN0 to PN7	8
PORTQ	PQ0 to PQ7	8	PQ0 to PQ7	8

3.2.2 Pin Count Setting

The setting in the sample code (PIN_SIZE=224) is for 224-pin products. The other pin counts supported by this application note are 176, 145, 144 and 100. If the pin count of the target device is other than 224, change the value of PIN_SIZE in r_init_port_initialize.h to match the target device.

3.3 Clock Settings

3.3.1 Clock Setting Procedure

Table 3.3 lists the steps in the clock setting procedure, the processing performed in each step, and the default settings of the sample code. Using the default settings, the sample code sets the PLL clock as the main clock and turns off the HOCO, sub-clock, PPLL clock, and CLKOUT.

Table 3.4 Clock Setting Procedure

Step	Processing	Details of Processing		Sample Code Settings
1	Sub-clock setting*1	Not used	Initializes the sub-clock control circuit.	The sub-clock is not used.
		Used	Initializes the sub-clock control circuit, sets the drive capacity, and sets in SOSCWTCR the waiting time until output of the sub-clock to the internal clock starts; then starts oscillation by the sub-clock. After this, waits for the clock oscillation stabilization waiting time*2.	
2	Main clock setting*1	Not used	No settings required.	The main clock is used.
		Used	Sets the main clock drive capacity and sets in MOSCWTCR the waiting time until output of the main clock to the internal clocks starts, then starts oscillation by the main clock. After this, waits for the clock oscillation stabilization waiting time*2.	
3	HOCO clock setting*1	Not used	Turns off the HOCO power supply.	The HOCO is not used.
		Used	Sets the HOCO frequency, then starts oscillation by the HOCO clock. After this, waits for the clock oscillation stabilization waiting time*2.	
4	Settings for specific applications *3	Clock source other than PPLL used	No settings required.	The PPLL is not used.
		PPLL used	Selects the clock source.	
5	PLL clock setting*1	Not used	No settings required.	The PLL clock is used.
		Used	Sets the PLL input division ratio and frequency multiplication factor, then starts oscillation by the PLL clock. After this, waits for the clock oscillation stabilization waiting time*2.	
6	PPLL clock setting*1	Not used	No settings required.	The PPLL clock is not used.
		Used	Sets the PPLL input division ratio and frequency multiplication factor, then starts oscillation by the PPLL clock. After this, waits for the clock oscillation stabilization waiting time*2 and then sets the PPLL clock division ratio.	

Step	Processing	Details of Processing		Sample Code Settings
7	Clock division ratio settings and system clock switching*4*5	Switches according to the system used.		• ICLK: × 1/1 • PCLKA: × 1/2 • PCLKB to PCLKD, BCLK, and FCLK: × 1/4 • BCLK: Output stopped Switches to PLL clock.
8	Operating power control mode setting	Sets the operating power control mode according to the operating frequency and operating voltage used.		High-speed operating mode is selected.
9	CLKOUT setting*6	Not used	No settings required.	The CLKOUT is not used.
		Used	Selects the clock source output on the CLKOUT pin and sets the clock division ratio. After this, enables output on the CLKOUT pin.	

Notes: 1. Change the values of the constants in r_init_clock.h as necessary to match the selection of the clocks you wish to use or not use.
2. Confirms that the appropriate bit in the oscillation stabilization flag register (OSCOVFSR) is set to 1.
3. Selects the clock source for the Ethernet-PHY external clock, and USB clock.
4. When changing the ICLK frequency from less than 70 MHz to 70 MHz or higher, and if the ratio of the frequencies before and after the change is greater than 4×, it is necessary to set the frequency once to 1/4 of the frequency after the change, wait 3 µs, and then set the target frequency. The sample code supports this processing. Change the settings in r_init_clock.h as required.
5. When changing the ICLK frequency from 70 MHz or higher to less than 70 MHz, and if the ratio of the frequencies before and after the change is greater than 1/4, it is necessary to set the frequency once to 1/4 of the frequency before the change, wait 3 µs, and then set the target frequency.
6. The sample code only makes the CLKOUT oscillation settings. To actually output this clock, refer to section 22, I/O Ports, and section 23, Multi-Function Pin Controller (MPC), in RX72N Group User's Manual: Hardware, and make settings appropriate for your system.

3.4 Section Composition

Figure 3.4 lists section information changed in the sample code. For instructions for adding, changing, and deleting sections, refer to the latest version of RX Family: CC-RX Compiler User's Manual.

Table 3.5 Changes to Section Information in Sample Code

Section Name	Change	Address	Description
End_of_RAM	Add	0007 FFFCh	On-chip RAM end address
End_of_EXRAM	Add	0087 FFFCh	On-chip Expansion RAM end address
End_of_ECCRAM	Add	00FF FFFCh	ECCRAM end address

3.5 File Composition

Table 3.5 lists the files used in the sample code. Files generated by the integrated development environment are not included in this table.

Table 3.6 Files Used in the Sample Code

File Name	Outline	Remarks
main.c	Main processing routine	
r_init_stop_module.c	Disable peripheral functions still running after a reset	
r_init_stop_module.h	Header file of r_init_stop_module.c	
r_init_port_initialize.c	Initial nonexistent port settings	
r_init_port_initialize.h	Header file of r_init_port_initialize.c	
r_init_clock.c	Initial clock settings	
r_init_clock.h	Header file of r_init_clock.c	
r_init_rom_cache.c	Initial ROM cache settings	
r_init_rom_cache.h	Header file of r_init_rom_cache.c	

3.6 Option-Setting Memory

Table 3.6 lists the option-setting memory configured in the sample code. When necessary, set a value suited to the user system.

Table 3.7 Option-Setting Memory Configured in the Sample Code

Symbol	Address	Setting Value	Contents
OFS0	FE7F 5D07 to FE7F 5D04h	FFFF FFFFh	IWDT stopped after a reset WDT stopped after a reset
OFS1	FE7F 5D0Bh to FE7F 5D08h	FFFF FFFFh	Voltage monitor 0 reset disabled after a reset HOCO oscillation disabled after a reset
MDE	FE7F 5D03h to FE7F 5D00h	FFFF FFFFh	Little endian Linear mode

3.7 Constants

Table 3.8 to Table 3.15 list the constants used by the sample code.

Table 3.8 Constants (User Changeable) Used by Sample Code (1/3)

Constant Name	Setting Value	Description
SEL_MAIN*1	B_USE	Main clock enable/disable selection B_USE: Used (main clock enabled) B_NOT_USE: Not used (main clock disabled)
MAIN_CLOCK_HZ*1	24,000,000 L	Main clock oscillator frequency (Hz)
REG_MOFCR*1	00h	Main clock oscillator drive capacity setting (setting value of MOFCR register)
REG_MOSCWTCR*1	53h	Setting value of main clock wait control register
SEL_SUB*1*2	B_NOT_USE	Sub-clock usage selection (used as system clock) B_USE: Used B_NOT_USE: Not used
SEL_RTC*1*2	B_NOT_USE	Sub-clock usage selection (used as RTC count source) B_USE: Used B_NOT_USE: Not used
SUB_CLOCK_HZ*1	32,768 L	Sub-clock oscillator frequency (Hz)
REG_SOSCWTCR*1	21h	Setting value of sub-clock wait control register
REG_RCR3*1	CL_STD	Sub-clock oscillator drive capacity selection CL_STD: Drive capacity for standard clock CL_LOW: Drive capacity for low clock
SEL_PLL*1	B_USE	PLL clock enable/disable selection B_USE: Used (PLL clock enabled) B_NOT_USE: Not used (PLL clock disabled)
REG_PLLCR*1	1300h	PLL input division ratio and frequency multiplication factor settings (setting value of PLLCR register)
SEL_PPLL*1	B_NOT_USE	PPLL clock enable/disable selection B_USE: Used (PPLL clock enabled) B_NOT_USE: Not used (PPLL clock disabled)
REG_PPLLCR*1	3102h	PPLL input division ratio and frequency multiplication factor settings (setting value of PPLLCR register)
SEL_CLKOUT*1	CKOUT_NOT_USE	CKOCR setting values CKOUT_USE: CLKOUT pin output enabled CKOUT_NOT_USE: CLKOUT pin output disabled (fixed low)

Notes: 1. Change the settings values in r_init_clock.h to match the target system.
2. The sub-clock oscillates when either SEL_SUB or SEL_RTC, or both of them, are set to B_USE (use).

Table 3.9 Constants (User Changeable) Used by Sample Code (2/3)

Constant Name	Setting Value	Description
CKO_CLK*1	CKO_LOCO	CLKOUT clock source selection CKO_LOCO: LOCO CKO_HOCO: HOCO CKO_MAIN: main clock CKO_SUB: sub-clock CKO_PLL: PLL CKO_PPLL: PPLL
CKO_DIV*1	0h	CLKOUT output division ratio selection 0h: × 1/1 1h: × 1/2 2h: × 1/4 3h: × 1/8 4h: × 1/16
SEL_HOCO*1	B_NOT_USE	HOCO clock enable/disable selection B_USE: Used (HOCO clock enabled) B_NOT_USE: Not used (HOCO clock disabled)
REG_HOCOCR2*1	FREQ_20MHZ	HOCO clock frequency selection FREQ_16MHZ: 16 MHz FREQ_18MHZ: 18 MHz FREQ_20MHZ: 20 MHz
SEL_SYSCLK*1	CLK_PLL	System clock source selection CLK_PLL: PLL CLK_ HOCO: HOCO CLK_ MAIN: main clock CLK_SUB: sub-clock
SEL_CLKOUT25M*1	PPLL_NOT_USE	Ethernet-PHY External Clock source selection PPLL_USE: Use frequency-divided PPLL clock. PPLL_NOT_USE: Do not use frequency-divided PPLL clock. (Use frequency-divided PLL clock.)
SEL_UCLK*1	PPLL_NOT_USE	USB module clock source selection PPLL_USE: Use frequency-divided PPLL clock. PPLL_NOT_USE: Do not use frequency-divided PPLL clock. (Use frequency-divided USB clock.)
ICLK_WAIT*1	B_USE	Selection of processing to support precautions when changing ICLK*2 B_USE: Use processing to support precautions. B_NOT_USE: Do not processing to support precautions.
REG_OPCCR*1	OPCM_HIGH	Operating power control mode selection*5 OPCM_HIGH: High-speed operating mode OPCM_LOW_1: Low-speed operating mode 1*3 OPCM_LOW_2: Low-speed operating mode 2*4

Notes: 1. Change the settings values in r_init_clock.h to match the target system.
2. When changing the ICLK frequency from less than 70 MHz to 70 MHz or higher, and if the ratio of the frequencies before and after the change is greater than 4×, it is necessary to set the frequency once to 1/4 of the frequency after the change, wait 3 µs, and then set the target frequency. Change the settings to match your system.
3. It is not possible to select low-speed operating mode 1 when the PLL or PPLL is set to oscillate.
4. Use this setting when PLL, PPLL, and HOCO are all set not to oscillate. Also, it is not possible to select low-speed operating mode 2 unless the sub-clock is set as the system clock and the ICK or FCK division ratio is set to 1/1.
5. The operating frequency range and operating voltage range differ depending on the operating mode. For details, see RX72N Group User's Manual: Hardware.

Table 3.10 Constants (User Changeable) Used by Sample Code (3/3)

Constant Name	Setting Value	Description
MSTP_STATE_EXDMAC*1	MODULE_STOP_ DISABLE	EXDMAC module stop state selection MODULE_STOP_DISABLE: Disable module stop MODULE_STOP_ENABLE: Transition to module stop
MSTP_STATE_DMACDTC*1	MODULE_STOP_ DISABLE	DMAC and DTC module stop state selection MODULE_STOP_DISABLE: Disable module stop MODULE_STOP_ENABLE: Transition to module stop
MSTP_STATE_STBYRAM*1	MODULE_STOP_ DISABLE	Standby RAM module stop state selection MODULE_STOP_DISABLE: Operating MODULE_STOP_ENABLE: Stopped
MSTP_STATE_ECCRAM*1	MODULE_STOP_ DISABLE	ECCRAM module stop state selection MODULE_STOP_DISABLE: Operating MODULE_STOP_ENABLE: Stopped
MSTP_STATE_RAM*1	MODULE_STOP_ DISABLE	RAM module stop state selection MODULE_STOP_DISABLE: Operating MODULE_STOP_ENABLE: Stopped
MSTP_STATE_EXRAM*1	MODULE_STOP_ DISABLE	Expansion RAM module stop state selection MODULE_STOP_DISABLE: Operating MODULE_STOP_ENABLE: Stopped
PIN_SIZE*2	224	Pin count of target device
SEL_ROM_CACHE*4	CACHE_ENABLE	ROM cache enable/disable CACHE_ENABLE: Cache enabled CACHE_DISABLE: Cache disabled
SEL_NON_CHCHEABLE_ AREA0*4	SEL_NON_ CACHEABLE_ AREA_DISABLE	Non-cacheable area 0 enable/disable SEL_NON_CACHEABLE_AREA_ENABLE: Enabled SEL_NON_CACHEABLE_AREA_DISABLE: Disabled
SEL_NON_CHCHEABLE_ AREA1*4	SEL_NON_ CACHEABLE_ AREA_DISABLE	Non-cacheable area 1 enable/disable SEL_NON_CACHEABLE_AREA_ENABLE: Enabled SEL_NON_CACHEABLE_AREA_DISABLE: Disabled
REG_MEMWAIT*3	MEMWAIT_1WAIT	Memory wait cycle selection MEMWAIT_0WAIT: 0 wait cycles MEMWAIT_1WAIT: 1 wait cycle

Notes: 1. Change the settings values in r_init_stop_module.h to match the target system.
2. Change the settings values in r_init_port_initialize.h to match the target system.
3. Do not select the 0 wait cycles setting when the ICLK frequency is 120 MHz or above. Do not select the 1 wait cycle setting when the operating power control state is low-speed operating mode 2.
4. Change the settings values in r_init_rom_cache.h to match the target system.

Table 3.11 Constants (Non User Changeable) Used by Sample Code

Constant Name	Setting Value	Description
B_NOT_USE	0	Not used
B_USE	1	Used
CL_LOW	02h	Sub-clock: Drive capacity for low clock
CL_STD	0Ch	Sub-clock: Drive capacity for standard clock
FREQ_16MHZ	00h	HOCO frequency: 16 MHz
FREQ_18MHZ	01h	HOCO frequency: 18 MHz
FREQ_20MHZ	02h	HOCO frequency: 20 MHz
CLK_PLL	0400h	System clock source: PLL
CLK_HOCO	0100h	System clock source: HOCO
CLK_SUB	0300h	System clock source: Sub-clock
CLK_MAIN	0200h	System clock source: Main clock
MEMWAIT_0WAIT	0	Memory wait cycles: 0 wait cycles
MEMWAIT_1WAIT	1	Memory wait cycles: 1 wait cycle
REG_SCKCR*1	20C9 1222h (PLL selected) 10C1 0111h (HOCO selected) 00C0 0000h (sub-clock selected) 55C5 5555h (other than the above)	Internal clock division ratio and BCLK/SDCLK pin output control settings (setting value of SCKCR register)
REG_SCKCR2	0011h	USB clock division ratio (set value when USB not used)
PPLL_USE	1	PPLL used as clock source
PPLL_NOT_USE	0	Other than PPLL used as clock source
CKOUT_USE	0	CLKOUT used LOCO selected, division ratio × 1/1, CLKOUT pin output enabled
CKOUT_NOT_USE	1	CLKOUT not used LOCO selected, division ratio × 1/1, CLKOUT pin output disabled
CKO_LOCO	0h	CLKOUT clock source: LOCO
CKO_HOCO	1h	CLKOUT clock source: HOCO
CKO_MAIN	2h	CLKOUT clock source: MAIN
CKO_SUB	3h	CLKOUT clock source: SUB
CKO_PLL	4h	CLKOUT clock source: PLL
CKO_PPLL	6h	CLKOUT clock source: PPLL
OPCM_HIGH	00h	Operating power control mode: High-speed operating mode
OPCM_LOW_1	06h	Operating power control mode: Low-speed operating mode 1
OPCM_LOW_2	07h	Operating power control mode: Low-speed operating mode 2
SUB_CLOCK_CYCLE	(1,000,000,000L / SUB_CLOCK_HZ)	Sub-clock cycle (ns)
RTC_WAIT_TIME	121212L	Count cycle (ns) of timer for RTC software wait cycles (CMT0) = 1/LOCO (264 kHz) × 32
ICLK_WAIT_TIME	533333L	Count cycle (µs) timer (CMT0) for ICLK change = 1/PLL4 (60 MHz) × 32
CACHE_ENABLE	1	ROM cache enabled
CACHE_DISABLE	0	ROM cache disabled

Constant Name	Setting Value	Description
MODULE_STOP_ENABLE	1	Transition to module stop state
MODULE_STOP_DISABLE	0	Module stop state canceled
NON_CACHEABLE_AREA_ENABLE	1	Non-cacheable area enabled
NON_CACHEABLE_AREA_DISABLE	0	Non-cacheable area disabled

Note: 1. The setting value differs depending on the selected system clock source.

Table 3.12 Constants for 224-Pin Products (PIN_SIZE=224)

Constant Name	Setting Value	Description
DEF_P0PDR	0x50	Port P0 direction register setting value
DEF_P1PDR	0x00	Port P1 direction register setting value
DEF_P2PDR	0x00	Port P2 direction register setting value
DEF_P3PDR	0x00	Port P3 direction register setting value
DEF_P4PDR	0x00	Port P4 direction register setting value
DEF_P5PDR	0x00	Port P5 direction register setting value
DEF_P6PDR	0x00	Port P6 direction register setting value
DEF_P7PDR	0x00	Port P7 direction register setting value
DEF_P8PDR	0x00	Port P8 direction register setting value
DEF_P9PDR	0x00	Port P9 direction register setting value
DEF_PAPDR	0x00	Port PA direction register setting value
DEF_PBPDR	0x00	Port PB direction register setting value
DEF_PCPDR	0x00	Port PC direction register setting value
DEF_PDPDR	0x00	Port PD direction register setting value
DEF_PEPDR	0x00	Port PE direction register setting value
DEF_PFPDR	0xC0	Port PF direction register setting value
DEF_PGPDR	0x00	Port PG direction register setting value
DEF_PHPDR	0x00	Port PH direction register setting value
DEF_PJPDR	0xD0	Port PJ direction register setting value
DEF_PKPDR	0x00	Port PK direction register setting value
DEF_PLPDR	0x00	Port PL direction register setting value
DEF_PMPDR	0x00	Port PM direction register setting value
DEF_PNPDR	0xC0	Port PN direction register setting value
DEF_PQPDR	0x00	Port PQ direction register setting value

Table 3.13 Constants for 176-Pin Products (PIN_SIZE=176)

Constant Name	Setting Value	Description
DEF_P0PDR	0x50	Port P0 direction register setting value
DEF_P1PDR	0x00	Port P1 direction register setting value
DEF_P2PDR	0x00	Port P2 direction register setting value
DEF_P3PDR	0x00	Port P3 direction register setting value
DEF_P4PDR	0x00	Port P4 direction register setting value
DEF_P5PDR	0x00	Port P5 direction register setting value
DEF_P6PDR	0x00	Port P6 direction register setting value
DEF_P7PDR	0x00	Port P7 direction register setting value
DEF_P8PDR	0x00	Port P8 direction register setting value
DEF_P9PDR	0x00	Port P9 direction register setting value
DEF_PAPDR	0x00	Port PA direction register setting value
DEF_PBPDR	0x00	Port PB direction register setting value
DEF_PCPDR	0x00	Port PC direction register setting value
DEF_PDPDR	0x00	Port PD direction register setting value
DEF_PEPDR	0x00	Port PE direction register setting value
DEF_PFPDR	0xC0	Port PF direction register setting value
DEF_PGPDR	0x00	Port PG direction register setting value
DEF_PHPDR	0xFF	Port PH direction register setting value
DEF_PJPDR	0xD0	Port PJ direction register setting value
DEF_PKPDR	0xFF	Port PK direction register setting value
DEF_PLPDR	0xFF	Port PL direction register setting value
DEF_PMPDR	0xFF	Port PM direction register setting value
DEF_PNPDR	0xFF	Port PN direction register setting value
DEF_PQPDR	0xFF	Port PQ direction register setting value

Table 3.14 Constants for 145 and 144-Pin Products (PIN_SIZE=145 or 144)

Constant Name	Setting Value	Description
DEF_P0PDR	0x50	Port P0 direction register setting value
DEF_P1PDR	0x03	Port P1 direction register setting value
DEF_P2PDR	0x00	Port P2 direction register setting value
DEF_P3PDR	0x00	Port P3 direction register setting value
DEF_P4PDR	0x00	Port P4 direction register setting value
DEF_P5PDR	0x80	Port P5 direction register setting value
DEF_P6PDR	0x00	Port P6 direction register setting value
DEF_P7PDR	0x00	Port P7 direction register setting value
DEF_P8PDR	0x30	Port P8 direction register setting value
DEF_P9PDR	0xF0	Port P9 direction register setting value
DEF_PAPDR	0x00	Port PA direction register setting value
DEF_PBPDR	0x00	Port PB direction register setting value
DEF_PCPDR	0x00	Port PC direction register setting value
DEF_PDPDR	0x00	Port PD direction register setting value
DEF_PEPDR	0x00	Port PE direction register setting value
DEF_PFPDR	0xDF	Port PF direction register setting value
DEF_PGPDR	0xFF	Port PG direction register setting value
DEF_PHPDR	0xFF	Port PH direction register setting value
DEF_PJPDR	0xD7	Port PJ direction register setting value
DEF_PKPDR	0xFF	Port PK direction register setting value
DEF_PLPDR	0xFF	Port PL direction register setting value
DEF_PMPDR	0xFF	Port PM direction register setting value
DEF_PNPDR	0xFF	Port PN direction register setting value
DEF_PQPDR	0xFF	Port PQ direction register setting value

Table 3.15 Constants for 100-Pin Products (PIN_SIZE=100)

Constant Name	Setting Value	Description
DEF_P0PDR	0x5F	Port P0 direction register setting value
DEF_P1PDR	0x03	Port P1 direction register setting value
DEF_P2PDR	0x00	Port P2 direction register setting value
DEF_P3PDR	0x00	Port P3 direction register setting value
DEF_P4PDR	0x00	Port P4 direction register setting value
DEF_P5PDR	0xC0	Port P5 direction register setting value
DEF_P6PDR	0xFF	Port P6 direction register setting value
DEF_P7PDR	0xFF	Port P7 direction register setting value
DEF_P8PDR	0xFF	Port P8 direction register setting value
DEF_P9PDR	0xFF	Port P9 direction register setting value
DEF_PAPDR	0x00	Port PA direction register setting value
DEF_PBPDR	0x00	Port PB direction register setting value
DEF_PCPDR	0x00	Port PC direction register setting value
DEF_PDPDR	0x00	Port PD direction register setting value
DEF_PEPDR	0x00	Port PE direction register setting value
DEF_PFPDR	0xFF	Port PF direction register setting value
DEF_PGPDR	0xFF	Port PG direction register setting value
DEF_PHPDR	0xFF	Port PH direction register setting value
DEF_PJPDR	0xF7	Port PJ direction register setting value
DEF_PKPDR	0xFF	Port PK direction register setting value
DEF_PLPDR	0xFF	Port PL direction register setting value
DEF_PMPDR	0xFF	Port PM direction register setting value
DEF_PNPDR	0xFF	Port PN direction register setting value
DEF_PQPDR	0xFF	Port PQ direction register setting value

3.8 Functions

Table 3.13 lists the functions.

Table 3.16 Functions

Function Name	Outline
main	Main processing routine
R_INIT_StopModule	Disable peripheral functions still running after a reset
R_INIT_Port_Initialize	Initial nonexistent port settings
R_INIT_Clock	Initial clock settings
R_INIT_ROM_Cache	Initial ROM cache settings
cgc_oscillation_main	Main clock oscillation enable
cgc_oscillation_hoco	HOCO clock oscillation enable
cgc_oscillation_pll	PLL clock oscillation enable
cgc_oscillation_ppll	PPLL clock oscillation enable
cgc_oscillation_sub	Sub-clock oscillation enable
cgc_disable_subclk	Sub-clock disable
oscillation_subclk	Sub-clock oscillation enable
resetting_wtcr_subclk	Sub-clock wait control register resetting
init_rtc	RTC initialization
set_ad_conversion_time	Initialization of time for A/D conversion by successive approximation
cmt0_wait	Software wait cycles using CMT0
set_specific_module_clk	Specific module clock source settings
switch_sysclk	System clock switching
enable_clkout	CLKOUT oscillation settings

3.9 Function Specifications

The following tables list the sample code function specifications.

main	
Outline	Main processing routine
Header	None
Declaration	void main(void)
Description	Calls the settings function for disabling peripheral functions still running after a reset, the initial nonexistent port settings function, the initial clock settings function, and the initial ROM cache settings function.
Arguments	None
Return Value	None

R_INIT_StopModule	
Outline	Disable peripheral functions still running after a reset
Header	r_init_stop_module.h
Declaration	void R_INIT_StopModule(void)
Description	Makes settings to transition to the module stop state.
Arguments	None
Return Value	None
Remarks	In the sample code, no transition to the module stop state occurs.

R_INIT_Port_Initialize	
Outline	Initial nonexistent port settings
Header	r_init_port_initialize.h
Declaration	void R_INIT_port_initialize (void)
Description	Makes initial settings to the port direction registers corresponding to the pins of nonexistent port.
Arguments	None
Return Value	None
Remarks	The setting in the sample code (PIN_SIZE=224) is for 224-pin products. When writing in byte units to PDR or PODR registers containing nonexistent ports after this function has been called, set the direction control bits corresponding to the nonexistent ports to 1 and the port output data storage bits corresponding to the nonexistent ports to 0.

R_INIT_Clock	
Outline	Initial clock settings
Header	r_init_clock.h
Declaration	void R_INIT_Clock(void)
Description	Makes initial clock settings and specifies the number of wait cycles for access.
Arguments	None
Return Value	None
Remarks	In the sample code processing is selected that sets the PLL clock as the system clock, specifies one memory wait cycle, and does not use HOCO, sub-clock, PPLL, and CLKOUT. The set_ad_conversion_time function, which is called by the R_INIT_Clock function, must be called when the PSW.I and ADCSR.ADST bits both have a value of 0. Therefore, clear the PSW.I bit to 0 (interrupts disabled) and the ADCSR.ADST bit to 0 before calling the R_INIT_Clock function.

R_INIT_ROM_Cache	
Outline	Initial ROM cache settings
Header	r_init_ROM_Cache.h
Declaration	void R_INIT_ROM_Cache(void)
Description	After specifying the non-cacheable areas, enables the ROM cache.
Arguments	None
Return Value	None
Remarks	In the sample code, this function only makes it possible for the ROM cache to operate. It is assumed that this function will be called while the ROM cache is in the disabled state after the system starts. To specify non-cacheable areas after the ROM cache has been enabled, first disable the ROM cache and then call this function.

cgc_oscillation_main	
Outline	Main clock oscillation enable
Header	r_init_clock.h
Declaration	static void cgc_oscillation_main (void)
Description	Sets the drive capacity of the main clock and sets the MOSCWTCR register, then starts oscillation of the main clock. After this, waits for the main clock oscillation stabilization waiting time.
Arguments	None
Return Value	None

cgc_oscillation_pll	
Outline	PLL clock oscillation enable
Header	r_init_clock.h
Declaration	void cgc_oscillation_pll (void)
Description	Sets the PLL input division ratio and frequency multiplication factor, then starts oscillation of the PLL clock. After this, waits for the PLL clock oscillation stabilization waiting time.
Arguments	None
Return Value	None

cgc_oscillation_ppll	
Outline	PPLL clock oscillation enable
Header	r_init_clock.h
Declaration	static void cgc_oscillation_ppll (void)
Description	Sets the PPLL input division ratio and frequency multiplication factor, then starts oscillation of the PPLL clock. After this, waits for the PPLL clock oscillation stabilization time and then sets the PPLL clock division ratio.
Arguments	None
Return Value	None

cgc_oscillation_HOCO	
Outline	HOCO clock oscillation enable
Header	r_init_clock.h
Declaration	static void cgc_oscillation_hoco (void)
Description	Sets the HOCO frequency, then starts oscillation of the HOCO. After this, waits for the HOCO oscillation stabilization waiting time.
Arguments	None
Return Value	None

cgc_oscillation_sub	
Outline	Sub-clock oscillation enable
Header	r_init_clock.h
Declaration	static void cgc_oscillation_sub (void)
Description	Makes settings for using the sub-clock as the system clock or as the RTC count source, or for both.
Arguments	None
Return Value	None

cgc_disable_subclk	
Outline	Sub-clock disable
Header	r_init_clock.h
Declaration	static void cgc_disable_subclk (void)
Description	Makes settings for when the sub-clock is not used as the system clock or as the RTC count source.
Arguments	None
Return Value	None

oscillation_subclk	
Outline	Sub-clock oscillation enable
Header	None
Declaration	static void oscillation_subclk (void)
Description	Makes settings to start sub-clock oscillation.
Arguments	None
Return Value	None

resetting_wtcr_subclk	
Outline	Sub-clock wait control register resetting
Header	None
Declaration	static void resetting_wtcr_subclk (void)
Description	Resets the wait control register when returning from software standby mode. In this case the wait control register is set to the minimum value.
Arguments	None
Remarks	

init_rtc	
Outline	RTC initialization
Header	None
Declaration	static void init_rtc (void)
Description	Initializes the RTC (clock supply setting and RTC software reset).
Arguments	None
Return Value	None

set_ad_conversion_time	
Outline	Initialization of time for A/D conversion by successive approximation
Header	None
Declaration	static void set_ad_conversion_time (void)
Description	Initializes the time for A/D conversion by successive approximation.
Arguments	None
Return Value	None

cmt0_wait	
Outline	Makes software wait settings
Header	None
Declaration	static void cmt0_wait (uint32_t cnt)
Description	This is used when waiting for the start of a write to the RTC register and when waiting before changing ICLK.
Arguments	uint32_t cnt CMCOR register settings
Return Value	None

set_specific_module_clk	
Outline	Specific module clock source settings
Header	None
Declaration	static void set_specific_module_clk (void)
Description	Sets the clock sources for Ethernet-PHY External Clock and USB clock.
Arguments	None
Return Value	None

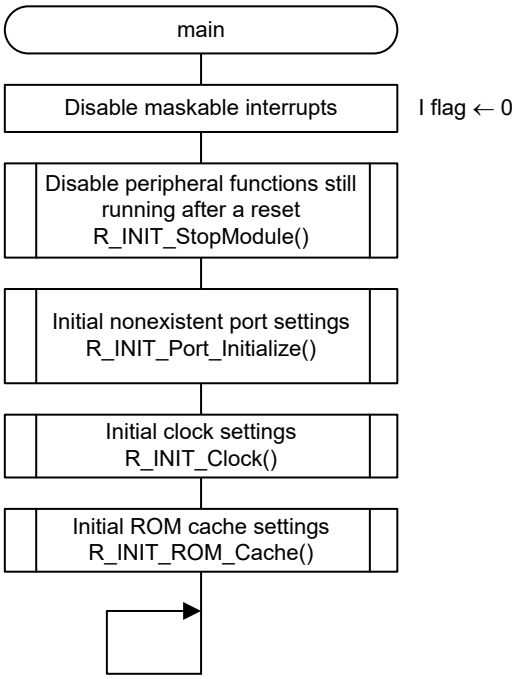
switch_sysclk	
Outline	System clock settings
Header	None
Declaration	static void swicht_sysclk (void)
Description	Sets the division ratio of the internal clock. Switches the system clock.
Arguments	None
Return Value	None

enable_clkout	
Outline	CLKOUT settings
Header	None
Declaration	static void enable_clkout (void)
Description	Makes CLKOUT oscillation settings.
Arguments	None
Return Value	None

3.10 Flowcharts

3.10.1 Main Processing

Figure 3.1 shows the main processing.

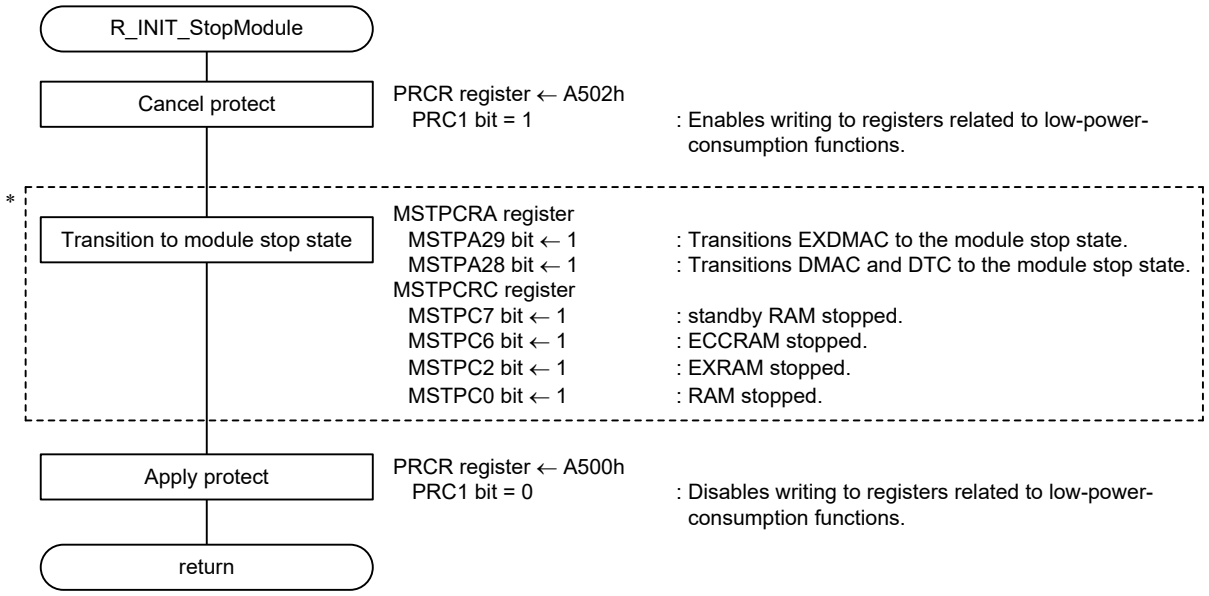


Note: Clear the PSW.I bit to 0 (interrupts disabled) and the ADCSR.ADST bit to 0 before calling this function. The default value of the ADCSR.ADST bit is 0, so the setting of ADCSR.ADST is not checked by the program accompanying this application note. If it is possible that the ADCSR.ADST may be manipulated before the R_INIT_Clock function is called, add appropriate processing to clear the ADCSR.ADST bit to 0.

Figure 3.1 Main Processing

3.10.2 Disable Peripheral Functions Still Running After a Reset

Figure 3.2 is a flowchart of the processing for disabling of peripheral functions still running after a reset.

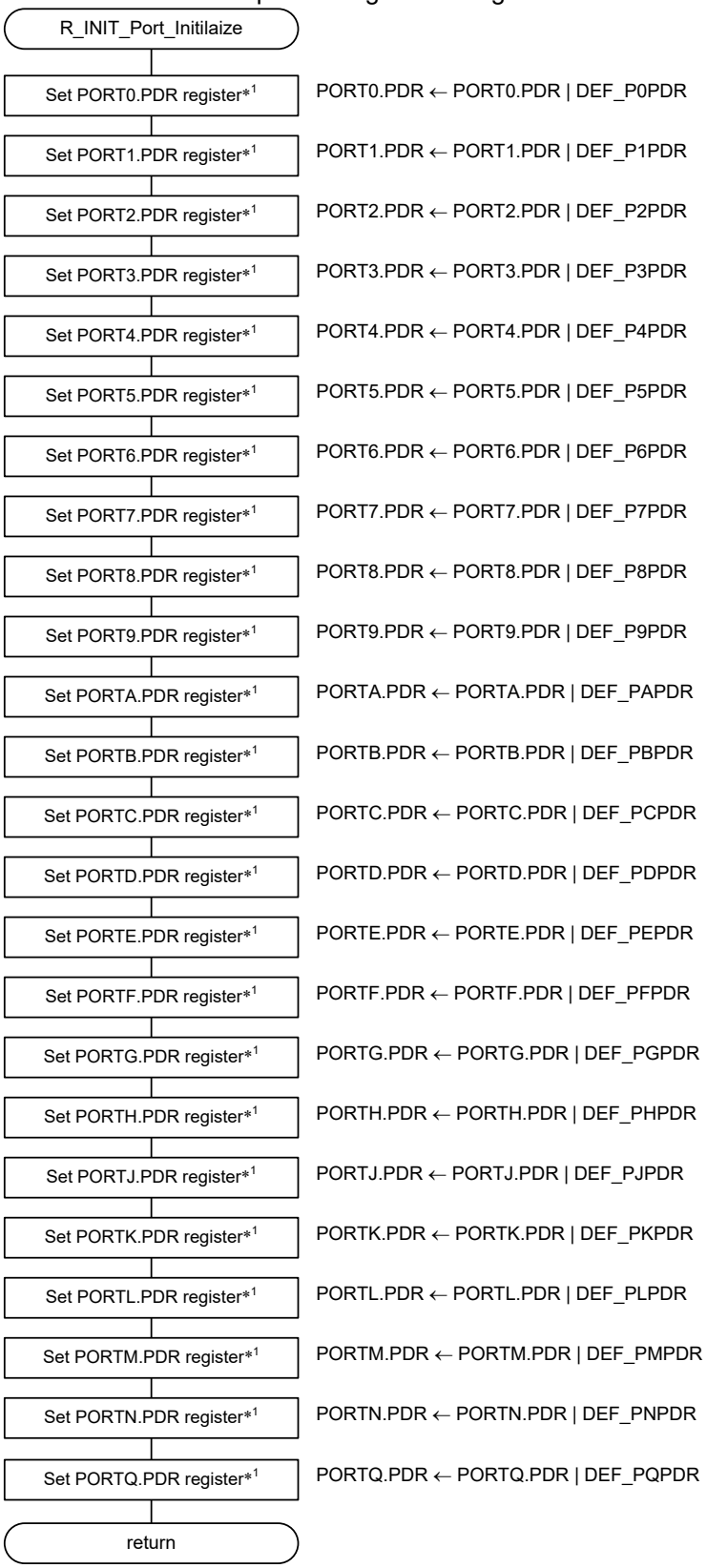


Note: 1.In the sample code the module stop state is canceled. To transition to the module stop state, set the corresponding constant #define MSTP_STATE_<target module name> to 1.

Figure 3.2 Disable Peripheral Functions Still Running After a Reset

3.10.3 Initial Nonexistent Port Settings

Figure 3.3 is a flowchart of the processing for making initial nonexistent port settings.

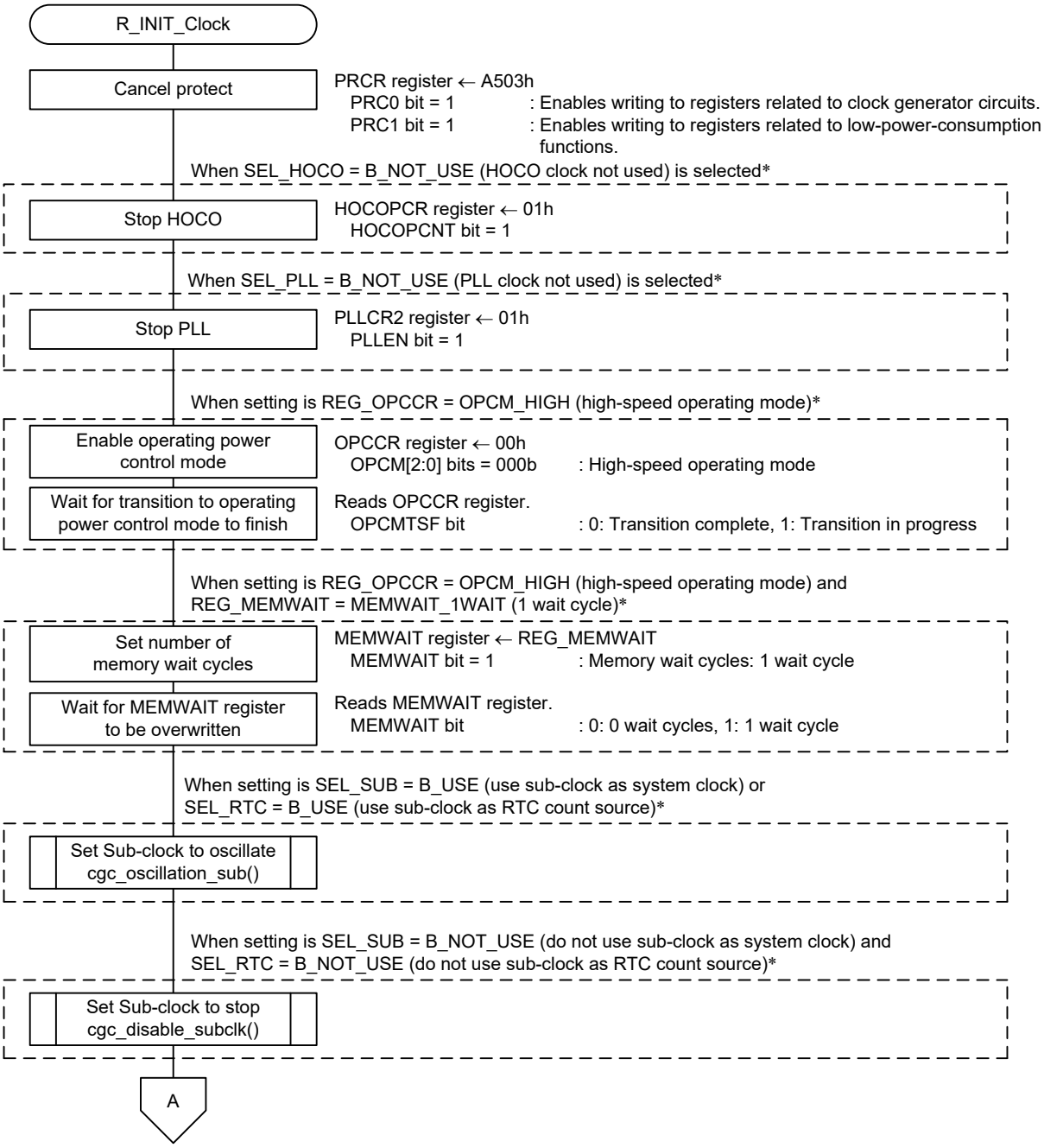


Note: 1.No processing of settings is performed for registers in which all bits correspond to existing pins (omitted during compile).

Figure 3.3 Initial Nonexistent Port Settings

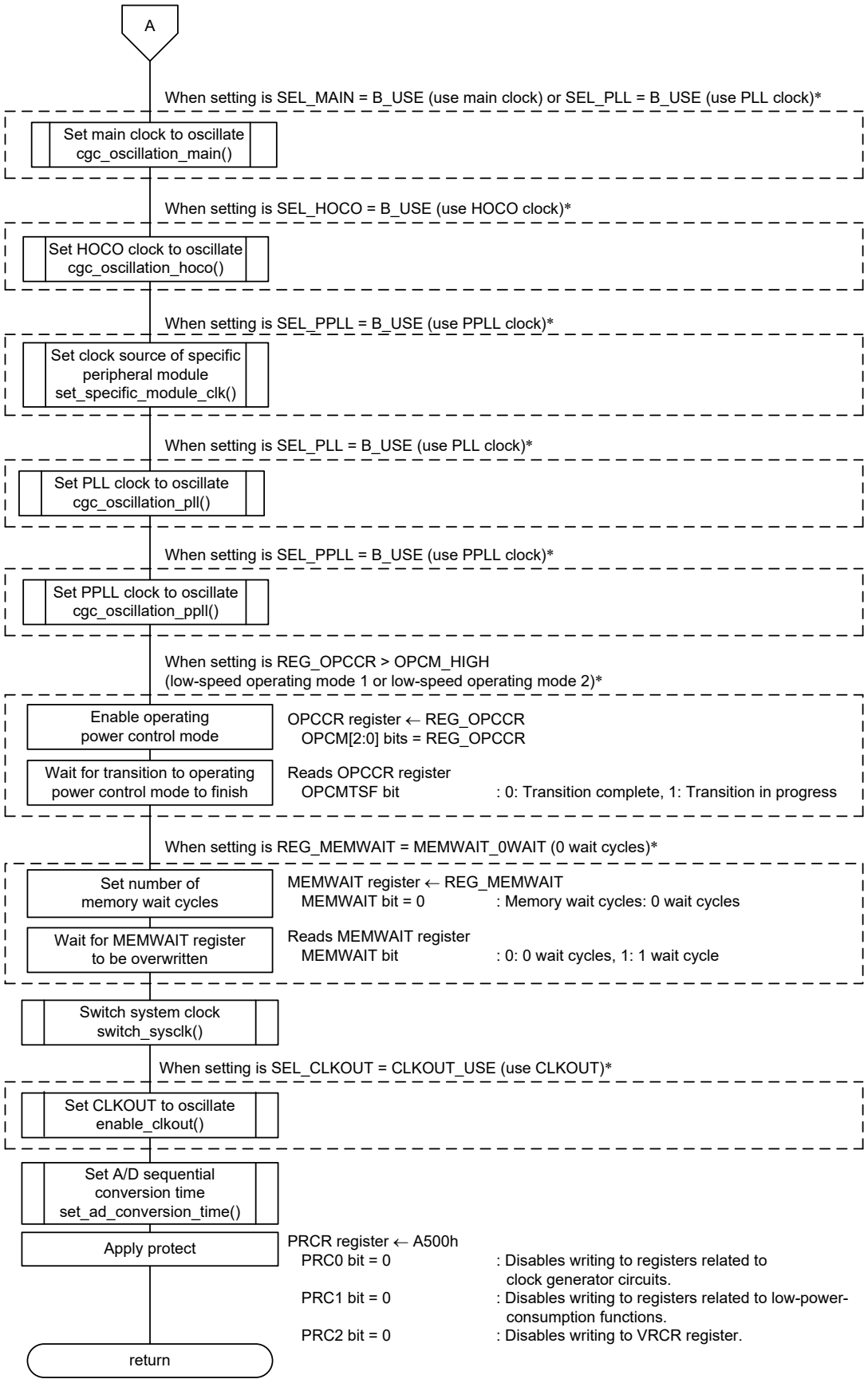
3.10.4 Initial Clock Settings

Figure 3.4 and Figure 3.5 are flowcharts of the processing for making initial clock settings (1/2) and (2/2).



Note: 1.Change the values of the relevant constants to match the characteristics of the target system.

Figure 3.4 Initial Clock Settings (1/2)

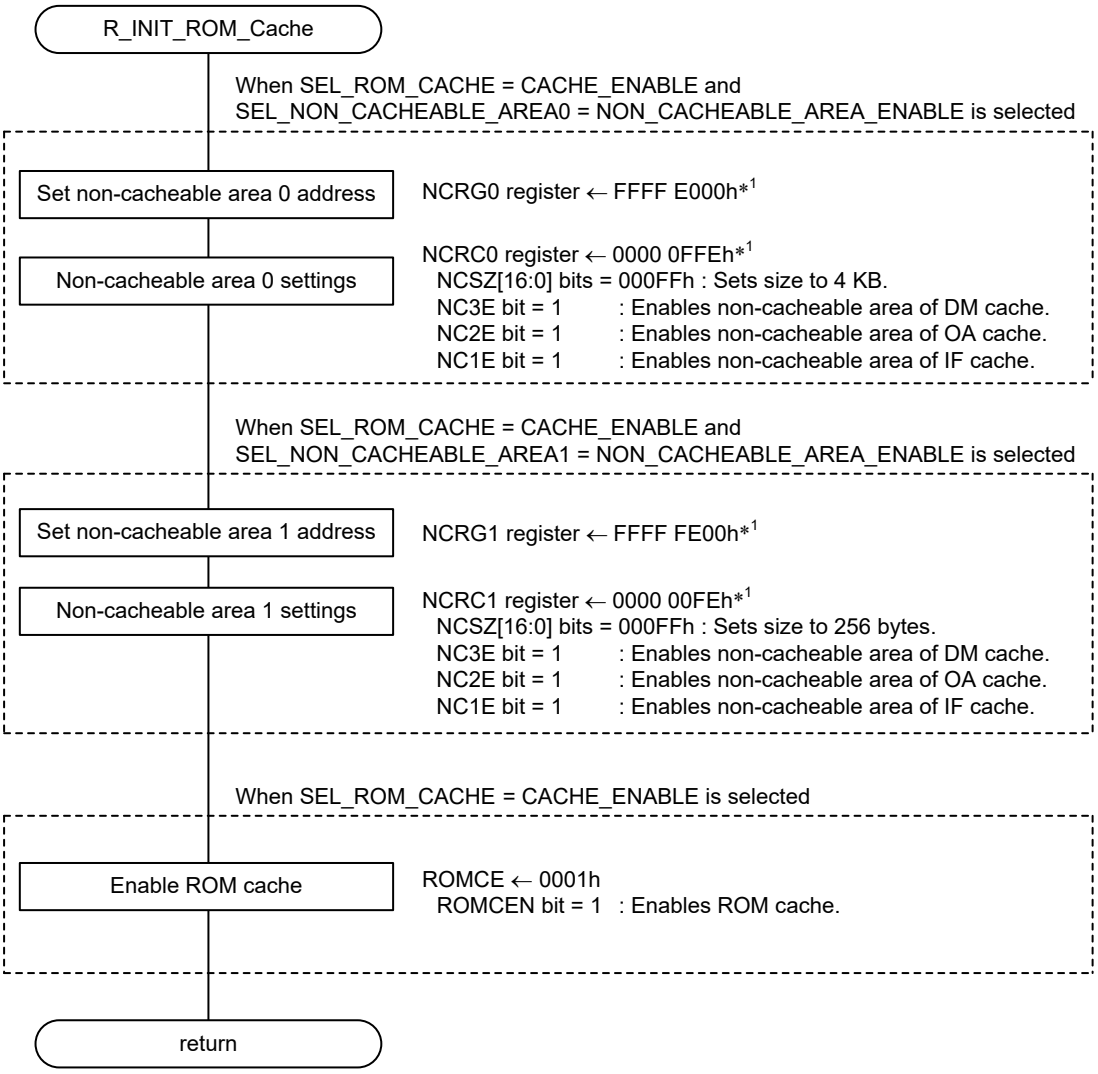


Note: 1.Change the values of the relevant constants to match the characteristics of the target system.

Figure 3.5 Initial Clock Settings (2/2)

3.10.5 ROM Cache Settings

Figure 3.6 is a flowchart of the processing for initial ROM cache settings.



Note: 1.Set the non-cacheable areas to match the characteristics of your system.

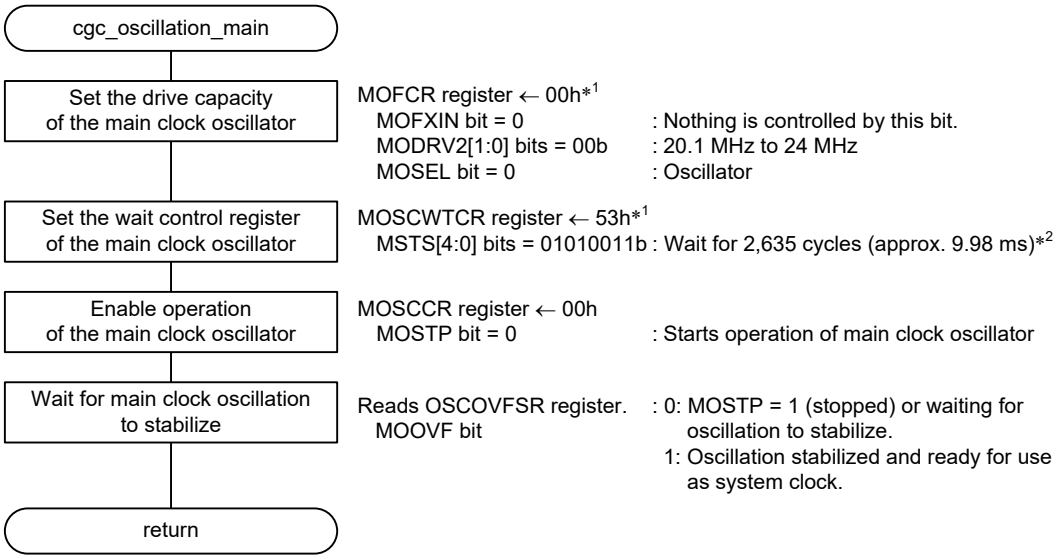
In the sample code it is assumed that this function will be called while the ROM cache is in the disabled state after the system starts.

To specify non-cacheable areas after the ROM cache has been enabled, first disable the ROM cache and then call this function.

Figure 3.6 Initial ROM Cache Settings

3.10.6 Main Clock Oscillation Enable

Figure 3.7 is a flowchart of the processing for starting oscillation of the main clock.



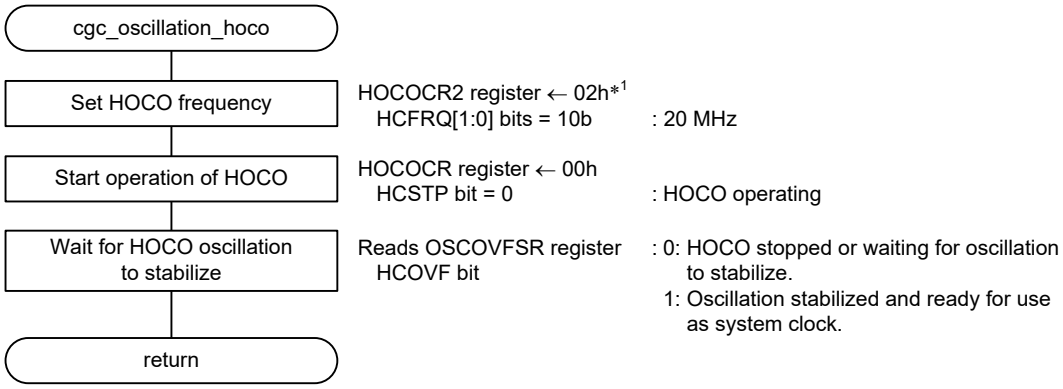
Notes: 1.Change the values of the relevant constants to match the characteristics of the target system.

2.The sample code accompanying this application note uses the initial value of the register.

Figure 3.7 Main Clock Oscillation Enable

3.10.7 HOCO Clock Oscillation Enable

Figure 3.8 is a flowchart of the processing for starting oscillation of the HOCO clock.



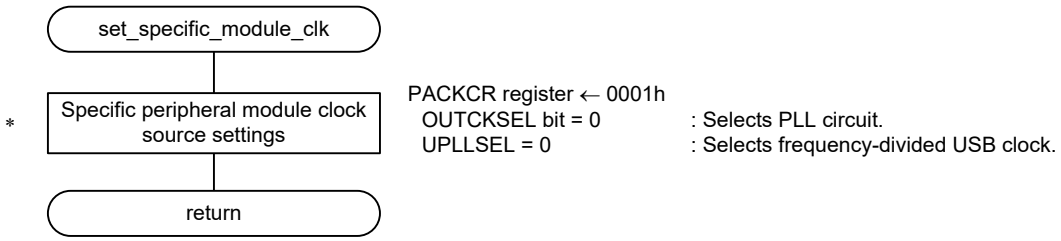
Notes: 1.Change the values of the relevant constants to match the characteristics of the target system.

2.The setting value differs according to the HOCO frequency selected by the constant.

Figure 3.8 HOCO Clock Oscillation Enable

3.10.8 Specific Module Clock Settings

Figure 3.9 is a flowchart of the processing for making specific module clock source settings.

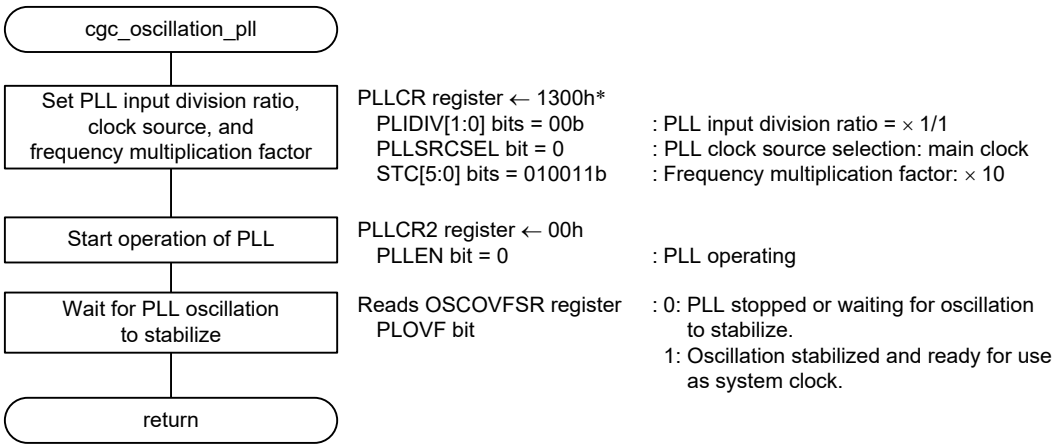


Note: 1.Change the clock source once only after a reset when PLL and PPLL are stopped and all modules that will be affected by the change are stopped.

Figure 3.9 Specific Module Clock Source Settings

3.10.9 PLL Clock Oscillation Enable

Figure 3.10 is a flowchart of the processing for starting oscillation of the PLL clock.

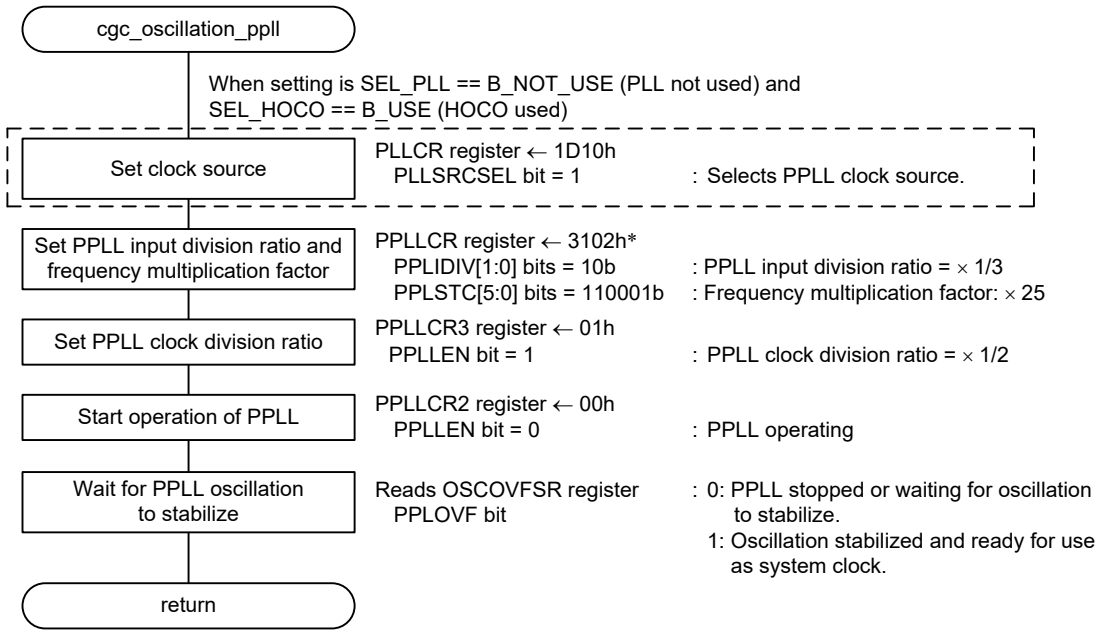


Note: 1.Change the values of the relevant constants to match the characteristics of the target system.

Figure 3.10 PLL Clock Oscillation Enable

3.10.10 PPLL Clock Oscillation Enable

Figure 3.11 is a flowchart of the processing for starting oscillation of the PPLL clock.

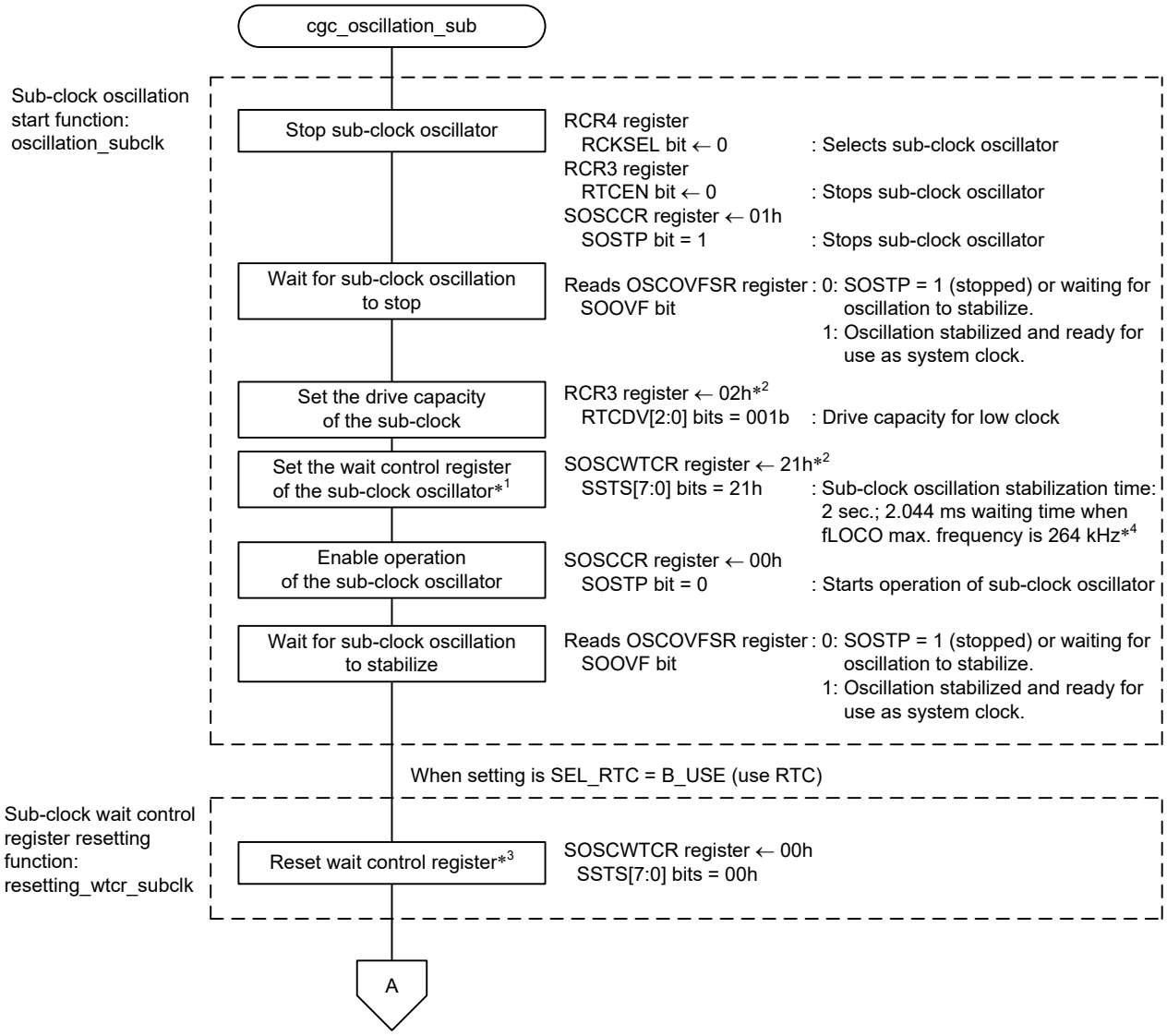


Note: 1.Change the values of the relevant constants to match the characteristics of the target system.

Figure 3.11 PPLL Clock Oscillation Enable

3.10.11 Sub-clock Oscillation Enable

Figure 3.12 and Figure 3.13 are flowcharts of the processing for starting oscillation of the sub-clock.



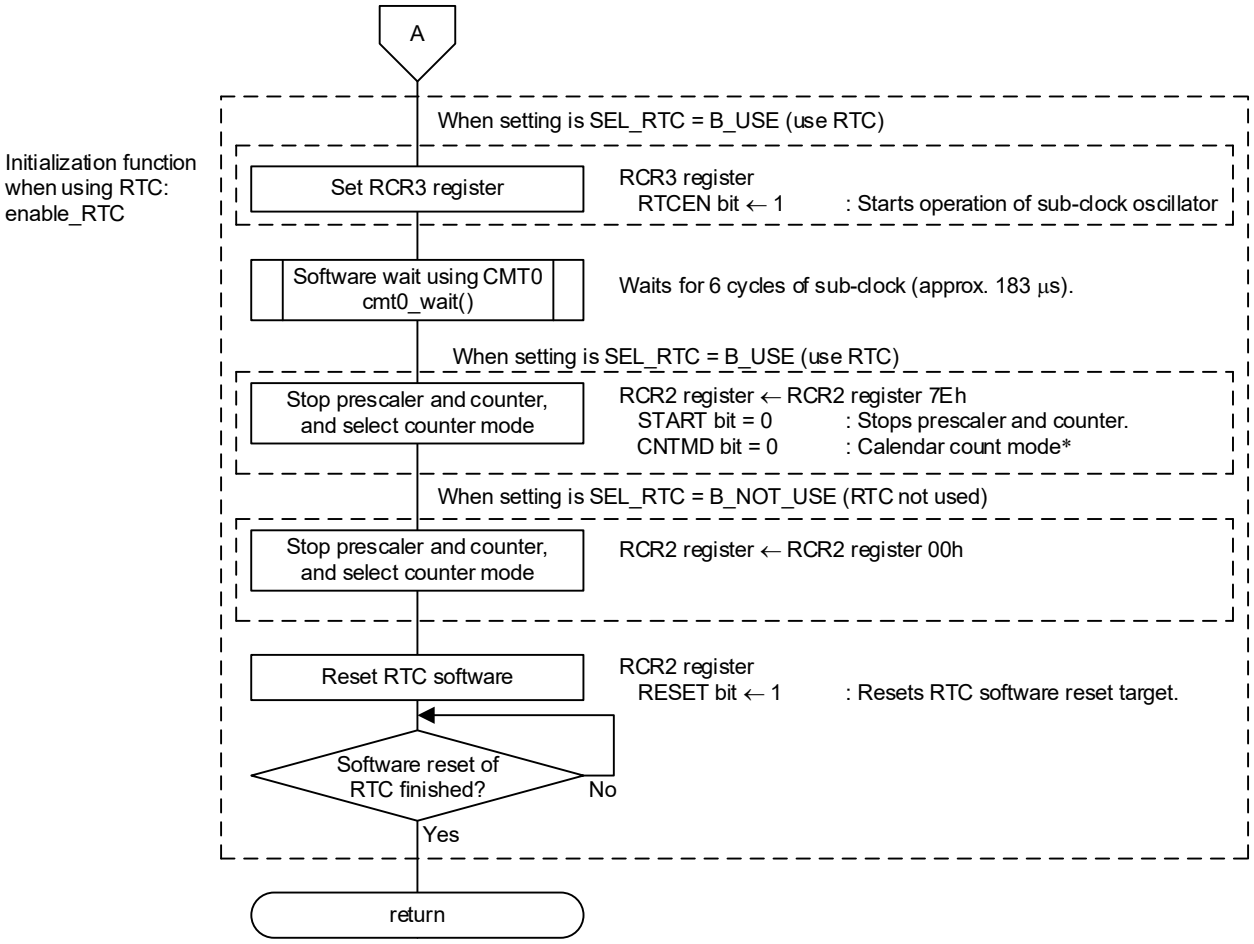
Notes: 1.Use the formulas in 9.2.18, Sub-Clock Oscillator Wait Control Register (SOSCWTCR), in RX72N Group User's Manual: Hardware to calculate the waiting time. Note that the sample code accompanying this application note uses the initial value of the register.

2.Change the value of the constant to match the characteristics of the target system.

3.When returning from software standby mode with the sub-clock selected as the system clock, supply of clock signals to the internals of the microcontroller starts after the time specified by bits SSTS4 to SSTS0 in SOSCWTCR has elapsed following generation of the return source. However, the sub-clock does not stop operating in software standby mode if value of the RTCEN bit in RCR3 is 1 (operates), in which case no oscillation stabilization time is needed for the sub-clock when returning from software standby mode. Therefore, bits SSTS7 to SSTS0 in SOSCWTCR are reset to 00h to minimize the sub-clock oscillation stabilization wait time.

4.The sample code accompanying this application note uses the initial value of the register.

Figure 3.12 Sub-clock Oscillation Enable (1/2)



Note: 1. The sample code accompanying this application note selects the calendar count mode. Change the values of the constants to match the characteristics of the target system.

Figure 3.13 Sub-clock Oscillation Enable (2/2)

3.10.12 Sub-clock Disable

Figure 3.14 is a flowchart of the processing for stopping the sub-clock.

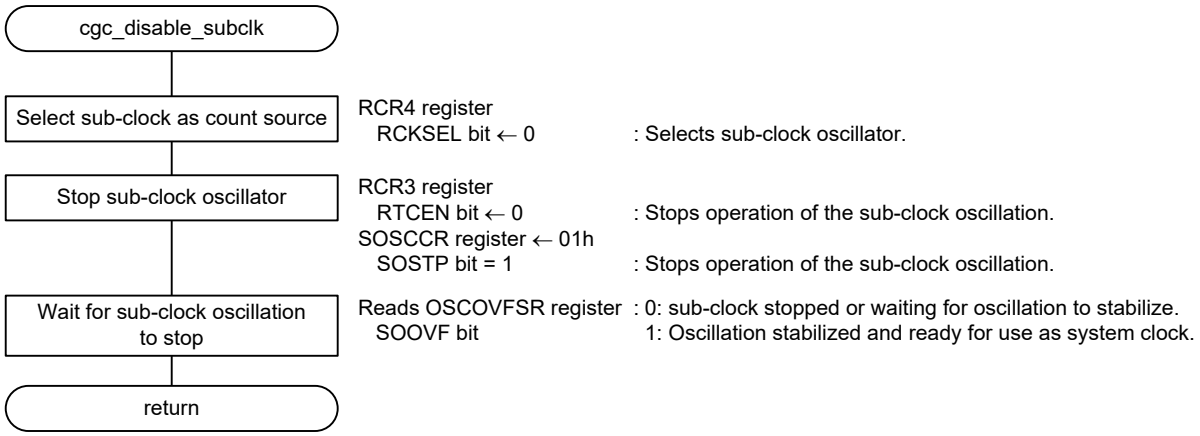
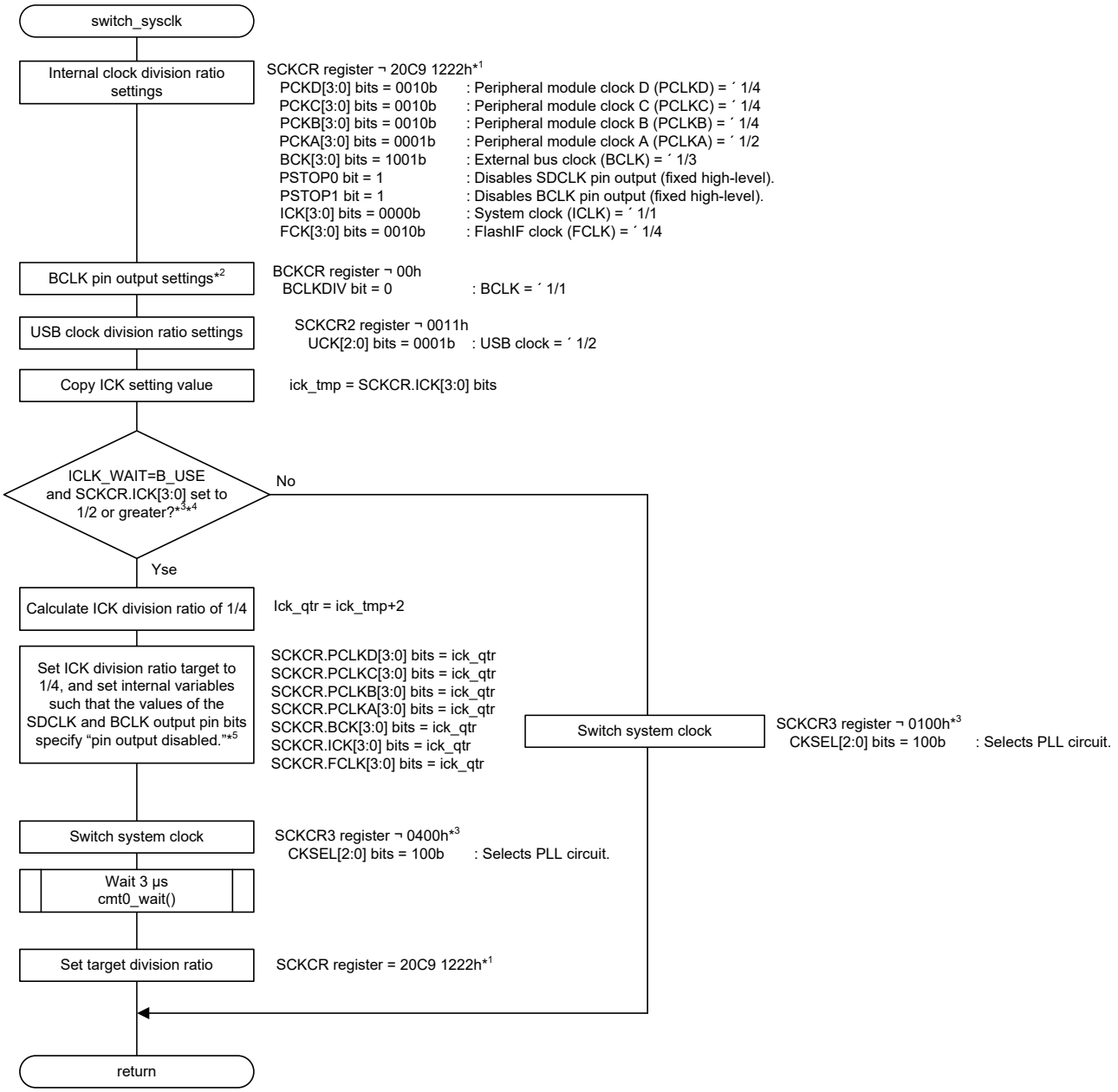


Figure 3.14 Sub-clock Disable

3.10.13 System Clock Switching

Figure 3.15 is a flowchart of the processing for switching the system clock.



Notes: 1. The value is set by the system clock, which is selected by a constant.

2. The maximum operating frequency of the output pin depends on the number of pins in the package.

3. Change the setting of the constant to match the characteristics of your system.

4. If the ICK division ratio is 1/4 or less, only the system clock is switched with the initial division ratio setting remaining unchanged.

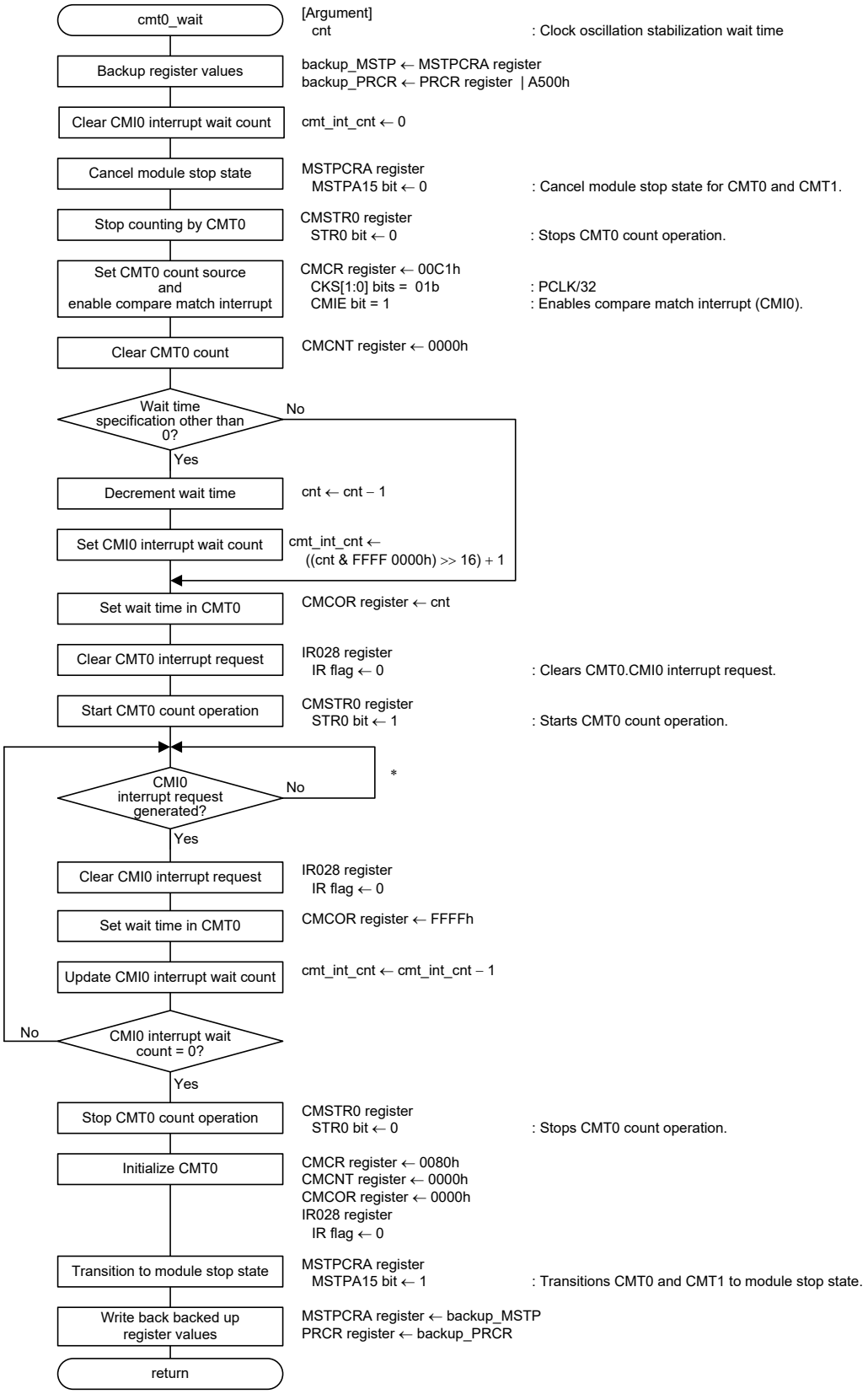
5. The relationship between the frequency of the system clock (ICLK) and the frequencies of the peripheral module clocks must be as follows:

ICLK:FCLK = N:1 or 1:N, ICLK:PCLKA = N:1 or 1:N, ICLK:PCLKB = N:1 or 1:N,
ICLK:PCLKC = N:1 or 1:N, ICLK:PCLKD = N:1 or 1:N, ICLK:BCLK = N:1

Figure 3.15 System Clock Switching

3.10.14 Software Wait Cycles Using CMT0

Figure 3.16 is a flowchart of the processing for implementing a software wait using CMT0.



Note: 1.When the watchdog timer (WDT) and independent watchdog timer (IWDT) are counting, use processing loop to refresh the WDT and IWDT.

Figure 3.16 Software Wait Cycles Using CMT0

3.10.15 A/D Sequential Conversion Time Settings

Figure 3.17 is a flowchart of the processing for making settings related to the time for A/D conversion by successive approximation.

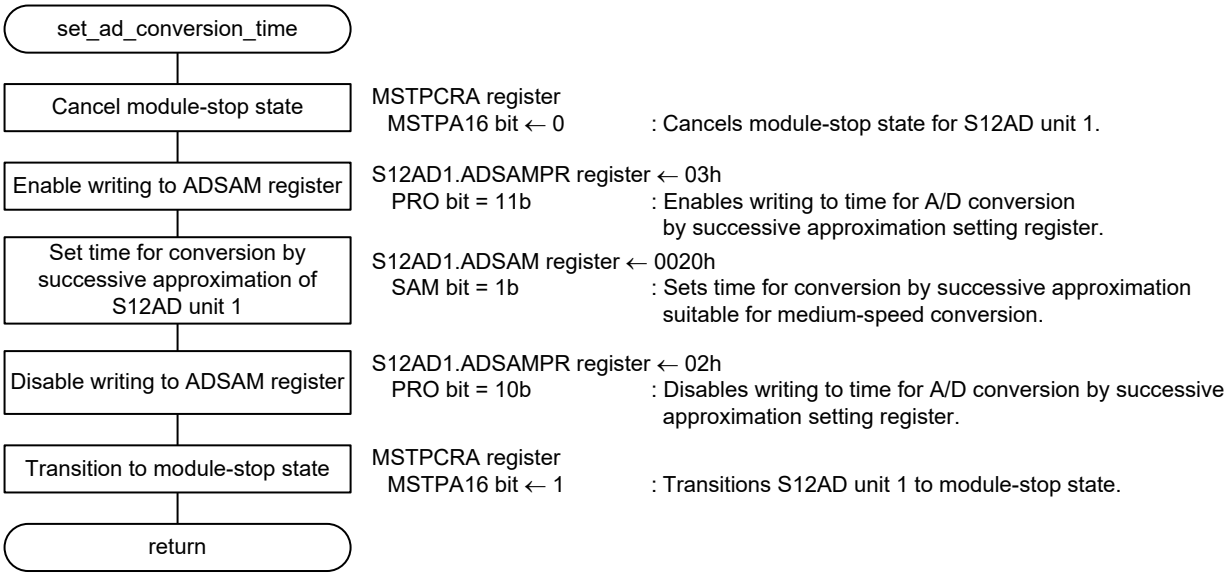
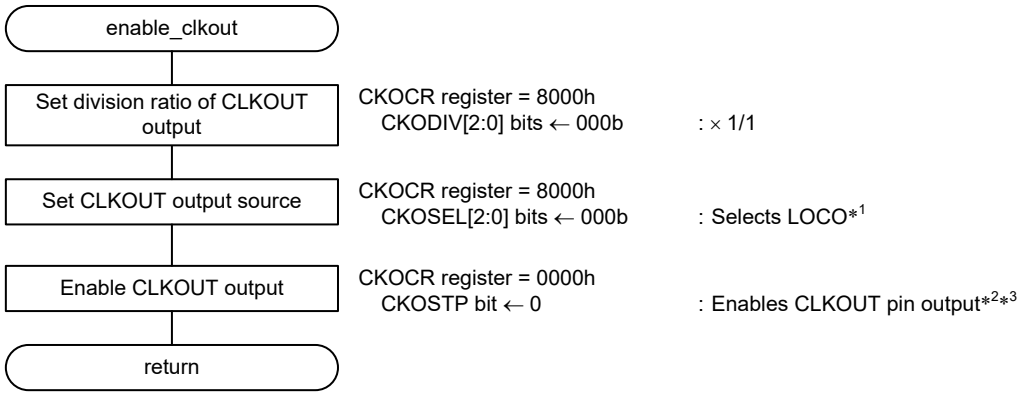


Figure 3.17 Time for A/D Conversion by Successive Approximation Settings

3.10.16 CLKOUT Oscillation Settings

Figure 3.18 is a flowchart of the processing for making CLKOUT oscillation settings.



Notes: 1. The initial settings example only makes operation settings. To actually output this clock, it is necessary to also make settings to the pin function control register and port mode register of the corresponding pin. Refer to section 22, I/O Ports, and section 23, Multi-Function Pin Controller (MPC), in RX72N Group User's Manual: Hardware, and make settings appropriate for your system.

2. Overwriting CKOSTP while the clock is oscillating may cause glitches in the output.

Figure 3.18 CLKOUT Oscillation Settings

4. Importing a Project

After importing the sample project, make sure to confirm build and debugger setting.

4.1 Importing a Project into e² studio

Follow the steps below to import your project into e² studio. Pictures may be different depending on the version of e² studio to be used.

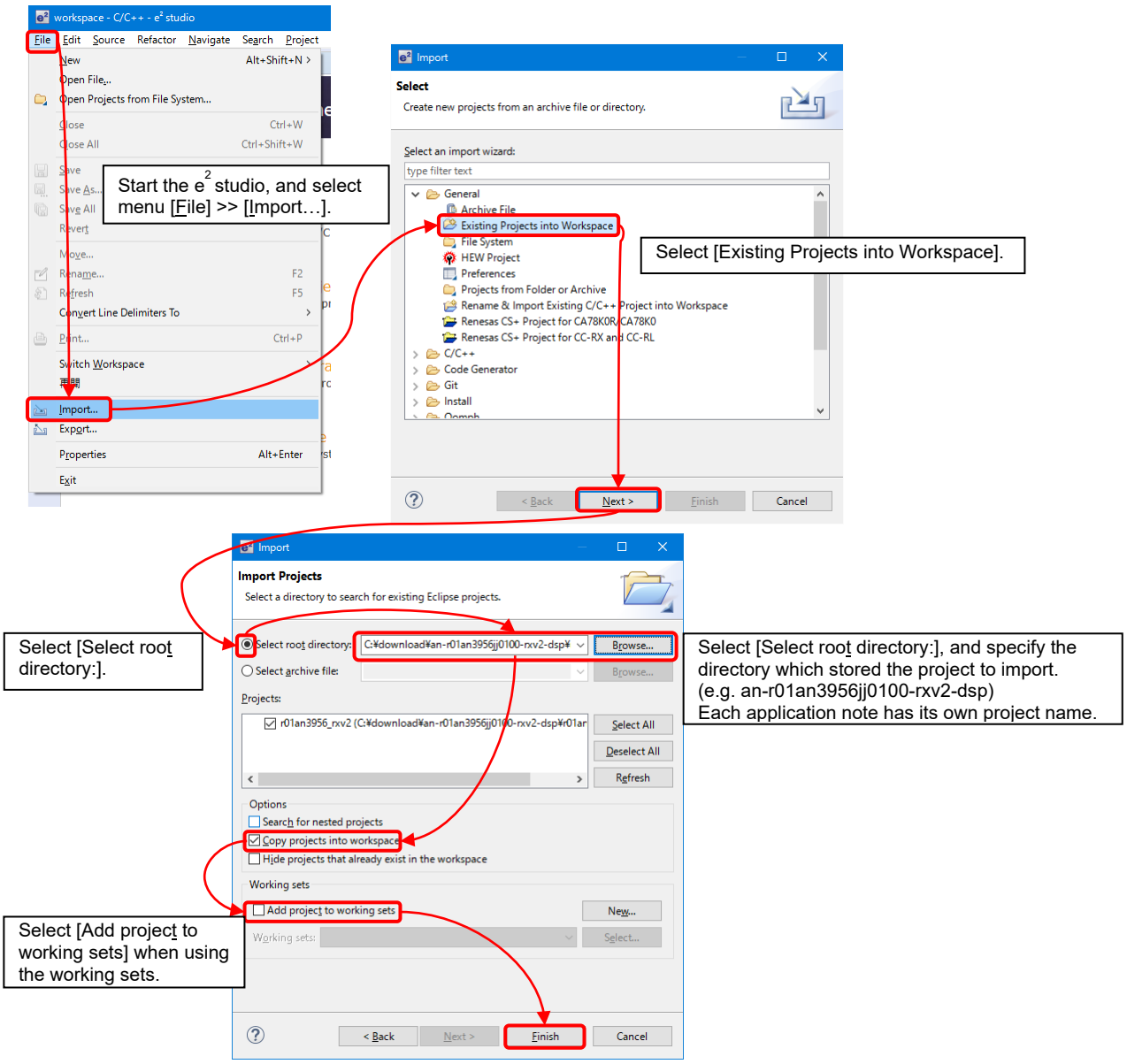


Figure 4.1 Importing a Project into e² studio

4.2 Importing a Project into CS+

Follow the steps below to import your project into CS+. Pictures may be different depending on the version of CS+ to be used.

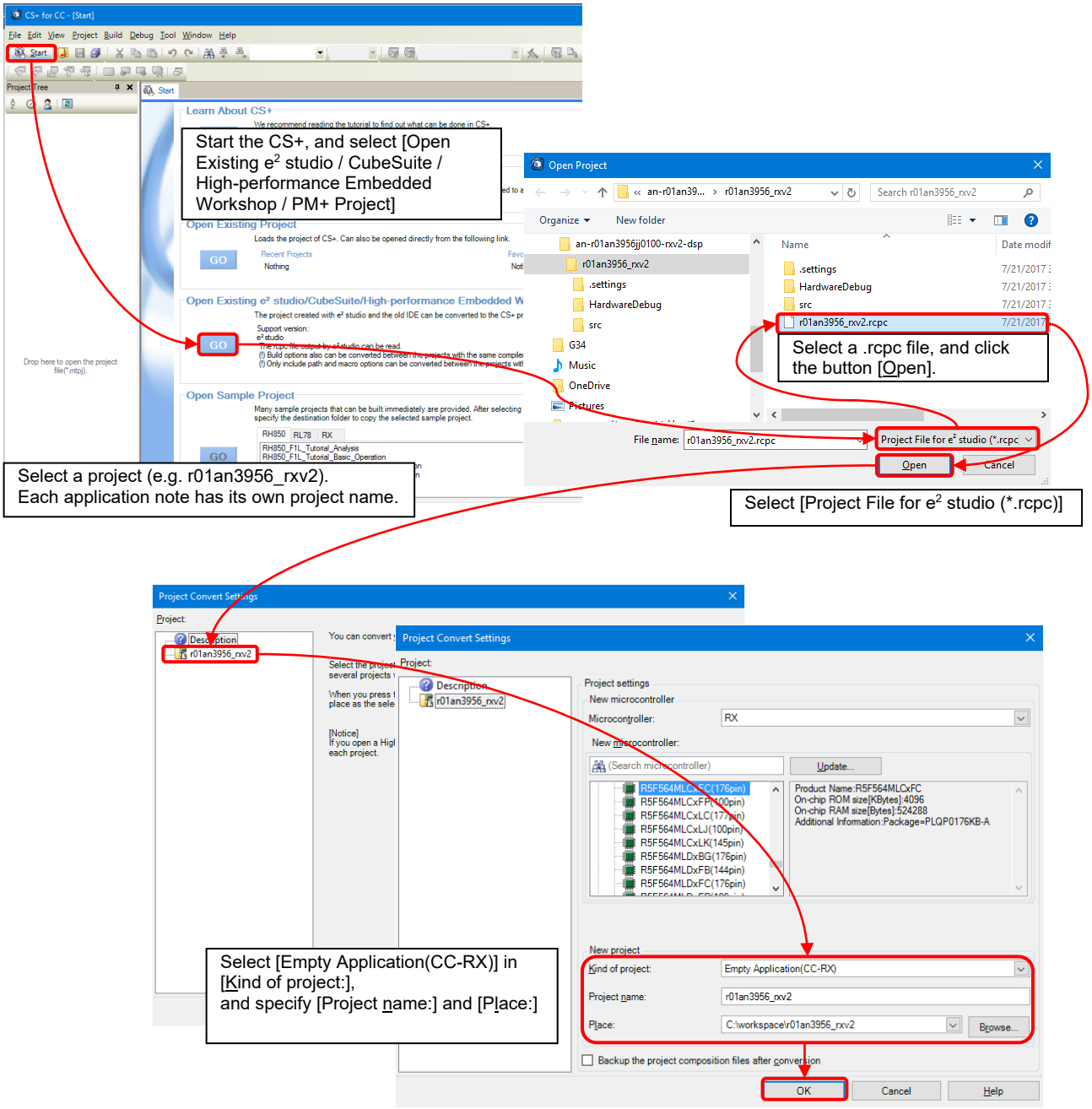


Figure 4.2 Importing a Project into CS+

5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

6. Reference Documents

User's Manual: Hardware
RX72N Group User's Manual: Hardware (R01UH0824EJ)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News
(The latest version can be downloaded from the Renesas Electronics website.)

User's Manual: Development Tools
RX Family CC-RX Compiler User's Manual (R20UT3248EJ)
(The latest version can be downloaded from the Renesas Electronics website.)

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jan. 31. 20	—	First edition issued.
1.01	Feb. 1. 21	8	Table 2.1 Integrated development environment, C compiler, iodefine.h and Sample code version, changed.
		42	Figure 3.13 Subclock Oscillation Enable (2/2), changed.
		49	Fixed the format of the date of Revision History.
		program	Technical update TN-RX*-A236B/E, supported.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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