RX63N Group, RX64M Group

Points of Difference Between RX63N Group and RX64M Group

R01AN1959EJ0101
Rev.1.01
Oct 26, 2015

Introduction

This application note is intended as a reference for confirming the points of difference between the I/O registers of the RX63N Group and RX64M Group.

Target Devices

- RX64M Group 177- and 176-pin versions, ROM capacity: 2 MB to 4 MB
- RX64M Group 145- and 144-pin versions, ROM capacity: 2 MB to 4 MB
- RX64M Group 100-pin version, ROM capacity: 2 MB to 4 MB

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Comparison of Functions of RX63N Group and RX64M Group

A comparison of the functions of the RX63N Group and RX64M Group is provided below. For details of the functions, see 2., Comparative Overview of Functions, and 3., Reference Documents.

Table 1.1 is a comparative listing of the functions of the RX63N and RX64M.

Table 1.1 Comparison of Functions of RX63N and RX64M

Function	RX63N	RX64M
Operating mode	△	△
Option-setting memory	△	△
Voltage detection circuit (LVDA)	△	△
Clock generation circuit	△	△
Frequency measurement circuit (MCK)	○	×
Clock frequency accuracy measurement circuit (CAC)	×	○
Low power consumption function	△	△
Battery backup function	○	○
Register write protection function	○	○
Interrupt controller (ICUb): RX63N, (ICUA): RX64M	△	△
Buses	○	○
Memory-protection unit (MPU)	△	△
DMA controller (DMACA): RX63N, (DMACAa): RX64M	△	△
EXDMA controller (EXDMACa):	○	○
Data transfer controller (DTCa)	○	○
Event link controller (ELC)	×	○
I/O port	△	△
Multi-function pin controller (MPC)	△	△
Multi-function timer pulse unit 2 (MTU2a): RX63N Multi-function timer pulse unit 3 (MTU3a): RX64M	△	△
Port output enable 2 (POE2a): RX63N Port output enable 3 (POE3a): RX64M	△	△
General PWM timer (GPTa)	×	○
16-bit timer pulse unit (TPUa)	○	○
Programmable pulse generator (PPG)	○	○
8-bit timer (TMR)	△	△
Compare match timer (CMT)	△	△
Compare match timer W (CMTW)	×	○
Realtime clock (RTCa): RX63N, (RTCd): RX64M	△	△
Watchdog timer (WDTA)	○	○
Independent watchdog timer (IWDTa)	○	○
Ethernet controller (ETHERC)	○	○
PTP module for the Ethernet controller (EPTPC)	×	○
Ethernet controller direct memory access controller (EDMAC): RX63N Ethernet controller direct memory access controller (EDMACa): RX64M	△	△
USB 2.0 Host/Function module (USBa): RX63N USB 2.0 FS Host/Function module (USBb): RX64M	△	△
USB 2.0 Full Speed Host/Function module (USBA)	×	○
Serial communications interface (SCIc, SCId): RX63N Serial communications interface (SCIg, SCIh): RX64M	△	△
FIFO embedded serial communications interface (SCIFA)	×	○
I²C bus interface (RIIC): RX63N, (RIICa): RX64M	△	△

Function	RX63N	RX64M
CAN module (CAN)	○	○
Serial peripheral interface (RSPI): RX63N, (RSPIa): RX64M	△	△
Quad serial peripheral interface (QSPI)	×	○
IEbus controller (IEB)	○	×
CRC calculator (CRC)	○	○
Serial sound interface (SSI)	×	○
Sampling rate converter (SRC)	×	○
SD host interface (SDHI)	×	○
Multimedia card interface (MMCIF)	×	○
Parallel data capture unit (PDC)	△	△
Boundary scan	○	○
AES	×	○
DES	×	○
SHA	×	○
RNG	×	○
12-bit A/D converter (S12ADa): RX63N, (S12ADC): RX64M	△	△
10-bit A/D converter (ADb)	○	×
D/A converter (DAa): RX63N 12-bit D/A converter (R12DA): RX64M	△	△
Temperature sensor	△	△
Data operation circuit (DOC)	×	○
RAM	△	△
Standby RAM	×	○
Flash memory	△	△

Note: ○: Function implemented, ×: Function not implemented, △: Differences exist between implementation of function on RX63N and RX4M.

2. Comparative Overview of Functions

2.1 Operating Modes

Table 2.1 shows a comparative listing of the operating mode registers.

Table 2.1 Comparative Listing of Operating Mode Registers

Register	Bit	RX63N	RX64M
SYSCR1	ECCRAME	—	ECCRAM enable bit
	SBYRAME	—	Standby RAM enable bit

2.2 Option-Setting Memory

Table 2.2 shows a comparative listing of the option-setting memory registers.

Table 2.2 Comparative Listing of Option-Setting Memory Registers

Register	Bit	RX63N	RX64M
SPCC	—	—	Serial command control register
OSIS	—	—	OCD/serial program ID setting register
OFS1	VDSEL[1:0]	—	Voltage detection 0 level select bits
MDEB	—	Endian select register B	—
MDES	—	Endian select register S	—
MDE	—	—	Endian select register
TMEF	—	—	TM enable flag register
TMINF	—	—	TM identification data register

2.3 Voltage Detection Circuit

Table 2.3 shows a comparative listing of the voltage detection circuit specifications, and Table 2.4 shows a comparative listing of the voltage detection circuit registers.

Table 2.3 Comparative Listing of Voltage Detection Circuit Specifications

		RX63N (LVDA)			RX64M (LVDA)		
Item		**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
VCC monitoring	Monitored voltage	Vdet0	Vdet1	Vdet2	Vdet0	Vdet1	Vdet2
	Detection target	Voltage falls lower than Vdet0.	Voltage rises or falls past Vdet1.	Voltage rises or falls past Vdet2.	Voltage falls lower than Vdet0.	Voltage rises or falls past Vdet1.	Voltage rises or falls past Vdet2.
	Detection voltage	One level fixed	Specify voltage using LVDLVLR.LVD1LVL[3:0] bits	Specify voltage using LVDLVLR.LVD2LVL[3:0] bits	Selectable from three levels using OFS1.VDSEL[1:0] bits.	Selectable from three levels using LVDLVLR.LVD1LVL[3:0] bits.	Selectable from three levels using LVDLVLR.LVD2LVL[3:0] bits.
	Monitor flag	—	LVD1SR.LVD1MON flag: Monitors if higher or lower than Vdet1.	LVD2SR.LVD2MON flag: Monitors if higher or lower than Vdet2.	—	LVD1SR.LVD1MON flag: Monitors if higher or lower than Vdet1.	LVD2SR.LVD2MON flag: Monitors if higher or lower than Vdet2.
			LVD1SR.LVD1DET flag: Detects rise or fall past Vdet1.	LVD2SR.LVD2DET flag: Detects rise or fall past Vdet2.		LVD1SR.LVD1DET flag: Detects rise or fall past Vdet1.	LVD2SR.LVD2DET flag: Detects rise or fall past Vdet2.
Voltage detection processing	Reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset
		Reset when Vdet0 > VCC: CPU operation restarts a fixed period of time after VCC > Vdet0.	Reset when Vdet1 > VCC: Selectable between CPU operation restarts a fixed period of time after VCC > Vdet1 and CPU operation restarts a fixed period of time after Vdet1 > VCC.	Reset when Vdet2 > VCC: Selectable between CPU operation restarts a fixed period of time after VCC > Vdet2 and CPU operation restarts a fixed period of time after Vdet2 > VCC.	Reset when Vdet0 > VCC: CPU operation restarts a fixed period of time after VCC > Vdet0.	Reset when Vdet1 > VCC: Selectable between CPU operation restarts a fixed period of time after VCC > Vdet1 and CPU operation restarts a fixed period of time after Vdet1 > VCC.	Reset when Vdet2 > VCC: Selectable between CPU operation restarts a fixed period of time after VCC > Vdet2 and CPU operation restarts a fixed period of time after Vdet2 > VCC.
	Interrupt	—	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt	—	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt
			Non-maskable interrupt	Non-maskable interrupt		Selectable between non-maskable interrupt and interrupt.	Selectable between non-maskable interrupt and interrupt.
			Interrupt request generated both when Vdet1 > VCC and when VCC > Vdet1, or one or the other.	Interrupt request generated both when Vdet2 > VCC and when VCC > Vdet2, or one or the other.		Interrupt request generated both when Vdet1 > VCC and when VCC > Vdet1, or one or the other.	Interrupt request generated both when Vdet2 > VCC and when VCC > Vdet2, or one or the other.

Item		RX63N (LVDA) Voltage Monitoring 0	RX63N (LVDA) Voltage Monitoring 1	RX63N (LVDA) Voltage Monitoring 2	RX64M (LVDA) Voltage Monitoring 0	RX64M (LVDA) Voltage Monitoring 1	RX64M (LVDA) Voltage Monitoring 2
Digital filter	Enable/ disable switching	—	Available	Available	—	Available	Available
	Sampling time	—	1/n LOCO frequency × 2 (n: 1, 2, 4, 8)	1/n LOCO frequency × 2 (n: 1, 2, 4, 8)	—	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)
Event link function		—	—	—	—	Available: Vdet pass-through detection event output	Available: Vdet pass-through detection event output

Table 2.4 Comparative Listing of Voltage Detection Circuit Registers

Register	Bit	RX63N (LVDA)	RX64M (LVDA)
LVD1CR1	LVD1IRQSEL	—	Voltage monitoring 1 interrupt type select bit
LVD2CR1	LVD2IRQSEL	—	Voltage monitoring 2 interrupt type select bit

2.4 Clock Generation Circuit

Table 2.5 shows a comparative listing of the clock generation circuit specifications, and Table 2.6 shows a comparative listing of the clock generation circuit registers.

Table 2.5 Comparative Listing of Clock Generation Circuit Specifications

Item	RX63N	RX64M
Uses	• Generates the system clock (ICLK) supplied to the CPU, DMAC, DTC, code flash memory, and RAM. • Generates the peripheral module clocks (PCLK) supplied to the ETHERC, EDMAC, and DEU. • Generates the peripheral module clocks (PCLKB) supplied to the peripheral module clocks. • Generates the FlashIF clock (FCLK) supplied to the FlashIF. • Generates the external bus clock (BCLK) supplied to the external bus. • Generates the SDRAM clock (SDCLK) supplied to the SDRAM. • Generates the USB clock (UCLK) supplied to the USB. • Generates the CAN clock (CANMCLK) supplied to the CAN. • Generates the IEBUS clock (IECLK) supplied to the IEBUS. • Generates the RTC-dedicated sub clock (RTCSCLK) supplied to the RTC. • Generates the RTC-dedicated main clock (RTCMCLK) supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) supplied to the IWDT. • Generates the JTAG clock (JTAGTCK) supplied to the JTAG.	• Generates the system clock (ICLK) supplied to the CPU, DMAC, DTC, code flash memory, and RAM. • Generates the peripheral module clocks (PCLK) supplied to the ETHERC, EDMAC, EPTPC, USBHS, RSPI, SCIF, MTU3, GPTA, and AES. • Generates the peripheral module clocks (PCLKB) supplied to the peripheral module clocks. • Generates the peripheral module (analog conversion) clocks (PCLKC: unit 0, PCLKD: unit 1) to be supplied to the S12ADC. • Generates the FlashIF clock (FCLK) supplied to the FlashIF. • Generates the external bus clock (BCLK) supplied to the external bus. • Generates the SDRAM clock (SDCLK) supplied to the SDRAM. • Generates the USB clock (UCLK) supplied to the PHY in the USB0 and USBA. • Generates the USBHS clock (USBMCLK) supplied to the PHY in the USBA. • Generates the CAC clock (CACCLK) supplied to the CAC. • Generates the CAN clock (CANMCLK) supplied to the CAN. • Generates the RTC sub clock (RTCSCLK) supplied to the RTC. • Generates the RTC main clock (RTCMCLK) supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) supplied to the IWDT. • Generates the JTAG clock (JTAGTCK) supplied to the JTAG.

Item	RX63N	RX64M
Operating frequencies	• ICLK: 100 MHz (max.) • PCLKA: 100 MHz (max.) • PCLKB: 50 MHz (max.) • FCLK: 4 MHz to 50 MHz (for programming and erasing the ROM and E2 data flash) 50 MHz (max.) (for reading from the E2 data flash) • BCLK: 100 MHz (max.) • BCLK pin output: 50 MHz (max.) • SDCLK pin output: 50 MHz (max.) • UCLK: 48 MHz (max.) • CANMCLK: 20 MHz (max.) • IECLK: 50 MHz (max.) • RTCSCLK: 32.768 kHz • RTCMCLK: 4 MHz to 16 MHz • IWDTCLK: 125 kHz • JTAGTCK: 10 MHz (max.)	• ICLK: 120 MHz (max.) • PCLKA: 120 MHz (max.) • PCLKB: 60 MHz (max.) • PCLKC: 60 MHz (max.) • PCLKD: 60 MHz (max.) • FCLK: 4 MHz to 60 MHz (for programming and erasing the code flash memory and data flash memory) 60 MHz (max.) (for reading from the data flash) • BCLK: 120 MHz (max.) • BCLK pin output: 60 MHz (max.) • SDCLK pin output: 60 MHz (max.) • UCLK: 48 MHz (max.) • USBMCLK: 20 MHz, 24 MHz • CACCLK: Same frequency as each oscillator • CANMCLK: 24 MHz (max.) • RTCSCLK: 32.768 kHz • RTCMCLK: 8 MHz to 16 MHz • IWDTCLK: 120 kHz • JTAGTCK: 10 MHz (max.)
Main clock oscillator	• Resonator frequency: 4 MHz to 16 MHz • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: Ceramic resonator, crystal resonator • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When oscillation stop of the main clock is detected, the system clock source is switched to LOCO, and MTU output can be forcedly driven to high-impedance.	• Resonator frequency: 8 MHz to 24 MHz • External clock input frequency: 24 MHz (max.) • Connectable resonator or additional circuit: Ceramic resonator, crystal resonator • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When oscillation stop of the main clock is detected, the system clock source is switched to LOCO, MTU, and GPT output can be forcedly driven to high-impedance.
Sub-clock oscillator	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal resonator • Connection pins: XCIN, XCOUT	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal resonator • Connection pins: XCIN, XCOUT
PLL	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz to 16 MHz • Frequency multiplication ratio: Selectable within range from 8, 10, 12, 16, 20, 24, 25, 50 • VCO oscillation frequency: 104 MHz to 200 MHz	• Input clock source: Main clock, HOCO • Input pulse frequency division ratio: Selectable from 1, 2, and 3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication ratio: Selectable within range from 10 to 30 • PLL frequency synthesizer output clock frequency: 120 MHz to 240 MHz
High-speed on-chip oscillator (HOCO)	• Oscillation frequency: 50 MHz • HOCO power supply control	• Oscillation frequency: Selectable from 16 MHz, 18 MHz, and 20 MHz • HOCO power supply control

Item	RX63N	RX64M
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 125 kHz	Oscillation frequency: 240 kHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 125 kHz	Oscillation frequency: 120 kHz
External clock input (TCK) for JTAG	Input clock frequency: 10 MHz (max.)	Input clock frequency: 10 MHz (max.)
Control of output on BCLK pin	• BCLK clock output or high output is selectable • BCLK or BCLK/2 is selectable as the output clock	• BCLK clock output or high output is selectable • BCLK or BCLK/2 is selectable as the output clock
Control of output on SDCLK pin	SDCLK clock output or high output is selectable	SDCLK clock output or high output is selectable
Event link function (output)	—	Main clock oscillator oscillation stop detection
Event link function (input)	—	Switching of clock source to low-speed on-chip oscillator

Table 2.6 Comparative Listing of Clock Generation Circuit Registers

Register	Bit	RX63N	RX64M
SCKCR	PCKD	—	Peripheral module clock D (PCLKD) select bit
	PCKC	—	Peripheral module clock C (PCLKC) select bit
SCKCR2	IEBCK	IEBUS clock (IECLK) select bit	—
PLLCR	PLLSRCSEL	—	PLL clock source select bit
HOCOCR2	—	—	High-speed on-chip oscillator control register 2
OSCOVFSR	—	—	Oscillation stabilization flag register
MOSCWTCR*	MSTS	Bits 0 to 4: Main clock oscillator wait time select bits	Bits 0 to 7: Main clock oscillator wait time select bits
SOSCWTCR*	SSTS	Bits 0 to 4: Sub-clock oscillator wait time select bits	Bits 0 to 7: Sub-clock oscillator wait time select bits
MOFCR	MODRV2 [1:0]	—	Main clock oscillator drive capability 2 switch bits
	MOSEL	—	Main clock oscillator switch bit

Note: * In the User's Manual: Hardware of the RX63N Group, MOSCWTCR and SOSCWTCR are described in section 11, Low Power Consumption.

2.5 Low Power Consumption Functions

Table 2.7 shows a comparative listing of the low power consumption, and Table 2.8 shows a comparative listing of the low power consumption function registers.

Table 2.7 Comparative Listing of Low Power Consumption Functions

Item	RX63N	RX64M
Reduction of power consumption by clock switching	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clock (ICLKA and PCLKB), external bus clock (BCLK), and Flash interface clock (FCLK).	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clock (ICLKA, PCLKB, PCLKC, and PCLKD), external bus clock (BCLK), and Flash interface clock (FCLK).
BCLK output control function	BCLK output or high-level output can be selected.	BCLK output or high-level output can be selected.
SDCLK output control function	SDCLK output or high-level output can be selected.	SDCLK output or high-level output can be selected.
Module stop function	Each peripheral module can be stopped independently.	Each peripheral module can be stopped independently.
Function for transition to low power consumption mode	It is possible to transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped.	It is possible to transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped.
Low power consumption modes	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode
Operating power reduction function	• Power consumption can be reduced in normal operation, sleep mode, and all-module clock stop mode by selecting an appropriate operating power consumption control mode according to the operating frequency and operating voltage. • Operating power control modes: 3 — High-speed operating mode — Low-speed operating mode 1 — Low-speed operating mode 2	• Power consumption can be reduced in normal operation, sleep mode, and all-module clock stop mode by selecting an appropriate operating power consumption control mode according to the operating frequency and operating voltage. • Operating power control modes: 3 — High-speed operating mode — Low-speed operating mode 1 — Low-speed operating mode 2

Table 2.8 Comparative Listing of Low Power Consumption Function Registers

Register	Bit	RX63N	RX64M
MSTPCRA	MSTPA0	—	Compare match timer W (unit 1) module stop bit
	MSTPA1	—	Compare match timer W (unit 0) module stop bit
	MSTPA7	—	General PWM timer
	MSTPA12	16-bit timer pulse unit 1 (unit 1) module stop bit	—
	MSTPA16	—	12-bit A/D converter (unit 1) module stop bit
	MSTPA23	10-bit A/D converter module stop bit	—
MSTPCRB	MSTPB6	—	Data operation circuit module stop bit
	MSTPB9	—	Event link controller module stop bit
	MSTPB12	—	Universal serial bus 2.0 FS interface module stop bit
	MSTPB14	—	Ethernet controller, Ethernet controller direct memory access controller (channel 1) module stop bit
	MSTPB16	Serial peripheral interface 1 module stop bit	—
	MSTPB18	Universal serial bus interface (port 1) module stop bit	—
	MSTPB20	I^2C bus interface 1 module stop bit	—
	MSTPC1	RAM1 module stop bit	—
MSTPCRC	MSTPC6	—	ECCRAM module stop bit
	MSTPC7	—	Standby RAM module stop bit
	MSTPC16	I^2C bus interface 3 module stop bit	—
	MSTPC18	IEBUS module stop bit	—
	MSTPC22	Serial peripheral interface 2 module stop bit	—
	MSTPC23	—	Quad serial parallel interface module stop bit
	MSTPC24	Serial communication interface 11 module stop bit	FIFO embedded communication interface 11 module stop bit
	MSTPC25	Serial communication interface 10 module stop bit	FIFO embedded communication interface 10 module stop bit
	MSTPC26	Serial communication interface 9 module stop bit	FIFO embedded communication interface 9 module stop bit
	MSTPC27	Serial communication interface 8 module stop bit	FIFO embedded communication interface 8 module stop bit
MSTPCRD	MSTPD0	—	Module stop D0 setting bit
	MSTPD1	—	Module stop D1 setting bit
	MSTPD2	—	Module stop D2 setting bit
	MSTPD3	—	Module stop D3 setting bit
	MSTPD4	—	Module stop D4 setting bit
	MSTPD5	—	Module stop D5 setting bit
	MSTPD6	—	Module stop D6 setting bit
	MSTPD7	—	Module stop D7 setting bit

Register	Bit	RX63N	RX64M
MSTPCRD	MSTPD14	—	Serial sound interface 1 module stop bit
	MSTPD15	—	Serial sound interface 0 module stop bit
	MSTPD19	—	SD host interface module stop bit
	MSTPD21	—	MMC host interface module stop bit
	MSTPD23	—	Sampling rate converter module stop bit
	MSTPD31	Data encryption unit (DEU) module stop bit	—
MOSCWTCR*	—	Bits 0 to 4: Main clock oscillator wait time select bits	Bits 0 to 7: Main clock oscillator wait time select bits
SOSCWTCR*	—	Bits 0 to 4: Main clock oscillator wait time select bits	Bits 0 to 7: Main clock oscillator wait time select bits
PLLWTCR		PLL wait control register	—

Note: * See the Clock Generation Circuit section of RX64M Group User's Manual: Hardware for a description of MOSCWTCR and SOSCWTCR.

2.6 Interrupt Controller

Table 2.9 shows a comparative listing of the interrupt controller specifications, and Table 2.10 shows a comparative listing of the interrupt controller registers.

Table 2.9 Comparative Listing of Interrupt Controller Specifications

Item		RX63N (ICUb)	RX64M (ICUA)
Interrupt	Peripheral function interrupts	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection (detection method is fixed for each interrupt source) • Interrupt grouping: Multiple interrupt sources can be grouped together and treated as a single interrupt source. — Number of groups for edge detection interrupts: 7 (groups 0 to 6) — Number of groups for edge detection interrupts: 1 (group 12)	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection (detection method is fixed for each interrupt source) • Interrupt grouping: Multiple interrupt sources can be grouped together and treated as a single interrupt source. — Group BE0 interrupt: Peripheral module interrupt source using PCLKB as operation clock (edge detection) — Group BL0 and BL1 interrupts: Peripheral module interrupt sources using PCLKB as operation clock (level detection) — Group AL0 and AL1 interrupts: Peripheral module interrupt sources using PCLKA as operation clock (level detection) • Selectable interrupt B: For each interrupt vector number from 128 to 207, one peripheral module interrupt source using PCLKB as operation clock may be assigned. • Selectable interrupt A: For each interrupt vector number from 208 to 255, one peripheral module interrupt source using PCLKA as operation clock may be assigned.
		• Interrupt unit selection: One of two interrupt requests can be selected as the interrupt request source. Number of units: 6	

Item		RX63N (ICUb)	RX64M (ICUA)
Interrupt	External pin interrupts	• Interrupts from signals input to IRQi pins (i = 0 to 15) • Interrupt detection: Low level, falling edge, rising edge, and rising and falling edges. One of these detection methods can be set for each source. • Digital filter may be used to suppress noise.	• Interrupts from signals input to IRQi pins (i = 0 to 15) • Interrupt detection: Low level, falling edge, rising edge, and rising and falling edges. One of these detection methods can be set for each source. • Digital filter may be used to suppress noise.
	Software interrupt	• Interrupts can be generated by writing to a register. • Interrupt sources: 1	• Interrupts can be generated by writing to a register. • Interrupt sources: 2
	Interrupt priority level	Specified in interrupt source priority register (IPR)	Specified in interrupt source priority register (IPR)
	Fast interrupt function	Shorter CPU response time can be specified for a single interrupt source.	Shorter CPU response time can be specified for a single interrupt source.
	DTC and DMAC control	The DTC and DMAC can be activated by interrupt sources.	The DTC and DMAC can be activated by interrupt sources.
	EXDMAC control	—	• EXDMAC0 can be activated by the interrupt specified in selectable interrupt B selection register 144 or selectable interrupt A selection register 208. • EXDMAC1 can be activated by the interrupt specified in selectable interrupt B selection register 145 or selectable interrupt A selection register 209.
Non-maskable interrupts	NMI pin interrupt	Interrupts from signals input to NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter may be used to suppress noise.	Interrupts from signals input to NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter may be used to suppress noise.
	Oscillation stop detection interrupt	Interrupt on detection of oscillation stop buy main clock oscillator	Interrupt on detection of oscillation stop buy main clock oscillator
	WDT underflow/refresh error interrupt	Interrupt on an underflow or refresh error of the watchdog timer	Interrupt on an underflow or refresh error of the watchdog timer
	IWDT underflow/refresh error interrupt	Interrupt on an underflow or refresh error of the watchdog timer	Interrupt on an underflow or refresh error of the watchdog timer
	Voltage monitoring 1 interrupt	Interrupt triggered by voltage detection circuit 1 (LVD1)	Interrupt triggered by voltage detection circuit 1 (LVD1)
	Voltage monitoring 2 interrupt	Interrupt triggered by voltage detection circuit 2 (LVD2)	Interrupt triggered by voltage detection circuit 1 (LVD2)
	RAM error	—	This interrupt occurs when an ECC error is detected in the ECCRAM.

Item		RX63N (ICUb)	RX64M (ICUA)
Return from low power consumption modes	Sleep mode	Return is initiated by any interrupt source.	Return is initiated by any interrupt source.
	All-module clock stop mode	Return is initiated by NMI pin interrupts, external pin interrupts, and peripheral function interrupts (voltage monitor 1, voltage monitor 2, oscillation stop detection, USB resume, RTC alarm, RTC period, IWDT, TMR interrupts).	Return is initiated by NMI pin interrupts, external pin interrupts, and peripheral function interrupts (voltage monitor 1, voltage monitor 2, oscillation stop detection, USB resume, RTC alarm, RTC period, IWDT, USBA resume, selectable interrupts 146 to 157).
	Software standby mode	Return is initiated by NMI pin interrupts, external pin interrupts, and peripheral function interrupts (voltage monitor 1, voltage monitor 2, USB resume, RTC alarm, RTC period, IWDT).	Return is initiated by NMI pin interrupts, external pin interrupts, and peripheral function interrupts (voltage monitor 1, voltage monitor 2, USB resume, RTC alarm, RTC period, IWDT, USBA resume).
	Deep software standby mode	Return is initiated by NMI pin interrupts, external pin interrupts, voltage monitor 1, voltage monitor 2, USB resume interrupts, RTC alarm, RTC period interrupts.	Return is initiated by NMI pin interrupts, some external pin interrupts, and peripheral function interrupts (voltage monitor 1, voltage monitor 2, USB resume, RTC alarm, RTC period, USBA resume).

Table 2.10 Comparative Listing Interrupt Controller Registers

Register	Bit	RX63N (ICUb)	RX64M (ICUA)
SWINT2R	—	—	Software interrupt 2 activation register
DMRSR4	—	—	DMAC activation request select register 4
DMRSR5	—	—	DMAC activation request select register 5
DMRSR6	—	—	DMAC activation request select register 6
DMRSR7	—	—	DMAC activation request select register 7
NMISR	ECCRAMST	—	RAM ECC error interrupt status flag
NMIER	ECCRAMEN	—	RAM ECC error interrupt enable bit
GRPm	—	Group m interrupt source register (m = 0 to 6, 12)	—
GRPBE0	—	—	Group BE0 interrupt request register
GRPBL0	—	—	Group BL0 interrupt request register
GRPBL1	—	—	Group BL1 interrupt request register
GRPAL0	—	—	Group AL0 interrupt request register
GRPAL1	—	—	Group AL1 interrupt request register
GENm	—	Group m interrupt enable register (m = 0 to 6, 12)	—
GENBE0	—	—	Group BE0 interrupt enable register
GENBL0	—	—	Group BL0 interrupt enable register
GENBL1	—	—	Group BL1 interrupt enable register
GENAL0	—	—	Group AL0 interrupt enable register
GENAL1	—	—	Group AL1 interrupt enable register
GCRm	—	Group m interrupt clear register (m = 0 to 6)	—
GCRBE0	—	—	Group BE0 interrupt clear register
SEL	—	Unit selecting register	—
PIBRk	—	—	Selectable interrupt B request register k (k = 0h to Ah)
PIARk	—	—	Selectable interrupt A request register k (k = 0h to Ah)
SLIBXRn	—	—	Selectable interrupt B select register Xn (n = 128 to 143)
SLIBRn	—	—	Selectable interrupt B select register n (n = 144 to 207)
SLIARn	—	—	Selectable interrupt A select register n (n = 208 to 255)
SELEXDR	—	—	EXDMAC activation interrupt select register
SLIPRCR	—	—	Selectable interrupt source select register write protection register

2.7 Memory Protection Unit

Table 2.11 shows a comparative listing of the memory protection unit registers.

Table 2.11 Comparative Listing of Memory Protection Unit Registers

Register	Bit	RX63N	RX64M
MPESTS	IA	Instruction memory protection error generated bit	—
	DA	Data memory protection error generated bit	—
	IMPER	—	Instruction memory protection error generated bit
	DMPER	—	Data memory protection error generated bit

2.8 DMA Controller

Table 2.12 shows a comparative overview of the DMA controller specifications, and Table 2.13 shows a comparative listing of the DMA controller registers.

Table 2.12 Comparative Overview of DMA Controller

Item		RX63N (DMACA)	RX64M (DMACAa)
Number of channels		4 (DMACm (m = 0 to 3))	8 (DMACm (m = 0 to 7))
Transfer space		512 MB (00000000h to 0FFFFFFFh and F0000000h to FFFFFFFFh, excluding reserved areas)	512 MB (00000000h to 0FFFFFFFh and F0000000h to FFFFFFFFh, excluding reserved areas)
Maximum transfer data count		1 M data units (maximum number of transfers in block transfer mode: 1,024 data units × 1,024 blocks)	64 M data units (maximum number of transfers in block transfer mode: 1,024 data units × 65,536 blocks)
DMA request sources		Activation source selectable for each channel • Software trigger • Interrupt requests from peripheral modules or trigger input to external interrupt input pins	Activation source selectable for each channel • Software trigger • Interrupt requests from peripheral modules or trigger input to external interrupt input pins
Channel priority		Channel 0 > channel 1 > channel 2 > channel 3 (channel 0: highest)	Channel 0 > channel 1 > channel 2 > channel 3 ... > channel 7 (channel 0: highest)
Transfer data	1 data unit	Bit length: 8, 16, 32 bits	Bit length: 8, 16, 32 bits
	Block size	Number of data units: 1 to 1,024 data units	Number of data units: 1 to 1,024 data units
Transfer modes	Normal transfer mode	• One data transfer per DMA transfer request • Setting in which total number of data transfers is not specified (free running mode) is available.	• One data transfer per DMA transfer request • Setting in which total number of data transfers is not specified (free running mode) is available.
	Repeat transfer mode	• One data transfer per DMA transfer request • Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination. • Maximum settable repeat size: 1,024	• One data transfer per DMA transfer request • Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination. • Maximum settable repeat size: 1,024
	Block transfer mode	• One block data transfer per DMA transfer request • Maximum settable block size: 1,024 data units	• One block data transfer per DMA transfer request • Maximum settable block size: 1,024 data units
Selective functions	Extended repeat area function	• Function in which data can be transferred by repeating the address values in the specified range with the upper bit values in the transfer address register fixed • Area of 2 bytes to 128 MB separately settable as extended repeat area for transfer source or destination	• Function in which data can be transferred by repeating the address values in the specified range with the upper bit values in the transfer address register fixed • Area of 2 bytes to 128 MB separately settable as extended repeat area for transfer source or destination

Item		RX63N (DMACA)	RX64M (DMACAa)
Interrupt request	Transfer end interrupt	Generated when transfer of the data count set in the transfer counter is completed.	Generated when transfer of the data count set in the transfer counter is completed.
	Transfer escape end interrupt	Generated when the repeat size of data transfer is completed or the extended repeat area overflows.	Generated when the repeat size of data transfer is completed or the extended repeat area overflows.
Event link activation		—	Event link request generated after one data transfer (or after one block transfer in case of block transfer operation).
Low power consumption function		It is possible to specify the module stop state.	It is possible to specify the module stop state.

Table 2.13 Comparative Listing of DMA Controller Registers

Register	Bit	RX63N (DMACA)	RX64M (DMACAa)
DMIST		—	DMAC74 interrupt status monitor register

2.9 I/O Ports

Table 2.14 shows a comparative listing of the I/O port registers.

Table 2.14 Comparative Listing of I/O Port Registers

Register	Bit	RX63N	RX64M
PSRA	—	Port switching register A	—
PSRB	—	Port switching register B	—

2.10 Multi-Function Pin Controller

Table 2.15 shows a comparative listing of the multi-function pin controller port registers.

Table 2.15 Comparative Listing of Multi-Function Pin Controller Registers

Register	Bit	RX63N	RX64M
PFBCR0	ADRHMS2	—	A18 to A20 output enable bit
	BCLKO	—	BCLK forced output bit
	ALES	—	ALE select bit
PFENET	PHYMODE	Ethernet mode setting bit	—
	PHYMODE0	—	Ethernet channel 0 setting bit
	PHYMODE1	—	Ethernet channel 1 setting bit
PFUSB0	—	USB0 control register	—
PFUSB1	—	USB1 control register	—

2.11 Multi-Function Timer Pulse Unit

Table 2.16 shows a comparative overview of multi-function timer pulse unit specifications, and Table 2.17 shows a comparative listing of the multi-function timer pulse unit registers.

Table 2.16 Comparative Overview of Multi-Function Timer Pulse Unit

Item	RX63N (MTU2a)	RX64M (MTU3a)
Pulse input/output	Maximum 16	Maximum 28
Pulse input	3	3
Count clocks	7 and 8 clocks for each channel (4 clocks for MTU5)	11 clocks for each channel (14 clocks for MTU0, 12 clocks for MTU1 and MTU2, and 10 clocks for MTU5
Operating frequency	Up to 50 MHz	Up to 120 MHz
Available operations	[MTU0 to MTU4] • Waveform output on compare match • Input capture function (noise filter setting available) • Counter-clearing operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing on compare match or input capture • Simultaneous input and output to registers in synchronization with counter operations • Up to 12-phase PWM output in combination with synchronous operation	[MTU0 to MTU4, MTU6, MTU7, and MTU8] • Waveform output on compare match • Input capture function (noise filter setting available) • Counter-clearing operation • Simultaneous writing to multiple timer counters (TCNT) (excluding MTU8) • Simultaneous clearing on compare match or input capture (excluding MTU8) • Simultaneous input and output to registers in synchronization with counter operations (excluding MTU8) • Up to 12-phase PWM output in combination with synchronous operation (excluding MTU8)
	[MTU0, MTU3 and MTU4] • Buffer operation specifiable • AC synchronous motor (brushless DC motor) drive mode using complementary PWM output or reset-synchronized PWM output is available and selection between two types of waveform output (chopping or level) is possible.	[MTU0, MTU3, MTU4, MTU6, MTU7, and MTU8] • Buffer operation specifiable [MTU3 and MTU4 only] • AC synchronous motor (brushless DC motor) drive mode using complementary PWM output or reset-synchronized PWM output is available and selection between two types of waveform output (chopping or level) is possible.

Item	RX63N (MTU2a)	RX64M (MTU3a)
Available operations	[MTU1 and MTU2] • Phase counting mode can be specified independently. • Cascade connection operation available • MTU1 and MTU2 interlocked operation in 32-bit phase counting mode is available (TMDR3.LWA = 1).	[MTU1 and MTU2] • Phase counting mode can be specified independently. • Cascade connection operation available • MTU1 and MTU2 interlocked operation in 32-bit phase counting mode is available (TMDR3.LWA = 1). [MTU0/MTU5, MTU1, MTU2, MTU8] • MTU1 or MTU2 can be used in combination with MTU0/MTU5 or MTU8 to enable 32-bit phase coefficient mode.
	[MTU3 and MTU4] • 6-phase waveform output consisting of three phases each for positive and negative complementary PWM or reset PWM output, can be achieved with linked operation.	[MTU3, MTU4, MTU6, and MTU7] • 12-phase waveform output consisting of six phases each for positive and negative complementary PWM or reset PWM output, can be achieved with linked operation. • In complementary PWM mode, transfer of values from buffer registers to temporary registers is supported at peaks and troughs of the timer-counter values or when writing to the buffer registers (MTU4.TGRD and MTU7.TGRD). • Double-buffering is selectable in complementary PWM mode.
	[MTU5] Dead-time compensation counter	[MTU5] Dead-time compensation counter
Interrupt skipping function (complementary PWM mode)	In complementary PWM mode, interrupts at counter peaks and troughs and triggers to start conversion by the A/D converter can be skipped.	In complementary PWM mode, interrupts at counter peaks and troughs and triggers to start conversion by the A/D converter can be skipped.
Interrupt sources	28	43
Buffer operation	Automatic transfer of register data	Automatic transfer of register data
Trigger generation	A/D converter start triggers can be generated.	A/D converter start triggers can be generated.
	Programmable pulse generator (PPG) output trigger generation is available.	Programmable pulse generator (PPG) output trigger generation is available.
	An A/D converter start request delaying function enables the A/D converter to be started at user-defined timing and to be synchronized with PWM output.	An A/D converter start request delaying function enables the A/D converter to be started at user-defined timing and to be synchronized with PWM output.
Low power consumption function	It is possible to specify the module stop state.	It is possible to specify the module stop state.

Table 2.17 Comparative Listing of Multi-Function Timer Pulse Unit Registers

Register	Bit	RX63N (MTU2a)	RX64M (MTU3a)
TCR2	—	—	Timer control register 2
TCR2U	—	—	Timer control register 2
TCR2V	—	—	Timer control register 2
TCR2W	—	—	Timer control register 2
TMDR	—	Timer mode register	—
TMDR1	—		Timer mode register 1
TMDR2A	—		Timer mode register 2A
TMDR2B	—		Timer mode register 2B
TMDR3	—		Timer mode register 3
TIER	TGIEC	TGR interrupt enable C bit (MTU0 to MTU4)	TGR interrupt enable C bit (MTU0, MTU3, MTU4, MTU6, MTU7, MTU8)
	TGIED	TGR interrupt enable D bit (MTU0 to MTU4)	TGR interrupt enable D bit (MTU0, MTU3, MTU4, MTU6, MTU7, MTU8)
	TGIEU	Underflow interrupt enable bit (MTU0 to MTU4)	Underflow interrupt enable bit (MTU1, MTU2)
	TTGE2	A/D converter start request enable 2 bit (MTU0 to MTU4)	A/D converter start request enable 2 bit (MTU4, MTU7)
	TTGE	A/D converter start request enable bit (MTU0 to MTU4)	A/D converter start request enable bit (MTU0 to MTU4, MTU6, MTU7)
TIER2	TTGE2	—	A/D converter start request enable 2 bit (MTU0)
TSR	TCFD	Count direction flag (MTU0 to MTU4)	Count direction flag (MTU1 to MTU4, MTU6, MTU7)
TBTM	TTSA	Timing select A bit (MTU0, MTU3, MTU4)	Timing select A bit (MTU0, MTU3, MTU4, MTU6, MTU7)
	TTSB	Timing select B bit (MTU0, MTU3, MTU4)	Timing select B bit (MTU0, MTU3, MTU4, MTU6, MTU7)
	TTSE	Timing select E bit (MTU0, MTU3, MTU4)	Timing select E bit (MTU0)
TSYCR	—	—	Timer synchro clear register
TCNTLW	—	—	Timer longword counter
TGRA	—	Timer general register A (MTU0 to MTU4)	Timer general register A (MTU0 to MTU4, MTU6, MTU7, MTU8)
TGRB	—	Timer general register B (MTU0 to MTU4)	Timer general register B (MTU0 to MTU4, MTU6, MTU7, MTU8)
TGRC	—	Timer general register C (MTU0, MTU3, MTU4)	Timer general register C (MTU0, MTU3, MTU4, MTU6, MTU7, MTU8)
TGRD	—	Timer general register D (MTU0, MTU3, MTU4)	Timer general register D (MTU0, MTU3, MTU4, MTU6, MTU7, MTU8)
TGRE	—	Timer general register E (MTU0)	Timer general register E (MTU0, MTU3, MTU4, MTU6, MTU7)
TGRF	—	Timer general register F (MTU0)	Timer general register F (MTU0, MTU4, MTU7)
TGRALW	—	—	Timer longword general register
TGRBLW	—	—	Timer longword general register
TSTR	—	Timer start register	—

Register	Bit	RX63N (MTU2a)	RX64M (MTU3a)
TSTRA	—	—	Timer start register (MTU0 to MTU4, MTU8)
TSTRB	—	—	Timer start register (MTU6, MTU7)
TSYR	—	Timer synchro register	—
TSYRA	—	—	Timer synchro register (MTU0 to MTU4)
TSYRB	—	—	Timer synchro register (MTU6, MTU7)
TCSYSTR	—	—	Timer counter synchro start register
TRWER	—	Timer read/write enable register	—
TRWERA	—	—	Timer read/write enable register
TRWERB	—	—	Timer read/write enable register
TOER	—	Timer output master enable register	—
TOERA	—	—	Timer output master enable register
TOERB	—	—	Timer output master enable register
TOCR1	—	Timer output control register 1	—
TOCR1A	—	—	Timer output control register 1
TOCR1B	—	—	Timer output control register 1
TOCR2	—	Timer output control register 2	—
TOCR2A	—	—	Timer output control register 2
TOCR2B	—	—	Timer output control register 2
TOLBR	—	Timer output level buffer register	—
TOLBRA	—	—	Timer output level buffer register
TOLBRB	—	—	Timer output level buffer register
TGCR	—	Timer gate control register	—
TGCRA	—	—	Timer gate control register A
TCNTS	—	Timer sub-counter	—
TCNTSA	—	—	Timer sub-counter
TCNTSB	—	—	Timer sub-counter
TCDR	—	Timer period data register	—
TCDRA	—	—	Timer period data register
TCDRB	—	—	Timer period data register
TCBR	—	Timer period buffer register	—
TCBRA	—	—	Timer period buffer register
TCBRB	—	—	Timer period buffer register
TDDR	—	Timer dead time data register	—
TDDRA	—	—	Timer dead time data register
TDDRB	—	—	Timer dead time data register
TDER		Timer dead time enable register	—
TDERA		—	Timer dead time enable register
TDERB		—	Timer dead time enable register
TBTER	—	Timer buffer transfer setting register	—
TBTERA	—	—	Timer buffer transfer setting register
TBTERB	—	—	Timer buffer transfer setting register
TWCR	—	Timer waveform control register	—
TWCRA	—	—	Timer waveform control register
TWCRB	—	—	Timer waveform control register
NFCR	—	Noise filter control register	—
NFCR0	—	—	Noise filter control register 0
NFCR1	—	—	Noise filter control register 1

Register	Bit	RX63N (MTU2a)	RX64M (MTU3a)
NFCR2	—	—	Noise filter control register 2
NFCR3	—	—	Noise filter control register 3
NFCR4	—	—	Noise filter control register 4
NFCR6	—	—	Noise filter control register 6
NFCR7	—	—	Noise filter control register 7
NFCR8	—	—	Noise filter control register 8
NFCRC	—	—	Noise filter control register C
NFCR5	—	——	Noise filter control register 5
TITMRA	—	—	Timer interrupt skipping mode register
TITMRB	—	—	Timer interrupt skipping mode register
TITCR	—	Timer interrupt skipping set register	—
TITCNT	—	Timer interrupt skipping counter	—
TITCR1A	—	—	Timer interrupt skipping set register 1
TITCR1B	—	—	Timer interrupt skipping set register 1
TITCNT1A	—	—	Timer interrupt skipping counter 1
TITCNT1B	—	—	Timer interrupt skipping counter 1
TITCR2A	—	—	Timer interrupt skipping set register 2
TITCR2B	—	—	Timer interrupt skipping set register 2
TITCNT2A	—	—	Timer interrupt skipping counter 2
TITCNT2B	—	—	Timer interrupt skipping counter 2

2.12 Port Output Enable

Table 2.18 shows a comparative overview of port output enable specifications, and Table 2.19 shows a comparative listing of the port output enable registers.

Table 2.18 Comparative Overview of Port Output Enable

Item	RX63N (POE2a)	RX64M (POE3)
Functions	• Each of the POE0# to POE3# and POE8# input pins can be set for falling edge, PCLK/8 × 16, PCLK/16 × 16, or PCLK/128 × 16 low-level sampling. • Pins for the MTU complementary PWM output and MTU0 pins can be placed in the high-impedance state by the POE0# to POE3#, POE8# falling-edge or low-level sampling. • Pins for complementary PWM output from the MTU and output pins for MTU0 can be placed in the high-impedance state when oscillation by the clock generation circuit stops. • Pins for the MTU complementary PWM output can be placed in the high-impedance state when output levels of the MTU complementary PWM output pins are compared and simultaneous active-level output continues for one cycle or more. • Pins for the MTU complementary PWM output and MTU0 pins can be placed in the high-impedance state by modifying the settings in the POE registers. • Interrupts can be generated by input level sampling or output level comparison.	• Each of the POE0#, POE4#, POE8#, POE10#, and POE11# input pins can be set for falling edge, PCLK/8 × 16, PCLK/16 × 16, or PCLK/128 × 16 low-level sampling. • Pins for the MTU complementary PWM output, MTU0, GPT output, and GPT3 pins can be placed in the high-impedance state by the POE0#, POE4#, POE8#, POE10#, and POE11# falling-edge or low-level sampling. • Pins for MTU complementary PWM output and the MTU0, GPT output, and GPT3 pins can be placed in the high-impedance state when stopped oscillation of the clock generator is detected. • Pins for the MTU complementary PWM output or GPT output (GPT0 to GPT2) can be placed in the high-impedance state when output levels of the MTU complementary PWM output pins or GPT output pins are compared and simultaneous active-level output continues for one cycle or more. • Pins for the MTU complementary PWM output, MTU0, GPT output, and GPT3 pins can be placed in the high-impedance state by modifying the settings in the POE registers. • Interrupts can be generated by input level sampling or output level comparison.

Table 2.19 Comparative Listing of Port Output Enable Registers

Register	Bit	RX63N (POE2a)	RX64M (POE3)
ICSR1	POE1M[1:0]	POE1 mode select bits	—
	POE2M[1:0]	POE2 mode select bits	—
	POE3M[1:0]	POE3 mode select bits	—
	POE1F	POE1 flag	—
	POE2F	POE2 flag	—
	POE3F	POE3 flag	—
ICSR2	POE4M[1:0]	—	POE4 mode select bits
	POE4F	—	POE4 flag
	POE8M[1:0]	POE8 mode select bits	—
	POE8E	POE8 high-impedance enable bit	—
	POE8F	POE8 flag	—
ICSR3	POE8M[1:0]	—	POE8 mode select bits
	PIE3		Port interrupt enable 3 bit
	POE8E	—	POE8 high-impedance enable bit
	POE8F	—	POE8 flag
	OSTSTE	OSTST high-impedance enable bit	—
	OSTSTF	OSTST high-impedance flag	—
ICSR4	—	—	Input level control/status register 4
ICSR5	—	—	Input level control/status register 5
ICSR6	—	—	Input level control/status register 6
OCSR2	—	—	Output level control/status register 2
ALR1	—	—	Active level register 1
SPOER	CH34HIZ	MTU3 and MTU4 output high-impedance enable bit	—
	CH0HIZ	MTU0 output high-impedance enable bit	—
	MTUCH34HIZ	—	MTU3, MTU4, and GPT0 to GPT2 output high-impedance enable bit
	MTUCH67HIZ	—	MTU6 and MTU7 output high-impedance enable bit
	MTUCH0HIZ	—	MTU0 output high-impedance enable bit
	GPT01HIZ	—	GPT0 and GPT1 output high-impedance enable bit
	GPT23HIZ	—	GPT2 and GPT3 output high-impedance enable bit
POECR1	PE0ZE	MTIOC0A high-impedance enable bit	—
	PE1ZE	MTIOC0B high-impedance enable bit	—
	PE2ZE	MTIOC0C high-impedance enable bit	—
	PE3ZE	MTIOC0D high-impedance enable bit	—
	MTU0AZE		MTIOC0A high-impedance enable bit
	MTU0BZE		MTIOC0B high-impedance enable bit

Register	Bit	RX63N (POE2a)	RX64M (POE3)
POECR1	MTU0CZE		MTIOC0C high-impedance enable bit
	MTU0DZE		MTIOC0D high-impedance enable bit
POECR2	P3CZEA	MTU port 3 high-impedance enable bit	—
	P2CZEA	MTU port 2 high-impedance enable bit	—
	P1CZEA	MTU port 1 high-impedance enable bit	—
	MTU7BDZE	—	MTIOC7B/7D high-impedance enable bit
	MTU7ACZE	—	MTIOC7A/7C high-impedance enable bit
	MTU6BDZE	—	MTIOC6B/6D high-impedance enable bit
	MTU4BDZE	—	MTIOC4B/4D high-impedance enable bit
	MTU4ACZE	—	MTIOC4A/4C high-impedance enable bit
	MTU3BDZE	—	MTIOC3B/3D high-impedance enable bit
POECR3	—	—	Port output enable control register 3
POECR4	—	—	Port output enable control register 4
POECR5	—	—	Port output enable control register 5
POECR6	—	—	Port output enable control register 6
G0SELR	—	—	GPT0 pin select register 0
G1SELR	—	—	GPT1 pin select register 1
G2SELR	—	—	GPT2 pin select register 2
G3SELR	—	—	GPT3 pin select register 3
M0SELR1	—	—	MTU0 pin select register 1
M0SELR2	—	—	MTU0 pin select register 2
M3SELR	—	—	MTU3 pin select register
M4SELR1	—	—	MTU4 pin select register 1
M4SELR2	—	—	MTU4 pin select register 2
MGSELR	—	—	MTU and GPT pin select register

2.13 8-Bit Timer

Table 2.20 shows a comparative overview of 8-bit timer specifications, and Table 2.21 shows a comparative listing of the 8-bit timer registers.

Table 2.20 Comparative Overview of 8-Bit Timer

Item	RX63N	RX64M
Count clocks	• Frequency-divided clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1,024, PCLK/8,192 • External clock	• Frequency-divided clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1,024, PCLK/8,192 • External clock
Number of channels	(8 bits × 2 channels) × 2 units	(8 bits × 2 channels) × 2 units
Compare match	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)
Counter clear	Selectable among compare match A, compare match B, and external reset signal.	Selectable among compare match A, compare match B, and external reset signal.
Timer output	Output pulses with a user-defined duty cycle or PWM output	Output pulses with a user-defined duty cycle or PWM output
Cascading of two channels	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode • TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).
Interrupt sources	Compare match A, compare match B, and overflow	Compare match A, compare match B, and overflow
Event link function (output)	—	Compare match A, compare match B, and overflow (TMR0 to TMR3)
Event link function (input)	—	Ability to perform one of three actions according to accepted event (1) Counter start (TMR0 to TMR3) (2) Event counter (TMR0 to TMR3) (3) Counter restart (TMR0 to TMR3)
DTC activation	The DTC can be activated by compare match A interrupts or compare match B interrupts.	The DTC can be activated by compare match A interrupts or compare match B interrupts.
Generation of trigger to start A/D converter	Compare match A of TMR0 or TMR2	Compare match A of TMR0 or TMR2
Generation of baud rate clock for SCI	Generation of baud rate clock for SCI	Generation of baud rate clock for SCI
Low power consumption function	The module stop state can be specified in each unit.	The module stop state can be specified in each unit.

Table 2.21 Comparative Listing of 8-Bit Timer Registers

Register	Bit	RX63N	RX64M
TCSTR	—	—	Time counter start register

2.14 Compare Match Timer

Table 2.22 shows a comparative overview of the compare match timer specifications.

Table 2.22 Comparative Overview of Compare Match Timer

Item	RX63N	RX64M
Count clocks	Four frequency-divided clocks One clock from among PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected individually for each channel.	Four frequency-divided clocks One clock from among PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected individually for each channel.
Interrupt	A compare match interrupt can be requested individually for each channel.	
Event link function (output)	—	Event signal output at CMT1 compare match
Event link function (input)	—	• Support for linked operation of specified module • Support for count start, event counter, or count restart when a specified event occurs
Low power consumption function	The module stop state can be specified in each unit.	The module stop state can be specified in each unit.

2.15 Realtime Clock

Table 2.23 shows a comparative overview of the realtime clock specifications, and Table 2.24 shows a comparative listing of the realtime clock registers.

Table 2.23 Comparative Overview of Realtime Clock

Item	RX63N (RTCa)	RX64M (RTCd)
Count modes	Calendar count mode	Calendar count mode, binary count mode
Count source	Sub-clock (XCIN) or main clock (EXTAL)	Sub-clock (XCIN) or main clock (EXTAL)
Clock and calendar functions	• Calendar count mode — Year, month, date, day of the week, hours, minutes, and seconds are counted and represented in BCD format — Selection of 12- or 24-hour mode — 30-second adjustment (30 seconds or less are rounded down to 00 seconds, and 30 seconds or more are rounded up to one minute.) — Automatic leap year adjustment — Start/stop function — Binary display of digits below seconds (1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, 64 Hz) — Time error adjustment function — Clock (1 Hz) output	• Calendar count mode — Year, month, date, day of the week, hours, minutes, and seconds are counted and represented in BCD format — Selection of 12- or 24-hour mode — 30-second adjustment (30 seconds or less are rounded down to 00 seconds, and 30 seconds or more are rounded up to one minute.) — Automatic leap year adjustment • Binary count mode 32-bit counting and binary display of seconds • Common to both modes — Start/stop function — Binary display of digits below seconds (1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, 64 Hz) — Time error adjustment function — Clock (1 Hz/64 Hz) output
Interrupt	• Alarm interrupt (ALM) Year, month, date, day of the week, hours, minutes, and seconds can be selected as conditions for the alarm interrupt. • Periodic interrupt (PRD) 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, 1/128 second, or 1/256 second can be selected as the interrupt period. • Carry interrupt (CUP) Generates interrupt requests at either of the following times: — At occurrence of a carry to the seconds counter from the 64 Hz counter — At coincidence of a change in the 64 Hz counter and read access to the R64CNT register	• Alarm interrupt (ALM) Any of the following can be selected as conditions for the alarm interrupt: — Calendar count mode: Year, month, date, day of the week, hours, minutes, and seconds — Binary count mode: Each bit of 32-bit binary counter • Periodic interrupt (PRD) 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, 1/128 second, or 1/256 second can be selected as the interrupt period. • Carry interrupt (CUP) Generates interrupt requests at either of the following times: — At occurrence of a carry to the seconds counter from the 64 Hz counter — At coincidence of a change in the 64 Hz counter and read access to the R64CNT register

Item	RX63N (RTCa)	RX64M (RTCd)
Interrupt	• Recovery from software standby mode or deep software standby mode can be performed by an alarm interrupt or periodic interrupt	• Recovery from software standby mode or deep software standby mode can be performed by an alarm interrupt or periodic interrupt
Time-capture function	Time capture using edge detection on the time capture event input pin is available. At each input event the month, date, hour, minute, and second is captured.	Time capture using edge detection on the time capture event input pin is available. At each input event the month, date, hour, minute, and second is captured, or the 32 -bit counter value is captured.
Event link function	—	Periodic event output

Table 2.24 Comparative Listing of Realtime Clock Registers

Register	Bit	RX63N (RTCa)	RX64M (RTCd)
BCNT0	—	—	Binary counter 0
BCNT1	—	—	Binary counter 1
BCNT2	—	—	Binary counter 2
BCNT3	—	—	Binary counter 3
BCNT0AR	—	—	Binary counter 0 alarm register
BCNT1AR	—	—	Binary counter 1 alarm register
BCNT2AR	—	—	Binary counter 2 alarm register
BCNT3AR	—	—	Binary counter 3 alarm register
BCNT0AER	—	—	Binary counter 0 alarm enable register
BCNT1AER	—	—	Binary counter 1 alarm enable register
BCNT2AER	—	—	Binary counter 2 alarm enable register
BCNT3AER	—	—	Binary counter 3 alarm enable register
RCR1	RTCOS	—	RTCOUT output select bit
RCR2	CNTMD	—	Count mode select bit
BCNT0CP0	—	—	BCNT0 capture register 0
BCNT0CP1	—	—	BCNT0 capture register 1
BCNT0CP2	—	—	BCNT0 capture register 2
BCNT1CP0	—	—	BCNT1 capture register 0
BCNT1CP1	—	—	BCNT1 capture register 1
BCNT1CP2	—	—	BCNT1 capture register 2
BCNT2CP0	—	—	BCNT2 capture register 0
BCNT2CP1	—	—	BCNT2 capture register 1
BCNT2CP2	—	—	BCNT2 capture register 2
BCNT3CP0	—	—	BCNT3 capture register 0
BCNT3CP1	—	—	BCNT3 capture register 1
BCNT3CP2	—	—	BCNT3 capture register 2

2.16 Ethernet Controller Direct Memory Access Controller

Table 2.25 shows a comparative overview of the Ethernet controller direct memory access controller specifications, and Table 2.26 shows a comparative listing of the Ethernet controller direct memory access controller registers.

Table 2.25 Comparative Overview of Ethernet Controller Direct Memory Access Controller

Item	RX63N (EDMAC)	RX64M (EDMACa)
Number of channels	• One channel for ETHERC	• One channel for ETHERC0 • One channel for ETHERC1 • One channel for EPTPC
Data transmission and reception	• Control of data transmission and reception according to descriptors • Support for single-buffer frame transmission and reception (one buffer per frame) and multi-buffer frame transmission and reception (multiple buffers per frame)	• Control of data transmission and reception according to descriptors • Support for single-buffer frame transmission and reception (one buffer per frame) and multi-buffer frame transmission and reception (multiple buffers per frame)
Functions	• Minimizing of system bus occupation time using block transfers (32-byte units) • Write-back of transmit/receive frame state to descriptors • Insertion of padding in receive data	• Minimizing of system bus occupation time using block transfers (32-byte units) • Write-back of transmit/receive frame state to descriptors • Insertion of padding in receive data
Low power consumption function	The module stop state can be specified in each unit.	The module stop state can be specified in each unit.

Table 2.26 Comparative Listing of Ethernet Controller Direct Memory Access Controller Registers

Register	Bit	RX63N (EDMAC)	RX64M (EDMACa)
PTPEDMAC.EESR	—	—	PTP/EDMAC status register
PTPEDMAC.EESIPR	—	—	PTP/EDMAC status interrupt enable register
TRSCER	CERFCE	CERF bit copy directive bit	—
	PRECE	PRE bit copy directive bit	—
	RTSFCE	RTSF bit copy directive bit	—
	RTLFCE	RTLF bit copy directive bit	—
	TROCE	TRO bit copy directive bit	—
	CDCE	CD bit copy directive bit	—
	DLCCE	DLC bit copy directive bit	—
	CNDCE	CND bit copy directive bit	—
RMCR	RNC	Receive request bit non-reset mode directive bit	—

2.17 USB 2.0 Host/Function Module

Table 2.27 shows a comparative overview of the USB 2.0 Host/Function module specifications, and Table 2.28 shows a comparative listing of the USB 2.0 Host/Function module registers.

Table 2.27 Comparative Overview of USB 2.0 Host/Function Module

Item	RX63N (USBa)	RX64M (USBb)
Ports	2	1
Features	• Integrated USB Device Controller (UDC) and transceiver for USB 2.0 — USB0: Support for Host controller, Function controller, and on-the-go (OTG) functionality — USB1: Support for Function controller • Software can switch between the Host controller and Function controller modes. • Self-power mode or bus-power mode can be selected.	• Integrated USB Device Controller (UDC) and transceiver for USB 2.0 — Support for Host controller, Function controller, and on-the-go (OTG) functionality • Software can switch between the Host controller and Function controller modes. • Self-power mode or bus-power mode can be selected.
	When Host controller operation is selected: • Full-speed transfer (12 Mbps) is supported. • Automatic scheduling of SOF and packet transmissions • Transfer interval setting function for isochronous and interrupt transfers • Communication with multiple peripheral devices connected via a single hub	When Host controller operation is selected: • Full-speed transfer (12 Mbps) and low-speed transfer (1.5 Mbps) are supported. • Automatic scheduling of SOF and packet transmissions • Transfer interval setting function for isochronous and interrupt transfers • Communication with multiple peripheral devices connected via a single hub
	When Function controller operation is selected: • Support for full-speed transfer (12 Mbps) • Control transfer stage control function • Device state control function • Auto response function for SET_ADDRESS requests • SOF interpolation function	When Function controller operation is selected: • Support for full-speed transfer (12 Mbps)* • Control transfer stage control function • Device state control function • Auto response function for SET_ADDRESS requests • SOF interpolation function
Communication data transfer types	• Control transfer • Bulk transfer • Interrupt transfer • Isochronous transfer	• Control transfer • Bulk transfer • Interrupt transfer • Isochronous transfer
Pipe configuration	• On-chip buffer memory for USB communications • Up to ten pipes can be selected (including the default control pipe). • Endpoint numbers can be assigned flexibly to PIPE1 to PIPE9.	• On-chip buffer memory for USB communications • Up to ten pipes can be selected (including the default control pipe). • Endpoint numbers can be assigned flexibly to PIPE1 to PIPE9.

Item	RX63N (USBa)	RX64M (USBb)
Pipe configuration	Transfer conditions that can be set for each pipe: • PIPE0: Control transfer only (default control pipe: DPC), buffer size: 8, 16, 32, and 64 bytes (single buffer) • PIPE1 and PIPE2: Bulk transfer or isochronous transfer, bulk transfer buffer size: 8, 16, 32, and 64 bytes (support for double buffer setting), isochronous transfer buffer size: 1 to 256 bytes (support for double buffer setting) • PIPE3 to PIPE5: Bulk transfer only, buffer size: 8, 16, 32, and 64 bytes (support for double buffer setting) • PIPE6 to PIPE9: Interrupt transfer only: buffer size: 1 to 64 bytes (single buffer)	Transfer conditions that can be set for each pipe: • PIPE0: Control transfer only (default control pipe: DPC), buffer size: 64 bytes (single buffer) • PIPE1 and PIPE2: Bulk transfer or isochronous transfer, bulk transfer buffer size: 64 bytes (support for double buffer setting), isochronous transfer buffer size: 256 bytes (support for double buffer setting) • PIPE3 to PIPE5: Bulk transfer only, buffer size: 64 bytes (support for double buffer setting) • PIPE6 to PIPE9: Interrupt transfer only: buffer size: 64 bytes (single buffer)
Other functions	• Reception end function using transaction count • Function that changes the BRDY interrupt event notification timing (BFRE) • Function that automatically clears the buffer memory after the data for the pipe specified at the DnFIFO (n = 0 or 1) port has been read (DCLRM) • NAK setting function for response PID generated by end of transfer (SHTNAK)	• Reception end function using transaction count • Function that changes the BRDY interrupt event notification timing (BFRE) • Function that automatically clears the buffer memory after the data for the pipe specified at the DnFIFO (n = 0 or 1) port has been read (DCLRM) • NAK setting function for response PID generated by end of transfer (SHTNAK) • On-chip DP/DM pull-up and pull-down resistors
Low power consumption function	It is possible to specify the module stop state.	It is possible to specify the module stop state.

Note: * Low-speed transfer (1.5 Mbps) is not supported when Function controller operation is selected.

Table 2.28 Comparative Listing of USB 2.0 Host/Function Module Registers

Register	Bit	RX63N (USBa)	RX64M (USBb)
SYSSTS0	SOFEA	—	Host controller operation SOF active monitor bit
PHYSLEW	—	—	PHY crosspoint adjustment register
DPUSR0R	RPUE0	—	DP pull-up resistor control bit
	DRPD0	—	D+/D– pull-down resistor control bit
	SRPC1	USB1 single end receiver control bit	—
	FIXPHY1	USB1 transceiver output fix bit	—
	DP1	USB1 DP input	—
	DM1	USB1 DM input	—
	DVBSTS1	USB1 VBUS input	—
DPUSR1R	DPINTE1	USB1 DP interrupt enable/clear bit	—
	DMINTE1	USB1 DM interrupt enable/clear bit	—
	DVBSE1	USB1 VBUS interrupt enable/clear bit	—
	DPINT1	USB1 DP interrupt source recovery bit	—
	DMINT1	USB1 DM interrupt source recovery bit	—
	DVBINT1	USB1 VBUS interrupt source recovery bit	—

2.18 Serial Communication Interface

The RX63N Group and RX631 Group have 13 independent serial communications interface (SCI) channels (SCIc: 12 channels, SCId: 1 channel).

The RX64M Group has 9 independent serial communications interface (SCI) channels (SCIg: 8 channels, SCIh: 1 channel).

Table 2.29 shows a comparative listing of the SCIc and SCIg specifications, Table 2.30 shows a comparative listing of the SCId and SCIh specifications, Table 2.31 shows a comparative listing of the SCI channel specifications, and Table 2.32 shows a comparative listing of the serial communications interface registers.

Table 2.29 Comparative Listing of SCIc and SCIg Specifications

Item		RX63N (SCIc)	RX64M (SCIg)
Number of channels		12 channels	8 channels
Serial communication modes		• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus
Transfer speed		Bit rate specifiable by on-chip baud rate generator.	Bit rate specifiable by on-chip baud rate generator. (The settable bit rates will differ due to differences in the electrical characteristics. See the user's manual for details.)
Full-duplex communication		• Transmitter: Continuous transmission possible using double-buffer configuration. • Receiver: Continuous reception possible using double-buffer configuration.	• Transmitter: Continuous transmission possible using double-buffer configuration. • Receiver: Continuous reception possible using double-buffer configuration.
Data transfer		Selectable between LSB-first or MSB-first transfer.*	Selectable between LSB-first or MSB-first transfer.*
Interrupt sources		Transmit end, transmit data empty, receive data full, receive error, completion of generation of start condition, restart condition, or stop condition (simple I²C mode)	Transmit end, transmit data empty, receive data full, receive error, completion of generation of start condition, restart condition, or stop condition (simple I²C mode)
Low power consumption function		The module stop state can be specified for each channel.	The module stop state can be specified for each channel.
Synchronous mode	Data length	7 or 8 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	The CTSn# and RTSn# pins can be used to control transmission and reception.	The CTSn# and RTSn# pins can be used to control transmission and reception.
	Start bit detection	Low level detection	Selectable between low level and falling edge.

Item		RX63N (SCIc)	RX64M (SCIg)
Synchronous mode	Break detection	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.
	Clock source	An internal or external clock can be selected. Transfer rate clock input from the TMR can be used (SCI5 and SCI6).	An internal or external clock can be selected. Transfer rate clock input from the TMR can be used (SCI5 and SCI6).
	Double-speed mode	—	Baud rate generator double-speed mode is selectable.
	Multi-processor communication function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate on-chip digital noise filters.	The signal paths from input on the RXDn pins incorporate on-chip digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	The CTSn# and RTSn# pins can be used to control transmission and reception.	The CTSn# and RTSn# pins can be used to control transmission and reception.
Smart card interface mode	Error processing	An error signal can be transmitted automatically when a parity error is detected during reception.	An error signal can be transmitted automatically when a parity error is detected during reception.
		Data can be retransmitted automatically when an error signal is received during transmission.	Data can be retransmitted automatically when an error signal is received during transmission.
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.
Simple I^2C mode	Communication format	I^2C bus format	I^2C bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer speed	Fast mode is supported.	Fast mode is supported.
	Noise canceler	The signal paths from input on the SSCLn and SSDAn pins incorporate on-chip digital noise filters, and the noise cancellation bandwidth is adjustable.	The signal paths from input on the SSCLn and SSDAn pins incorporate on-chip digital noise filters, and the noise cancellation bandwidth is adjustable.
Simple SPI mode	Data length	8 bits	8 bits
	Error detection	Overrun error	Overrun error
	SS input pin function	Applying a high-level signal to the SSn# pin causes the output pins to enter the high-impedance state.	Applying a high-level signal to the SSn# pin causes the output pins to enter the high-impedance state.
	Clock settings	Selectable among four clock phase and clock polarity settings.	Selectable among four clock phase and clock polarity settings.
Bit rate modulation function		—	On-chip baud rate generator output correction can reduce errors.
Event link function		—	Error (receive error, error signal detection) event output
		—	Receive data full event output
		—	Transmit data empty event output
		—	Transmit end event output

Note: * Only MSB-first is available in simple I^2C mode.

Table 2.30 Comparative Listing of SCId and SCIh Specifications

Item		RX63N (SCId)	RX64M (SCIh)
Number of channels		1 channel	1 channel
Serial communication modes		• Asynchronous • Clock synchronous • Smart card interface • Simple I^2C bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I^2C bus • Simple SPI bus
Transfer speed		Bit rate specifiable by on-chip baud rate generator.	Bit rate specifiable by on-chip baud rate generator.
Full-duplex communication		• Transmitter: Continuous transmission possible using double-buffer configuration. • Receiver: Continuous reception possible using double-buffer configuration.	• Transmitter: Continuous transmission possible using double-buffer configuration. • Receiver: Continuous reception possible using double-buffer configuration.
Data transfer		Selectable between LSB-first or MSB-first transfer.*	Selectable between LSB-first or MSB-first transfer.*
Interrupt sources		Transmit end, transmit data empty, receive data full, receive error, completion of generation of start condition, restart condition, or stop condition (simple I^2C mode)	Transmit end, transmit data empty, receive data full, receive error, completion of generation of start condition, restart condition, or stop condition (simple I^2C mode)
Low power consumption function		It is possible to specify the module stop state.	It is possible to specify the module stop state.
Synchronous mode	Data length	7 or 8 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection	The CTSn# and RTSn# pins can be used to control transmission and reception.	The CTSn# and RTSn# pins can be used to control transmission and reception.
	Hardware flow control	The CTSn# and RTSn# pins can be used to control transmission and reception.	The CTSn# and RTSn# pins can be used to control transmission and reception.
	Start bit detection	Low level detection	Selectable between low level and falling edge.
	Break detection	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.
	Clock source	An internal or external clock can be selected. Transfer rate clock input from the TMR can be used (SCI5 and SCI6).	An internal or external clock can be selected. Transfer rate clock input from the TMR can be used (SCI5 and SCI6).
	Double-speed mode	—	Baud rate generator double-speed mode is selectable.
	Multi-processor communication function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate on-chip digital noise filters.	The signal paths from input on the RXDn pins incorporate on-chip digital noise filters.

Item		RX63N (SCId)	RX64M (SCIh)
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	The CTSn# and RTSn# pins can be used to control transmission and reception.	The CTSn# and RTSn# pins can be used to control transmission and reception.
Smart card interface mode	Error processing	An error signal can be transmitted automatically when a parity error is detected during reception.	An error signal can be transmitted automatically when a parity error is detected during reception.
		Data can be retransmitted automatically when an error signal is received during transmission.	Data can be retransmitted automatically when an error signal is received during transmission.
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.
Simple I^2C mode	Communication format	I^2C bus format	I^2C bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer speed	Fast mode is supported.	Fast mode is supported.
	Noise canceler	The signal paths from input on the SSCLn and SSDAn pins incorporate on-chip digital noise filters, and the noise cancellation bandwidth is adjustable.	The signal paths from input on the SSCLn and SSDAn pins incorporate on-chip digital noise filters, and the noise cancellation bandwidth is adjustable.
Simple SPI mode	Data length	8 bits	8 bits
	Error detection	Overrun error	Overrun error
	SS input pin function	Applying a high-level signal to the SSn# pin causes the output pins to enter the high-impedance state.	Applying a high-level signal to the SSn# pin causes the output pins to enter the high-impedance state.
	Clock settings	Selectable among four clock phase and clock polarity settings.	Selectable among four clock phase and clock polarity settings.
Extended serial mode	Start frame transmission	• Output of the break field low width and generation of an interrupt on detection • Detection of bus collisions and the generation of interrupts on detection	• Output of the break field low width and generation of an interrupt on detection • Detection of bus collisions and the generation of interrupts on detection

Item		RX63N (SCId)	RX64M (SCIh)
Extended serial mode	Start frame reception	• Detection of the break field low width and generation of an interrupt on detection • Comparison of data in control fields 0 and 1 and generation of an interrupt when the two match • Two kinds of data for comparison (primary and secondary) can be set in control field 1. • A priority interrupt bit can be set in control field 1. • Support for handling of start frames that do not include a break field • Support for handling of start frames that do not include control field 0 • Function for measuring bit rates	• Detection of the break field low width and generation of an interrupt on detection • Comparison of data in control fields 0 and 1 and generation of an interrupt when the two match • Two kinds of data for comparison (primary and secondary) can be set in control field 1. • A priority interrupt bit can be set in control field 1. • Support for handling of start frames that do not include a break field • Support for handling of start frames that do not include control field 0 • Function for measuring bit rates
	I/O control functions	• Selectable polarity for TXDX12 and RXDX12 signals • Ability to enable digital filter function for RXDX12 • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Selectable timing for the sampling of data received through RXDX12 • Signals received on RXDX12 can be passed through to SCIc when the extended serial mode control section is off.	• Selectable polarity for TXDX12 and RXDX12 signals • Ability to enable digital filter function for RXDX12 • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Selectable timing for the sampling of data received through RXDX12 • Signals received on RXDX12 can be passed through to SCIc when the extended serial mode control section is off.
	Timer function	Usable as a reloading timer	Usable as a reloading timer
Bit rate modulation function		—	On-chip baud rate generator output correction can reduce errors.

Note: * Only MSB-first is available in simple I^2C mode.

Table 2.31 Comparative Listing of SCI Channel Specifications

Item	RX63N (SCIc, SCId)	RX64M (SCIg, SCIh)
Synchronous mode	SCI0 to SCI12	SCI0 to SCI7, SCI12
Clock synchronous mode	SCI0 to SCI12	SCI0 to SCI7, SCI12
Smart card interface mode	SCI0 to SCI12	SCI0 to SCI7, SCI12
Simple I^2C mode	SCI0 to SCI12	SCI0 to SCI7, SCI12
Simple SPI mode	SCI0 to SCI12	SCI0 to SCI7, SCI12
Extended serial mode	SCI12	SCI12
TMR clock input	SCI5, SCI6, SCI12	SCI5, SCI6, SCI12
Event link function	—	SCI5

Table 2.32 Comparative Listing of Serial Communication Interface Registers

Register	Bit	RX63N (SCIc, SCId)	RX64M (SCIg, SCIh)
RDRHL	—	—	Receive data register HL
TDRHL	—	—	Transmit data register HL
SSR	RDRF	—	Receive data full flag
	TDRF	—	Transmit data empty flag
SCMR	CHR1	—	Character length bit 1
MDDR	—	—	Modulation duty register
SEMR	BRME	—	Bit rate modulation enable bit
	BGDM	—	Baud rate generator double-speed mode select bit
	RXDESEL	—	Asynchronous start bit edge detection select bit

2.19 I²C Bus Interface

Table 2.33 shows a comparative overview of the I²C bus interface specifications, and Table 2.34 shows a comparative listing of the I²C bus interface registers.

Table 2.33 Comparative Overview of I²C Bus Interface

Item	RX63N (RIIC)	RX64M (RIICa)
Number of channels	4 channels	2 channels
Communication format	• I²C bus format or SMBus format • Selectable between master mode or slave mode. • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate	• I²C bus format or SMBus format • Selectable between master mode or slave mode. • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate
Transfer speed	Fast mode is supported.	Fast mode is supported.
SCL clock	For master operation, the duty cycle of the SCL clock is selectable in the range from 4% to 96%.	For master operation, the duty cycle of the SCL clock is selectable in the range from 4% to 96%.
Issuing and detection conditions	Start, restart, and stop conditions are generated automatically. Start conditions (including restart conditions) and stop conditions are detectable.	Start, restart, and stop conditions are generated automatically. Start conditions (including restart conditions) and stop conditions are detectable.
Slave addresses	• Up to three different slave addresses can be set. • 7-bit and 10-bit address formats are supported (along with the use of both at once). • General call addresses, device ID addresses, and SMBus host addresses are detectable.	• Up to three different slave addresses can be set. • 7-bit and 10-bit address formats are supported (along with the use of both at once). • General call addresses, device ID addresses, and SMBus host addresses are detectable.
Acknowledgement	• For transmission, the acknowledge bit is loaded automatically. — Transfer of the next data for transmission can be suspended automatically on reception of a not-acknowledge bit. • For reception, the acknowledge bit is transmitted automatically. — If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible.	• For transmission, the acknowledge bit is loaded automatically. — Transfer of the next data for transmission can be suspended automatically on reception of a not-acknowledge bit. • For reception, the acknowledge bit is transmitted automatically. — If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible.
Wait function	For reception, the following wait periods can be obtained by holding the SCL clock at the low level: • Wait between the eighth and ninth clock cycles • Wait between the ninth and first clock cycles (wait function)	For reception, the following wait periods can be obtained by holding the SCL clock at the low level: • Wait between the eighth and ninth clock cycles • Wait between the ninth and first clock cycles
SDA output delay function	Timing of the output of transmitted data, including the acknowledge bit, can be delayed.	Timing of the output of transmitted data, including the acknowledge bit, can be delayed.

Item	RX63N (RIIC)	RX64M (RIICa)
Arbitration	• Multi-master support Operation to synchronize the SCL clock in cases of conflict with the SCL clock from another master is possible. When issuing a start condition, loss of arbitration is detected by testing for non-matching of the signals for the SDA line. In master operation, loss of arbitration is detected by testing for non-matching of transmit data. • Loss of arbitration due to detection of a start condition while the bus is busy is detectable (to prevent the issuing of double start conditions). • Loss of arbitration in transfer of a not-acknowledge bit due to the signals for the SDA line not matching is detectable. • Loss of arbitration due to non-matching of data is detectable in slave transmission.	• Multi-master support Operation to synchronize the SCL clock in cases of conflict with the SCL clock from another master is possible. When issuing a start condition, loss of arbitration is detected by testing for non-matching of the signals for the SDA line. In master operation, loss of arbitration is detected by testing for non-matching of transmit data. • Loss of arbitration due to detection of a start condition while the bus is busy is detectable (to prevent the issuing of double start conditions). • Loss of arbitration in transfer of a not-acknowledge bit due to the signals for the SDA line not matching is detectable. • Loss of arbitration due to non-matching of data is detectable in slave transmission.
Timeout detection function	The internal timeout function is capable of detecting long-interval stop of the SCL clock.	The internal timeout function is capable of detecting long-interval stop of the SCL clock.
Noise canceler	The interface incorporates digital noise filters for both the SCL and SDA inputs, and the bandwidth for noise cancellation by the filters is adjustable by software.	The interface incorporates digital noise filters for both the SCL and SDA inputs, and the bandwidth for noise cancellation by the filters is adjustable by software.
Interrupt sources	Four sources • Communication error or event occurrence Arbitration detection, NACK detection, timeout detection, start condition detection (including restart condition), stop condition detection • Receive data full (including matching with a slave address) • Transmit data empty (including matching with a slave address) • Transmit end	Four sources • Communication error or event occurrence Arbitration detection, NACK detection, timeout detection, start condition detection (including restart condition), stop condition detection • Receive data full (including matching with a slave address) • Transmit data empty (including matching with a slave address) • Transmit end
Low power consumption function	It is possible to specify the module stop state.	It is possible to specify the module stop state.
Event link function	—	• Communication error/event generation • Receive data full • Transmit data empty • Transmit end

Table 2.34 Comparative Listing of I²C Bus Interface Registers

Register	Bit	RX63N (RIIC)	RX64M (RIICa)
ICMR2	TMWE	Timeout internal counter write enable bit	—
TMOCNTL	—	Timeout internal counter L	—
TMOCNTU	—	Timeout internal counter U	—

2.20 Serial Peripheral Interface

Table 2.35 shows a comparative overview of the serial peripheral interface specifications, and Table 2.36 shows a comparative listing of the serial peripheral interface registers.

Table 2.35 Comparative Overview of Serial Peripheral Interface

Item	RX63N (RSPI)	RX64M (RSPIc)
Number of channels	3 channels	1 channel
RSPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communication through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Transmit-only operation is available. • Communication mode: Full-duplex or transmit-only can be selected. • Switching of the polarity of RSPCK is supported. • Switching of the phase of RSPCK is supported.	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communication through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Transmit-only operation is available. • Communication mode: Full-duplex or transmit-only can be selected. • Switching of the polarity of RSPCK is supported. • Switching of the phase of RSPCK is supported.
Data format	• Selectable between MSB-first and LSB-first. • Transfer bit length is selectable among 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (with each frame consisting of up to 32 bits).	• Selectable between MSB-first and LSB-first. • Transfer bit length is selectable among 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (with each frame consisting of up to 32 bits).
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from 2 to 4,096). • In slave mode, the minimum PCLK clock divided by 8 can be input as RSPCK (the maximum frequency of RSPCK is PCLK divided by 8). Width at high level: 4 cycles of PCLK; width at low level: 4 cycles of PCLK	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from 2 to 4,096). • In slave mode, the minimum PCLK clock divided by 8 can be input as RSPCK (the maximum frequency of RSPCK is PCLK divided by 8). Width at high level: 4 cycles of PCLK; width at low level: 4 cycles of PCLK (The settable bit rates will differ due to differences in the electrical characteristics. See the user's manual for details.)

Item	RX63N (RSPI)	RX64M (RSPIc)
Buffer configuration	• The transmit and receive buffers have a double buffer configuration. • The transmit and receive buffers are each 128 bits in size.	• The transmit and receive buffers have a double buffer configuration. • The transmit and receive buffers are each 128 bits in size.
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection	• Mode fault error detection • Overrun error detection When master receive and the RSPCK auto-stop function are enabled, the transfer clock stops at the point in time when overrun error detection occurs, so no overrun error is generated. • Parity error detection
SSL control function	• Four SSL signals (SSLn0 to SSLn3) for each channel • In single-master mode, SSLn0 to SSLn3 signals are output. • In multi-master mode: SSLn0 signal is input, and SSLn1 to SSLn3 signals are either output or unused. • In slave mode: SSLn0 signal is input, and SSLn1 to SSLn3 signals are unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • SSL polarity-change function	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin is input, and SSLA1 to SSLA3 pins are either output or unused. • In slave mode: SSLA0 pin is input, and SSLA1 to SSLA3 pins are unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • SSL polarity-change function
Control in master transfer	• Transfers of up to eight commands can be performed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, LSB/MSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • The MOSI signal value when SSL is negated can be specified.	• Transfers of up to eight commands can be performed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, LSB/MSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • The MOSI signal value when SSL is negated can be specified. • RSPCK auto-stop function

Item	RX63N (RSPI)	RX64M (RSPIc)
Interrupt sources	• Receive buffer full interrupt • Transmit buffer empty interrupt • RSPI error interrupt (mode fault, overrun, parity error) • RSPI idle interrupt (RSPI idle)	• Receive buffer full interrupt • Transmit buffer empty interrupt • RSPI error interrupt (mode fault, overrun, parity error) • RSPI idle interrupt (RSPI idle)
Event link function (output)	—	The following events can be output to the event link controller: • Receive buffer run event signal • Transmit buffer empty event signal • Mode fault, overrun, or parity error event signal • RSPI idle event signal • Transmit end event signal
Other functions	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loopback mode function	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loopback mode function
Low power consumption function	It is possible to specify the module stop state.	It is possible to specify the module stop state.

Table 2.36 Comparative Listing of Serial Peripheral Interface Registers

Register	Bit	RX63N (RSPI)	RX64M (RSPIa)
SPSR	SPTEF	—	Transmit buffer empty flag
	SPRF	—	Receive buffer full flag
SPCR2	SCKASE	—	RSPCK auto-stop function enable bit

2.21 Parallel Data Capture Unit

Table 2.37 shows a comparative overview of the parallel data capture unit interface specifications.

Table 2.37 Comparative Overview of Parallel Data Capture Unit Interface

Item	RX63N (PDC)	RX64M (PDC)
Capture range	User-specified amounts of parallel data within the following ranges in the vertical and horizontal directions: Vertical direction: 1 to 4,095 lines Horizontal direction: 4 to 4,095 bytes	User-specified amounts of parallel data within the following ranges in the vertical and horizontal directions: Vertical direction: 1 to 4,095 lines Horizontal direction: 4 to 4,095 bytes
Parallel transfer clock (PIXCLK)	Operating frequency: 1 to 27 MHz	Operating frequency: 1 to 27 MHz
Interrupt sources	• Receive data ready • Frame end • Overrun • Underrun • Error in the setting for the number of vertical lines • Error in setting for the number of horizontal bytes per line	• Receive data ready • Frame end • Overrun • Underrun • Error in the setting for the number of vertical lines • Error in setting for the number of horizontal bytes per line
DTC/DMAC activation	Support for activation by receive data ready interrupt	Support for activation by receive data ready interrupt
Parallel transfer clock output (PCKO)	• Operating frequency: 1 to 25 MHz • Clock source: Peripheral module clock B (PCLKB) • Frequency division ratio: Selectable among 2, 4, 6, 8, 10, 12, 14, and 16	• Operating frequency: 1 to 30 MHz • Clock source: Peripheral module clock B (PCLKB) • Frequency division ratio: Selectable among 2, 4, 6, 8, 10, 12, 14, and 16
Other functions	• PDC reset function • Selectable polarity for VSYNC and HSYNC signals • Monitoring of VSYNC and HSYNC signals • Endianness selection function	• PDC reset function • Selectable polarity for VSYNC and HSYNC signals • Monitoring of VSYNC and HSYNC signals • Endianness selection function
Low power consumption function	It is possible to specify the module stop state.	It is possible to specify the module stop state.
Internal bus interface	Connected to internal peripheral bus 3	Connected to internal peripheral bus 3

2.22 12-Bit A/D Converter

Table 2.38 shows a comparative overview of the 12-bit A/D converter specifications, and Table 2.39 shows a comparative listing of the 12-bit A/D converter registers.

Table 2.38 Comparative Overview of 12-Bit A/D Converter

Item	RX63N (S12ADa)	RX64M (S12ADC)
Number of units	1 unit	2 units
Input channels	21 channels	Unit 0: 8 channels Unit 1: 21 channels + one extended channel
Extended analog function	Temperature sensor output, internal reference voltage	Temperature sensor output, internal reference voltage
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12 bits	12 bits
Conversion time	1.0 µs per channel (when operating with A/D conversion clock ADCLK = 50 MHz)	• (0.48 µs) per channel (12-bit conversion mode) • (0.45 µs) per channel (10-bit conversion mode) • (0.42 µs) per channel (8-bit conversion mode) (Operating with A/D conversion clock ADCLK = 60 MHz)
A/D conversion clock (ADCLK)	4 clocks: PCLK, PCLK/2, PCLK/4, PCLK/8	Peripheral module clock PCLKB and A/D conversion clock ADCLK can be set so that the division ratio is one of the following: PCLKB: ADCLK division ratio = 1:1, 1:2, 1:4, 1:8 ADCLK is set using the clock generation circuit (CPG).
Data register	• For analog input: 21 data registers	• For analog input: 29 data registers (unit 0: 8 data registers, unit 1: 21 data registers), one data register for each unit for A/D conversion data multiplexing in double trigger mode, two data registers for each unit for A/D conversion data multiplexing in double trigger mode extended operation
	• For temperature sensor: One data register • For internal reference voltage: One data register • The results of A/D conversion are stored in 12-bit A/D data registers.	• For temperature sensor: One data register (unit 1 only) • For internal reference voltage: One data register (unit 1 only) • The results of A/D conversion are stored in 12-bit A/D data registers. • Output of A/D conversion results at 8-, 10-, or 12-bit precision
	• In A/D-converted value addition mode, A/D conversion results are stored in a 14-bit A/D data register.	• The value obtained by adding up A/D-converted results is stored as a value (number of conversion accuracy bits + 2 bits) in the A/D data registers in A/D-converted value addition mode.

Item	RX63N (S12ADa)	RX64M (S12ADC)
Data register		• Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers): A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.
Operating mode	• Single scan mode: — A/D conversion is performed only once on the analog inputs of up to 21 user-selected channels. — A/D conversion is performed only once on the temperature sensor output. — A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: — A/D conversion is performed repeatedly on the analog inputs of up to 21 user-selected channels. (Continuous scan mode should not be used when temperature sensor output or the internal reference voltage is selected.)	• Single scan mode: — A/D conversion is performed only once on the analog inputs of up to 8 (unit 0) or up to 12 (unit 1) user-selected channels. — A/D conversion is performed only once on the temperature sensor output (unit 1 only). — A/D conversion is performed only once on the internal reference voltage (unit 1 only). — A/D conversion is performed only once on the extended analog input (unit 1 only). • Continuous scan mode: — A/D conversion is performed repeatedly on the analog inputs of up to 8 (unit 0) or up to 21 (unit 1) user-selected channels, the temperature sensor output (unit 1 only), or the internal reference voltage (unit 1 only). — A/D conversion is performed repeatedly on the extended analog input (unit 1 only). • Group scan mode: — The analog inputs of up to 8 (unit 0) or up to 21 (unit 1) user-selected channels, the temperature sensor output (unit 1 only), and the internal reference voltage (unit 1 only) are divided up among group A and group B, and A/D conversion is performed only once on the analog inputs selected as a group unit. — The scanning start conditions (synchronous triggers) can be selected independently for group A and group B, allowing conversion to start at a different time for each group.

Item	RX63N (S12ADa)	RX64M (S12ADC)
Operating mode		• Group scan mode (with group A priority control selected): — If a group A trigger is input when A/D conversion on group B is in progress, scanning of group B is stopped and scanning of group A starts. — Restart of A/D conversion on group B (rescan) after completion of A/D conversion on group A can be enabled.
A/D conversion start conditions	• Software trigger • Synchronous trigger Conversion start is triggered by the MTU, TPU, and TMR. • Asynchronous trigger A/D conversion can be triggered by the ADTRG0# pin.	• Software trigger • Synchronous trigger Conversion start is triggered by the MTU, TPU, TMR, GPT, and ELC. • Asynchronous trigger A/D conversion can be started by the external trigger ADTRG0# pin (unit 0) or ADTRG1# pin (unit 1).
Functions	• Sample-and-hold function • Variable sampling state count • Selectable A/D-converted value adding mode	• Sample-and-hold function • Channel-dedicated sample-and-hold function (3 channels: unit 1) • Variable sampling state count • Self-diagnostic function for 12-bit A/D converter • Selectable A/D-converted value adding mode or averaging mode • Analog input disconnection detection function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Function for switching among 12-, 10-, and 8-bit conversion • A/D data register auto-clear function • Extended analog input function • Digital comparison (comparison of values in the comparison register and the data register, and comparison between values in the data registers)
Interrupt sources	• An scan end interrupt request (S12ADI0) can be generated on completion of A/D conversion.	• In modes other than double trigger mode and group scan mode, an A/D scan end interrupt request (S12ADI) can be generated on completion of a single scan. • In double trigger mode, an A/D scan end interrupt request (S12ADI) can be generated on completion of a double scan.

Item	RX63N (S12ADa)	RX64M (S12ADC)
Interrupt sources	• A S12ADI0 interrupt can activate the DMAC and DTC.	• In group scan mode, a scan end interrupt request (S12ADI) can be generated on completion of a group A scan. On completion of a group B scan a dedicated group B scan end interrupt request (S12GBADI) can be generated. • When double trigger mode is selected in group scan mode, a scan end interrupt request (S12ADI) can be generated on completion of two scans of group A. On completion of a group B scan a dedicated scan end interrupt request (S12GBADI) can be generated. • A compare interrupt (S12CMPI) can be generated when the digital compare function comparison conditions are met. • The DMAC or DTC can be activated by the S12ADI or S12GBADI interrupt.
Event link function	—	• In group scan mode an ELC event can be generated on completion of scans other than group B scan. • Scanning can be started by a trigger from the ELC.
Low power consumption function	It is possible to specify the module stop state.	It is possible to specify the module stop state.

Table 2.39 Comparative Listing of 12-Bit A/D Converter Registers

Register	Bit	RX63N (S12ADa)	RX64M (S12ADC)
ADDBLDR	—	—	A/D data duplication register
ADDBLDRA	—	—	A/D data duplication register A
ADDBLDRB	—	—	A/D data duplication register B
ADRD	—	—	A/D self-diagnostic data register
ADCSR	DBLANS[4:0]	—	Double trigger channel select bits
	GBADIE	—	Group B scan end interrupt enable bit
	DBLE	—	Double trigger mode select bit
	EXTRG	Trigger select bit	Trigger select bit
	TRGE	Trigger start enable bit	Trigger start enable bit
	CKS[1:0]	A/D conversion clock select bits	—
	ADIE	Scan end interrupt enable bit	Scan end interrupt enable bit
	ADCS	Scan mode select bit	—
	ADCS[1:0]	—	Scan mode select bits
	ADST	A/D conversion start bit	A/D conversion start bit
ADANS0	—	A/D channel select register 0	—
ADANS1	—	A/D channel select register 1	—
ADANSA0	—	—	A/D channel select register A0
ADANSA1	—	—	A/D channel select register A1
ADANSB0	—	—	A/D channel select register B0
ADANSB1	—	—	A/D channel select register B1
ADADS0	—	A/D-converted value addition mode select register 0	A/D-converted value addition/averaging mode select register 0
ADADS1	—	A/D-converted value addition mode select register 1	A/D-converted value addition/averaging mode select register 1
ADADC	AVEE	—	Average mode enable bit
ADCER	ADPRC[1:0]	—	A/D conversion precision setting bits
	ACE	Automatic clearing enable bit	A/D data register automatic clearing enable bit
	DIAGVAL [1:0]	—	Self-diagnostic conversion voltage select bits
	DIAGLD	—	Self-diagnostic mode select bit
	DIAGM	—	Self-diagnostic enable bit
ADSTRGR	ADSTRS [3:0]	A/D conversion start trigger select bits	—
	TRSB[5:0]	—	A/D conversion start trigger for group B select bits
	TRSA[5:0]	—	A/D conversion start trigger select bits
ADEXICR	TSSAD	Temperature sensor output A/D-converted value addition mode select bit	Temperature sensor output A/D-converted value addition/averaging mode select bit
	OCSAD	Internal reference voltage A/D conversion select bit	Internal reference voltage A/D-converted value addition/average mode select bit
	TSS	Temperature sensor output A/D conversion select bit	—

Register	Bit	RX63N (S12ADa)	RX64M (S12ADC)
ADEXICR	TSSA	—	Temperature sensor output A/D conversion select bit
	OCS	Internal reference voltage A/D-converted select bit	—
	OCSA	—	Internal reference voltage A/D conversion select bit
	TSSB	—	Temperature sensor output A/D conversion select bit
	OCSB	—	Internal reference voltage A/D conversion select bit
	EXSEL[1:0]	—	Extended analog input select bits
	EXOEN	—	Extended analog output control bit
ADSSTR01	—	A/D sampling state register 01	Extended analog input select bits
ADSSTR23	—	A/D sampling state register 23	—
ADSSTR0	—	—	A/D sampling state register 0
ADSSTR1	—	—	A/D sampling state register 1
ADSSTR2	—	—	A/D sampling state register 2
ADSSTR3	—	—	A/D sampling state register 3
ADSSTR4	—	—	A/D sampling state register 4
ADSSTR5	—	—	A/D sampling state register 5
ADSSTR6	—	—	A/D sampling state register 6
ADSSTR7	—	—	A/D sampling state register 7
ADSSTRL	—	—	A/D sampling state register L
ADSSTRT	—	—	A/D sampling state register T
ADSSTRO	—	—	A/D sampling state register O
ADSHCR	—	—	A/D sample-and-hold circuit control register
ADDISCR	—	—	A/D disconnection detection control register
ADGSPCR	—	—	A/D group scan priority control register
ADCMPCR	—	—	A/D compare control register
ADCMPANSR0	—	—	A/D compare channel select register 0
ADCMPANSR1	—	—	A/D compare channel select register 1
ADCMPANSER	—	—	A/D compare select extended register
ADCMPLR0	—	—	A/D compare level register 0
ADCMPLR1	—	—	A/D compare level register 1
ADCMPLER	—	—	A/D compare level extended register
ADCMPDR0	—	—	A/D compare data register 0
ADCMPDR1	—	—	A/D compare data register 1
ADCMPSR0	—	—	A/D compare status register 0
ADCMPSR1	—	—	A/D compare status register 1
ADCMPSER	—	—	A/D compare status extended register

2.23 D/A Converter

Table 2.40 shows a comparative overview of the D/A converter specifications, and Table 2.41 shows a comparative listing of the D/A converter registers.

Table 2.40 Comparative Overview of D/A Converter

Item	RX63N (DAa)	RX64M (R12DA)
Resolution	10 bits	12 bits
Output channel	2 channels	2 channels
Measure against mutual interference between analog modules	Measure against interference between D/A and A/D conversion: D/A converted data update timing is controlled by the 10-bit A/D converter synchronous D/A conversion enable input signal output by the the 10-bit A/D converter. (Degradation of A/D conversion accuracy caused by interference is reduced by controlling the D/A converter inrush current generation timing with the enable signal.)	Measure against interference between D/A and A/D conversion: D/A converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable input signal output by the the 12-bit A/D converter (unit 1). Degradation of 12-bit A/D conversion accuracy caused by interference is reduced by controlling the D/A converter inrush current generation timing with the enable signal.
Low power consumption function	It is possible to specify the module stop state.	It is possible to specify the module stop state.
Event link function (input)	—	Ability to activate DA0 by event signal input
D/A output mode switching	—	Switchable between output amplifier and output amplifier though output

Table 2.41 Comparative Listing of D/A Converter Registers

Register	Bit	RX63N (DAa)	RX64M (R12DA)
DAAMPCR	—	—	D/A output amplifier control register
DAADUSR	—	—	D/A-A/D sync unit select register

2.24 Temperature Sensor

Table 2.42 shows a comparative overview of the temperature sensor specifications, and Table 2.43 shows a comparative listing of the temperature sensor registers.

Table 2.42 Comparative Overview of Temperature Sensor

Item	RX63N	RX64M
Temperature sensor voltage output	Output to 12-bit A/D converter	Output to 12-bit A/D converter (unit 1)
Low power consumption function	It is possible to specify the module stop state.	It is possible to specify the module stop state.
Temperature sensor calibration data registers	When shipped from the factory the registers contain temperature sensor calibration data based on measurement of each individual chip.	—

Table 2.43 Comparative Listing of Temperature Sensor Registers

Register	Bit	RX63N	RX64M
TSCDRH	—	Temperature sensor calibration data register	—
TSCDRL	—	Temperature sensor calibration data register	—

2.25 RAM

Table 2.44 shows a comparative overview of the RAM specifications, and Table 2.45 shows a comparative listing of the RAM registers.

Table 2.44 Comparative Overview of RAM

Item	RX63N	RX64M	
		No ECC Error Correction	ECC Error Correction (ECCRAM)
RAM capacity	• 64 KB RAM0: 64 KB • 128 KB RAM0: 64 KB, RAM1: 64 KB • 192 KB RAM0: 64 KB, RAM1: 128 KB • 256 KB RAM0: 64 KB, RAM1: 192 KB	• 512 KB RAM0: 512 KB	32 KB
RAM address	• When the RAM capacity is 64 KB RAM0: 0000 0000h to 0000 FFFFh (64 KB) RAM1: None • When the RAM capacity is 128 KB RAM0: 0000 0000h to 0000 FFFFh (64 KB) RAM1: 0001 0000h to 0001 FFFFh (64 KB) • When the RAM capacity is 192 KB RAM0: 0000 0000h to 0000 FFFFh (64 KB) RAM1: 0001 0000h to 0002 FFFFh (128 KB) • When the RAM capacity is 256 KB RAM0: 0000 0000h to 0000 FFFFh (64 KB) RAM1: 0001 0000h to 0003 FFFFh (192 KB)	RAM0: 0000 0000h to 0007 FFFFh	ECCRAM: 00FF 8000h to 00FF FFFFh
Access	• Single-cycle access is possible for both reading and writing. • The RAM can be enabled or disabled.	• Single-cycle access is possible for both reading and writing. • The RAM can be enabled or disabled.	• Without ECC error correction: Access is done in two cycles for both reading and writing. • With ECC error correction (when no error has occurred): Access is done in two cycles for both reading and writing.

Item	RX63N	RX64M	
		No ECC Error Correction	ECC Error Correction (ECCRAM)
Access			• With ECC error correction (when an error has occurred): Access is done in two cycles for both reading and writing. • The RAM can be enabled or disabled.
Data retention function	Data in RAM0 can be retained in deep software standby mode.	Data is not retained in deep software standby mode. (Data can be retained in standby RAM.)	Data is not retained in deep software standby mode. (Data can be retained in standby RAM.)
Low power consumption function	The module-stop state is independently selectable for RAM0 and RAM1.	It is possible to specify the module stop state.	It is possible to specify the module stop state.
Error checking function	None	None	• Correction of 1-bit errors and detection of 2-bit errors • Generation of non-maskable interrupt or interrupt when an error occurs

Table 2.45 Comparative Listing of RAM Registers

Register	Bit	RX63N	RX64M
SYSCR1*	ECCRAME	—	ECCRAM enable bit
	SBYRAME	—	Standby RAM enable bit
ECCRAMMODE	—	—	ECCRAM operating mode control register
ECCRAM2STS	—	—	ECCRAM 2-bit error status register
ECCRAM1STSEN	—	—	ECCRAM 1-bit error information update enable register
ECCRAM1STS	—	—	ECCRAM 1-bit error status register
ECCRAMPRCR	—	—	ECCRAM protect register
ECCRAM2ECAD	—	—	ECCRAM 2-bit error address capture register
ECCRAM1ECAD	—	—	ECCRAM 1-bit error address capture register
ECCRAMPRCR2	—	—	ECCRAM protect register 2
ECCRAMETST	—	—	ECCRAM test control register

Note: * See the Operating Modes section of RX64M Group User's Manual: Hardware for a description of ECCRAME and SBYRAME.

2.26 Flash Memory

Table 2.46 shows a comparative listing of the flash memory specifications, and Table 2.47 shows a comparative listing of the flash memory registers.

Table 2.46 Comparative Listing of Flash Memory Specifications

	RX63N		RX64M	
Item	**ROM**	**E2 Data Flash**	**Code Flash Memory**	**Data Flash Memory**
Memory space	• User area: Maximum 2 MB • User boot area: 16 KB	Data area: 32 KB	• User area: Maximum 4 MB • User boot area: 32 KB	Data area: 64 KB
Read cycle	High-speed read operation using 1 cycle of ICLK is supported.	A read operation takes six cycles of FCLK for word or byte access.	High-speed read operation using 1 cycle of ICLK is supported.	A read operation takes eight cycles of FCLK for word or byte access.
Value after erase	FFh	Undefined value	FFh	Undefined value
Programming/ erasing method	• On-chip dedicated sequencer (FCU) for programming the ROM and E2 data flash • Programming and erasing the ROM and E2 data flash by issuing commands to the FCU		• Programming and erasing the code flash memory and data flash memory can be accomplished with FACI commands specified in the FACI command generation area (007E 0000h). • Programming (serial programming) can be accomplished by a dedicated flash memory programmer via serial interface communication. • Programming of the flash memory can be accomplished with a program written by the user (self-programming).	
Security function	Prevents unauthorized modification or reading of data.		Prevents unauthorized modification or reading of data.	
Protection function	Prevents unintentional programming of the flash memory.		Prevents unintentional programming of the flash memory.	
Trusted Memory (TM)	—		Prevents unauthorized reading of blocks 8 and 9 in the code flash memory.	
Background operation (BGO) function	Data can be read from the ROM while the E2 data flash is being programmed.		• The code flash memory can be read while the data flash memory is being programmed. • The code flash memory can be read while the code flash memory is being programmed (with limitations on the combinations of address ranges in which reading and writing occur).	
Units of programming and erasure	• Programming the user area and user boot area: 128 bytes • Erasing the user area: One block • Erasing the user boot area: 16 KB	• Programming the data area: 2 bytes • Erasing the data area: 32 bytes	• Programming the user area and user boot area: 256 bytes • Erasing the user area: One block • Erasing the user boot area: 32 KB	• Programming the data area: 4 bytes • Erasing the data area: 64 bytes

Item	RX63N		RX64M	
	ROM	**E2 Data Flash**	**Code Flash Memory**	**Data Flash Memory**
Other functions	Ability to accept interrupts during self-programming		Ability to accept interrupts during self-programming	
	Ability to specify initial settings for the microcontroller in option-setting memory		Ability to specify initial settings for the microcontroller in option-setting memory	
On-board programming (four types)	• Programming in boot mode — The asynchronous serial interface (SCI1) is used. — The communication speed is adjusted automatically. — The user boot area can also be programmed. • Programming in USB boot mode — USB0 is used. — Dedicated hardware is not required, so direct connection to a PC is possible. • Programming in user boot mode — Users can create their own boot programs. • Programming by a routine for ROM or E2 data flash programming within the user program — This allows ROM and E2 data flash programming without resetting the system.		• Programming in boot mode (SCI interface) — The asynchronous serial interface (SCI1) is used. — The communication speed is adjusted automatically. — The user boot area can also be programmed. • Programming in USB boot mode — USBb is used. — Dedicated hardware is not required, so direct connection to a PC is possible. • Programming in user boot mode — Users can create their own boot programs. • Programming by a routine for code flash memory or data flash memory programming within the user program — This allows programming of the code flash memory or data flash memory without resetting the system.	
Off-board programming (products with 100 pins or more)	A flash programmer can be used to program the user area and user boot area.	A flash programmer cannot be used to program the data area.	A flash programmer can be used to program the user area and user boot area.	A flash programmer cannot be used to program the data area.

Table 2.47 Comparative Listing of Flash Memory Registers

Register	Bit	RX63N	RX64M
FWEPROR	FLWE[1:0]	Flash programming/erasure bits	Flash write/erase bits
FMODR	—	Flash mode register	—
FASTAT	DFLWPE	E2 data flash programming/erasure protection violation flag	—
	ECRCT	—	Error flag
	DFLRPE	E2 data flash read protection violation flag	—
	DFLAE	E2 data flash access violation flag	—
	DFAE	—	Data flash memory access violation flag
	CMDLK	FCU command lock flag	Command lock flag
	ROMAE	ROM access violation flag	—
	CFAE	—	Code flash memory access violation flag
FAEINT	DFLWPEIE	E2 data flash programming/erasure protection violation interrupt enable bit	—
	ECRCTIE	—	Error interrupt enable bit
	DFLRPEIE	E2 data flash read protection violation interrupt enable bit	—
	DFLAEIE	E2 data flash access violation interrupt enable bit	—
	DFAEIE	—	Data flash memory access violation interrupt enable bit
	CMDLKIE	FCU command lock interrupt enable bit	Command lock interrupt enable bit
	ROMAEIE	ROM access violation interrupt enable bit	—
	CFAEIE	—	Code flash memory access violation interrupt enable bit
DFLRE0	—	E2 data flash read enable register 0	—
DFLRE1	—	E2 data flash read enable register 1	—
DFLWE0	—	E2 data flash P/E enable register 0	—
DFLWE0	—	E2 data flash P/E enable register 1	—
FSADDR	—	—	FACI command processing start address register
FEADDR	—	—	FACI command processing end address register
FCURAME	FRAMTRAN	—	FCURAM transfer mode bit
FSTATR0	—	Flash status register 0	—
FSTATR1	—	Flash status register 1	—
FSTATR	—	—	Flash status register
FENTRYR	FENTRY0	ROM P/E mode entry bit 0	—
	FENTRYC	—	Code flash P/E mode entry bit
	FENTRY1	ROM P/E mode entry bit 1	—
	FENTRY2	ROM P/E mode entry bit 2	—
	FENTRY3	ROM P/E mode entry bit 3	—
	FENTRYD	E2 data flash P/E mode entry bit	Data flash P/E mode entry bit
	FEKEY[7:0]	Key code	—
	KEY[7:0]	—	Key code bits

Register	Bit	RX63N	RX64M
FPROTR	FPKEY[7:0]	Key code	—
	KEY[7:0]	—	Key code bits
FRESETR	—	Flash reset register	—
FSUINITR	—	—	Flash sequencer setting initialization register
FLKSTAT	—	—	Lock bit status register
FCMDR	—	FCU command register	FACI command register
FCPSR	—	FCU processing switching register	Flash sequencer processing switching register
DFLBCCNT	—	E2 data flash blank check control register	—
FPESTAT	—	P/E error status bits	P/E error status flag
DFLBCSTAT	—	E2 data flash blank check status register	—
FBCCNT	—	—	Data flash blank check control register
FBCSTAT	—	—	Data flash blank check status register
FPSADDR	—	—	Data flash write start address register
PCKAR	—	Peripheral clock notification register	—
FPCKAR	—	—	Flash sequencer processing clock notification register
UIDRn*	—	Unique ID register n	—

Note: * Implemented on G product versions only.

3. Reference Documents

User's Manual: Hardware

RX63N Group, User's Manual: Hardware Rev.1.80 (R01UH0041EJ0180)
(The latest version can be downloaded from the Renesas Electronics website.)

RX64M Group User's Manual: Hardware Rev.1.00 (R01UH0377EJ0100)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News
(The latest version can be downloaded from the Renesas Electronics website.)

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Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Apr. 04, 2014	—	First edition issued
1.01	Oct. 26, 2015	—	Application note amended to reflect updates to user's manuals
		2, 3	Table 1.1 amended
		4	2.1 Operating Modes added 2.2 Option-Setting Memory added
		6	Table 2.4 amended
		7 to 9	Table 2.5 amended
		9	Table 2.6 amended
		11, 12	Table 2.8 amended
		13 to 15	Table 2.9 amended
		17	2.7 Memory Protection Unit added
		18, 19	Table 2.12 amended
		19	2.9 I/O Ports added 2.10 Multi-Function Pin Controller added
		20, 21	Table 2.16 amended
		22 to 24	Table 2.17 amended
		28, 29	2.13 8-Bit Timer added
		29	2.14 Compare Match Timer added
		30, 31	Table 2.23 amended
		32	Table 2.26 amended
		33, 34	Table 2.27 amended
		35	Table 2.28 amended
		36, 37	Table 2.29 amended
		38 to 40	Table 2.30 amended
		41	Table 2.32 amended
		42, 43	Table 2.33 amended
		46	Table 2.36 amended
		47	2.21 Parallel Data Capture Unit added
		48 to 51	Table 2.38 amended
		52, 53	Table 2.39 amended
		55	2.24 Temperature Sensor added
		56, 57	Table 2.44 amended
		58	Table 2.45 amended
		60, 61	Table 2.47 amended
		62	3. Reference Documents amended

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to a product with a different type number, confirm that the change will not lead to problems.
   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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