
RX Family

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Specification Differences Between the RSPI and SCI (Simple SPI Mode) and Selection Guide

Abstract

This document describes the specification differences between the serial peripheral interface (RSPI) and simple SPI mode (simple SPI) of the serial communications interface (SCI) and also describes the procedure to select whether to use the RSPI or simple SPI.

Products

RX Family *¹

Note 1. The RX610, RX62N, RX621, RX62T, and RX62G Groups do not have the simple SPI.

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1. Specifications

Table 1.1 lists the Specification Differences Between the RSPI and Simple SPI. Some specifications vary depending on the product.

Table 1.1 Specification Differences Between the RSPI and Simple SPI

Item		RSPI	Simple SPI
Bit rate *1	Master	Maximum 25 Mbps	Maximum 12.5 Mbps
	Slave	Maximum 6.25 Mbps	Maximum 6.25 Mbps
Transfer function	Clock polarity	Selectable	Selectable
	Clock phase	Selectable	Selectable
Data format	MSB first/ LSB first	Selectable	Selectable
	Transfer bit length	Selectable from 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32	8 bits fixed
	Transmit/ receive buffer	32 bits × 4-stage buffer	8 bits × 1-stage buffer
	Shift register	32 bits	8 bits
	Maximum frames	4 frames	1 frame
	Parity	Whether or not to add a parity bit can be selected.	Parity bit cannot be added.
Slave select pin output control		Hardware control with the dedicated pin	Software control with the general port
Pin control when a mode fault occurs		Place pins PSPCK and MOSI in high-impedance to release the SPI bus	Place pins SCK and SMOSI in high-impedance to release the SPI bus
Error detection	Overrun	Detectable	Detectable
	Mode fault	Detectable	Detectable
	Parity	Detectable	Not detectable
Interrupt sources		Receive buffer full, transmit buffer empty, mode fault, overrun, parity error, RSPI idle	Receive data full, transmit data empty, receive error, transmit end

Note 1. The specifications vary depending on the product. Refer to the Timing of On-Chip Peripheral Modules section in the Electrical Characteristics chapter of the corresponding User's Manual: Hardware.

2. Reference Application Note

For additional information associated with this document, refer to the following application note.

- RX Family RSPI Sequence Control and Interrupt Generation Timing (R01AN1105EJ)

3. Flowchart for Selecting the SPI Module

Figure 3.1 shows a flowchart for selecting the recommended SPI module based on the differences between the RSPI and simple SPI in the RX63N Group. Some specifications vary with the product.

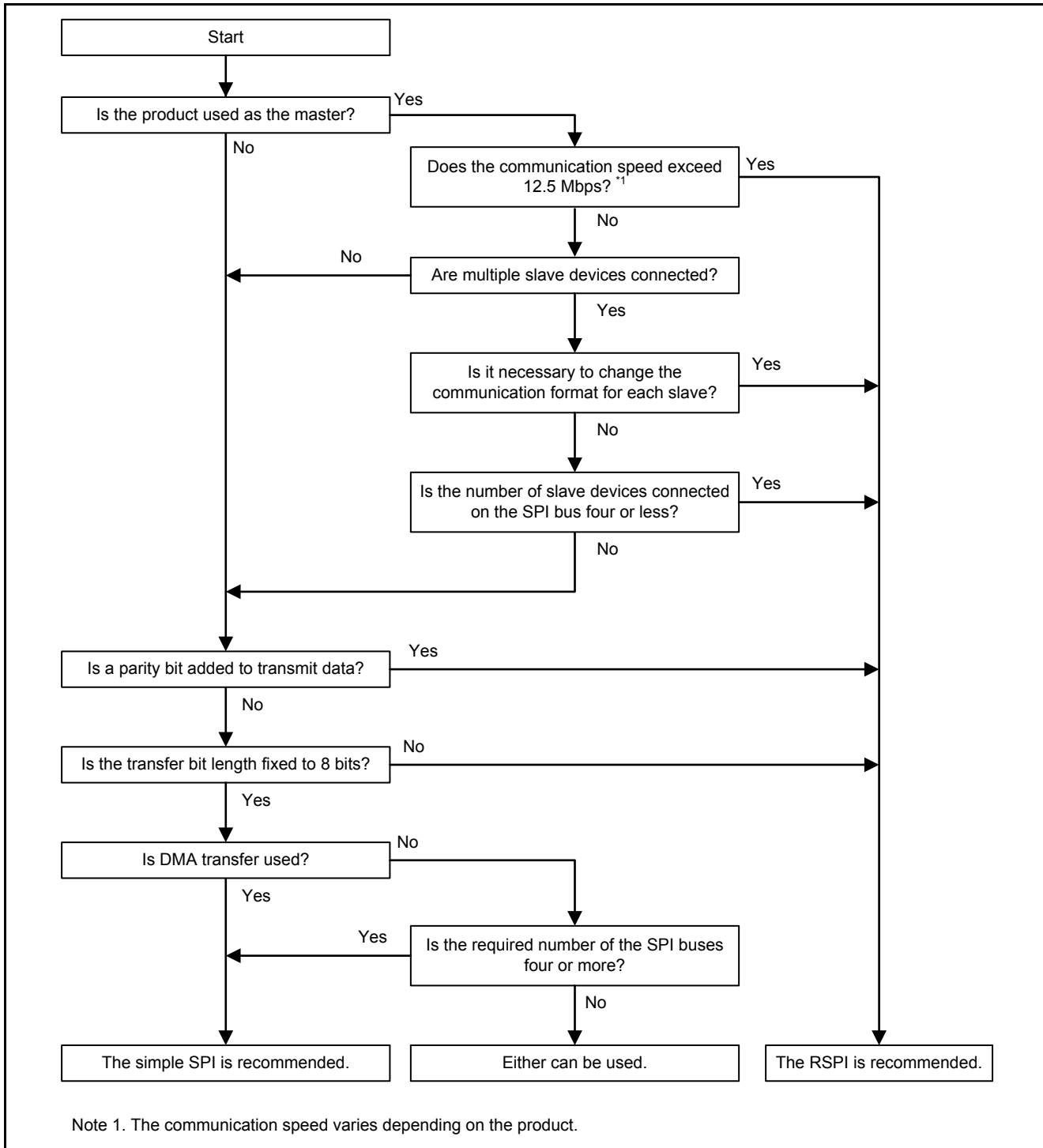


Figure 3.1 Selecting the SPI Module

4. Reference Documents

User's Manual: Hardware

RX63N Group, RX631 Group User's Manual: Hardware Rev.1.80 (R01UH0041EJ)

The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

User's Manual: Development Tools

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REVISION HISTORY	RX Family Application Note Specification Differences Between the RSPI and SCI (Simple SPI Mode) and Selection Guide
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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

- The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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SALES OFFICES

Renesas Electronics Corporation

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Renesas Electronics America Inc.

2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited

1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH

Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.

Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.

Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited

Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.

13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.

80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jin Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.

12F., 234 Teheran-ro, Gangnam-Ku, Seoul, 135-920, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141