RX Family

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Mar 31, 2017

PTP Synchronous Pulse Output Using Firmware Integration Technology Modules

Introduction

This document explains one of the EPTPC FIT (Firmware Integration Technology) module [1] usage examples. This example outputs the pulses synchronous with the PTP (Precision Time Protocol) defined by the IEEE1588-2008 specification [2].

Target Device

This API supports the following device.

- RX64M Group
- RX71M Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Overview

This document explains one of the typical usage examples of the EPTPC FIT module (hereafter PTP driver). This example outputs the two positive and negative PWM (Pulse Width Modulation) pulses with duty 50%. The pulse output nodes are synchronous with the PTP and start the creation of pulses when the time of each nodes coincidence with the specified time set by user. Thereafter, those nodes continue to output the pulses to the general ports (I/O Ports) via Event Link Controller (ELC) without CPU operation. The period and width of the pulse outputted from each node are corrected based on the synchronous time. Users can apply those synchronous PWM pulse output method to their own systems.

1.1 PTP Synchronous Pulse Output Using FIT Modules

This module is implemented in a project and used as the application example of the PTP driver.

1.2 Related documents

[1] RX Family EPTPC Module Using Firmware Integration Technology, Rev.1.13, Document No. R01AN1943EJ0113, Mar 31, 2017

[2] IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems, Revision of IEEE Std 1588-2008, Mar 2008

[3] RX Family Ethernet Module Using Firmware Integration Technology, Rev.1.12, Document No. R01AN2009EJ0112, Nov 11, 2016

[4] RX64M Group Renesas Starter Kit+ User's Manual For e^2 studio, Rev. 1.10, Document No. R20UT2593EG0110, Jun 25, 2015

[5] RX71M Group Renesas Starter Kit+ User's Manual, Rev. 1.00, Document No. R20UT3217EG0100, Jan 23, 2015

1.3 Terms and Abbreviations

Please refer to EPTPC FIT module application note (Sec.1.3) [1].

1.4 Hardware Structure

The Ethernet peripheral modules of the RX64M/71M group are composed of the EPTPC, the PTP Host interface peripheral module (PTPEDMAC), dual channel Ethernet MAC ones (ETHERC (CH0), ETHERC (CH1)) and dual channel Ethernet Host interface ones (EDMAC (CH0), EDMAC (CH1)). The EPTPC is divided to PTP Frame Operation (CH0) part, PTP Frame Operation (CH1) part, Packet Relation Control part and Statistical Time Correction Algorithm part from their functionality. The EPTPC is also connected to the general ports (I/O ports) and motor control timers (MTU3 and GPT peripheral modules) via ELC peripheral module to output synchronous pulses.

Figure 1.1 shows the related hardware's block diagram and the green arrows and parts indicate the connection and using parts respectively in this example.

In detail, please refer to RX64M/71M Group User's Manual: Hardware.

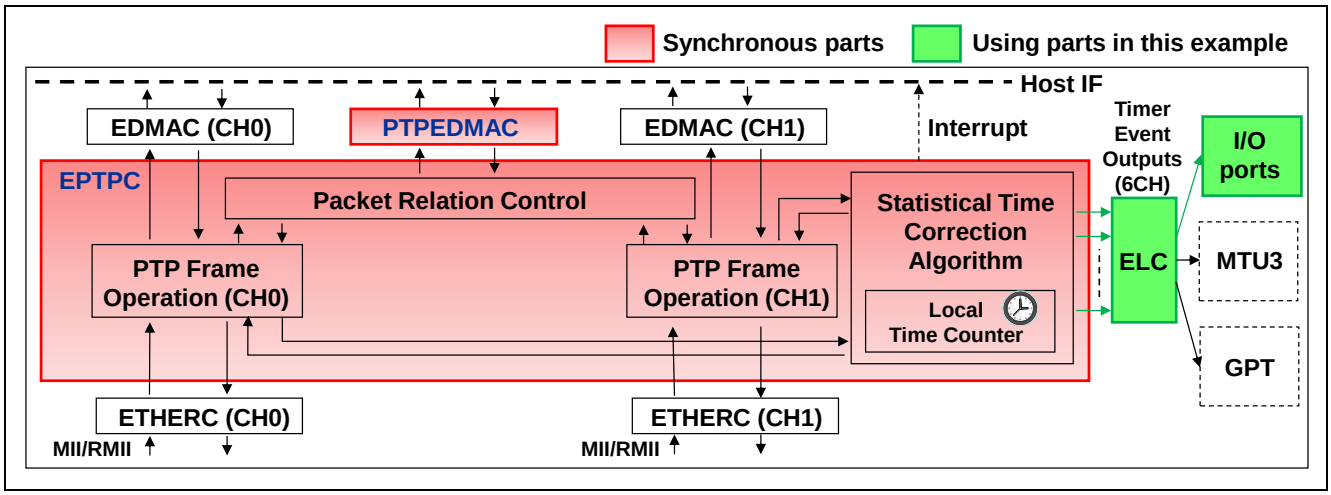

Figure 1.1 Hardware block diagram

1.5 Software Structure

This sample is operations example of the application layer applied to plural FIT modules. Those operations are to set a PTP configuration such as MAC address, IP address, the kind of Clock[1], Master or Slave and delay mechanism (P2P or E2E) to the PTP driver, set the pulses parameter such as the specific pulse output start time, period and width to the PTP driver, set an event link connection between EPTPC and I/O ports to the ELC driver, set I/O ports initial setting to the I/O ports driver, and control the PTP protocol sequences using the PTP driver and Ethernet FIT module (hereafter Ether driver [3]). The PTP driver always should be used with Ether driver. TCP/IP middle ware does not include in this example. Therefore, user needs to implement TCP/IP middle ware when this example applied to the TCP/IP system. Figure 1.2 shows the software structure of this sample.

[1] This example supports only OC (not support BC and TC).

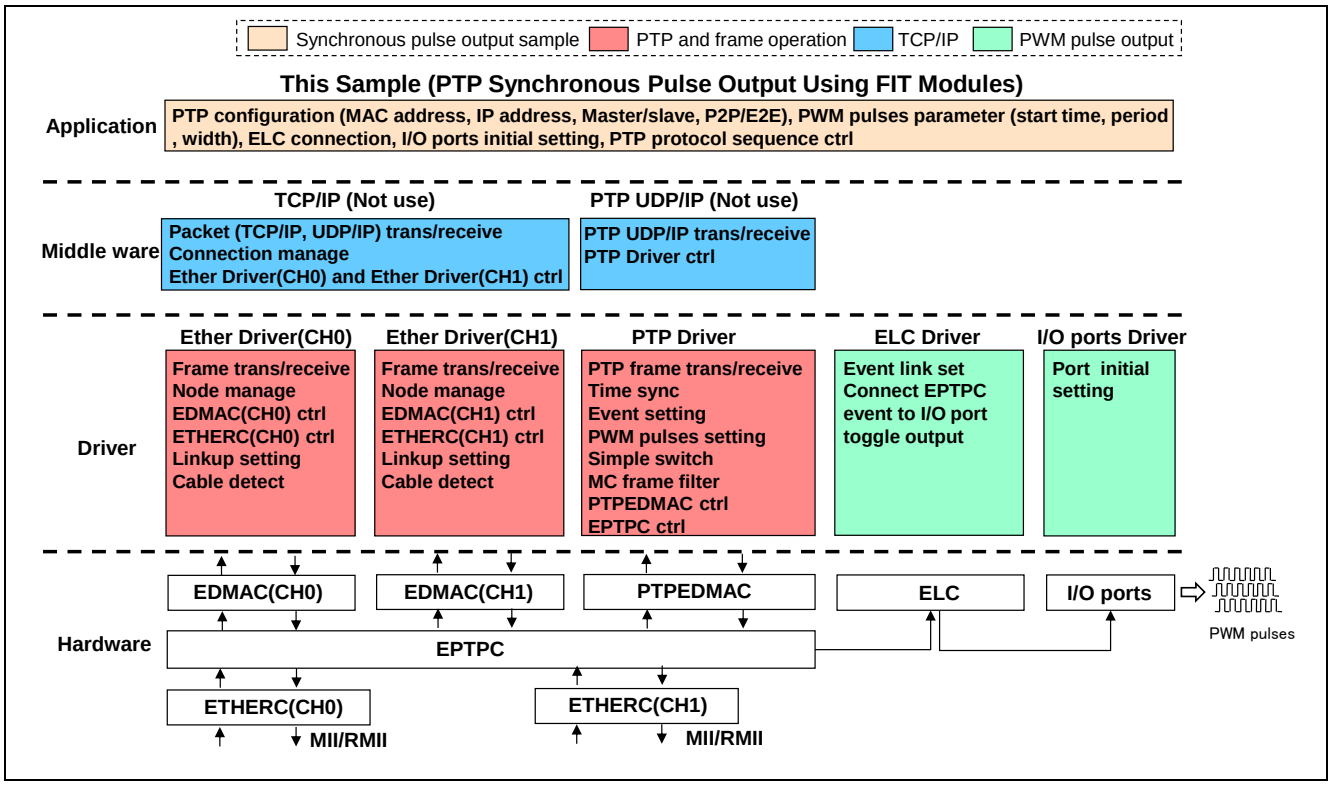

Figure 1.2 Software structure of this sample

1.6 File Structure

This sample codes are stored in the “demo_src” and lower hierarchical folders. ELC and I/O ports drivers are stored each driver folders respectively. Figure 1.3 shows the file structure of this sample. As for other FIT based modules include the PTP driver FIT module, please refer to the documentation of the each FIT module.

```
demo_src: main operation and configuration
|   sample_main.c
|   sample_main.h
|
+ --- usr: LED control
|       led.c
|       led.h
|
+ --- sync: PTP synchronize operation
|       sync.c
|       sync.h
|
r_bsp: BSP (Board Support Package) FIT module
|
r_config: configuration setting of FIT modules
|       r_bsp_config.h
|       r_bsp_interrupt_config.h
|       r_ether_rx_config.h
|       r_ptp_rx_config.h

r_elc_rx: ELC driver folder
|   r_elc_rx_if.h ;ELC driver header file
|
+ --- src:
|       r_elc.c ;ELC driver source file
|
r_ether_rx: Ethernet  Driver FIT module
|
r_io_rx: I/O ports driver folder
|   r_io_rx_if.h ;I/O ports driver header file
|
+ --- src:
|       r_io.c ;I/O ports driver source file
|
r_ptp_rx: PTP Driver  FIT module
|
```

Figure 1.3 File structure of this example

2. Functional Information

This example is developed by the following principles.

2.1 Hardware Requirements

This driver requires your MCU supports the following feature:

- EPTPC
- PTPEDMAC
- ETHERC
- EDMAC
- ELC
- I/O Ports

2.2 Hardware Resource Requirements

This section details the hardware peripherals that this example requires. Unless explicitly stated, these resources must be reserved for the following driver, and the user cannot use them.

2.2.1 EPTPC Channel

This example uses the EPTPC. This resource needs to the synchronization based on the PTP and create synchronous PWM waves.

2.2.2 ETHERC Channel

This example uses the ETHEC (CH0) or ETHEC (CH1). Those resources need to the Ethernet MAC operations.

2.2.3 EDMAC Channel

This example uses the EDMAC (CH0) or EDMAC (CH1). Those resources need to the CPU Host interface of standard Ethernet frame operations.

2.2.4 ELC

This example uses the ELC to connect events between EPTPC and I/O ports. This resource needs to output the pulses synchronously.

2.2.5 I/O Ports

This example uses the I/O ports for the synchronous PWM output. Please do not modify the settings or try to use the peripheral during driver operations.

2.3 Software Requirements

This example depends on the following packages (FIT modules):

- r_bsp
- r_ether_rx
- r_ptp_rx

2.4 Supported Toolchains

This example is tested and works with the following toolchain:

- Renesas RX Toolchain v2.06.00

2.5 Header Files

Each functions call are accessed by including a single file, *sample_main.h, sync.h, led.h, r_elc_rx_if.h or r_io_rx_if.h* which is supplied with this driver's project code.

2.6 Integer Types

This project uses ANSI C99. These types are defined in *stdint.h*.

2.7 Configuration Overview

The configuration options in this project are specified in *sample_main.h.* The option names and setting values are listed in the table below.

Configuration options	
#define DEVICE_ID **- Default value = 0**	Set the device id number of the demo.
#define MODE_PORT **- Default value = 1**	Specify the kind of clock. - When this is set to 0, clock is OC port0. - When this is set to 1, clock is OC port1. BC and TC are not supported in this sample. If select OC port0, please set "ETHER_CFG_CH0/1_PHY_ACCESS = 0" in the r_ether_rx_config.h. If select OC port1, please set "ETHER_CFG_CH0/1_PHY_ACCESS = 1" in the r_ether_rx_config.h.
#define MS_PORT0/1 **- Default value = 0**	Select Master or Slave for port0/port1 - When this is set to 0, clock is Master. - When this is set to 1, clock is Slave.
#define SYNC_PORT0/1 **- Default value = 1**	Select the delay mechanism (P2P or E2E) for port0/port1 - When this is set to 0, the delay mechanism is P2P. - When this is set to 1, the delay mechanism is E2E.
#define PLS_CH0/1 **- Default value = 0 (1st pulse)** **- Default value = 1 (2nd pulse)**	Select the channel of pulse output timer for 1st pulse/2nd pulse. - Set 0 to 5 Please set the different channel between 1st pulse and 2nd pulse each other.
#define PLS_CYC0/1 **- Default value = 400000 (1st pulse)** **- Default value = 100000 (2nd pulse)**	Set the pulse period for 1st/2nd pulse in the nanosecond unit. Half of this value is set to the pulse setting function (=R_PTP_Tmr_Set) of the PTP driver and the registers (=TMCYCRm) of the EPTPC. Please keep in mind the resolution of the pulse period is 50nsec due to STCA clock one. In detail, please refer to RX64M /71M Group User's manual (Sec.36.2.27).
#define PLS_HW0/1 **- Default value = 200000 (1st pulse)** **- Default value = 50000 (2nd pulse)**	Set the pulse high width for 1st/2nd pulse in the nanosecond unit. Half of this value is set to the pulse setting function (=R_PTP_Tmr_Set) of the PTP driver and the registers (=TMPLSRm) of the EPTPC. Please keep in mind the resolution of the pulse high width is 50nsec due to STCA clock one. In detail, please refer to RX64M /71M Group User's manual (Sec.36.2.28).
#define TIMER_EDGE **- Default value = 0**	Select the rise or fall edge of ELC event signal trigger. - When this is set to 0, rising edge is selected. - When this is set to 1, falling edge is selected. This setting is common to 1st and 2nd pulses.
#define MAC_ADDR_1H/2H **- Default value = 0x00007490**	Set the Ethernet MAC address upper 16 bits for port0/port1. The lower 16 bits of default value are set the upper 16bits of the Renesas vendor ID (=74-90-50). The upper 16 bits of default value are reserved field and should be set 00-00. Please change this value when users applied to this sample their own system.
#define MAC_ADDR_1H/2H	Set the Ethernet MAC address lower 32 bits for port0/port1.

Configuration options	
Case of device id = 0, **- Default value = 0x5000791D (port0)** **- Default value = 0x5000791E (port1)** **Case of device id = 1,** **- Default value = 0x5000791F (port0)** **- Default value = 0x50007920 (port1)** **Case of device id = 2,** **- Default value = 0x50007921 (port0)** **- Default value = 0x50007922 (port1)**	The upper 8 bits of default value are set the lower 8bits of the Renesas vendor ID (=74-90-50). The lower 24 bits of default value are set the unique value for this sample. Please change this value when users applied to this sample their own system.
#define IP_ADDR_1/2 **Case of device id = 0,** **- Default value = 0x06070809 (port0)** **- Default value = 0x16171819 (port1)** **Case of device id = 1,** **- Default value = 0x26272829 (port0)** **- Default value = 0x36373839 (port1)** **Case of device id = 2,** **- Default value = 0x46474849 (port0)** **- Default value = 0x56575859 (port1)**	Set the IP (IPv4) address for port0/port1. Please change this value when users applied to this sample their own system.
#define PULSE_START_H/L **- Default value = 0x00000007 (High)** **- Default value = 0x037F7915 (Low)**	Set the pulse start time in the nanosecond unit. The default value equals to 30,123,456,789 nsec. PULSE_START_H and PULSE_START_L are higher 32bits and lower 32bits respectively. This setting is common to 1st and 2nd pulses. Please keep in mind those setting value should be after local clock counter initial value.

2.8 Data Structures

No specific data structure exists in this sample.

2.9 Return Values

This section describes return values of the functions of this example. Those return values are located in *r_elc_rx_if.h* and *r_io_rx_if.h* as the prototype declarations.

```
/* ELC driver return value */
ELC_OK (0) /* No error */
ELC_ERROR (-1) /* General error */
```

```
/* I/O Ports driver return value */
IO_OK (0) /* No error */
IO_ERROR (-1) /* General error */
```

3. Specification of This Example

3.1 Outline of Functions

The function of this example shows Table 3.1.

Table 3.1 Function of This Example

Item	Contents
main()	Main operation of this sample.
ReadPTPMsg()	Read PTP messages. If announce message is received, update Master port identity.
led_init()	Initialize user LED.
led_ctrl()	Update user LED pattern
R_ELC_Init()	Initialize ELC (start ELC).
R_ELC_Set_Timer_Event()	Connect EPTPC timer event to IO port (PE0/PE1) toggle output event.
R_ELC_Ctr_Timer_Event()	Enable/disable EPTPC timer event.
R_IO_Init()	Initialize IO port (PE0/PE1).

3.2 Environment and Execution

Execution of this example needs RX64M/71M RSK boards[1] more than two (Master node and more than one Slave node), an Ethernet Hub (hereafter HUB), an Ethernet cable and an Oscilloscope. The synchronous pulse output pin of the each RX64M/71M RSK boards connects the input of the oscilloscope. The outline of the execution sequence is following.

- Write the sample project execution code to all RX64M/71M RSK boards (hereafter RSK boards).
- Connect all RSK boards one another via the Hub by the Ethernet cable.
- Connect the synchronous pulse output pins of each RSK board to oscilloscope.
- Power on the all RSK boards and other devices.
- When the RSK boards finishes Ethernet, I/O ports and ELC driver initialization and open process, the user LED composed of LED0, LED1, LED2 and LED3 shows the all-on pattern (LED0: ON, LED1: ON, LED2: ON, LED3: ON).
- Push the SW1 switch. Each clock (RSK board) initializes and open PTP driver with setting the output pulses features such as start time, period and width.
- When each clock starts the synchronization without any error, the user LED shows the even pattern (LED0: ON, LED1: OFF, LED2: ON, LED3: OFF).
- Each clock outputs the pulses from I/O ports (PE0 and PE1) via ELC when the local clock counter synchronized of the EPTPC compares matches the timer start time whose field is composed of higher and lower 32 bits of nanosecond order field (=TMSTTRUm and TMSTTRLm)[2].
- User can observe the synchronous pulses.
- If any error occurred during this operation, this example finishes with the odd pattern (LED0: OFF, LED1: ON, LED2: OFF, LED3: ON) of the user LED.

[1] Product name is a Renesas Starter Kit+ for RX64M [4] or a Renesas Starter Kit+ for RX71M [5].

[2] The index “m” indicates pulse output timer channel from 0 to 5.

Figure 3.1 shows the environment using two board configuration.

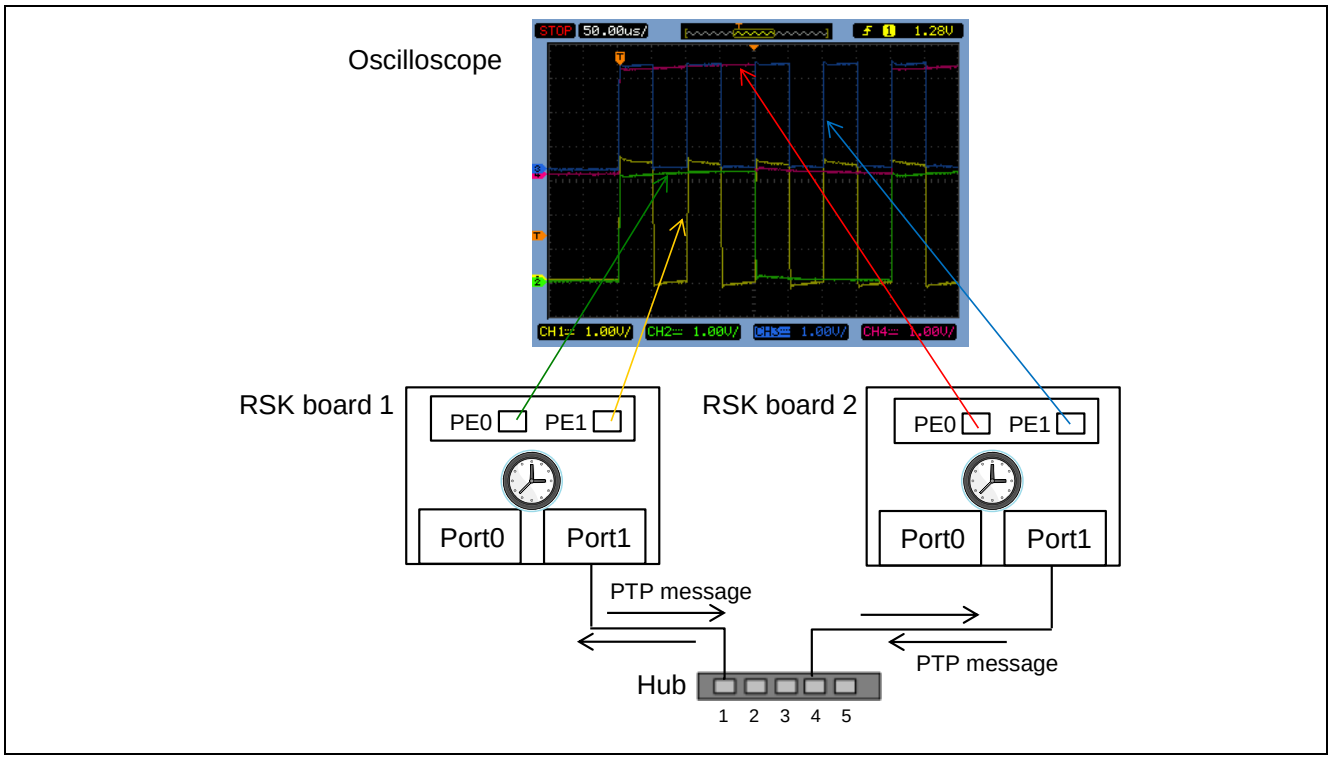

Figure 3.1 Environment (two board configuration)

Figure 3.2, Figure 3.3, Figure 3.4 and Figure 3.5 show the software flow overview. Figure 3.2 describes the initial setting of related peripheral modules such as ETERC, EDMAC, EPTPC, ELC, I/O Ports and so on. Figure 3.3 describes the operation to enable Ether communication including PTP message frames. Figure 3.4 describes the operation executed after PTP message receive interrupt occurrence. Figure 3.5 describes the operation executed after timer event interrupt occurrence.

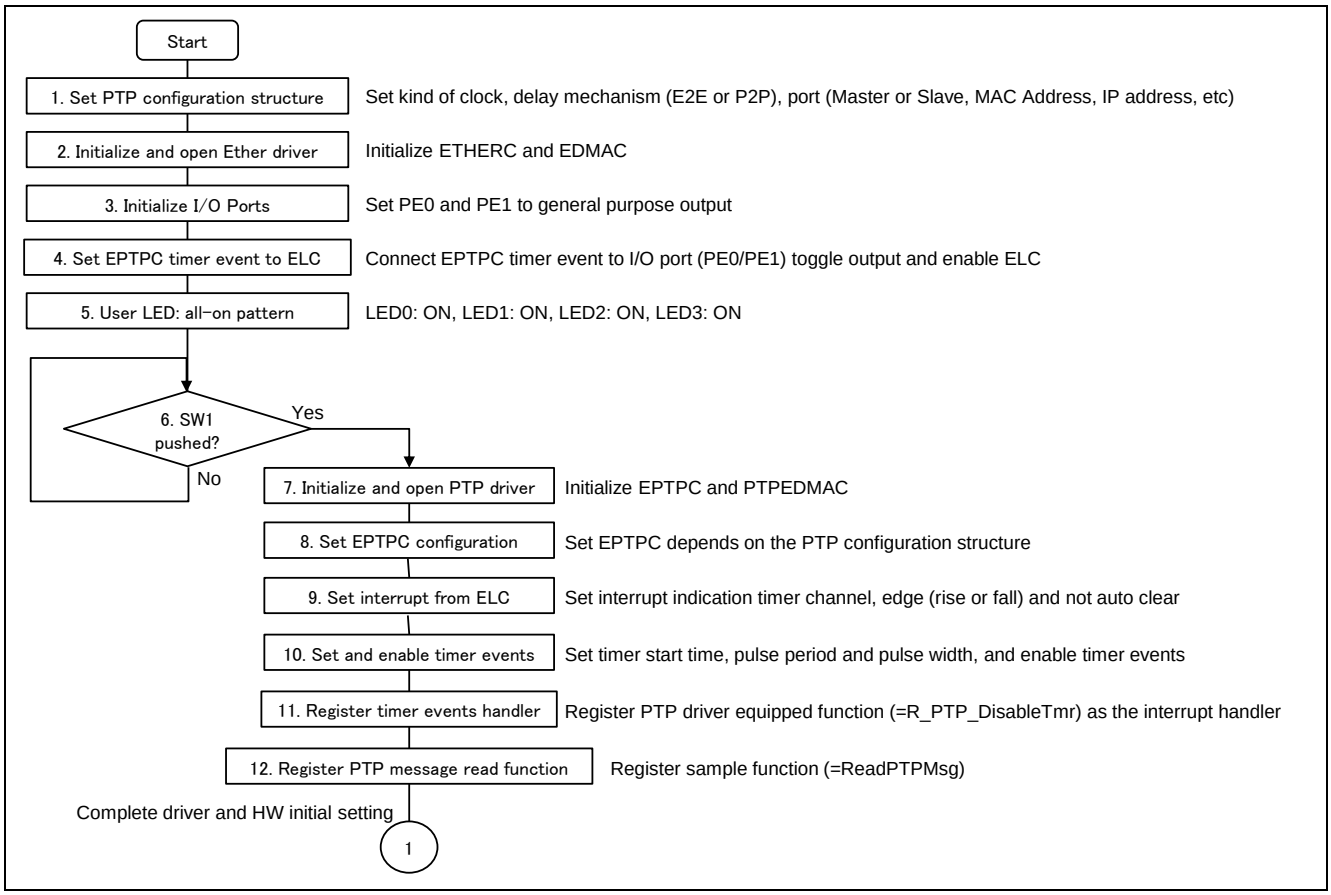

Figure 3.2 (1) Initial setting of related HW

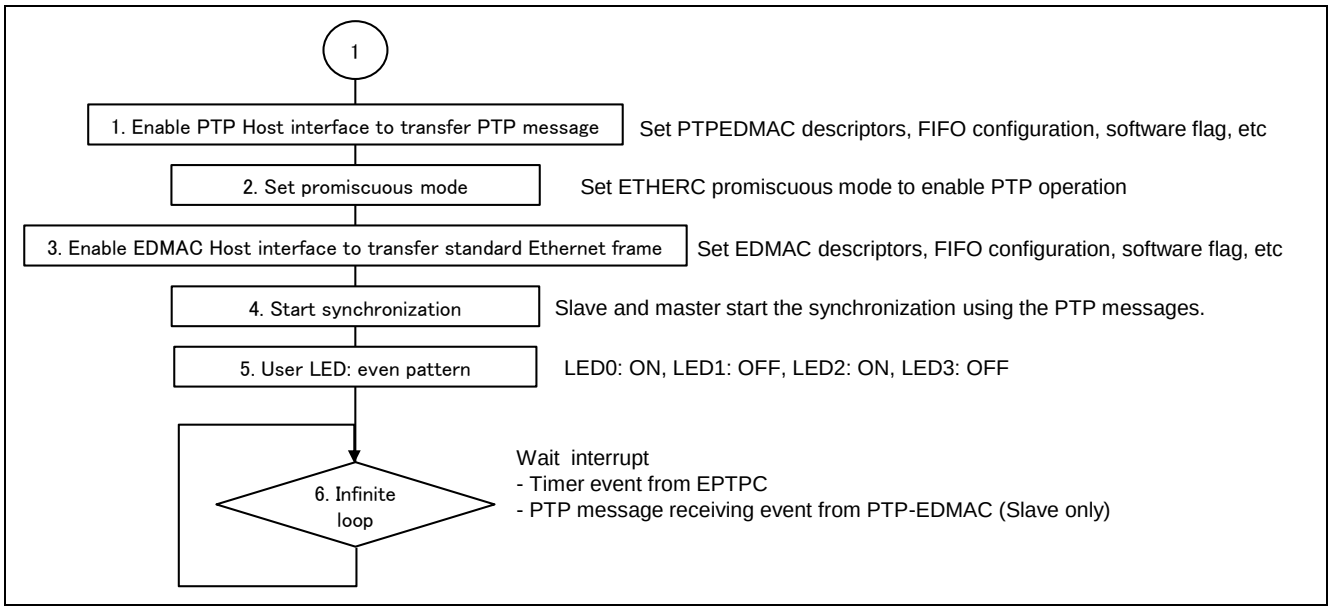

Figure 3.3 (2) Enable Ether communication

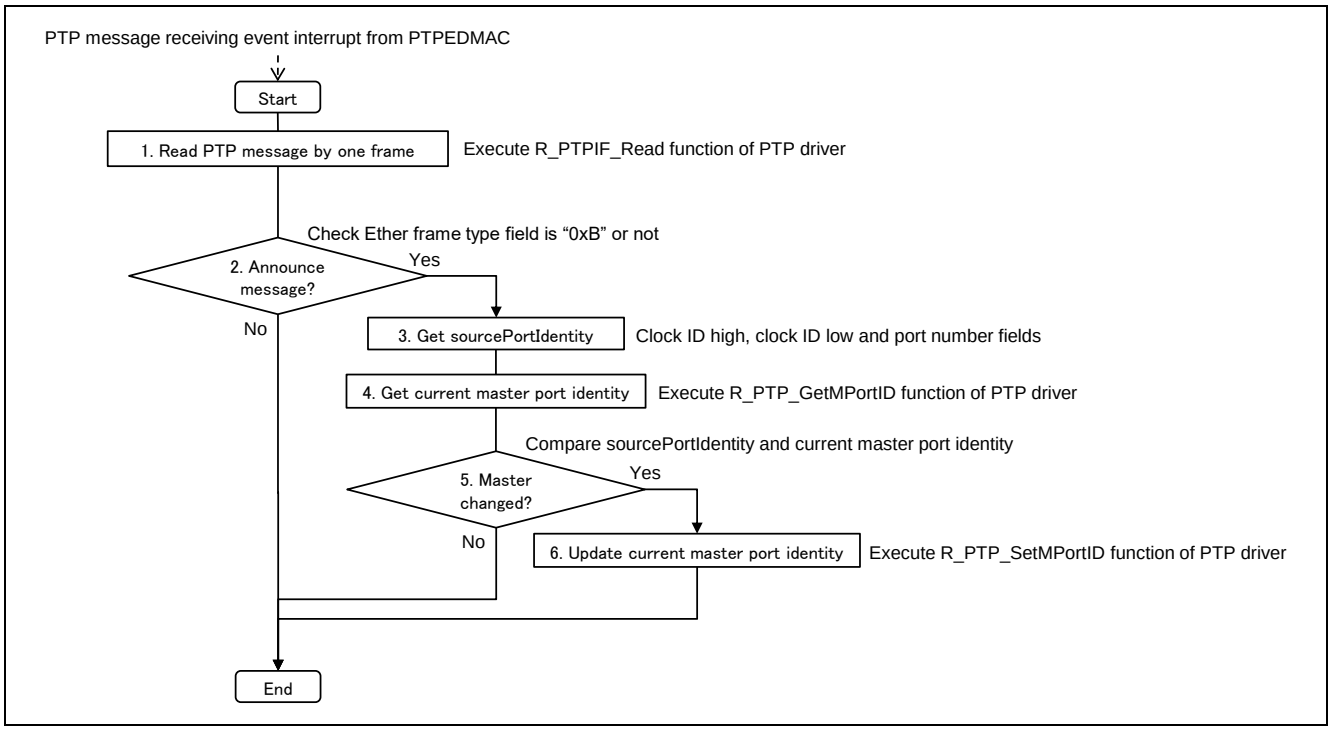

Figure 3.4 (3) PTP message receive interrupt

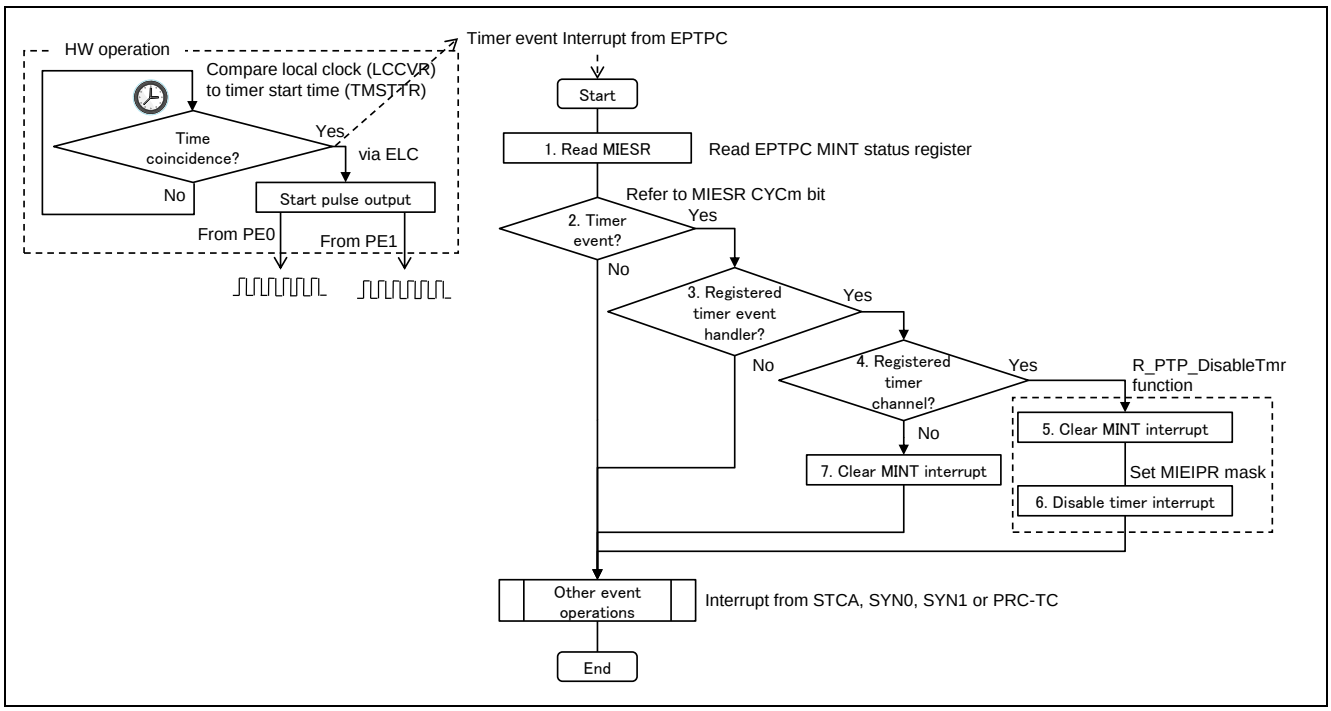

Figure 3.5 (4) Timer event interrupt

3.3 Board Setting

There are two jumpers setting of the RX64M/71M RSK board depending on the PHY access channel of the configuration option. When the product name of the RX64M/71M RSK board is R0K50564MC001BR or R0K5RX71MC010BR, Figure 3.6 indicates their changing. And when the product name of the RX71M RSK board is R0K50571MC000BR, Figure 3.7 indicates their changing depending.

Jumper	LINK_CH = 1[1] (Default setting)	LINK_CH = 0[2]	Functional use
J3	2-3	1-2	ETHERC ET0MDIO or ET1MDIO
J4	2-3	1-2	ETHERC ET0MDC or ET1MDC

[1] In case of MODE_PORT = 1, LINK_CH = 1 is selected.
[2] In case of MODE_PORT = 0, LINK_CH = 0 is selected.

Figure 3.6 Jumper setting

Jumper	LINK_CH = 1[1] (Default setting)	LINK_CH = 0[2]	Functional use
J13	2-3	1-2	ETHERC ET0MDIO or ET1MDIO
J9	2-3	1-2	ETHERC ET0MDC or ET1MDC

[1] In case of MODE_PORT = 1, LINK_CH = 1 is selected.
[2] In case of MODE_PORT = 0, LINK_CH = 0 is selected.

Figure 3.7 Jumper setting

User need to connect the PWM output pin of the RX64M/71M RSK board to the oscilloscope pin. Figure 3.8 indicates the board pins outputted PWM wave.

Application header	Pin	Header name	MCU pin	Output pulse
JA3	29	D8	135	1st pulse
JA3	30	D9	134	2nd pulse

Figure 3.8 output pulse observing pins

3.4 Operation Examples

The operation example applied to two board configuration showed as Figure 3.1 describes following as the typical one.

3.4.1 Condition

- Topology

Using one RX64M RSK board (Master) and one RX71M RSK boards (Slave).

- Protocol

OC (port1) and E2E

- Synchronous mode

The gradient correction, which is the functionality of STCA unit, was applied (=mode2).

- PTP commands interval

PTP commands interval was 1sec[1].

[1] The intervals of Sync and Delay_Req message were 1sec.

- Pulse output timer setting

Using channel: CH0 for 1st pulse (PE0), CH1 for 2nd pulse (PE1)

Start time: 30,123,456,789 nsec (TMSTTRUm: 0x00000007, TMSTTRLm: 0x037F7915)

- Pulse specifications

1st pulse (PE0): 400µsec period, 200µsec width (Duty: 50%)

2nd pulse (PE1): 100µsec period, 50µsec width (Duty: 50%)

3.4.2 Mechanism

The pulse output timer creates the pulse synchronized with PTP continuously connecting timer events to the toggle output of I/O ports. The period and width of the output pulse are enhanced two times compare to the pulse output timer original ones. Figure 3.9 and Figure 3.10 show the creation mechanism when the event signal trigger is rise and fall edge respectively in this operation example.

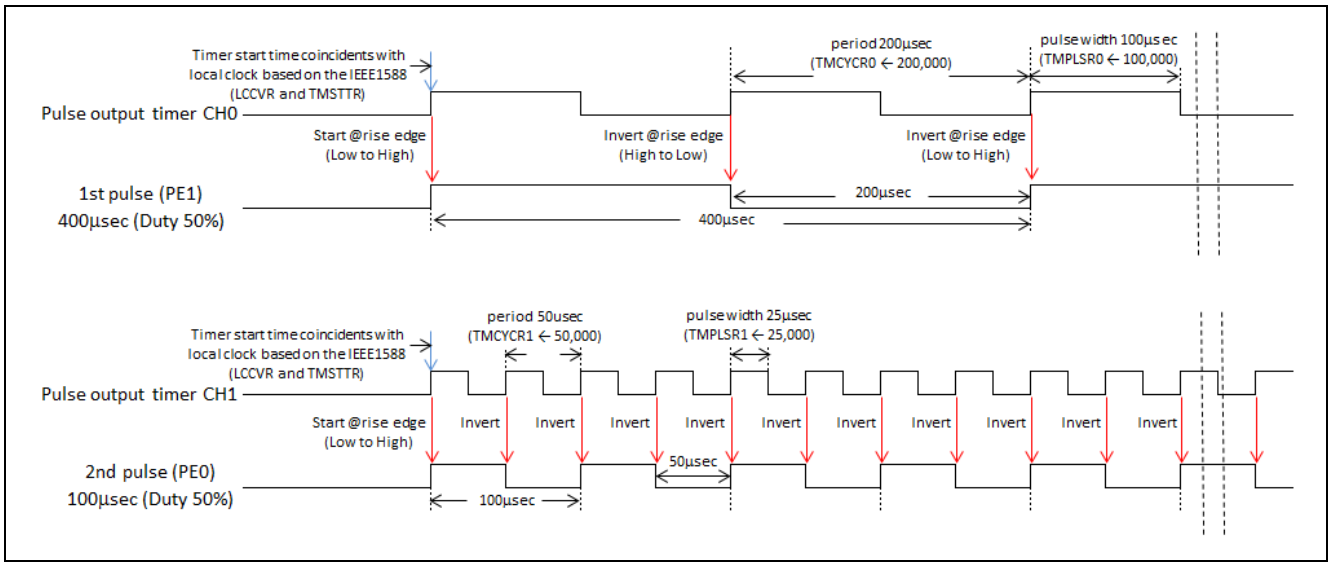

Figure 3.9 Synchronous pulse creation (Rise edge)

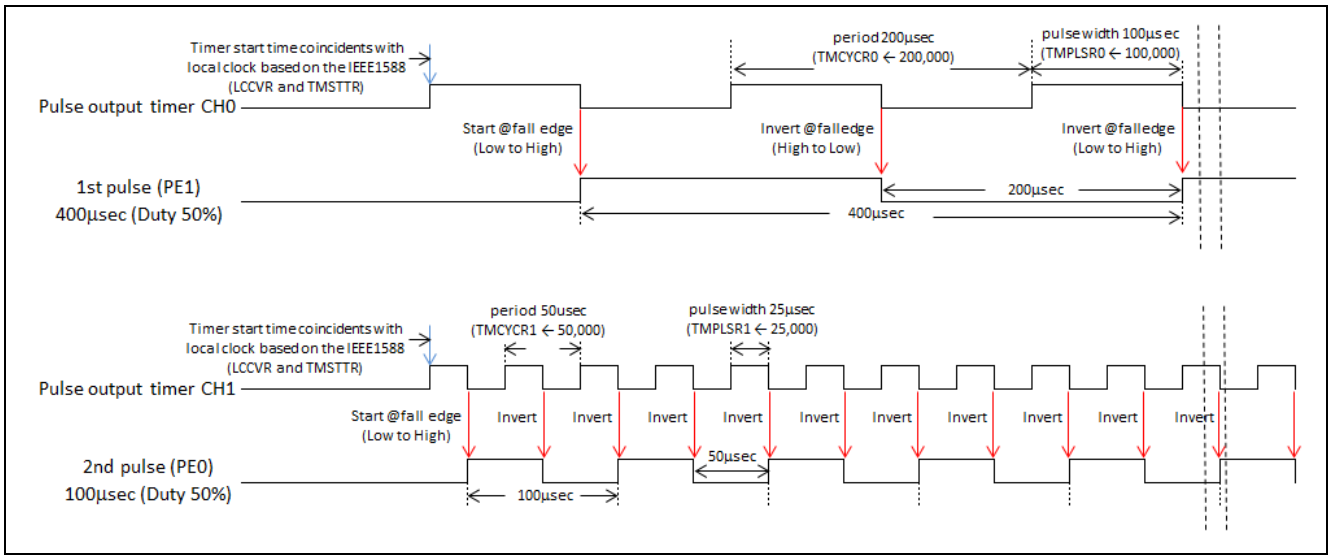

Figure 3.10 Synchronous pulse creation (Fall edge)

3.4.3 Output Pulse

Figure 3.11 shows the output pulses in the Sec 3.4.1 conditions when the event signal trigger is rise edge and this time scale is 50µsec per unit coordinate. The blue line and red line indicate the 2nd pulse and 1st pulse outputted from RX64M RSK board Slave respectively. The yellow line and green line indicate the 2nd pulse and 1st pulse outputted from RX71M RSK board Master respectively.

Please keep your mind those result are depend on the measurement condition and environment.

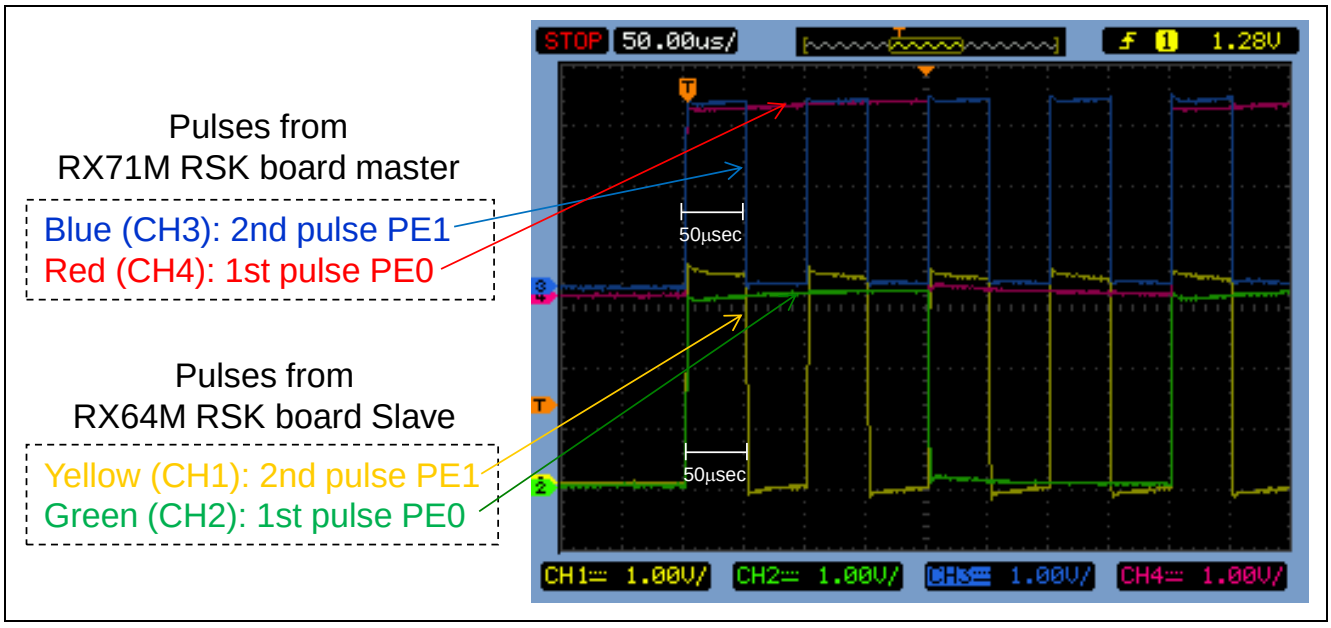

Figure 3.11 Output pulse example (Rise edge, 50µsec scale unit)

4. Reference Documents

User's Manual: Hardware

RX64M Group User's Manual: Hardware Rev.1.10 (R01UH0377EJ)
RX71M Group User's Manual: Hardware Rev.1.00 (R01UH0493EJ)
The latest version can be downloaded from the Renesas Electronics website.

User's Manual: Software

RX Family RXv2 Instruction Set Architecture User's Manual: Hardware Rev.1.00 (R01US0071EJ)
The latest version can be downloaded from the Renesas Electronics website.

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Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Jul 24, 2015	**—**	First edition issued.
1.10	Mar 31, 2016	**—**	Applied PTP driver Rev.1.10.
1.11	Nov 11, 2016	**—**	Applied PTP driver Rev.1.12 and Ethernet driver Rev.1.12.
		14	Corrected header name of output pulse pin (Fig 3.8).
1.12	Mar 31, 2017	**—**	Applied PTP driver Rev.1.13.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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SALES OFFICES

Renesas Electronics Corporation

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Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL II Stage, Indiranagar, Bangalore, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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