RL78/L12

Serial Array Unit (UART Communication) CC-RL

R01AN3316EJ0100
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Introduction

This application note explains how to use UART communication through the serial array unit (SAU). ASCII characters transmitted from the device on the opposite side are analyzed to make responses.

Target Device

RL78/L12

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specifications

In this application note, UART communication is performed through the serial array unit (SAU). ASCII characters transmitted from the device on the opposite side are analyzed to make responses.

Table 1.1 shows the peripheral function to be used and its use. Figures 1.1 and 1.2 illustrate UART communication operation.

Table 1.1 Peripheral Function to be Used and its Use

Peripheral Function	Use
Serial array unit 0	Perform UART communication using the TxD0 pin (transmission) and the RxD0 pin (reception).

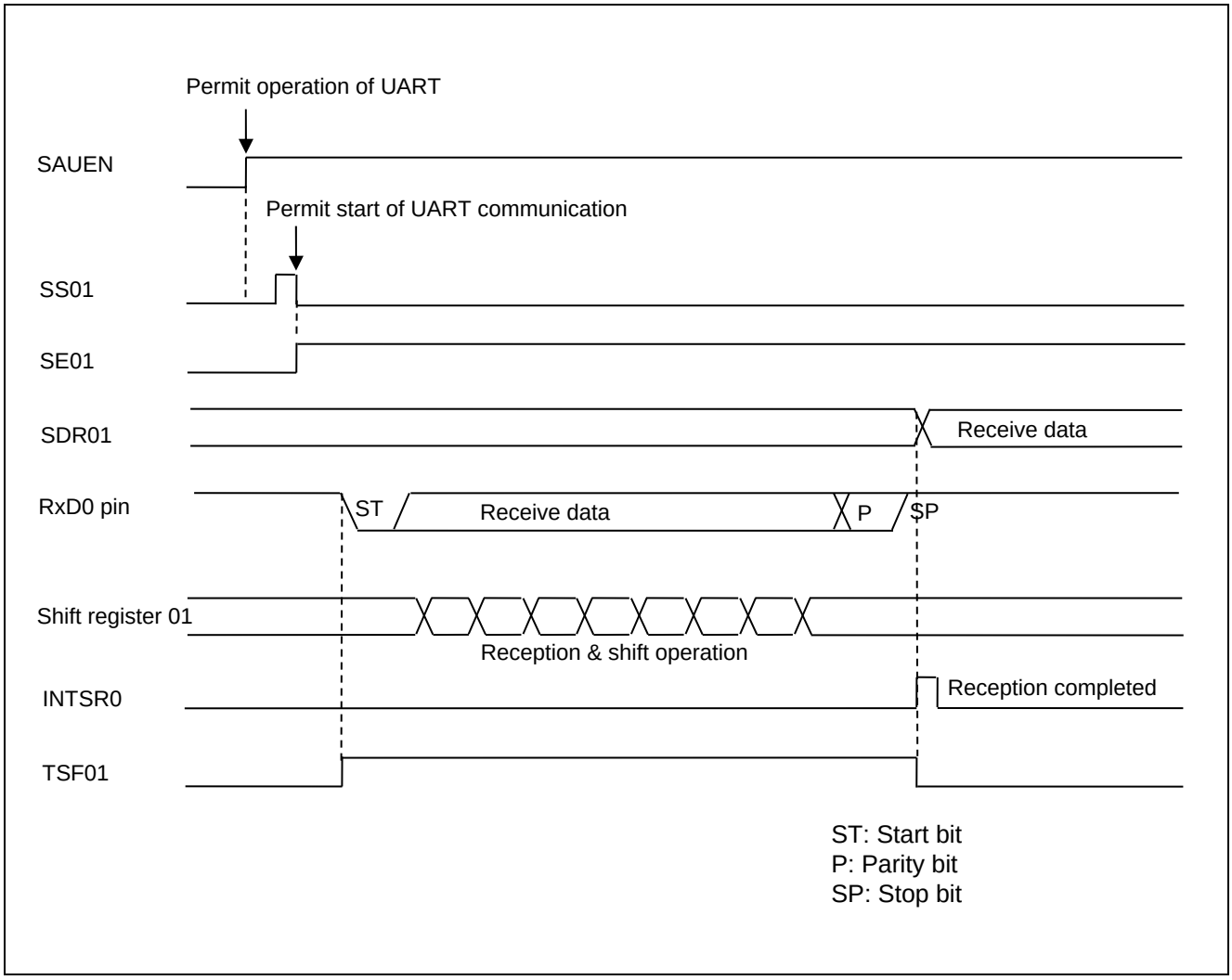

Figure 1.1 UART Reception Timing Chart

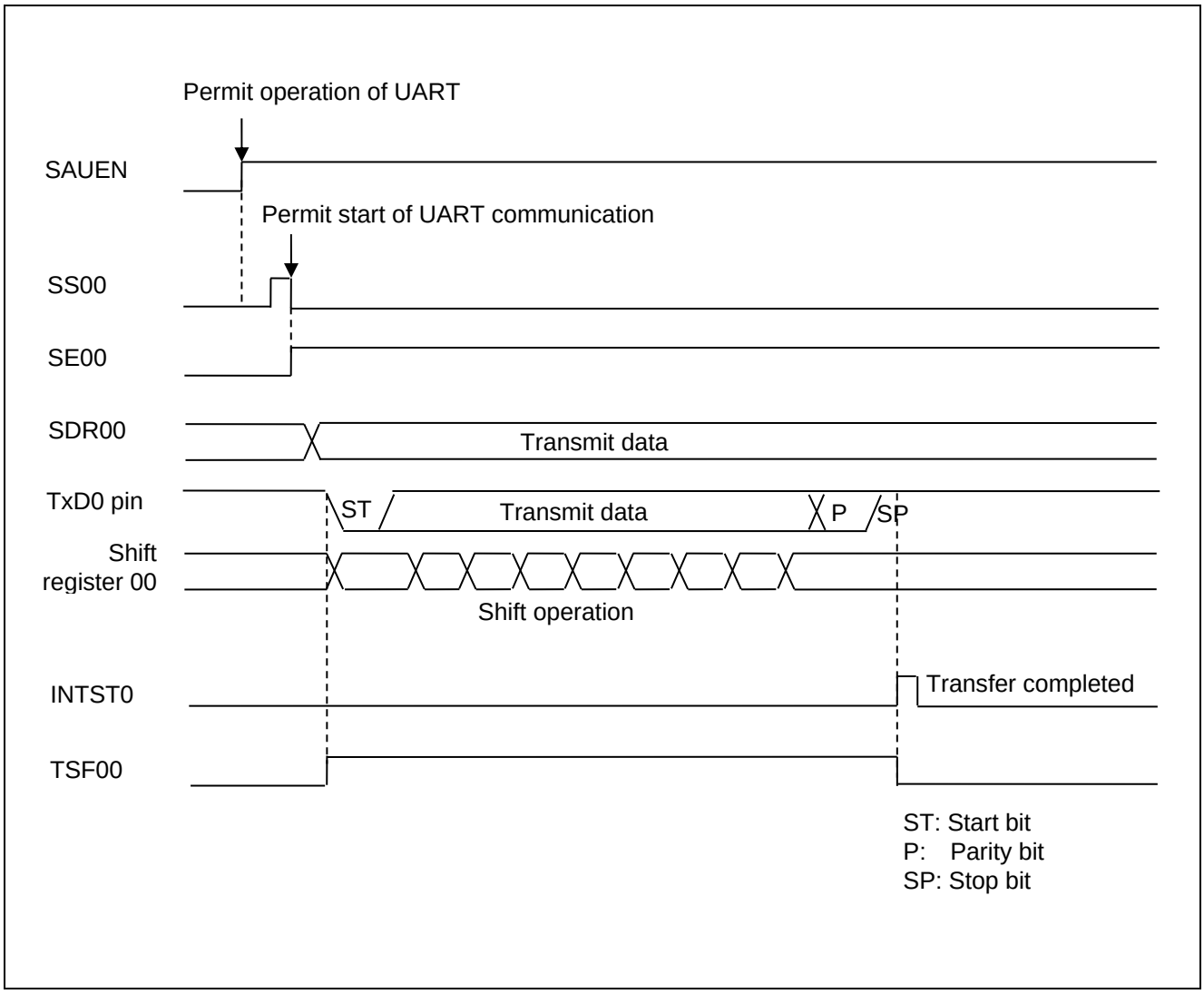

Figure 1.2 UART Transmission Timing Chart

2. Operation Check Conditions

The sample code contained in this application note has been checked under the conditions listed in the table below.

Table 2.1 Operation Check Conditions

Item	Description
Microcontroller used	RL78/L12 (R5F10RLC)
Operating frequency	• High-speed on-chip oscillator (HOCO) clock: 24 MHz • CPU/peripheral hardware clock: 24 MHz
Operating voltage	5.0 V (can run on a voltage range of 2.9 V to 5.5 V.) LVD operation (V_{LVD}): Reset mode 2.81 V (2.76V to 2.87V)
Integrated development environment (CS+)	Renesas Electronics Corporation CS+ for CC V3.03.00
C compiler (CS+)	Renesas Electronics Corporation CC-RL V1.02.00
Integrated development environment (e^2 studio)	Renesas Electronics Corporation e^2 studio V4.0.0.26
C compiler (e^2 studio)	Renesas Electronics Corporation CC-RL V1.02.00
Board	RL78/L12 CPU board (R0K5010RLC010BR)

3. Related Application Note

The application note that is related to this application note is listed below for reference.

RL78/G13 Serial Array Unit (UART communication) CC-RL (R01AN2517E) Application Note

4. Description of the Hardware

4.1 Hardware Configuration Example

Figure 4.1 shows an example of hardware configuration that is used for this application note.

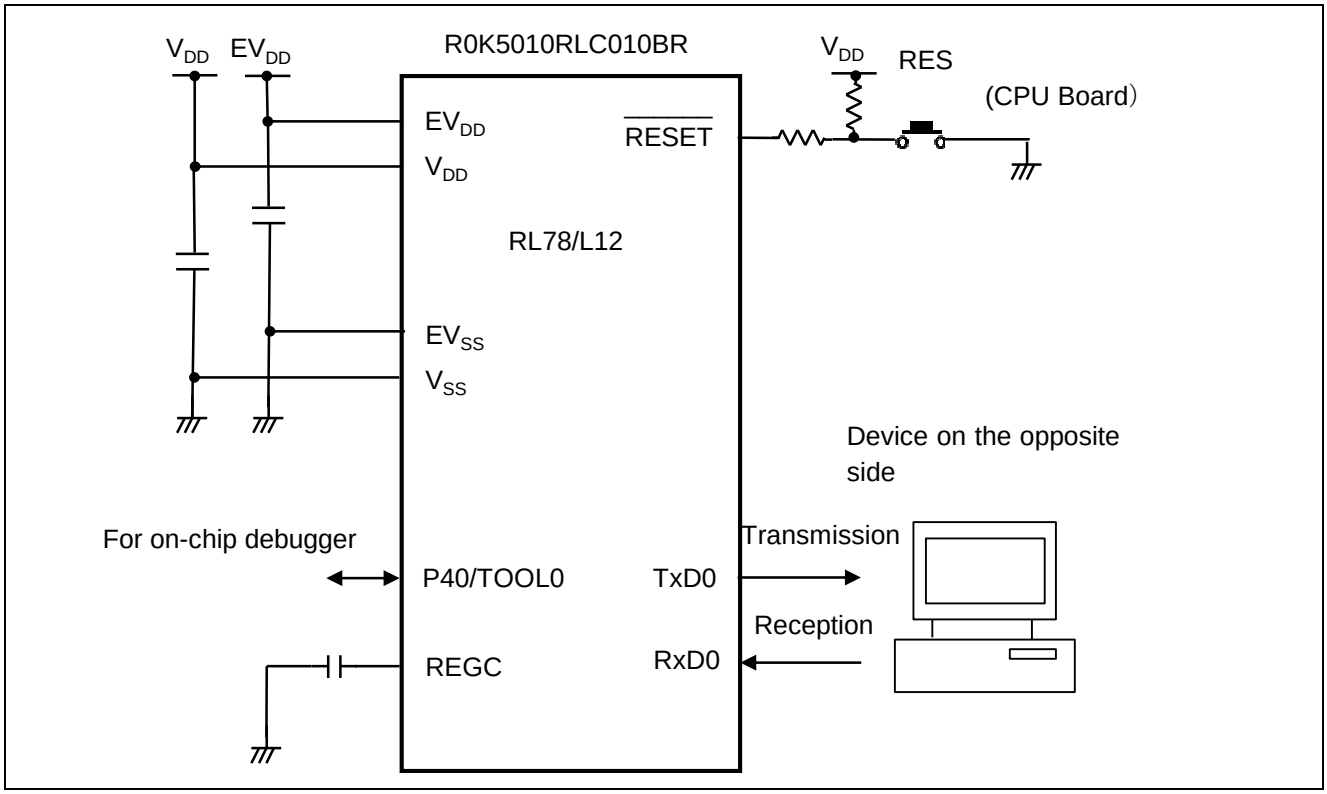

Figure 4.1 Hardware Configuration

Caution: 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V_{DD} or V_{SS} via a resistor).
2. Connect any pins whose name begins with EV_{SS} to V_{SS} and any pins whose name begins with EV_{DD} to V_{DD}, respectively.
3. V_{DD} must be held at not lower than the reset release voltage (V_{LVD}) that is specified as LVD.

4.2 List of Pins to be Used

Table 4.1 lists the pins to be used and their function.

Table 4.1 Pins to be Used and their Functions

Pin Name	I/O	Description
P12/ SO00/TxD0/TOOLTxD/SEG30	Output	Data transmission pin
P11/ SI00/RxD0/TOOLRxD/SEG29	Input	Data reception pin

5. Description of the Software

5.1 Operation Outline

This sample code transmits, to the device on the opposite side, the data corresponding to that received from the device. If an error occurs, it transmits to the device the data corresponding to the error. Tables 5.1 and 5.2 show the correspondence between transmit data and receive data.

Table 5.1 Correspondence between Receive Data and Transmit Data

Receive Data	Response (Transmit) Data
T (54H)	O (4FH), K (4BH), ”CR” (0DH), ”LF” (0AH)
t (74H)	o (6FH), k (6BH), ”CR” (0DH), ”LF” (0AH)
Other than above	U (55H), C (43H), ”CR” (0DH), ”LF” (0AH)

Table 5.2 Correspondence between Error and Transmit Data

Error	Response (Transmit) Data
Parity error	P (50H), E (45H), ”CR” (0DH), ”LF” (0AH)
Framing error	F (46H), E (45H), ”CR” (0DH), ”LF” (0AH)
Overrun error	O (4FH), E (45H), ”CR” (0DH), ”LF” (0AH)

(1) Perform initial setting of UART.
<UART Setting Conditions>

- Use SAU0 channels 0 and 1 as UART.
- Use the P11/TxD0 pin and the P12/RxD0 pin for data output and data input, respectively.
- The data length is 8 bits.
- Set the data transfer direction to LSB first.
- Use even parity as the parity setting.
- Set the receive data level to standard.
- Set the transfer rate to 9600 bps.
- Use reception end interrupt (INTSR0), transmission end interrupt (INTST0), and error interrupt (INTSRE0).
- Select interrupt priority level 2 or 1 for INTSR0 and for INTSRE0. Select the low interrupt priority level (level 3) for INTST0.

(2) After the system is made to enter a UART communication wait state by using the serial channel start register, a HALT instruction is executed. Processing is performed in response to reception end interrupt (INTSR0) and error interrupt (INTSRE0).

- When an INTSR0 occurs, the received data is taken in and the data corresponding to the received data is transmitted. When an INTSRE0 occurs, error handling is performed to transmit the data corresponding to the error.
- After data transmission, a HALT instruction is executed again to wait for reception end interrupt (INTSR0) and error interrupt (INTSRE0).

5.2 List of Option Byte Settings

Table 5.1 summarizes the settings of the option bytes.

Table 5.1 Option Byte Settings

Address	Value	Description
000C0H/010C0H	01101110B	Disables the watchdog timer. (Stops counting after the release from the reset state.)
000C1H/010C1H	01111111B	LVD reset mode, 2.81 V (2.76V to 2.87V)
000C2H/010C2H	11100000B	HS mode, HOCO: 24MHz
000C3H/010C3H	10000101B	Enables the on-chip debugger.

5.3 List of Constants

Table 5.2 lists the constants that are used in this sample program.

Table 5.2 Constants for the Sample Program

Constant	Setting	Description
g_messageOK[4]	"OK¥r¥n"	Response message to reception of “T”.
g_messageok[4]	"ok¥r¥n"	Response message to reception of “t”.
g_messageUC[4]	"UC¥r¥n"	Response message to reception of characters other than “T” or “t”.
g_messageFE[4]	"FE¥r¥n"	Response message to a framing error.
g_messagePE[4]	"PE¥r¥n"	Response message to a parity error.
g_messageOE[4]	"OE¥r¥n"	Response message to an overrun error.

5.4 List of Variables

Table 5.3 lists the global variable that is used by this sample program.

Table 5.3 Global Variable

Type	Variable Name	Contents	Function Used
uint8_t	g_uart0_rx_buffer	Receive data buffer	main()
uint8_t	gp_uart0_tx_address	Transmit data pointer	R_UART0_Send(), R_UART0_Interrupt_Send()
uint16_t	g_uart0_tx_count	Transmit data number counter	R_UART0_Send(), R_UART0_Interrupt_Send()
uint8_t	gp_uart0_rx_address	Receive data pointer	R_UART0_Receive(), R_UART0_Interrupt_Receive(), R_UART0_Interrupt_Error()
uint16_t	g_uart0_rx_ count	Receive data number counter	R_UART0_Receive(), R_UART0_Interrupt_Receive()
uint16_t	g_uart0_rx_length	Receive data number	R_UART0_Receive(), R_UART0_Interrupt_Receive()
MD_STATUS	g_uart0_tx_end	Transmit status	main(), r_uart0_callback_sendend()
unit8_t	g_uart0_rx_error	Receive error status	main(), r_uart0_callback_receiveend(), r_uart0_callback_error()

5.5 List of Functions

Table 5.4 lists the functions that are used in this sample program.

Table 5.4 Functions

Function Name	Outline
R_UART0_Start	UART0 operation start
R_UART0_Receive	UART0 reception status initialization function
R_UART0_Send	UART0 data transmission function
r_uart0_interrupt_receive	UART0 reception end interrupt handling
r_uart0_callback_receiveend	UART0 receive data classification function
r_uart0_interrupt_error	UART0 error interrupt handling
r_uart0_callback_error	UART0 reception error classification function
r_uart0_interrupt_send	UART0 transmission end interrupt handling
r_uart0_callback_sendend	UART0 transmission end processing function
r_uart0_callback_softwareoverrun	UART0 overflow data receive function

5.6 Function Specifications

This section describes the specifications for the functions that are used in this sample program.

[Function Name]R_ UART0_Start

Synopsis	UART0 operation start
Header	r_cg_macrodriver.h, r_cg_serial.h, and r_cg_userdefine.h
Declaration	void R_ UART0_Start(void)
Explanation	Starts operation of channel 0 of serial array units 0 and 1 to make the system enter a communication wait state.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_UART0_Receive

Synopsis	UART0 reception status initialization function	
Header	r_cg_macrodriver.h, r_cg_serial.h, r_cg_userdefine.h	
Declaration	MD_STATUS R_UART0_Receive(uint8_t *rx_buf, uint16_t rx_num)	
Explanation	Makes initial setting for UART0 reception.	
Arguments	uint8_t *rx_buf	: [Receive data buffer address]
	uint16_t rx_num	: [Receive data buffer size]
Return value	[MD_OK]: Reception setting is completed [MD_ARGERROR]: Reception setting failed	
Remarks	None	

[Function Name] R_UART0_Send

Synopsis	UART0 data transmission function	
Header	r_cg_macrodriver.h, r_cg_serial.h, r_cg_userdefine.h	
Declaration	MD_STATUS R_UART0_Send(uint8_t* tx_buf, uint16_t tx_num)	
Explanation	Makes initial setting for UART0 transmission, and starts data transmission.	
Arguments	uint8_t *tx_buf	: [Transmit data buffer address]
	uint16_t tx_num	: [Transmit data buffer size]
Return value	[MD_OK]: Transmission setting is completed	
	[MD_ARGERROR]: Transmission setting failed	
Remarks	None	

[Function Name] r_uart0_interrupt_receive

Synopsis	UART0 reception end interrupt handling
Header	r_cg_macrodriver.h, r_cg_serial.h, and r_cg_userdefine.h
Declaration	static void __near r_uart0_interrupt_receive(void)
Explanation	Makes a response (data transmission) corresponding to received data.
Arguments	None
Return value	None
Remarks	None

[Function Name] r_uart0_interrupt_erro

Synopsis	UART error interrupt function
Header	r_cg_macrodriver.h, r_cg_serial.h, and r_cg_userdefine.h
Declaration	static void __near r_uart0_interrupt_error(void)
Explanation	Transmits the data corresponding to a detected error.
Arguments	None
Return value	None
Remarks	None

[Function Name] r_uart0_callback_receiveend

Synopsis	UART0 receive data classification function
Header	r_cg_macrodriver.h, r_cg_serial.h, and r_cg_userdefine.h
Declaration	static void r_uart0_callback_receiveend(void)
Explanation	Clears the reception error flag.
Arguments	None
Return value	None
Remarks	None

[Function Name] r_uart0_callback_error

Synopsis	UART0 reception error classification function	
Header	r_cg_macrodriver.h, r_cg_serial.h, and r_cg_userdefine.h	
Declaration	static void r_uart0_callback_error(uint8_t err_type)	
Explanation	Makes flag setting for transmission of the data corresponding to an error.	
Arguments	err_type	: Error type
Return value	None	
Remarks	None	

[Function Name] r_uart0_interrupt_send

Synopsis	UART0 transmission end interrupt handling
Header	r_cg_macrodriver.h, r_cg_serial.h, and r_cg_userdefine.h
Declaration	static void __near r_uart0_interrupt_send(void)
Explanation	Transmits a specified number of pieces of data.
Arguments	None
Return value	None
Remarks	None

[Function Name] r_uart0_callback_sendend

Synopsis	UART0 transmission end processing function
Header	r_cg_macrodriver.h, r_cg_serial.h, r_cg_userdefine.h
Declaration	static void r_uart0_callback_sendend(void)
Explanation	Makes transmission end flag setting.
Arguments	None
Return value	None
Remarks	None

[Function Name] r_uart0_callback_softwareoverrun

Synopsis	UART0 overflow data receive function
Header	r_cg_macrodriver.h, r_cg_serial.h, r_cg_userdefine.h
Declaration	static void r_uart0_callback_softwareoverrun(void)
Explanation	Executes when detected overflow of data by software.
Arguments	None
Return value	None
Remarks	Unused function

5.7 Flowcharts

Figure 5.1 shows the overall flow of the sample program described in this application note.

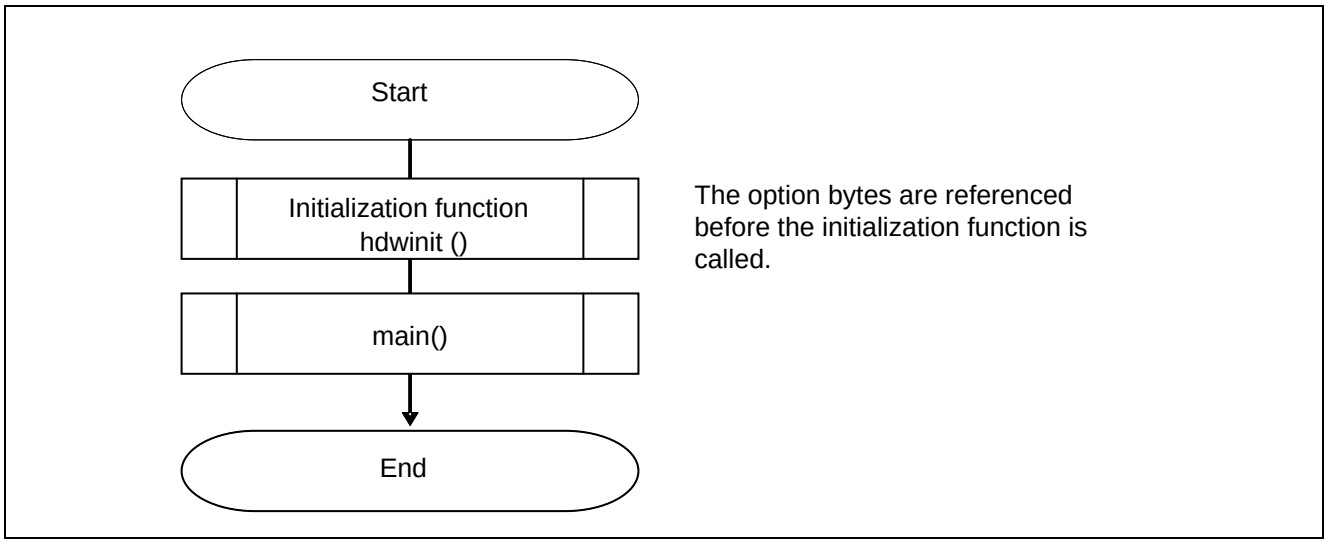

Figure 5.1 Overall Flow

Note: Startup routine is executed before and after the initialization function.

5.7.1 Initialization Function

Figure 5.2 shows the flowchart for the initialization function.

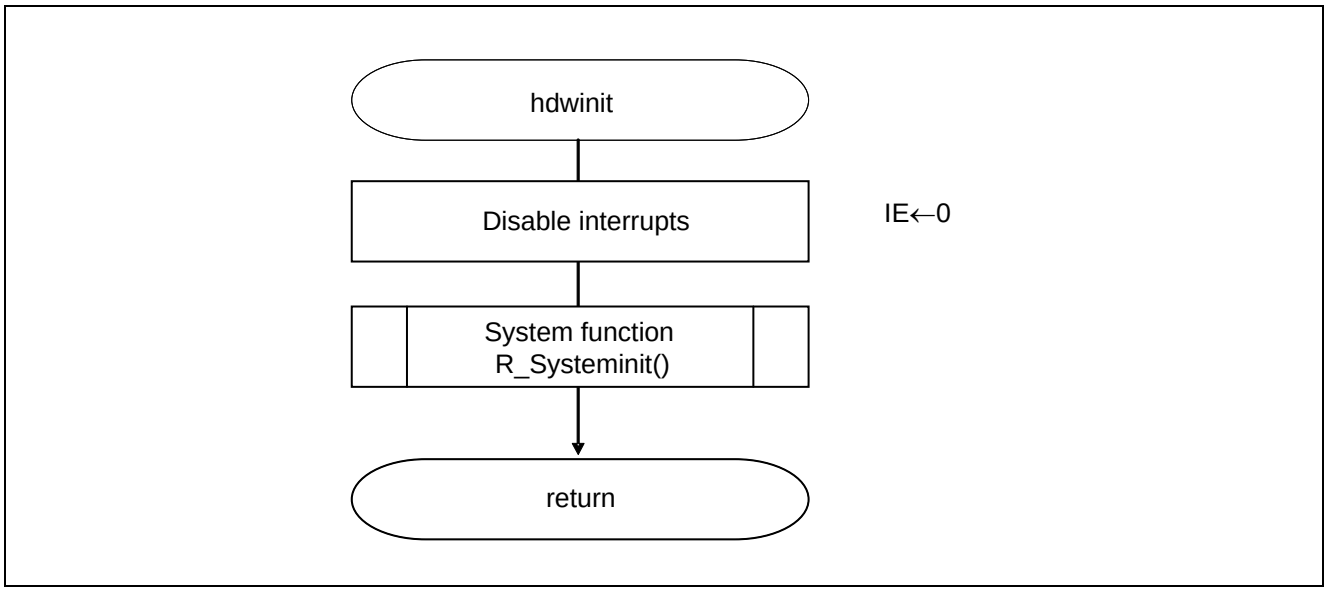

Figure 5.2 Initialization Function

5.7.2 System Function

Figure 5.3 shows the flowchart for the system function.

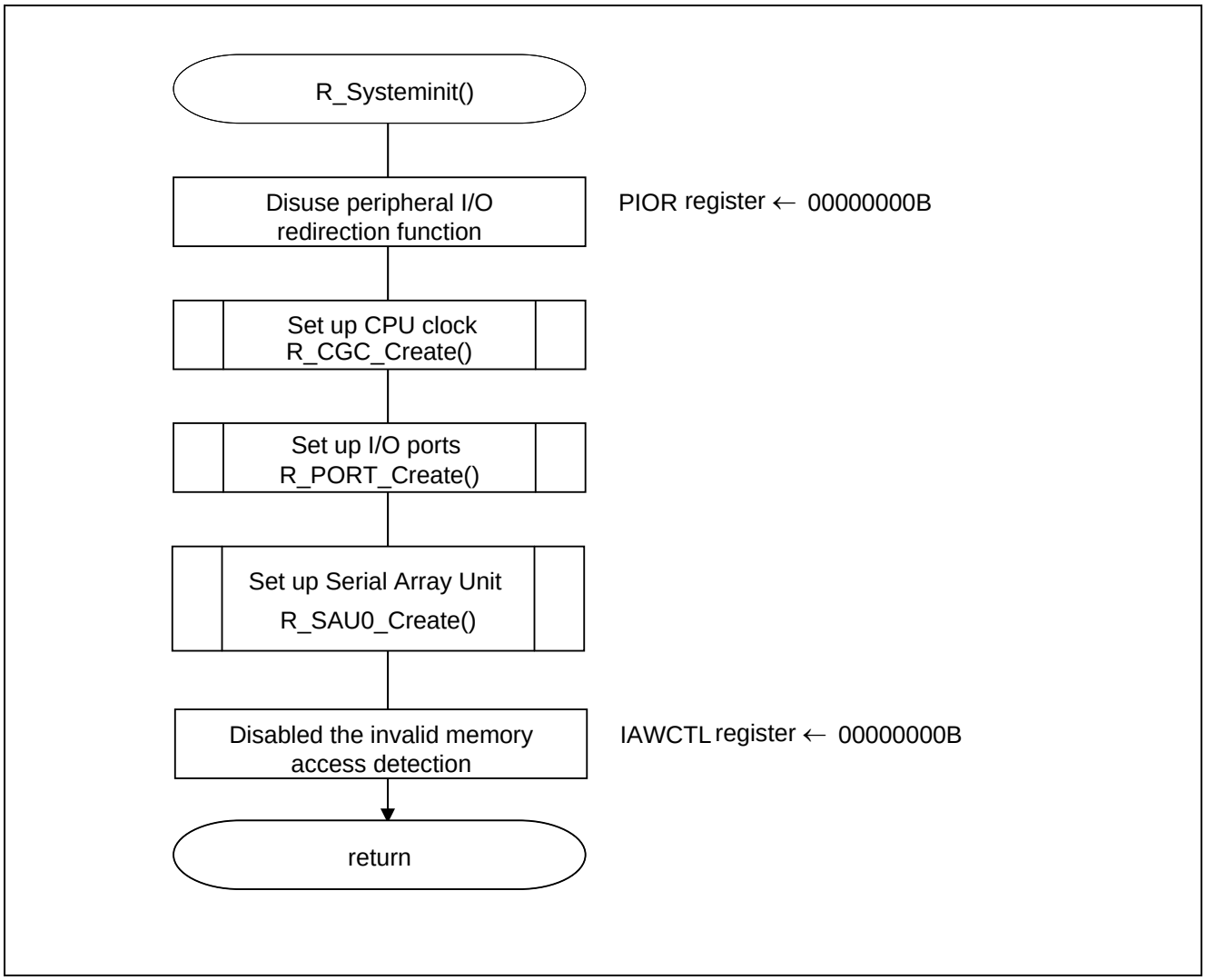

Figure 5.3 System Function

5.7.3 I/O Port Setup

Figure 5.4 shows the flowchart for setting up the I/O ports.

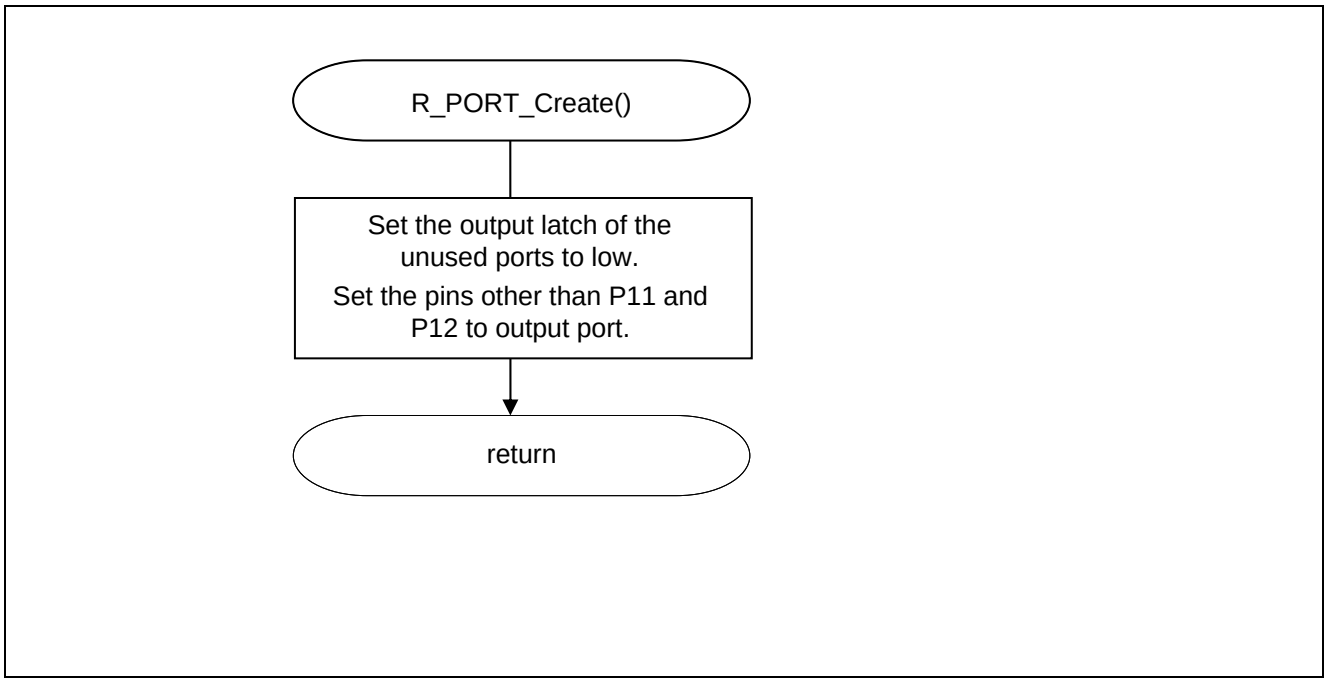

Figure 5.4 I/O Port Setup

Note: Refer to the RL78/L12 User's Manual: Hardware for the configuration of the unused ports.

Caution: Provide proper treatment for unused pins so that their electrical specifications are observed. Connect each of any unused input-only ports to V_{DD} or V_{SS} via a separate resistor.

5.7.4 CPU Clock Setup

Figure 5.5 shows the flowchart for setting up the CPU clock.

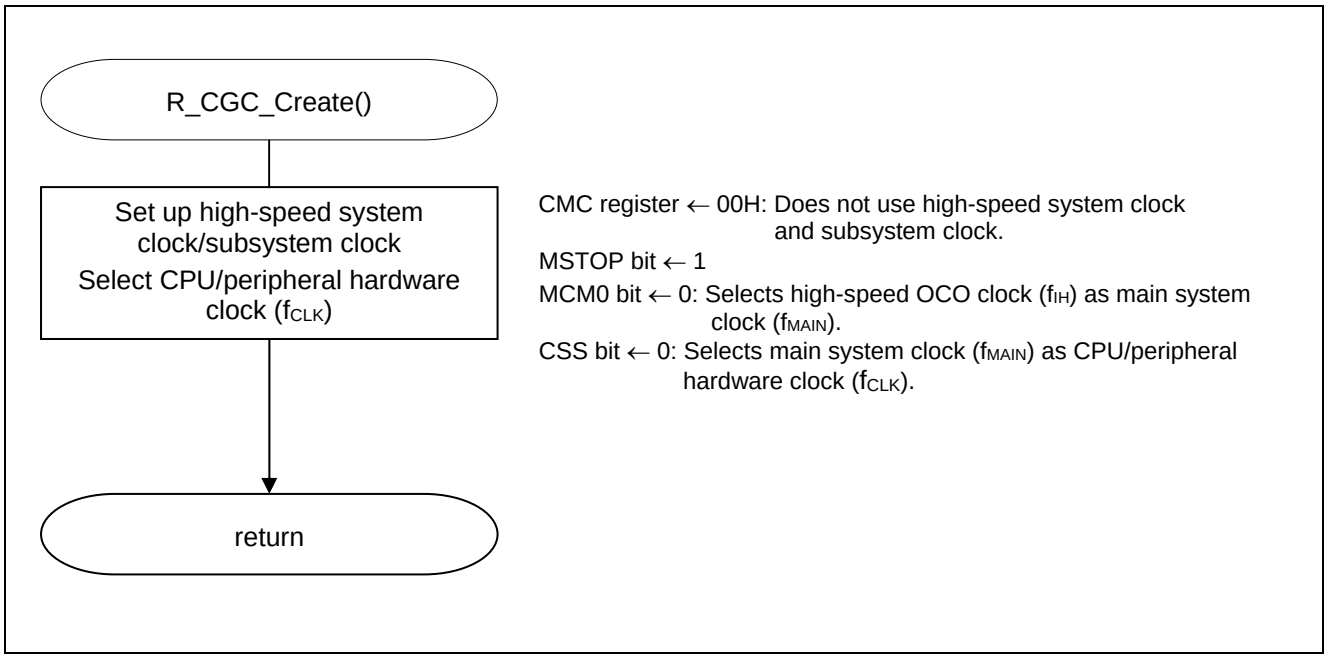

Figure 5.5 CPU Clock Setup

5.7.5 Serial Array Unit Setup

Figure 5.6 shows the flowchart for setting up the serial array unit.

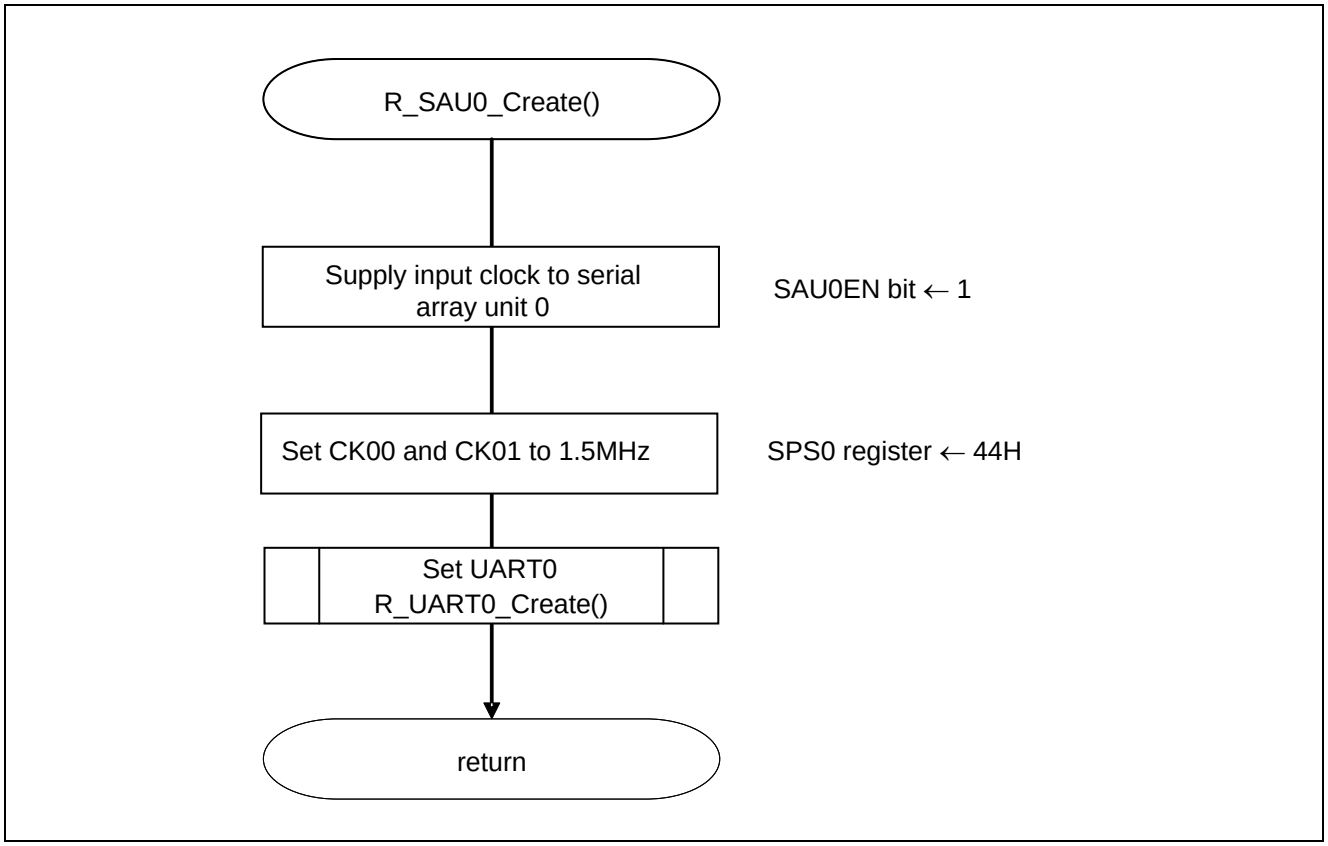

Figure 5.6 Serial Array Unit Setup

Start supplying clock to the SAU

- Peripheral enable register 0 (PER0)
  Clock supply

Symbol: PER0

7	6	5	4	3	2	1	0
RTCEN	0	ADCEN	IICA0EN	0	SAU0EN	0	TAU0EN
x	0	x	x	0	**1**	0	x

Bit 2

SAU0EN	Input clock control for serial array unit 0
0	Stops supply of input clock.
1	**Starts supply of input clock.**

Select serial clock

- Serial clock select register 0 (SPS0)
  Operation clock setting

Symbol: SPS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	PRS 013	PRS 012	PRS 011	PRS 010	PRS 003	PRS 002	PRS 001	PRS 000
0	0	0	0	0	0	0	0	**0**	**1**	**0**	**0**	**0**	**1**	**0**	**0**

Bits 7 to 0

PRS 0n3	PRS 0n2	PRS 0n1	PRS 0n0	Operation clock (CK00) selection (n = 0, 1)					
					f_{CLK} = 2 MHz	f_{CLK} = 5 MHz	f_{CLK} = 10 MHz	f_{CLK} = 20 MHz	f_{CLK} = 24MHz
0	0	0	0	f_{CLK}	2 MHz	5 MHz	10 MHz	20 MHz	24MHz
0	0	0	1	$f_{CLK}/2$	1 MHz	2.5 MHz	5 MHz	10 MHz	12 MHz
0	0	1	0	$f_{CLK}/2^2$	500 kHz	1.25 MHz	2.5 MHz	5 MHz	6 MHz
0	0	1	1	$f_{CLK}/2^3$	250 kHz	625 kHz	1.25 MHz	2.5 MHz	3 MHz
0	**1**	**0**	**0**	**$f_{CLK}/2^4$**	**125 kHz**	**312.5 kHz**	**625 kHz**	**1.25 MHz**	**1.5 MHz**
0	1	0	1	$f_{CLK}/2^5$	62.5 kHz	156.2 kHz	312.5 kHz	625 kHz	750 kHz
0	1	1	0	$f_{CLK}/2^6$	31.25 kHz	78.1 kHz	156.2 kHz	312.5 kHz	375 kHz
0	1	1	1	$f_{CLK}/2^7$	15.62 kHz	39.1 kHz	78.1 kHz	156.2 kHz	187.5 kHz
1	0	0	0	$f_{CLK}/2^8$	7.81 kHz	19.5 kHz	39.1 kHz	78.1 kHz	93.8 kHz
1	0	0	1	$f_{CLK}/2^9$	3.91 kHz	9.76 kHz	19.5 kHz	39.1 kHz	46.9 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.95 kHz	4.88 kHz	9.76 kHz	19.5 kHz	23.4 kHz
1	0	1	1	$f_{CLK}/2^{11}$	977 Hz	2.44 kHz	4.88 kHz	9.76 kHz	11.7 kHz
1	1	0	0	$f_{CLK}/2^{12}$	488 Hz	1.22 kHz	2.44 kHz	4.88 kHz	5.86 kHz
1	1	0	1	$f_{CLK}/2^{13}$	244 Hz	610 Hz	1.22 kHz	2.44 kHz	2.93 kHz
1	1	1	0	$f_{CLK}/2^{14}$	122 Hz	305 Hz	610 Hz	1.22 kHz	1.46 kHz
1	1	1	1	$f_{CLK}/2^{15}$	61 Hz	153 Hz	305 Hz	610 Hz	732 Hz

Caution: For details on the register setup procedures, refer to RL78/L12 User's Manual: Hardware.

5.7.6 UART0 Setup

Figures 5.7, 5.8, and 5.9 show the flowcharts for setting up UART0.

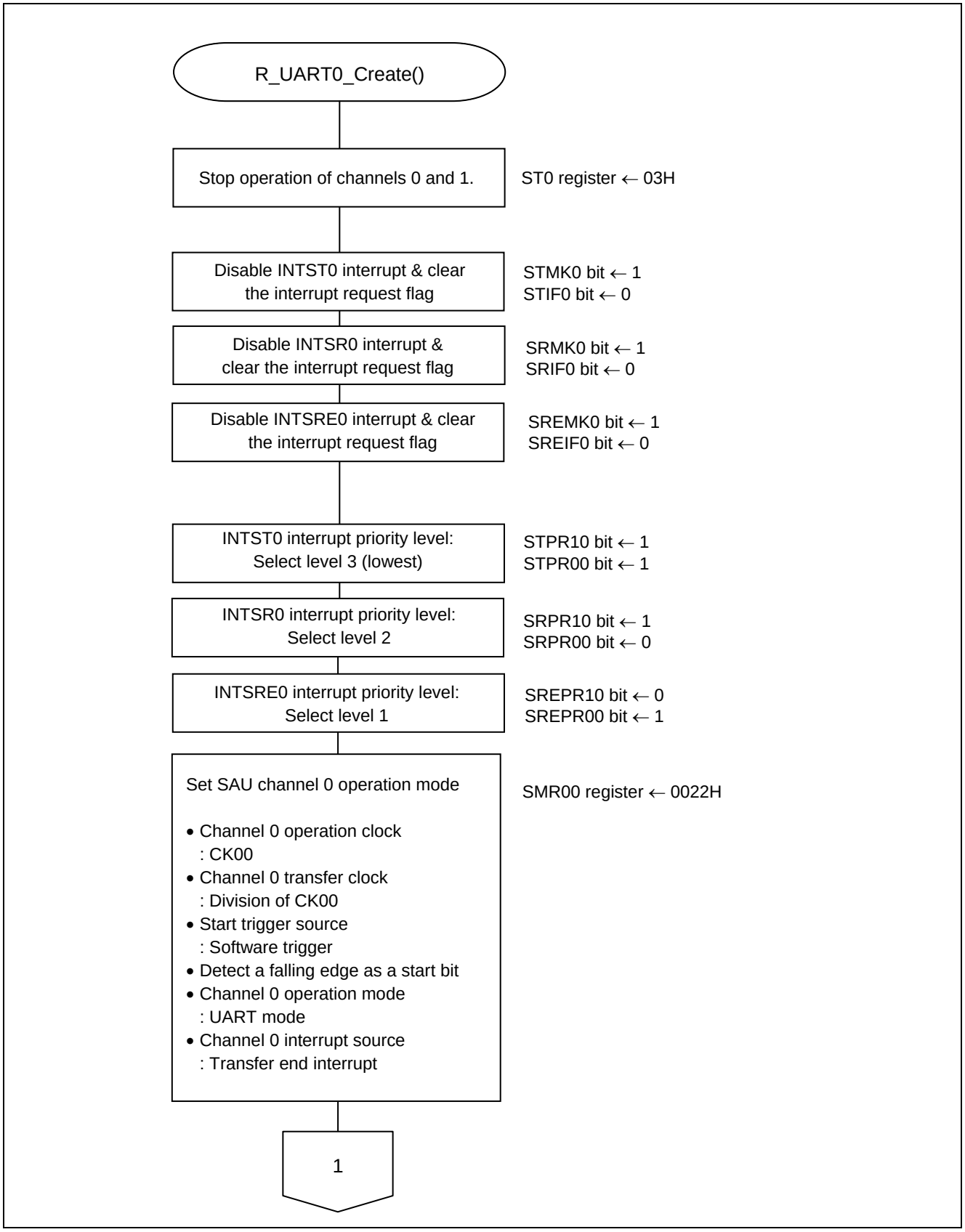

Figure 5.7 UART0 Setup (1/3)

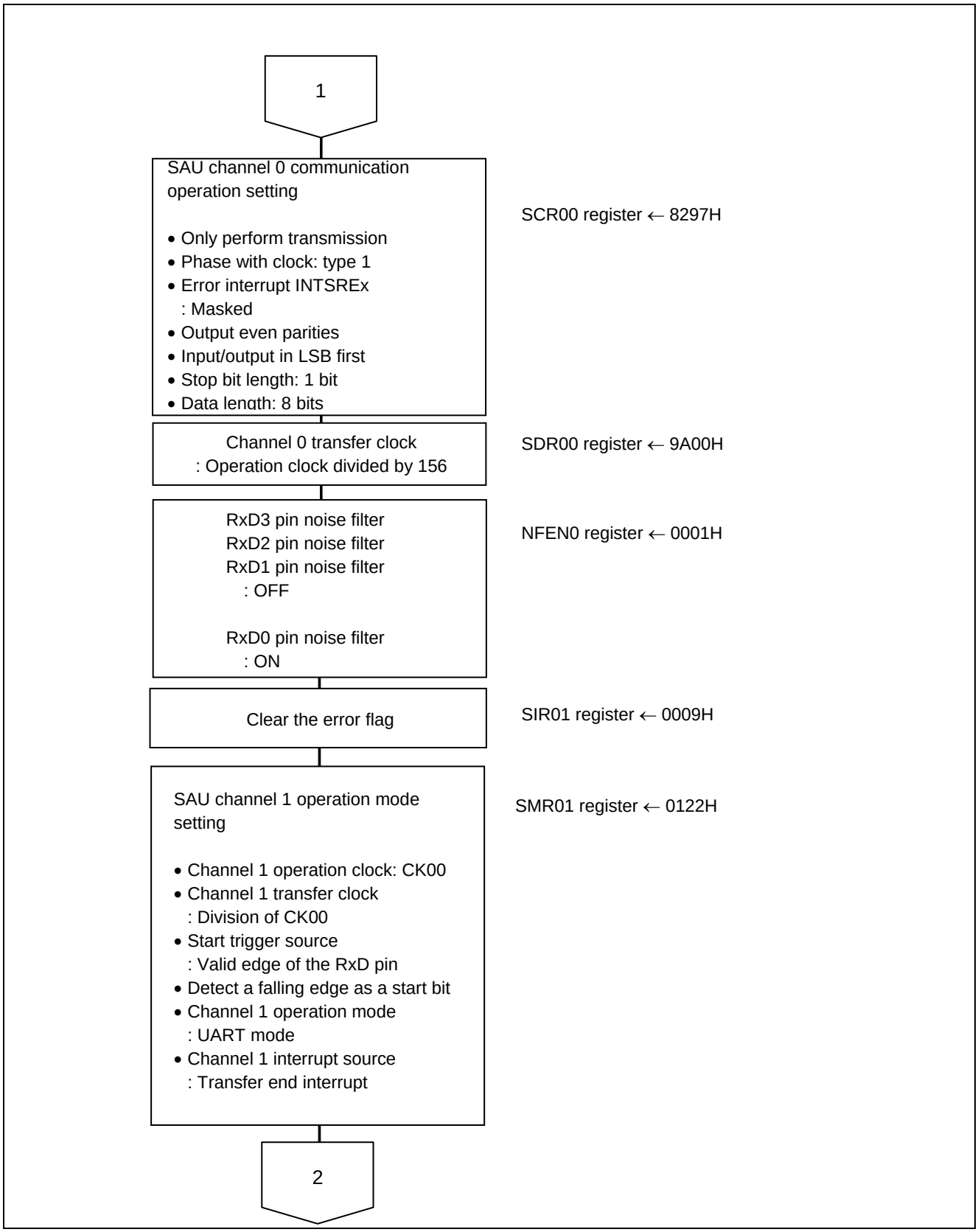

Figure 5.8 UART0 Setup (2/3)

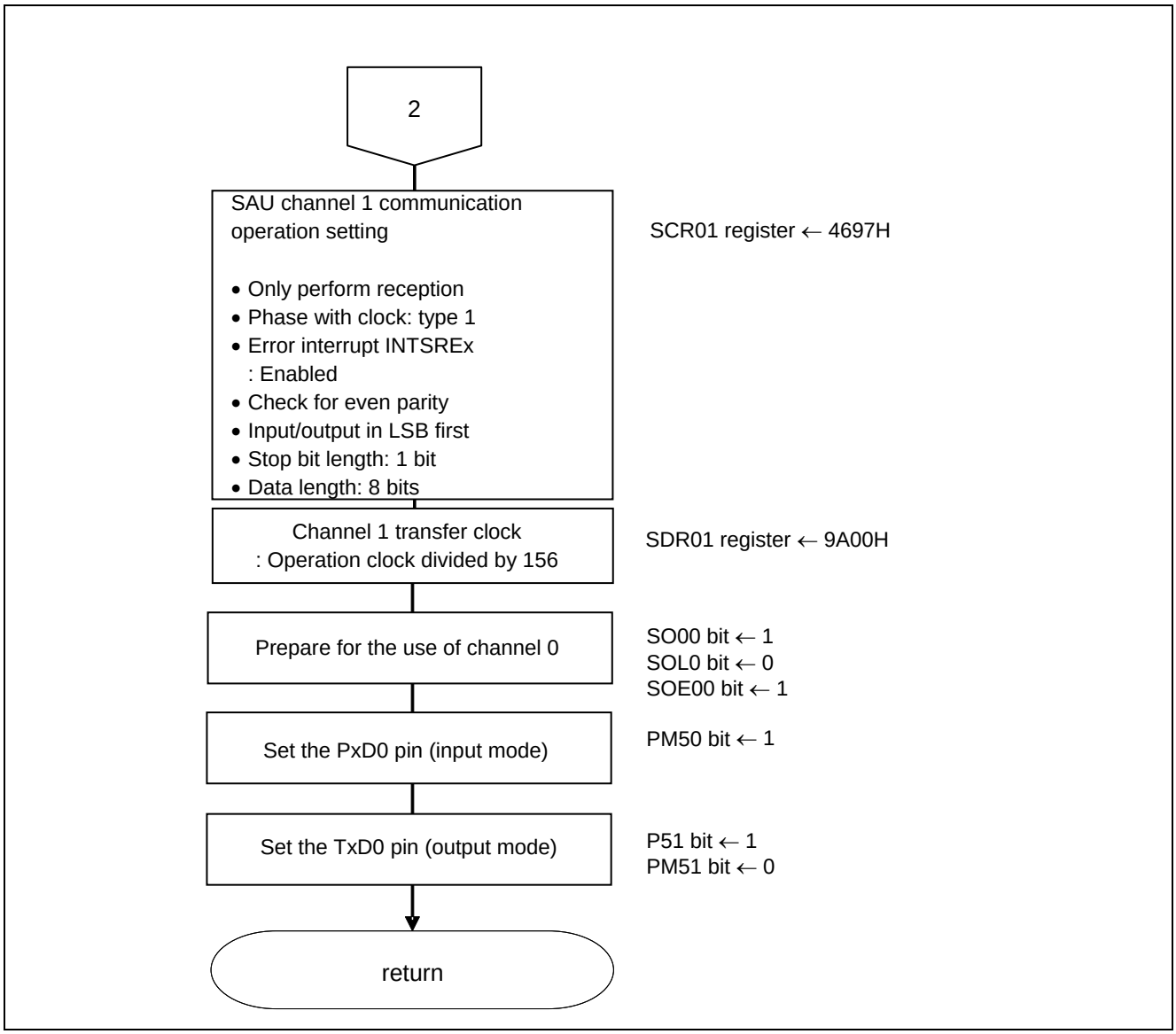

Figure 5.9 UART0 Setup (3/3)

Transmission channel operation mode setting

- Serial mode register 00 (SMR00)
  Interrupt source
  Operation mode
  Transfer clock selection
  f_{MCK} selection

Symbol: SMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 00	CCS 00	0	0	0	0	0	0	0	0	1	0	0	MD 002	MD 001	MD 000
0	**0**	0	0	0	0	0	0	0	0	1	0	0	**0**	**1**	**0**

Bit 15

CKS00	Channel 0 operation clock (f_{MCK}) selection
0	**Prescaler output clock CK00 configured by the SPS0 register**
1	Prescaler output clock CK01 configured by the SPS0 register

Bit 14

CCS00	Channel 0 transfer clock (TCLK) selection
0	**Clock obtained by dividing the operation clock f_{MCK} specified by the CKS00 bit.**
1	Clock input from the SCK pin.

Bits 2 and 1

MD002	MD001	Channel 0 operation mode setting
0	0	CSI mode
0	**1**	**UART mode**
1	0	Simplified I^2C mode
1	1	Setting prohibited

Bit 0

MD000	Channel 0 interrupt source selection
0	**Transfer end interrupt**
1	Buffer empty interrupt

Caution: For details on the register setup procedures, refer to RL78/L12 User's Manual: Hardware.

Transmission channel communication operation setting

- Serial communication operation setting register 00 (SCR00)
  Data length setting, data transfer order, error interrupt signal mask availability, and operation mode

Symbol: SCR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXE00	RXE00	DAP00	CKP00	0	EOC00	PTC001	PTC000	DIR00	0	SLC001	SLC000	0	1	DLS001	DLS000
1	**0**	**0**	**0**	0	**0**	**1**	**0**	**1**	0	**0**	**1**	0	1	**1**	**1**

Bits 15 and 14

TXE00	RXE00	Channel 0 operation mode setting
0	0	Communication prohibited
0	1	Reception Only
1	**0**	**Transmission only**
1	1	Both transmission and reception

Bit 10

EOC00	Error interrupt signal (INTSREx (x = 0, 1)) mask availability selection
0	**Error interrupt INTSREx is masked**
1	Generation of error interrupt INTSREx is enabled

Bits 9 and 8

PTC001	PTC000	Parity bit setting in UART mode	
		Transmission	Reception
0	0	No parity bit is output	Data is received without parity
0	1	0 parity is output	No parity check is made
1	**0**	**Even parity is output**	Check is made for even parity
1	1	Odd parity is output	Check is made for odd parity

Bit 7

DIR00	Selection of data transfer order in CSI and UART modes
0	Input and output in MSB first
1	**Input and output in LSB first**

Bits 5 and 4

SLC001	SLC000	Stop bit setting in UART mode
0	0	No stop bit
0	**1**	**Stop bit length = 1 bit**
1	0	Stop bit length = 2 bits
1	1	Setting prohibited

Caution: For details on the register setup procedures, refer to RL78/L12 User's Manual: Hardware.

Symbol: SCR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXE 00	RXE 00	DAP 00	CKP 00	0	EOC 00	PTC 001	PTC 000	DIR 00	0	SLC 001	SLC 000	0	1	DLS 001	DLS 000
1	**0**	**0**	**0**	0	**0**	**1**	**0**	**1**	0	**0**	**1**	0	1	**1**	**1**

Bits 1 and 0

DLS001	DLS000	Data length setting in CSI mode
0	1	9-bit data length
1	0	7-bit data length
1	**1**	**8-bit data length**
Others		Setting prohibited

Transmission channel transfer clock setting

- Serial data register 00 (SDR00)
  Transfer clock frequency: f_{MCK}/156(≈ 9600 Hz)

Symbol: SDR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	**0**	**0**	**1**	**1**	**0**	**1**	0	x	x	x	x	x	x	x	x

Bits 15 to 9

SDR00[15:9]							Transfer clock setting by dividing operation clock (f_{MCK})
0	0	0	0	0	0	0	f_{MCK} /2
0	0	0	0	0	0	1	f_{MCK} /4
0	0	0	0	0	1	0	f_{MCK} /6
0	0	0	0	0	1	1	f_{MCK} /8
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
1	**0**	**0**	**1**	**1**	**0**	**1**	**f_{MCK} /156**
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
1	1	1	1	1	1	0	f_{MCK} /254
1	1	1	1	1	1	1	f_{MCK} /256

Caution: For details on the register setup procedures, refer to RL78/G1C User's Manual: Hardware.

Reception channel operation mode setting

- Serial mode register 01 (SMR01)
  Interrupt source
  Operation mode
  Transfer clock selection
  f_{MCK} selection

Symbol: SMR01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 01	CCS 01	0	0	0	0	0	STS 01	0	SIS 010	1	0	0	MD 012	MD 011	MD 010
0	**0**	0	0	0	0	0	**1**	0	**0**	1	0	0	**0**	**1**	**0**

Bit 15

CKS01	Channel 1 operation clock (f_{MCK}) selection
0	**Prescaler output clock CK00 configured by the SPS0 register**
1	Prescaler output clock CK01 configured by the SPS0 register

Bit 14

CCS01	Channel 1 transfer clock (TCLK) selection
0	**Clock obtained by dividing the operation clock f_{MCK} specified by the CKS01 bit**
1	Clock input from the SCK pin

Bit 8

STS01	Start trigger source selection
0	Only software trigger is valid
1	**Valid edge of the RxD pin (selected during UART reception)**

Bit 6

SIS010	Control of receive data level inversion on channel 1 in UART mode
0	**Falling edge is detected as a start bit**
1	Rising edge is detected as a start bit

Bits 2 and 1

MD012	MD011	Channel 1 operation mode setting
0	0	CSI mode
0	**1**	**UART mode**
1	0	Simplified I^2C mode
1	1	Setting prohibited

Bit 0

MD010	Channel 1 interrupt source selection
0	**Transfer end interrupt**
1	Buffer empty interrupt

Caution: For details on the register setup procedures, refer to RL78/L12 User's Manual: Hardware.

Reception channel communication operation setting

- Serial communication operation setting register 01 (SCR01)
  Data length setting, data transfer order, error interrupt signal mask availability, and operation mode

Symbol: SCR01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXE01	RXE01	DAP01	CKP01	0	EOC01	PTC011	PTC010	DIR01	0	0	SLC010	0	1	DLS011	DLS010
0	**1**	**0**	**0**	0	**1**	**1**	**0**	**1**	0	0	**1**	0	1	**1**	**1**

Bits 15 and 14

TXE01	RXE01	Channel 1 operation mode setting
0	0	Communication prohibited
0	**1**	**Reception only**
1	0	Transmission only
1	1	Both transmission and reception

For UART reception, wait for 4 f_{CLK} clock cycles or more before setting SS01 to 1, after setting the RXE01 bit of the SCR01 register to 1.

Bit 10

EOC01	Error interrupt signal (INTSRE1) mask availability selection
0	Error interrupt INTSRE1 is masked
1	**Generation of error interrupt INTSRE1 is enabled**

Bits 9 and 8

PTC011	PTC010	Parity bit setting in UART mode	
		Transmission	Reception
0	0	No parity bit is output	Data is received without parity
0	1	0 parity is output	No parity check is made
1	**0**	Even parity is output	**Check is made for even parity**
1	1	Odd parity is output	Check is made for odd parity

Bit 7

DIR01	Selection of data transfer order in CSI and UART modes
0	Input and output in MSB first
1	**Input and output in LSB first**

Bits 5 and 4

SLC011	SLC010	Stop bit setting in UART mode
0	0	No stop bit
0	**1**	**Stop bit length = 1 bit**
1	0	Stop bit length = 2 bits
1	1	Setting prohibited

Caution: For details on the register setup procedures, refer to RL78/L12 User's Manual: Hardware.

Symbol: SCR01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXE 01	RXE 01	DAP 01	CKP 01	0	EOC 01	PTC 011	PTC 010	DIR 01	0	0	SLC 010	0	1	DLS 011	DLS 010
0	**1**	**0**	**0**	0	**1**	**1**	**0**	**1**	0	0	**1**	0	1	**1**	**1**

Bits 1 and 0

DLS011	DLS010	Data length setting in CSI mode
0	1	9-bit data length
1	0	7-bit data length
1	**1**	**8-bit data length**
others		Setting prohibited

Reception transfer clock setting

- Serial data register 01 (SDR01)
  Transfer clock frequency: f_{MCK}/156 (≈ 9600 Hz)

Symbol: SDR01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	**0**	**0**	**1**	**1**	**0**	**1**	0								

Bits 15 to 9

SDR01[15:9]							Transfer clock setting by dividing operation clock (f_{MCK})
0	0	0	0	0	0	0	f_{MCK} /2
0	0	0	0	0	0	1	f_{MCK} /4
0	0	0	0	0	1	0	f_{MCK} /6
0	0	0	0	0	1	1	f_{MCK} /8
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
1	**0**	**0**	**1**	**1**	**0**	**1**	**f_{MCK} /156**
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
1	1	1	1	1	1	0	f_{MCK} /254
1	1	1	1	1	1	1	f_{MCK} /256

Caution: For details on the register setup procedures, refer to RL78/L12 User's Manual: Hardware.

Initial output level setting

- Serial output register 0 (SO0)
  Initial output: 1

Symbol: SO0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	CKO 03	CKO 02	CKO 01	CKO 00	0	0	0	0	SO 03	SO 02	SO 01	SO 00
0	0	0	0	x	x	x	x	0	0	0	0	x	x	x	**1**

Bit 0

SO00	Channel 0 serial data output
0	Serial data output value is “0”
1	**Serial data output value is “1”**

Enabling of data output on target channel

- Serial output enable register 0 (SOE0)
  Output enable

Symbol: SOE0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	SOE 03	SOE 02	SOE 01	SOE 00
0	0	0	0	0	0	0	0	0	0	0	0	x	x	x	**1**

Bit 0

SOE00	Channel 0 serial output enable/stop
0	Serial communication output is stopped
1	**Serial communication output is enabled**

Caution: For details on the register setup procedures, refer to RL78/L12 User's Manual: Hardware.

Port setting

- Port register 1 (P1)
- Port mode register 1 (PM1)
  Port setting for each of transmit data and receive data.

Symbol: P1

7	6	5	4	3	2	1	0
P17	P16	P15	P14	P13	P12	P11	P10
0	0	0	0	0	**1**	x	x

Bit 2

P12	Output data control (in output mode)
0	0 is output
1	**1 is output**

Symbol: PM1

7	6	5	4	3	2	1	0
PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10
x	x	x	x	x	**0**	**1**	x

Bit 2

PM51	P51 I/O mode selection
0	**Output mode (output buffer is on)**
1	Input mode (output buffer is off)

Bit 1

PM50	P50 I/O mode selection
0	Output mode (output buffer is on)
1	**Input mode (output buffer is off)**

Caution: For details on the register setup procedures, refer to RL78/L12 User's Manual: Hardware.

5.7.7 Main Function

Figures 5.10, 5.11 and 5.12 show the flowchart for the main function.

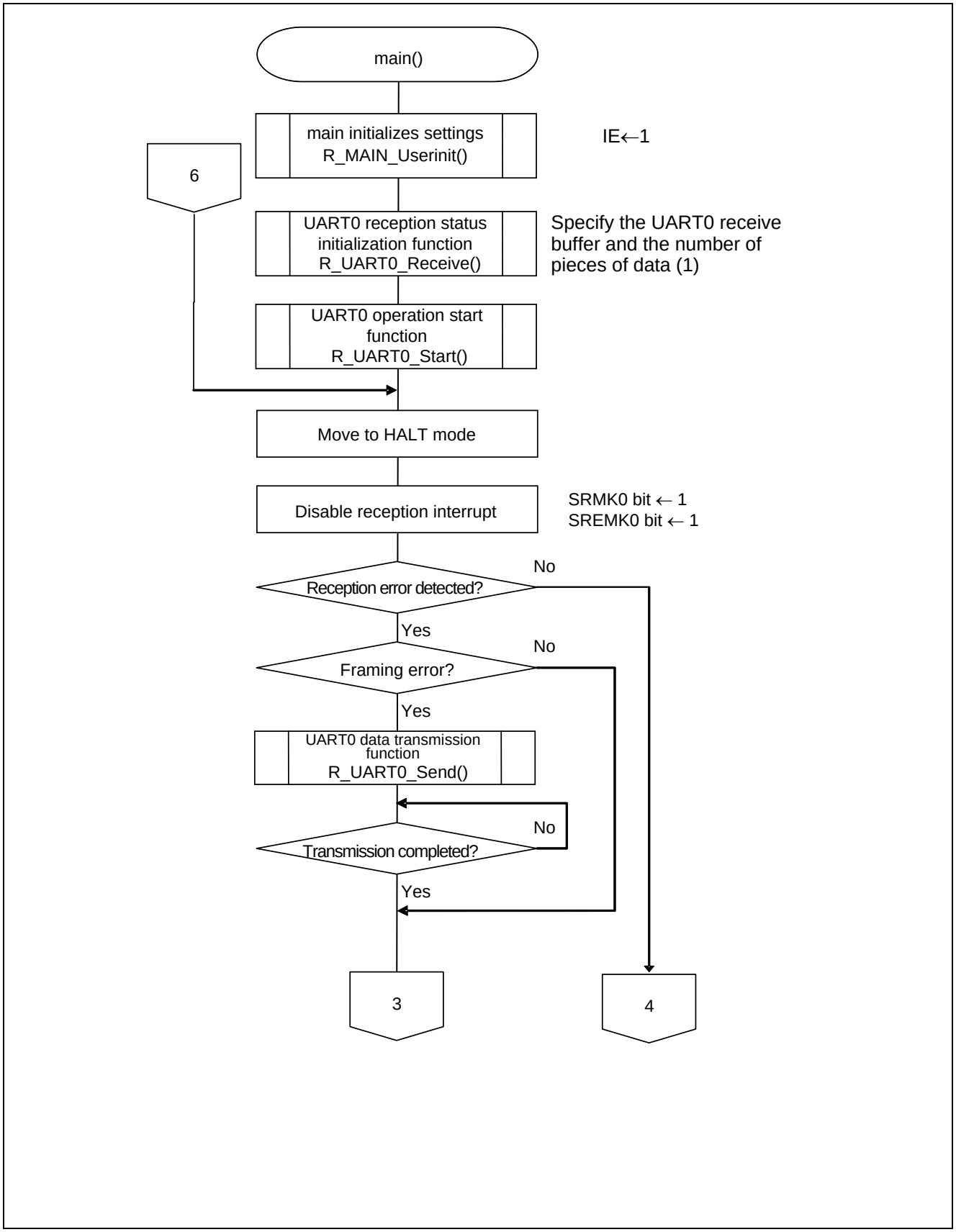

Figure 5.10 Main Function (1/3)

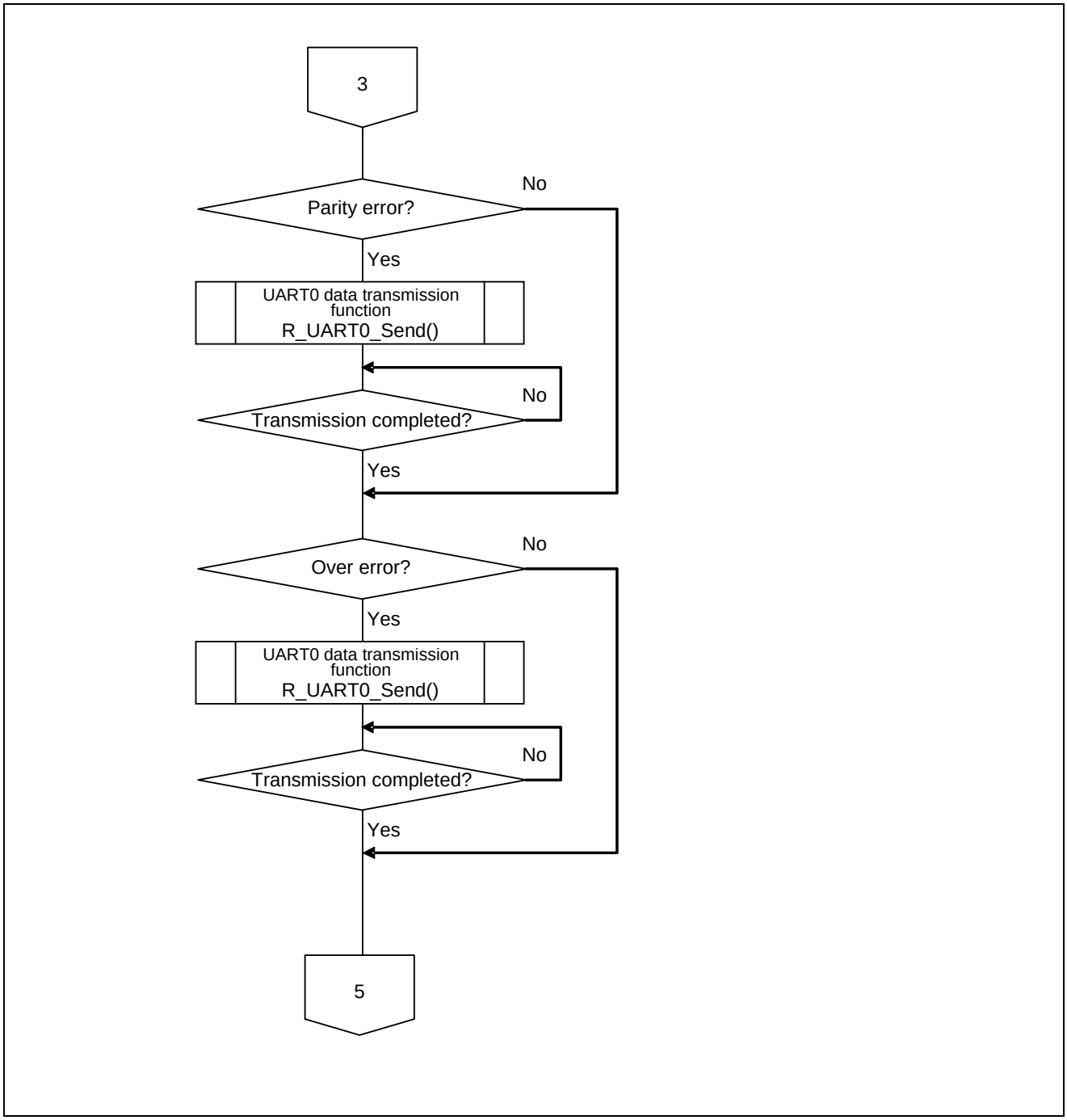

Figure 5.11 Main Function (2/3)

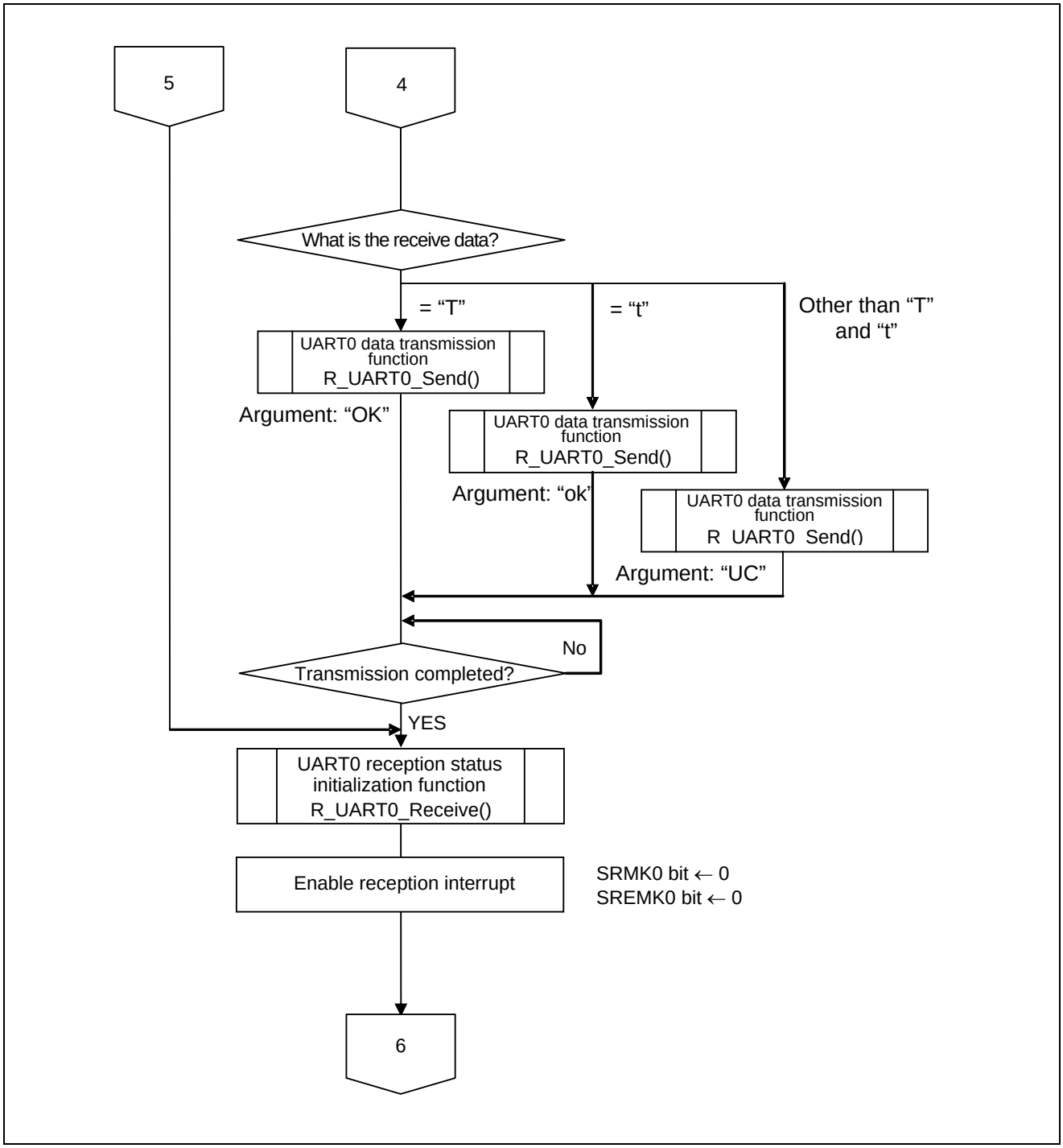

Figure 5.12 Main Function (3/3)

5.7.8 Main initializes settings

Figure 5.13 shows the flowchart for the main initializes settings.

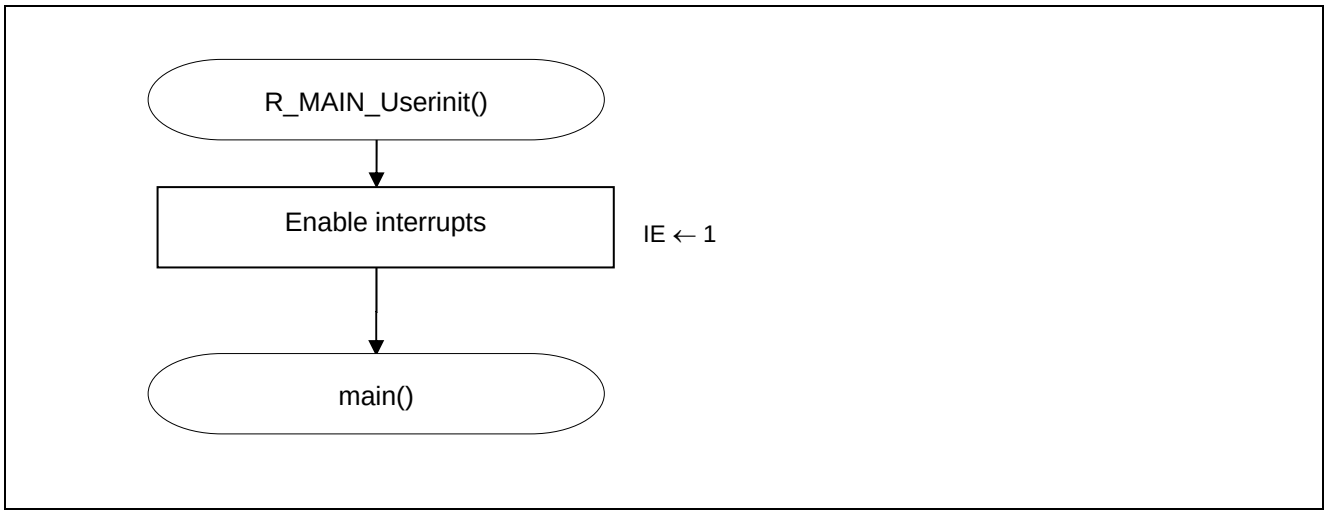

Figure 5.13 Main initializes settings

5.7.9 UART0 Reception Status Initialization Function

Figure 5.14 shows the flowchart for the UART0 reception status initialization function.

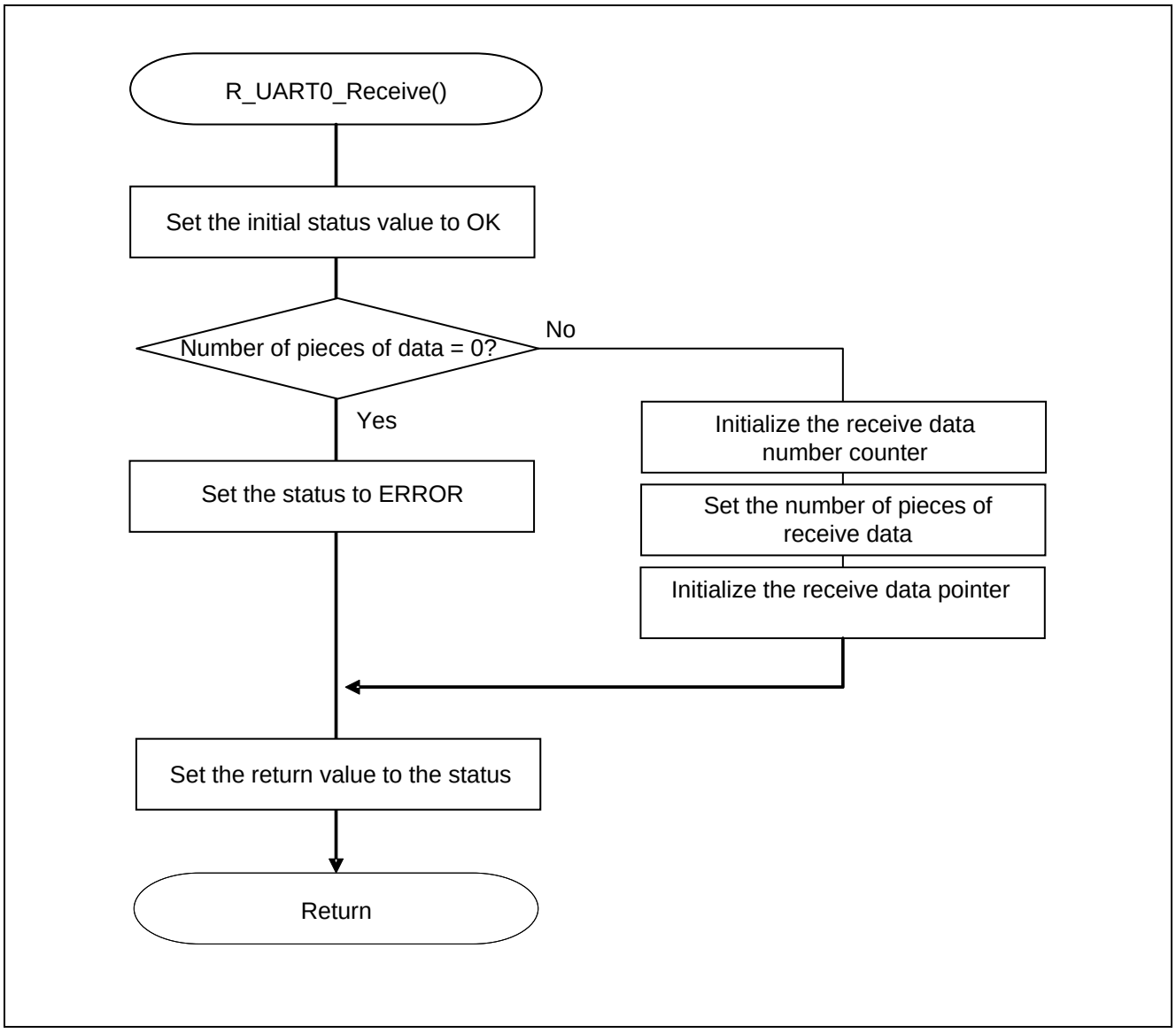

Figure 5.14 UART0 Reception Status Initialization Function

5.7.10 UART0 Operation Start Function

Figure 5.15 shows the flowchart for the UART0 operation start function.

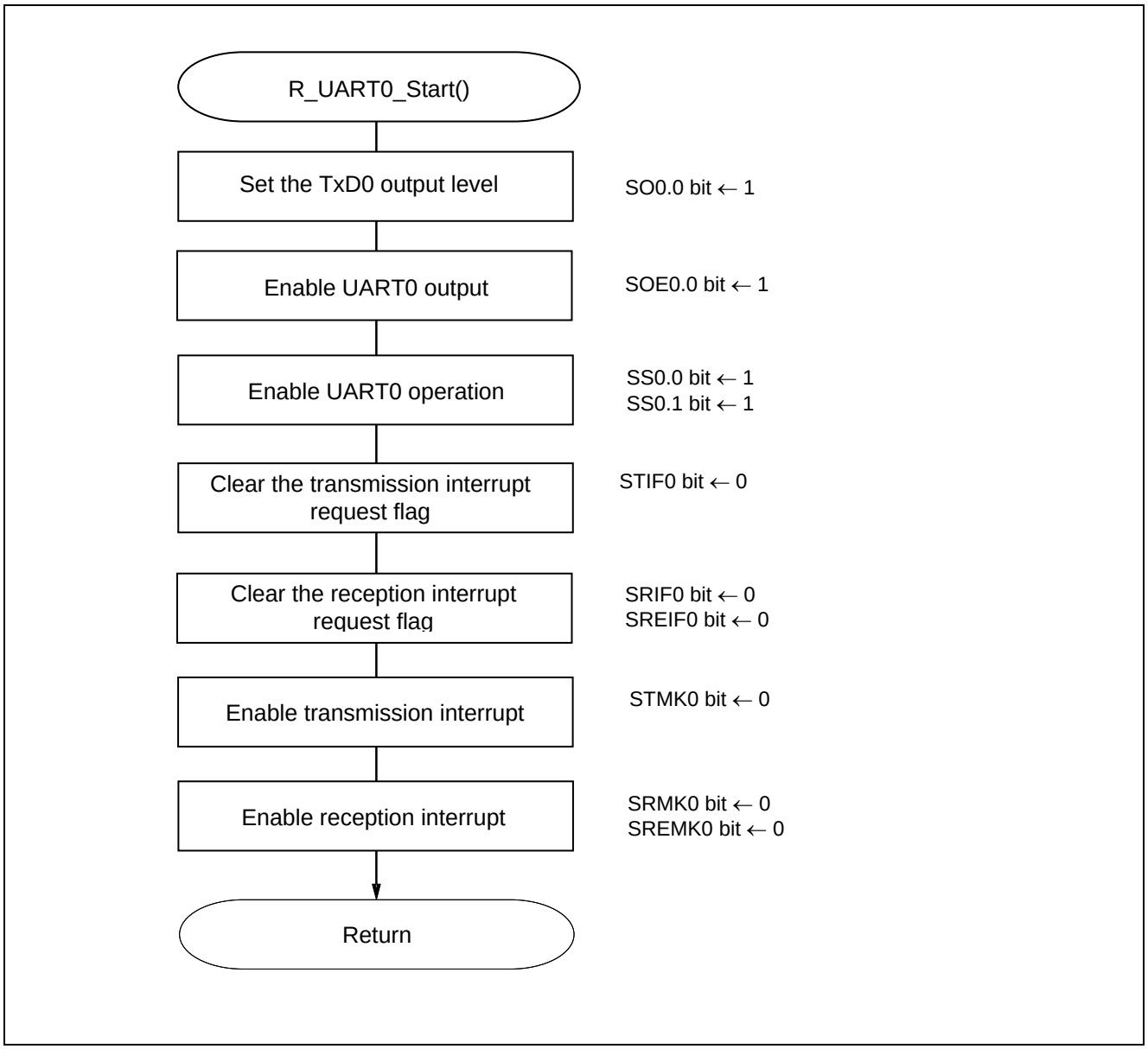

Figure 5.15 UART0 Operation Start Function

Interrupt setting

- Interrupt request flag register (IF0H)
  Clear the interrupt request flag
- Interrupt mask flag register (MK0H)
  Cancel interrupt mask

Symbol: IF0H

7	6	5	4	3	2	1	0
0	TMIF00	0	SREIF0 TMIF0H	SRIF0 CSIIF01	STIF0 CSIIF00	DMAIF1	DMAIF0
0	x	0	**0**	**0**	**0**	x	x

Bit 4

SREIF0	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Bit 3

SRIF0	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Bit 2

STIF0	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Caution: For details on the register setup procedures, refer to RL78/L12 User's Manual: Hardware.

Symbol: MK0H

7	6	5	4	3	2	1	0
0	TMIF00	0	SREIF0 TMIF0H	SRIF0 CSIIF01	STIF0 CSIIF00	DMAIF1	DMAIF0
0	x	0	**0**	**0**	**0**	x	x

Bit 4

SREMK0	Interrupt processing control
0	**Enables interrupt processing.**
1	Disables interrupt processing.

Bit 3

SRMK0	Interrupt processing control
0	**Enables interrupt processing.**
1	Disables interrupt processing.

Bit 2

STMK0	Interrupt processing control
0	**Enables interrupt processing.**
1	Disables interrupt processing.

Caution: For details on the register setup procedures, refer to RL78/L12 User's Manual: Hardware.

Transition to communication wait state

- Serial channel start register 0 (SS0)
  Operation start

Symbol: SS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	SS01	SS00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**Note	**1**

Bits 3 to 0

SS0n	Channel n operation start trigger
0	Trigger operation is not performed
1	**SE0n is set to 1, and a communication wait state is entered.**

Note For UART reception, wait for 4 f_{CLK} clock cycles or more before setting SS0n to 1, after setting the RXE0n bit of the SCR0n register to 1.

Caution: For details on the register setup procedures, refer to RL78/L12 User's Manual: Hardware.

5.7.11 INTSR0 Interrupt Service Routine

Figure 5.16 shows the flowchart for the INTSR0 interrupt service routine.

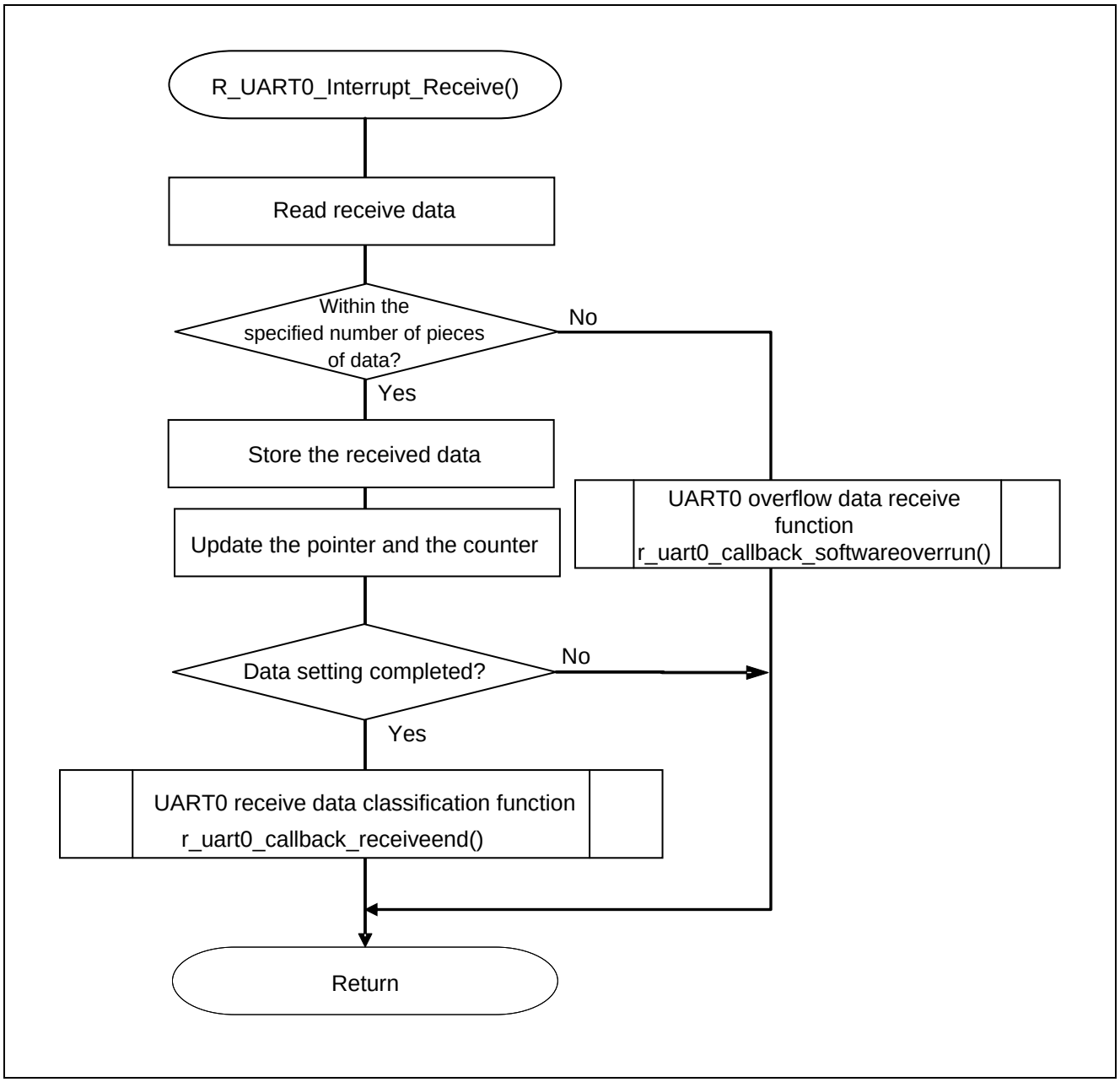

Figure 5.16 INTSR0 Interrupt Service Routine

5.7.12 UART0 Receive Data Classification Function

Figure 5.17 shows the flowchart for the UART0 receive data classification function.

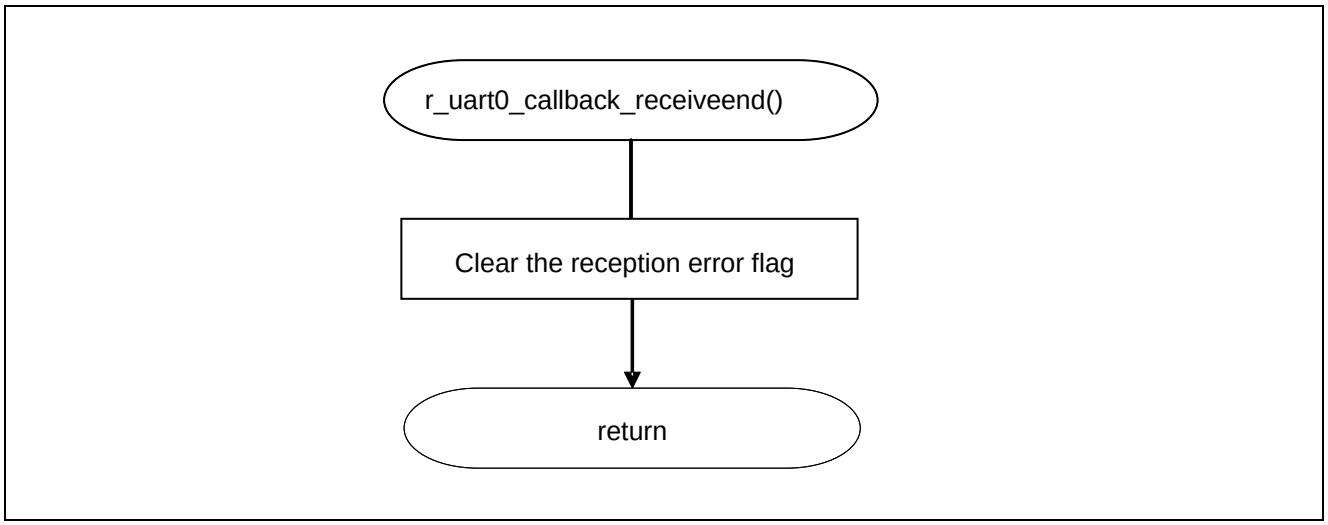

Figure 5.17 UART0 Receive Data Classification Function

5.7.13 UART0 Data Transmission Function

Figure 5.18 shows the flowchart for the UART0 data transmission function.

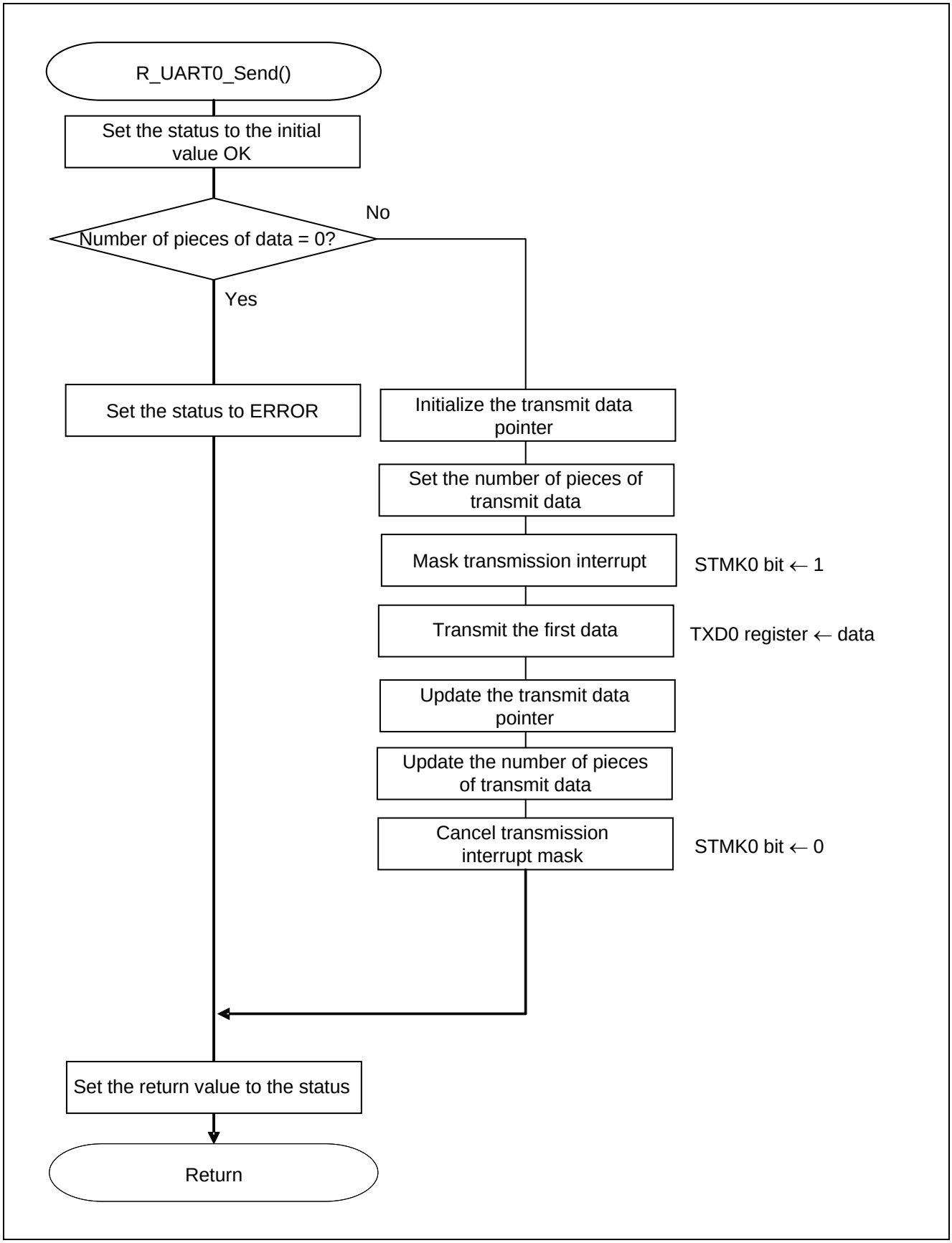

Figure 5.18 UART0 Data Transmission Function

5.7.14 UART0 Reception Error Interrupt Function

Figure 5.19 shows the flowchart for the UART0 reception error interrupt function.

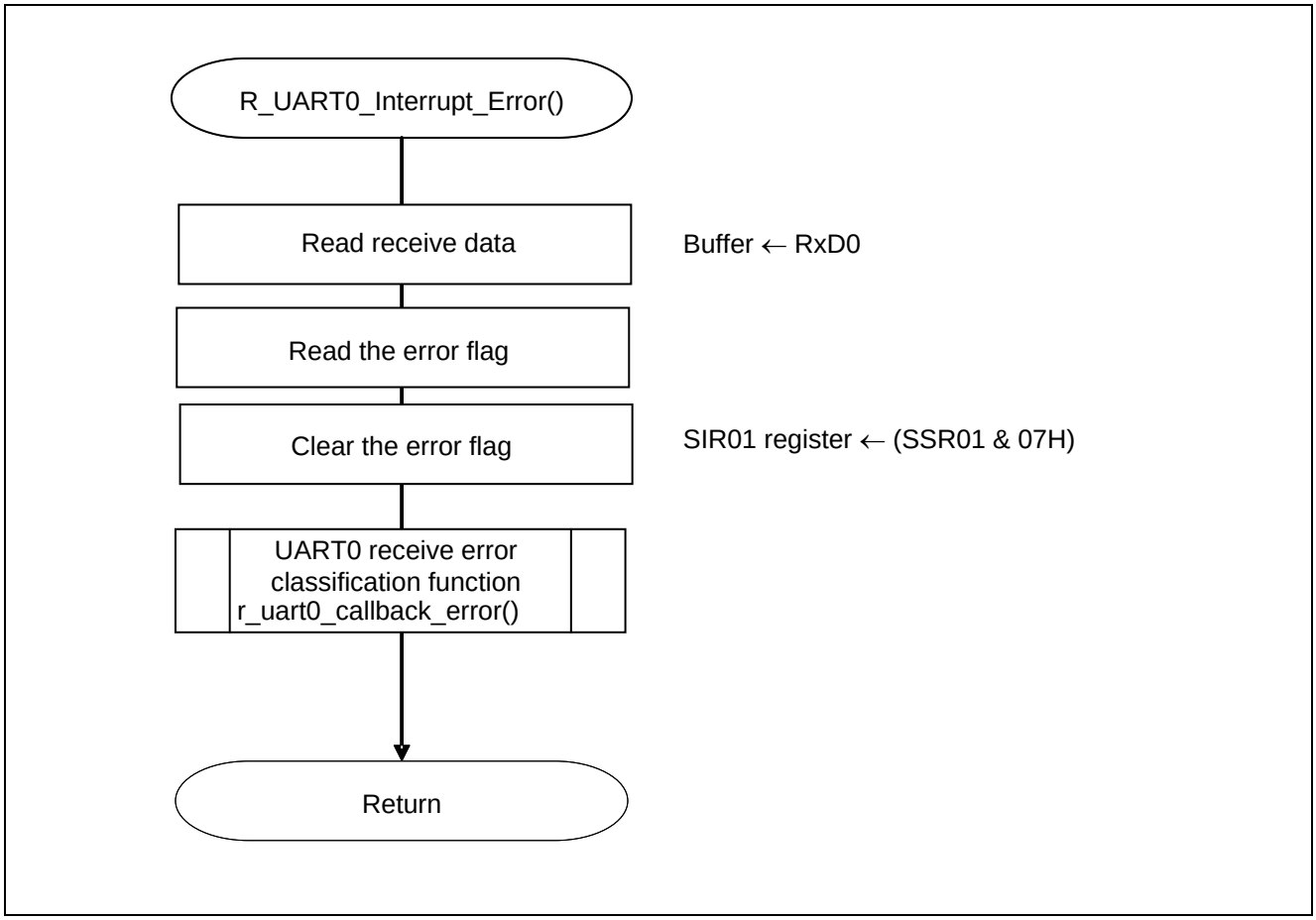

Figure 5.19 UART0 Reception Error Interrupt Function

5.7.15 UART0 Reception Error Classification Function

Figure 5.20 shows the flowchart for the UART0 reception error classification function.

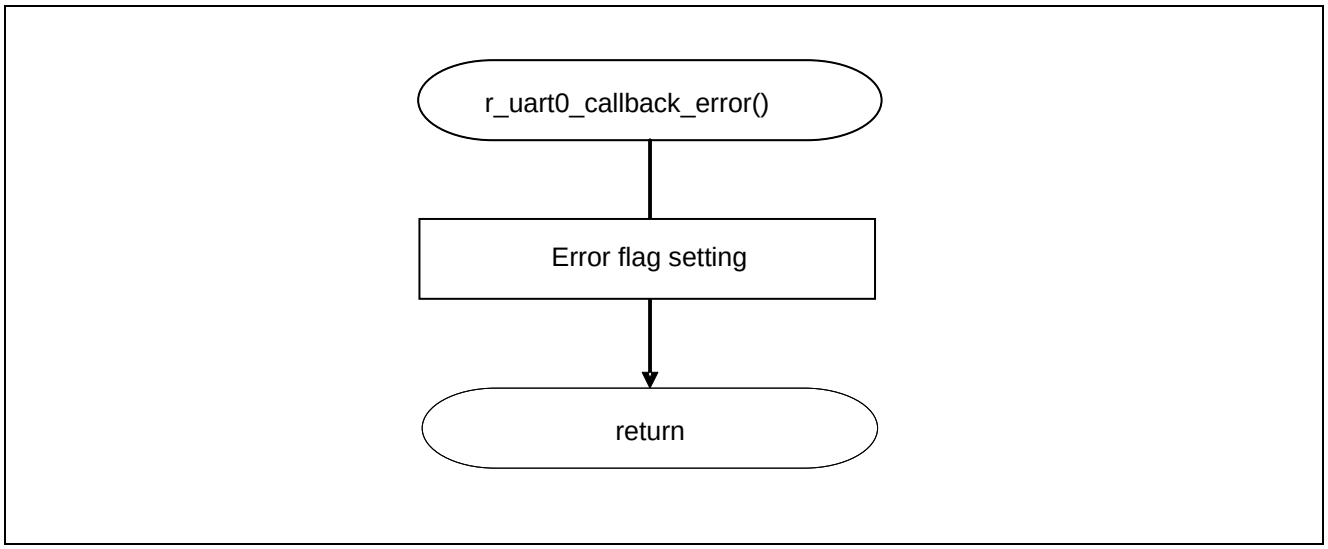

Figure 5.20 UART0 Reception Error Classification Function

5.7.16 INTST0 Interrupt Service Routine

Figure 5.21 shows the flowchart for the INTST0 interrupt service routine.

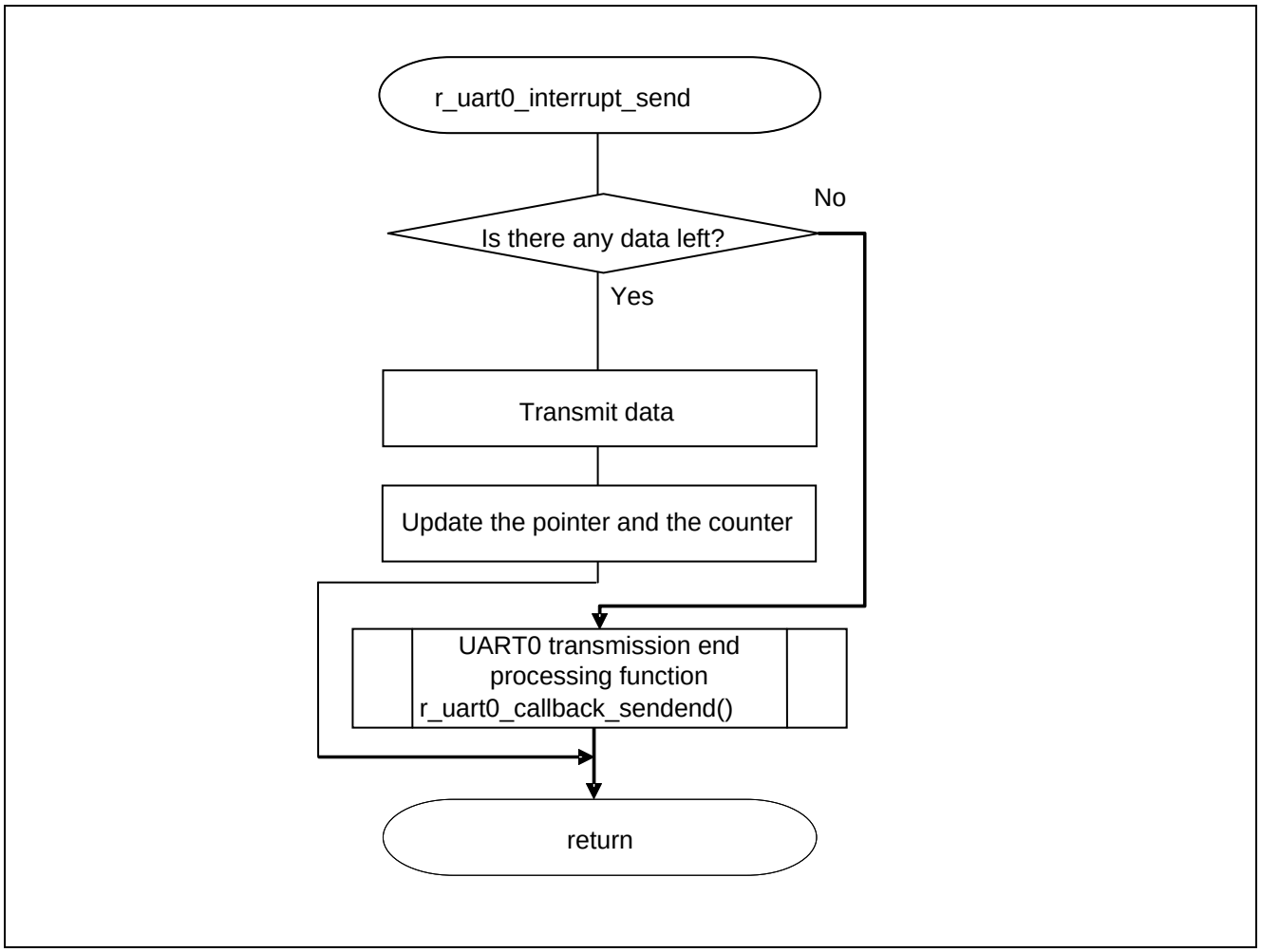

Figure 5.21 INTST0 Interrupt Service Routine

5.7.17 UART0 Transmission End Processing Function

Figure 5.22 shows the flowchart for the UART0 transmission end processing function.

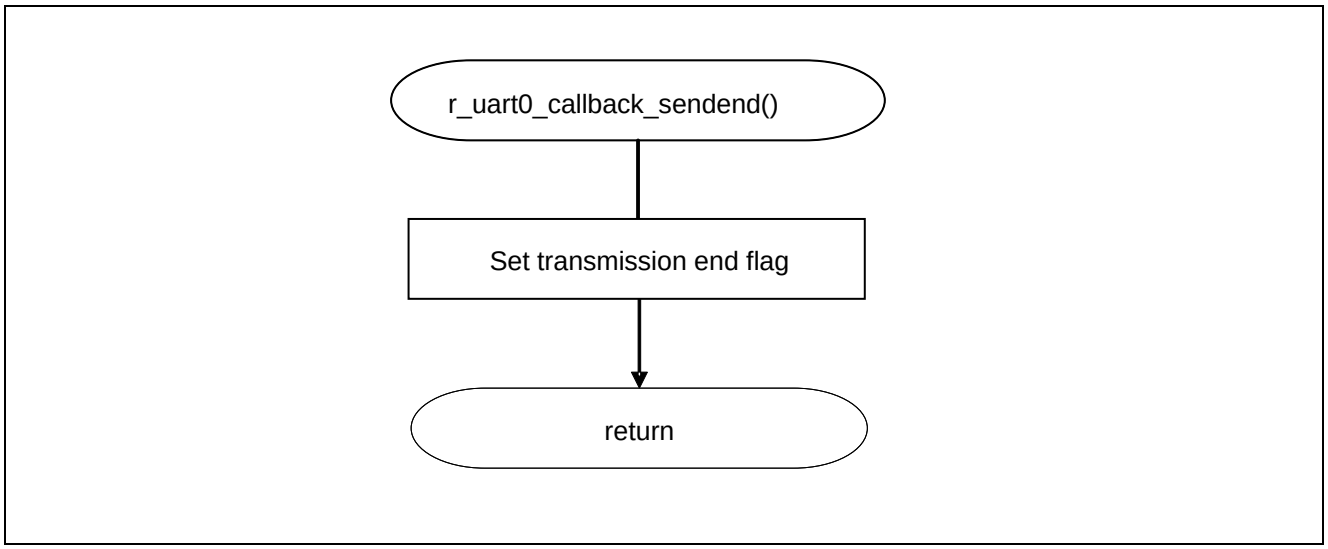

Figure 5.22 UART0 Transmission End Processing Function

6. Sample Code

The sample code is available on the Renesas Electronics Website.

7. Documents for Reference

RL78/L12 User's Manual: Hardware (R01UH0330E)

RL78 Family User's Manual: Software (R01US0015E)

(The latest versions of the documents are available on the Renesas Electronics Website.)

Technical Updates/Technical Brochures

(The latest versions of the documents are available on the Renesas Electronics Website.)

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Revision Record	RL78/L12 Serial Array Unit (UART Communication) CC-RL

Rev.	Date	Description	
		Page	Summary
1.00	July 20, 2016	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

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