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RL78/G14, H8/3687 Group

Migration Guide from H8/3687 to RL78/G14: Timer RD

Abstract

This document describes how to migrate from the H8/3687 Group timer Z to the RL78/G14 timer RD.

Target Devices

RL78/G14, H8/3687 Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.



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1. Differences between Timer Z in the H8/3687 Group and Timer RD in RL78/G14

Table 1.1 lists the differences between timer Z in the H8/3687 Group and timer RD in RL78/G14.

Item	Timer Z in H8/3687 Group	Timer RD inRL78/G14
Count source	• \$	• fCLK
	• 0 /2	• fCLK/2
	• •	• fCLK/4
	• \$ /8	• fCLK/8
	• FTIOA0 (TCLK)	• fCLK/32
		• fHOCO
		TRDCLK (Note 1)
Clock supply enable/disable	N/A	Available
Operating mode	Timer mode	Timer mode
	PWM mode	PWM mode
	(Reset synchronous, complementary PWM)	(Reset synchronous, complementary PWM, PWM3)
Count stop at compare match	N/A	Available (Select either to stop or to continue at compare match with TRDGRA0/1)
Pulse output forced cutoff method	WKP4	INTP0, ELC0, or ELC1 (Note 2)
Pin used for pulse output forced cutoff	WKP4	INTP0
Pin state setting for pulse output forced cutoff	Set the registers PCR6 and PDR6 of the corresponding I/O port.	Set the TRDDFi register.
Pulse output forced cutoff	Set 0 to the master enable bit in the	Set 0 to the TRDSHUTS bit in the
cancel method	TOER register after inputting "H" to	TRDOER2 register after inputting "H"
	WKP4 pin.	to the INTP0 pin.
Timer Z/RD pins	P6_0 to P6_7 (Note 3)	P10 to P17 (Note 3)
Digital filter	N/A	Available
A/D trigger generation	Available (Note 4)	N/A (Note 5)
Event input from ELC	N/A	Available

i = 0 or 1

Notes

- 1. TRDCLK cannot be selected in the PWM3 mode.
- The pulse output is cutoff during the low input period for forced cutoff from the INTP0 pin, but the pulse output is cutoff once by a single event input from the ELC for forced cutoff by the ELC event. Setting procedures: (1) Set timer RD as the ELC event link destination. (2) Set bits ELCICEi (i = 0 or 1) and ELCOBEi (i = 0 or 1) in the TRDELC register to 1.
- 3. See Table 1.2.
- 4. This function is valid only in the complementary PWM mode.
- 5. Using the event link controller enables to generate an A/D trigger. The trigger is generated at peak in the complementary PWM mode.
 - Event source: Timer RD0 input capture A/compare match A
 - Event link destination: A/D converter

The trigger is generated at trough in the complementary PWM mode.

- Event source: Timer RD1 underflow
- Event link destination: A/D converter

1.1 Assigned I/O Pins

Table 1.2 lists the assigned I/O pins to use in the timer Z in the H8/3687 Group and the timer RD in RL78/G14.

Table 1.2 I/O Pins in the H8/3687 Group and RL78/G14
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Pin name	H8/3687 Group	Pin name	RL78/G14	I/O
FTIOA0/TCLK	P6_0	TRDIOA0/TRDCLK	P17	I/O
FTIOB0	P6_2	TRDIOB0	P15	I/O
FTIOC0	P6_1	TRDIOC0	P16	I/O
FTIOD0	P6_3	TRDIOD0	P14	I/O
FTIOA1	P6_4	TRDIOA1	P13	I/O
FTIOB1	P6_5	TRDIOB1	P12	I/O
FTIOC1	P6_6	TRDIOC1	P11	I/O
FTIOD1	P6_7	TRDIOD1	P10	I/O



2. Register Compatibility

Register compatibility between the H8/3687 Group and RL78/G14 is listed in Table 2.1.

Table 2.1 Register Compatibility

Item	H8/3687 Group	RL78/G14
Clock supply enable/disable		TRD0EN bit in the PER1 register
Timer RD synchronous	SYNC bit in the TMDR register	TRDSYNC bit in the TRDMR register
General register/buffer register select	BFki bit in the TMDR register	TRDBFki bit in the TRDMR register
Timer mode/PWM mode select	PWMBi bit in the TPMR register, PWMCi bit in the PWMDi register	Bits TRDPWMBi, TRDPWMCi, and TRDPWMDi in the TRDPMR register
PWM3 mode setting	—	PWM3 bit in the TRDFCR register
Count select at compare match with TRDGRAi	_	CSELi bit in the TRDSTR register
A/D trigger enable	ADTRG bit in the TFCR register	—
A/D trigger edge select	ADEG bit in the TFCR register	—
Pulse output forced cutoff signal input enable	WKP4 bit in the PMR5 register	TRDPTO bit in the TRDOER2 register
TRDIOj pin digital filter function enable	_	DFj bit in the TRDDFi register
Digital filter function clock select	_	DFCKi bit in the TRDDFi register
Count source select	Bits TPSC0 to TPSC2 in the TCRi register	Bits TCK0 to TCK2 in the TRDCRi register
Interrupt priority level select	_	 TRDPR0i bit in the PR02H register TRDPR1i bit in the PR12H register
Interrupt request bit	Bits UDF ^(Note 1) , OVF, and IMFj in the TSRi register	TRDIFi bit in the IF2H register
Interrupt enable/disable	Bits OVIE and IMIEj in the TIERi register	TRDMKi bit in the MK2H register
Forced cutoff flag	_	TRDSHUTS bit in the TRDOER2 register
TRDIOB pin pulse forced cutoff control	_	PENBi bit in the TRDDFi register
ELC event input i select for input capture		ELCICEi bit in the TRDELC register
ELC event input i enable for pulse output forced cutoff	_	ELCOBEi bit in the TRDELC register

-: No register is applicable.

i = 0 or 1

 $j=A,\,B,\,C,\,or\;D$

k = C or D

Note

1. The TSR0 register has no UDF flag. Bit 5 in the TSR0 register is reserved. This bit is always read as 1.

2.1 Changes in Registers

2.1.1 PER1 register (i = 0 or 1) (RL78/G14 Only)

In RL78/G14, consumption power and noise can be reduced by setting the TRD0EN bit in the PER1 register to 0 for stopping clock supply. When using the timer RD, make sure to set the bit 4 (TRD0EN) to 1.

• PER1 (RL78/G14)

_	b7	b6	b5	b4	b3	b2	b1	b0
	DACEN	TRGEN	CMPEN	TRD0EN	DTCEN		—	TRJ0EN

2.1.2 TFCR Register and TRDFCR Register

In the H8/3687 Group, whether to enable or disable an A/D trigger can be selected by setting the ADTRG bit in the TFCR register, and an A/D trigger edge can be selected by the ADEG bit in the TFCR register.

In RL78/G14, the timer RG cannot be used as an A/D conversion start trigger.

The PWM3 bit has been added to RL78/G14 for setting the PWM3 mode. However, the PWM3 mode cannot be used in the H8/3687 Group.

• TFCR (H8/3687 Group)

 b7	b6	b5	b4	b3	b2	b1	b0
_	STCLK	ADEG	ADTRG	OLS1	OLS0	CMD1	CMD0

• TRDFCR (RL78/G14)

_	b7	b6	b5	b4	b3	b2	b1	b0
	PWM3	STCLK			OLS1	OLS0	CMD1	CMD0



2.1.3 TRDDFi Register (i = 0 or 1) (RL78/G14 Only)

In RL78/G14, the digital filter function of the TRDIOj pin can be used. The bits DFj and DFCKi in the TRDDFi register are used to select whether to enable or disable the digital filter function and which clock should be used for the function. Table 2.2 lists the clocks for the digital filter function. In the H8/3687 Group, this function may not be used.

i = 0 or 1 j = A, B, C, or D

Table 2.2 Clocks for the Digital Filter Function

DFCK1	DFCK0	RL78/G14
0		fclk/32 ^(Note 1)
0		fclk/8 ^(Note 1)
1	0	fclk ^(Note 1)
1	1	Count source (Clock selected by bits TCK0 to TCK2 in the TRDCRi register)
i = 0 or 1		

Note

1. When FRQSEL4 in the user option byte (000C2H/010C2H) = 1, fcLk/32, fcLk/8, and fcLk become fHoco/32, fHoco/8, and fHoco respectively.

In RL78/G14, the bits PENB0 and PENB1 are added for TRDIOB pin pulse forced cutoff control.

• TRDDFi (RL78/G14)

_	b7	b6	b5	b4	b3	b2	b1	b0
I	DFCK1	DFCK0	PENB1	PENB0	DFD	DFC	DFB	DFA



2.1.4 TCRi Register and TRDCRi Register (i = 0 or 1)

Count source which can be specified is different between the H8/3687 Group and RL78/G14. Table 2.3 lists the comparison of count sources.

TCK2	TCK1	TCK0	H8/3687 Group TCRi	RL78/G14 TRDCRi
0	0	0	φ	fclk, fhoco
0	0	1	φ/2	fclk/2
0	1	0	φ/4	fclk/4
0	1	1	φ/8	fclk/8
1	0	0		fclk/32
1	0	1	FTIOA0 (TCLK) pin input	TRDCLK input (Note 1)
1	1	0		Do not set.
1	1	1		Do not set.

Table 2.3 Comparison of Count Sources

Note

1. This function cannot be selected in the PWM3 mode.

2.1.5 PMR5 Register and TRDOER2 Register

In the H8/3687 Group, pulse output forced cutoff signal input is enabled by setting the WKP4 bit in the PMR5 register to 1, while it is enabled in RL78/G14 by setting the TRDPTO bit in the TRDOER2 register to 1.

The TRDSHUTS bit has been added to RL78/G14 to indicate the forced cutoff. When the pulse output is forcibly cut off, the TRDSHUTS bit in the TRDOER2 register is set to 1. Such bit is not available in the H8/3687 Group.

• PMR5 (H8/3687 Group)

 b7	b6	b5	b4	b3	b2	b1	b0
POF57	POF56	WP5	WKP4	WKP3	WKP2	WKP1	WKP0

• TRDOER2 (RL78/G14)

_	b7	b6	b5	b4	b3	b2	b1	b0
	TRDPTO		—		—	—	—	TRDSHUTS

2.1.6 TRDELC Register (RL78/G14 Only)

Bits ELCICEi and ELCOBEi have been added to RL78/G14 to select the ELC event input for the input capture, and to enable the ELC event for pulse output forced cutoff (i = 0 or 1).

• TRDELC (RL78/G14)

b7	b6	b5	b4	b3	b2	b1	b0
	—	ELCOBE1	ELCICE1	_	_	ELCOBE0	ELCICE0

2.1.7 TSTR Register and TRDSTR Register

The CSELi bit has been added to RL78/G14 to set count operation at compare match with the TRDGRAi register (i = 0 or 1).

• TSTR (H8/3687 Group)

b7	b6	b5	b4	b3	b2	b1	b0
	—					STR1	STR0

• TRDSTR (RL78/G14)

b7	b6	b5	b4	b3	b2	b1	b0
-	—	—	—	CSEL1	CSEL0	TSTART1	TSTART0



3. Reference Documents

RL78/G14 User's Manual: Hardware Rev. 2.00 H8/3687 Group Hardware Manual Rev.5.00 The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

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