RL78/G14, H8/36109

Migration Guide from H8 to RL78: Band-Gap Regulator, Power-On Reset & Low-Voltage Detection Circuits

Introduction

This application note describes how to migrate Band-Gap Regulator, Power-On Reset, and Low-Voltage Detection Circuits of H8/36109 to Power-on-reset Circuit and Voltage Detector of RL78/G14.

Target Device

RL78/G14, H8/36109

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

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1.1 Differences between Power-On Reset and Power-on-reset Circuit

Table 1.1 shows the differences between Power-On Reset and Power-on-reset Circuit.

Table 1.1 Differences between Power-On Reset and Power-on-reset Circuit

Item	H8/36109 Power-On Reset	RL78/G14 Power-on-reset Circuit
Reset detection voltage	Initial value: TYP. 3.6V (3.3V to 3.9V) Falling detection voltage (Optional): TYP. 2.3V (Max. 2.6V)	Detection voltage TYP. 1.51V Rising edge: 1.51V to 1.55V Falling edge: 1.46V to 1.51V
On-chip pull-up resistor of $\overline{\text{RES}}$ pin	Yes	None

As the power-supply voltage rises of power-on reset circuit for H8/36109, the capacitor which is externally connected to the $\overline{\text{RES}}$ pin is gradually charged via the on-chip pull-up resistor. Since the level of the $\overline{\text{RES}}$ signal is transmitted within this LSI, prescaler S and the entire LSI are in their reset states. When the level of the $\overline{\text{RES}}$ signal reaches the threshold level, the prescaler S is released from its reset state and it starts counting. The OVF signal of the prescaler S is generated and the internal reset signal is released.

The power-on reset circuit of the RL78/G14 generates an internal reset signal at power-on. The reset signal is released when the supply voltage (V_{DD}) exceeds the detection voltage (V_{POR}). The reset state must be retained until the operating voltage becomes in the range defined. This is done by utilizing the voltage detection circuit or controlling the externally input reset signal.

With the RL78/G14, set the flash operation mode by using an option byte according to the main system clock frequency (f_{MAIN}) and the power supply voltage (V_{DD}) used.

Table 1.2 shows the RL78/G14 flash operation mode setting.

Table 1.2 RL78/G14 Setting of flash operation mode

Operation mode	Operating Frequency Range (f_{MAIN})	Operating Voltage Range (V_{DD})
LV (low voltage main) mode	1 MHz to 4 MHz	1.6 V to 5.5 V
LS (low speed main) mode	1 MHz to 8 MHz	1.8 V to 5.5 V
HS (high speed main) mode	1 MHz to 16 MHz	2.4 V to 5.5 V
	1 MHz to 32 MHz	2.7 V to 5.5 V

1.2 Differences between Low-Voltage Detection Circuits and Voltage Detector

Table 1.3 summarizes the differences between the functions of the Low-Voltage Detection Circuits in H8/36109 and the Voltage Detector in RL78/G14.

Table 1.3 Summary of differences between Function

Item	H8/36109 Low-Voltage Detection Circuits	RL78/G14 Voltage Detector
Detection target	Supply voltage (V_{CC})	Supply voltage (V_{DD})
Operation Functions	- Low-voltage-detection reset - Low-voltage-detection interrupt	- Reset mode - Interrupt mode - Interrupt & reset mode
Detection levels	2 levels	14 levels
Setting Method	By the SFR	By the option byte

The low-voltage detection reset circuit (LVDR) of the H8/36109 low-voltage detection circuit is enabled after a power-on reset is released. When the power-supply voltage falls below the Vreset voltage (typ. = 2.3 V or 3.6 V), a reset is generated. The low-voltage detection reset state remains in place until a power-on reset is generated. When the power-supply voltage rises above the Vreset voltage (typ. = 3.6 V) again, releases the internal reset signal.

The low-voltage detection interrupt circuit (LVDI) in H8/36109 generates an interrupt request when the power-supply voltage falls below the Vint (D) voltage (typ.= 3.7 V). In this case, the necessary data must be saved in the external EEPROM, etc, and a transition must be made to the standby or subsleep mode. Until this processing is completed, the power supply voltage must be higher than the lower limit of the guaranteed operating voltage. When the power-supply voltage does not fall below Vreset1 (typ. = 2.3 V) voltage but rises above Vint (U) (typ. = 4.0 V) voltage, an interrupt request is generated. If the power supply voltage (Vcc) falls below Vreset1 (typ. = 2.3 V) voltage, Low-voltage-detection reset (LVDR) is performed.

The operation mode and detection voltages (VLVDH, VLVDL, VLVD) for the voltage detector of RL78/G14 is set by using the option byte (000C1H).

Select an operating mode from reset mode, interrupt mode, or interrupt and reset mode. The LVD circuit compares the supply voltage (VDD) with the detection voltage (VLVDH, VLVDL, VLVD), and generates an internal reset or internal interrupt signal. The detection level for the power supply detection voltage (VLVDH, VLVDL) can be selected by using the option byte as one of 14 levels. Operable in STOP mode. After power is supplied, the reset state must be retained until the operating voltage becomes. This is done by utilizing the voltage detector or controlling the externally input reset signal. After the power supply is turned off, this LSI should be placed in the STOP mode, or placed in the reset state by utilizing the voltage detector or controlling the externally input reset signal before the voltage falls below the operating range.

2. Comparison between Registers

Table 2.1 shows registers for low-voltage detection circuits in H8/36109 and voltage detector in RL78/G14.

Table 2.1 Comparison between Registers for Low-Voltage Detection Circuits in H8/36109 and Voltage Detector in RL78/G14

Item	H8/36109 Low-Voltage Detection Circuits	RL78/G14 Voltage Detector
Low-Voltage-Detection Control Register	LVDCR register	None
LVDR Detection Level Select	LVDCR register LVDSEL bit	None
Voltage-Fall-Interrupt Enable	LVDCR register LVDDE bit	None
Voltage-Rise-Interrupt Enable	LVDCR register LVDUE bit	None
Low-Voltage-Detection Status Register	LVDSR register	None
LVD Power-Supply Voltage Fall Flag	LVDSR register LVDDF bit	None
LVD Power-Supply Voltage Rise Flag	LVDSR register LVDUF bit	None
Enables or disables operation	None	Address: 000C1H / 010C1H(Note1) (Note 2) VPOC2 bit, LVIMDS0 bit
Voltage detection selection	None	Address: 000C1H / 010C1H(Note1) (Note2) LVIMDS1 bit, LVIMDS0 bit
Voltage detection flag	None	LVIM register LVIF bit
Select voltage detection level	None	Address: 000C1H / 010C1H(Note1) (Note2) VPOC1 bit, VPOC0 bit, LVIS1 bit, LVIS0 bit
Enable or disable rewriting the voltage detection level register (LVIS)	None	LVIM register LVISEN bit
Mask status flag of LVD output	None	LVIM register LVIOMSK bit
Operation mode of voltage detection	None	LVIS register LVIMD bit(Note3)
LVD detection level	None	LVIS register LVILV bit

Note1. If the corresponding register is the option byte, the address of the option byte is shown.

Note2. Only when using the boot swap function.

Note3. Writing “0” can only be allowed in the interrupt & reset mode. Do not set in other cases.

3. Sample Code for Voltage Detector

The sample code for the Voltage Detector is explained in the following application notes.

- RL78/G13 Voltage Detector (Reset Mode) CC-RL (R01AN2834)

4. Documents for Reference

User's Manual:

- RL78/G14 User's Manual: Hardware (R01UH0186)
- H8/36109 Group User's Manual: Hardware (R01UH0294)

  The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News:

The latest information can be downloaded from the Renesas Electronics website.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Oct. 06, 2020	-	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

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1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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