RL78/G13

Low-power Consumption Operation (UART in SNOOZE Mode)

CC-RL

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Introduction

This application note explains how to make low power consumption settings for UART reception in SNOOZE mode. The sample application covered in this application note uses the SNOOZE mode to receive data through the UART communication without starting the CPU. The application judges the receive data and displays the result on an LED.

Target Device

RL78/G13

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specifications

This application note explains how to make low power consumption settings for UART reception operation in SNOOZE mode. The sample application covered in this application note sets up the serial array unit (SAU) for UART reception and enables the SNOOZE mode. Subsequently, it executes the STOP instruction. When an input is detected at the RxDq pin in STOP mode, the application starts data reception in SNOOZE mode. It compares the data received via UART with the predefined data and turns on an LED if a match is found and off the LED otherwise.

Note: The SNOOZE mode can be enabled only when the high-speed on-chip oscillator clock is selected as the source of the CPU/peripheral hardware clock (f_{CLK}).

Table 1.1 lists the peripheral functions to be used and their uses. Figure 1.1 shows the outline of the operation of the sample code.

Table 1.1 Peripheral Functions to be Used and their Uses

Peripheral Function	Use
Serial array unit	Used for UART reception via the P11/RxD0 pin.

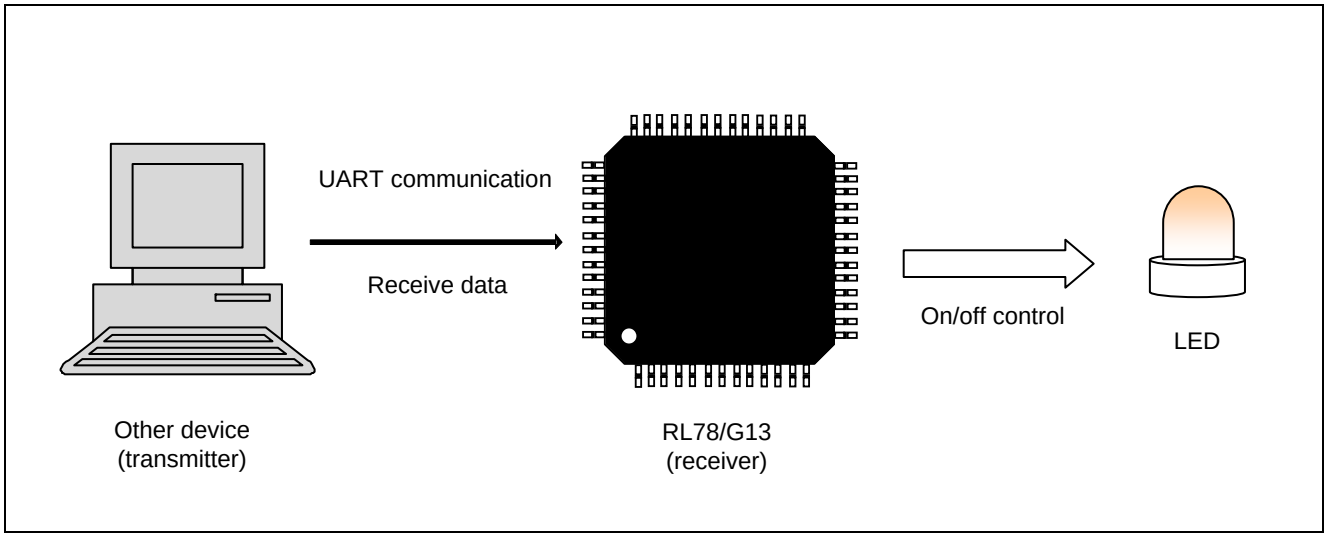


Figure 1.1 Outline of Operation

Figure 1.2 shows the outline of UART reception in SNOOZE mode. The HALT mode is generally used to receive data via a UART. When a device which supports the SNOOZE mode is to be used, the STOP mode which supports lower operating current than the HALT mode is available in addition to the HALT mode. In UART reception in SNOOZE mode, the application switches from STOP mode to SNOOZE mode upon detection of the falling edge of the RxD0 signal and performs data reception via a UART0 without starting the CPU. If an error occurs during reception, the application returns to the STOP mode and waits for the next data. If the data reception is successful without an error, the application exits the SNOOZE mode and starts the CPU.

The actions that the application are to take when a receive error occurs can be configured using the SSECm bits. The sample code covered in this application note make settings so that it returns to the STOP mode when a receive error occurs as shown in figure 1.2. The SNOOZE mode can be configured only when the high-speed on-chip oscillator clock is selected as the source of the CPU/peripheral hardware clock (f_{CLK}).

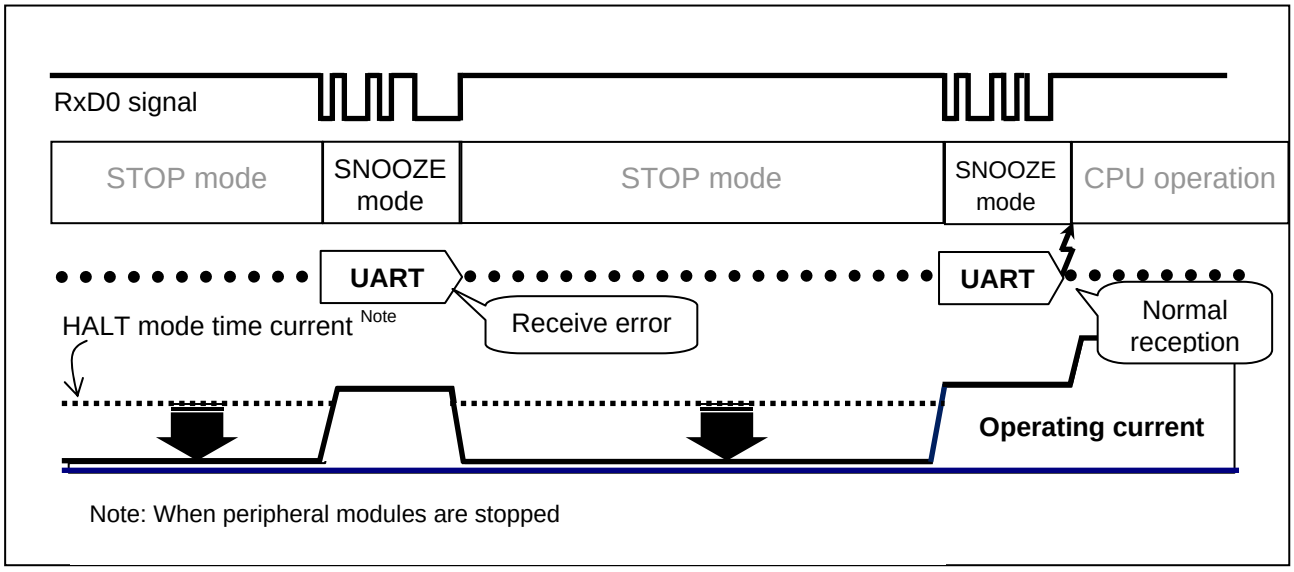
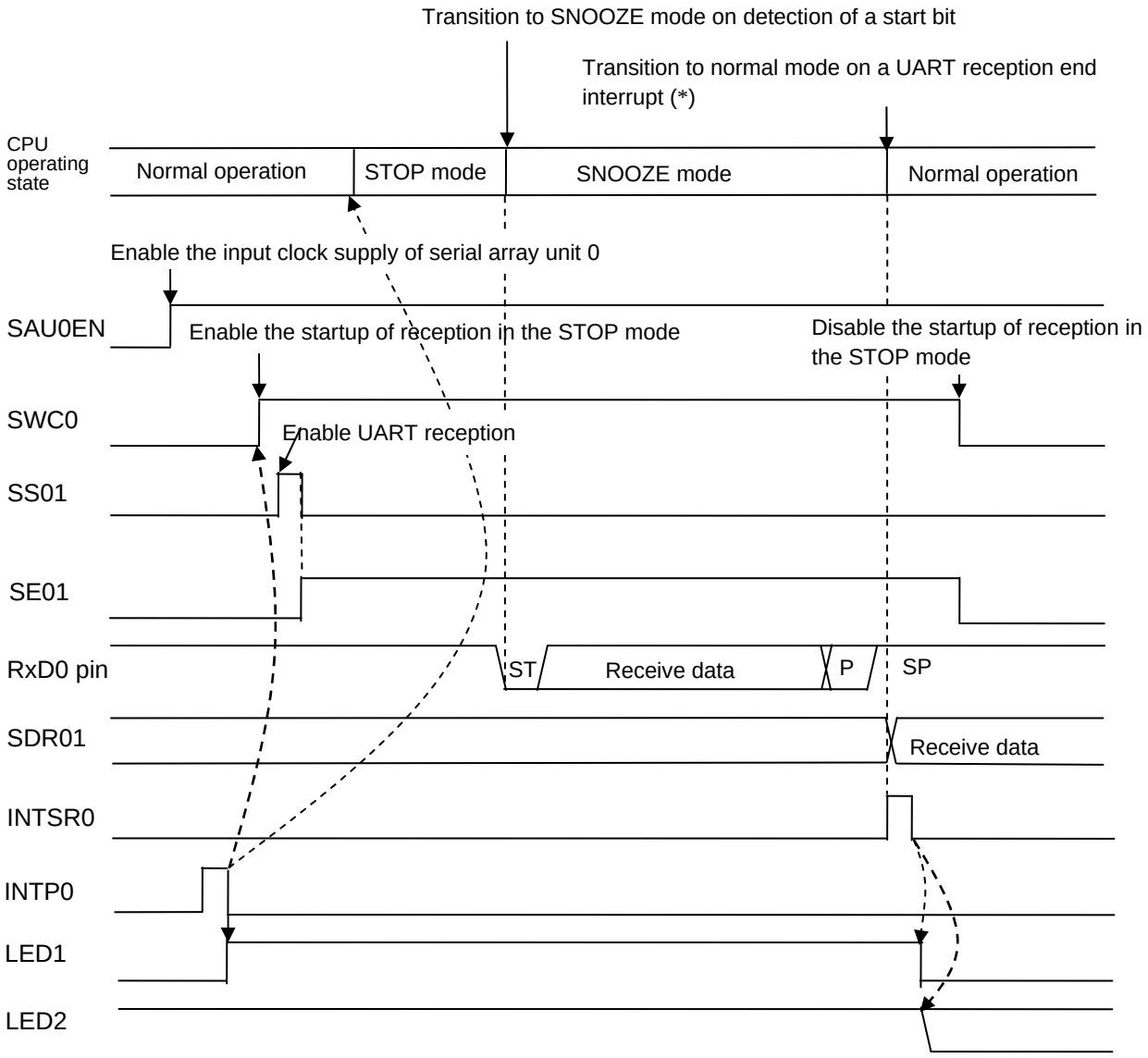


Figure 1.2 Outline of UART Receive Operation in SNOOZE Mode

Figure 1.3 shows the timing chart for the SNOOZE mode operation.



(*) Transition to the STOP mode again when a communication error occurs.

Note: Set the STm1 bit to 1 and clear the SEm1 bit (stop operation) when the reception in SNOOZE mode is completed. Also disable the startup of reception in SNOOZE mode by setting the SWCm bit to 0.

Figure 1.3 Timing Chart of SNOOZE Mode Operation

2. Operation Check Conditions

The sample code described in this application note has been checked under the conditions listed in the table below.

Table 2.1 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G13 (R5F100LEA)
Operating frequency	• High-speed on-chip oscillator (HOCO) clock: 32 MHz • CPU/peripheral hardware clock: 32 MHz
Operating voltage	5.0V (can run on a voltage range of 2.9 V to 5.5 V.) LVD operation (V_{LVD}): Reset mode 2.81 V (2.76 V to 2.87 V)
Integrated development environment (CS+)	CS+ V3.01.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.01.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V4.0.0.26 from Renesas Electronics Corp.
C compiler (e^2 studio)	CC-RL V1.01.00 from Renesas Electronics Corp.

3. Related Application Notes

The application notes that are related to this application note are listed below for reference.

RL78/G13 Initialization (R01AN2575E) Application Note
RL78/G13 Serial Array Unit (UART Communication) (R01AN2517E) Application Note

4. Description of the Hardware

4.1 Hardware Configuration Example

Figure 4.1 shows an example of the hardware configuration used for this application note.

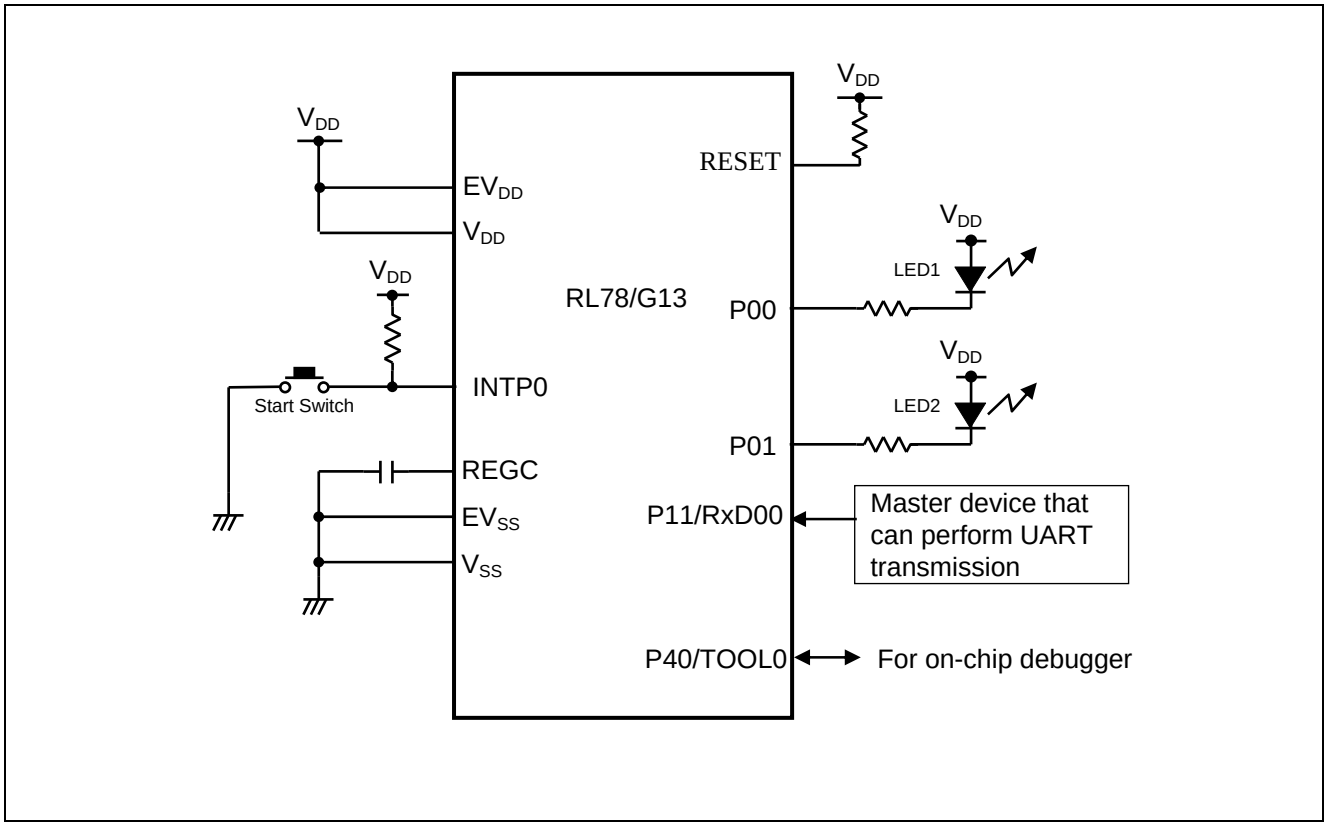


Figure 4.1 Hardware Configuration

Cautions: 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V_{DD} or V_{SS} via a resistor).

2. Connect any pins whose name begins with EV_{SS} to V_{SS} and any pins whose name begins with EV_{DD} to V_{DD}, respectively.
3. V_{DD} must be held at not lower than the reset release voltage (V_{LVD}) that is specified as LVD.

4.2 List of Pins to be Used

Table 4.1 lists the pins to be used and their functions.

Table 4.1 Pins to be Used and their Functions

Pin Name	I/O	Description
P11/RxD0	Input	UART0 receive input pin
P137/INTP0	Input	UART0 reception start trigger input
P00	Output	LED1 lighting control port
P01	Output	LED2 lighting control port

5. Software Description

5.1 Operation Outline

The sample application covered in this application note receives data via UART in SNOOZE mode, compares the receive data with the predefined data value, and turns on an LED when these data are matched.

The application turns on LED1 and waits for a switch input. If a switch input is present, the application turns off LED1 and LED2 , sets UART reception and the SNOOZE mode, and then transitions to the STOP mode. When an input is detected at the RxD0 pin after switching to the STOP mode, the application starts UART reception in SNOOZE mode. The CPU returns to the normal operation mode if the reception is successful and returns to the STOP mode if a UART receive error is detected. After returning to the normal operation mode, the application turns on LED2 if the receive data is 0.

(1) Initialize the SAU0.
<Conditions for setting>

- Use the SAU0 in UART mode, receive only.
- Use even parity as the parity setting.
- Set the data transfer order to LSB first.
- Set the transfer data size to 8 bits.
- Use one stop bit.
- Set the receive data level to standard.
- Set the transfer rate to 9600 bps.
- Set P11 to the RxD0 pin.
- Set the priority level of the INTSR0 and INTSRE0 interrupts to the lowest level.
- Use the UART reception transfer end interrupt (INTSR0) as the interrupt source.

(2) Set up I/O ports
<Conditions for setting>

- LED lighting control ports (LED1 and LED2): Set ports P00 and P01 to output ports.
- UART0 reception start switch: Set the P137/INTP0 pin for INTP0 interrupts in falling edge detection mode (using an external pull-up resistor).

(3) Turn on LED1, transition to HALT mode, and wait for a switch input.
(4) In the presence of a switch input, exit the HALT mode, turn off LED1 and LED2, and set up the UART and SNOOZE mode.

- Disable error interrupts and enable the startup of reception in STOP mode.
- Enable INTSR0 interrupts and transition to the communication wait status.

(5) Transition to STOP mode and wait for the completion of the UART reception.
The UART reception is carried out by hardware in STOP mode. When a start bit (RxD0 pin input) is detected, a UART reception is started in SNOOZE mode. When the reception ends successfully, the application transitions to the normal operation mode and performs the step (6). If a receive error occurs, the application transitions to STOP mode and waits for a start bit again.
(6) Read the receive data after switching into normal operation mode.
(7) Stop the UART operation and disable the transition to SNOOZE mode.

- Disable INTSR0 interrupts and stop communication operation.
- Enable error interrupts and disable the startup of reception in STOP mode.

(8) Confirm the receive data and turn on LED2 if a 0 is received. Subsequently, repeats steps (3) through (8).

Caution: For information about the precautions in using the device, refer to RL78/G13 User's Manual: Hardware.

5.2 List of Option Byte Settings

Table 5.1 summarizes the settings of the option bytes.

Table 5.1 Option Byte Settings

Address	Value	Description
000C0H/010C0H	11101111B	Disables the watchdog timer. (Stops counting after the release from the reset status.)
000C1H/010C1H	01111111B	LVD reset mode, 2.81 V (2.76 V to 2.87 V)
000C2H/010C2H	11101000B	HS mode HOCO: 32 MHz
000C3H/010C3H	10000100B	Enables the on-chip debugger.

5.3 List of Constants

Table 5.2 list the constants that are used in this sample program.

Table 5.2 Constants for the Sample Program

Constant	Setting	Description
_0002_SAU_CH1_START_TRG_ON	0x0002	Serial channel enable status register 0 (SE0) value for enabling communication operation
_0002_SAU_CH1_STOP_TRG_ON	0x0002	Serial channel stop register 0 (ST0) value for stopping communication operation
MD_OK	0x00	Successful reception state
MD_ARGERROR	0x81	Error state
LED1_NOMAL	P0_bit.no0	LED1 lighting control port
LED2_RCV_0	P0_bit.no1	LED2 lighting control port

5.4 List of Variables

Table 5.3 lists the global variable that is used by this sample program.

Table 5.3 Global Variable

Type	Variable Name	Contents	Function Used
volatile uint16_t	g_uart0_rx_count	Number of UART data bytes received	R_UART0_Receive r_uart0_interrupt_receive
volatile uint16_t	g_uart0_rx_length	Number of UART data bytes to be received	R_UART0_Receive r_uart0_interrupt_receive
volatile uint8_t	*gp_uart0_rx_address	Address of location for storing the UART data to be received next	R_UART0_Receive r_uart0_interrupt_receive R_UART0_GetRxData

5.5 List of Functions

Table 5.4 lists the functions that are used in this sample program.

Table 5.4 Functions

Function Name	Outline
R_SAU0_SnoozeOn	Enabling UART0 for SNOOZE mode
R_SAU0_SnoozeOff	Disabling UART0 for SNOOZE mode
R_UART0_Start	Starting UART0 reception
R_UART0_Stop	Stopping UART0 reception
R_UART0_Receive	Setting UART0 receive buffer
R_INTC0_Start	Starting INTP0 operation
R_INTC0_Stop	Stopping INTP0 operation
R_UART0_GetRxData	Getting UART0 receive data

5.6 Function Specifications

This section describes the specifications for the functions that are used in this sample program.

[Function Name] R_SAU0_SnoozeOn

Synopsis	Enabling UART0 for SNOOZE mode
Header	r_cg_serial.h
Declaration	void R_SAU0_SnoozeOn(void)
Explanation	This function enables SNOOZE mode (SWC0 = 1).
Arguments	None
Return value	None
Remarks	None

[Function Name] R_SAU0_SnoozeOff

Synopsis	Disabling UART0 for SNOOZE mode
Header	r_cg_serial.h
Declaration	void R_SAU0_SnoozeOff(void)
Explanation	This function disables SNOOZE mode (SWC0 = 0).
Arguments	None
Return value	None
Remarks	None

[Function Name] R_UART0_Start

Synopsis	Starting UART0 reception
Header	r_cg_serial.h
Declaration	void R_UART0_Start(void)
Explanation	This function resets UART0 reception interrupt mask to enable UART0 reception.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_UART0_Stop

Synopsis	Stopping UART0 reception
Header	r_cg_serial.h
Declaration	void R_UART0_Stop(void)
Explanation	This function sets UART0 reception interrupt mask to disable UART0 reception.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_UART0_Receive

Synopsis	Setting UART0 receive buffer	
Header	r_cg_macrodriver.h	
Declaration	MD_STATUS R_UART0_Receive(uint8_t * const rx_buf, uint16_t rx_num)	
Explanation	This function sets the UART receive buffer address and the number of data bytes to receive.	
	An argument error is returned if the receive data count is set to not more than 1.	
Arguments	rx_buf	Address of receive data buffer
Return value	rx_num	Number of data bytes to receive
Remarks	[MD_OK]: Setup completed	
	[MD_ARGERROR]: Argument error	
Synopsis	None	

[Function Name] R_INTC0_Start

Synopsis	Starting INTP0 operation
Header	None
Declaration	void R_INTC0_Start(void)
Explanation	This function resets INTP0 interrupt mask.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_INTC0_Stop

Synopsis	Stopping INTP0 operation
Header	None
Declaration	void R_INTC0_Stop(void)
Explanation	This function sets INTP0 interrupt mask.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_UART0_GetRxData

Synopsis	Getting UART0 receive data
Header	None
Declaration	void R_UART0_GetRxData(void)
Explanation	This function stores the UART receive data in the buffer set by R_UART0_Receive.
Arguments	None
Return value	None
Remarks	None

5.7 Flowcharts

Figure 5.1 shows the overall flow of the sample program described in this application note.

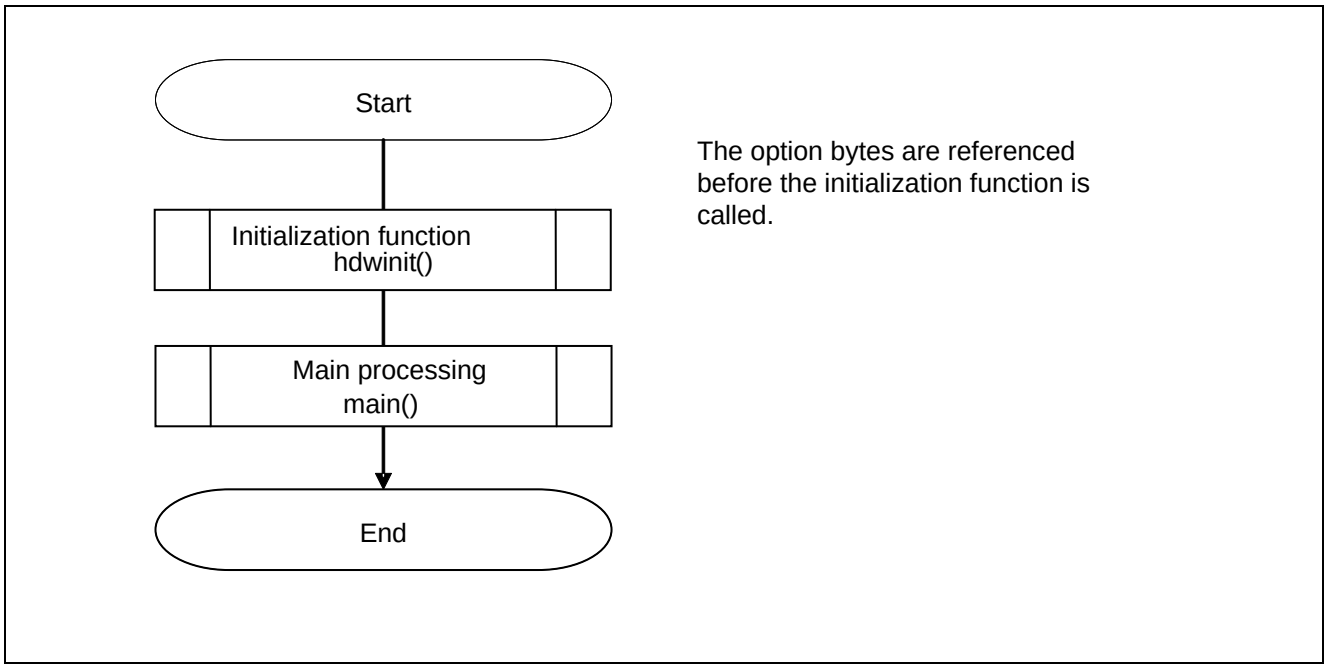


Figure 5.1 Overall Flow

5.7.1 Initialization Function

Figure 5.2 shows the flowchart for the initialization function.

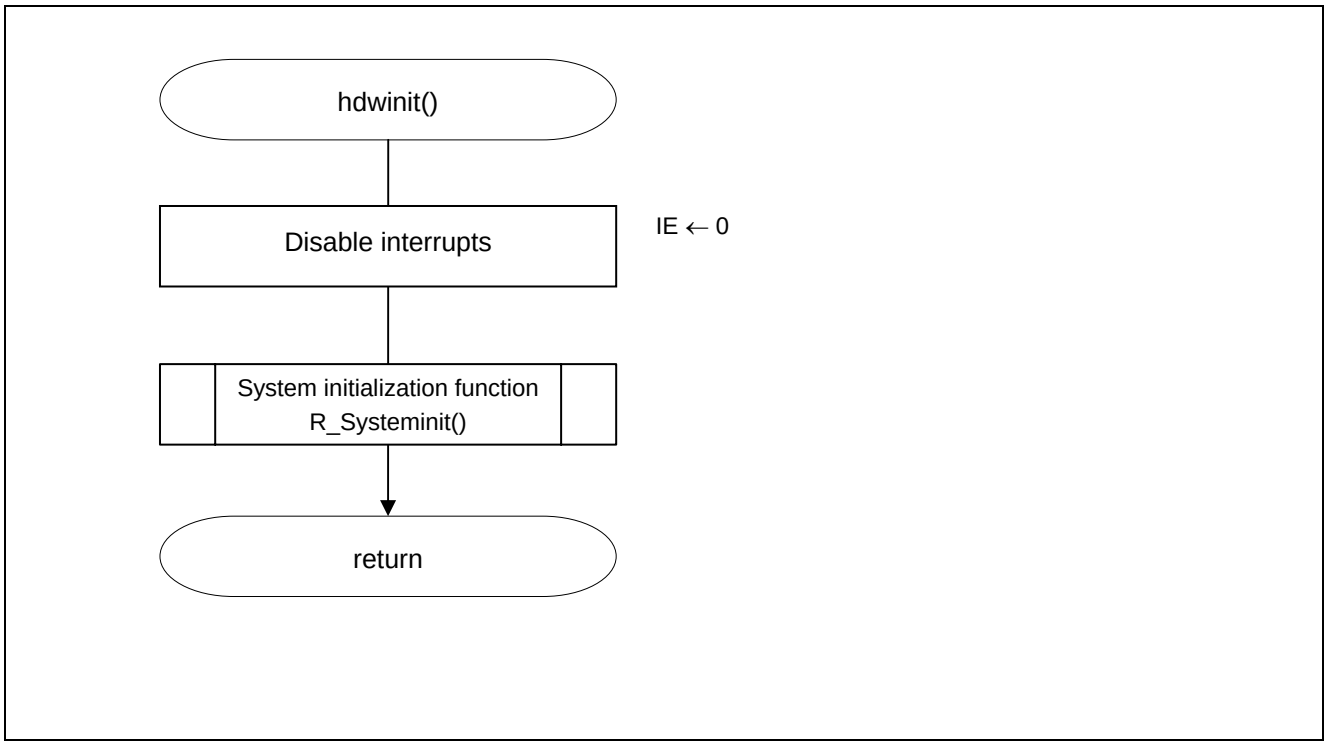


Figure 5.2 Initialization Function

5.7.2 System Initialization function

Figure 5.3 shows the flowchart for the system initialization function.

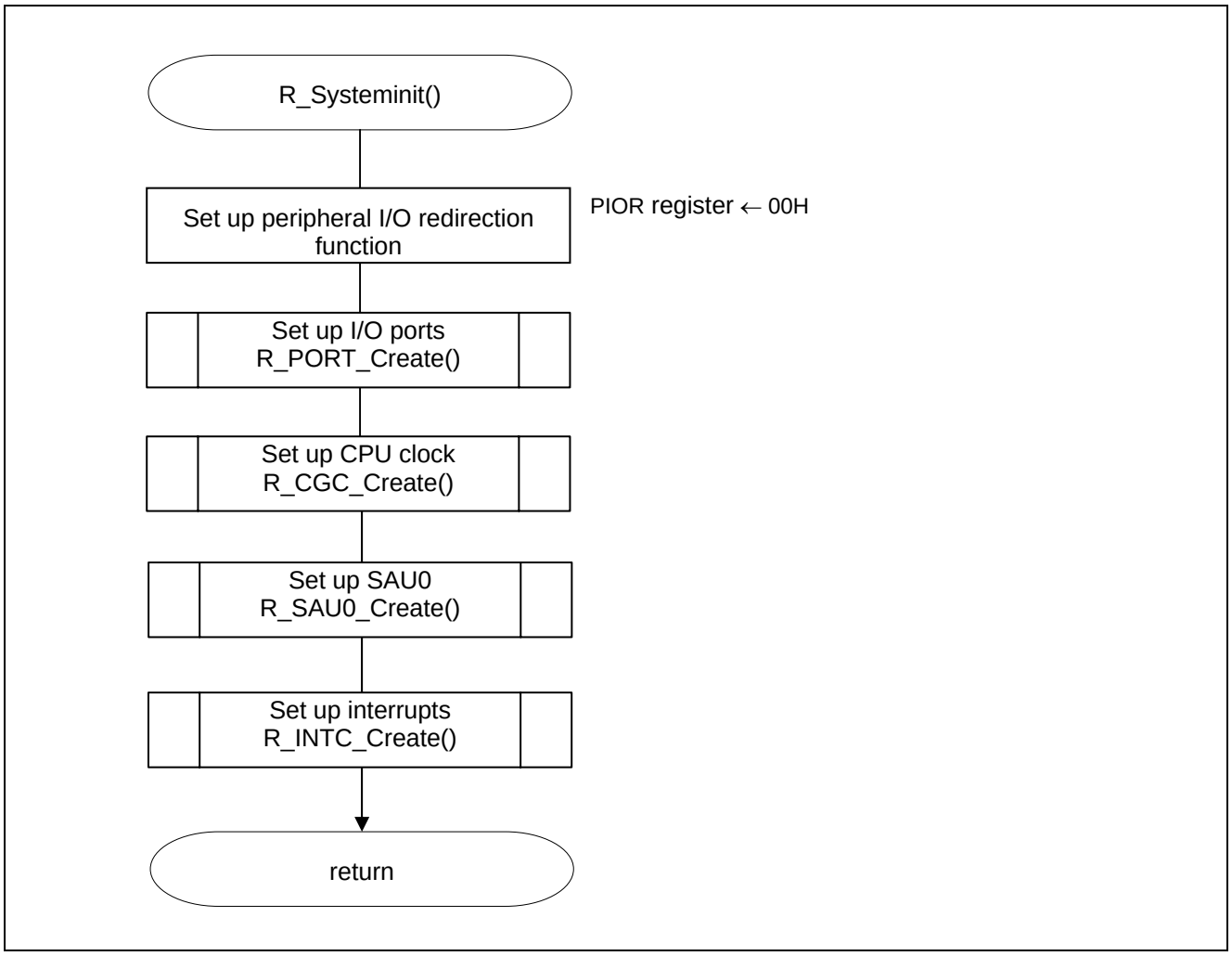


Figure 5.3 System Initialization Function

5.7.3 I/O Port Setup

Figure 5.4 shows the flowchart for setting up the I/O ports.

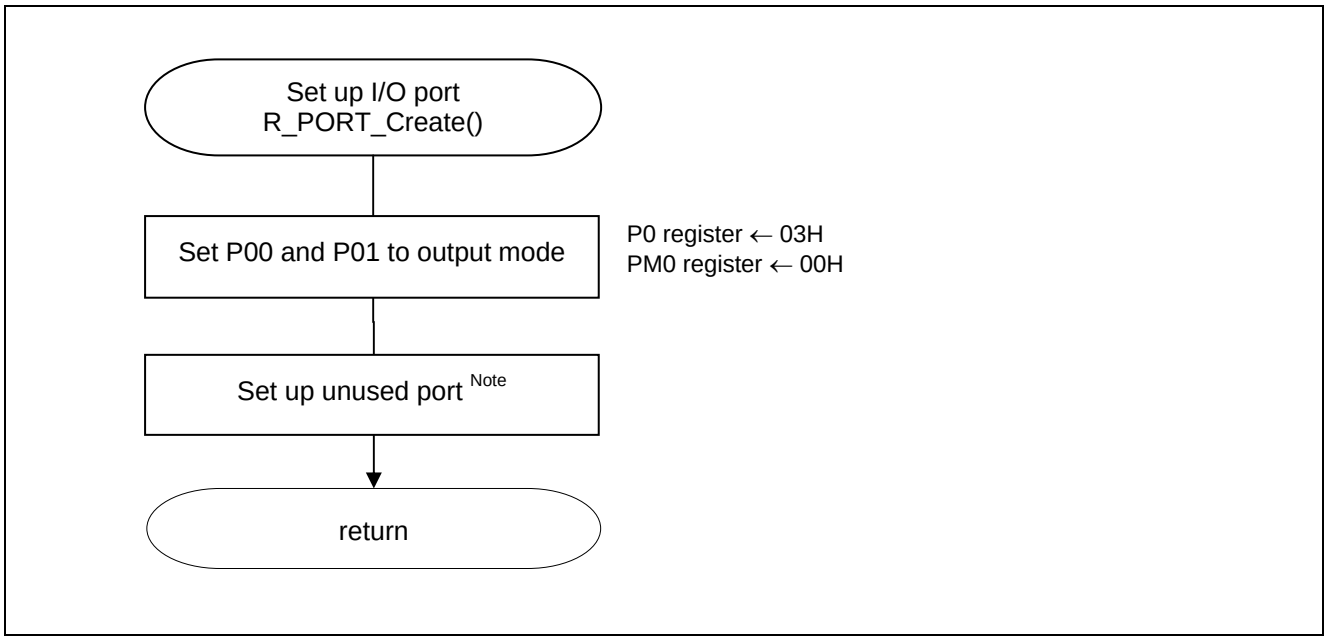


Figure 5.4 I/O Port Setup

Note: Refer to the section entitled "Flowcharts" in RL78/G13 Initialization Application Note (R01AN2575E) for the configuration of the unused ports.

Caution: Provide proper treatment for unused pins so that their electrical specifications are met. Connect each of any unused input-only ports to V_{DD} or V_{SS} via a separate resistor.

Setting to turn off LEDs

- Port register 0 (P0)
  Set up LED lighting control port for inactive output.
- Port mode register 1 (PM0)
  Select LED output mode of lighting control port

Symbol: P0

7	6	5	4	3	2	1	0
P07	P06	P05	P04	P03	P02	P01	P00
x	x	x	x	x	x	**1**	**1**

Bits 1 and 0

P00, P01	P00 and P01 output selection
0	Output low level (LED on)
1	**Output high level (LED off)**

Symbol: PM0

7	6	5	4	3	2	1	0
PM07	PM06	PM05	PM04	PM03	PM02	PM01	PM00
x	x	x	x	x	x	**0**	**0**

Bits 1 and 0

PM00, PM01	PM00 and PM01 I/O mode selection
0	**Output mode (output buffer on)**
1	Input mode (output buffer off)

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.4 CPU Clock Setup

Figure 5.5 shows the flowchart for setting up the CPU clock

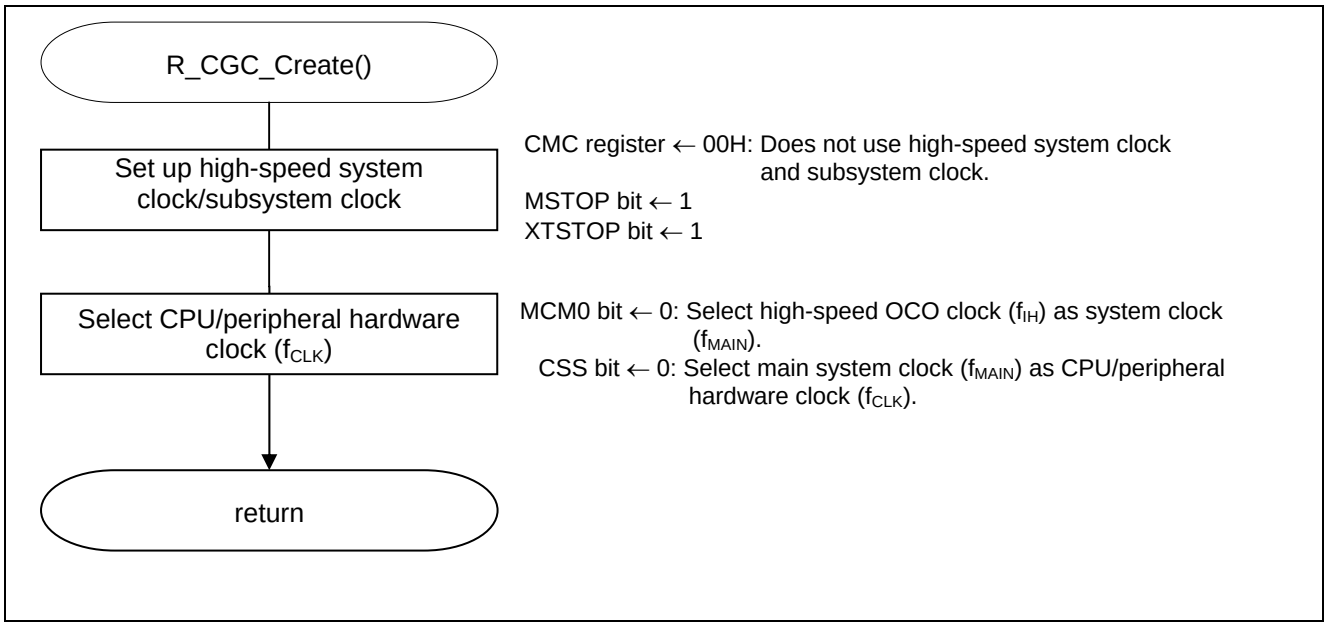


Figure 5.5 CPU Clock Setup

Caution: For details on the procedure for setting up the CPU clock (R_CGC_Create ()), refer to the section entitled "Flowcharts" in RL78/G13 Initialization Application Note (R01AN2575E).

5.7.5 SAU0 Setup

Figure 5.6 shows the flowchart for setting up the SAU0.

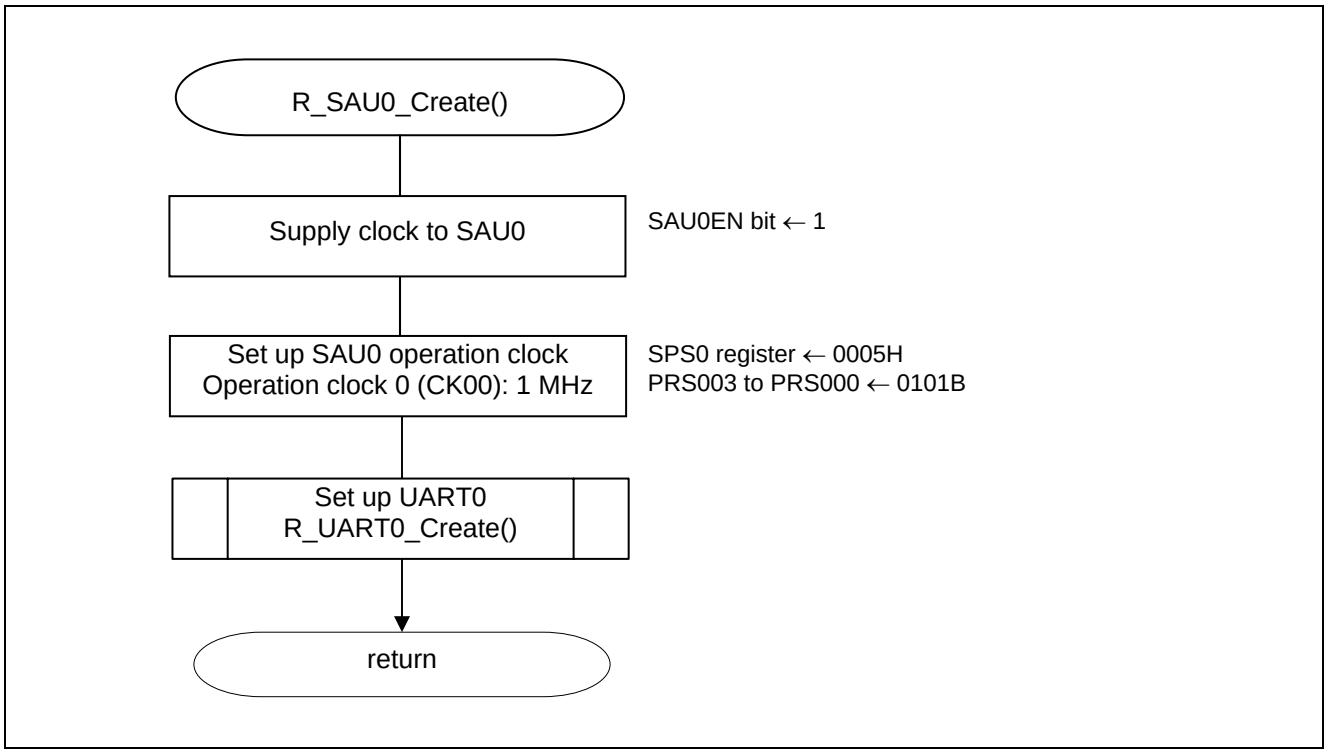


Figure 5.6 SAU0 Setup

Caution: For details on the procedure for setting up the SAU0 (R_SAU0_Create ()), refer to the section entitled "Flowcharts" in RL78/G13 Serial Array Unit (UART Communication) Application Note (R01AN2517E).

Starting supplying clock to the SAU0

- Peripheral enable register 0 (PER0)
  Start supplying clock to SAU0.

Symbol: PER0

7	6	5	4	3	2	1	0
RTCEN	IICA1EN	ADCEN	IICA0EN	SAU1EN	SAU0EN	TAU1EN	TAU0EN
x	x	x	x	x	**1**	x	x

Bit 2

SAU0EN	Control of serial array unit 0 input clock supply
0	Stops supply of input clock.
1	**Enables input clock supply.**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting serial clock

- Serial clock select register (SPS0)
  Operation clock (CK00 = 1 MHz).

Symbol: SPS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	PRS 013	PRS 012	PRS 011	PRS 010	PRS 003	PRS 002	PRS 001	PRS 000
0	0	0	0	0	0	0	0	0	0	0	0	**0**	**1**	**0**	**1**

Bits 3 to 0

PRS003	PRS002	PRS001	PRS000		Selection of operation clock (CK00)				
					f_{CLK} = 2 MHz	f_{CLK} = 5 MHz	f_{CLK} = 10 MHz	f_{CLK} = 2 MHz	**f_{CLK} = 32 MHz**
0	0	0	0	f_{CLK}	2 MHz	5 MHz	10 MHz	20 MHz	32 MHz
0	0	0	1	$f_{CLK}/2$	1 MHz	2.5 MHz	5 MHz	10 MHz	16 MHz
0	0	1	0	$f_{CLK}/2^2$	500 kHz	1.25 MHz	2.5 MHz	5 MHz	8 MHz
0	0	1	1	$f_{CLK}/2^3$	250 kHz	625 kHz	1.25 MHz	2.5 MHz	4 MHz
0	1	0	0	$f_{CLK}/2^4$	125 kHz	313 kHz	625 kHz	1.25 MHz	2 MHz
0	**1**	**0**	**1**	**$f_{CLK}/2^5$**	62.5 kHz	156 kHz	313 kHz	625 kHz	**1 MHz**
0	1	1	0	$f_{CLK}/2^6$	31.3 kHz	78.1 kHz	156 kHz	313 kHz	500 kHz
0	1	1	1	$f_{CLK}/2^7$	15.6 kHz	39.1 kHz	78.1 kHz	156 kHz	250 kHz
1	0	0	0	$f_{CLK}/2^8$	7.81 kHz	19.5 kHz	39.1 kHz	78.1 kHz	125 kHz
1	0	0	1	$f_{CLK}/2^9$	3.91 kHz	9.77 kHz	19.5 kHz	39.1 kHz	62.5 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.95 kHz	4.88 kHz	9.77 kHz	19.5 kHz	31.3 kHz
1	0	1	1	$f_{CLK}/2^{11}$	977 Hz	2.44 kHz	4.88 kHz	9.77 kHz	15.6 kHz
1	1	0	0	$f_{CLK}/2^{12}$	488 Hz	1.22 kHz	2.44 kHz	4.88 kHz	7.81 kHz
1	1	0	1	$f_{CLK}/2^{13}$	244 Hz	610 Hz	1.22 kHz	2.44 kHz	3.91 kHz
1	1	1	0	$f_{CLK}/2^{14}$	122 Hz	305 Hz	610 Hz	1.22 kHz	1.95 kHz
1	1	1	1	$f_{CLK}/2^{15}$	61 Hz	153 Hz	305 Hz	610 Hz	977 Hz

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.6 UART0 Setup

Figure 5.7 shows the flowcharts for setting up the UART0.

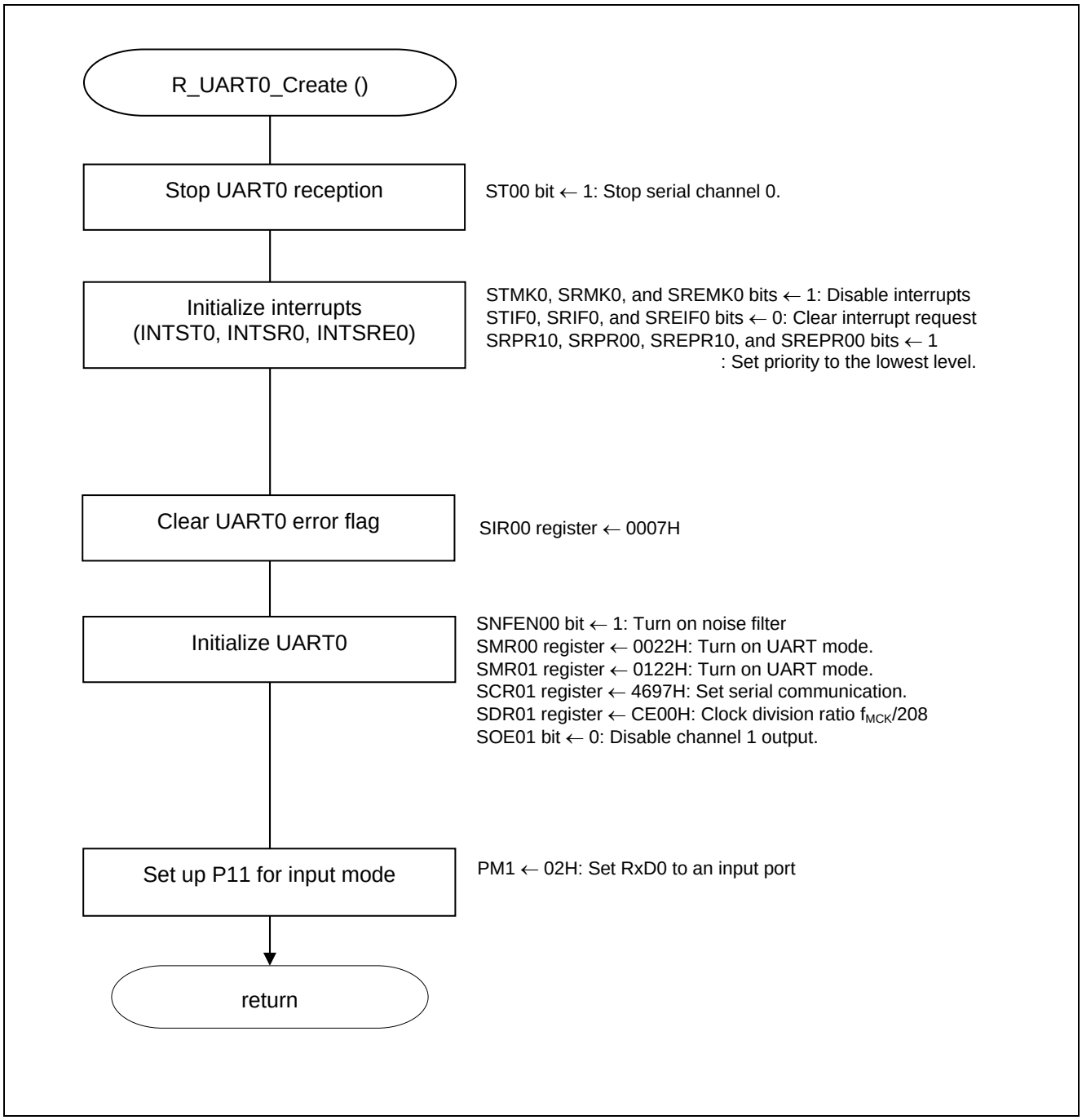


Figure 5.7 UART0 Setup

Caution: For details on the procedure for setting up the UART0 (R_UART0_Create ()), refer to the section entitled "Flowcharts" in RL78/G13 Serial Array Unit (UART Communication) Application Note (R01AN2517E).

Stopping serial channel 0

- Serial channel stop register 0 (ST0)
  Stop serial channel 1 communication.

Symbol: ST0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	ST03	ST02	ST01	ST00
0	0	0	0	0	0	0	0	0	0	0	0	**0**	**0**	**1**	**0**

Bits 3 to 0

ST01	Operation stop trigger of channel
0	No trigger operation
1	**Clears the SE01 bit to 0 and stops the communication.**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Initializing UART interrupt control

- Interrupt request flag register (IF0H)
  Clear interrupt request flag.
- Interrupt mask flag register (MK0H)
  Clear interrupt mask.

Symbol: IF0H

7	6	5	4	3	2	1	0
SREIF0 TMIF01H	SRIF0 CSIIF01 IICIF01	STIF0 CSIIF00 IICIF00	DMAIF1	DMAIF0	SREIF2 TMIF11H	SRIF2 CSIIF21 IICIF21	STIF2 CSIIF20 IICIF20
0	**0**	**0**	x	x	x	x	x

Bit 5

STIF0	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Bit 6

SRIF0	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Bit 7

SREIF0	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Symbol: MKH

7	6	5	4	3	2	1	0
SREMK0 TMMK01H	SRMK0 CSIMK01 IICMK01	STMK0 CSIMK00 IICMK00	DMAMK1	DMAMK0	SREMK2 TMMK11H	SRMK2 CSIMK21 IICMK21	STMK2 CSIMK20 IICMK20
1	**1**	**1**	x	x	x	x	x

Bit 5

STMK0	Interrupt processing control
0	Interrupt processing enabled
1	**Interrupt processing disabled**

Bit 6

SRMK0	Interrupt processing control
0	Interrupt processing enabled
1	**Interrupt processing disabled**

Bit 7

SREMK0	Interrupt processing control
0	Interrupt processing enabled
1	**Interrupt processing disabled**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting interrupt priorities

- Priority specification flag registers (PR00H, PR10H)
  Clear interrupt request flags.

Symbol: PR00H

7	6	5	4	3	2	1	0
SREPR00 TMPR001H	SRPR00 CSIPR001 IICPR001	STPR00 CSIPR000 IICPR000	DMAPR01	DMAPR00	SREPR02 TMPR011H	SRPR02 CSIPR021 IICPR021	STPR02 CSIPR020 IICPR020
1	**1**	x	x	x	x	x	x

Symbol: PR10H

7	6	5	4	3	2	1	0
SREPR10 TMPR101H	SRPR10 CSIPR101 IICPR101	STPR10 CSIPR100 IICPR100	DMAPR11	DMAPR10	SREPR12 TMPR111H	SRPR12 CSIPR121 IICPR121	STPR12 CSIPR120 IICPR120
1	**1**	x	x	x	x	x	x

Bit 6

SRPR10	SRPR00	Priority level selection
0	0	Specify level 0 (highest level)
0	1	Specify level 1
1	0	Specify level 2
1	**1**	**Specify level 3 (lowest level)**

Bit 7

SREPR10	SREPR00	Priority level selection
0	0	Specify level 0 (highest level)
0	1	Specify level 1
1	0	Specify level 2
1	**1**	**Specify level 3 (lowest level)**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Clearing error flags

- Serial flag clear trigger register 01 (SIR01)
  Clear error information of channel 1.

Symbol: SIR01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	FECT01	PECT01	OVCT01
0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	**1**	**1**

Bit 0

FECT01	Clear trigger of framing error of channel 1
0	Not cleared
1	**Clears the FEF01 bit of the SSR01 register to 0.**

Bit 1

PECT01	Clear trigger of parity error of channel 1
0	Not cleared
1	**Clears the PEF01 bit of the SSR01 register to 0.**

Bit 2

OVCT01	Clear trigger of overrun error of channel 1
0	Not cleared
1	**Clears the OVF01 bit of the SSR01 register to 0.**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up noise filter for RxD0 pin

- Noise filter enable register 0 (NFEN0)
  Turn on channel 0 noise filter.

Symbol: NFEN0

7	6	5	4	3	2	1	0
0	SNFEN30	0	SNFEN20	0	SNFEN10	0	SNFEN00
0	x	0	x	0	x	0	**1**

Bit 0

SNFEN00	Use of noise filter of RxD0 pin
0	Noise filter OFF
1	**Noise filter ON**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up operation mode

- Serial mode register 00 (SMR00)
  Operation clock (f_{MCK}): Operation clock CK00 set by SPS0 register
  Transfer clock (f_{TCLK}): Divided operation clock f_{MCK} specified by CKS00 bit
  Operation mode: Select UART.
  Interrupt source: Select transfer end interrupt.

Symbol: SMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS00	CCS00	0	0	0	0	0	0	0	0	1	0	0	MD002	MD001	MD000
0	**0**	0	0	0	0	0	0	0	0	1	0	0	**0**	**1**	**0**

Bit 15

CKS00	Selection of operation clock (f_{MCK}) of channel 0
0	**Operation clock CK00 set by the SPS0 register**
1	Operation clock CK01 set by the SPS0 register

Bit 14

CCS00	Selection of transfer clock (f_{TCLK}) of channel 0
0	**Divided operation clock f_{MCK} specified by the CKS00 bit**
1	Clock input f_{SCK} from the SCK00 pin (slave transfer in CSI mode)

Bits 2 and 1

MD002	MD001	Setting of operation mode of channel 0
0	0	CSI mode
0	**1**	**UART mode**
1	0	Simplified I^2C mode
1	1	Setting prohibited

Bit 0

MD000	Selection of interrupt source of channel 0
0	**Transfer end interrupt**
1	Buffer empty interrupt (Occurs when data is transferred from the SDR00 register to the shift register.)

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up operation mode

- Serial mode register 01 (SMR01)
  Operation clock (f_{MCK}): Operation clock CK00 set by SPS0 register
  Transfer clock (f_{TCLK}): Divided operation clock f_{MCK} specified by CKS00 bit
  Start trigger source: Select valid edge of the RxD0 pin.
  Start bit detection and data inversion: Select start bit on detection of a falling edge
  Capture the input communication data as is.
  Operation mode: Select UART.
  Interrupt source: Select transfer end interrupt.

Symbol: SMR01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS01	CCS01	0	0	0	0	0	STS01	0	SIS010	1	0	0	MD012	MD011	MD010
0	**0**	0	0	0	0	0	**1**	0	**0**	1	0	0	**0**	**1**	**0**

Bit 15

CKS01	Selection of operation clock (f_{MCK}) of channel 1
0	**Operation clock CK00 set by the SPS0 register**
1	Operation clock CK01 set by the SPS0 register

Bit 14

CCS01	Selection of transfer clock (f_{TCLK}) of channel 1
0	**Divided operation clock f_{MCK} specified by the CKS01 bit**
1	Clock input f_{SCK} from the SCK00 pin (slave transfer in CSI mode)

Bit 8

STS01	Selection of start trigger source
0	Only software trigger is valid (selected for CSI, UART transmission, and simplified I^2C mode)
1	**Valid edge of the RxD0 pin (selected for UART reception)**

Bit 6

SIS00	Controls inversion of level of receive data of channel 0 in UART mode
0	**Falling edge is detected as the start bit.** **The input communication data is captured as is.**
1	Rising edge is detected as the start bit. The Input communication data is inverted and captured.

Bits 2 and 1

MD002	MD001	Setting of operation mode of channel 0
0	0	CSI mode
0	**1**	**UART mode**
1	0	Simplified I^2C mode
1	1	Setting prohibited

Bit 0

MD000	Channel 0 interrupt source select
0	**Transfer end interrupt**
1	Buffer empty interrupt (Occurs when data is transferred from the SDR00 register to the shift register.)

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up communication format

- Serial communication operation setting register 01 (SCR01)
  Operation mode: Reception only
  Parity bit setting: Even parity
  Data transfer sequence: LSB first
  Stop bit length: 1 bit
  Data length: 8 bits

Symbol: SCR01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXE01	RXE01	DAP01	CKP01	0	EOC01	PTC011	PTC010	DIR01	0	SLC011	SLC010	0	1	DLS011	DLS010
0	**1**	**0**	**0**	0	**1**	**1**	**0**	**1**	0	**0**	**1**	0	1	**1**	**1**

Bits 15 and 14

TXE01	RXE01	Setting of operation mode of channel 1
0	0	Disable communication.
0	**1**	**Reception only**
1	0	Transmission only
1	1	Transmission/reception

Bits 13 and 12

DAP01	CKP01	Selection of data and clock in CSI mode
0	**0**	**Type 1**
0	1	Type 2
1	0	Type 3
1	1	Type 4

Set DAP01, CKP01 = 0, 0 in the UART mode and simplified I^2C mode.

Bit 10

EOC01	Selection of masking of error interrupt signal (INTSREx (x = 0 to 3))
0	Masks error interrupts INTSREx (INTSRx is not masked).
1	**Enables generation of error interrupts INTSREx (INTSRx is masked if an error occurs).**

Set EOC01 = 1 during UART reception.

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Bits 9 and 8

PTC011	PTC010	Setting of parity bit in UART mode	
		Transmission	Reception
0	0	Does not output the parity bit.	Receives without parity
0	1	Outputs 0 parity Note 3	No parity judgment
1	**0**	Outputs even parity.	**Judges as even parity.**
1	1	Outputs odd parity.	Judges as odd parity.

Bit 7

DIR01	Selection of data transfer sequence in CSI and UART modes
0	Inputs/outputs data with MSB first.
1	**Inputs/outputs data with LSB first.**

Bits 5 and 4

SLC011	SLC010	Setting of stop bit in UART mode
0	0	No stop bit
0	**1**	**Stop bit length = 1 bit**
1	0	Setting prohibited
1	1	Setting prohibited

Set 1 bit (SLCmn1, SLCmn0 = 0, 1) during UART reception and in the simplified I^2C mode.

Bits 1 and 0

DLS011	DLS010	CSI/UART mode data length setting
0	1	9-bit data length (stored in bits 0 to 8 of the SDR01 register) (settable in UART mode only)
1	0	8-bit data length (stored in bits 0 to 6 of the SDR01 register)
1	**1**	**8-bit data length (stored in bits 0 to 7 of the SDR01 register)**
Other than above		Setting prohibited

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up frequency division ratio of operation clock (f_{MCK})

- Serial data register 01 (SDR01)
  Transfer clock: f_{MCK}/208

Symbol: SDR01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Frequency division ratio of operation clock (f_{MCK})							Transmit/receive buffer								
1	**1**	**0**	**0**	**1**	**1**	**1**	x	x	x	x	x	x	x	x	x

Bits 15 to 9

b15	b14	b13	b12	b11	b10	b9	Transfer clock setting by dividing the operating clock (f_{MCK})
0	0	0	0	0	0	0	f_{MCK}/2
0	0	0	0	0	0	1	f_{MCK}/4
0	0	0	0	0	1	0	f_{MCK}/6
0	0	0	0	0	1	1	f_{MCK}/8
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
1	**1**	**0**	**0**	**1**	**1**	**1**	**f_{MCK}/208**
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
1	1	1	1	1	1	0	f_{MCK}/254
1	1	1	1	1	1	1	f_{MCK}/256

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Enabling/disabling data output through target channel

- Serial output enable register 0 (SOE0)
  Disable output.

Symbol: SOE0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	SOE 03	SOE 02	SOE 01	SOE 00
0	0	0	0	0	0	0	0	0	0	0	0	x	x	**0**	x

SOE01	Serial output enable/stop of channel 1
0	**Stops output by serial communication operation.**
1	Enables output by serial communication operation.

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up UART RxD0 pin

- Port mode register 1 (PM1)
  Select I/O mode of serial input port.

Symbol: PM1

7	6	5	4	3	2	1	0
PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10
x	x	x	x	x	x	**1**	x

Bit 1

PM11	PM11 pin I/O mode selection
0	Output mode (output buffer on)
1	**Input mode (output buffer off)**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.7 Setting up Interrupts

The sample code covered in this application note uses the external interrupt INTP0.

Figure 5.8 shows the flowchart for setting this type of interrupts.

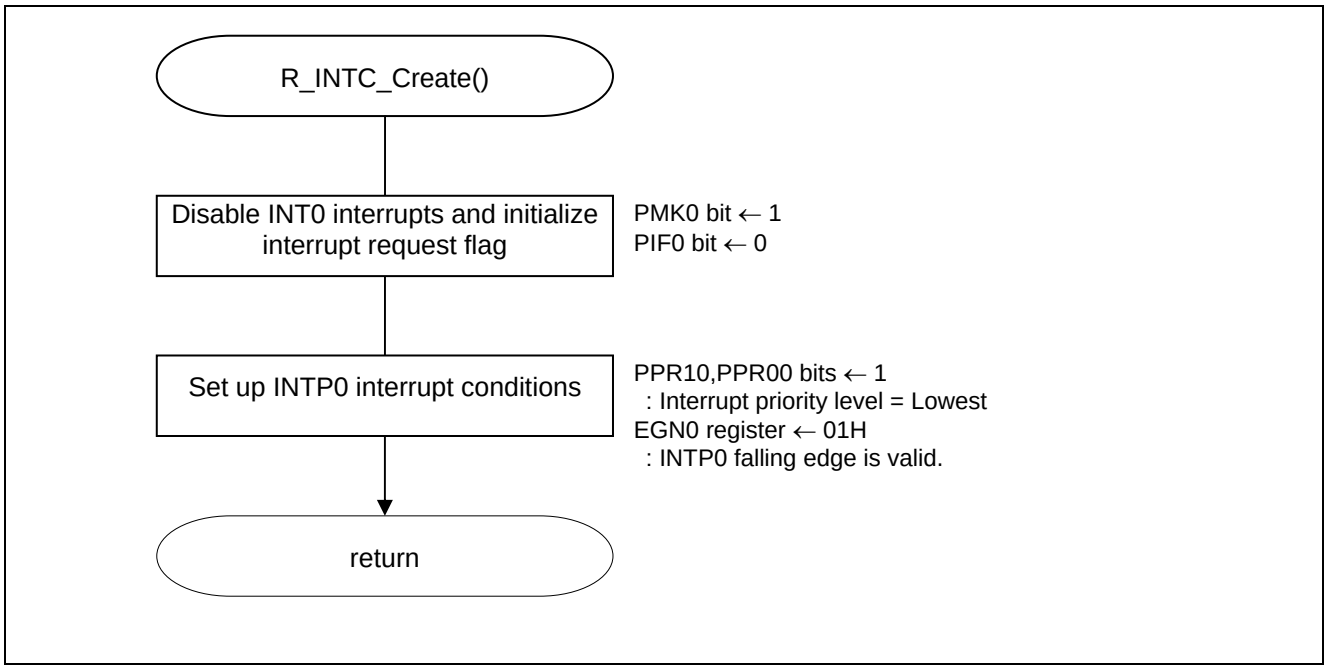


Figure 5.8 Setting up Interrupts

Setting up the INTP0 interrupt

- Interrupt request flag register (IF0L)
  Clear the interrupt request flag.
- Interrupt mask flag register (MK0L)
  Clear the interrupt mask.

Symbol: IF0L

7	6	5	4	3	2	1	0
PIF5	PIF4	PIF3	PIF2	PIF1	PIF0	LVIIF	WDTIIF
x	x	x	x	x	**0**	x	x

Bit 7

PIF0	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Symbol: MK0L

7	6	5	4	3	2	1	0
PMK5	PMK4	PMK3	PMK2	PMK1	PMK0	LVIMK	WDTIMK
x	x	x	x	x	**1**	x	x

Bit 7

PMK0	Interrupt processing control
0	Interrupt processing enabled
1	**Interrupt processing disabled**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up the INTP0 interrupt priority

- Priority specification flag registers (PR00L, PR10L)
  Interrupt priority level: Level 3 (lowest level)

Symbol: PR00L

7	6	5	4	3	2	1	0
PPR05	PPR04	PPR03	PPR02	PPR01	PPR00	LVIPR0	WDTIPR0
x	x	x	x	x	**1**	x	x

; Symbol: PR10L

7	6	5	4	3	2	1	0
PPR15	PPR14	PPR13	PPR12	PPR11	PPR10	LVIPR1	WDTIPR1
x	x	x	x	x	**1**	x	x

Bit 2

PPR00	PPR10	Priority level selection
0	0	Specify level 0 (highest level)
0	1	Specify level 1
1	0	Specify level 2
1	**1**	**Specify level 3 (lowest level)**

Setting up INTP0 pin edge sense mode

- External interrupt rising edge enable register (EGP0)
- External interrupt falling edge enable register (EGN0)
  INTP0 pin edge detection mode: Falling edge

Symbol: EGP0

7	6	5	4	3	2	1	0
EGP7	EGP6	EGP5	EGP4	EGP3	EGP2	EGP1	EGP0
x	x	x	x	x	x	x	**0**

Symbol: EGN0

7	6	5	4	3	2	1	0
EGN7	EGN6	EGN5	EGN4	EGN3	EGN2	EGN1	EGN0
x	x	x	x	x	x	x	**1**

Bit 0

EGP0	EGN0	INTP0 pin valid edge selection
0	0	Edge detection disabled
0	**1**	**Falling edge**
1	0	Rising edge
1	1	Both rising and falling edges

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.8 Main Processing

Figures 5.9 shows the flowcharts for the main processing.

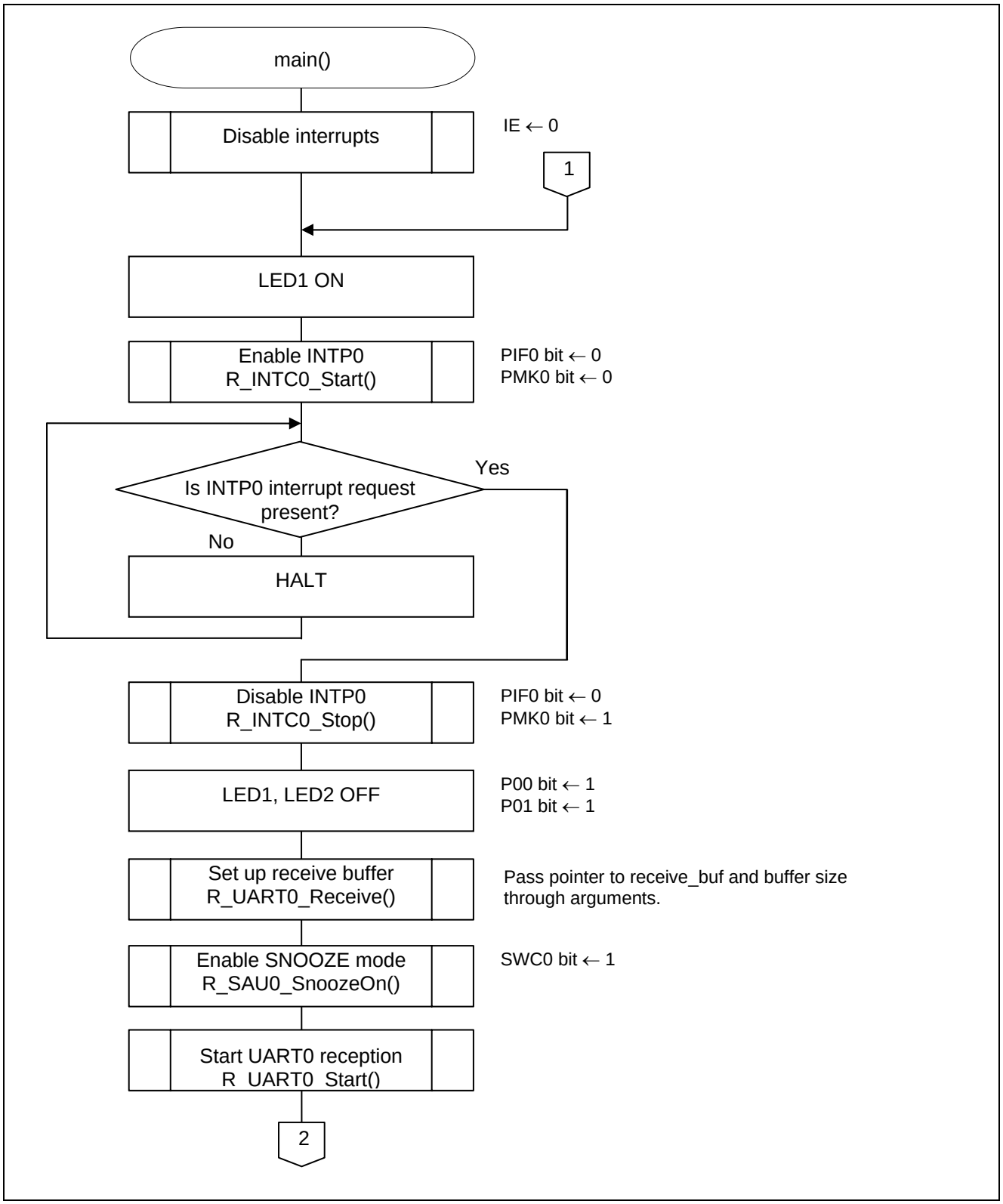


Figure 5.9 Main Processing (1/2)

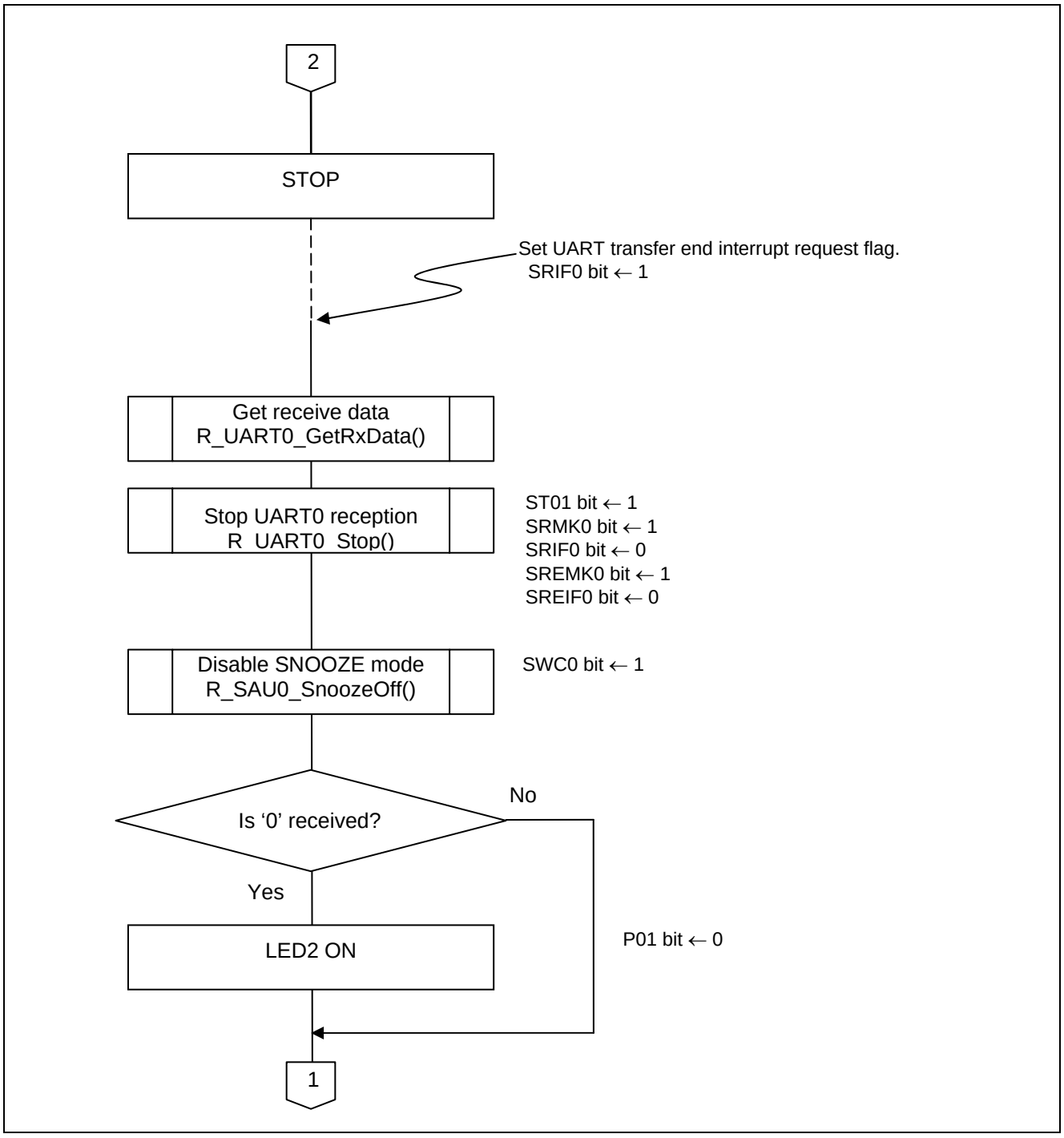


Figure 5.9 Main Processing (2/2)

5.7.9 Enabling UART0 Operation in SNOOZE Mode

Figure 5.10 shows the flowchart for enabling the UART0 operation in SNOOZE mode.

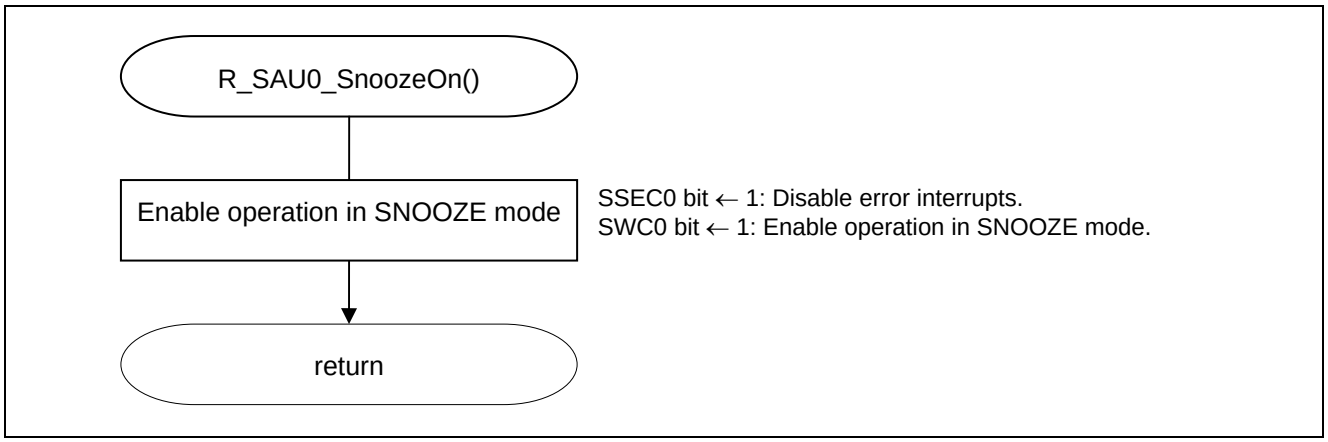


Figure 5.10 Enabling UART0 Operation in SNOOZE Mode

Controlling the SNOOZE mode

- Serial standby control register 0 (SSC0)
  Disable error interrupts (INTSRE0/INTSRE2).
  Enable the startup of reception in STOP mode.

Symbol: SSC0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	SSEC0	SWC0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	**1**

Bit 1

SSEC0	Selection of whether to enable or stop the generation of transfer end interrupts
0	Enable the generation of error interrupts (INTSRE0/INTSRE2). In the following cases, the clock request signal (an internal signal) to the clock generator is also cleared: • When the SWC0 bit is cleared to 0 • When the UART reception start bit is mistakenly detected
1	**Stop the generation of error interrupts (INTSRE0/INTSRE2).** **In the following cases, the clock request signal (an internal signal) to the clock generator is also cleared:** • **When the SWC0 bit is cleared to 0** • **When the UART reception start bit is mistakenly detected** • **When the transfer end interrupt generation timing is based on a parity error or framing error**

Bit 0

SWC0	Selection of whether to enable or stop the startup of CSI00 or UART0 reception while in the STOP mode
0	Stop the startup of reception while in the STOP mode.
1	**Enable the startup of reception while in the STOP mode.** **(During asynchronous CSI00/CSI20 reception or UART0/UART2 reception, the baud rate adjustment function is enabled.)**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.10 Disabling UART0 Operation in SNOOZE Mode

Figure 5.11 shows the flowchart for disabling the UART0 operation in SNOOZE mode.

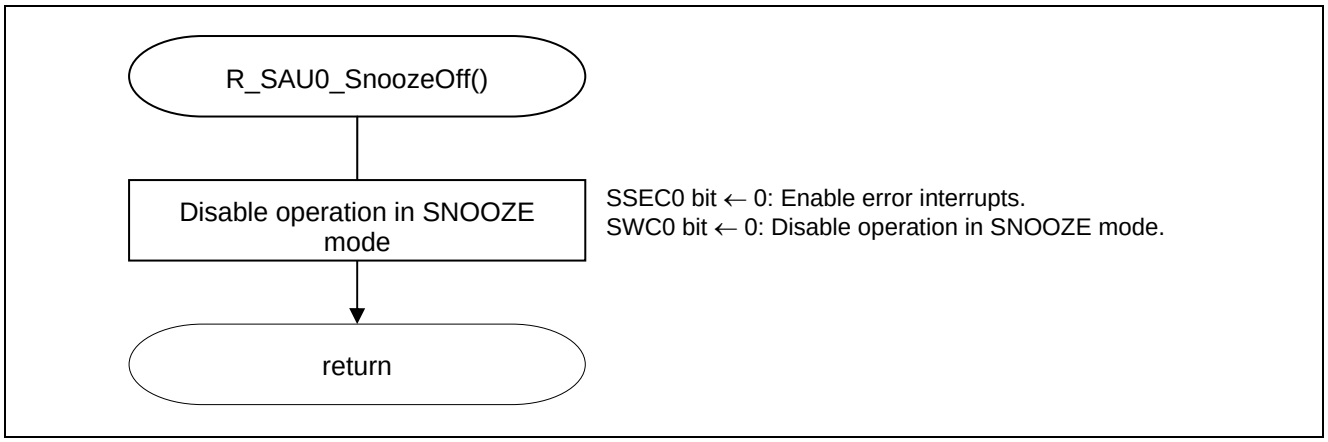


Figure 5.11 Disabling UART0 Operation in SNOOZE Mode

Controlling the SNOOZE mode

- Serial standby control register (SSC0)
  Enable error interrupts (INTSRE0/INTSRE2).
  Disable startup of reception in STOP mode.

Symbol: SSC0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	SSEC0	SWC0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0**	**0**

Bit 1

SSEC0	Selection of whether to enable or stop the generation of transfer end interrupts
0	**Enable the generation of error interrupts (INTSRE0/INTSRE2).** **In the following cases, the clock request signal (an internal signal) to the clock generator is also cleared:** • **When the SWC0 bit is cleared to 0** • **When the UART reception start bit is mistakenly detected**
1	Stop the generation of error interrupts (INTSRE0/INTSRE2). In the following cases, the clock request signal (an internal signal) to the clock generator is also cleared: • When the SWC0 bit is cleared to 0 • When the UART reception start bit is mistakenly detected • When the transfer end interrupt generation timing is based on a parity error or framing error

Bit 0

SWC0	Selection of whether to enable or stop the startup of CSI00 or UART0 reception while in the STOP mode
0	**Stop the startup of reception while in the STOP mode.**
1	Enable the startup of reception while in the STOP mode. (During asynchronous CSI00/CSI20 reception or UART0/UART2 reception, the baud rate adjustment function is enabled.)

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.11 Starting UART0 Reception

Figure 5.12 shows the flowchart for starting UART0 reception.

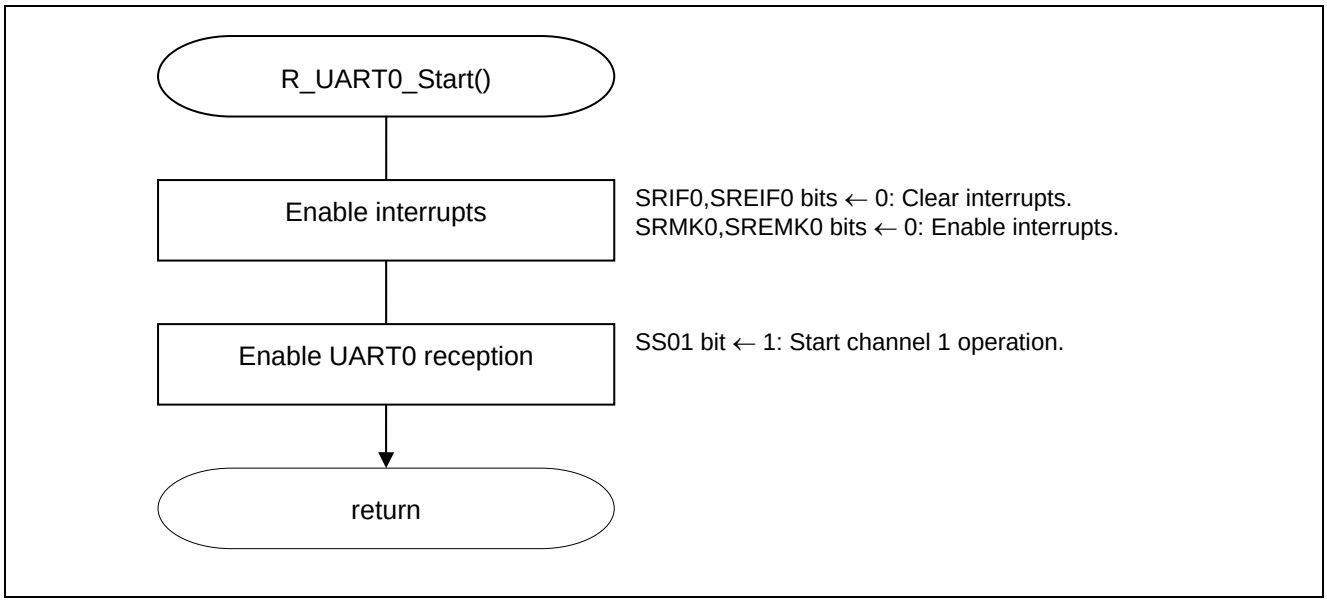


Figure 5.12 Starting UART0 Reception

Setting the startup standby of UART0 reception

- Serial channel start register 0 (SS0)
  Switch channel 1 to communication wait status.

Symbol: SS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	SS03	SS02	SS01	SS00
0	0	0	0	0	0	0	0	0	0	0	0	**0**	**0**	**1**	**0**

Bits 3 to 0

SS01	Operation start trigger of channel 1
0	No trigger operation
1	**Sets the SE01 bit to 1 and enters the communication wait status.**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.12 Stopping UART Reception

Figure 5.13 shows the flowchart for stopping UART reception.

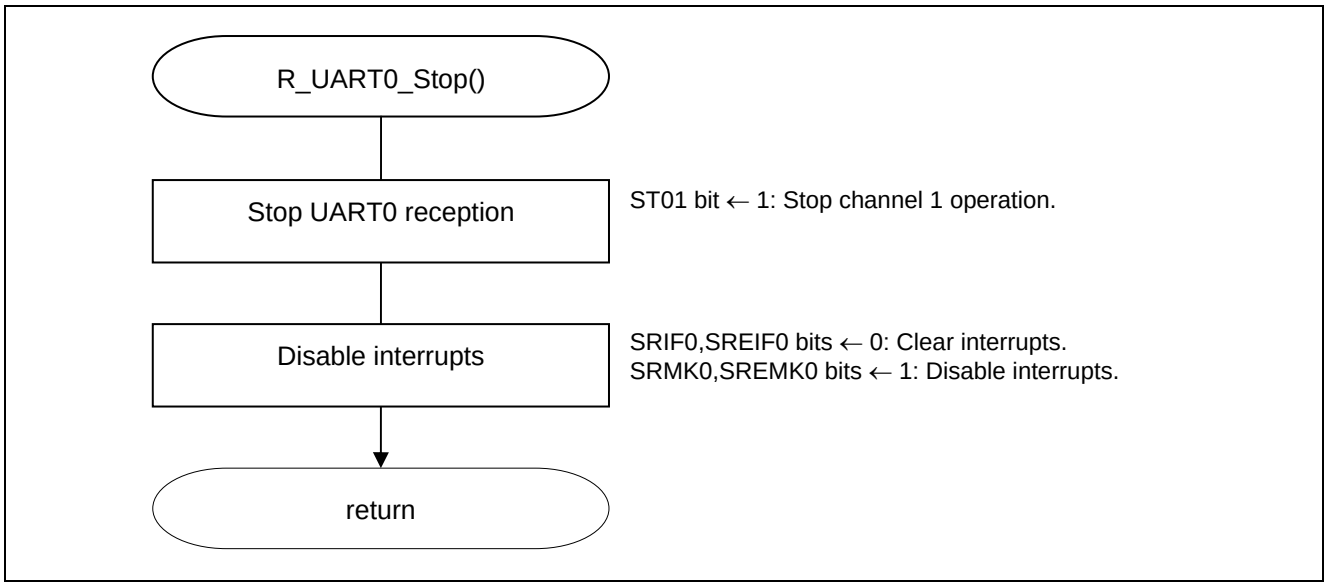


Figure 5.13 Stopping UART Reception

Setting the startup standby of UART0 reception

- Serial channel stop register 0 (ST0)
  Enable stopping channel 1 communication.

Symbol: ST0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	ST03	ST02	ST01	ST00
0	0	0	0	0	0	0	0	0	0	0	0	**0**	**0**	**1**	**0**

Bits 3 to 0

ST01	Operation start trigger of channel 1
0	No trigger operation
1	**Sets the SE01 bit to 1 and enters the communication wait status [Note].**

Note: Communication stops while holding the value of the control register and shift register, and the status of the serial clock I/O pin, serial data output pin, and each error flag (FEFmn: framing error flag, PEFmn: parity error flag, and OVFmn: overrun error flag).

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.13 Setting up UART0 Receive Buffer

Figure 5.14 shows the flowchart for setting up the UART0 receive buffer.

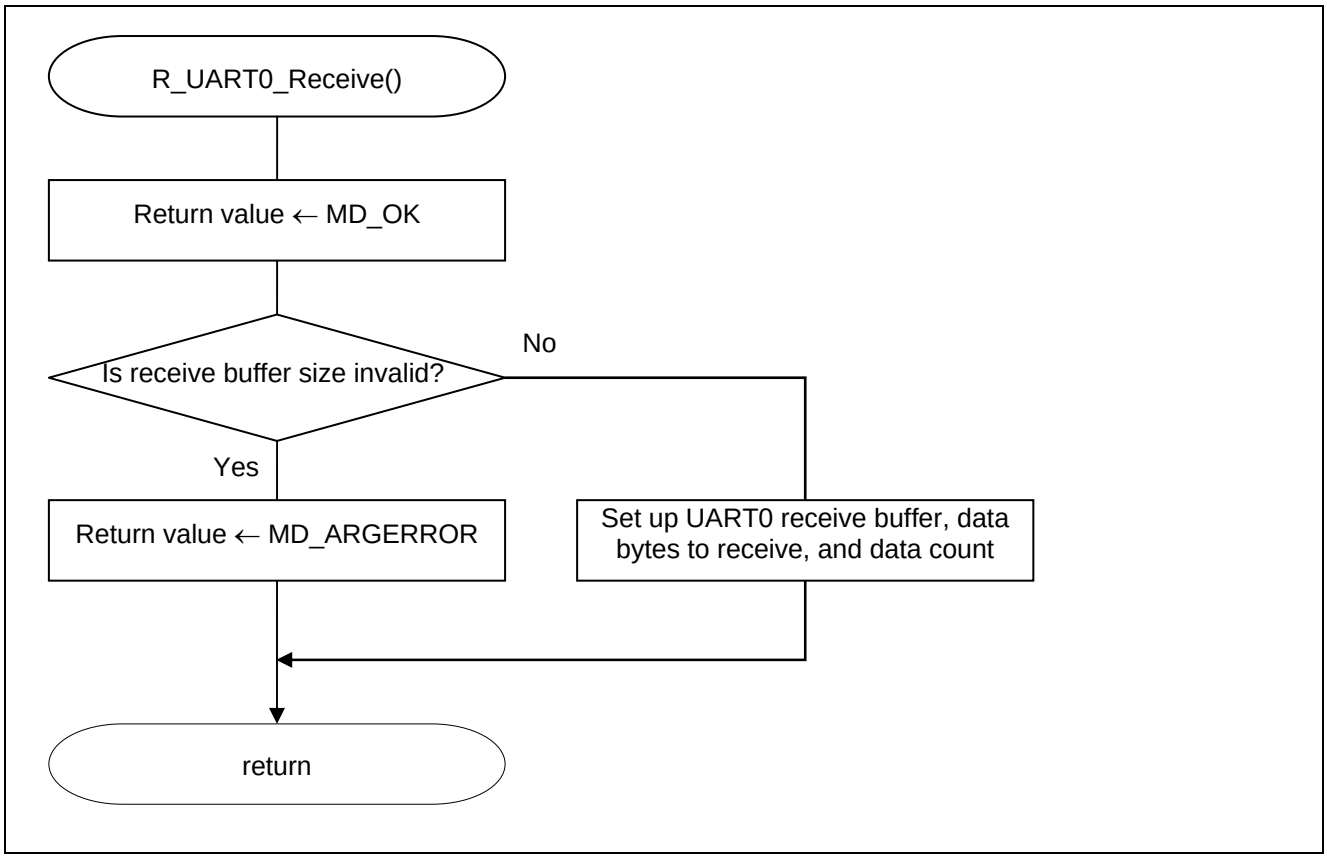


Figure 5.14 Setting up UART0 Receive Buffer

5.7.14 Starting INTP0 Operation

Figure 5.15 shows the flowchart for starting INTP0 operation.

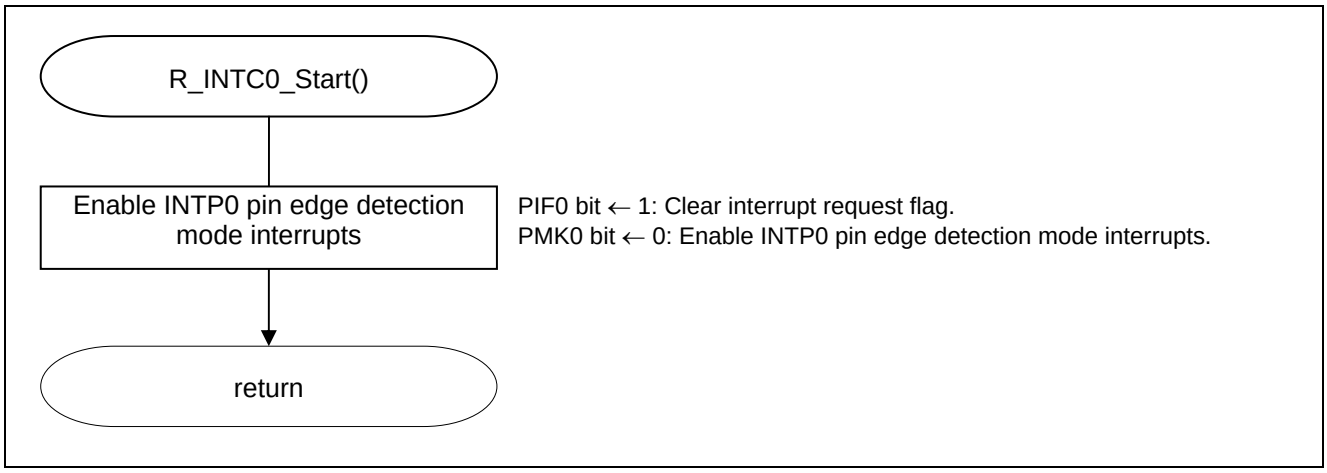


Figure 5.15 Starting INTP0 Operation

Setting up the INTP0 interrupt

- Interrupt request flag register (IF0L)
  Clear interrupt request flag.
- Interrupt mask flag register (MK0L)
  Clear interrupt mask.

Symbol: IF0L

7	6	5	4	3	2	1	0
PIF5	PIF4	PIF3	PIF2	PIF1	PIF0	LVIIF	WDTIIF
x	x	x	x	x	**0**	x	x

Bit 2

PIF0	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Symbol: MK0L

7	6	5	4	3	2	1	0
PMK5	PMK4	PMK3	PMK2	PMK1	PMK0	LVIMK	WDTIMK
x	x	x	x	x	**0**	x	x

Bit 0

PMK0	Interrupt processing control
0	**Interrupt processing enabled**
1	Interrupt processing disabled

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.15 Stopping INTP0

Figure 5.16 shows the flowchart for stopping INTP0.

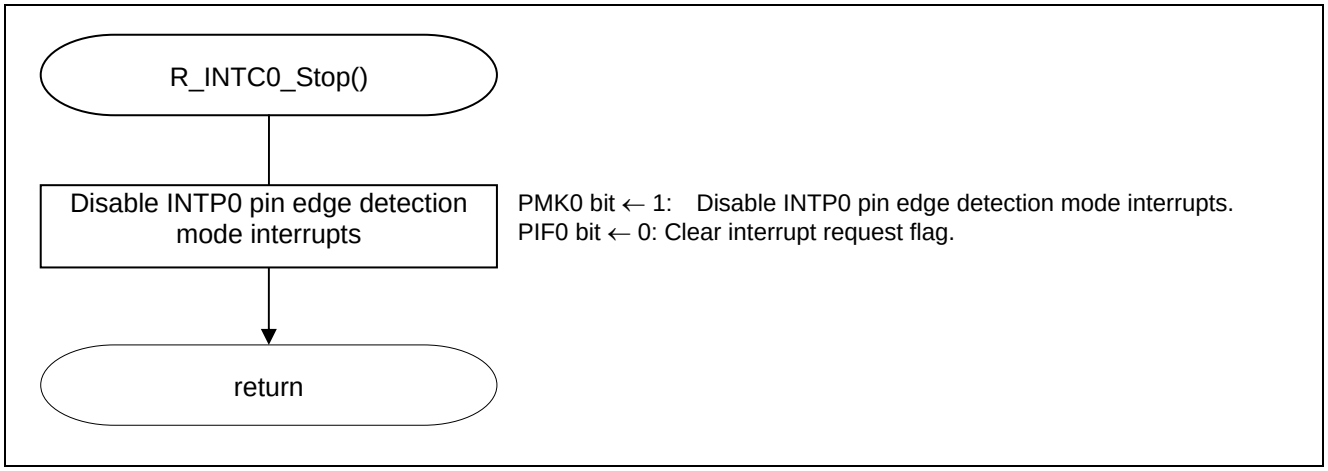


Figure 5.16 Stopping INTP0 Operation

5.7.16 Getting UART0 Receive Data

Figure 5.17 shows the flowchart for getting UART0 receive data.

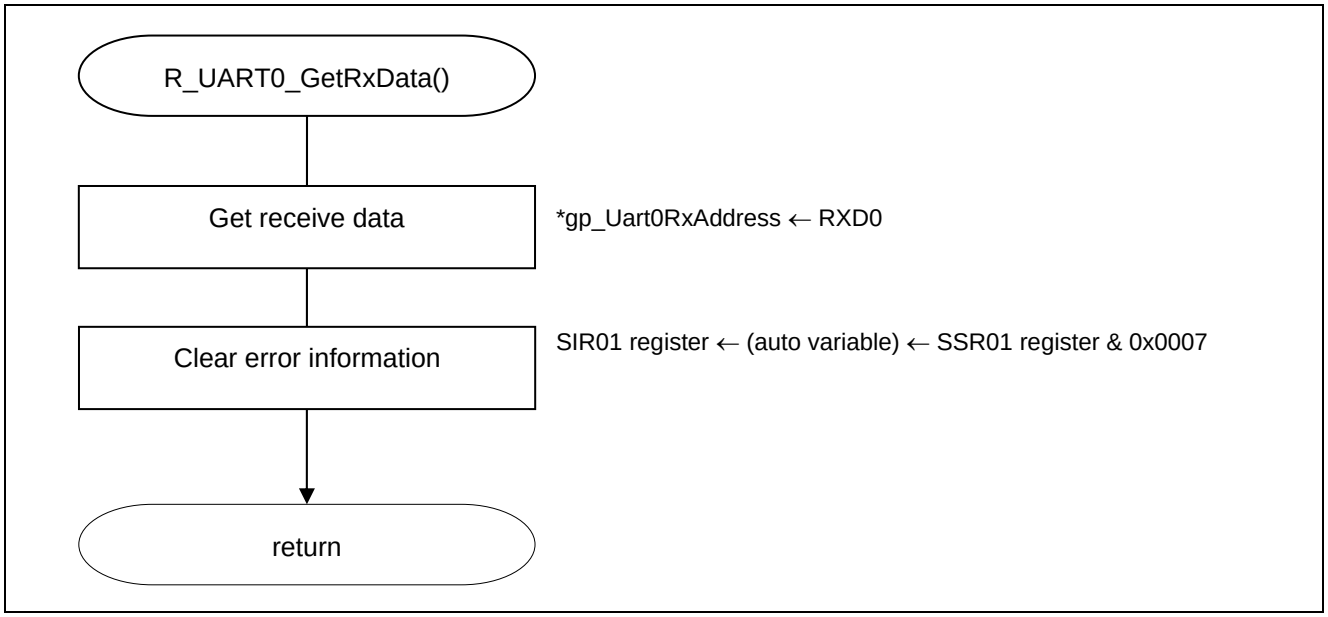
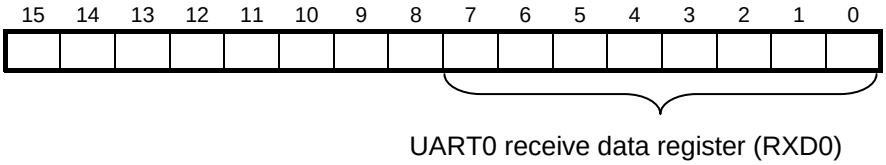


Figure 5.17 Getting UART0 Receive Data

Getting UART0 receive data

- Serial data register 01 (SDR01)
  Receive buffer RXD0

Symbol: SDR01



The receive data is written to the lower 8 bits of SDR01.

The lower 8 bits are accessed as the RXD0 register.

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

6. Sample Code

The sample code is available on the Renesas Electronics Website.

7. Documents for Reference

RL78/G13 User's Manual: Hardware (R01UH0146E)

RL78 Family User's Manual: Software (R01US0015E)

(The latest versions of the documents are available on the Renesas Electronics Website.)

Technical Updates/Technical Brochures

(The latest versions of the documents are available on the Renesas Electronics Website.)

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Revision Record	RL78/G13 Low-power Consumption Operation (UART in SNOOZE Mode)

Rev.	Date	Description	
		Page	Summary
1.00	Apr. 16, 2015	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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