RL78/G13

A/D Converter (SNOOZE Mode)

Introduction

This application note describes how to use the low power consumption setting which uses the SNOOZE mode of A/D conversion. By using the SNOOZE mode, this sample program performs A/D conversion without starting the CPU. The converted values are stored in the RL78/G13's internal RAM and the latest 10 A/D conversion values are retained.

Target Device

RL78/G13

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specification

This application note provides examples of using the SNOOZE mode of the A/D converter. The A/D conversion trigger is set to "Hardware trigger (real-time clock interrupt signal)," the SNOOZE mode of the A/D converter is specified as "Use the SNOOZE mode function," and the A/D conversion standby status is set. Then, the STOP instruction is executed. When a hardware trigger is detected in the STOP mode, the A/D conversion starts in the SNOOZE mode.

Subsequently, the conversion result is subjected to data conversion (shifting the data by six bits to the right) and the result is stored in the RL78/G13's internal RAM. Table 1.1 lists the peripheral function to be used and its use. Figure 1.1 shows the outline of the SNOOZE mode operation of the A/D converter. The numbers in Figure 1.1 correspond to those in section 5.1, Operation Outline.

Table 1.1   Peripheral Function to be Used and its Use

| Peripheral Function	Use
A/D converter	Converts the level of the analog signal input from the P20/ANI0 pin.
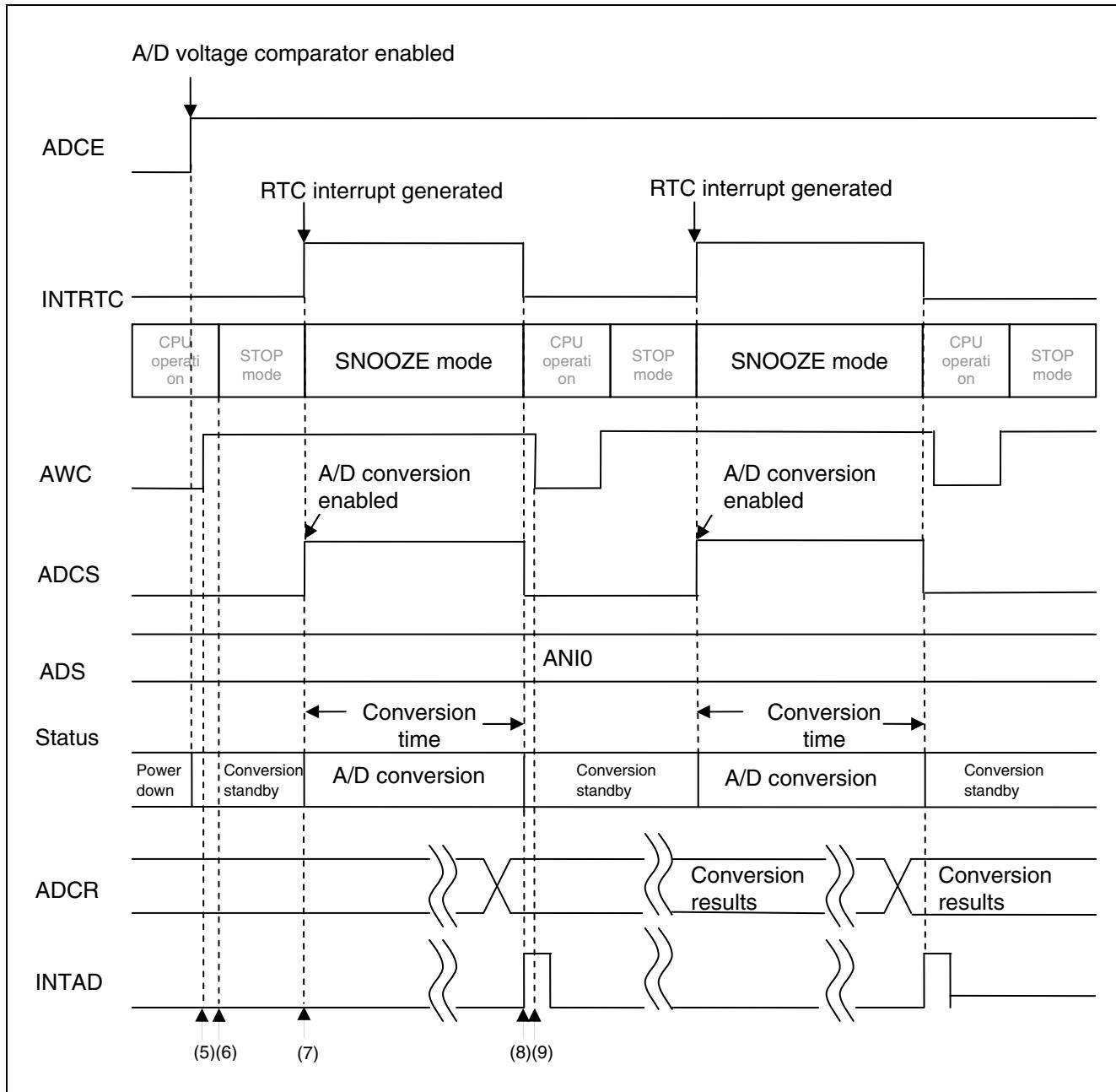
Figure 1.1 Outline of SNOOZE Operation of A/D Converter

Remark For (5) to (9) in Figure 1.1, refer to section 5.1, Operation Outline.

R01AN1464EJ0100 Rev. 1.00   Page 4 of 42

Sep 10, 2013

2.   Operation Check Conditions

The sample code contained in this application note has been checked under the conditions listed in the table below.

Table 2.1   Operation Check Conditions

Item	Description
Microcontroller used	RL78/G13 (R5F100LEA)
Operating frequency	• High-speed on-chip oscillator clock: 32 MHz • CPU/peripheral hardware clock: 32 MHz
Operating voltage	5.0 V (Operation is possible over a voltage range of 2.9 V to 5.5 V.) LVD operation (V_{LVI}): Reset mode which uses 2.81 V (2.76 V to 2.87 V)
Integrated development environment	CubeSuite + V1.03.00 from Renesas Electronics Corp.
C compiler	CA78K0R V1.50 from Renesas Electronics Corp.
Board to be used	RSK for RL78/G13 CPU board (R0K5010RLC010BR)

3.   Related Application Notes

The application notes that are related to this application note are listed below for reference.

RL78/G13 Initialization (R01AN0451E) Application Note
RL78/G13 A/D Converter (Software Trigger and Sequential Conversion Modes) (R01AN0452E) Application Note

4. Description of the Hardware

4.1 Hardware Configuration Example

Figure 4.1 shows hardware that is used for this application note.
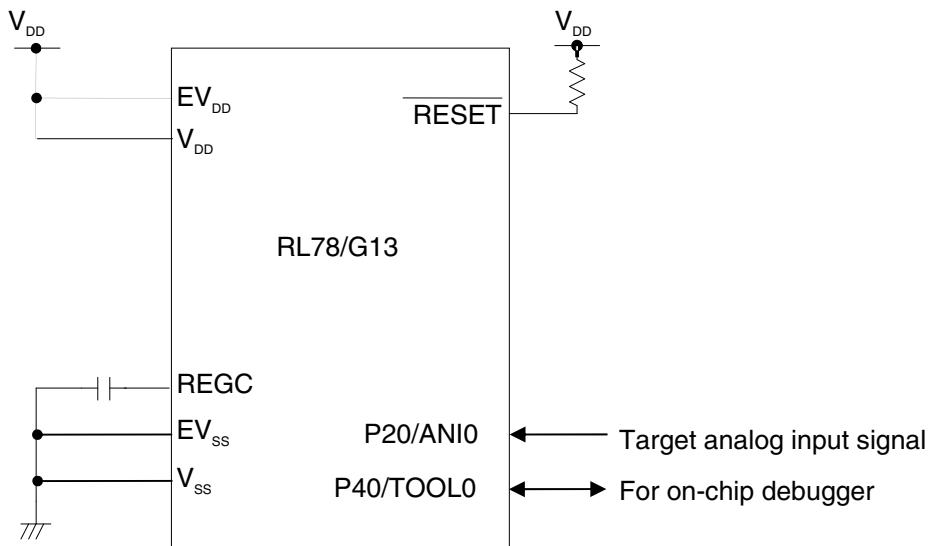
**Figure 4.1   Hardware Configuration Example**

Cautions   1   The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-dedicated ports separately to V_{DD} or V_{SS} via a resistor).

           2   Connect any pins whose name begins with EV_{SS} to V_{SS} and any pins whose name begins with EV_{DD} to V_{DD}, respectively.

           3   V_{DD} must be held at not lower than the reset release voltage (V_{LVI}) that is specified as LVD.

4.2 List of Pins to be Used

Table 4.1 lists the pin to be used and its function.

Table 4.1   Pin to be Used and its Function

Pin Name	I/O	Function
P20/ANI0	Input	A/D converter analog input port

5.   Description of the Software

5.1   Operation Outline

This sample code, which uses the SNOOZE mode of the A/D converter, performs A/D conversion on the analog voltage that is input to pin ANI0 by the input of a hardware trigger in the STOP mode. It waits the generation of A/D conversion end interrupts. After A/D conversion is completed, the sample code shifts the result of A/D conversion by six bits to the right and places the result in the internal RAM of the RL78/G13.

The bottom in Figure 1.1 describes the timing when the processing below is performed.

(1) Initialize the A/D converter.
<Setup conditions>

- Pin P20/ANI0 is used for the analog input.
- A/D conversion channel selection mode is set to select mode.
- A/D conversion operation mode is set to one-shot conversion mode.
- A/D conversion is started using the hardware trigger.
- The real-time clock signal is used for the hardware trigger signal.
- The A/D conversion end interrupt (INTAD) is used.

(2) Initialize the RTC (used as a hardware trigger)
<Setup conditions>

- The constant-period interrupt is used for the RTC once per second.
(3) After initialization is completed, the ADCE bit in the ADM0 register is set to 1 (A/D conversion standby).

(4) The RTCE bit in the RTCC0 register is set to 1 (Starts counter operation) and the RTCMK bit in the MK1H register is set to 1 (RTC interrupt servicing disabled).

(5) The AWC bit is set to 1 and the SNOOZE mode is set.

(6) After entering the STOP mode, the sample code waits a hardware trigger.

(7) When a hardware trigger is input, A/D conversion starts.

(8) After completing the A/D conversion of the voltage input from pin ANI0, the A/D converter transfers the result of A/D conversion to the ADCR register and generates an A/D conversion end interrupt.

(9) When the A/D conversion end interrupt is generated, the A/D converter makes a transition from the SNOOZE mode to the normal operation mode and the AWC bit in the ADM2 register is set to 0. Subsequently, the sample code reads the result of A/D conversion from the ADCR register, shifts the result by six bits to the right, and stores the shifted data in the internal RAM of the RL78/G13.

(10) The sample code returns to step (5) to enter the SNOOZE mode again.

Caution   Refer to RL78/G13 User's Manual for notes on device use.

5.2 List of Option Byte Settings

Table 5.1 summarizes the settings of the option bytes.

Table 5.1   Option Byte Settings

Address	Value	Description
000C0H/010C0H	11101111B	Disables the watchdog timer. (Stops counting after the release of the reset state.)
000C1H/010C1H	01111111B	LVD reset mode, 2.81 V (2.76 to 2.87 V)
000C2H/010C2H	11101000B	HS mode HOCO: 32 MHz
000C3H/010C3H	10000100B	Enables the on-chip debugger. Erases data of flash memory in case of failures in authenticating on-chip debug security ID.

5.3 List of Constants

Table 5.2 lists the constant that is used in this sample program

Table 5.2   Constants for the Sample Program

Constant	Value	Description
MAX_BUFFER	AH	Number of buffers to retain A/D conversion results

5.4 List of Variables

Table 5.3 lists the global variables that are used by this sample program.

Table 5.3   Global Variables

Type	Variable Name	Description	Function Used
uint8_t	g_buffer_count	Number of buffer to be used	main ()
unsigned short	g_result_buffer [MAX_BUFFER]	Area for storing the A/D conversion results	main ()

5.5   List of Functions

Table 5.4 lists the functions that are used by this sample program.

Table 5.4   Functions

Function Name	Outline
R_ADC_Create	Sets the A/D converter.
R_ADC_Set_OperationOn	Enables the A/D voltage comparator.
R_ADC_Start	Starts waiting an A/D conversion trigger.
R_ADC_Get_Result	Obtains A/D conversion results.
R_ADC_Set_SnoozeOn	Starts the SNOOZE mode function of A/D conversion.
R_ADC_Set_SnoozeOff	Stops the SNOOZE mode function of A/D conversion.
R_RTC_Create	Sets the real-time clock.
R_RTC_Start	Starts the real-time clock.
R_MAIN_UserInit	Performs processing for starting the A/D converter and RTC.

5.6   Function Specifications

This section describes the specifications for the functions that are used in the sample code.

[Function Name] R_ADC_Create

Synopsis	Sets the A/D converter.
Header	r_cg_adc.h
Declaration	void R_ADC_Create (void)
Explanation	Enables the clock supply to the A/D converter (ADCEN = 1) and makes the settings related to A/D conversion as follows.
	Priority level of conversion end interrupt: 3 (ADPR0 = 1, ADPR1 = 1)
	Conversion time of A/D converter: About 3 µs (FR2 to FR0 = 101B)
	Channel selection mode: Select mode (ADMD = 0)
	Trigger mode: Hardware trigger wait mode (ADTMD1 and ADTMD0 = 11B)
	Operation mode: One-shot conversion mode (ADSCM = 1)
	Hardware trigger signal to be used: RTC interrupt signal (ADTRS1 and ADTRS0 = 10B)
	Resolution: 10-bit resolution (ADTYP = 0)
	+ side reference voltage source: V_{DD} (ADREFP1 and ADREF0 = 00B)
	- side reference voltage source: V_{SS} (ADREFM = 0)
	Upper limit of conversion result comparison: 255 (ADUL = FFH)
	Lower limit of conversion result comparison: 0 (ADLL = 00H)
	Analog input channel: ANI0 (ADS4 to ADS0 = 00000B, ADISS = 0)
Arguments	None
Return value	None
Remarks	None

[Function Name] R_ADC_Set_OperationOn

Synopsis	Enables the A/D voltage comparator.
Header	r_cg_adc.h
Declaration	void R_ADC_Set_OperationOn(void)
Explanation	Enables the A/D comparator (ADCE = 1).
Arguments	None
Return value	None
Remarks	None

[Function Name] R_ADC_Start

Synopsis	Starts waiting an A/D conversion trigger.
Header	r_cg_adc.h
Declaration	void R_ADC_Start (void)
Explanation	Clears the A/D conversion end interrupt flag (ADIF = 0), enables the A/D conversion end interrupt (ADMK = 0), and then starts controlling the RTC (RTCE = 1).
Arguments	None
Return value	None
Remarks	None

[Function Name] R_ADC_Get_Result

Synopsis	Obtains A/D conversion results.	
Header	r_cg_adc.h	
Declaration	void R_ADC_Get_Result(uint16_t *buffer)	
Explanation	Shifts the A/D conversion results 6 bits to the right and stores the results in the area designated by the argument.	
Arguments	buffer	Address of the area for storing the A/D conversion results
Return value	None	
Remarks	None	

[Function Name] R_ADC_Set_SnoozeOn

Synopsis	Starts the SNOOZE mode function of A/D conversion.
Header	r_cg_adc.h
Declaration	void R_ADC_Set_SnoozeOn(void)
Explanation	Uses the SNOOZE mode function of A/D conversion (AWC = 1).
Arguments	None
Return value	None
Remarks	None

[Function Name] R_ADC_Set_SnoozeOff

Synopsis	Stops the SNOOZE mode function of A/D conversion.
Header	r_cg_adc.h
Declaration	void R_ADC_Set_SnoozeOff(void)
Explanation	Stops the SNOOZE mode function of A/D conversion (AWC = 0).
Arguments	None
Return value	None
Remarks	None

[Function Name] R_RTC_Create

Synopsis	Sets the real-time clock.
Header	R_cg_rtc.h
Declaration	void R_RTC_Create (void)
Explanation	Starts the input clock supply to the RTC (RTCEN = 1), sets the RTC interrupt priority level to 3 (RTCPR1 = 1, RTCPR0 = 1), and sets the generation period of the RTC interrupt to once per second (CT2 to CT0 = 010B).
Arguments	None
Return value	None
Remarks	None

[Function Name] R_RTC_Start

Synopsis	Starts the real-time clock.
Header	R_cg_rtc.h
Declaration	void R_RTC_Start(void)
Explanation	Clears the RTC interrupt request flag (RTCIF = 0), enables the RTC interrupt servicing (RTCMK = 0), and then starts the real-time clock (RTCE = 1).
Arguments	None
Return value	None
Remarks	None

[Function Name] R_MAIN_UserInit

Synopsis	Performs processing for starting the A/D converter and RTC.
Header	R_cg_rtc.h
Declaration	void R_MAIN_UserInit (void)
Explanation	Calls R_ADC_Set_OperationOn. Calls R_ADC_Start after the stabilization time of the A/D voltage comparator has elapsed. Starts the A/D converter. Then, calls R_RTC_Start to start the RTC. After the start of the RTC, performs processing below for making a transition to the HALT/STOP mode. Sets RWAIT to 1. Performs polling until RWST is set to 1. Sets RWAIT to 0. Performs polling until RWST is set to 0. Then, disable the RTC interrupt servicing (RTCMK = 1).
Arguments	None
Return value	None
Remarks	None

5.7   Flowcharts

Figure 5.1 shows the overall flow of the sample program described in this application note.
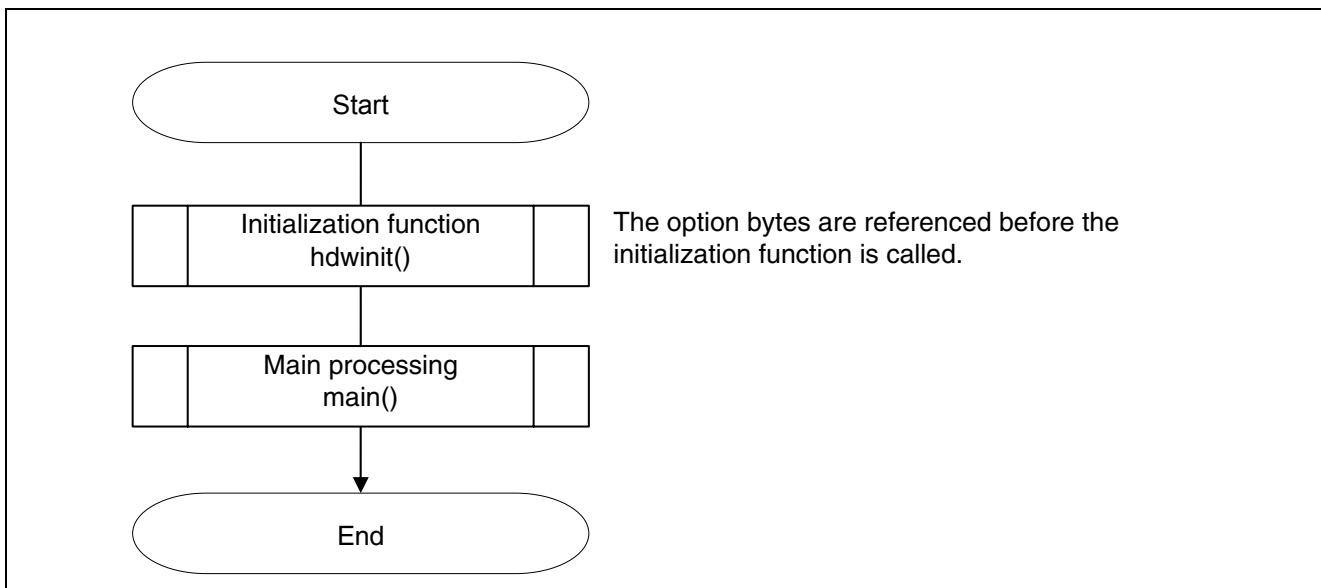

Figure 5.1   Overall Flow

5.7.1　Initialization Function

Figure 5.2 shows the flowchart for the initialization function.
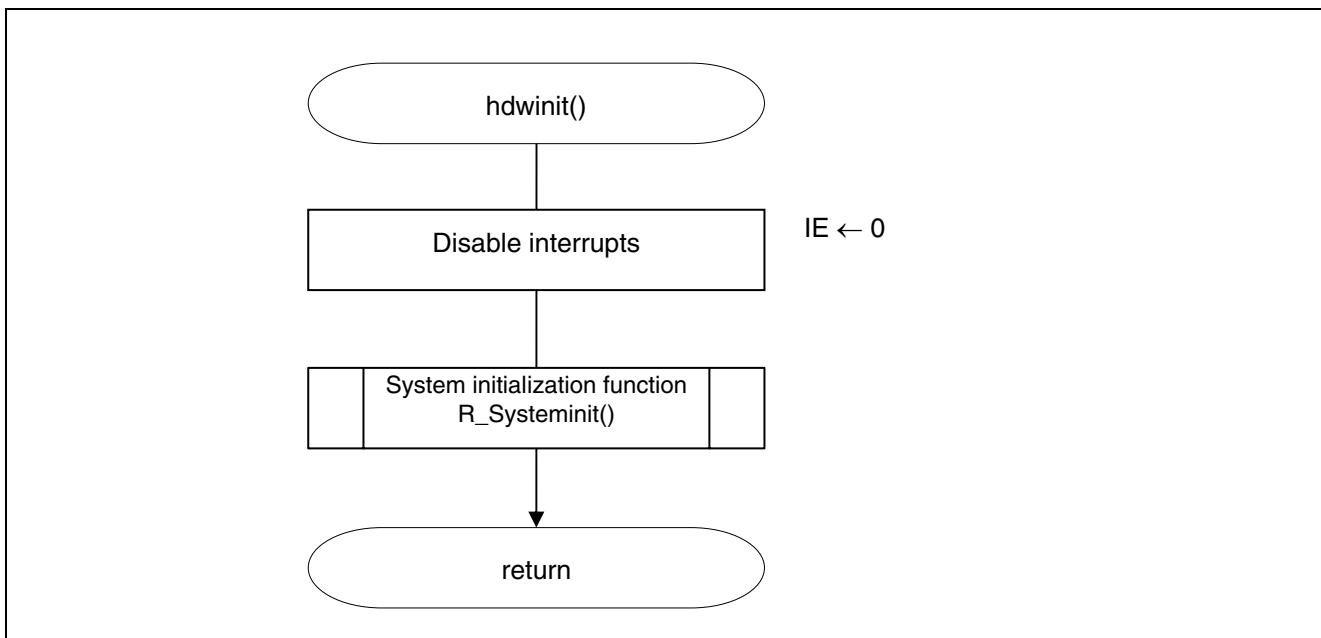
Figure 5.2　　Initialization Function

5.7.2   System Initialization Function

Figure 5.3 shows the flowchart for the system initialization function.
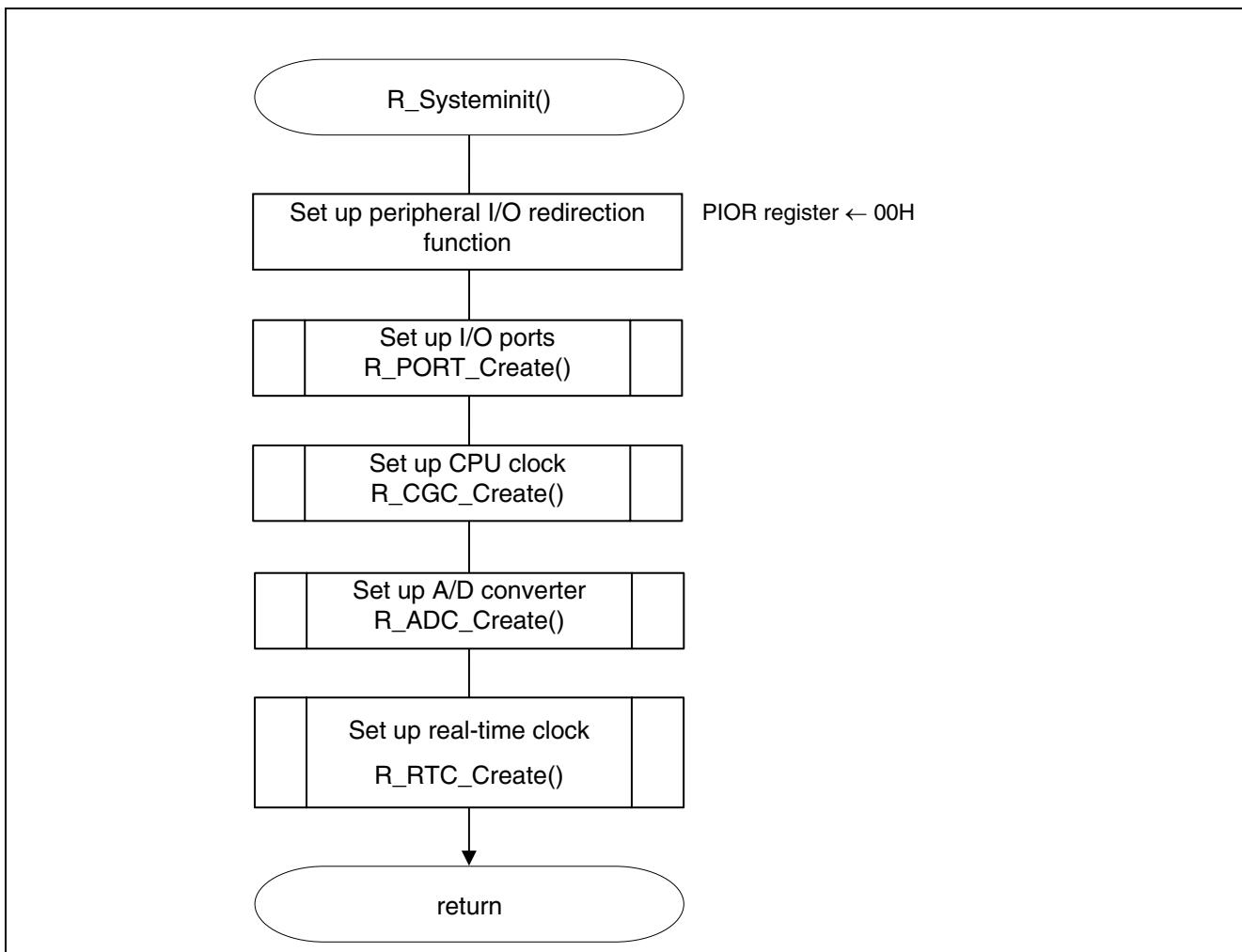
Figure 5.3   System Initialization Function

5.7.3   I/O Port Setup

Figure 5.4 shows the flowchart for setting up the I/O port.
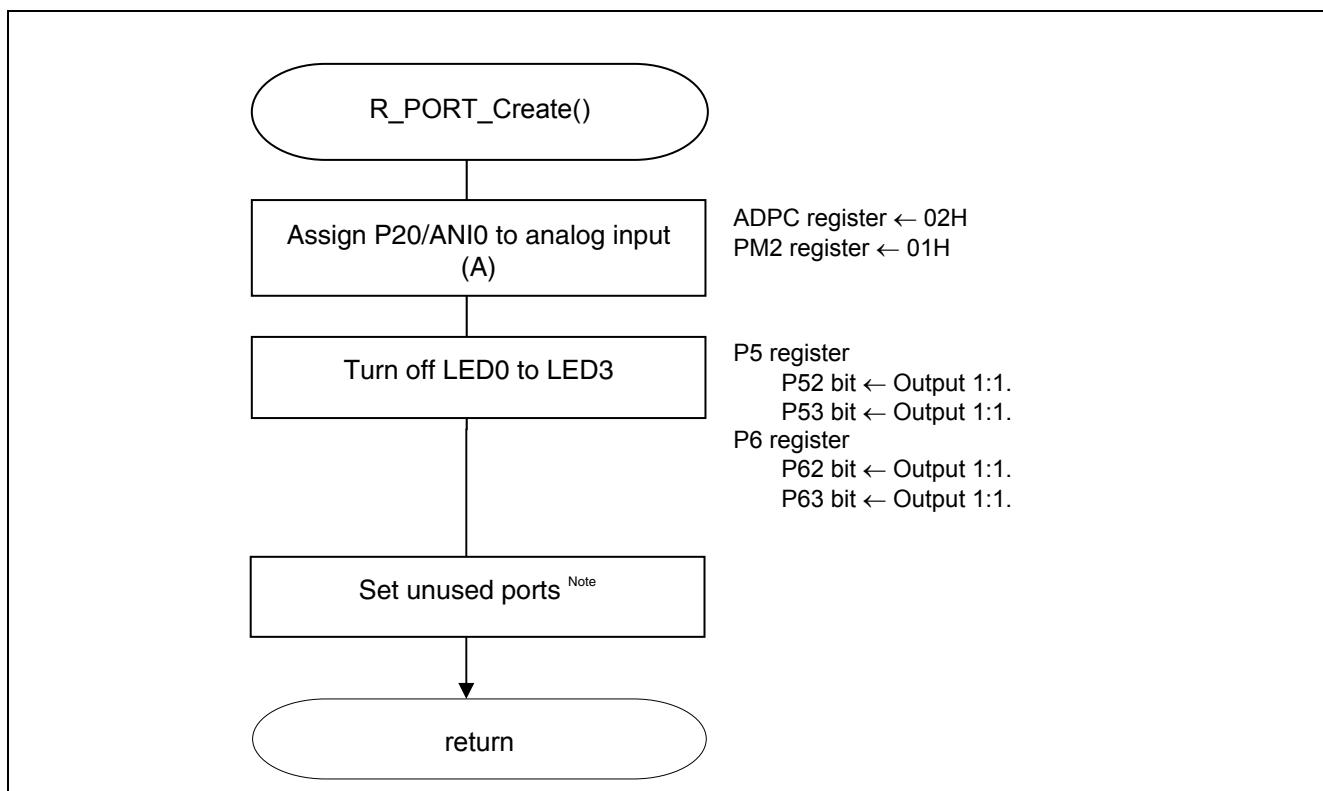

Figure 5.4   I/O Port Setup

Note   Refer to the section entitled "Flowcharts" in RL78/G13 Initialization Application Note (R01AN0451E) for the configuration of the unused ports.

Caution   Provide proper treatment for unused pins so that their electrical specifications are observed. Connect each of any unused input-only ports to V_{DD} or V_{SS} via separate resistors.

Setting up the channel to be used for A/D conversion

- A/D port configuration register (ADPC)
  Switches between A/D converter analog input and port digital I/O.
- Port mode register 2 (PM2)
  Selects the I/O mode of the LED lighting control port and output latch.

Symbol: ADPC

7	6	5	4	3	2	1	0
0	0	0	0	ADPC3	ADPC2	ADPC1	ADPC0
0	0	0	0	**0**	**0**	**1**	**0**

Bits 3 to 0

ADPC3	ADPC2	ADPC1	ADPC0	Available Analog Input
0	0	0	0	ANI0 to ANI14
0	0	0	1	None
0	**0**	**1**	**0**	**ANI0**
0	0	1	1	ANI0 to ANI1
0	1	0	0	ANI0 to ANI2
0	1	0	1	ANI0 to ANI3
0	1	1	0	ANI0 to ANI4
0	1	1	1	ANI0 to ANI5
1	0	0	0	ANI0 to ANI6
1	0	0	1	ANI0 to ANI7
1	0	1	0	ANI0 to ANI8
1	0	1	1	ANI0 to ANI9
1	1	0	0	ANI0 to ANI10
1	1	0	1	ANI0 to ANI11
1	1	1	0	ANI0 to ANI12
1	1	1	1	ANI0 to ANI13

Symbol: PM2

7	6	5	4	3	2	1	0
PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20
x	x	x	x	x	x	x	**1**

Bit 0

PM20	PM20 pin I/O mode selection
0	Output mode (output buffer on)
1	**Input mode (output buffer off)**

Caution   For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.4   CPU Clock Setup

Figure 5.5 shows the flowchart for setting up the CPU clock.

The flowchart:

- **R_CGC_Create()**
- **Set up high-speed system clock/subsystem clock**
  - CMC register ← 10H: Use high-speed system clock.
  - MSTOP bit ← 1: Use subsystem clock.
  - XTSTOP bit ← 0
- **Select CPU/peripheral hardware clock (f_{CLK})**
  - MCM0 bit ← 0: Select high-speed OCO clock (f_{IH}) as main system clock (f_{MAIN}).
  - CSS bit ← 0: Select main system clock (f_{MAIN}) as CPU/peripheral hardware clock (f_{CLK}).
- **return**
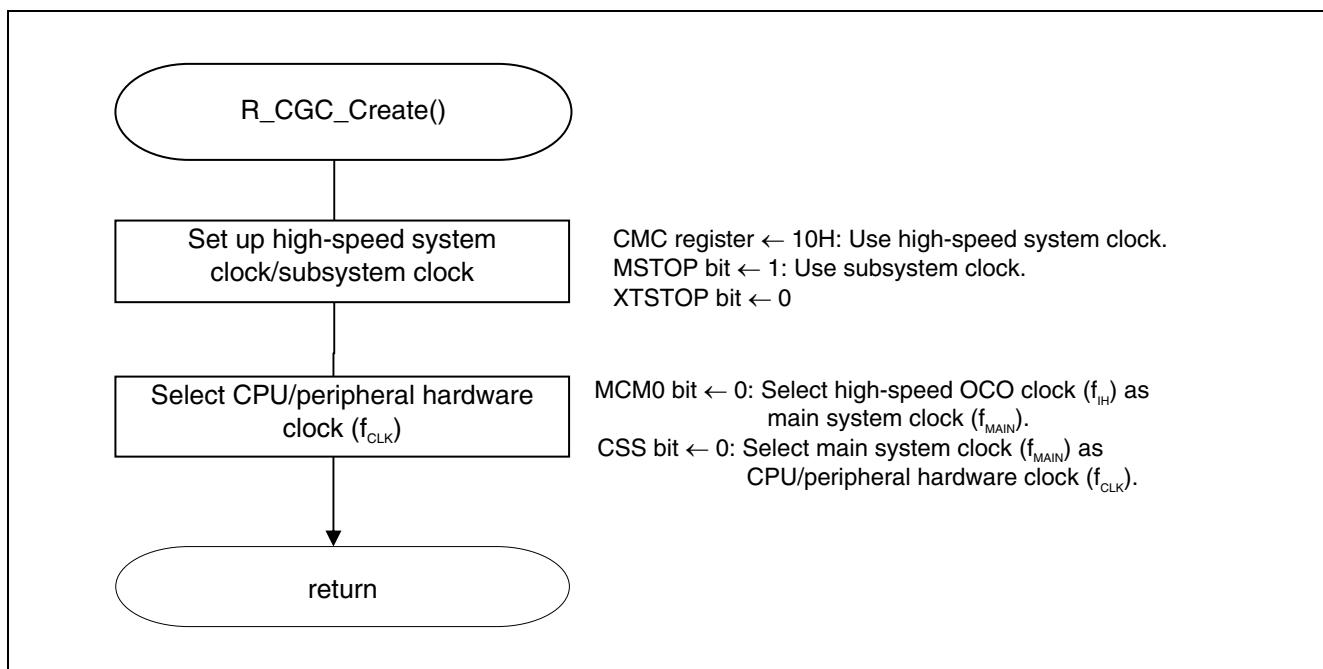
Figure 5.5   CPU Clock Setup

Caution   For details on the procedure for setting up the CPU clock (R_CGC_Create ()), refer to the section entitled "Flowcharts" in RL78/G13 Initialization Application Note (R01AN0451E).

5.7.5 A/D Converter Setup

Figure 5.6 shows the flowchart for setting up the A/D converter.

The following lists the flowchart contents:

R_ADC_Create ()

Process	Register settings
Supply clock to A/D converter circuit	ADCEN bit ← 1: Start supply of input clock.
Stop A/D converter	ADM0 register ← 00H
Clear A/D conversion end interrupt request flag	ADIF bit ← 0: Clear interrupt request flag.
Disable A/D conversion end interrupts	ADMK bit ← 1: Disable A/D conversion end interrupt servicing.
Set A/D converter interrupt priority level to 3	ADPR0 bit ← 1 ADPR1 bit ← 1

Initialize A/D converter
• Set conversion time to about 3 μs
• Set select mode
• Set software trigger mode
	ADM0 register ← 28H
	   FR2 to FR0 bits = 101B: $f_{CLK}/5$ (f_{CLK} = 32 MHz)
	   ADMD bit ← 0: Select mode
	ADM1 register ← E2H
	   ADTMD1 and ADTMD0 bits = 11B
	   : Hardware trigger wait mode
	ADSCM bit ← 1: One-shot conversion mode
	   ADTRS1 and ADTRS0 bits ← 10B
	   : Real-time clock interrupt signal

Set up reference voltage source
• 10-bit resolution
• Set + side reference voltage source to V_{DD}
• Set - side reference voltage source to V_{SS}
	ADM2 register ← 00H
	   ADREFP1 and ADREF0 bits = 00B
	   : Supply power from V_{DD}
	   ADTYP ← 0: 10-bit resolution
	   ADREFM ← 0: Supply power from V_{SS}

Set up upper/lower limit of conversion result comparison
• Set upper limit comparison to FFH
• Set lower limit comparison to 00H
	ADUL register ← FFH
	   Set the upper limit of conversion result comparison.
	ADLL register ← 00H
	   Set the lower limit of conversion result comparison.

Specify analog input channel
• Set analog input channel to ANI0
	ADS register ← 00H
	   ADS4 to ADS0 bits = 00000B
	   ADISS bit ← 0

return

Figure 5.6   A/D Converter Setup

Starting the supply of clock to the A/D converter

- Peripheral enable register 0 (PER0)
  Starts the supply of the clock to the A/D converter.

Symbol: PER0

7	6	5	4	3	2	1	0
RTCEN	IICA1EN	ADCEN	IICA0EN	SAU1EN	SAU0EN	TAU1EN	TAU0EN
x	x	**1**	x	x	x	x	x

Bit 5

ADCEN	Control of A/D converter input clock supply
0	Stops input clock supply.
1	**Enables input clock supply.**

Caution   For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up the A/D conversion time and operation mode

- A/D converter mode register 0 (ADM0)
  Controls the A/D conversion operation.
  Specifies the A/D conversion channel selection mode.

Symbol: ADM0

7	6	5	4	3	2	1	0
ADCS	ADMD	FR2	FR1	FR0	LV1	LV0	ADCE
x	0	1	0	1	0	0	x

Bit 6

ADMD	Specification of the A/D conversion channel selection mode
0	**Select mode**
1	Scan mode

Bits 5 to 1

ADM0					Mode	Conversion Time Selection					Conversion clock (f_{AD})
FR2	FR1	FR0	LV1	LV2		f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 32 MHz	
0	0	0	**0**	**0**	**Normal 1**	Setting prohibited	Setting prohibited	Setting prohibited	108 µs	54 µs	f_{CLK}/64
0	0	1						108 µs	54 µs	27 µs	f_{CLK}/32
0	1	0					108 µs	54 µs	27 µs	13.5 µs	f_{CLK}/16
0	1	1					54 µs	27 µs	13.5 µs	6.75 µs	f_{CLK}/8
1	0	0					40.5 µs	20.25 µs	10.125 µs	5.0625 µs	f_{CLK}/6
1	**0**	**1**				135 µs	33.75 µs	16.875 µs	8.4375 µs	**4.21875 µs**	**f_{CLK}/5**
1	1	0				108 µs	27 µs	13.5 µs	6.75 µs	3.375 µs	f_{CLK}/4
1	1	1				54 µs	13.5 µs	6.75 µs	3.375 µs	Setting prohibited	f_{CLK}/2
0	0	0	0	1	Normal 2	Setting prohibited	Setting prohibited	Setting prohibited	100 µs	50 µs	f_{CLK}/64
0	0	1						100 µs	50 µs	25 µs	f_{CLK}/32
0	1	0					100 µs	50 µs	25 µs	12.5 µs	f_{CLK}/16
0	1	1					50 µs	25 µs	12.5 µs	6.25 µs	f_{CLK}/8
1	0	0					37.5 µs	18.75 µs	9.375 µs	4.6875 µs	f_{CLK}/6
1	0	1				125 µs	31.25 µs	15.625 µs	7.8125 µs	3.90625 µs	f_{CLK}/5
1	1	0				100 µs	25 µs	12.5 µs	6.25 µs	3.125 µs	f_{CLK}/4
1	1	1				50 µs	12.5 µs	6.25 µs	3.125 µs	Setting prohibited	f_{CLK}/2

Caution For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up the A/D conversion trigger mode

- A/D converter mode register 1 (ADM1)
  Selects the A/D conversion trigger mode.
  Selects the A/D conversion mode.
  Selects the hardware trigger signal.

Symbol: ADM1

7	6	5	4	3	2	1	0
ADTMD1	ADTMD0	ADSCM	0	0	0	ADTRS1	ADTRS0
1	**1**	**1**	x	x	x	**1**	**0**

Bits 7 and 6

ADTMD1	ADTMD0	Selection of the A/D conversion trigger mode
0	x	Software trigger mode
1	0	Hardware trigger no-wait mode
1	**1**	**Hardware trigger wait mode**

Bit 5

ADSCM	Specification of the A/D conversion mode
0	Sequential conversion mode
1	**One-shot conversion mode**

Bits 1 and 0

ADTRS1	ADTRS0	Selection of the hardware trigger signal
0	0	End of timer channel 01 count or capture interrupt signal (INTTM01)
0	1	Setting prohibited
1	**0**	**Real-time clock interrupt signal (INTRTC)**
1	1	12-bit interval timer interrupt signal (INTIT)

Caution   For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up the reference voltage source

- A/D converter mode register 2 (ADM2)
  Selects the + side reference voltage source of the A/D converter.
  Selects the – side reference voltage source of the A/D converter.
  Checks the upper limit and lower limit conversion result values.
  Sets up the SNOOZE mode.
  Sets up the A/D conversion resolution.

Symbol: ADM2

7	6	5	4	3	2	1	0
ADREFP1	ADREFP0	ADREFM	0	ADRCK	AWC	0	ADYTP
0	**0**	**0**	x	**0**	**0**	**0**	**0**

Bits 7 and 6

ADREFP1	ADREFP0	Selection of the + side reference voltage source of the A/D converter
0	**0**	**Supplied from V_{DD}**
0	1	Supplied from P20/AV_{REFP}/ANI0
1	0	Supplied from the internal reference voltage (1.45 V)
1	1	Setting prohibited

Bit 5

ADREFM	Selection of the − side reference voltage source of the A/D converter
0	**Supplied from V_{SS}**
1	Supplied from P21/AV_{REFM}/ANI1

Bit 3

ADRCK	Checking the upper limit and lower limit conversion result values
0	**The interrupt signal (INTAD) is output when the ADLL register ≤ the ADCR register ≤ the ADUL register.**
1	The interrupt signal (INTAD) is output when the ADCR register < the ADLL register (AREA 2) or the ADUL register < the ADCR register.

Bit 2

AWC	Specification of the SNOOZE mode
0	**Do not use the SNOOZE mode function.**
1	Use the SNOOZE mode function.

Bit 0

ADTYP	Selection of the A/D conversion resolution
0	**10-bit resolution**
1	8-bit resolution

Caution   For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up the conversion result comparison upper limit/lower limit

- Conversion result comparison upper limit setting register (ADUL)
- Conversion result comparison lower limit setting register (ADLL)
  Sets up the conversion result comparison upper- and lower-limit values.

Symbol: ADUL

7	6	5	4	3	2	1	0
ADUL7	ADUL6	ADUL5	ADUL4	ADUL3	ADUL2	ADUL1	ADUL0
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Symbol: ADLL

7	6	5	4	3	2	1	0
ADLL7	ADLL6	ADLL5	ADLL4	ADLL3	ADLL2	ADLL1	ADLL0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Caution   For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Specifying the input channel

- Analog input channel specification register (ADS)
  Specifies the input channel for the analog voltage to be subjected to A/D conversion.

  Symbol: ADS

7	6	5	4	3	2	1	0
ADISS	0	0	ADS4	ADS3	ADS2	ADS1	ADS0
0	x	x	**0**	**0**	**0**	**0**	**0**

Bits 7 and 4 to 0

ADISS	ADS4	ADS3	ADS2	ADS1	ADS0	Analog input channel	Input source
0	**0**	**0**	**0**	**0**	**0**	**ANI0**	**P20/ANI0 pin/AV$_{REFP}$ pin**
0	0	0	0	0	1	ANI1	P21/ANI1 pin/AV$_{REFM}$ pin
0	0	0	0	1	0	ANI2	P22/ANI2 pin
0	0	0	0	1	1	ANI3	P23/ANI3 pin
0	0	0	1	0	0	ANI4	P24/ANI4 pin
0	0	0	1	0	1	ANI5	P25/ANI5 pin
0	0	0	1	1	0	ANI6	P26/ANI6 pin
0	0	0	1	1	1	ANI7	P27/ANI7 pin
0	0	1	0	0	0	ANI8	P150/ANI8 pin
0	0	1	0	0	1	ANI9	P151/ANI9 pin
0	0	1	0	1	0	ANI10	P152/ANI10 pin
0	0	1	0	1	1	ANI11	P153/ANI11 pin
0	0	1	1	0	0	ANI12	P154/ANI12 pin
0	0	1	1	0	1	ANI13	P155/ANI13 pin
0	0	1	1	1	0	ANI14	P156/ANI14 pin
0	0	1	1	1	1	Setting prohibited	
0	1	0	0	0	0	ANI16	P03/ANI16 pin [Note 1]
0	1	0	0	0	1	ANI17	P02/ANI17 pin [Note 2]
0	1	0	0	1	0	ANI18	P147/ANI18 pin
0	1	0	0	1	1	ANI19	P120/ANI19 pin
0	1	0	1	0	0	ANI20	P100/ANI20 pin
0	1	0	1	0	1	ANI21	P37/ANI21 pin
0	1	0	1	1	0	ANI22	P36/ANI22 pin
0	1	0	1	1	1	ANI23	P35/ANI23 pin
0	1	1	0	0	0	ANI24	P117/ANI24 pin
0	1	1	0	0	1	ANI25	P116/ANI25 pin
0	1	1	0	1	0	ANI26	P115/ANI26 pin
0	1	1	0	1	1	Setting prohibited	
1	0	0	0	0	0	—	Temperature sensor output voltage [Note 3]
1	0	0	0	0	1	—	Internal reference voltage (1.45 V) [Note 3]
Other than above						Setting prohibited	

Notes 1 20-, 24-, 25-, 30-, 32-pin products: P01/ANI16 pin
       2 20-, 24-, 25-, 30-, 32-pin products: P00/ANI17 pin
       3 This setting can be used only in HS (high-speed main) mode.
Caution For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up A/D conversion end interrupts
- Interrupt request flag register (IF1H)
  Clears the interrupt request flag.
- Interrupt mask flag register (MK1H)
  Disables interrupt servicing.

Symbol: IF1H

7	6	5	4	3	2	1	0
TMIF04	TMIF13	SRIF3 CSIIF31 IICIF31	STIF3 CSIIF30 IICIF30	KRIF	ITIF	RTCIF	ADIF
x	x	x	x	x	x	x	**0**

Bit 0

ADIF	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Symbol: MK1H

7	6	5	4	3	2	1	0
TMMK04	TMMK13	SRMK3 CSIMK31 IICMK31	STMK3 CSIMK30 IICMK30	KRMK	ITMK	RTCMK	ADMK
x	x	x	x	x	x	x	**1**

Bit 0

ADMK	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

Caution   For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.6 Real-Time Clock Setup

Figure 5.7 shows the flowchart for setting up the real-time clock.
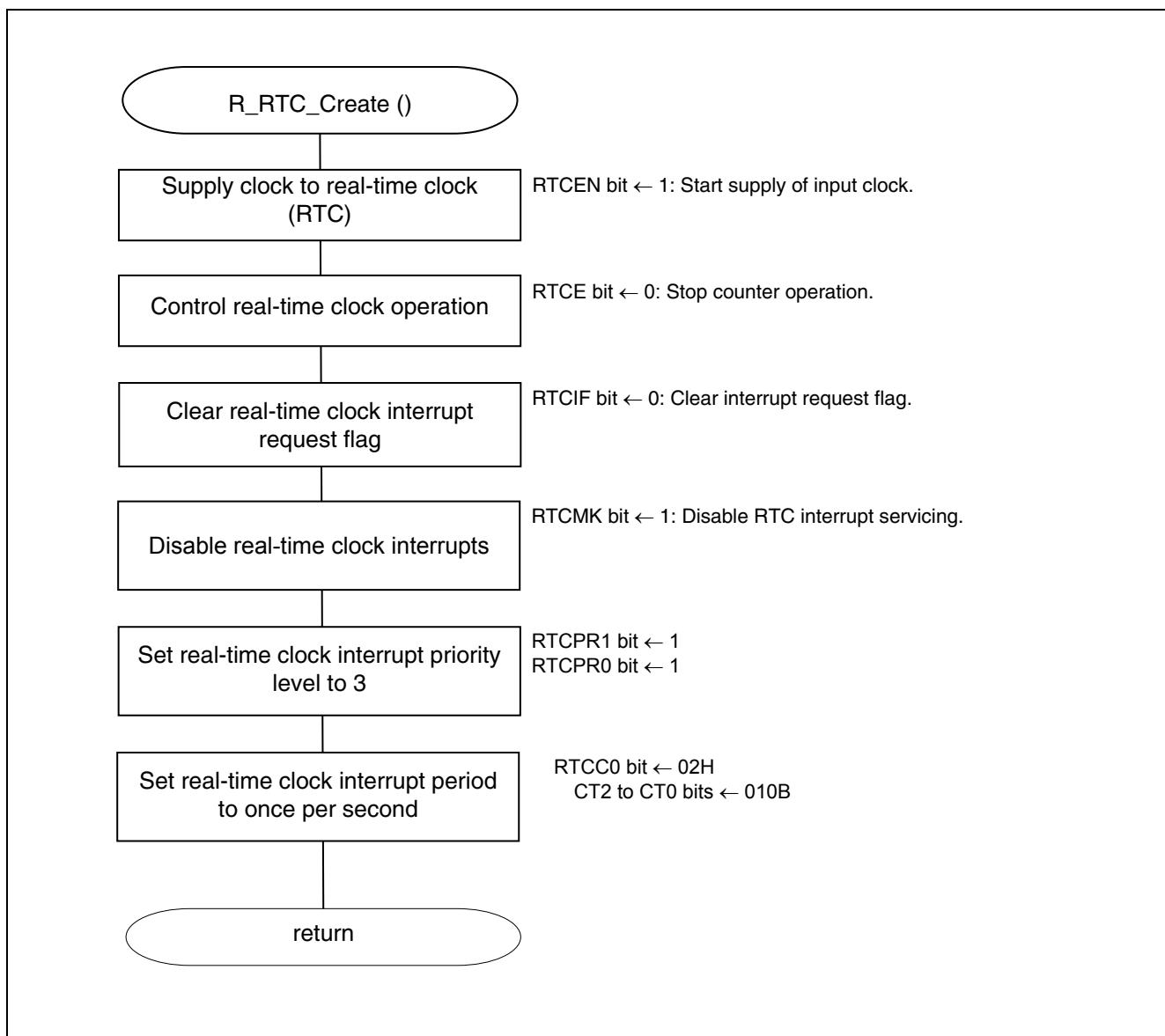

Figure 5.7   Real-Time Clock Setup

Starting the supply of clock to the real-time clock

- Peripheral enable register 0 (PER0)
  Starts the supply of the clock to the real-time clock.

Symbol: PER0

7	6	5	4	3	2	1	0
RTCEN	IICA1EN	ADCEN	IICA0EN	SAU1EN	SAU0EN	TAU1EN	TAU0EN
1	x	x	x	x	x	x	x

Bit 7

RTCEN	Control of A/D converter input clock supply
0	Stops input clock supply.
1	**Enables input clock supply.**

Setting up the operation of the real-time clock and interrupt priority level

- Peripheral enable register 0 (RTCC0)
  Stops the counter operation of the real-time clock.
  Sets the interrupt period.

Symbol: RTCC0

7	6	5	4	3	2	1	0
RTCE	0	RCLOE1	0	AMPM	CT2	CT1	CT0
0	x	x	x	x	**0**	**1**	**0**

Bit 7

RTCE	Control of A/D converter input clock supply
0	**Stops counter operation.**
1	Starts counter operation.

Bits 2 to 0

CT2	CT1	CT0	Constant-period interrupt (INTRTC) selection
0	0	0	Does not use constant-period interrupt function.
0	0	1	Once per 0.5 s (synchronized with second count up)
0	**1**	**0**	**Once per 1 s (same time as second count up)**
0	1	1	Once per 1 m (second 00 of every minute)
1	0	0	Once per 1 hour (minute 00 and second 00 of every hour)
1	0	1	Once per 1 day (hour 00, minute 00, and second 00 of every day)
1	1	×	Once per 1 month (Day 1, hour 00 a.m., minute 00, and second 00 of every month)

Caution   For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up real-time clock interrupts
- Interrupt request flag register (IF1H)
  Clears the interrupt request flag.
- Interrupt mask flag register (MK1H)
  Disables interrupt servicing.

Symbol: IF1H

7	6	5	4	3	2	1	0
TMIF04	TMIF13	SRIF3 CSIIF31 IICIF31	STIF3 CSIIF30 IICIF30	KRIF	ITIF	RTCIF	ADIF
x	x	x	x	x	x	**0**	x

Bit 1

RTCIF	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Symbol: MK1H

7	6	5	4	3	2	1	0
TMMK04	TMMK13	SRMK3 CSIMK31 IICMK31	STMK3 CSIMK30 IICMK30	KRMK	ITMK	RTCMK	ADMK
x	x	x	x	x	x	**1**	x

Bit 1

RTCMK	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

Caution   For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.7 Main Processing

Figure 5.8 shows the flowchart for the main processing.
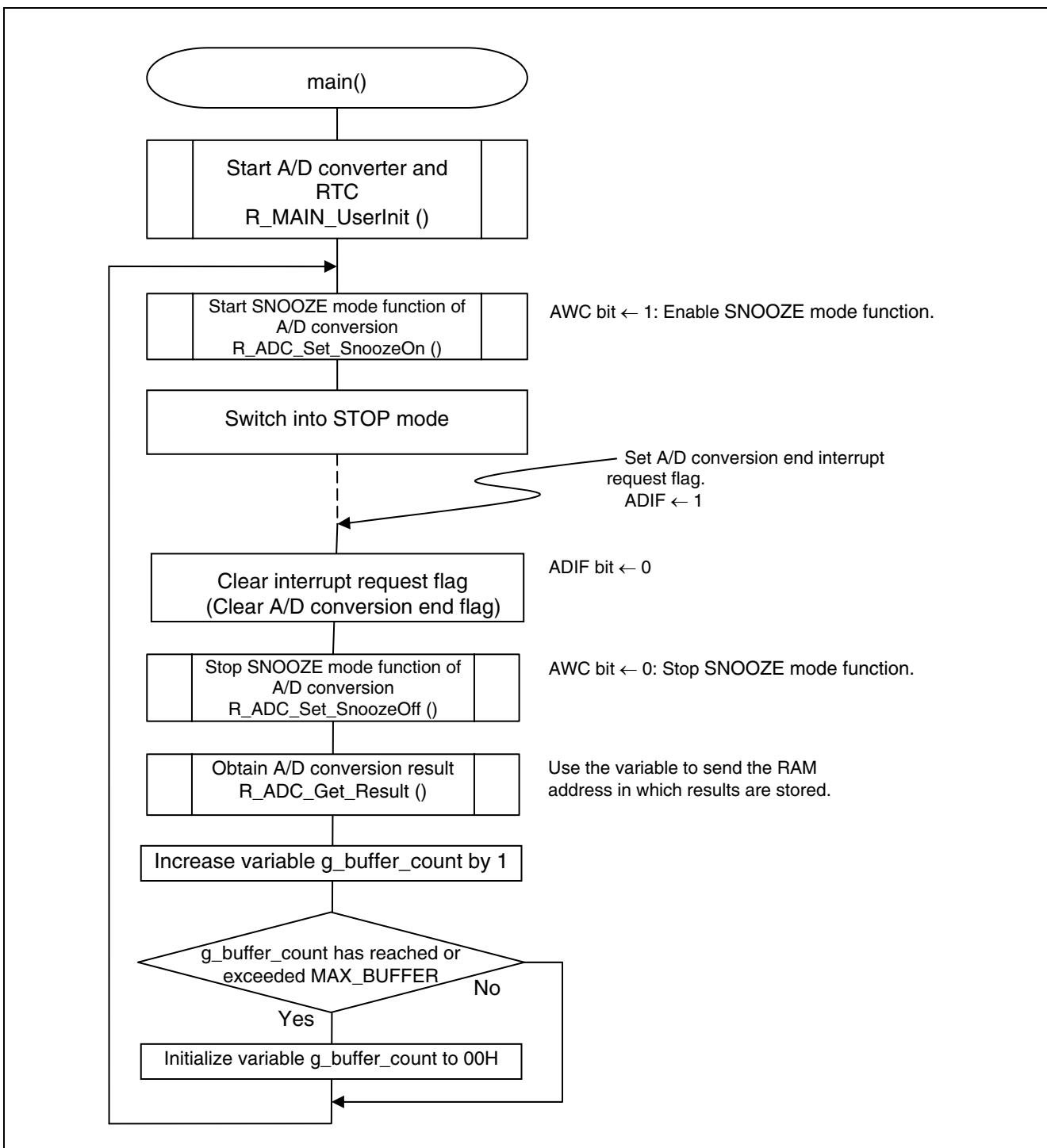
Figure 5.8   Main Processing

Setting up interrupt request flags
- Interrupt request flag register (IF1H)
  Clears the interrupt request flag.

Symbol: IF1H

7	6	5	4	3	2	1	0
TMIF04	TMIF13	SRIF3 CSIIF31 IICIF31	STIF3 CSIIF30 IICIF30	KRIF	ITIF	RTCIF	ADIF
x	x	x	x	x	x	x	**0**

Bit 0

ADIF	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Caution   For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.8 Starting A/D Converter and RTC

Figure 5.9 shows the flowcharts for starting the A/D converter and RTC.
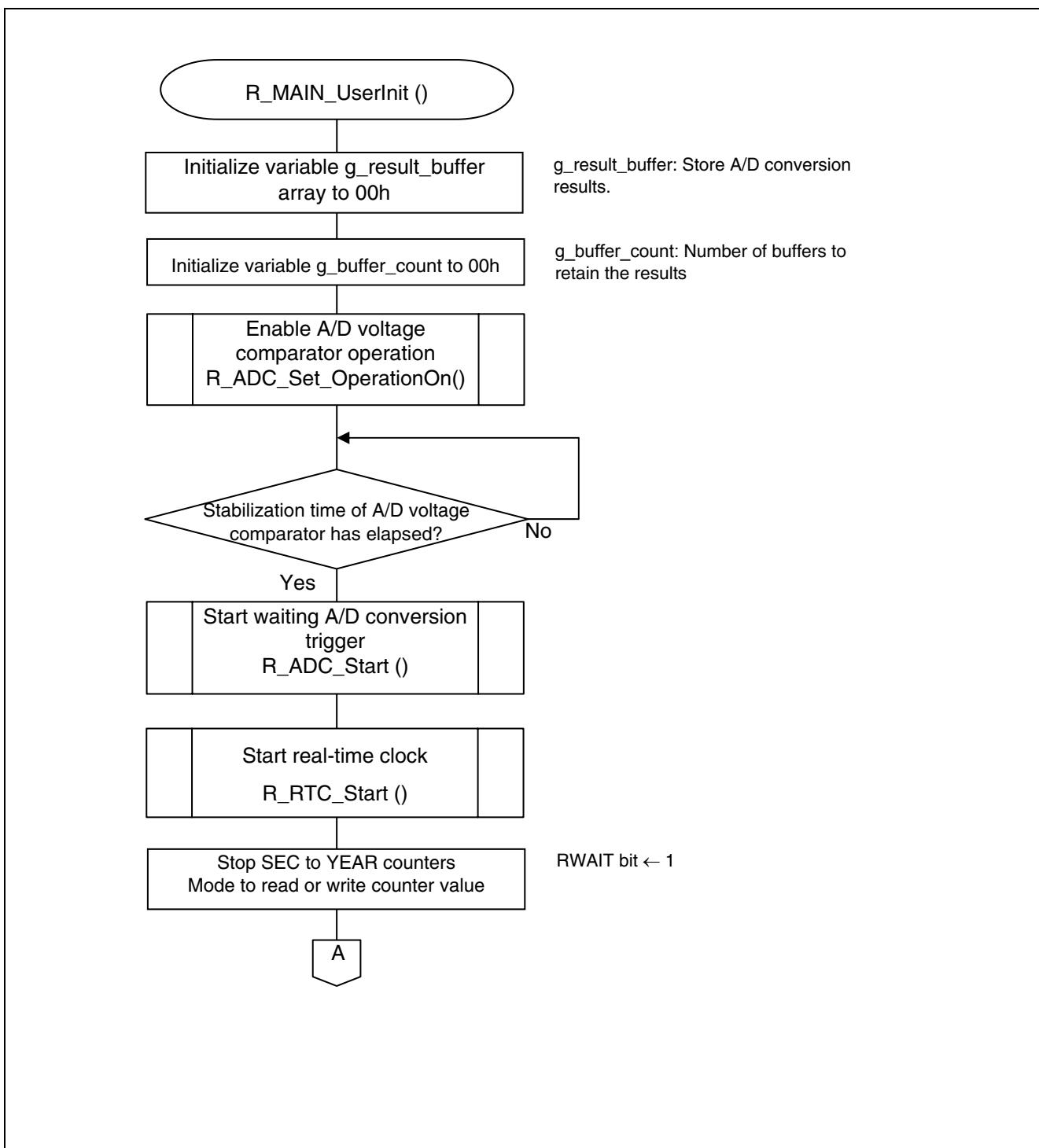
Figure 5.9   Starting A/D Converter and RTC (1/2)
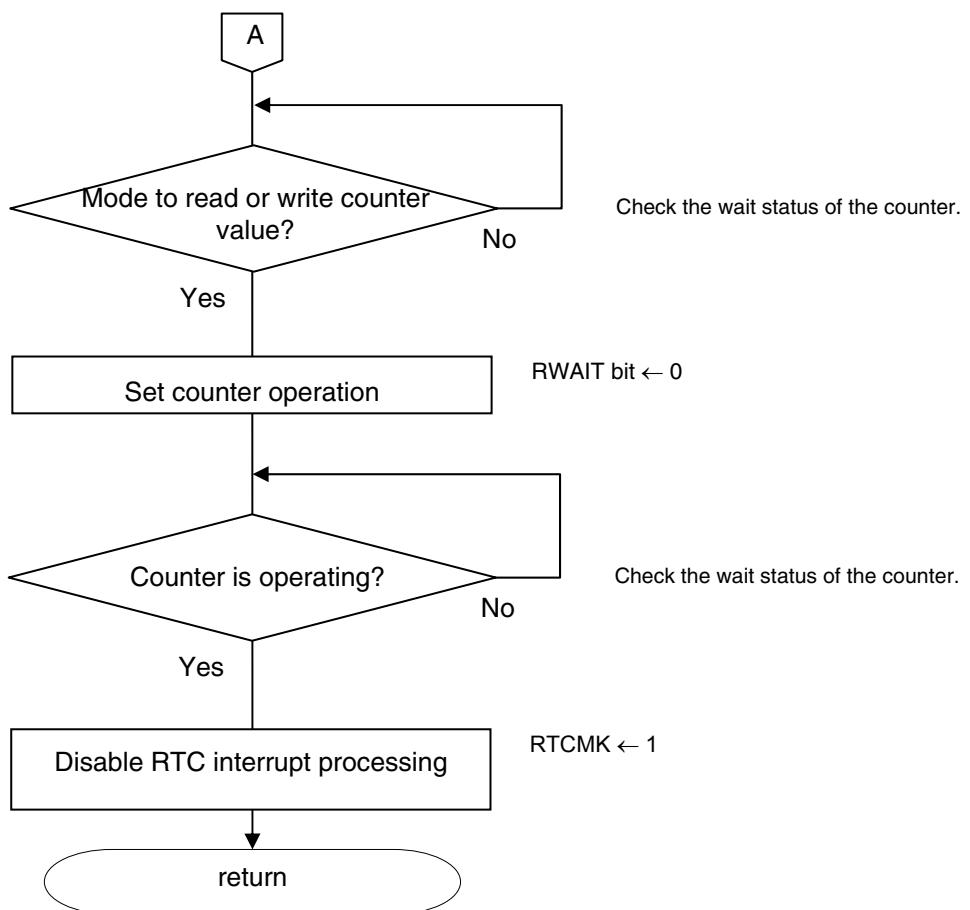
Figure 5.9   Starting A/D Converter and RTC (2/2)

Setting up real-time clock interrupts

- Interrupt mask flag register (MK1H)
  Disables interrupt servicing.

Symbol: MK1H

7	6	5	4	3	2	1	0
TMMK04	TMMK13	SRMK3 CSIMK31 IICMK31	STMK3 CSIMK30 IICMK30	KRMK	ITMK	RTCMK	ADMK
x	x	x	x	x	x	**1**	x

Bit 1

RTCMK	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

Setting up the real-time clock control register

- Real-time clock control register 1 (RTCC1)
  Performs wait control.

Symbol: RTCC1

7	6	5	4	3	2	1	0
WALE	WALIE	0	WAFG	RIFG	0	RWST	RWAIT
x	x	0	x	x	0	x	**0/1**

Bit 0

RWAIT	Wait control of real-time clock
0	**Sets counter operation.**
1	**Stops SEC to YEAR counters. Mode to read or write counter value**

Caution   For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.9   Enabling A/D Voltage Comparator

Figure 5.10 shows the flowchart for enabling the A/D voltage comparator.
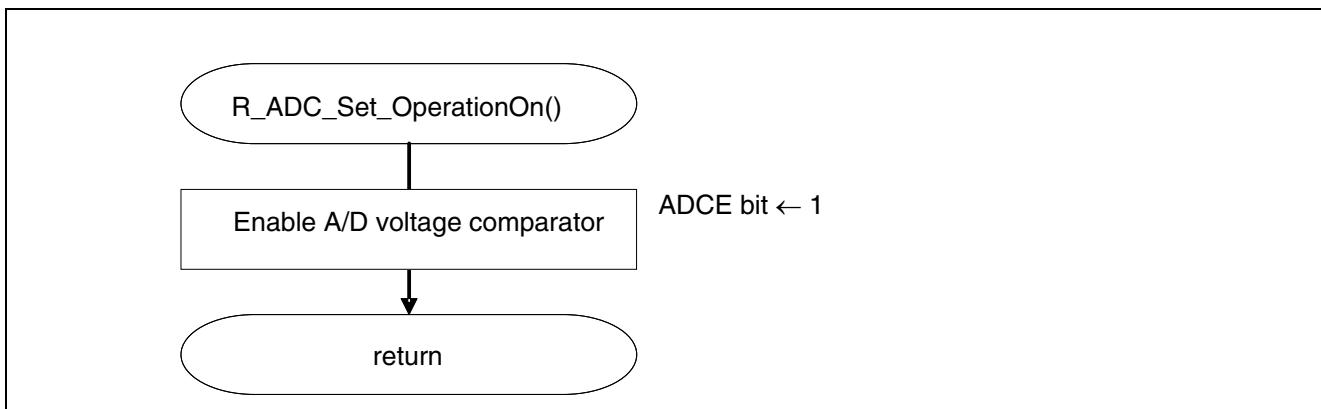
Figure 5.10   Enabling A/D Voltage Comparator

Starting the A/D voltage comparator

- A/D converter mode register 0 (ADM0)
  Controls the A/D voltage comparator operation.

Symbol: ADM0

7	6	5	4	3	2	1	0
ADCS	ADMD	FR2	FR1	FR0	LV1	LV0	ADCE
x	x	x	x	x	x	x	**1**

Bit 0

ADCE	A/D voltage comparator operation control
0	Stops A/D voltage comparator operation
1	**Enables A/D voltage comparator operation**

Caution   For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.10   Starting to Wait A/D Conversion Trigger

Figure 5.11 shows the flowchart for starting to wait an A/D conversion trigger.
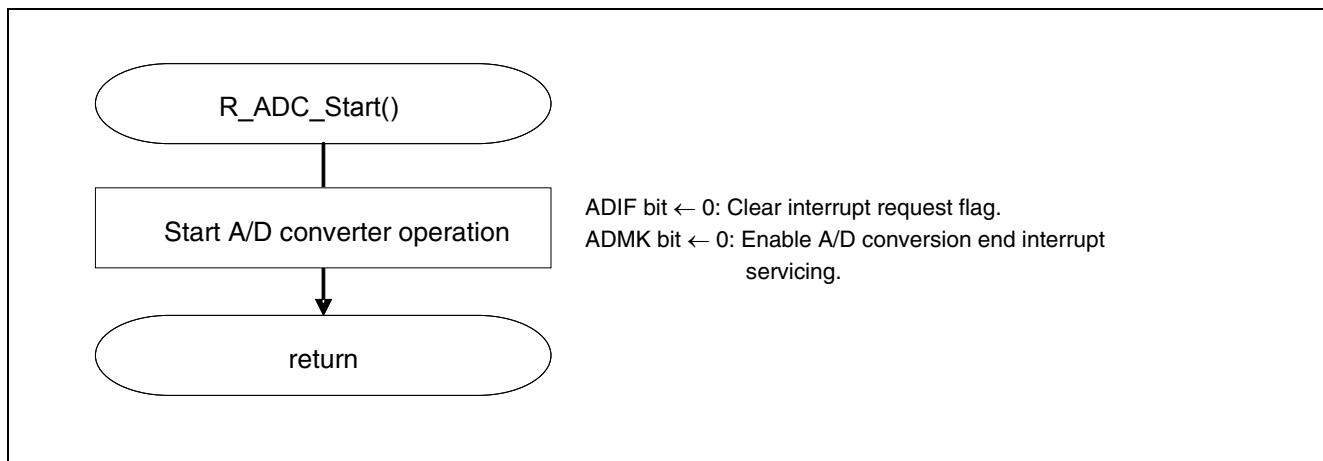
Figure 5.11   Starting to Wait A/D Conversion Trigger

Setting up A/D conversion end interrupts

- Interrupt request flag register (IF1H)
  Clears the interrupt request flag.
- Interrupt mask flag register (MK1H)
  Enables interrupt servicing.

Symbol: IF1H

7	6	5	4	3	2	1	0
TMIF04	TMIF13	SRIF3 CSIIF31 IICIF31	STIF3 CSIIF30 IICIF30	KRIF	ITIF	RTCIF	ADIF
x	x	x	x	x	x	x	**0**

Bit 0

ADIF	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Symbol: MK1H

7	6	5	4	3	2	1	0
TMMK04	TMMK13	SRMK3 CSIMK31 IICMK31	STMK3 CSIMK30 IICMK30	KRMK	ITMK	RTCMK	ADMK
x	x	x	x	x	x	x	**0**

Bit 0

ADMK	Interrupt servicing control
0	**Interrupt servicing enabled**
1	Interrupt servicing disabled

Caution   For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.11 Starting Real-Time Clock

Figure 5.12 shows the flowchart for starting the real-time clock.
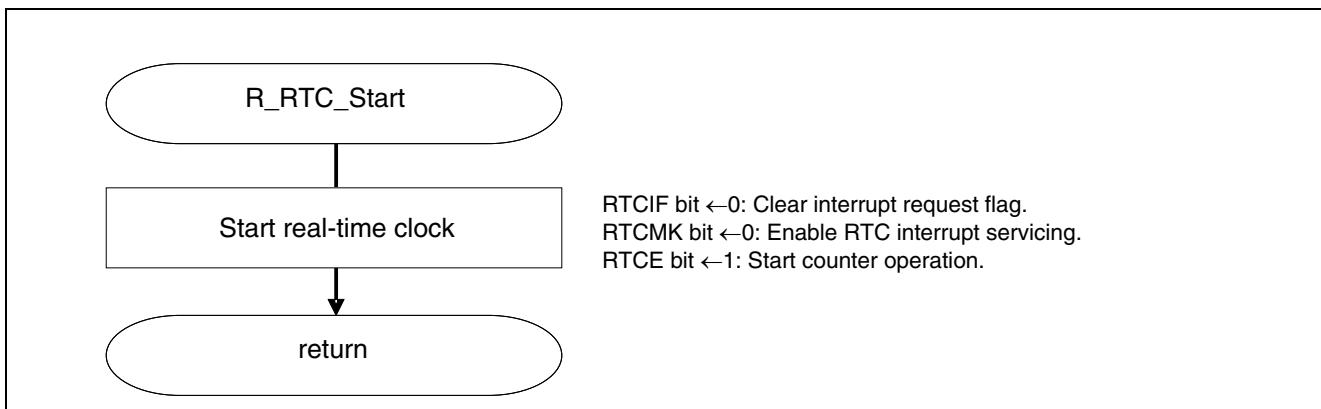
Figure 5.12   Starting Real-Time Clock

Setting up real-time clock interrupts

- Interrupt request flag register (IF1H)
  Clears the interrupt request flag.
- Interrupt mask flag register (MK1H)
  Enables interrupt servicing.

Symbol: IF1H

7	6	5	4	3	2	1	0
TMIF04	TMIF13	SRIF3 CSIIF31 IICIF31	STIF3 CSIIF30 IICIF30	KRIF	ITIF	RTCIF	ADIF
x	x	x	x	x	x	**0**	x

Bit 1

RTCIF	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Symbol: MK1H

7	6	5	4	3	2	1	0
TMMK04	TMMK13	SRMK3 CSIMK31 IICMK31	STMK3 CSIMK30 IICMK30	KRMK	ITMK	RTCMK	ADMK
x	x	x	x	x	x	**0**	x

Bit 1

RTCMK	Interrupt servicing control
0	**Interrupt servicing enabled**
1	Interrupt servicing disabled

Setting up the real-time clock operation

- Real-time clock control register 0 (RTCC0)
  Starts the counter operation of the real-time clock.

Symbol: RTCC0

7	6	5	4	3	2	1	0
RTCE	0	RCLOE1	0	AMPM	CT2	CT1	CT0
1	x	x	x	x	x	x	x

Bit 7

RTCE	Real-time clock operation control
0	Stops counter operation.
1	**Starts counter operation.**

Caution   For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.12   Starting SNOOZE Mode Function of A/D Conversion

Figure 5.13 shows the flowchart for starting the SNOOZE mode function of A/D conversion.

AWC bit ← 1: Enable the SNOOZE mode function.
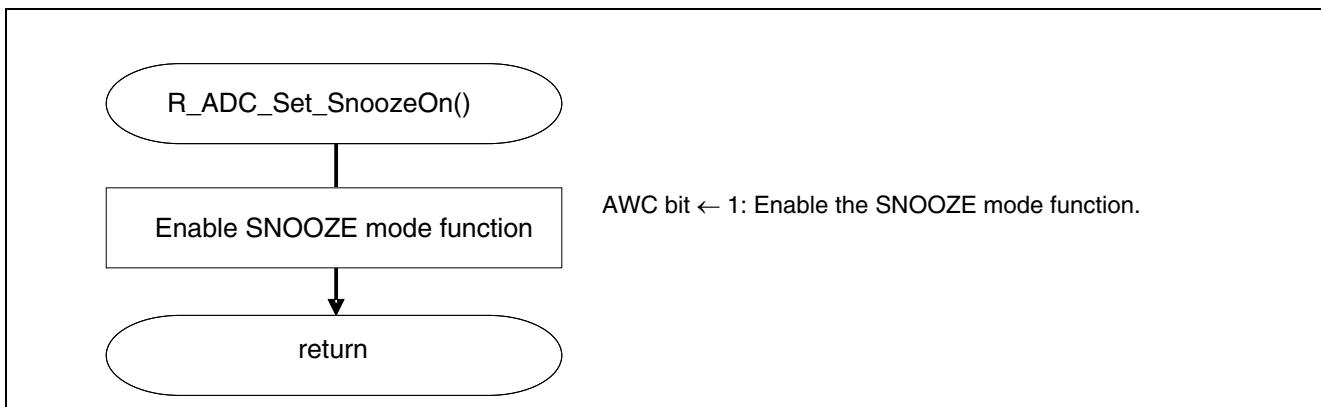
Figure 5.13   Starting SNOOZE Mode Function of A/D Conversion

Specifying the SNOOZE mode

- A/D converter mode register 2 (ADM2)
  Specifies the SNOOZE mode.

Symbol: ADM2

7	6	5	4	3	2	1	0
ADREFP1	ADREFP0	ADREFM	0	ADRCK	AWC	0	ADYTP
x	x	x	x	x	**1**	x	x

Bit 2

AWC	Specification of the SNOOZE mode
0	Do not use the SNOOZE mode function.
1	**Use the SNOOZE mode function.**

Caution   For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.13   Stopping SNOOZE Mode Function of A/D Conversion

Figure 5.14 shows the flowchart for stopping the SNOOZE mode function of A/D conversion.
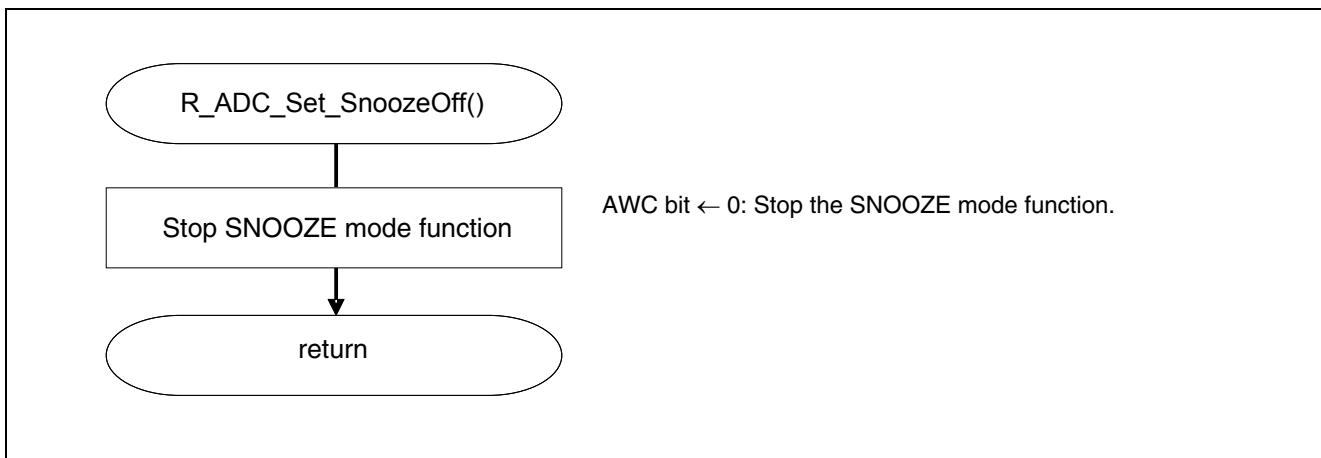
Figure 5.14   Stopping SNOOZE Mode Function of A/D Conversion

Specifying the SNOOZE mode

- A/D converter mode register 2 (ADM2)
  Specifies the SNOOZE mode.

Symbol: ADM2

7	6	5	4	3	2	1	0
ADREFP1	ADREFP0	ADREFM	0	ADRCK	AWC	0	ADYTP
x	x	x	x	x	**0**	x	x

Bit 2

AWC	Specification of the SNOOZE mode
0	**Do not use the SNOOZE mode function.**
1	Use the SNOOZE mode function.

Caution   For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.14 Obtaining A/D Conversion Results

Figure 5.15 shows the flowchart for obtaining A/D conversion results.
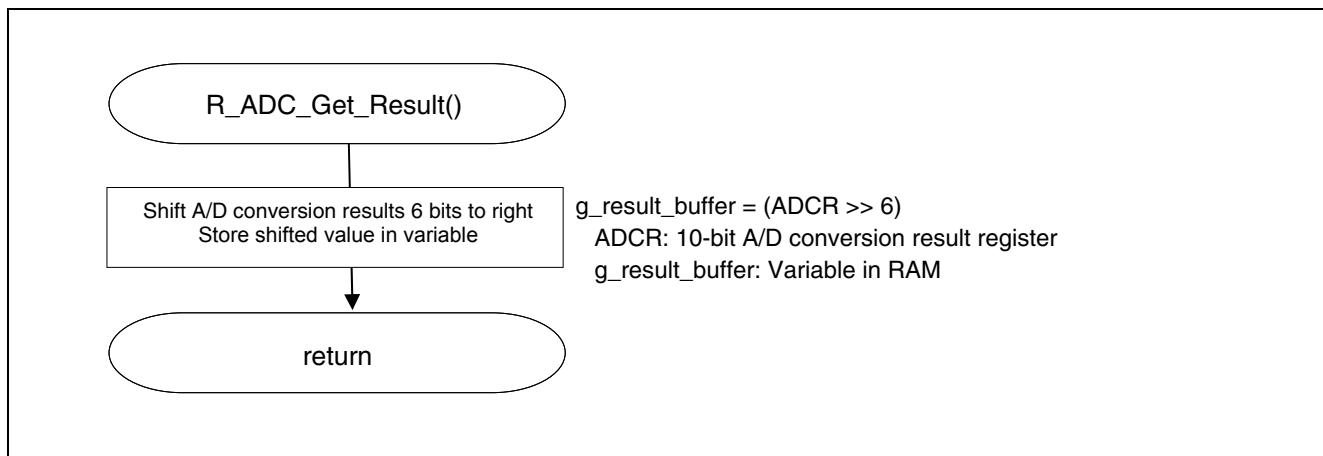
Figure 5.15   Obtaining A/D Conversion Results

6.   Sample Code

The sample code is available on the Renesas Electronics Website.

7.   Documents for Reference

RL78/G13 User's Manual: Hardware (R01UH0146E)

RL78 Family User's Manual: Software (R01US0015E)

 (The latest versions of the documents are available on the Renesas Electronics Website.)

Technical Updates/Technical Brochures

 (The latest versions of the documents are available on the Renesas Electronics Website.)

Website and Support

Renesas Electronics Website

- http://www.renesas.com/index.jsp

Inquiries

- http://www.renesas.com/contact/

Revision Record	RL78/G13 A/D Converter (SNOOZE Mode)

Rev.	Date	Description	
		Page	Summary
1.00	Sep 10, 2013	—	First edition issued

All trademarks and registered trademarks are the property of their respective owners.

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different type number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

RENESAS

Renesas Electronics Corporation

http://www.renesas.com