RL78/G10

Security Alarm Using Shock Sensor

R01AN4058EJ0100
Rev.1.00
Nov 30, 2017

Introduction

This application note describes how to implement the security alarm using a shock sensor and a buzzer.

Target Device

RL78/G10

When applying the sample program covered in this application note to another microcontroller, modify the program according to the specifications of the microcontroller and conduct an extensive evaluation of the modified program.

Contents

1. Specifications

When the power is turned on, the system causes the LED to blink for 10 seconds (in 50-ms period), and then to go off, and enters standby mode. If the shock sensor detects any vibration, the system causes the LED to blink (in 500-ms period) and sound the buzzer simultaneously. After 20 seconds after buzzer, the system turns off the LED, and enters standby mode again.
Figure 1.1 shows the outline of the system configuration.

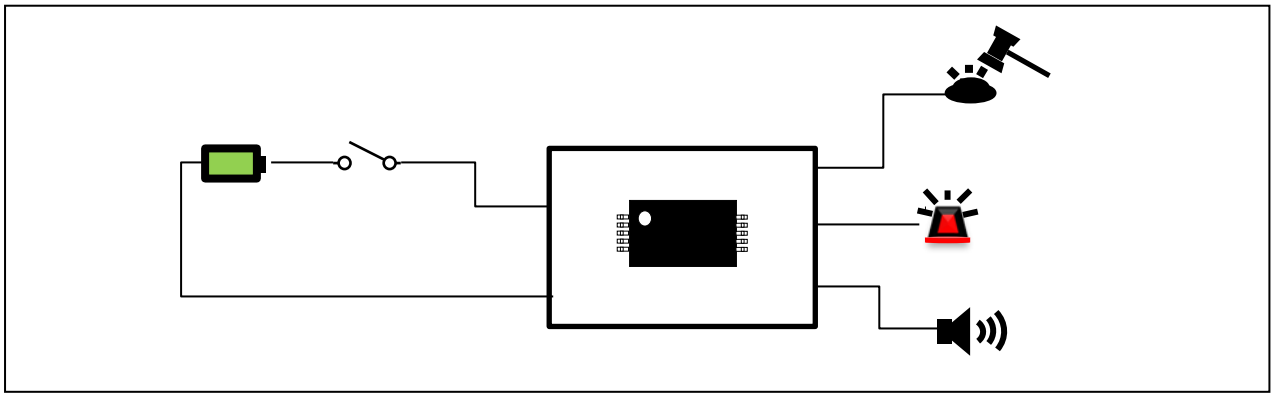

Figure 1.1 the system configuration

1.1 Shock Sensor

The sample program covered in this application note uses the shock sensor, which outputs the impulse voltage. The shock sensor outputs the voltage in proportion to the impulse value. If an excessive shock is applied to the shock sensor, the shock sensor may apply an excessive voltage to the microcontroller, which may ruin the microcontroller. When actually preparing the circuit, the circuit should be designed so that the electrical characteristics are satisfied.

2. Operation Check Conditions

The sample code contained in this application note has been checked under the conditions listed in the table below.

Table 2.1 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G10 (R5F10Y16ASP)
Operating frequency	• High-speed on-chip oscillator (HOCO) clock: 5 MHz • CPU/peripheral hardware clock: 5 MHz
Operating voltage	4.5 V (can run on a voltage range of 2.7 V to 5.5 V.) SPOR operation: 2.16 V at fall, 2.11 V at rise
Integrated development environment (CS+)	CS+ for CC V5.00.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.04.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V5.1.0.022 from Renesas Electronics Corp.
C compiler (e^2 studio)	CC-RL V1.04.00 from Renesas Electronics Corp.

3. Related Application Note

The application note that is related to this application note is listed below for reference.

RL78/G10 Initialization (R01AN2668E) Application Note

4. Hardware Descriptions

4.1 Hardware Configuration

Figure 4.1 shows an example of the hardware configuration used for this application.

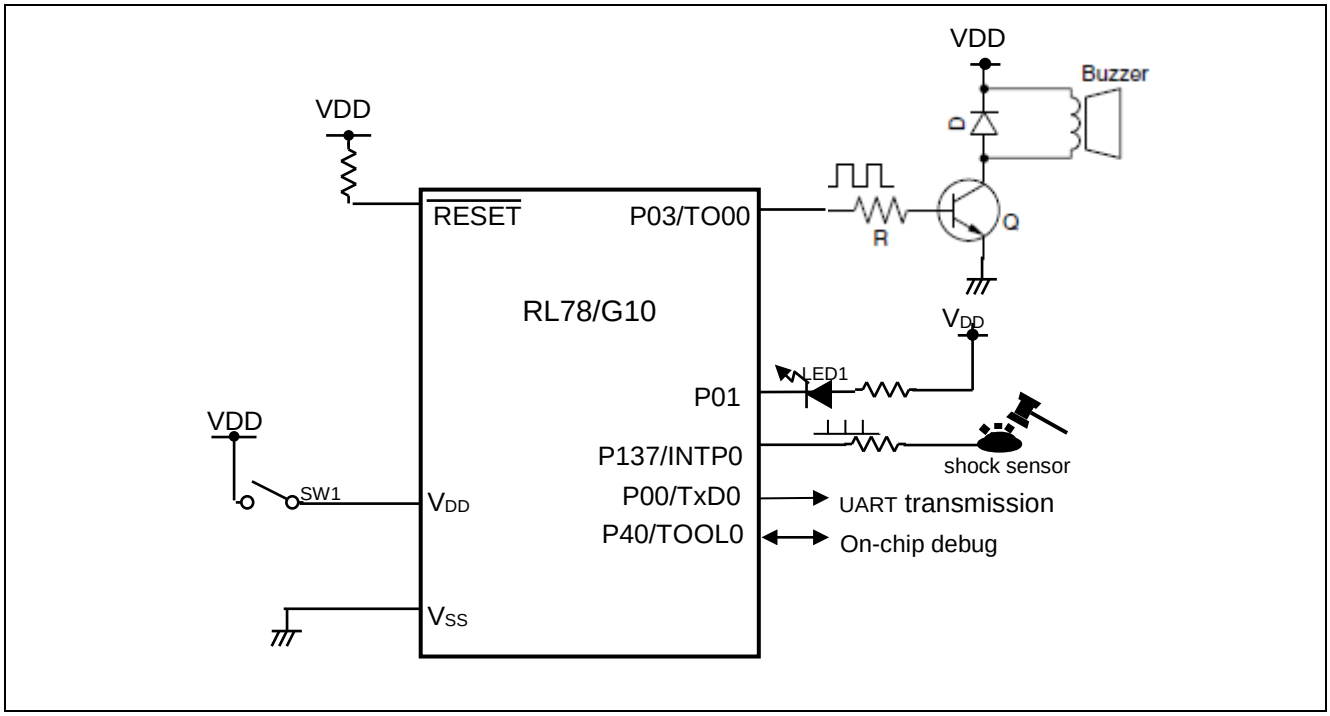

Figure 4.1 the hardware configuration used for this application

Notes: 1. The above figure is a simplified circuit image for showing the outline of the connections. The actual circuit should be designed so that the pins are handled appropriately and that the electrical characteristics are satisfied (input-only ports should be each connected to V_{DD} or V_{SS} via a resistor).

2. VDD must be equal to or greater than the reset release voltage (V_{SPOR}) specified with SPOR.

4.2 List of Pins Used

Table 4.1 lists the pins used and their functions.

Table 4.1 Pins Used and Their Functions

Pin Name	I/O	Description
P00/TxD0	Output	UART transmission port
P01	Output	LED control port
P03/TO00	Output	Buzzer drive port
P137/INTP0	Input	Shock sensor input port
P40/TOOL0	I/O	For on-chip debugging
P125/RESET	Input	Reset port

5. Software Descriptions

5.1 Operation Summary

With the sample program covered in this application note, the timer array unit channel 0 is used to control the LED blinking period. The lower 8-bit timer of the timer array unit channel 1 is also used to provide the square waveform having a 50% duty cycle for the buzzer output. In addition, serial array unit 0 is used to perform UART communication (transmission).

5.2 List of Option Byte Settings

Table 5.1 shows the option byte settings.

Table 5.1 Option Byte Settings

Address	Setting	Description
000C0H	11101111B	Disables the watchdog timer. (Stops counting after the release from the reset state.)
000C1H	11111111B	SPOR detection voltage: 2.16 V at fall; 2.11 V at rise
000C2H	11111011B	HOCO: 5 MHz
000C3H	10000101B	Enables the on-chip debugger.

5.3 List of Variables

Table 5.2 lists the global variables.

Table 5.2 Global Variables

Type	Variable Name	Contents	Function Used
unsigned short	g_1ms_Blink	LED blinking flag	main()
unsigned short	g_flag_Intp	External interrupt flag	main()
unsigned char	g_date_Fre[]	Buzzer frequency	main()
unsigned short	g_flag_Buzzer	Buzzer flag	R_TAU0_Buzzer()

5.4 List of Functions (Subroutines)

Table 5.3 lists the functions (subroutines).

Table 5.3 List of Functions (Subroutines)

Function (Subroutine) Name	Outline
R_TAU0_Ch0Start	Starts count operation of the timer array unit channel 0.
R_TAU0_Ch0Stop	Stops count operation of the timer array unit channel 0.
R_TAU0_Ch1Low8bitStart	Starts count operation of the lower 8-bit timer of the timer array unit channel 1.
R_TAU0_Ch1Low8bitStop	Stops count operation of the lower 8-bit timer of the timer array unit channel 1.
R_TAU0_Buzzer	Outputs the timer array unit channel 0 to buzzer.
R_INTC0_Start	Enables interrupts.
R_INTC0_Stop	Disables interrupts.
R_UART0_Start	Starts UART transmission.
R_UART0_Stop	Stops UART transmission.

5.5 Function Specifications

This section gives the specifications of the functions used in the sample program.

[Function Name] R_TAU0_Ch0Start		
Synopsis	Starting count operation of the timer array unit channel 0.	
Header	r_cg_tau.h	
Declaration	void R_TAU0_Ch0Start(void)	
Explanation	Starts count operation of the timer array unit channel 0.	
Arguments	None	
Return value	None	
Remarks	None	

[Function Name] R_TAU0_Ch0Stop		
Synopsis	Stopping count operation of the timer array unit channel 0.	
Header	r_cg_tau.h	
Declaration	void R_TAU0_Ch0Stop(void)	
Explanation	Stops count operation of the timer array unit channel 0.	
Arguments	None	
Return value	None	
Remarks	None	

[Function Name] R_TAU0_Ch1Low8bitStart		
Synopsis	Starting count operation of the lower 8-bit timer of the timer array unit channel 1	
Header	r_cg_tau.h	
Declaration	void R_TAU0_Ch1Low8bitStart(void)	
Explanation	Starts count operation of the lower 8-bit timer of the timer array unit channel 1.	
Arguments	None	
Return value	None	
Remarks	None	

[Function Name] R_TAU0_Ch1Low8bitStop		
Synopsis	Stopping count operation of the lower 8-bit timer of the timer array unit channel 1	
Header	r_cg_tau.h	
Declaration	void R_TAU0_Ch1Low8bitStop(void)	
Explanation	Stops count operation of the lower 8-bit timer of the timer array unit channel 1.	
Arguments	None	
Return value	None	
Remarks	None	

[Function Name] R_TAU0_Buzzer		
Synopsis	Outputting the timer array unit channel 0 to buzzer	
Declaration	r_cg_tau.h	
Explanation	Outputs the timer array unit channel 0 to buzzer.	
Arguments	None	
Return value	None	
Remarks	None	

[Function Name] R_INTC0_Start		
Synopsis	Enabling external interrupts.	
Header	r_cg_intp.h	
Declaration	void R_INTC0_Start(void)	
Explanation	Starts external interrupts.	
Arguments	None	
Return value	None	
Remarks	None	

[Function Name] R_INTC0_Stop		
Synopsis	Disabling external interrupts.	
Header	r_cg_intp.h	
Declaration	void R_INTC0_Stop(void)	
Explanation	Disables external interrupts.	
Arguments	None	
Return value	None	
Remarks	None	

[Function Name] R_UART0_Start		
Synopsis	Starting UART transmission	
Header	r_cg_sau.h	
Declaration	void R_UART0_Start(void)	
Explanation	Starts UART transmission.	
Arguments	None	
Return value	None	
Remarks	None	

[Function Name] R_UART0_Stop		
Synopsis	Stopping UART transmission	
Header	r_cg_sau.h	
Declaration	void R_UART0_Stop(void)	
Explanation	Stops UART transmission.	
Arguments	None	
Return value	None	
Remarks	None	

[Function Name] main		
Synopsis	Main function	
Declaration	—	
Explanation	main processing function of the sample program	
Arguments	None	
Return value	None	
Remarks	None	

5.6 Flowcharts

Figure 5.1 shows an overall flow of the sample program described in this application note.

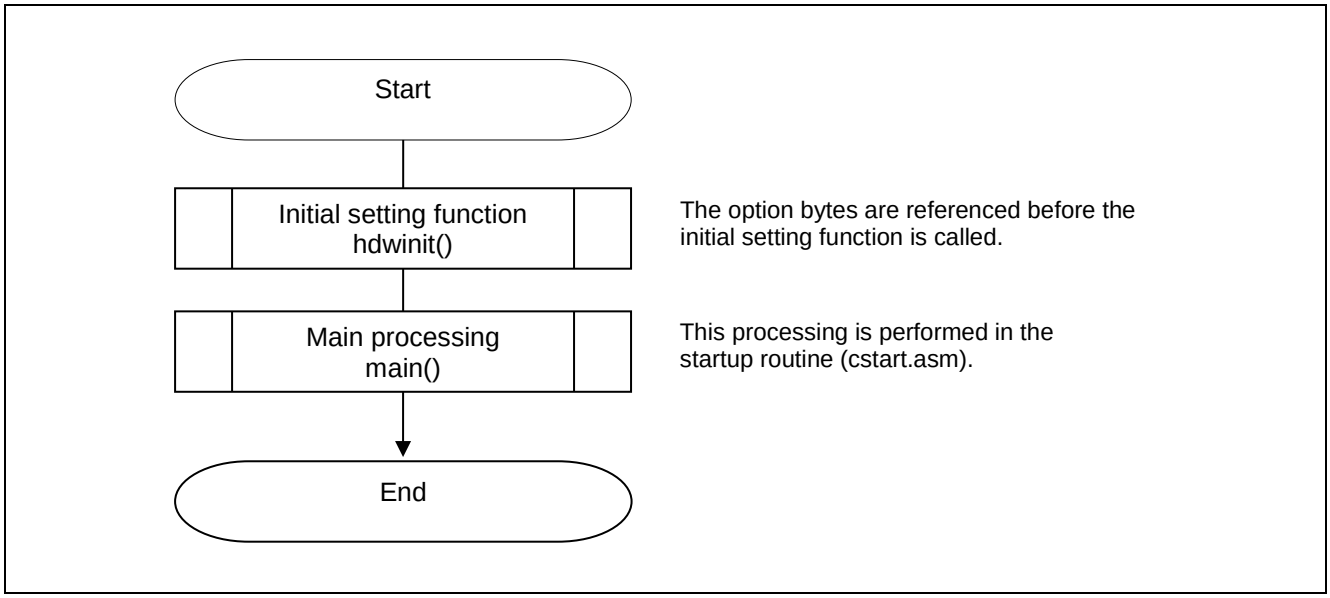

Figure 5.1 the **hardware configuration used for this application**

Note: The main processing is performed in the startup routine (cstart.asm etc.). Memory-related settings are made between the initial setting function and calling of the main processing function.

5.6.1 Initial Setting Function

Figure 5.2 shows the flowchart of the initial setting function.

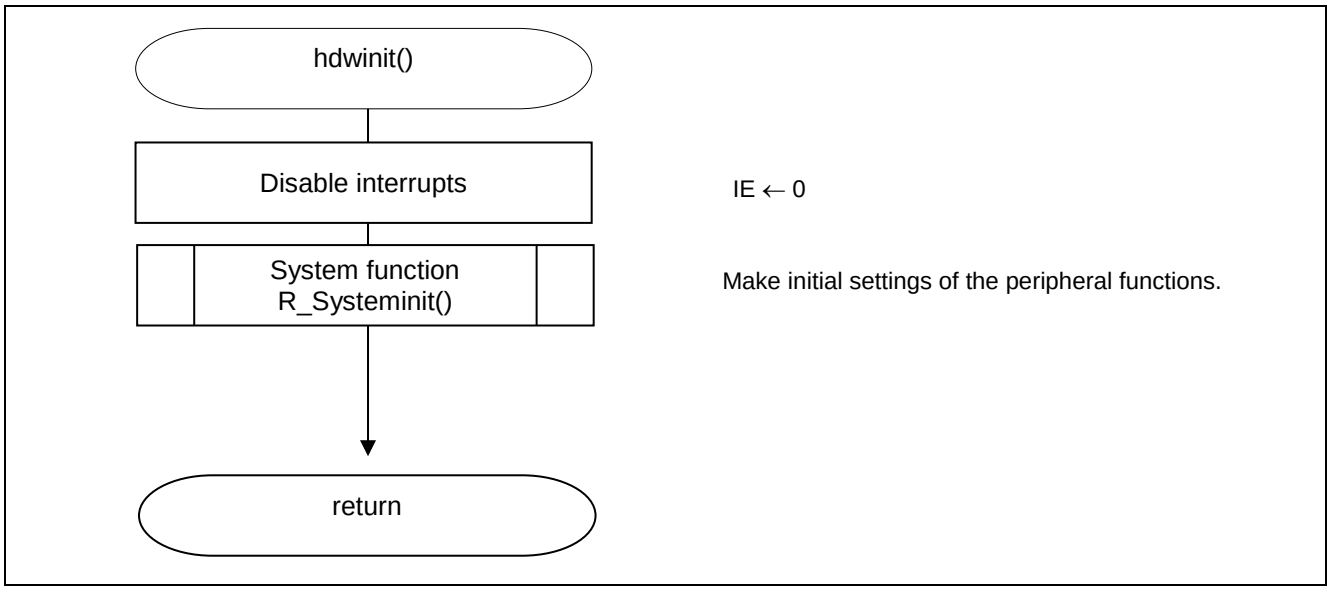

Figure 5.2 Initial Setting Function

5.6.2 System Function

Figure 5.3 shows the flowchart of the system function.

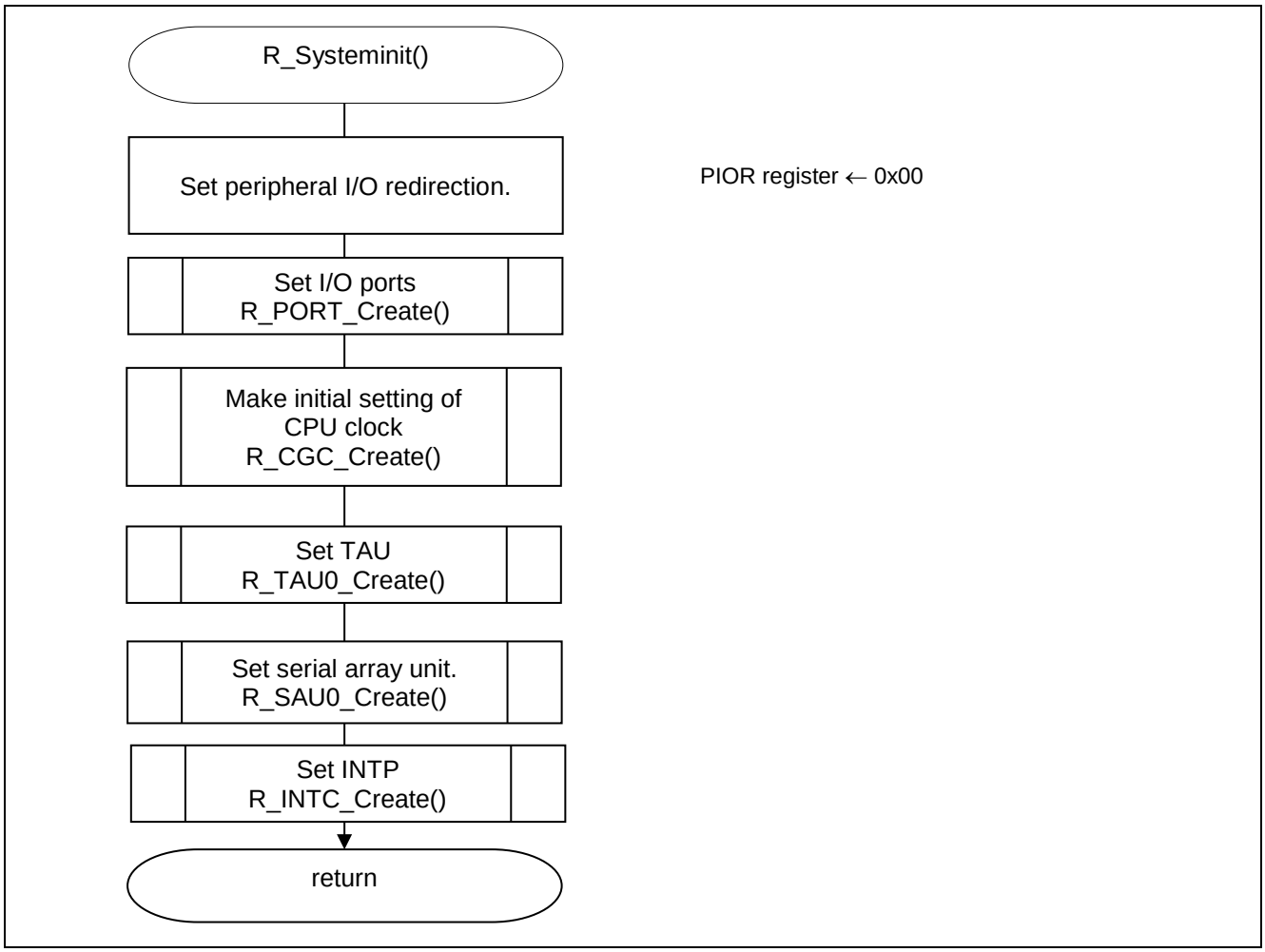

Figure 5.3 System Function

5.6.3 I/O Port Setup

Figure 5.4 shows the flowchart for setting up the I/O ports.

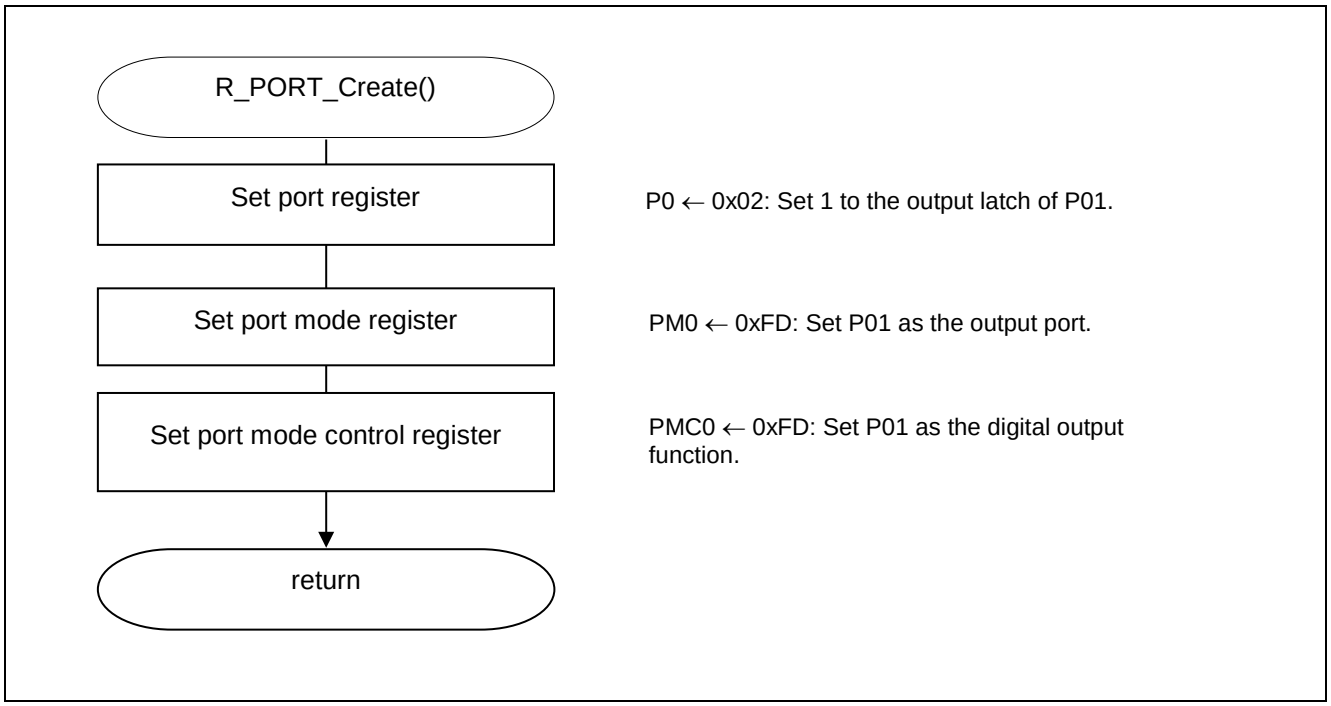

Figure 5.4 I/O Port Setup

Notes: 1. For details on register setting when using the ports as the alternate functions of the peripheral functions, refer to the RL78/G10 User's Manual: Hardware.

2. Provide proper treatment for unused pins so that their electrical specifications are observed. Connect each of unused input-only ports to V_{DD} or V_{SS} via a separate resistor.

5.6.4 CPU Clock Setup

Figure 5.5 shows the flowchart for setting up the CPU clock.

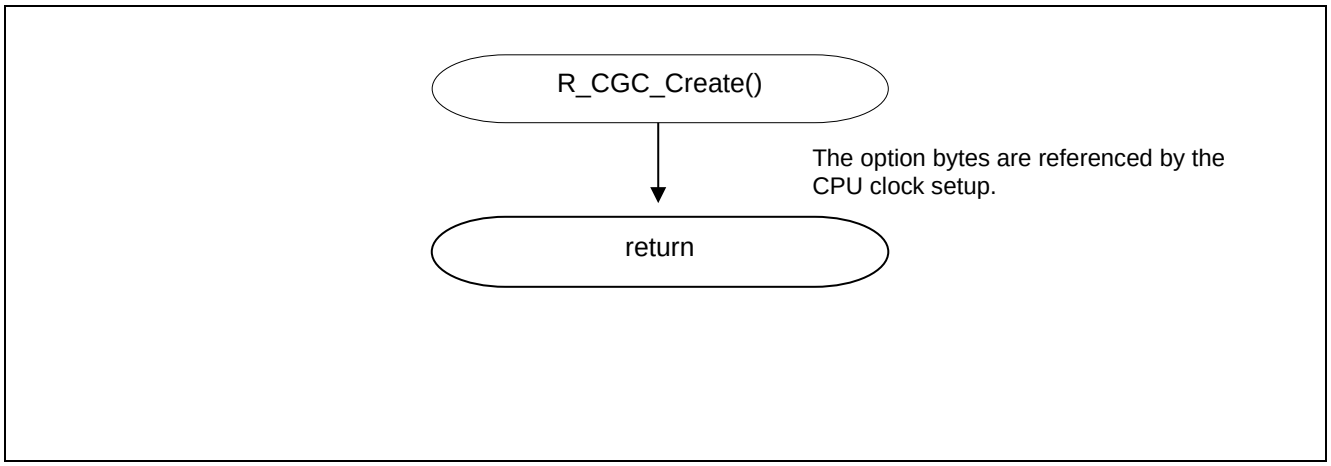

Figure 5.5 CPU Clock Setup

5.6.5 Timer Array Unit Setup

Figure 5.6 shows the flowchart for setting up the timer array unit.

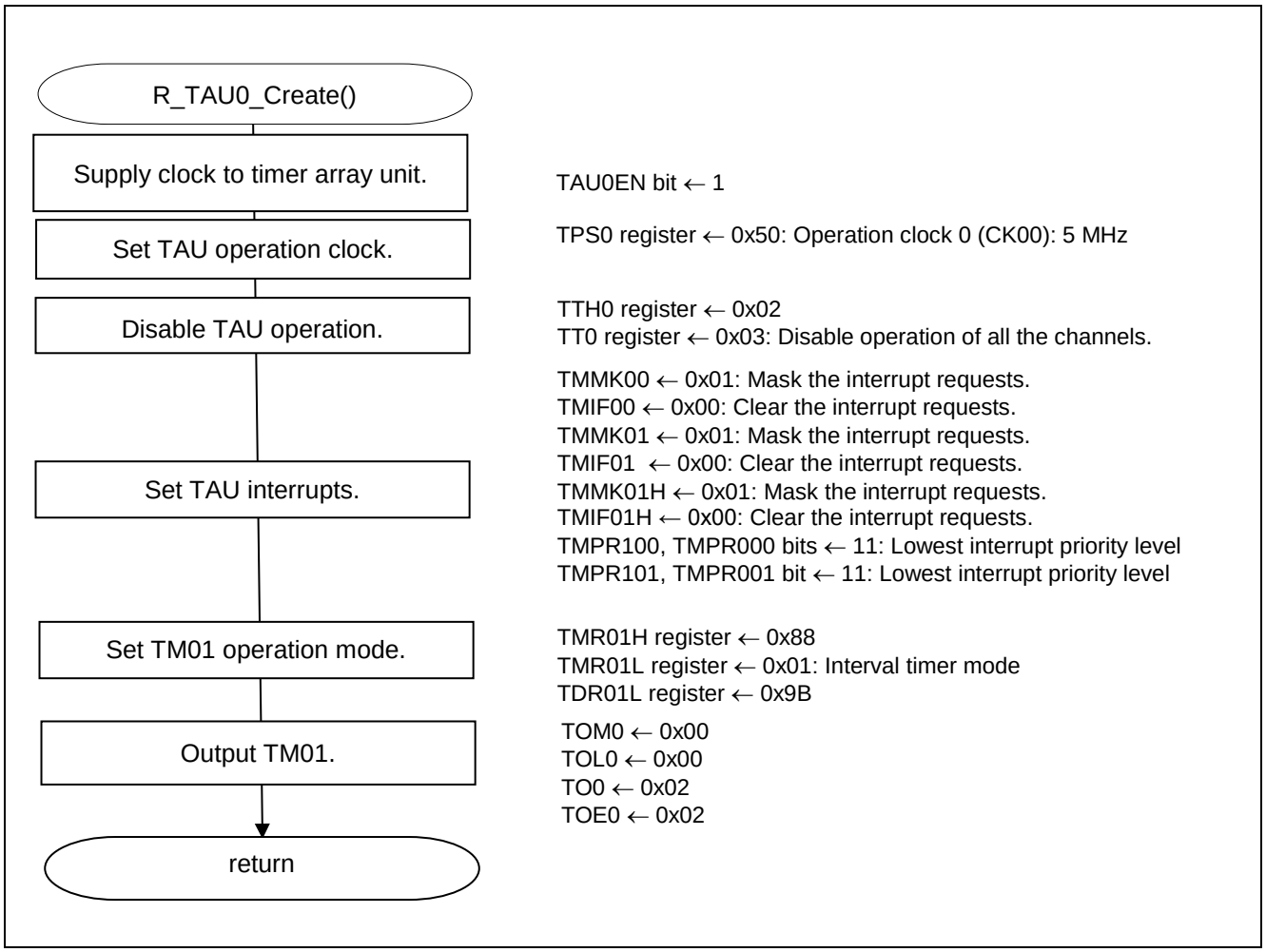

Figure 5.6 Timer Array Unit Channel1 Setup

Starting clock supply to the timer array unit 0

Peripheral enable register 0 (PER0)

Start supplying clock to the timer array unit 0.

Symbol: PER0

7	6	5	4	3	2	1	0
TMKAEN[Note]	CMPEN[Note]	ADCEN	IICA0EN[Note]	0	SAU0EN	0	TAU0EN
0	0	x	0	0	x	0	**1**

bit 0

TAU0EN	Control of timer array unit 0 input clock supply
0	Stops supply of input clock.
1	**Supplies input clock.**

Note: 16-pin products only.

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Stop timer channel

Timer channel stop register 0 (TT0, TTH0(8-bit mode))

Select timer channel to stop operation.

Symbol：TTH0、TT0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	TTH03	0	TTH01	0	0	0	0	0	TT03	TT02	TT01	TT00
0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	**1**	**1**

bit n

TT0n	Operation stop trigger of channel n (n=0 to 3)
0	No trigger operation
1	**TE0n is cleared to 0, and counting operation is stopped**

Configuring the timer clock frequency

Timer clock select register 0 (TPS0)

Select an operation clock for timer array unit 0.

Symbol: TPS0

7	6	5	4	3	2	1	0
PRS013	PRS012	PRS011	PRS010	PRS003	PRS002	PRS001	PRS000
0	**1**	**0**	**1**	**0**	**0**	**0**	**0**

Bits 3 to 0

PRS 003	PRS 002	PRS 001	PRS 000		Selection of operation clock (CK00)				
					f_{CLK}= 1.25MHz	f_{CLK}= 2.5MHz	f_{CLK}= 5MHz	f_{CLK}= 10MHz	**f_{CLK}= 20MHz**
0	**0**	**0**	**0**	**f_{CLK}**	1.25 MHz	2.5 MHz	5 MHz	10 MHz	**20 MHz**
0	0	0	1	$f_{CLK}/2$	625 kHz	1.25 MHz	2.5 MHz	5 MHz	10 MHz
0	0	1	0	$f_{CLK}/2^2$	313 kHz	625 kHz	1.25 MHz	2.5 MHz	5 MHz
0	0	1	1	$f_{CLK}/2^3$	156 kHz	313 kHz	625 kHz	1.25 MHz	2.5 MHz
0	1	0	0	$f_{CLK}/2^4$	78 kHz	156 kHz	313 kHz	625 kHz	1.25 MHz
0	**1**	**0**	**1**	$f_{CLK}/2^5$	39 kHz	78 kHz	**156 kHz**	313 kHz	625 kHz
0	1	1	0	$f_{CLK}/2^6$	19.5 kHz	39 kHz	78 kHz	156 kHz	313 kHz
0	1	1	1	$f_{CLK}/2^7$	9.8 kHz	19.5 kHz	39 kHz	78 kHz	156 kHz
1	0	0	0	$f_{CLK}/2^8$	4.9 kHz	9.8 kHz	19.5 kHz	39 kHz	78 kHz
1	0	0	1	$f_{CLK}/2^9$	2.5 kHz	4.9 kHz	9.8 kHz	19.5 kHz	39 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.22 kHz	2.5 kHz	4.9 kHz	9.8 kHz	19.5 kHz
1	0	1	1	$f_{CLK}/2^{11}$	625 Hz	1.22 kHz	2.5 kHz	4.9 kHz	9.8 kHz
1	1	0	0	$f_{CLK}/2^{12}$	313 Hz	625 Hz	1.22 kHz	2.5 kHz	4.9 kHz
1	1	0	1	$f_{CLK}/2^{13}$	152 Hz	313 Hz	625 Hz	1.22 kHz	2.5 kHz
1	1	1	0	$f_{CLK}/2^{14}$	78 Hz	152 Hz	313 Hz	625 Hz	1.22 kHz
1	1	1	1	$f_{CLK}/2^{15}$	39 Hz	78 Hz	152 Hz	313 Hz	625 Hz

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Timer interrupt

- Interrupt mask flag registers（MK0L）
  Interrupt mask selection
- Interrupt request flag registers（IF0L）
  clear interrupt request
- Priority specification flag registers（PR00L、PR10L）
  low priority selection

Symbol：MK0L

bit 7,6

××MK××	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

Symbol：IF0L

bit 7,6

××IF××	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Symbol：PR00L、PR10L

bit 7

TMPR100	TMPR000	Priority Level Selection
0	0	Specifying level 0(high priority)
0	1	Specifying level 1
1	0	Specifying level 2
1	**1**	**Specifying level 3(low priority)**

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Setting up the operation mode of channel 0,1

Timer mode register 01 (TMR01H, TMR01L)
Select an operation clock (fMCK).
Select a count clock.
Set up the start trigger and capture trigger
Select the valid edge of TI00 pin.
Set up the operation mode.

Symbol：TMR01H、TMR01L

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 0n1	0	0	CCS 0n	SPLIT 0n	STS 0n2	STS 0n1	STS 0n0	CIS 0n1	CIS 0n0	0	0	MD 0n3	MD 0n2	MD 0n1	MD 0n0
1	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	0	0	**0**	**0**	**0**	**1**

CKS0n1	CKS000	Selection of operation clock (f_{MCK}) of channel 0
0	0	Operation clock CK00 set by timer clock select register 0 (TPS0)
1	0	Operation clock CK01 set by timer clock select register 0 (TPS0)

CCS0n	Selection of count clock (f_{TCLK}) of channel 0
0	Operation clock (f_{MCK}) specified by the CKS000 and CKS001 bits
1	Valid edge of the input signal from the TI00 pin

SPLIT0n	Selection of count clock (f_{TCLK}) of channel 0
0	16bit timer operation
1	8bit timer operation

STS002	STS001	STS000	Setting of start trigger or capture trigger of channel 0
0	0	0	Only software trigger start is valid (other trigger sources are unselected).
0	0	1	Valid edge of the TI00 pin input is used as both the start trigger and capture trigger.
0	1	0	Both the edges of the TI00 pin input are used as a start trigger and capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Bit 7-6

CIS 001	CIS 000	Selection of TI00 pin input valid edge
0	0	Falling edge
0	1	Rising edge
1	0	Both edges (when low-level width is measured)
1	1	Both edges (when high-level width is measured)

Bit 3-0

MD 003	MD 002	MD 001	MD 000	Operation mode of channel 0	Corresponding function	Counting operation of TCR
0	0	0	1/0	Interval timer mode	Interval timer/Square wave output/Divider function /PWM output (master)	Counting down
0	1	0	1/0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	0	Event counter mode	External event counter	Counting down
1	0	0	1/0	One-count mode	Delay counter/One-shot pulse output/PWM output (slave)	Counting down
1	1	0	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above				Setting prohibited		

Operation mode (Value set by the MD003 to MD001 bits) (See the above table)	MD000	Setting of starting count and interrupt
• Interval timer mode (0, 0, 0) • Capture mode (0, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
	1	Timer interrupt is generated when counting is started (timer output also changes).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
	1	Start trigger is valid during counting operation. At that time, interrupt is also generated.
• Capture/one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
Other than above		Setting prohibited

Setting the interval timer cycle time

Timer data register 01 (TDR01H, TDR01L)
Setting delay time

Symbol：TDR01H、TDR01L

TDR01H								TDR01L							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
×	×	×	×	×	×	×	×	**1**	**0**	**0**	**1**	**1**	**0**	**1**	**1**

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Enabling the timer output

timer putout register 0 (TO0)
setting putout 0
Timer output enable register 0 (TOE0)
Enable/disable the timer output for each channel.

Symbol：TO0

7	6	5	4	3	2	1	0
0	0	0	0	TO03	TO02	TO01	TO00
0	0	0	0	**0**	**0**	1	**0**

bit 1

TO01	**Timer output of channel n**
0	Timer output value is “0”
1	**Timer output value is “1”**

Symbol：TOE0

7	6	5	4	3	2	1	0
0	0	0	0	TOE03	TOE02	TOE01	TOE00
0	0	0	0	0	0	1	**0**

bit 1

TOE01	**Timer output enable/disable of channel 0**
0	**Disables the timer output.** **Timer operation is not reflected in the TO00 bit, and the output is fixed.** **Writing to the TO00 bit is allowed.**
1	**Enables the timer output.** **Timer operation is reflected in the TO00 bit, and output waveform is generated.** **Writing to the TO00 bit is ignored.**

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

5.6.6 Timer Array Unit Channel 0 Setup

Figure 5.7 shows the flowchart for setting up the timer array unit.

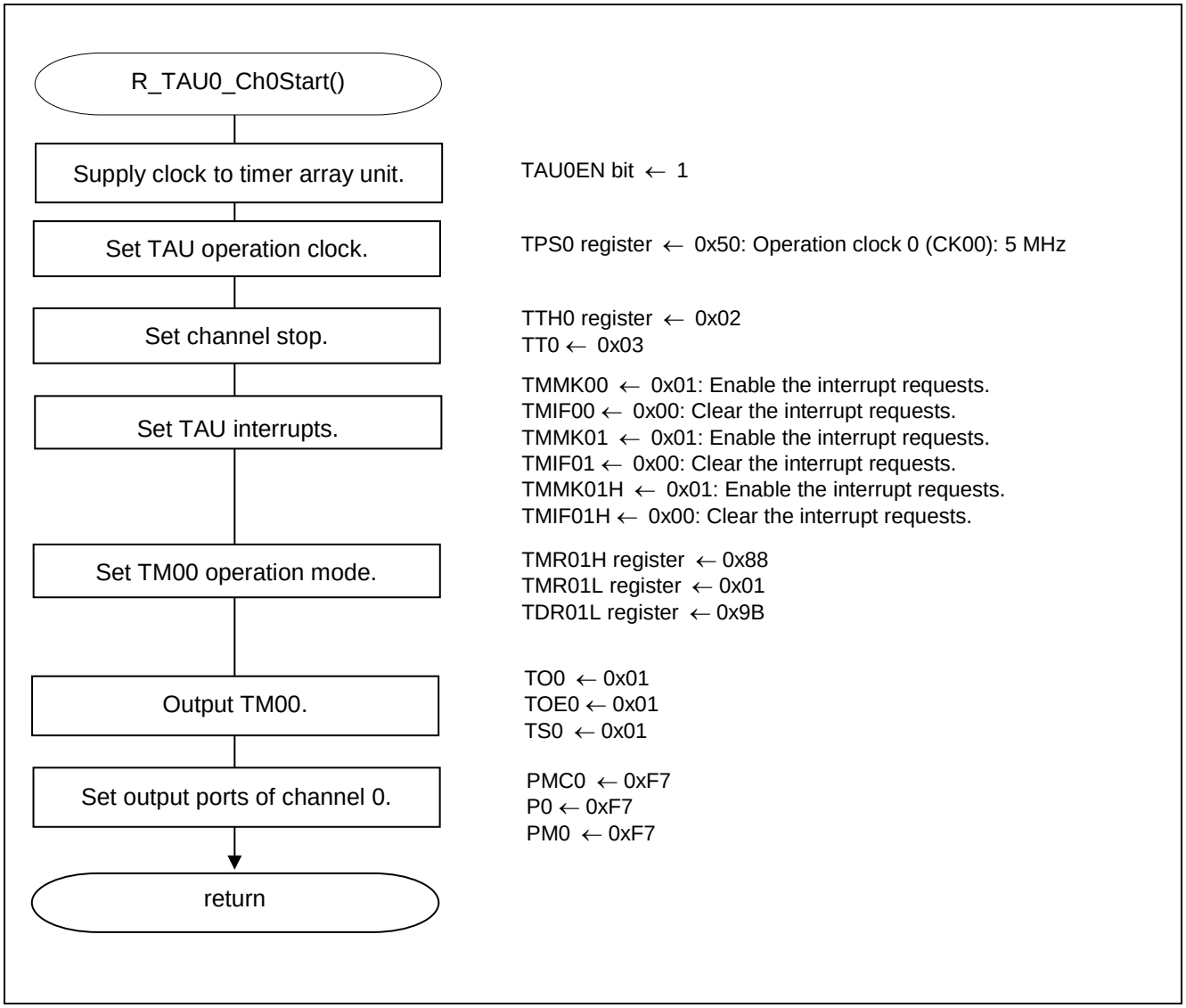

Figure 5.7 Timer Array Unit Channel1 Setup

5.6.7 Serial Array Unit Setup

Figure 5.8 shows the flowchart for setting up the serial array unit.

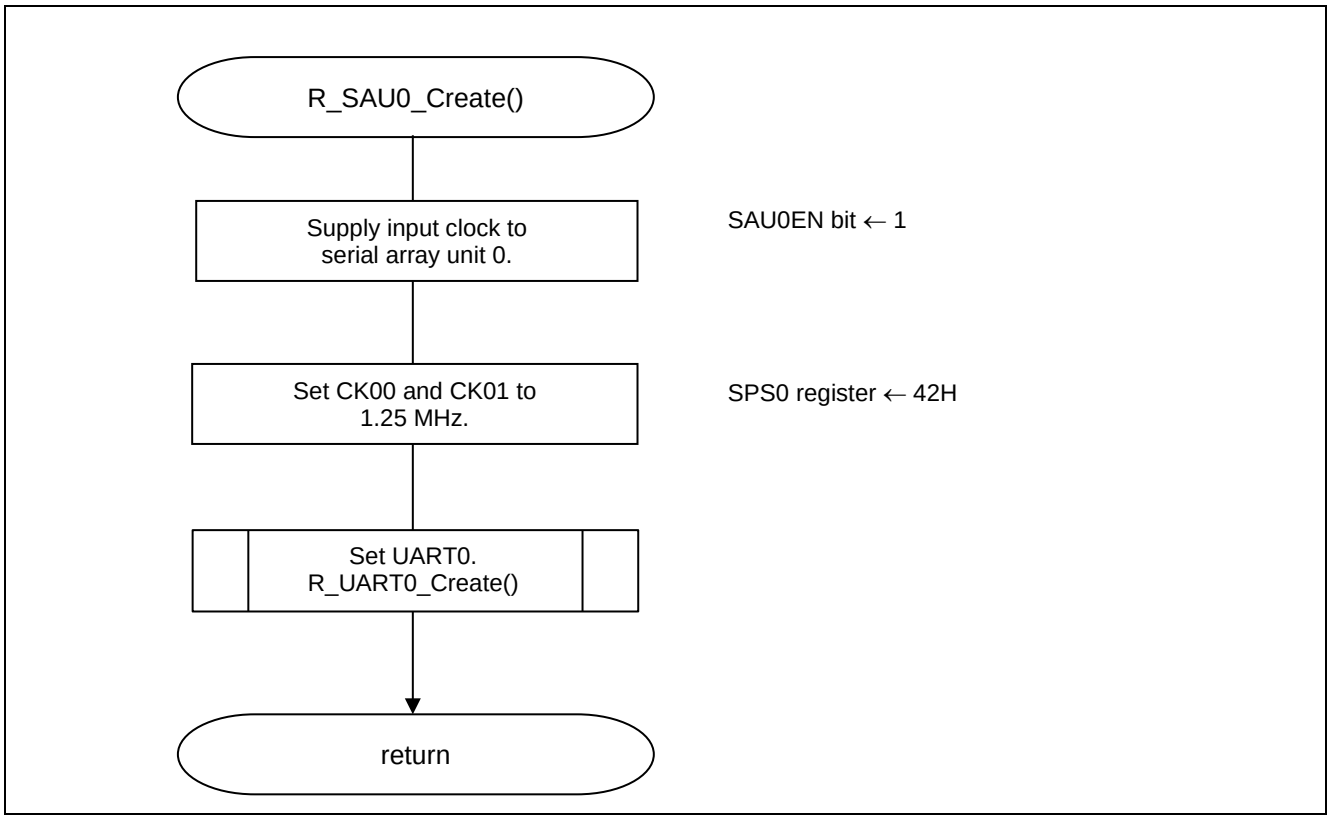

Figure 5.8 Serial Array Unit Setup

Start supplying clock to the SAU

Peripheral enable register 0 (PER0)
Clock supply

Symbol: PER0

7	6	5	4	3	2	1	0
TMKAE Note	0	ADCEN	IICA0EN Note	SAU1EN	SAU0EN	0	TAU0EN
x	0	x	x	x	**1**	0	x

Bit 2

SAU0EN	Input clock control for serial array unit 0
0	Stops supply of input clock.
1	**Starts supply of input clock.**

Note 16-pin products only.

Select serial clock

Serial clock select register 0 (SPS0)
Operation clock setting

Symbol: SPS0

7	6	5	4	3	2	1	0
PRS 013	PRS 012	PRS 011	PRS 010	PRS 003	PRS 002	PRS 001	PRS 000
0	**1**	**0**	**0**	**0**	**0**	**1**	**0**

Bits 7 to 0

PRS 0n3	PRS 0n2	PRS 0n1	PRS 0n0	Operation clock (CK0n) selection (n = 0, 1)					
					f_{CLK} = 1.25 MHz	f_{CLK} = 2.5 MHz	f_{CLK} = 5 MHz	f_{CLK} = 10 MHz	f_{CLK} = 20 MHz
0	0	0	0	f_{CLK}	1.25 MHz	2.5 MHz	5 MHz	10 MHz	20 MHz
0	0	0	1	$f_{CLK}/2$	625 kHz	1.25 MHz	3.5 MHz	5 MHz	10 MHz
0	**0**	**1**	**0**	$f_{CLK}/2^2$	313 kHz	625 kHz	**1.25 MHz**	2.5 MHz	5 MHz
0	0	1	1	$f_{CLK}/2^3$	156 kHz	313 kHz	625 kHz	1.25 MHz	2.5 MHz
0	**1**	**0**	**0**	$f_{CLK}/2^4$	**78 kHz**	**156 kHz**	**313 kHz**	**625 kHz**	**1.25 MHz**
0	1	0	1	$f_{CLK}/2^5$	39 kHz	78 kHz	156 kHz	313 kHz	625 kHz
0	1	1	0	$f_{CLK}/2^6$	19.5 kHz	39 kHz	78 kHz	156 kHz	313 kHz
0	1	1	1	$f_{CLK}/2^7$	9.8 kHz	19.5 kHz	39 kHz	78 kHz	156 kHz
1	0	0	0	$f_{CLK}/2^8$	4.9 kHz	9.8 kHz	19.5 kHz	39 kHz	78 kHz
1	0	0	1	$f_{CLK}/2^9$	2.5 kHz	4.9 kHz	9.8 kHz	19.5 kHz	39 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.22 kHz	2.5 kHz	4.9 kHz	9.8 kHz	19.5 kHz
1	0	1	1	$f_{CLK}/2^{11}$	625 Hz	1.22 kHz	2.5 kHz	4.9 kHz	9.8 kHz
1	1	0	0	$f_{CLK}/2^{12}$	313 Hz	625 Hz	1.22 kHz	2.5 kHz	4.9 kHz
1	1	0	1	$f_{CLK}/2^{13}$	152 Hz	313 Hz	625 Hz	1.22 kHz	2.5 kHz
1	1	1	0	$f_{CLK}/2^{14}$	78 Hz	152 Hz	313 Hz	625 Hz	1.22 kHz
1	1	1	1	$f_{CLK}/2^{15}$	39 Hz	78 Hz	152 Hz	313 Hz	625 Hz

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

5.6.8 UART0 Setup

Figure 5.9 and figure 5.10 show the flowcharts for setting up the UART0.

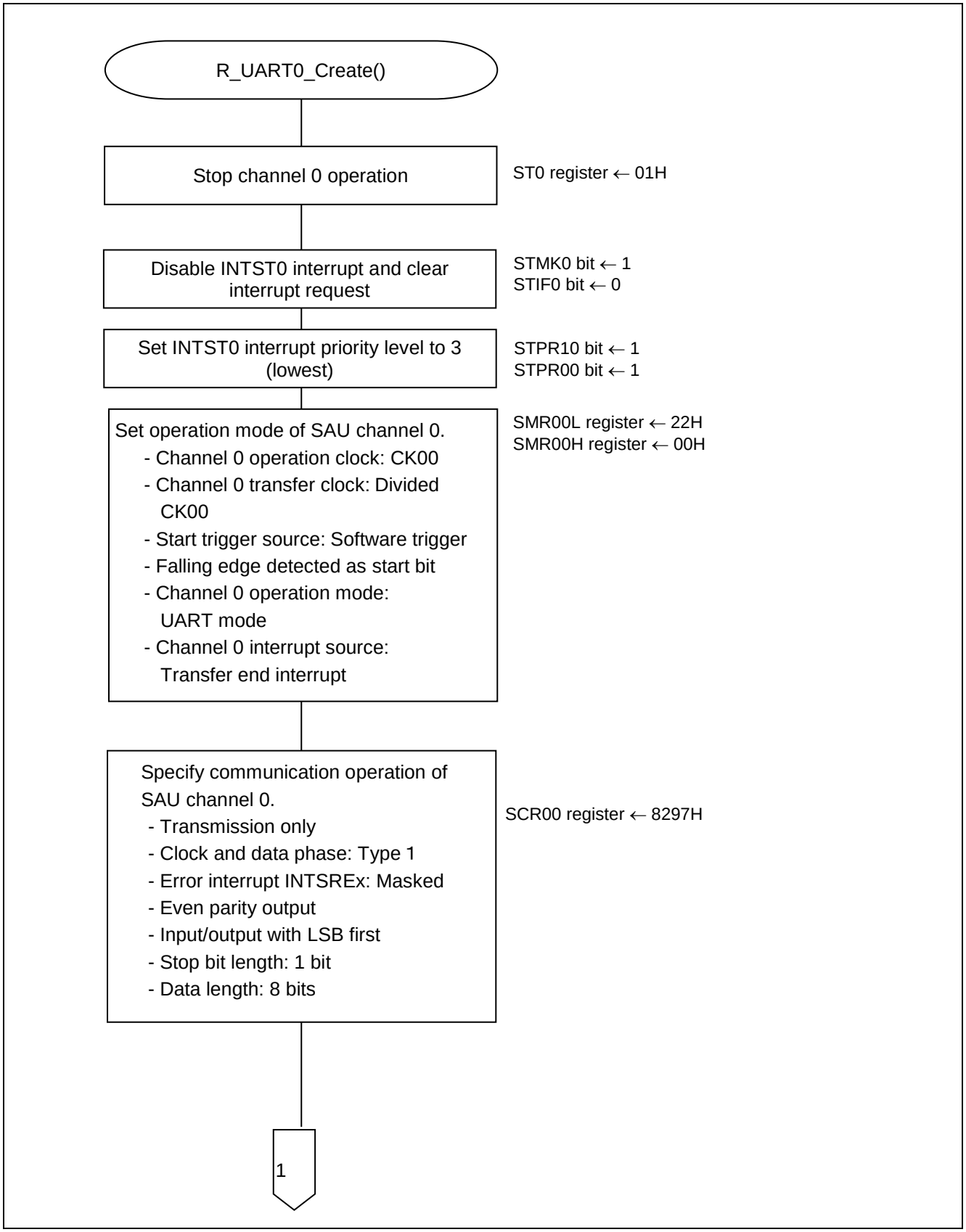

Figure 5.9 UART0 Setup (1/2)

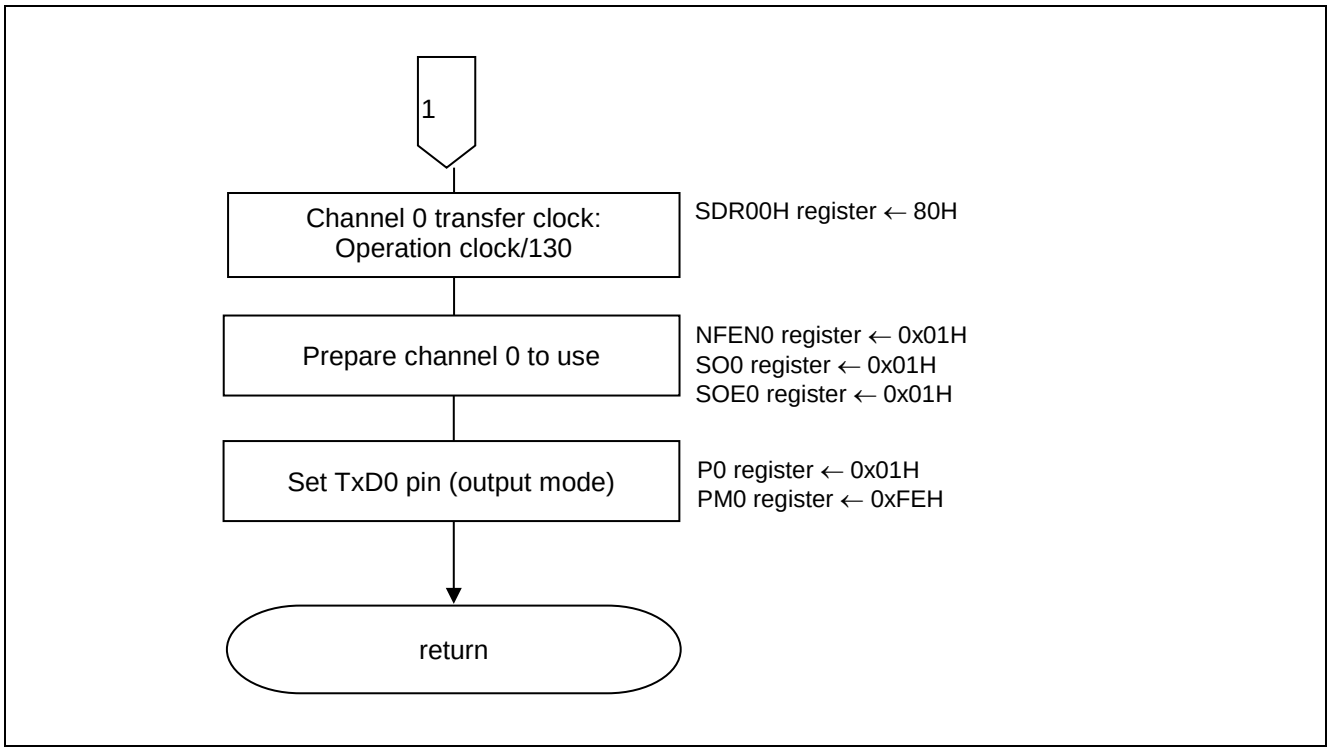

Figure 5.10 UART0 Setup (2/2)

Transmission channel operation mode setting

Serial mode register 00 (SMR00H, SMR00L)

Interrupt source

Operation mode

Transfer clock selection

f_{MCK} selection

Symbol: SMR00H, SMR00L

SMR00H SMR00L

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 00	CCS 00	0	0	0	0	0	STS 00	0	0	1	0	0	MD 002	MD 001	MD 000
0	**0**	0	0	0	0	0	**0**	0	0	1	0	0	**0**	**1**	**0**

Bit 15

CKS00	Channel 0 operation clock (f_{MCK}) selection
0	**Prescaler output clock CK00 configured by the SPS0 register**
1	Prescaler output clock CK01 configured by the SPS0 register

Bit 14

CCS00	Channel 0 transfer clock (TCLK) selection
0	**Clock obtained by dividing the operation clock f_{MCK} specified by the CKS00 bit.**
1	Clock input from the SCK pin.

Bit 8

STS00	Selection of start trigger factor
0	**Only the software trigger is valid.**
1	Valid edge of the RxD pin (selected for UART reception)

Bits 2 and 1

MD002	MD001	Channel 0 operation mode setting
0	0	CSI mode
0	**1**	**UART mode**
1	0	Simplified I^2C mode
1	1	Setting prohibited

Bit 0

MD000	Channel 0 interrupt source selection
0	**Transfer end interrupt**
1	Buffer empty interrupt

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Transmission channel communication operation setting

Serial communication operation setting register 00 (SCR00H, SCR00L)
Data length setting, data transfer order, error interrupt signal mask availability, and operation mode

Symbol: SCR00H, SCR00L

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXE00	RXE00	DAP00	CKP00	0	EOC00	PTC001	PTC000	DIR00	0	SLC001	SLC000	0	1	DLS001	DLS000
1	**0**	**0**	**0**	0	**0**	**1**	**0**	**1**	0	**0**	**1**	0	1	**1**	**1**

Bit 15 and 14

TXE00	RXE00	Channel 0 operation mode setting
0	0	Communication prohibited
0	1	Reception Only
1	**0**	**Transmission only**
1	1	Both transmission and reception

Bit 10

EOC00	Error interrupt signal (INTSRE0) mask availability selection
0	**Error interrupt INTSRE0 is masked**
1	Generation of error interrupt INTSREx is enabled

Bit 9 and 8

PTC001	PTC000	Parity bit setting in UART mode	
		Transmission	Reception
0	0	No parity bit is output	Data is received without parity
0	1	0 parity is output	No parity check is made
1	**0**	**Even parity is output**	**Check is made for even parity**
1	1	Odd parity is output	Check is made for odd parity

Bit 7

DIR00	Selection of data transfer order in CSI and UART modes
0	Input and output in MSB first
1	**Input and output in LSB first**

Bit 5 and 4

SLC001	SLC000	Stop bit setting in UART mode
0	0	No stop bit
0	**1**	**Stop bit length = 1 bit**
1	0	Stop bit length = 2 bits
1	1	Setting prohibited

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Symbol: SCR00H, SCR00L

SCR00H SCR00L

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXE 00	RXE 00	DAP 00	CKP 00	0	EOC 00	PTC 001	PTC 000	DIR 00	0	SLC 001	SLC 000	0	1	DLS 001	DLS 000
1	**0**	**0**	**0**	0	**0**	**1**	**0**	**1**	0	**0**	**1**	0	1	**1**	**1**

Bit 1 and 0

DLS001	DLS000	Data length setting in CSI mode
0	1	9-bit data length
1	0	7-bit data length
1	**1**	**8-bit data length**
Others		Setting prohibited

Transmission channel transfer clock setting

Serial data register 00（SDR00h,SDR00L）
transfer clock frequency : f_{MCK}/130（≒9600Hz）

Symbol：SDR00H,SDR00L

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	**0**	**0**	**0**	**0**	**0**	**0**	0	x	x	x	x	x	x	x	x

Bit 15-9

SDR00[15:9]							period of operation clock（f_{MCK}） transfer setting
0	0	0	0	0	0	0	f_{MCK} /2
0	0	0	0	0	0	1	f_{MCK} /4
0	0	0	0	0	1	0	f_{MCK} /6
0	0	0	0	0	1	1	f_{MCK} /8
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
1	**0**	**0**	**0**	**0**	**0**	**0**	**f_{MCK} /130**
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
1	1	1	1	1	1	0	f_{MCK} /254
1	1	1	1	1	1	1	f_{MCK} /256

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

port setting

port register0（P0）
port mode register0（PM0）
setting transmission data to port

Symbol ：P0

7	6	5	4	3	2	1	0
0	0	0	P04	P03	P02	P01	P00
x	x	x	x	x	x	x	**1**

Bit 0

P00	putout data（putout mode）
0	putout 0
1	**putout 1**

Symbol：PM0

7	6	5	4	3	2	1	0
1	1	1	1	1	PM02	PM01	PM00
1	1	1	1	1	x	x	**0**

Bit 0

PM00	**input/output mode selecting of P00**
0	**output mode（output buffer on）**
1	input mode（output buffer off）

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware

5.6.9 External Interrupt Setup

Figure 5.11 shows the flowchart for setting up the external interrupts.

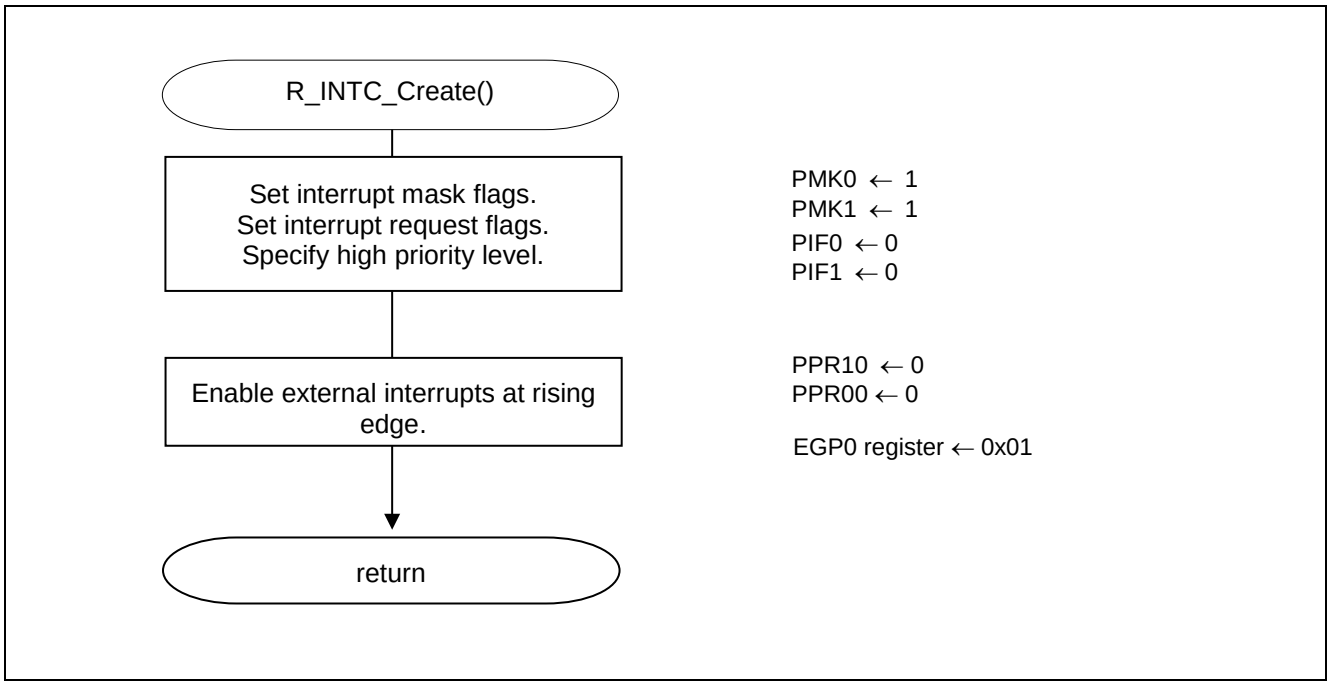

Figure 5.11 External Interrupt Setup

5.6.10 Main Processing

Figure 5.12 shows the flowchart of the main processing.

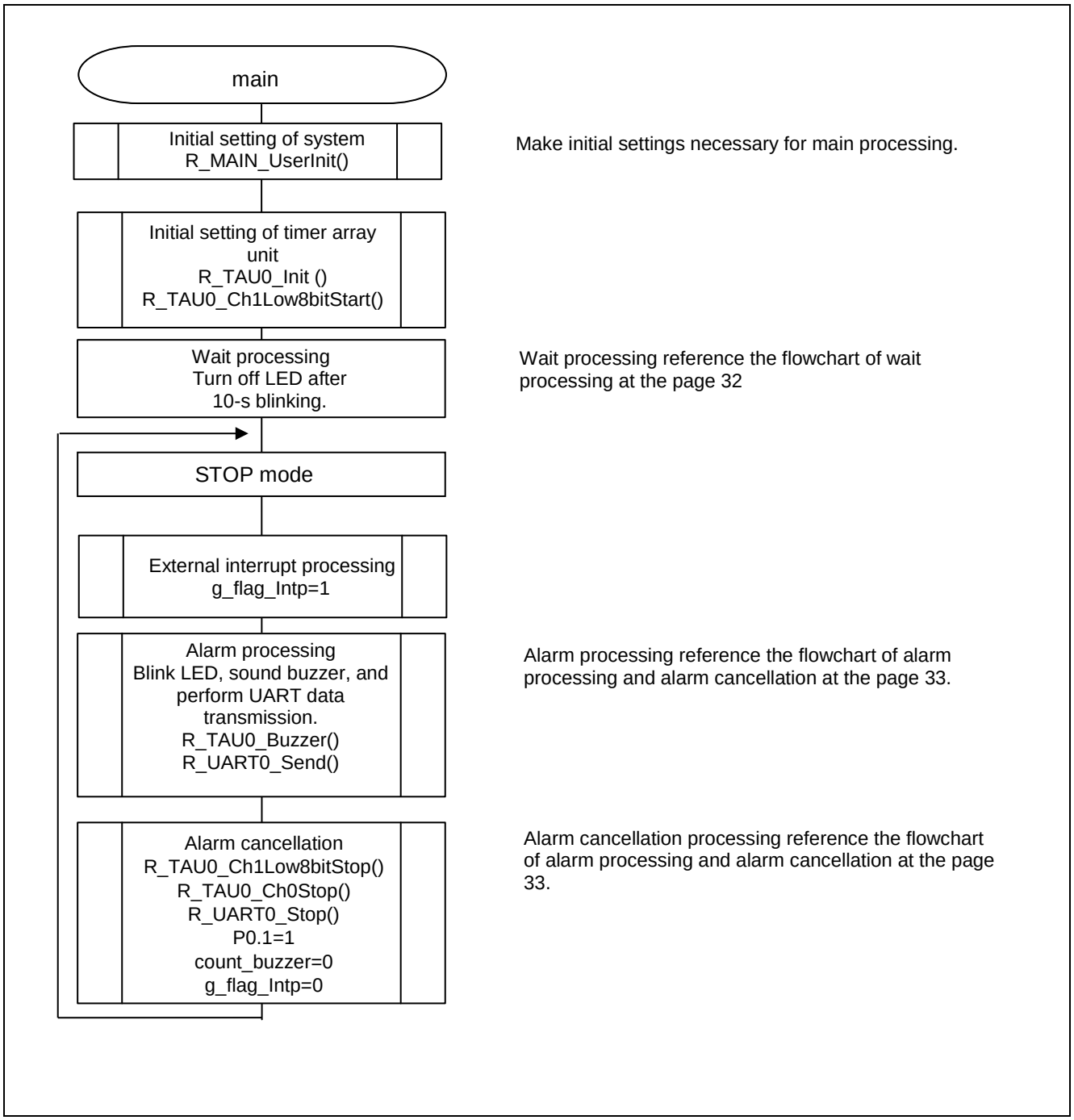

Figure 5.12 Main Processing Flowchart

5.6.11 Wait Processing Flowchart

Figure 5.13 shows the flowchart of the wait processing in the main processing.

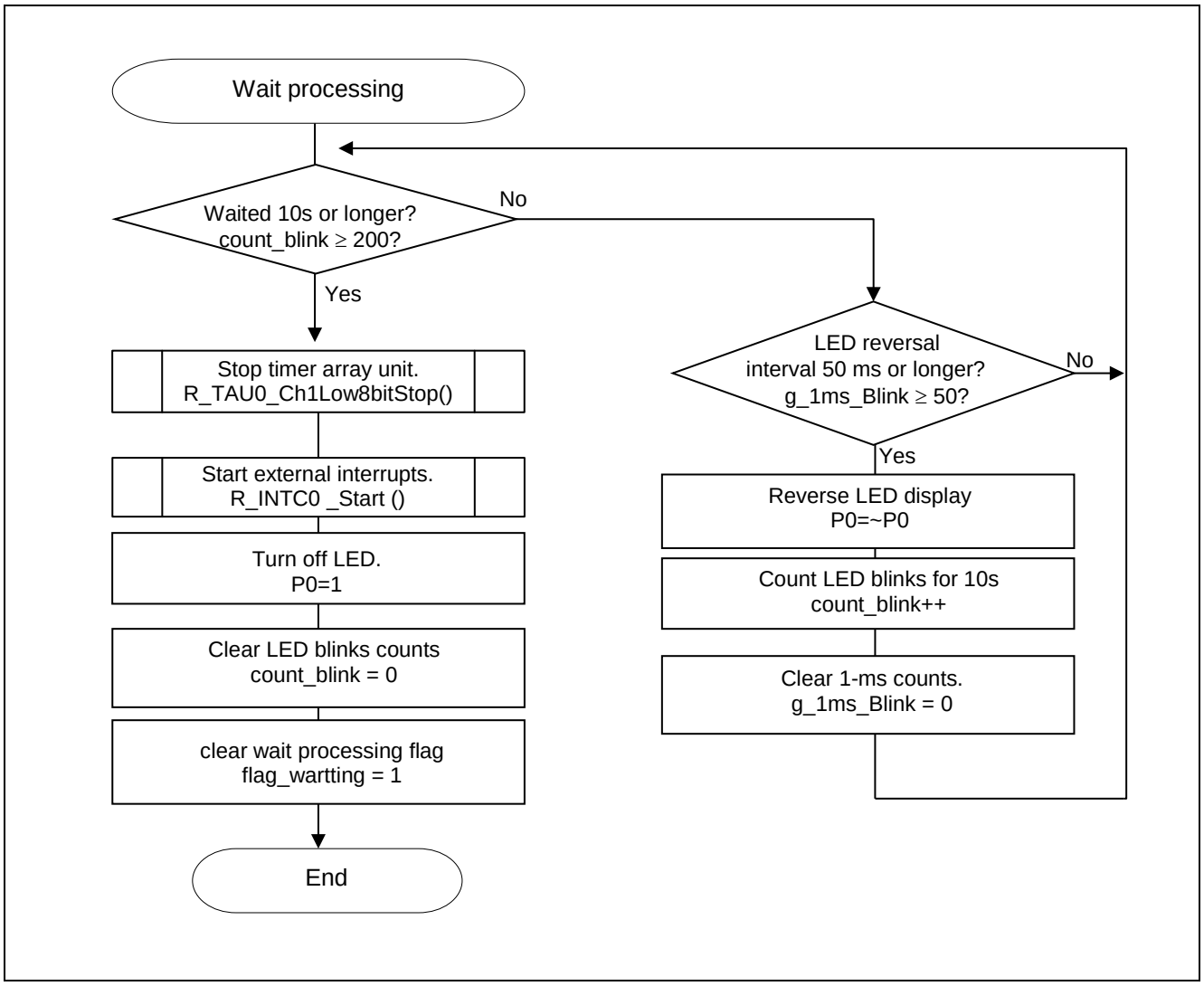

Figure 5.13 Flowchart of Wait Processing in Main Processing

5.6.12 Alarm Processing and Cancellation

Figure 5.14 shows the flowchart for processing and cancelling alarm in the main processing.

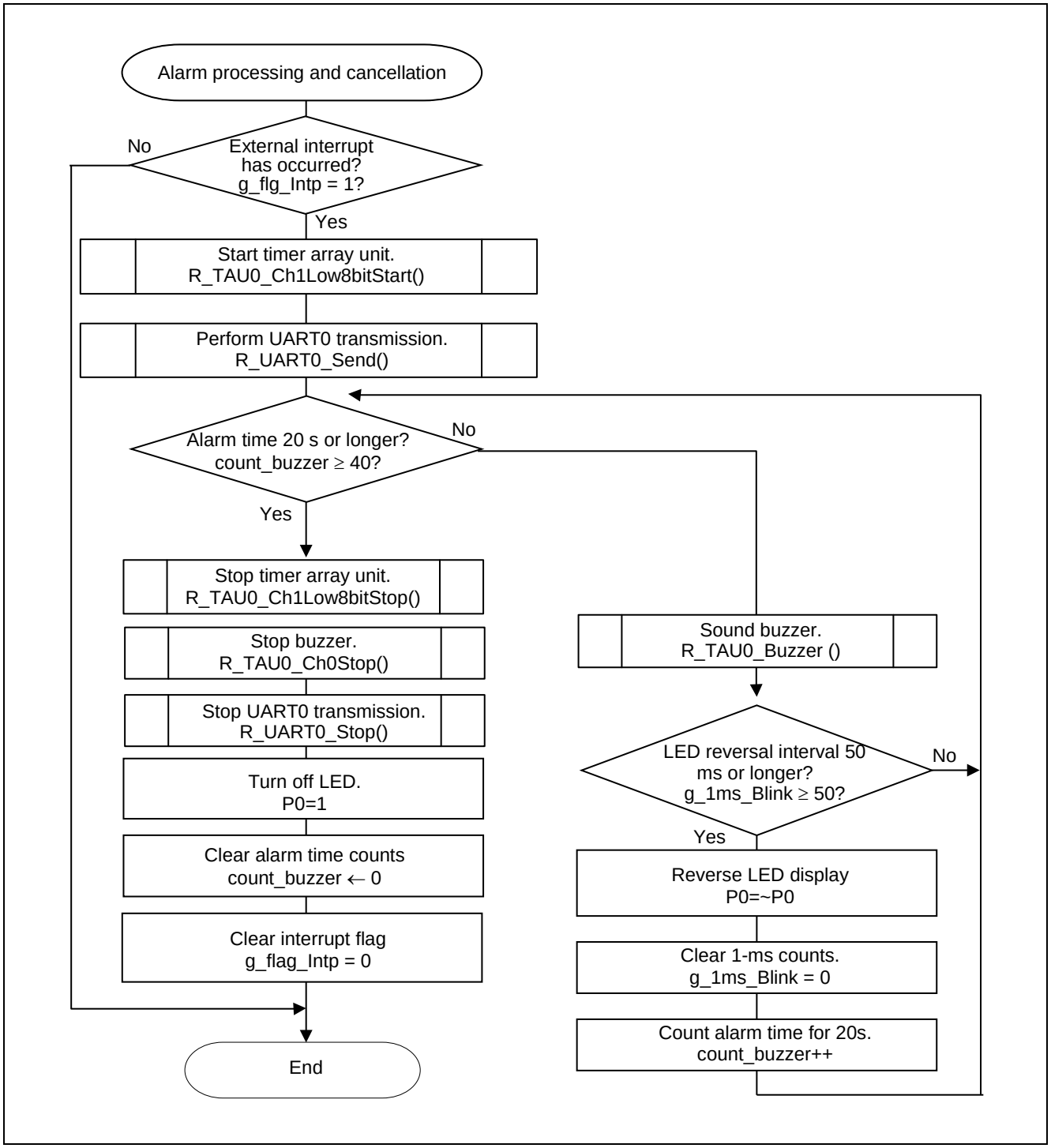

Figure 5.14 Flowchart for Processing and Cancelling Alarm in Main Processing

5.6.13 UART0 Starting Function

Figure 5.15 shows the flowchart of the UART0 starting function.

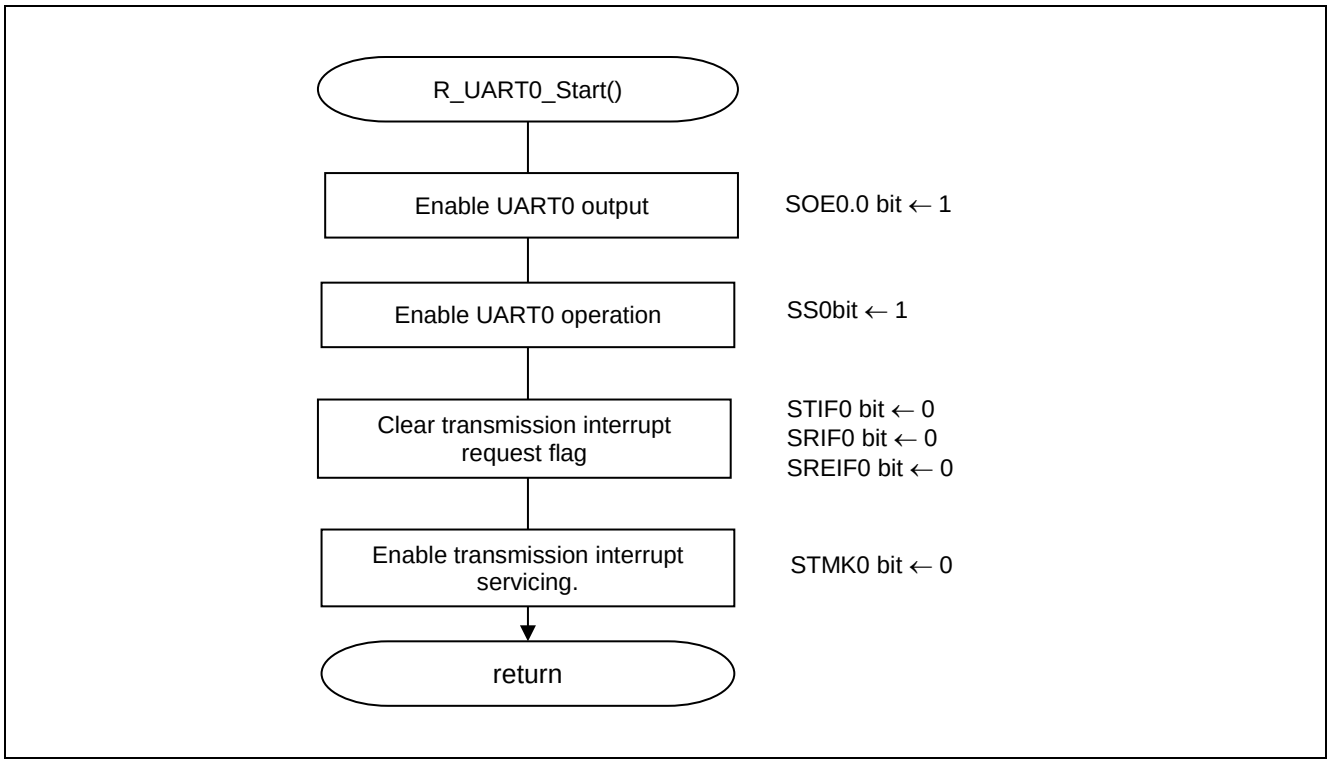

Figure 5.15 UART0 Starting Function

Interrupt setting

・Interrupt request flag registers(IF0L)
interrupt request flag cleared
・Interrupt mask flag registers(MK0L)
interrupt mask flag disabled

Symbol : IF0L (10 pin only)

7	6	5	4	3	2	1	0
TMIF00	TMIF01H	SREIF0	SRIF0	STIF0 CSIIF00 IICIF00	PIF1	PIF0	WDTIIF
x	x	**0**	**0**	**0**	x	x	x

SREIF0	SRIF0	STIF0	Interrupt request flag
0	**0**	**0**	**No interrupt request signal is generated**
1	1	1	Interrupt request is generated, interrupt request status

Symbol : MK0L (10 pin only)

7	6	5	4	3	2	1	0
TMMK00	TMMK01H	SREMK0	SRMK0	STMK0 CSIMK00 IICMK00	PMK1	PMK0	WDTIMK
x	x	**0**	**0**	**1**	x	x	x

SREMK0	SRMK0	STMK0	Interrupt servicing control
0	**0**	0	**Interrupt servicing enabled**
1	1	**1**	**Interrupt servicing disabled**

transmission operation enable

・serial channel start register0(SS0)
operation start

Symbol : SS0

7	6	5	4	3	2	1	0
0	0	0	0	SS03	SS02	SS01	SS00
0	0	0	0	x[note]	x	**1**[note]	**1**

Bit 3-0

SS0n	Operation start trigger of channel n
0	No trigger operation
1	**Sets the SE0n bit to 1 and enters the communication wait status[note]**

Note For the UART reception, set the RXE0n bit of SCR0nH register to 1, and then be sure to set SS0n to 1 after 4 or more fMCK clocks have elapsed.

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware

5.6.14 UART Data Transmission Function

Figure 5.16 shows the flowchart for the UART data transmission function.

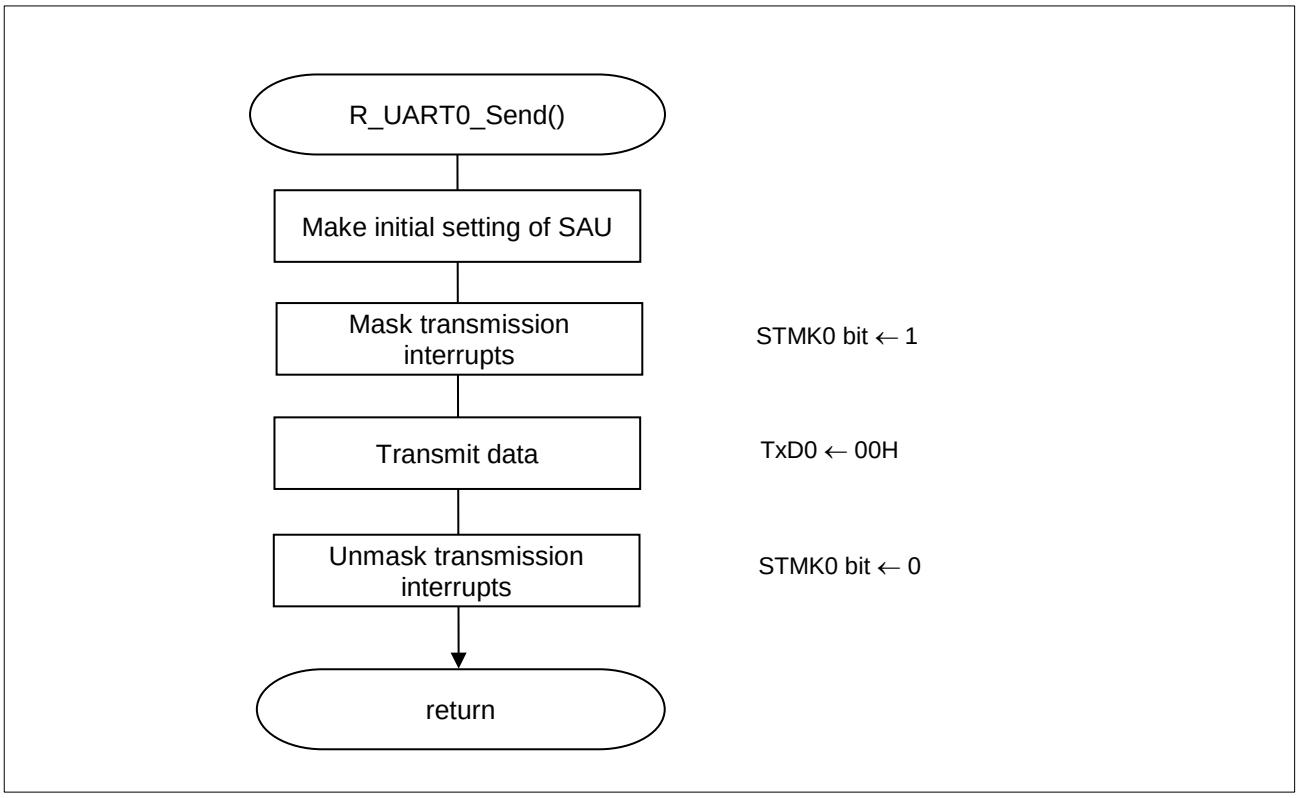

Figure 5.16 Flowchart of UART Data Transmission Function

5.6.15 Interrupt Processing

Figure 5.17 shows the flowchart of interrupt setup.

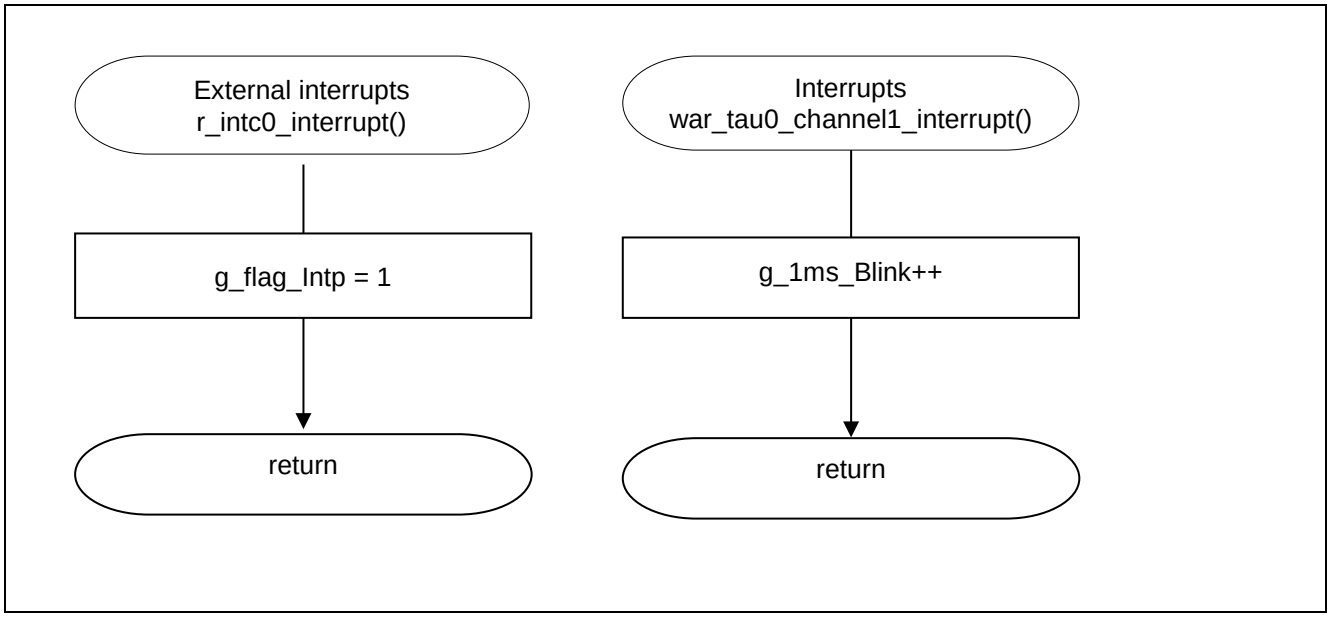

Figure 5.17 Flowchart of Interrupt Processing

Website and Support

Renesas Electronics Website
http://www.renesas.com/

Inquiries
http://www.renesas.com/contact/

Revision History <revision history,rh>

Rev.	Date	Description	
		Page	Summary
1.00	2017.11.30	-	

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other disputes involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawing, chart, program, algorithm, application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copy or otherwise misappropriation of Renesas Electronics products.
5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots etc.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Renesas Electronics products are neither intended nor authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems, surgical implantations etc.), or may cause serious property damages (space and undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for which the product is not intended by Renesas Electronics.
6. When using the Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat radiation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions or failure or accident arising out of the use of Renesas Electronics products beyond such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please ensure to implement safety measures to guard them against the possibility of bodily injury, injury or damage caused by fire, and social damage in the event of failure or malfunction of Renesas Electronics products, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures by your own responsibility as warranty for your products/system. Because the evaluation of microcomputer software alone is very difficult and not practical, please evaluate the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please investigate applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive carefully and sufficiently and use Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall not use Renesas Electronics products or technologies for (1) any purpose relating to the development, design, manufacture, use, stockpiling, etc., of weapons of mass destruction, such as nuclear weapons, chemical weapons, or biological weapons, or missiles (including unmanned aerial vehicles (UAVs)) for delivering such weapons, (2) any purpose relating to the development, design, manufacture, or use of conventional weapons, or (3) any other purpose of disturbing international peace and security, and you shall not sell, export, lease, transfer, or release Renesas Electronics products or technologies to any third party whether directly or indirectly with knowledge or reason to know that the third party or any other party will engage in the activities described above. When exporting, selling, transferring, etc., Renesas Electronics products or technologies, you shall comply with any applicable export control laws and regulations promulgated and administered by the governments of the countries asserting jurisdiction over the parties or transactions.
10. Please acknowledge and agree that you shall bear all the losses and damages which are incurred from the misuse or violation of the terms and conditions described in this document, including this notice, and hold Renesas Electronics harmless, if such misuse or violation results from your resale or making Renesas Electronics products available any third party.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.3.0-1 November 2016)

SALES OFFICES

Renesas Electronics Corporation

http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL II Stage, Indiranagar, Bangalore, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

Colophon 6.0