RL78

Minimizing Power Consumption when Sensing Switch Inputs

Introduction

The following document describes methods to minimize power dissipation when monitoring switch inputs.

Target Device

RL78

The principles in this application note are common for most MCU's. However, the specific example calculations and clock descriptions are based on the RL78/G13 device
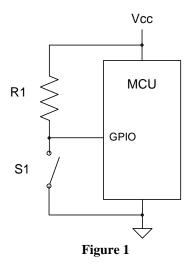
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1.   Introduction

A switch input is one of the simplest interfaces to an MCU. However, when very low power designs are needed the pullup or pulldown resistor for the switch can draw a significant current. If the switch input is a momentary switch the current flow is very short so it is rarely significant. However, if the switch input is a door switch or level sensing switch or any other switch which may remain in the active state for a relatively long time the energy used must be considered

Most of the discussion that follows gives examples for pull-up devices with the switches, the same principles apply for pull-down components. Also all the discussions assume that the EVdd = Vdd (all ports powered from the same supply voltage).

2.   Maximum Pull-up Resistor Size

Figure 1 shows a switch connected to a input pin on an MCU. If this was a door switch and the switch was in the position shown with the door closed the only current drain would be leakage currents from the GPIO, which are extremely low, and the MCU standby current. For a device like the RL78 this standby current will be significantly less than a microamp depending on the exact mode used.

Figure 1

When the door is opened there is a continuous current drain through the switch circuit until the door is closed again. For example, if the pull-up resistor was 10K and the power supply was 3V the current in the circuit is 300 uA. In applications where there are quite a few switches or the battery life needs to be extended as much as possible this becomes an issue. In many system designs S1 will be closed for normal operation so a break in wiring or connection causes an alarm or active state. In this case the current that is continuously flowing through the pull-up resistor can be even more of an issue.

An obvious improvement is to increase the size of R1. If the resistance was increased from 10K to 100K the current would decrease to 33 uA from 300 uA. Then the question becomes "How large can I make the pull-up resistor?" The size of the pull-up resistor is limited by the maximum port pin leakage current and the threshold for the port. For the RL78 the electrical characteristics section lists the maximum leakage current as 1 uA. The high level input threshold varies depending on the port but will typically be 0.8 or 0.7 * EVdd as shown below. Some ports which are TTL buffer inputs have different thresholds depending on the value of EVdd

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	Normal input buffer	$0.8EV_{DD}$		EV_{DD}	V
	V_{IH2}	P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143	TTL input buffer $4.0\ V \le EV_{DD} \le 5.5\ V$	2.2		EV_{DD}	V
			TTL input buffer $3.3\ V \le EV_{DD} < 4.0\ V$	2.0		EV_{DD}	V
			TTL input buffer $1.6\ V \le EV_{DD} < 3.3\ V$	1.50		EV_{DD}	V
	V_{IH3}	P20 to P27, P150 to P156		$0.7V_{DD}$		V_{DD}	V
	V_{IH4}	P60 to P63		$0.7EV_{DD}$		EV_{DD}	V
	V_{IH5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{RESET}$		$0.8V_{DD}$		V_{DD}	V

Figure 2

If we consider using P60 the input threshold would be 0.7 * Vdd . If the system is powered from 3.0V this means the minimum voltage that can be guaranteed to be considered a high would be 2.1V or 0.9V less than Vdd. The voltage drop due to leakage current flowing through the resistor must therefore be less than 0.9V This results in a maximum pull-up resistance of 0.9V / 1 uA = 900K ohms. Typically the leakage current would be much less but this calculation places a limit on what is guaranteed to give a high level.

Though the pull-up resistance can be increased to a very high level it is not always the best solution. This level would reduce the current to approximately 3.3 uA with a 3V supply but noise performance could be compromised. With a very large pull-up resistor it does not take much noise energy to create a false input transition. If the switch is remote there is also the possibility of external DC leakage paths which could cause a false trigger. It is also important to ensure that the switch or relay contact is rated for very low "wetting" currents. Some switches have a minimum current rating.

3.   Alternatives to a large pull-up resistors

Increasing the size of the pull-up resistor can have a negative impact on noise performance and still allows a fairly significant current to flow. Figure 3 shows an alternative design which can provide good noise performance and very low average currents in all states.
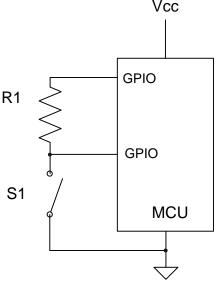
Figure 3

This design connects the top side of the pullup resistor to another IO pin on the MCU instead of Vcc. In the normal, open switch, state the port pin is driving the topside of the resistor to a high level and the operation is the same as having the resistor connected to Vcc. When the switch is closed an interrupt can still be used to "wake-up" the processor. However, when the processor wakes up the operation of the switch now changes. The input switch status is now configured for a polling operation. The MCU drives the topside of R1 low to minimize power then transitions into a low power state or performs other tasks. After some time a clock signal wakes the MCU up. The port pin driving R1 is switched high and the input level of the switch input is tested. If it is still closed polling continues. If it is now open the system goes back to the "normal" state. This operation allows a very low power mode to be used for the "normal" state and still provides good response since an interrupt is used. Switching to a polling mode once the switch circuit is active minimizes power consumption with a pull-up resistance which provides good performance.

The same concept would work using the internal pull-up available on most GPIO inputs. In this case a separate IO pin is not required. The pin connected to the switch is alternately configured as an input with the pullup resistor on when monitoring and an output driven low in the low power non-monitoring state. This method only works when the switch is connected from the input to ground. If the switch was on the Vcc side it would require a device with an internal pull-down and the output would be driven high for low power

With some MCU devices this method has the drawback that the system must have a 32 kHz crystal to enable a low power clock source to wake-up. With the RL78 the low speed on-chip oscillator (OCO) can be used to provide the wake-up clock source since the time between polls is not critical. In many applications the system design can be simplified by always polling the switch, using a 32 kHz oscillator or the internal OCO to maintain the low power clocking signals. This is especially true if the time spent with the switch in an active state is relatively long or the switch being used is normally closed. The extremely low RTC mode current of the RL78 makes this mode of operation more efficient, in most cases, then relying on large pull-up resistors which are constantly drawing current when the switch is closed. Table 1 shows the average current for various sampling rates when using a 10K resistor connected as shown in figure 1. For the data shown below the MCU is waking to an 8 MHz clock.

Polling Interval	Average Current
1 millisecond	11.4 uA
10 milliseconds	1.6 uA
50 milliseconds	0.7 uA

Table 1

When the timer generates an interrupt the top side of the resistor is driven high for approximately 3 uS then the input level on the switch input is monitored. The 3 uS delay allows the capacitance of the system to be charged so there is a valid level at the pin input. In this example the RL78 interval timer is driven from the internal low speed oscillator so there is no additional cost for a 32 kHz crystal. If a 32 kHz crystal is used the MCU could wake to the 32 kHz (sub-clock) which would result in lower average currents. Notice that a 50 millisecond sampling rate results in a current draw that is well under 1 uA. This low current draw would require approximately 6 mAH from a battery in a year and the 50 millisecond response time is fast enough that a person would not recognize any noticeable delay in the actuation.

4.   Summary

When designing low power systems even simple connections like switch inputs must be considered. The current consumed by the pull-up or pull-down resistor when the switch is active can be much larger than the standby current of the MCU. The RL78 MCU has extremely low currents, less than 1 uA, while a timer is still operating from the low speed on-chip oscillator or external 32 kHz crystal. These very low currents give an option to the designer to poll the inputs for excellent power performance rather than increasing the resistance value to a level which may result in poor noise performance or erratic operation

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Revision Record

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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