RH850/F1Kx

Using Serial flash memory interface SFMA

R02AN0046EE0100
Rev.1.00
September 7, 2021

Introduction

RH850/F1Kx series provide Serial flash memory interface (SFMA) for external NOR or NAND serial flash memory.

This document provides a general introduction of serial flash memory type, SFMA configuration flow and sample software.

Target Device

This document describes the SFMA sample software on RH850/F1Kx series.

Used device for sample application is RH850/F1KH-D8 R7F7017093AFP. Concept described in this document applies to all member of RH850/F1Kx series which have SFMA.

Presence of SFMA in RH850/F1Kx series

Product name			RH850/F1KH-D8 176pin	RH850/F1KH-D8 233pin	RH850/F1KH-D8 324pin
Number of unit			1	1	1
Name			SFMAn(n=0)	SFMAn(n=0)	SFMAn(n=0)
Product name	RH850/F1KM-S4 100pin	RH850/F1KM-S4 144pin	RH850/F1KM-S4 176pin	RH850/F1KM-S4 233pin	RH850/F1KM-S4 272pin
Number of unit	0	1	1	1	1
Name		SFMAn(n=0)	SFMAn(n=0)	SFMAn(n=0)	SFMAn(n=0)
Product name	RH850/F1KM-S2 100pin	RH850/F1KM-S2 144pin	RH850/F1KM-S2 176pin		
Number of unit	0	1	1		
Name		SFMAn(n=0)	SFMAn(n=0)		
Product name	RH850/F1KM-S1 48pin	RH850/F1KM-S1 n 64pi	RH850/F1KM-S1 80pin	RH850/F1KM-S1 100pin	
Number of unit	0	0	0	0	
Name					

Disclaimer

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1. Serial flash memory types

There two type of non-volatile serial flash memory – NOR and NAND. The names stand for different logic gate used in the memory. Commercial NOR flash memory was first introduced by Intel in 1988. NAND flash was introduced by Toshiba in 1989(source Wikipedia)

One of the main differences is capacity, NAND flash have higher density compare to NOR flash. The other difference is access speed - NAND flash is faster than NOR flash. In both types NOR and NAND, memory is organized in sectors, blocks and pages. Before write to those memories you need to erase the cell, the smallest part to write is sector, the volume of it depends of producer how they make their product memory map. In both memory information is accessible by byte, but write access is always by smallest part – sector, hence you can't write only one byte of data, always need to write the complete sector at byte level. Serial flash memories support SPI protocol.

In this document used serial flash memory is NOR, with smallest sector to write/erase of 4KB, organized in 16383 sectors of 4KB or 2047 Blocks of 32KB or 1023 block of 64 KB in total 512Mb or 64MB.

2. RH850/F1Kx Serial Flash Memory Interface A

In RH850/F1Kx devices line are implemented serial flash memory interface A periphery. SFMA is part of H-Bus, outputs control signal to external serial flash memory are connected to the SPI multi I/O bus space, thus enable direct connection to external serial flash memory.

Module allows two type of access to external serial flash memory – SPI operating mode for read/write operation and External Address space read operating mode only for read operation.

SFMA set in External Address space read operating mode, translate read operation from internal address space ($3000\ 0000_H$ to $33FF\ FFFF_H$) to SPI bus sequence.

2.1 Overview

2.1.1 External Input/Output signals

SFMA module allow only one external serial flash memory to be connected to the device and is available only in Port11 in RH850/F1Kx series.

Table 1 External Input/Output Signals (RH850/F1KH-D8, RH850/F1KM-S4, RH850/F1KM-S2)

Unit signal name	Description	Alternative port Pin Signal
SFMA0		
SPBCLK	Clock output	SFMA0CLK
SPBSSL	Slave select	SFMA0SSL
SPBMO/SPBIO0	Master transmit data/Data 0	SFMA0IO0
SPBMI/SPBIO1	Master input data/Data 1	SFMA0IO1
SPBIO2	Data 2	SFMA0IO2
SPBIO3	Data 3	SFMA0IO3

2.1.2 Clock supply

- Register access clock source are CPUCLK_L, CKSCLK_IPERI1
- Bϕ source clock is CKSCLK_IPERI1 – for SFMA bit rate generator, generated by division of Bϕ. Maximum bit rate is 40MHz

2.1.3 Reset sources

- All reset sources (ISORES)

2.1.4 Interrupt sources

- SFMA do not support any interrupt

2.1.5 Registers

SFMA module have 18 register separated in four type with base address 1004 0000_H

1. Common control registers – for setting bit rate, SSL delay and communication transfer bus dimension
2. Data read control registers – for setting up an External Address space read operating mode
3. SPI mode registers – for setting up a SPI operating mode
4. Common status register

2.1.6 Block diagram

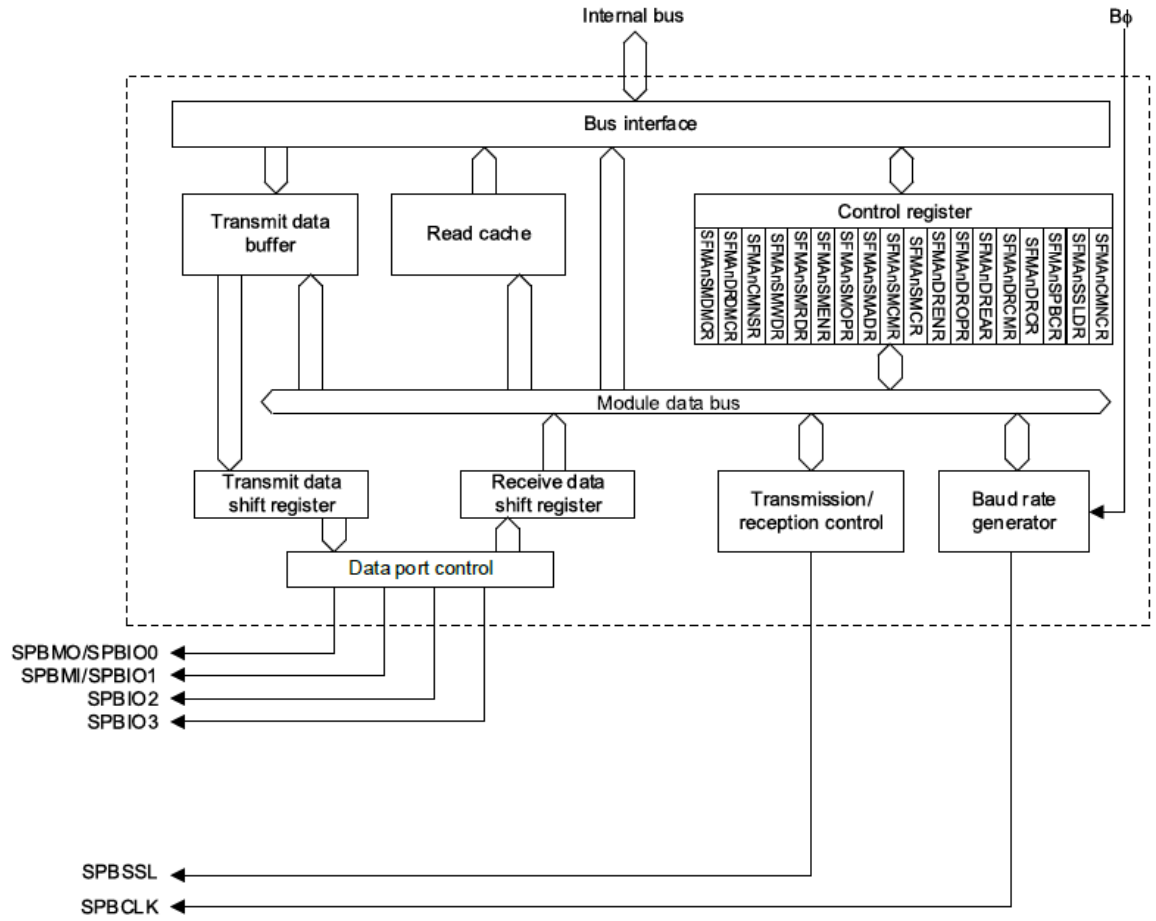


Figure 1 SFMA block diagram

2.1.7 Bit rate calculation

Bit rate for SFMA module is calculated of SPBR[7:0] and BRDV[1:0] set in register SFMAnSPBCR.

$$\text{Bit rate} = \frac{\text{B}\phi}{(2 * \text{SPBR}[7:0] * 2^{\text{BRDV}[1:0]})} [MHz]$$

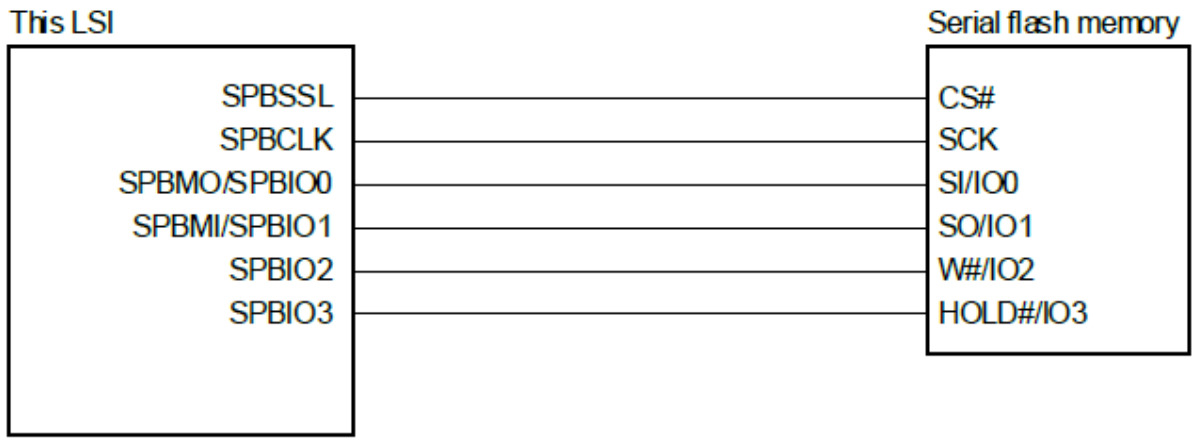
Bϕ = CKSCLK_IPERI1

SPBR[7:0] is prohibited to be 0, before SFMA start SPI operation SPBR[7:0] need to be changed to non-zero value

2.2 Operation modes

2.2.1 System configuration

SFMA module support 3 type of SPI bus data size – 1bit, 2bit and 4bit



Note: Figure shows 4bit data size bus.
Recommendation is to attach external flash memory always like 4bit data size. SPBIO2,SPBIO3 can be configured durigng negation and idle period, when use 1bit or 2bit data size bus,to be on state which corespond with external memory demands for hold, word tansfer or hw write protection.

Notes: 1. Common used pin in independent of data bus size are SPBSSL,SPBCLK
2. 1bit size – used pin are SPBMO and SPBMI
3. 2bit size – used pin are SPBIO0 and SPBIO1
4. 4bit size – used pin are SPBIO0, SPBIO1, SPBIO2, SPBIO3

Figure 2 SFMA system configuration

2.2.2 SPI operation mode

SFMA SPI operation mode support 1bit, 2bit, and 4bit data size bus. Can transfer 8bit or 16bit command, 24bit or 32bit address as well as option bytes – 1byte, 2byte, 3byte or 4 bytes. SFMA SPI read operation can be perform only in 8bit, 16bit or 32bit – all other states are forbidden.

- If it is needed to transfer only command to external flash memory it is important to set SPIDE[3:0] in SFMAnSMENR to 0000, no matter if SPIRE=0 in SFMAnSMCR. Some serial flash memory accept command only when SSL pin goes high at the end of the command send ends. To be able SFMA to fulfil this demand, above suggestion should be kept.
- When use 2bit or 4bit data size bus – it is forbidden Read and Write operation to be set in SFMAnSMCR at the same time
- External serial flash support auto increment address during Read and Write operation for faster access, once first address is send it is automatically increment when read or write access is issued – in this case SSL signal should be kept low during all operation and goes high after operation is completed – this is controlled by SSLKP bit in SFMAnSMCR
- In 2bit or 4bit data size some serial flash needs dummy cycle after address transfer to be send – bus size of dummy cycle is controlled by DMDB[1:0] in SFMAnSMDMCR register the number of dummy cycle are controlled by DMCYC[2:0] in SFMAnSMDMCR register. Enable or disable transfer of dummy cycles is controlled by DME bit in SFMAnSMENR register. SFMA support from 1 to 8 cycles.

2.2.3 SPI initial setting flow

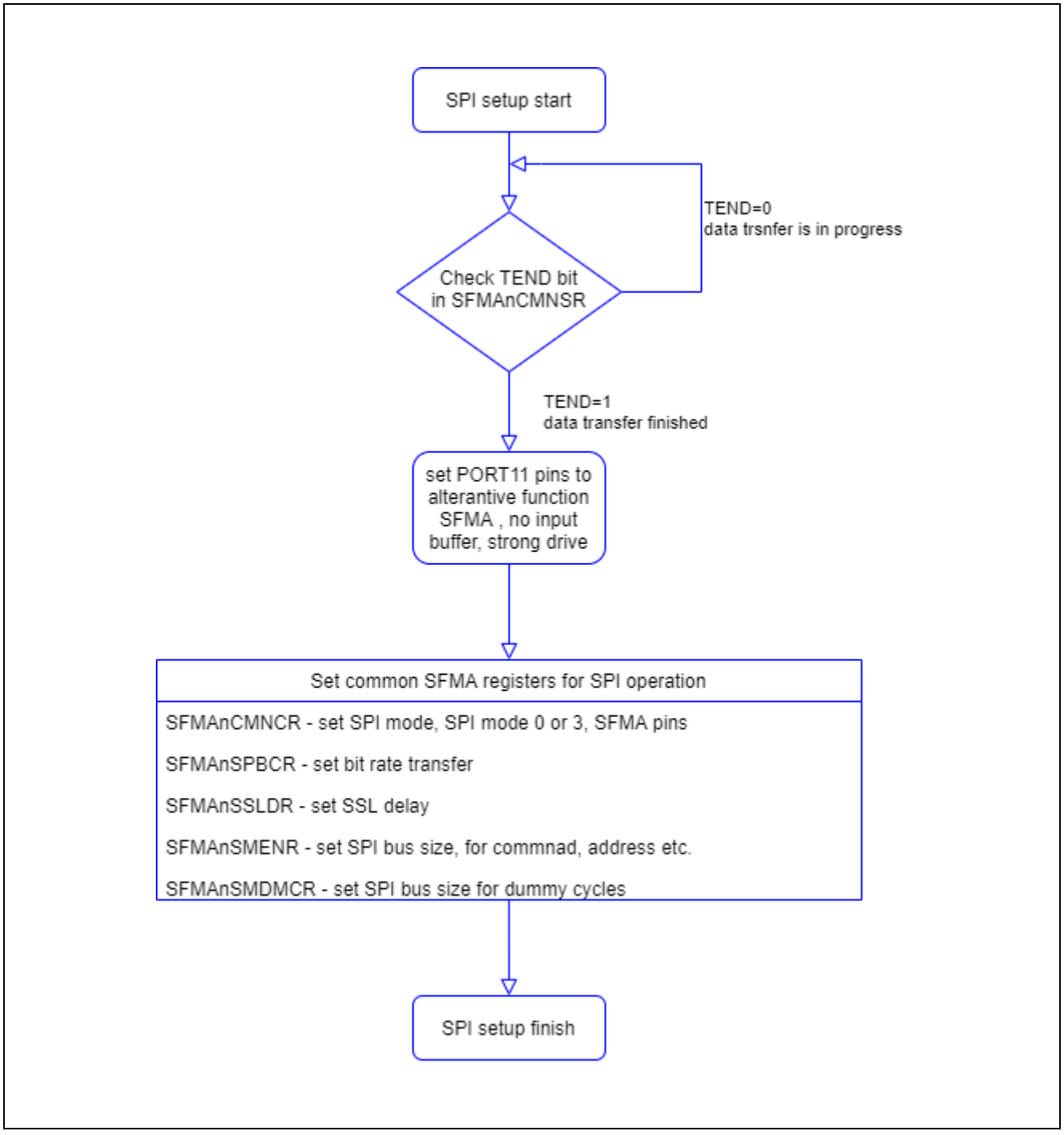


Figure 3 SPI initial setting flow

2.2.4 External Address Space Read Mode

SFMA External Address Space Read mode support 1bit, 2bit, and 4bit data size bus. Can transfer 8bit or 16bit command, 24bit or 32bit address as well as option bytes – 1byte, 2byte, 3byte or 4 bytes.

- In this mode external serial flash memory are connected to the SPI multi I/O bus space. With other words read access issued to internal address (3000 0000_H to 33FF $FFFF_H$) will be transform to SPI bus sequence. Since this space is only 64MB, only part of external serial flash can be accessed. To extend up to 4GB address space SFMA module have SFMAnDREAR — Data Read Extended Address Setting Register, where upper 6bits of 32bit serial flash address can be stored.
- In 2bit or 4bit data size some serial flash needs dummy cycle after address transfer to be send – bus size of dummy cycle is controlled by DMDB[1:0] in SFMAnDRDMCR register the number of dummy cycle are controlled by DMCYC[2:0] in SFMAnDRDMCR register. Enable or disable transfer is controlled by DME bit in SFMAnDRENR register. SFMA support from 1 to 8 cycles.
- In normal External Address Space Read operation – read can be issued by byte, word or double word depends of the internal address space access issued.
- External Address Space Read mode support also burst read – in this mode read operation is always 64bit. This mode can use built-in read cache with size of 64bits and 16 entries.

2.2.5 External address space initial setting flow

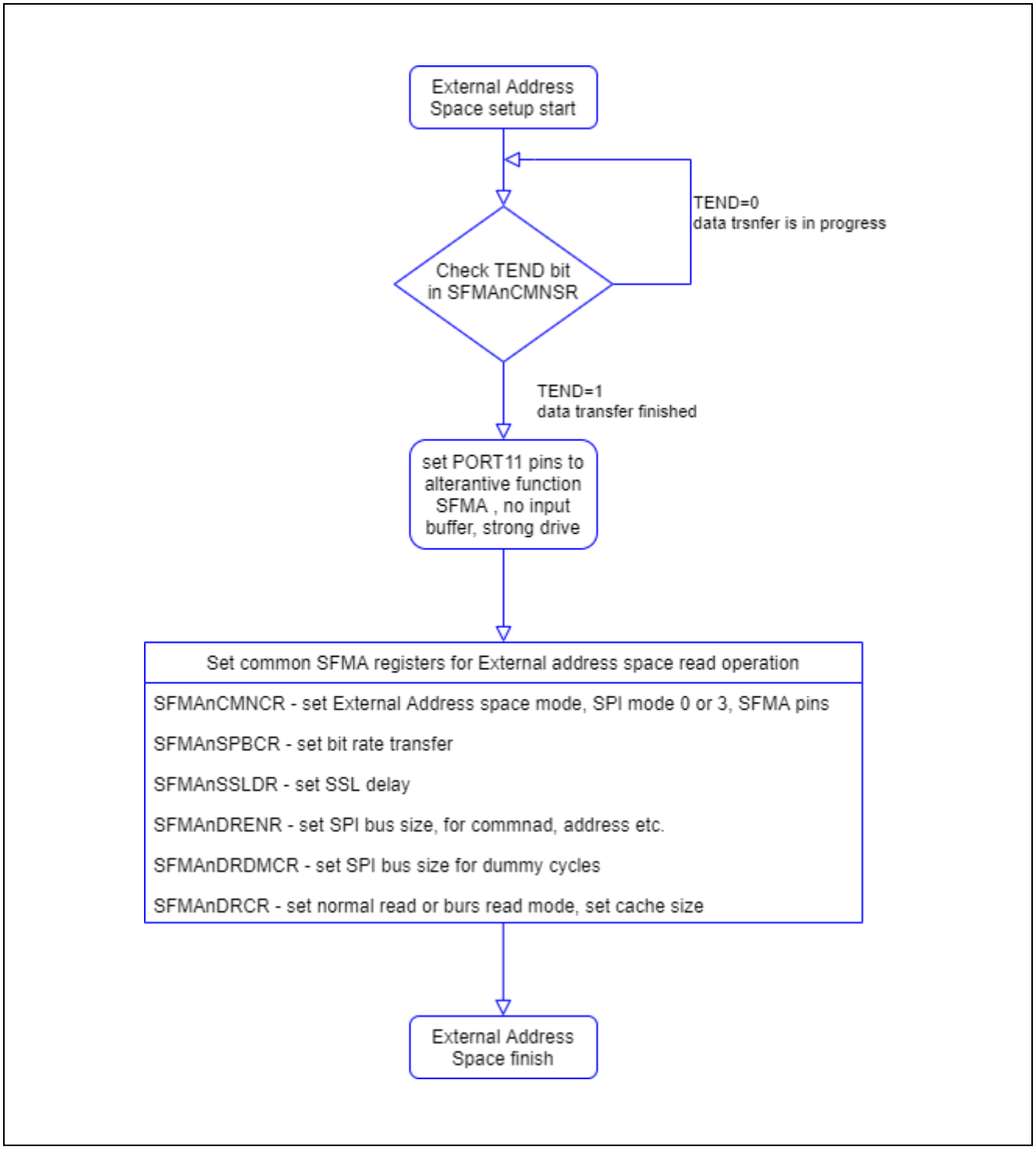


Figure 4 External address space initial setting flow

3. Software and hardware tools

This section contains information what tools and hardware development platform are used to implement SFMA samples software

3.1 Software development tools

- Compiler used for sample SFMA software is GHS v2020.1.5 for RH850/F1Kx series
- Debug probe – Renesas E2 emulator

3.2 Hardware development tools

- Main board - Y-RH850-X2X-MB-T1-V, the last version of this document can be obtained from the following web location: Y-RH850-X2X-MB-T1-V1 Documents
- PiggyBack board - Y-RH850-F1X-176PIN-PB-T1-V4 with mounted device RH850/F1KH-D8 R7F7017093AFP, the latest document can be obtained from the following web location: Y-RH850-F1X-176PIN-PB-T1-V4 Documents
- Peripheral module eMMC/SFMA - RH850-EMMC-SFMA-EXT-BRD. The extension board includes one eMMC IC (swissbit SFEM4096B1EA1, 4GB NAND flash) and one serial flash NOR IC (Macronix MX25L51245GMISFMA, 512Mbit). Schematic and description of connection are described in Y-RH850-X2X-MB-T1-V user manual section 4.9 eMMC/SFMA module.

3.2.1 Setup hardware tools

This section describes how to connect main board, piggy board, and peripheral module

- Peripheral module eMMC/SFMA by default have main bord connection to CN2, PiggyBack board - Y-RH850-F1X-176PIN-PB-T1-V4 do not have Port11 connection to CN2, to use SFMA interface additional 7 pin header 2,54mm pitch should be added (**Figure 5** yellow ellipse). Jumper JP2 (**Figure 5** red ellipse) should be applied to power supply serial flash IC.
- Connection between target device RH850/F1KH-D8 R7F7017093A on piggy board and serial flash IC should be done by wire (**Figure 6**). Please refer to **Table 2**

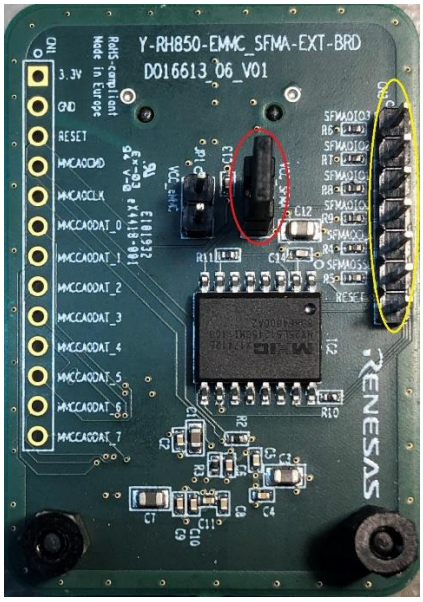


Figure 5 Peripheral module eMMC/SFMA - RH850-EMMC-SFMA-EXT-BRD

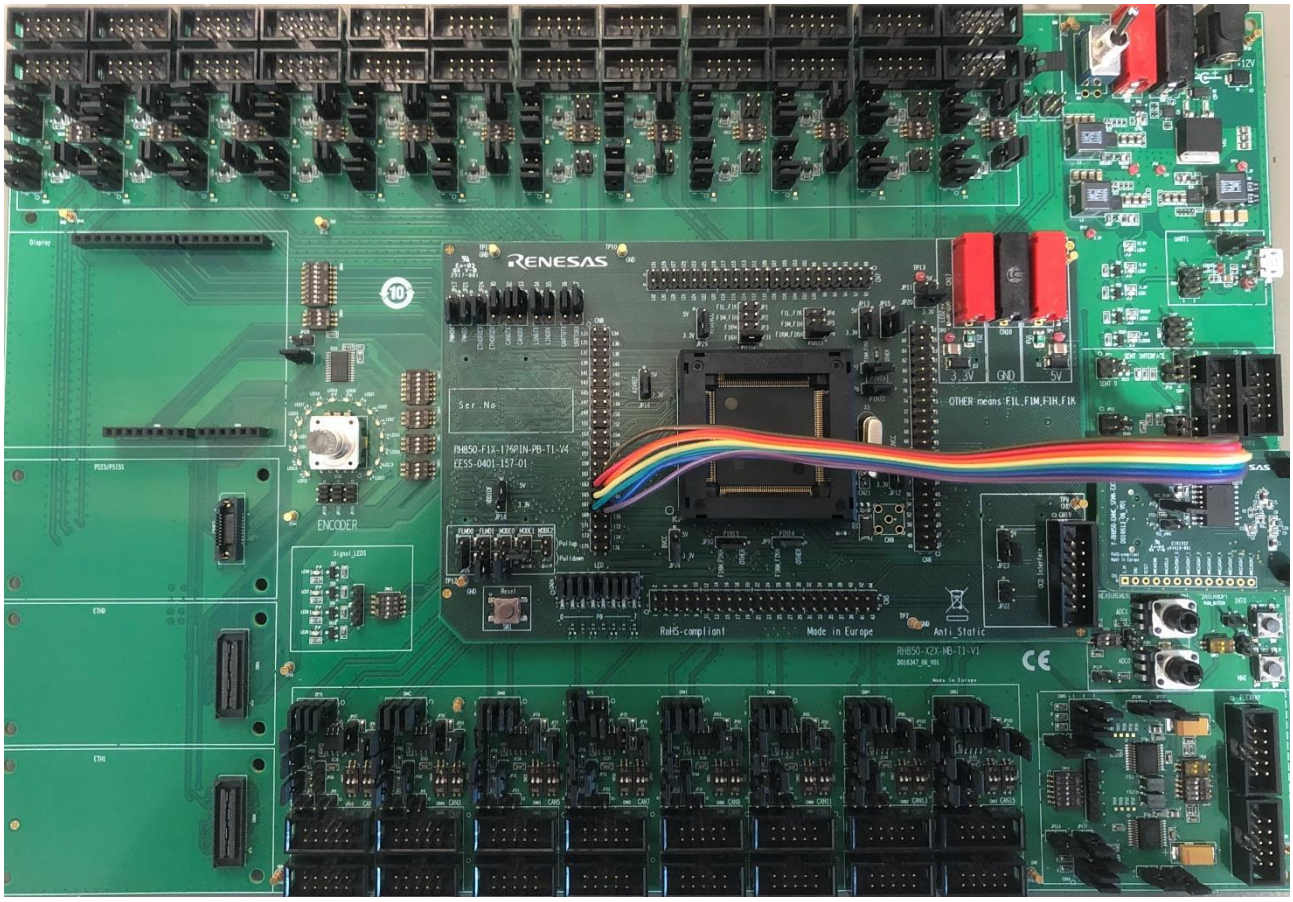


Figure 6 Wire connection piggy board to peripheral module eMMC/SFMA

Table 2 Connection table between piggy board and peripheral module eMMC/SFMA

SFMA signal name	Alternative port Pin Signal	Device port	F1x-176pin device	PiggyBack board RH850/F1x-176pin	eMMC/SFMA extension module
		Port11	pin	CN8	CN3
SPBCLK	SFMA0CLK	Port11_7	167	CN8_35	CN3_5
SPBSSL	SFMA0SSL	Port11_6	166	CN8_34	CN3_6
SPBMO/SPBIO0	SFMA0IO0	Port11_5	165	CN8_33	CN3_4
SPBMI/SPBIO1	SFMA0IO1	Port11_4	164	CN8_32	CN3_3
SPBIO2	SFMA0IO2	Port11_3	163	CN8_31	CN3_2
SPBIO3	SFMA0IO3	Port11_2	162	CN8_30	CN3_1

4. Sample SFMA software

This section describes SFMA sample software

- Location of SFMA driver - {Project folder}\peripherals\sfma
- Contain 2 file – sfma.c and sfma.h

4.1 Functions description in sfma.c

- void R_SFMA_DeInit(void); - put SFMA module register in reset state
- r_Error_t R_SFMA_Init(uint32_t mode, uint32_t bus_size); - Set SFMA module to SPI or Address space mode, 1bit, 2bit or 4bit
- uint32_t R_SFMA_ExecCmd(uint8_t cmd, uint16_t response); - send command via SFMA to external flash memory, return readed value if desired.
- void R_SFMA_SectorErase4B(uint32_t address); - execute sector erase sequence: WREN(write enable commnad) then Erase command
- void R_SFMA_ReadSPI4B(uint32_t readAddress,uint32_t byteNum,char_t * readBuff); - read desire bytes from given address in external flash memory and store it in pointed buffer
- void R_SFMA_WriteSPI4B(uint32_t writeAddress,uint32_t byteNum,char_t * writeBuff); - execute write sequence .Sector Erase ->WREN -> write desire bytes to external flash to given address from pointed buffer

4.2 Sample SFMA Software Block Schema

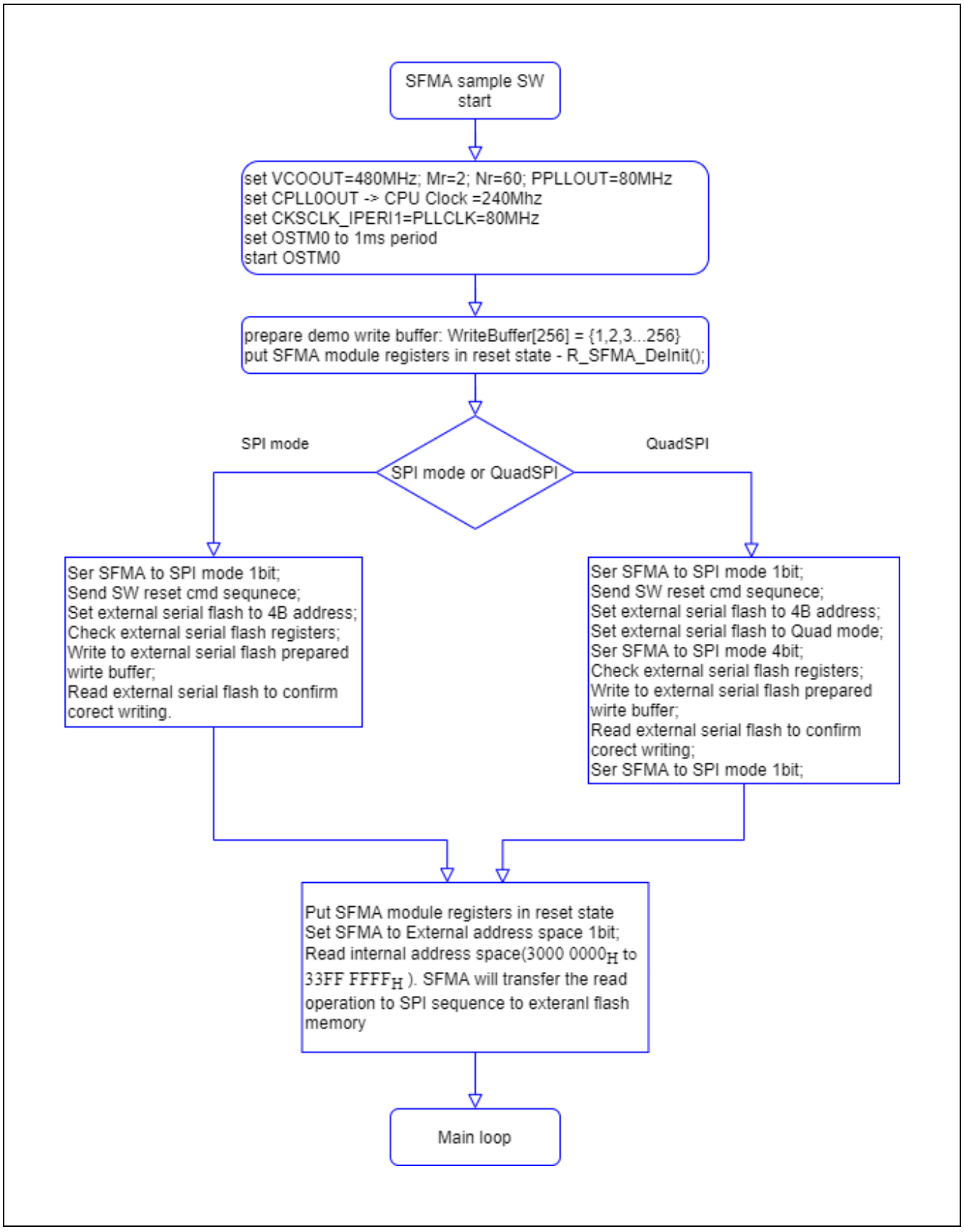


Figure 7 Sample SW block schema

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Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	23.08.2021		Initial release

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2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

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   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

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