R8C/L3AC Group

Timer RA Event Counter Mode
(Counting Both Edges Using Event Input Control)

REJ05B1188-0110
Rev.1.10
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1. Abstract

This document describes the setting method and an application example for counting both edges of an input pulse using the event input control of timer RA (event counter mode) in the R8C/L3AC Group.

2. Introduction

The application example described in this document applies to the following microcomputer (MCU):

- MCU: R8C/L3AC Group

This application note can be used with other R8C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Application Example

3.1 Program Outline

The number of both edges of the external signal input to the TRAIO pin is counted based on the $\overline{\text{INT2}}$ input level. The timer RA interrupt is generated each time both edges are counted five times.

Settings

- The event input is enabled while $\overline{\text{INT2}}$ input is high.
- The TRAIO pin is assigned to $\overline{\text{INT4}}$.
- Both edges of the TRAIO input are counted.
- No TRAIO input filter is selected.
- The programmable I/O port is set as the TRAO pin function.

Figure 3.1 shows an Operating Example and Table 3.1 lists the pins used and their functions.

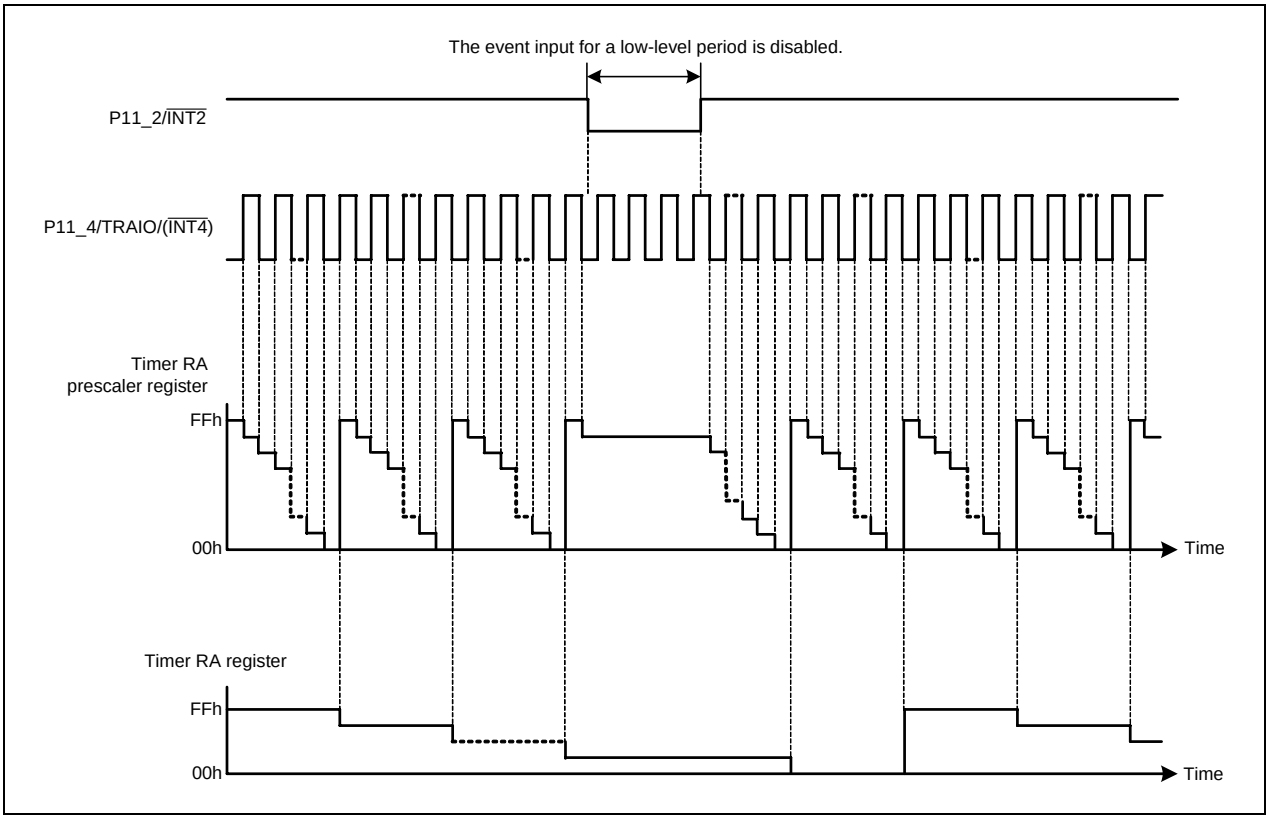


Figure 3.1 Operating Example

Table 3.1 Pins and Their Functions

Pin Name	I/O	Function
P11_2/$\overline{\text{INT2}}$	Input	Event input control
P11_4/TRAIO/($\overline{\text{INT4}}$)	Input	External signal input

3.2 Memory

Table 3.2 Memory

Memory	Size	Remarks
ROM	195 bytes	In the rej05b1188_src.c module
RAM	2 bytes	In the rej05b1188_src.c module
Maximum user stack	10 bytes	
Maximum interrupt stack	18 bytes	

Memory size varies depending on the C compiler version and compile options.
The above applies to the following conditions:
C compiler: M16C/60, 30, 20, 10, and Tiny and R8C/Tiny Series Compiler V.5.45 Release 00
Compile option: -c -finfo -dir “$(CONFIGDIR)” -R8C

4. Software

This section shows the initial setting procedures and values to set the example described in section **3. Application Example**. Refer to the latest **R8C/L3AC Group hardware user's manual** for details on individual registers.

The × in the register's Setting Value represents bits not used in this application, blank spaces represent bits that do not change, and the dash represents reserved bits or bits that have nothing assigned.

4.1 Function Tables

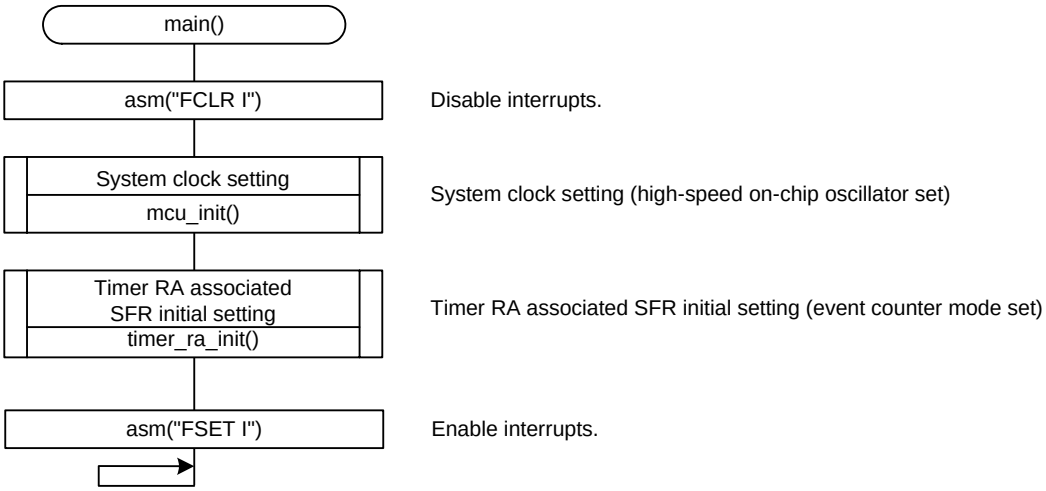
Declaration	void mcu_init(void)		
Outline	System clock setting		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Set the system clock (high-speed on-chip oscillator).		

Declaration	void timer_ra_init(void)		
Outline	Timer RA associated SFR initial setting		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Perform the initial setting for the SFR register to use timer RA in event counter mode (the event input for a high-level period is enabled and it is counted at both edges).		

Declaration	void timer_ra_interrupt(void)		
Outline	Timer RA interrupt handling		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Count timer RA underflow.		

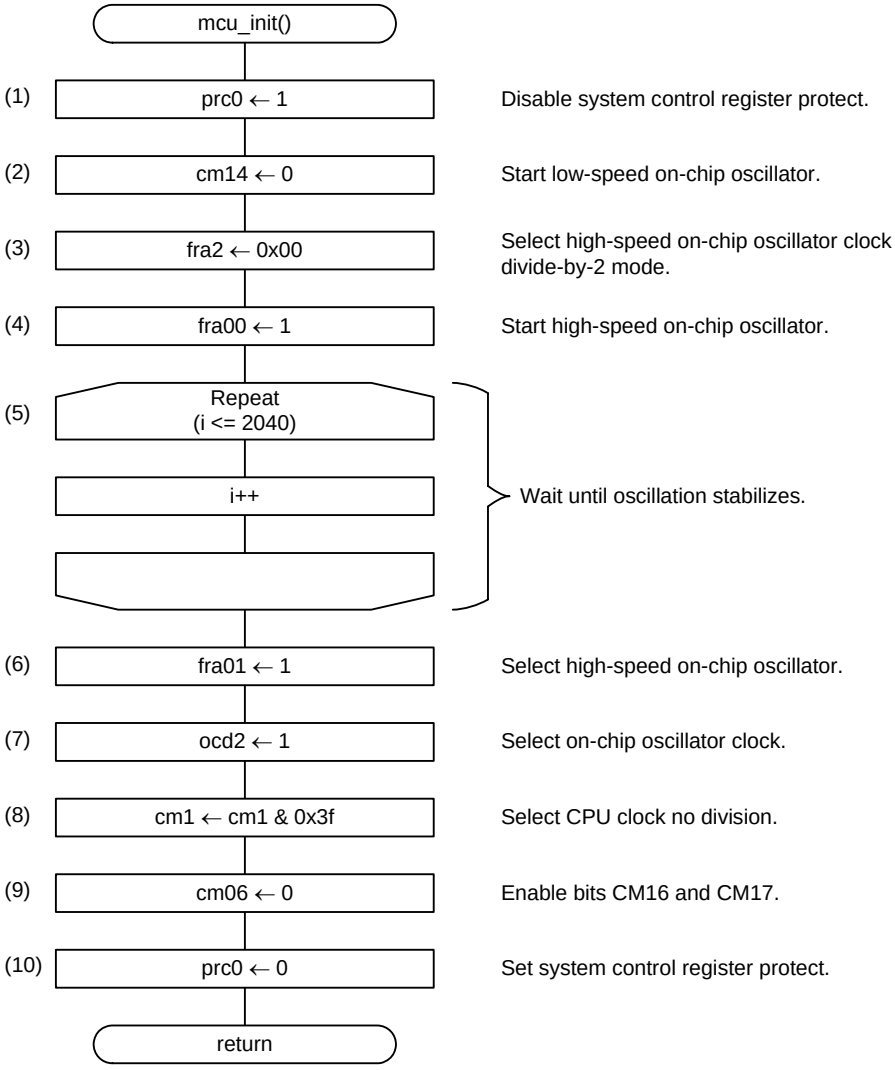
4.2 Main Function

- Flowchart



4.3 System Clock Setting

- Flowchart



• Register settings

(1) Enable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	—	x	1

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 1: Write enabled	R/W

(2) Start the low-speed on-chip oscillator.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			—	0	x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b4	CM14	Low-speed on-chip oscillator stop bit	0: Low-speed on-chip oscillator on	R/W

(3) Set the division ratio for the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 2 (FRA2)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	—	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FRA20	High-speed on-chip oscillator frequency switching bit	Division selection These bits select the division ratio for the high-speed on-chip oscillator clock. b2 b1 b0 0 0 0: Divide-by-2 mode	R/W
b1	FRA21			R/W
b2	FRA22			R/W

(4) Start the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	—		1

Bit	Symbol	Bit Name	Function	R/W
b0	FRA00	High-speed on-chip oscillator enable bit	1: High-speed on-chip oscillator on	R/W

(5) Wait until oscillation stabilizes.

(6) Select the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	—	1	

Bit	Symbol	Bit Name	Function	R/W
b1	FRA01	High-speed on-chip oscillator select bit	1: High-speed on-chip oscillator selected	R/W

(7) Select the on-chip oscillator clock as the system clock.

Oscillation Stop Detection Register (OCD)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	1	x	x

Bit	Symbol	Bit Name	Function	R/W
b2	OCD2	On-chip oscillator clock select bit	1: On-chip oscillator clock selected	R/W

(8) Set CPU clock division select bit 1.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	—		x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b6	CM16	CPU clock division select bit 1	b7 b6 0 0: No division mode	R/W
b7	CM17			R/W

(9) Set CPU clock division select bit 0.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	0	x	x	x	x	x	—

Bit	Symbol	Bit Name	Function	R/W
b6	CM06	CPU clock division select bit 0	0: Bits CM16 and CM17 in CM1 register enabled	R/W

(10) Disable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

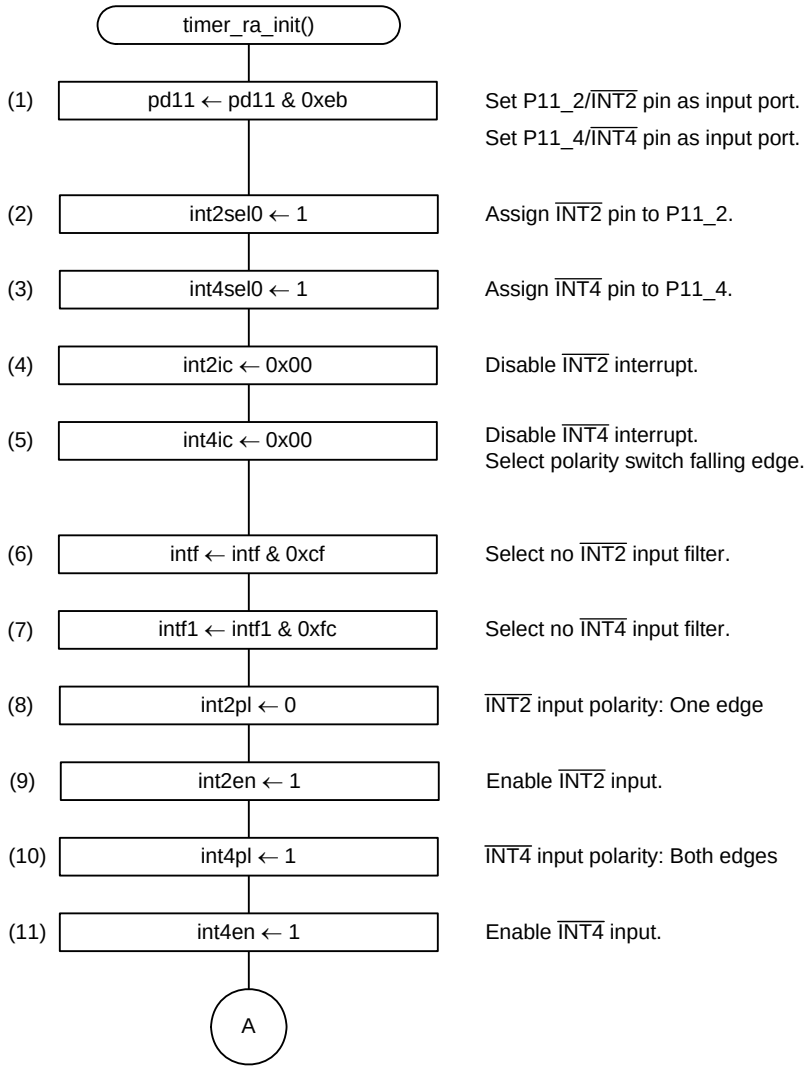
Protect Register (PRCR)

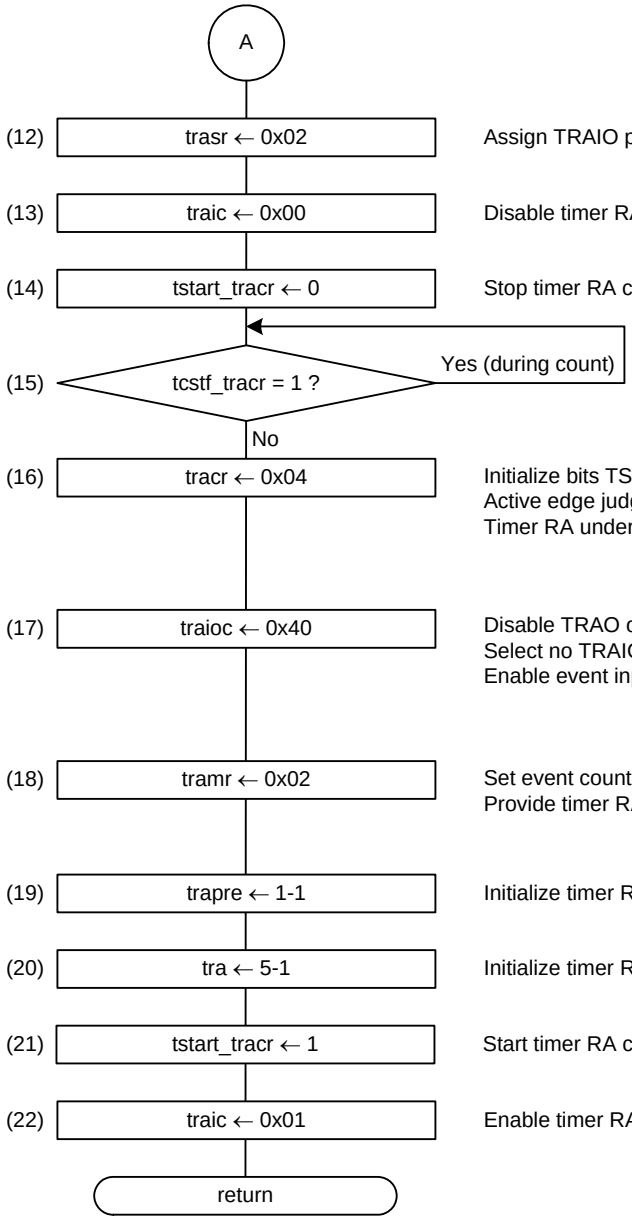
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	—	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 0: Write disabled	R/W

4.4 Timer RA Associated SFR Initial Setting

- Flowchart




A
(12)
trasr ← 0x02
Assign TRAIO pin to INT4.
(13)
traic ← 0x00
Disable timer RA interrupt.
(14)
tstart_tracr ← 0
Stop timer RA count.
(15)
tcstf_tracr = 1 ?
Yes (during count)
No
(16)
tracr ← 0x04
Initialize bits TSTART and TCSTF, and registers TRAPRE and TRA.
Active edge judgment flag: Set it to 0 in event counter mode.
Timer RA underflow flag: Set it to 0 in event counter mode.
(17)
traioc ← 0x40
Disable TRAO output.
Select no TRAIO input filter.
Enable event input for INT2 high-level period.
(18)
tramr ← 0x02
Set event counter mode.
Provide timer RA count source.
(19)
trapre ← 1-1
Initialize timer RA prescaler register.
(20)
tra ← 5-1
Initialize timer RA register.
(21)
tstart_tracr ← 1
Start timer RA count.
(22)
traic ← 0x01
Enable timer RA interrupt.
return

• Register settings

(1) Set P11_2 and P11_4 as input ports.

Port P11 Direction Register (PD11)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	x	0	x	0	x	x

Bit	Symbol	Bit Name	Function	R/W
b2	PD11_2	Port P11_2 direction bit	0: Input mode (functions as an input port)	R/W
b4	PD11_4	Port P11_4 direction bit		R/W

(2) Assign the $\overline{\text{INT2}}$ pin to port P11_2.

INT Interrupt Input Pin Select Register (INTSR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	x		x	1	x	x

Bit	Symbol	Bit Name	Function	R/W
b2	INT2SEL0	$\overline{\text{INT2}}$ pin select bit	1: P11_2 assigned	R/W

(3) Assign the $\overline{\text{INT4}}$ pin to port P11_4.

INT Interrupt Input Pin Select Register (INTSR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	x	1	x		x	x

Bit	Symbol	Bit Name	Function	R/W
b4	INT4SEL0	$\overline{\text{INT4}}$ pin select bit	1: P11_4 assigned	R/W

(4) Set the $\overline{\text{INT2}}$ interrupt control register.

INT2 Interrupt Control Register (INT2IC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	x	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested	R/W

(5) Set the $\overline{\text{INT4}}$ interrupt control register.

INT4 Interrupt Control Register (INT4IC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested	R/W
b4	POL	Polarity switch bit	0: Falling edge selected	R/W

(6) Set no $\overline{\text{INT2}}$ input filter.

INT Input Filter Select Register 0 (INTF)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	0	0	x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b4	INT2F0	$\overline{\text{INT2}}$ input filter select bit	b5 b4 0 0: No filter	R/W
b5	INT2F1			R/W

(7) Set no $\overline{\text{INT4}}$ input filter.

INT Input Filter Select Register 1 (INTF1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	x	x	x	x	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT4F0	$\overline{\text{INT4}}$ input filter select bit	b1 b0 0 0: No filter	R/W
b1	INT4F1			R/W

(8) Set the $\overline{\text{INT2}}$ input polarity to one edge.

External Input Enable Register 0 (INTEN)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	0		x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b5	INT2PL	$\overline{\text{INT2}}$ input polarity select bit	0: One edge	R/W

(9) Set $\overline{INT2}$ input enabled.

External Input Enable Register 0 (INTEN)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x		1	x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b4	INT2EN	$\overline{INT2}$ input enable bit	1: Enabled	R/W

(10) Set the $\overline{INT4}$ input polarity to both edges.

External Input Enable Register 1 (INTEN1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	x	x	x	x	1	

Bit	Symbol	Bit Name	Function	R/W
b1	INT4PL	$\overline{INT4}$ input polarity select bit	1: Both edges	R/W

(11) Set $\overline{INT4}$ input enabled.

External Input Enable Register 1 (INTEN1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	x	x	x	x		1

Bit	Symbol	Bit Name	Function	R/W
b0	INT4EN	$\overline{INT4}$ input enable bit	1: Enabled	R/W

(12) Assign the TRAIO pin to $\overline{INT4}$.

Timer RA Pin Select Register (TRASR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	—	—	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRAIOSEL0	TRAIO pin select bit	b1 b0 1 0: $\overline{INT4}$ assigned	R/W
b1	TRAIOSEL1			R/W

(13) Disable the timer RA interrupt.

Interrupt Control Register (TRAIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested	R/W

(14) Stop the timer RA count.

Timer RA Control Register (TRACR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—			—			0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RA count start bit	0: Count stops	R/W

(15) Wait until the timer RA count stops.

Timer RA Control Register (TRACR)

Bit	Symbol	Bit Name	Function	R/W
b1	TCSTF	Timer RA count status flag	0: Count stops 1: During count operation	R

(16) Set the timer RA control register.

Timer RA Control Register (TRACR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	0	0	—	1	0	

Bit	Symbol	Bit Name	Function	R/W
b1	TCSTF	Timer RA count status flag	0: Count stops	R
b2	TSTOP	Timer RA count forcible stop bit	When this bit is set to 1, the count is forcibly stopped. When read, the content is 0.	R/W
b4	TEDGF	Active edge judgment flag	0: Active edge not received	R/W
b5	TUNDF	Timer RA underflow flag	0: No underflow	R/W

(17) Set the timer RA I/O control register.

Timer RA I/O Control Register (TRAIOC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	1	0	0	0	0	0	x

Bit	Symbol	Bit Name	Function	R/W
b1	TOPCR	TRAIO output control bit	Set to 0 in event counter mode.	R/W
b2	TOENA	TRAO output enable bit	0: Port P11_5	R/W
b3	TIOSEL	Hardware LIN function select bit	Set to 0.	R/W
b4	TIPF0	TRAIO input filter select bit	b5 b4 0 0: No filter	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRAIO event input control bit	b7 b6 0 1: Event input enabled at $\overline{\text{INT2}}$ level	R/W
b7	TIOGT1			R/W

(18) Set the timer RA mode register.

Timer RA Mode Register (TRAMR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	x	x	x	—	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	TMOD0	Timer RA operating mode select bit	b2 b1 b0 0 1 0: Event counter mode	R/W
b1	TMOD1			R/W
b2	TMOD2			R/W
b7	TCKCUT	Timer RA count source cutoff bit	0: Count source provided	R/W

(19) Initialize the timer RA prescaler register to 1-1 (00h).

Timer RA Prescaler Register (TRAPRE)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	0	0	0	0	0

Bit	Mode	Function	Setting Range	R/W
b7 to b0	Event counter mode	Counts an external count source.	00h to FFh	R/W

(20) Initialize the timer RA register to 5-1 (04h).

Timer RA Register (TRA)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	0	0	1	0	0

Bit	Mode	Function	Setting Range	R/W
b7 to b0	All modes	Counts the TRAPRE register underflows.	00h to FFh	R/W

(21) Start the timer RA count.

Timer RA Control Register (TRACR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—			—			1

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RA count start bit	1: Count starts	R/W

(22) Enable the timer RA interrupt.

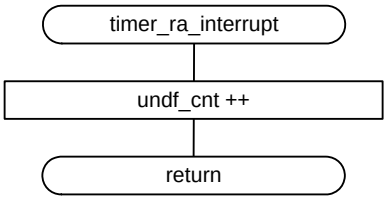
Interrupt Control Register (TRAIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	0	0	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 1: Level 1	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested	R/W

4.5 Timer RA Interrupt Handling

- Flowchart



Update underflow counter.

5. Sample Program

A sample program can be downloaded from the Renesas Electronics website.
To download, click “Application Notes” in the left-hand side menu of the R8C Family page.

6. Reference Documents

R8C/L3AC Group User’s Manual: HardwareRev.0.10
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics website
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Revision History	R8C/L3AC Group Timer RA Event Counter Mode (Counting Both Edges Using Event Input Control)

Rev.	Date	Description	
		Page	Summary
1.10	May 20, 2010	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
7F, No. 363 Fu Shing North Road Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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