R8C/35C Group

DTC Operation in Chain Transfers

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Abstract

This document describes DTC operation in chain transfers with the R8C/35C Group.

Product

R8C/35C Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

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1. Specifications

Perform A/D conversion on an analog input voltage and store the converted results to the internal RAM. Use the DTC chain transfer to transfer the results to the internal RAM.

Table 1.1 lists the Peripheral Functions and Their Applications. Figure 1.1 shows a Data Transfer.

Table 1.1 Peripheral Functions and Their Applications

Peripheral Function	Application
DTC	Transfer A/D converted results to the internal RAM
A/D converter	Convert analog input voltage in single sweep mode

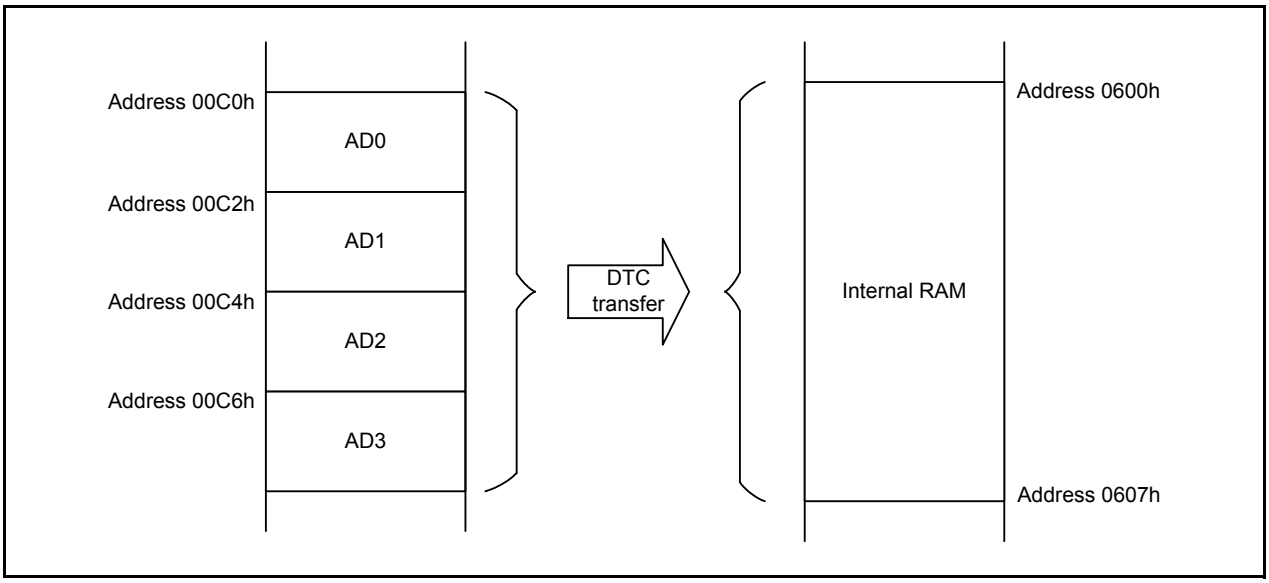

Figure 1.1 Data Transfer

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	R8C/35C Group
Operating frequencies	• High-speed on-chip oscillator clock: 20 MHz (typical) • System clock: 20 MHz • CPU clock: 20 MHz
Operating voltage	5.0 V (2.7 to 5.5 V)
Integrated development environment	Renesas Electronics Corporation High-performance Embedded Workshop Version 4.07
C compiler	Renesas Electronics Corporation M16C Series, R8C Family C Compiler V.5.45 Release 01
	Compile options -D__UART0__ -c -finfo -dir "$(CONFIGDIR)" -R8C (Default setting is used in the integrated development environment.)

3. Hardware

3.1 Pins Used

Table 3.1 lists the Pins Used and Their Functions.

Table 3.1 Pins Used and Their Functions

Pin Name	I/O	Function
P1_0/AN8	Input	Analog input of the A/D converter
P1_1/AN9	Input	Analog input of the A/D converter
P1_2/AN10	Input	Analog input of the A/D converter
P1_3/AN11	Input	Analog input of the A/D converter

4. Software

4.1 Operation Overview

In this sample program, A/D converted values that have been stored to A/D registers (AD0 to AD3) are transferred to the internal RAM using the DTC chain transfer. Using the chain transfer, the DTC can successively read two control data (control data 0 and control data 1) from a single activation source generated when A/D conversion is completed. The DTC transfers A/D converted results of AD0 and AD1 by control data 0, and AD2 and AD3 by control data 1 to the internal RAM. After DTC transfer is completed, perform A/D conversion interrupt handling by a program.

Table 4.1 shows the Setting of the DTC Activation Source.

Table 4.1 Setting of the DTC Activation Source

Activation Source	Register Setting
A/D conversion (source number 9)	Set 0 to DTC control vector 9 (control data 0).

Table 4.2 DTC Settings

Setting Item	Setting Value	
	Control data 0	Control data 1
Transfer mode	Normal mode	Normal mode
Source address control	Fixed	Fixed
Destination address control	Fixed	Fixed
Chain transfer	Enabled	Disabled
Transfer block size	4 bytes	4 bytes
Number of DTC transfers	1	1
Transfer source address	AD0 (addresses 00C0h to 00C1h) AD1 (addresses 00C2h to 00C3h)	AD2 (addresses 00C4h to 00C5h) AD3 (addresses 00C6h to 00C7h)
Transfer destination address	ad_value[0] (addresses 0600h to 0601h) ad_value[1] (addresses 0602h to 0603h)	ad_value[2] (addresses 0604h to 0605h) ad_value[3] (addresses 0606h to 0607h)

(1) Perform an initial setting for the DTC and A/D converter by a program.
(2) Set the DTCEN16 bit in the DTCEN1 register to 1 (DTC activation enabled by the A/D conversion interrupt), and the ADST bit in the ADCON0 register to 1 (A/D conversion starts) by a program.
(3) After A/D conversion is completed, the DTC is activated by an A/D conversion interrupt request.
(4) Once the DTC is activated, it reads control data 0 and transfers values of registers AD0 and AD1 to the internal RAM according to control data 0. Since chain transfer is enabled, the DTC successively reads control data 1.
(5) Once the DTC is activated, it reads control data 1 and transfers values of registers AD2 and AD3 to the internal RAM according to control data 1. Since chain transfer is disabled in control data 1, data transfer by the DTC is completed.
(6) Since the DTC transfer count register value becomes from 01h to 00h, an A/D conversion interrupt is generated after DTC transfer is completed.
(7) In the A/D conversion interrupt handling, read the A/D converted values that have been DTC transferred to the internal RAM to variables an8_value, an9_value, an10_value, and an11_value. Then, set DTC data transfer count register values of both control data 0 and control data 1 to 01h, set the DTCEN16 bit to 1 (DTC activation enabled by the A/D conversion interrupt), and set the ADST bit to 1 (A/D conversion starts). Repeat steps (3) to (7).

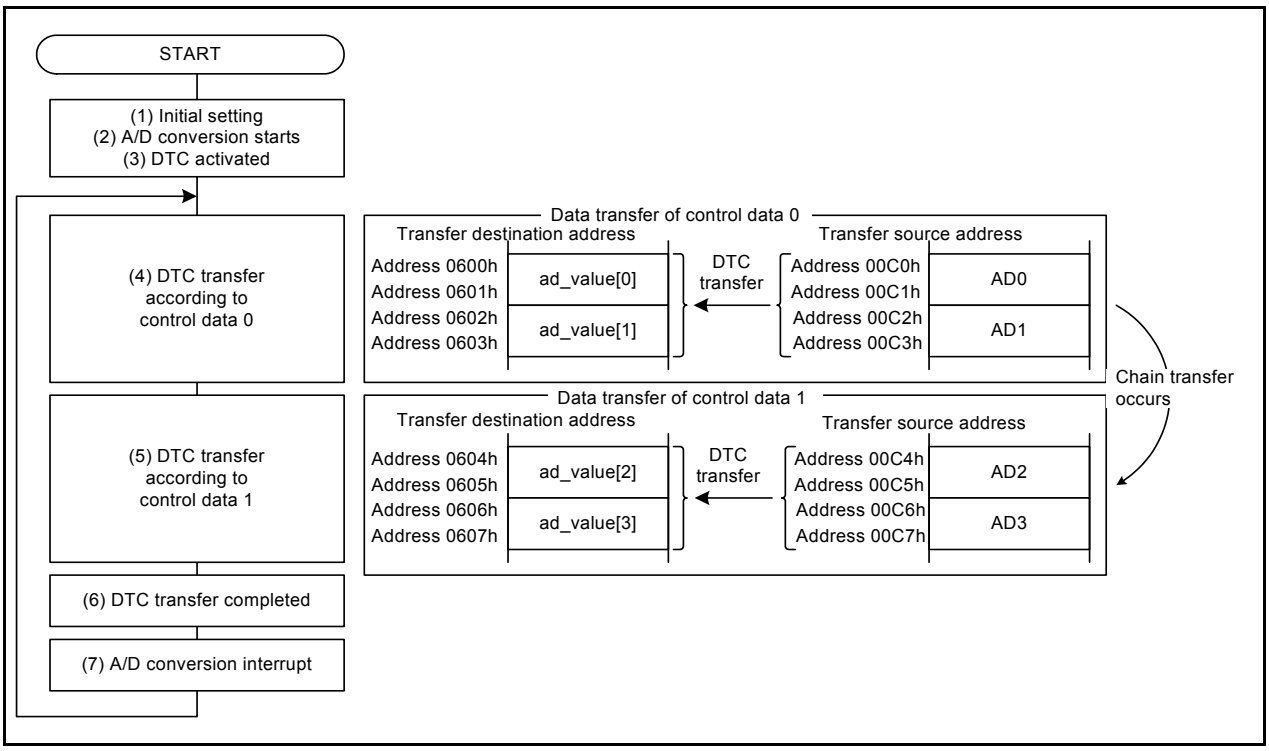

Figure 4.1 Example of Chain Transfer

4.2 Required Memory Size

Table 4.3 lists the Required Memory Size.

Table 4.3 Required Memory Size

Memory Used	Size	Remarks
ROM	291 bytes	In the r01an0372_src.c module
RAM	8 bytes	In the r01an0372_src.c module
Maximum user stack usage	13 bytes	
Maximum interrupt stack usage	18 bytes	

The required memory size varies depending on the C compiler version and compile options.

4.3 Constant

Table 4.4 lists the Constant Used in the Sample Code.

Table 4.4 Constant Used in the Sample Code

Constant Name	Setting Value	Contents
ad_value	00600h	DTC transfer destination address

4.4 Variables

Table 4.5 lists the Global Variables.

Table 4.5 Global Variables

Type	Variable Name	Contents	Function Used
unsigned short	ad_value[4]	A/D converted result storage address of AN8 to AN11	ad_converter_int
unsigned short	an8_value	Store A/D converted result of AN8	ad_converter_int
unsigned short	an9_value	Store A/D converted result of AN9	ad_converter_int
unsigned short	an10_value	Store A/D converted result of AN10	ad_converter_int
unsigned short	an11_value	Store A/D converted result of AN11	ad_converter_int

4.5 Functions

Table 4.6 lists the Functions.

Table 4.6 Functions

Function Name	Outline
mcu_init	System clock setting
ad_converter_enable	Initial setting of A/D converter
dtc_enable	Initial setting of DTC
ad_converter_int	A/D conversion interrupt handling

4.6 Function Specifications

The following tables list the sample code function specifications.

mcu_init	
Outline	System clock setting
Header	None
Declaration	void mcu_init(void)
Description	Set the system clock.
Argument	None
Returned value	None
Remark	—

ad_converter_enable	
Outline	Initial setting of A/D converter
Header	None
Declaration	void ad_converter_enable(void)
Description	Perform initial setting to use the A/D converter in single-sweep mode.
Argument	None
Returned value	None
Remark	—

dtc_enable	
Outline	Initial setting of DTC
Header	None
Declaration	void dtc_enable(void)
Description	Perform an initial setting for chain transfer of the DTC in normal mode.
Argument	None
Returned value	None
Remark	—

ad_converter_int	
Outline	A/D conversioin interrupt handling
Header	None
Declaration	void ad_converter_int(void)
Description	• Perform interrupt handling when A/D conversion is completed. After DTC transfer is completed, activate this interrupt handling. • Set A/D converted values of AN8 to AN11 transferred by the DTC to each variable.
Argument	None
Returned value	None
Remark	—

4.7 Flowcharts

4.7.1 Main Processing

Figure 4.2 shows the Main Processing.

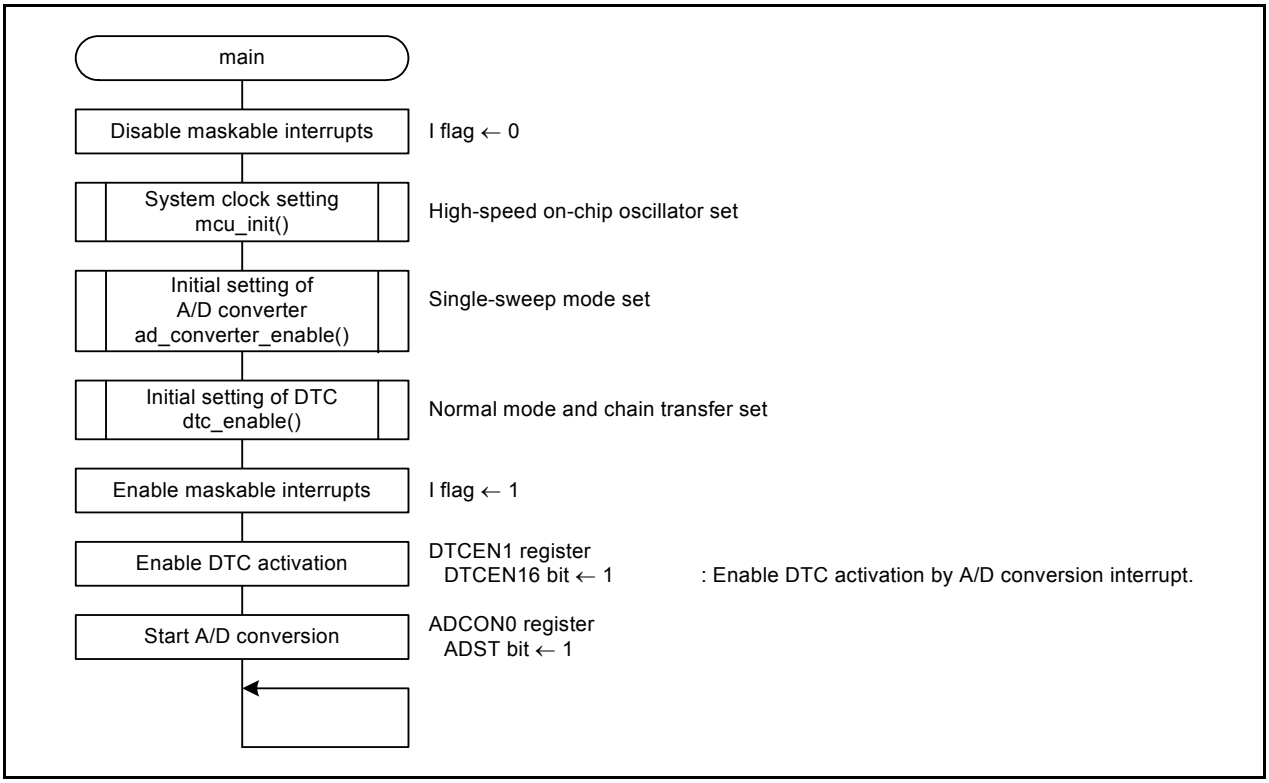

Figure 4.2 Main Processing

4.7.2 System Clock Setting

Figure 4.3 shows the System Clock Setting.

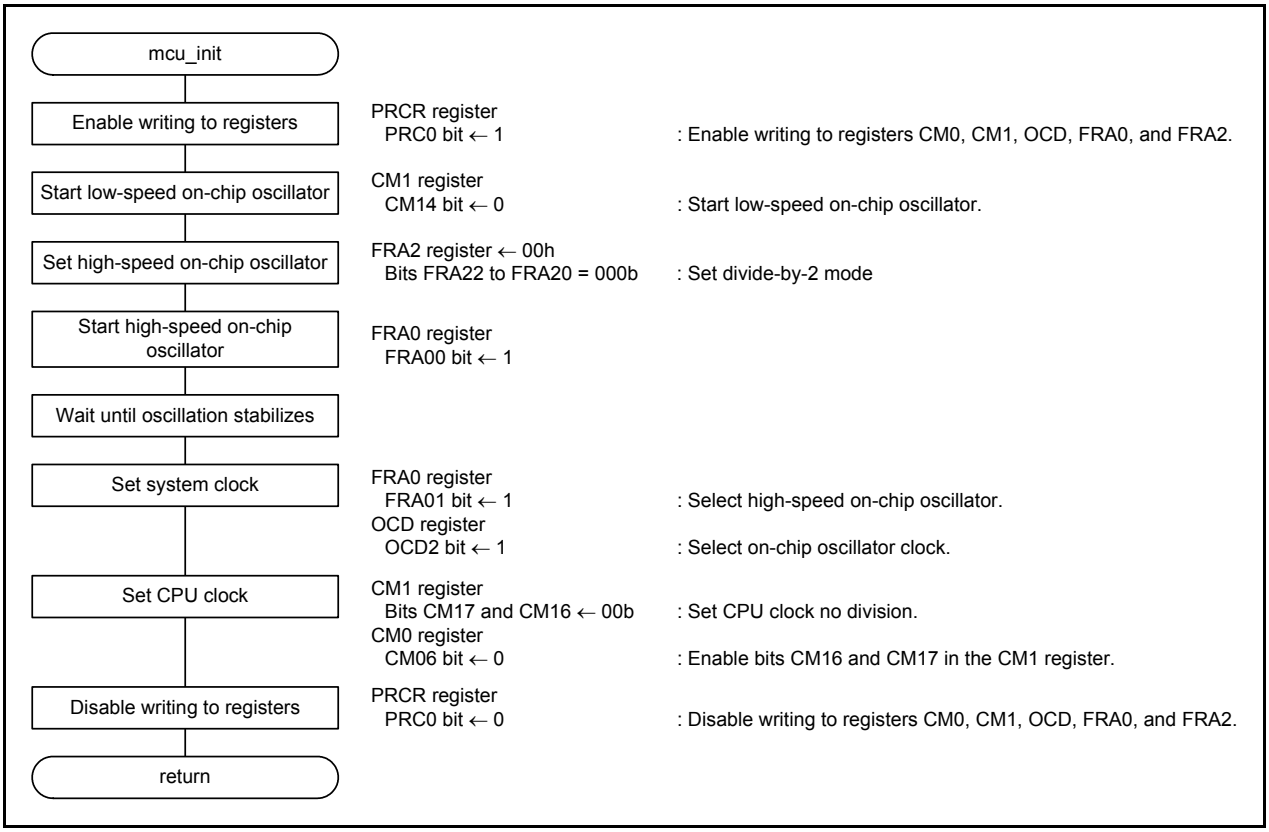

Figure 4.3 System Clock Setting

4.7.3 Initial Setting of the A/D Converter

Figure 4.4 shows the Initial Setting of the A/D Converter.

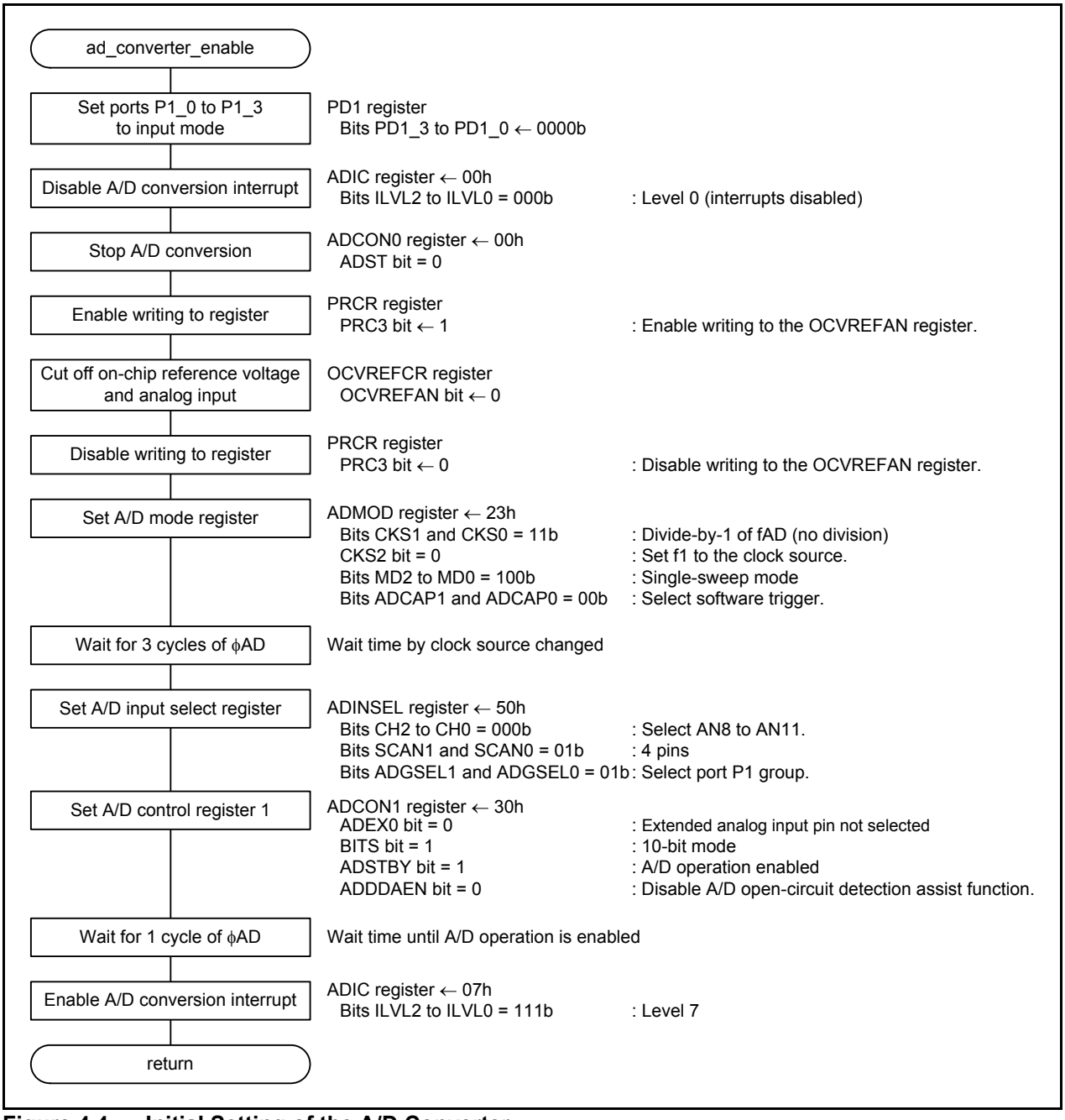

Figure 4.4 Initial Setting of the A/D Converter

4.7.4 Initial Setting of the DTC

Figure 4.5 shows the Initial Setting of the DTC.

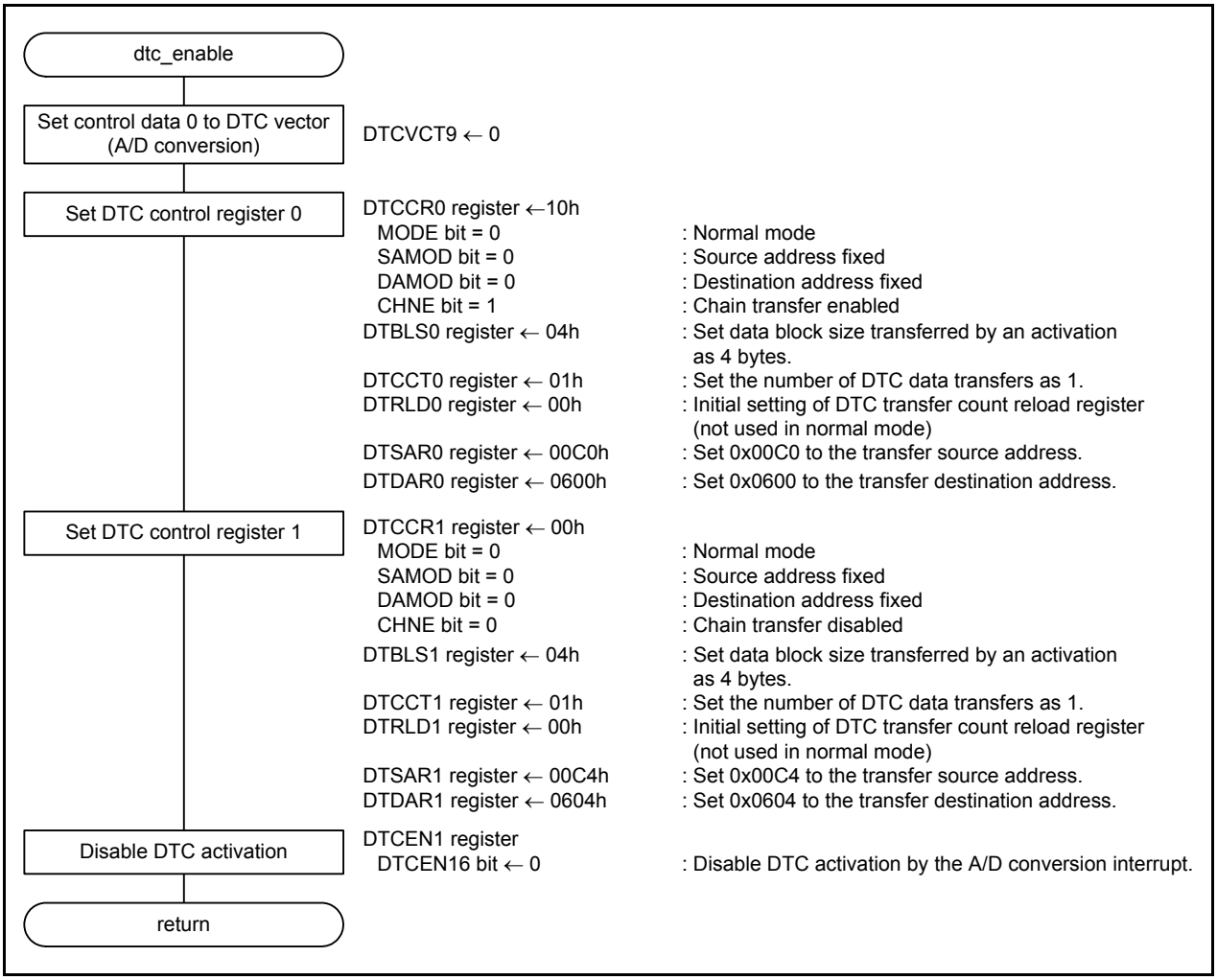

Figure 4.5 Initial Setting of the DTC

4.7.5 A/D Conversion Interrupt Handling

Figure 4.6 shows the A/D Conversion Interrupt Handling.

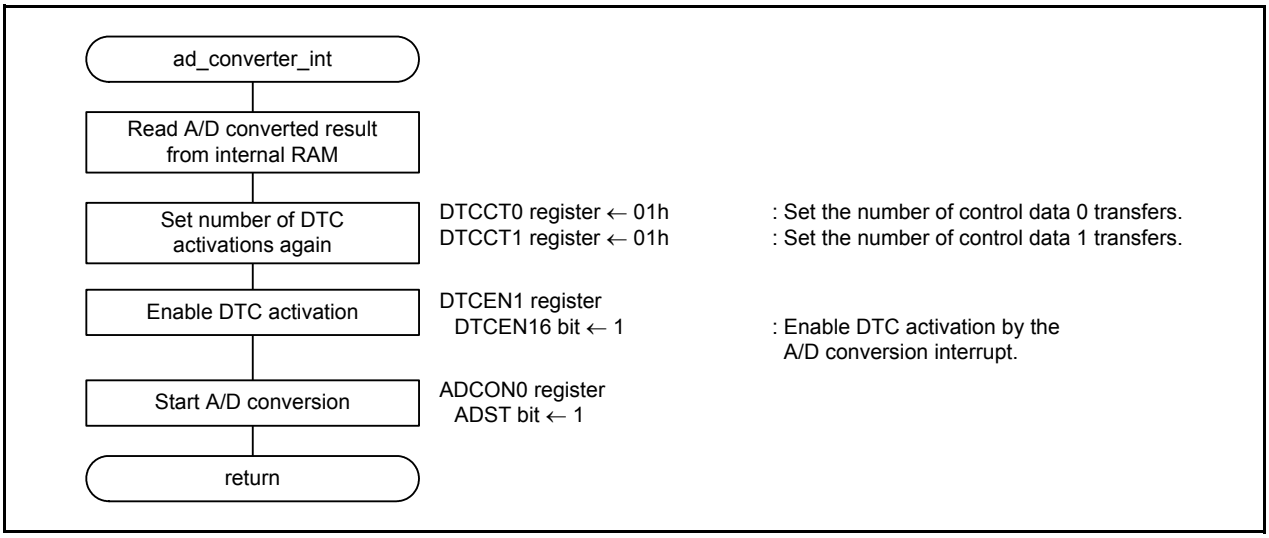

Figure 4.6 A/D Conversion Interrupt Handling

5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

6. Reference Documents

R8C/35C Group User's Manual: Hardware Rev.1.00
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

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Revision History	R8C/35C Group DTC Operation in Chain Transfers

Rev.	Date	Description	
		Page	Summary
1.00	Oct. 4, 2011	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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