R8C/25, R8C/35C Groups

Differences of R8C/25 and R8C/35C Groups

REJ05B1312-0120
Rev.1.20
July 14, 2010

1. Abstract

This document is reference material for identifying differences of the R8C/25 Group and R8C/35C Group.

2. Introduction

This document is applied to the following MCUs:

- Applicable MCU: R8C/25 Group and R8C/35C Group

3. R8C/35C Group Replaces R8C/25 Group

Since the R8C/35C Group is an upward compatible product for the R8C/25 Group, replacing the R8C/25 Group with the R8C/35C Group is easy. For more details, refer to Chapter 4 in this document and to the hardware manual.

3.1 Upward Compatibility of Functions

Additional functions for the R8C/35C Group are shown as follows:

- Add detection level of voltage detection 0 and voltage detection 1 selectable.
- Add DTC (data transfer controller).
- Add the low-speed on-chip oscillator for the watchdog timer.
- Add event input control to timer RA.
- Add timer RC.
- Add A/D trigger generation to modes other than timer RD complementary PWM mode.
- Add one channel of the serial interface (UART2) with clock synchronous serial I/O mode, clock asynchronous serial I/O mode (UART mode), special mode (I^2C mode), and multiprocessor communication function.
- Add bus collision detection to the hardware LIN during Synch Break transmission.
- Add repeat mode 1, single sweep mode, and repeat sweep mode to A/D converter operating mode. Add timer RC and external trigger for the A/D conversion start conditions of repeat mode 0. Add AD1 to AD7 to the storage registers for the A/D conversion results.
- Add the D/A converter.
- Add the comparator B.
- Add the data protect function and BGO (BackGroud Operation) function to flash memory. Add two blocks of data flash.

4. Group Differences

4.1 Function and Specification Differences

Table 4.1 and Table 4.6 list differences in the functions and specifications. Refer to 4.2 Pin Function Differences.

Table 4.1 Function and Specification Differences (1) (1)

Item		R8C/25 Group	R8C/35C Group
Flash memory	ROM/RAM	• 16 KB/1 KB • 24 KB/2 KB • 32 KB/2 KB • 48 KB/2.5 KB • 64 KB/3 KB	• 16 KB/1.5 KB • 24 KB/2 KB • 32 KB/2.5 KB • 48 KB/4 KB • 64 KB/6 KB • 96 KB/8 KB • 128 KB/10KB
Reset		• Reset source determination function: Not included • CPU clock after reset: low-speed on-chip oscillator divided by 8 • Flash memory start time of reset sequence: 14 cycles of CPU clock (CPU clock is the low-speed on-chip oscillator divided by 8.)	• Reset source determination function: Included • CPU clock after reset: low-speed on-chip oscillator no division • Flash memory start time of reset sequence: 148 cycles of CPU clock (CPU clock is the low-speed on-chip oscillator no division)
Voltage detection circuits	Voltage detection 0	• Detection voltage cannot be selected. • Digital filter function: Included (selectable if the digital filter is included or not.)	• Detection voltage can be selected (four levels). • Digital filter function: Not included
	Voltage detection 1	• Detection voltage cannot be selected. • Detection edge cannot be selected. • Digital filter sampling time: (fOCO-S divided by n) x 4 n: 1, 2, 4, 8 • Voltage monitor 1 reset: Included • Voltage monitor 1 interrupt: Included (non-maskable interrupt fixed)	• Detection voltage can be selected (16 levels). • Detection edge can be selected (one edge or both edges). • Digital filter sampling time: (fOCO-S divided by n) x 2 n: 1, 2, 4, 8 • Voltage monitor 1 reset: Not included • Voltage monitor 1 interrupt: Included (non-maskable interrupt or maskable interrupt can be selected.)
	Voltage detection 2	• Detection edge cannot be selected. • Digital filter sampling time: (fOCO-S divided by n) x 4 n: 1, 2, 4, 8 • Voltage monitor 2 reset: Included • Voltage monitor 2 interrupt: Included (non-maskable interrupt fixed)	• Detection edge can be selected (one edge or both edges). • Digital filter sampling time: (fOCO-S divided by n) x 2 n: 1, 2, 4, 8 • Voltage monitor 2 reset: Not included • Voltage monitor 2 interrupt: Included (non-maskable interrupt or maskable interrupt can be selected.)

Note:
1. Refer to the hardware manual for details and electrical characteristics.

Table 4.2 Function and Specification Differences (2) (1)

Item	R8C/25 Group	R8C/35C Group
I/O ports	• I/O ports: 41 • Input ports: 3 • Input threshold value cannot be selected. • Drive capacity can be controlled (only for port P2). • Ports for LED drive: 8	• I/O ports: 47 • Input ports: 1 • Input threshold value can be selected. • Drive capacity can be controlled. • High current drive ports: 47
Clock generation circuits	• Wait control bit (CM30): Not included • External clock is input from the XIN pin. • CPU clock when exitting wait mode or stop mode cannot be selected. • Clock source for fOCO128 depends on the FRA01 bit. • fC cannot be selected for the system clock. • fC cannot be selected for the peripheral function clock. • Low-speed on-chip oscillator for watchdog timer: Not included • XIN-XOUT drive capacity can be selected. • XCIN-XCOUT drive capacity can be selected.	• Wait control bit (CM30): Included • External clock is input from the XOUT pin. • CPU clock when exitting wait mode or stop mode can be selected. • Clock source for fOCO128 depends on the FRA03 bit. • fC can be selected for the system clock. • fC can be selected for the peripheral function clock. • Low-speed on-chip oscillator for watchdog timer: Included • XIN-XOUT drive capacity cannot be selected. • XCIN-XCOUT drive capacity cannot be selected.
High-speed on-chip oscillator	• No correction value for 32 MHz • Frequency correction data every supply voltage range: Necessary	• Correction value for 32 MHz • Frequency correction data every supply voltage range: Not necessary
Interrupts	• Interrupt sources: 26 • External interrupt inputs: 8 ($\overline{\text{INT}}$ x 4, key input x 4)	• Interrupt sources: 36 • External interrupt inputs: 9 ($\overline{\text{INT}}$ x 5, key input x 4)
Watchdog timer	• Underflow period cannot be selected. • Refresh acknowledgement period cannot be selected. • 15 bits x 1 channel	• Underflow period can be selected (four steps). • Refresh acknowledgement period can be selected (four steps). • 14 bits x 1 channel
DTC (data transfer control)	Not included	Included

Note:
1. Refer to the hardware manual for details and electrical characteristics.

Table 4.3 Function and Specification Differences (3) (1)

Item		R8C/25 Group	R8C/35C Group
Timer RA	Count source	fC cannot be selected.	fC can be selected.
	–	Event input control function: Not included	Event input control function: Included
Timer RC		Not included	Included
Timer RD	Count source	• fOCO-F cannot be selected. • fC2 cannot be selected.	• fOCO-F can be selected. • fC2 can be selected.
	–	Module operation enable bit (MSTTRD bit): Not included	Module operation enable bit (MSTTRD bit): Included
	Output compare function	A/D trigger is not generated.	A/D trigger generation can be selected.
	PWM mode	A/D trigger is not generated.	A/D trigger generation can be selected.
	Reset synchronous PWM mode	A/D trigger is not generated.	A/D trigger generation can be selected.
	PWM3 mode	A/D trigger is not generated.	A/D trigger generation can be selected.
Timer RE (real-time clock mode)	TREO pin output function	Either f2, f4, or f8 is output	Either f2, f4, f8, fC, or 1 Hz is output
Timer RE (output compare mode)	TREO pin output function	Either f2, f4, f8, or compare output is output	Either f2, f4, f8, fC, or compare output is output
Serial interface (UART0)	Count source	fC cannot be selected.	fC can be selected.
Serial interface (UART1)	Count source	fC cannot be selected.	fC can be selected.
Serial interface (UART2)		Not included	Included
Clock synchronous serial interface (synchronous serial communication unit)		• Module operation enable bit (MSTIIC bit): Not included • Transfer data length: 8 bits fixed • Transmit/receive data register length: 8 bits	• Module operation enable bit (MSTIIC bit): Included • Transfer data length: 8 bits to 16 bits can be selected. • Transmit/receive data register length: 16 bits
Clock synchronous serial interface (I^2C bus interface) (2)		• Module operation enable bit (MSTIIC bit): Not included • Transfer rate double or half cannot be selected. • SDA digital delay: Not included	• Module operation enable bit (MSTIIC bit): Included • Transfer rate double or half can be selected. • SDA digital delay: Included (three steps)

Notes:
1. Refer to the hardware manual for details and electrical characteristics.
2. I^2C bus is a trademark of Koninklijke Philips Electronics N. V.

Table 4.4 Function and Specification Differences (4) (1)

Item		R8C/25 Group	R8C/35C Group
Hardware LIN		Bus collision during Sync Break transmission cannot be detected.	Bus collision during Sync Break transmission can be detected. (Enable/ disable can be switched.)
A/D converter	Operating mode	• One-shot mode • Repeat mode	• One-shot mode • Repeat mode 0 • Repeat mode 1 • Single sweep mode • Repeat sweep mode
	A/D conversion start condition	• Software trigger • Timer RD	• Software trigger • Timer RC • Timer RD • External trigger
	Storage register for A/D conversion result	One register	Eight registers
	Operating clock (ϕAD)	• f1, f2, f4, and fOCO-F • Maximum 10 MHz	• fAD, fAD divided by 2, fAD divided by 4, fAD divided by 8 (fAD = f1 or fOCO-F) • Maximum 20 MHz
	Conversion rate (2)	33 ϕAD cycles	Minimum 44 ϕAD cycles
	Other functions	• Sample and hold function included or not included: Can be selected • On-chip reference voltage: Not included • A/D open-circuit detection assist function: Not included	• Sample and hold function included: Fixed • On-chip reference voltage: Included (3) • A/D open-circuit detection assist function: Included
D/A converter		Not included	Included
Comparator B		Not included	Included

Notes:
1. Refer to the hardware manual for details and electrical characteristics.
2. Conversion rate is for one-shot mode, 10-bit resolution, and the sample and hold function
3. Any variation in VREF can be confirmed using the on-chip reference voltage.

Table 4.5 Function and Specification Differences (5) (1)

Item	R8C/25 Group	R8C/35C Group
Flash memory	• Size 8 KB/16 KB/32 KB per one block of program ROM • Data flash area: 1 KB x 2 blocks • Data protect function: Not included • BGO function: Not included • Erase/write error: Interrupts not included • Flash access error: Interrupts not included • Flash ready status: Interrupts not included • Areas in which a rewrite control program can be executed in EW0 mode: Transfer to any area other than the flash memory before executing. • Mode after program or erase in EW0 mode: Read status register mode • Rewrite control for program ROM area: Each block can be controlled by the blocks 0/block 1 rewrite disable bit (FMR15 and FMR16) • Rewrite control for data flash area: Each block cannot be controlled. • CPU clock limit of EW0 mode: 5 MHz or below • Program suspend function: Included • Read status register command: Included • Lock bit program command: Not included • Read lock bit status command: Not included • Block blank check command: Not included	• Size 4 KB/8 KB/16 KB/32 KB per one block of program ROM • Data flash area: 1 KB x 4 blocks • Data protect function: Included • BGO function: Included • Erase/write error: Interrupts included • Flash access error: Interrupts included • Flash ready status: Interrupts included • Areas in which a rewrite control program can be executed in EW0 mode: The program can be executed in the program ROM area when rewriting the data flash area. • Modes after program or erase in EW0 mode: Read array mode • Rewrite control for program ROM area: Each block can be controlled by the lock bit disable select bit (FMR13) and software command. • Rewrite control for data flash area: Each block can be controlled by the data flash block A, block B, block C, block D rewrite disable bit (FMR14, FMR15, FMR16, FMR17). • CPU clock limit of EW0 mode: 20 MHz or below • Program suspend function: Not included • Read status register command: Not included • Lock bit program command: Included • Read lock bit status command: Included • Block blank check command: Included

Note:
1. Refer to the hardware manual for details and electrical characteristics.

Table 4.6 Function and Specification Differences (6) (1)

Item	R8C/25 Group	R8C/35C Group
Supply voltage	• VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz) • VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz) • VCC = 2.2 to 5.5 V (f(XIN) = 5 MHz)	• VCC = 2.7 to 5.5 V (f(XIN) = 20 MHz) • VCC = 1.8 to 5.5 V (f(XIN) = 5 MHz)
Low current consumption	• Typical 10 mA (VCC = 5 V, f(XIN) = 20 MHz) • Typical 6 mA (VCC = 3 V, f(XIN) = 10 MHz) • Typical 2.0 μA (VCC = 3 V, wait mode) (f(XCIN) = 32 kHz) • Typical 0.7 μA (VCC = 3 V, stop mode)	• Typical 6.5 mA (VCC = 5 V, f(XIN) = 20 MHz) • Typical 3.5 mA (VCC = 3 V, f(XIN) = 10 MHz) • Typical 3.5 μA (VCC = 3 V, wait mode) (f(XCIN) = 32 kHz) • Typical 2.0 μA (VCC = 3 V, stop mode)
Package	• 52-pin molded-plastic LQFP • 64-pin molded-plastic FLGA	• 52-pin LQFP

Note:
1. Refer to the hardware manual for details and electrical characteristics.

4.2 Pin Function Differences

Table 4.7 to Table 4.8 list the pin function differences.

Table 4.7 Pin Function Differences (1)

Pin Name	R8C/25 Group	R8C/35C Group
$\overline{\text{INT1}}$	P1_7,P1_5	P3_6,P3_2,P2_0,P1_7,P1_5
$\overline{\text{INT2}}$	P6_6	P6_6,P3_2
$\overline{\text{INT3}}$	P6_7	P6_7,P3_3
$\overline{\text{INT4}}$	–	P6_5
TRAIO	P1_7,P1_5	P3_2,P1_7,P1_5
TRAO	P3_0	P5_6,P3_0,P3_7
TRBO	P3_1	P3_1,P1_3
TRCCLK	–	P3_3,P1_4
TRCIOA	–	P1_1,P0_2,P0_1,P0_0
TRCIOB	–	P6_5,P2_0,P1_2,P0_5,P0_4,P0_3
TRCIOC	–	P6_6,P3_4,P2_1,P1_3,P0_7
TRCIOD	–	P6_7,P3_5,P2_2,P1_0,P0_6
TRCTRG	–	P1_1,P0_2,P0_1,P0_0
TRDIOB0	P2_1	P2_2
TRDIOC0	P2_2	P2_1
TREO	P6_0	P6_0,P0_4
CLK1	P6_5	P6_5,P6_2,P0_3
RXD1	P6_7	P6_4,P0_2
TXD1	P6_6	P6_3,P0_1
CLK2	–	P6_5,P3_5
RXD2	–	P4_5,P3_7,P3_4
TXD2	–	P6_6,P3_7,P3_4
$\overline{\text{CTS2}}$	–	P3_3
$\overline{\text{RTS2}}$	–	P3_3
SDA	P3_4	P3_7
SCL2	–	P4_5,P3_7,P3_4
SDA2	–	P6_6,P3_7,P3_4
SSI	P3_3	P3_4
$\overline{\text{SCS}}$	P3_4	P3_3

Table 4.8 Pin Function Differences (2)

Pin Name	R8C/25 Group	R8C/35C Group
$\overline{\text{ADTRG}}$	–	P4_5
DA0	–	P0_6
DA1	–	P0_7
IVCMP1	–	P1_7
IVCMP3	–	P3_3
IVREF1	–	P1_6
IVREF3	–	P3_4

4.3 SFR Differences

Table 4.9 to Table 4.13 list the differences in the SFRs.

Table 4.9 SFR Differences (1)

R8C/25 Group	R8C/35C Group	Remarks
–	RSTFR	
–	CMPA	
–	VCAC	
VCA1	VCA1	Allocation addresses are different.
VCA2	VCA2	Allocation addresses are different.
–	VD1LS	
VW0C	VW0C	• Reset values are different. • Bits 1, 4 to 7 deleted.
VW1C	VW1C	• Reset values are different. • Bit 6 deleted. • Allocation addresses are different.
VW2C	VW2C	• Reset values are different. • Bit 6 deleted. • Allocation addresses are different.
P3	P3	Bits 2 and 6 added.
PD3	PD3	Bits 2 and 6 added
PD4	PD4	Bits 6 and 7 added
–	P5	
–	PD5	
PMR	–	• Bit 4 moved to bits 0 to 5 in U1SR and functions changed. • Bit 7 moved to bit 0 in SSUIICSR.
–	TRASR	
–	TRBRCSR	
–	TRCPSR0	
–	TRCPSR1	
–	TRDPSR0	
–	TRDPSR1	
–	TIMSR	
–	U0SR	
U1SR	U1SR	Allocation addresses and functions are different.
–	U2SR0	
–	U2SR1	
–	SSUIICSR	
–	INTSR	
–	PINSR	
PUR0	PUR0	Bits 6 and 7 functions changed and allocation addresses are different.
PUR1	PUR1	• Reset values are different. • Bit 1 functions changed. • Allocation addresses are different

Table 4.10 SFR Differences (2)

R8C/25 Group	R8C/35C Group	Remarks
–	P1DRR	
P2DRR	P2DRR	Allocation addresses are different.
–	DRR0	
–	DRR1	
–	VLT0	
–	VLT1	
CM0	CM0	• Reset values are different. • Bits 3 and 7 functions changed.
CM1	CM1	Bit 5 added.
–	CM3	
FRA0	FRA0	Bit 3 added.
–	FRA3	
FRA4	FRA4	Functions are different.
–	FRA5	
FRA6	FRA6	Functions are different.
FRA7	FRA7	Functions and allocation addresses are different.
PRCR	PRCR	Bits 0 and 3 functions changed.
–	FMRDYIC	
–	TRCIC	
–	S2TIC	
–	S2RIC	
–	U2BCNIC	
–	VCMP1IC	
–	VCMP2IC	
–	INT4IC	
INTEN	INTEN	Allocation addresses are different.
–	INTEN1	
INTF	INTF	Allocation addresses are different.
–	INTF1	
KIEN	KIEN	Allocation addresses are different.
AIER	AIER0	• Register name changed and allocation addresses are different. • Bit 1 functions moved to bit 0 in AIER1.
–	AIER1	
RMAD0	RMAD0	Allocation addresses are different and reset values are different.
RMAD1	RMAD1	Allocation addresses are different and reset values are different.
WDC	WDTC	• Reset values are different. • Register name changed and bit 5 added.

Table 4.11 SFR Differences (3)

R8C/25 Group	R8C/35C Group	Remarks
–	DTCTL	
–	DTCEN0	
–	DTCEN1	
–	DTCEN2	
–	DTCEN3	
–	DTCEN5	
–	DTCEN6	
–	DTCD0	
–	DTCD1	
–	DTCD2	
–	DTCD3	
–	DTCD4	
–	DTCD5	
–	DTCD6	
–	DTCD7	
–	DTCD8	
–	DTCD9	
–	DTCD10	
–	DTCD11	
–	DTCD12	
–	DTCD13	
–	DTCD14	
–	DTCD15	
–	DTCD16	
–	DTCD17	
–	DTCD18	
–	DTCD19	
–	DTCD20	
–	DTCD21	
–	DTCD22	
–	DTCD23	
TRAIOC	TRAIOC	• Bit 3 functions changed. • Bit 3 functions moved to bits 0 and 1in TRASR, and bits 1 to 3 in INTSR. • Bits 6 and 7 added.
TRAMR	TRAMR	Functions added to bits 4 to 6.
–	MSTCR	
–	TRCMR	
–	TRCCR1	
–	TRCIER	
–	TRCIOR0	
–	TRCIOR1	
–	TRC	
–	TRCGRA	
–	TRCGRB	
–	TRCGRC	
–	TRCGRD	
–	TRCCR2	

Table 4.12 SFR Differences (4)

R8C/25 Group	R8C/35C Group	Remarks
–	TRCDF	
–	TRCOER	
–	TRCADCR	
–	TRDECR	
TRDCR0	TRDCR0	Bits 0 to 2 functions added.
TRDCR1	TRDCR1	Bits 0 to 2 functions added.
TRECSR	TRECSR	Bit 4 added and bits 5 and 6 functions added.
U0C01	U0C1	Bits 0 and 1 functions added.
U1MR	U1MR	Allocation addresses are different.
U1BRG	U1BRG	Allocation addresses are different.
U1TB	U1TB	Allocation addresses are different.
U1C0	U1C0	Allocation addresses are different and bits 0 and 1 functions added.
U1C1	U1C1	Allocation addresses are different.
U1RB	U1RB	Allocation addresses are different.
–	U2MR	
–	U2BRG	
–	U2TB	
–	U2C0	
–	U2C1	
–	U2RB	
–	URXDF	
–	U2SMR	
–	U2SMR2	
–	U2SMR3	
–	U2SMR4	
–	U2SMR5	
–	SSBR	
SSTDR/ICDRT	SSTDR/ICDRT	SSTDR register sizes and allocation addresses are different.
–	SSTDRH	
SSRDR/ICDRR	SSRDR/ICDRR	SSRDR register sizes and allocation addresses are different.
–	SSRDRH	
SSCRH/ICCR1	SSCRH/ICCR1	Allocation addresses are different.
SSCRL/ICCR2	SSCRL/ICCR2	Allocation addresses are different.
SSMR/ICMR	SSMR/ICMR	• Reset values are different. • Allocation addresses are different and bit 3 added (SSMR only).
SSMR2/SAR	SSMR2/SAR	Allocation addresses are different.
SSER/ICIER	SSER/ICIER	Allocation addresses are different.
SSSR/ICSR	SSSR/ICSR	Allocation addresses are different.
–	LINCR2	

Table 4.13 SFR Differences (5)

R8C/25 Group	R8C/35C Group	Remarks
–	OCVREFCR	
AD	AD0	Register name changed.
–	AD1	
–	AD2	
–	AD3	
–	AD4	
–	AD5	
–	AD6	
–	AD7	
–	ADMOD	
–	ADINSEL	
ADCON0	ADCON0	• Bits 0 to 2 functions moved to bits 0 to 2 in ADINSEL. • Bit 3 functions moved to bits 3 to 5 in ADMOD and functions added. • Bit 4 functions moved to bits 6 and 7 in ADINSEL and functions added. • Bit 6 functions moved to bit 0. • Bit 7 fucntions moved to bits 0 to 2 in ADMOD and functions added.
ADCON1	ADCON1	• Bit 0 added. • Bit 3 functions moved to bit 4. • Bit 4 functions moved to bits 0 to 2 in ADMOD and functions added. • Bit 5 symbol name changed. • Bits 6 and 7 added.
ADCON2	–	
–	DA0	
–	DA1	
–	DACON	
–	INTCMP	
–	FST	
FMR0	FMR0	• Reset values are different. • Bit 0 functions moved to bit 7 in FST. • Bit 2 functions changed. • Bits 4 and 5 added. • Bit 6 functions moved to bit 4 in FST. • Bit 6 functions chagned. • Bit 7 functions moved to bit 5 in FST. • Bit 7 functions changed. • Allocation addresses are different.
FMR1	FMR1	• Bit 1 functions moved to bit 2 in FMR0. • Bits 3, 4, and 7 added. • Bits 5 and 6 functions changed.
FMR4	FMR2	• Bits 0 and 2 functions changed. • Bits 3, 4, and 6 deleted.

Table 4.14 Option Function Select Area Differences (1)

R8C/25 Group	R8C/35C Group	Remarks
OFS	OFS	• Bits 4 added and bit 5 functions changed. • Bits 5 functions moved to bit 6.
–	OFS2	

Note:
1. The option function select area is allocated in the flash memory, not in the SFRs.

4.4 Interrupt Vector Differences

Table 4.15 lists the differences in the relocatable vector table.

Table 4.15 Relocatable Vector Table Differences

Software Interrupt Number	R8C/25 Group Interrupt Source	R8C/35C Group Interrupt Source
1	–	Flash memory ready
2	–	$\overline{\text{INT4}}$
11	–	UART2 transmit/NACK2
12	–	UART2 receive/ACK2
30	–	UART2 bus collision detection
50	–	Voltage monitor 1
51	–	Voltage monitor 2

5. Reference Document

R8C/25 Group Hardware Manual Rev.3.00
R8C/35C Group Hardware Manual Rev.0.10
(Use the most recent version of the document on the Renesas Electronics website.)

Technical News/Technical Update
(Use the most recent version of the document on the Renesas Electronics website.)

Website and Support

Renesas Electronics website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry

REVISION HISTORY	R8C/25, R8C/35C Groups Differences of R8C/25 and R8C/35C Groups

Rev.	Date	Description	
		Page	Summary
1.00	Oct 27, 2009	–	First Edition issued
1.10	June 24, 2010	3	Number of interrupt sources changed
1.20	July 14, 2010	5	A/D conversion rate for R8C/35C Group changed

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

Notice

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